

Layout Considerations and Thermal Analysis of a 1.8 MHz Resonant VRM

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Abstract - Practical realization of modern high current and high switching frequency converters (with strong skin and proximity effects) requires a good control on layout-dependent parasitic components and on the power losses (thermal management), in order to meet the goal of high efficiency and reliability. In this paper, the physical realization of a VRM rated at 1.3 V - 50 A and switching at 1.8 MHz is analyzed in detail and discussed. Three prototypes, with same layout but different PCB structures and SR MOSFETs, have been tested. Moreover, an accurate thermal model was developed and experimentally validated in order to predict the maximum temperature of critical components.

I. INTRODUCTION

High frequency dc-dc converters for Voltage Regulator Module (VRM) applications require a great attention on the physical realization, in order to have a good control on layout-dependent parasitic components and on the power losses (thermal management). In fact, the combination of low voltage, high current at the output side and high switching frequency (strong skin and proximity effects), makes the goal of high efficiency and reliability a great challenge.

The aim of this paper is to analyze and discuss the physical realization of the 1.8 MHz VRM described in [1], by investigating both layout and thermal issues. It will be shown that component placement and routing have a strong impact not only on parasitic components, but also on the overall converter efficiency, thus affecting the thermal management. Three prototypes, with same layout but different PCB structures and SR MOSFETs (IRF7836 from International Rectifier and STS12NH3LL from STMicroelectronics), have been tested. Moreover, an accurate thermal model was developed in order to predict the maximum temperature of critical components.

In section II a brief review of the converter operation is given, while in section III the parasitic components are analyzed through discussion of different layout choices. Section IV reports an analysis of the converter losses distribution through suitable measurements. Section V reports the developed thermal model and its simulations, while section VI shows the results of thermal measurement of the PCB structures.

II. CONVERTER DESCRIPTION

The scheme of the 1.8 MHz resonant VRM described in [1] and its main waveforms are shown in Fig. 1, while table I reports specifications and main component values. As we can see, the primary switches operate with 50% duty-cycle supplying a fixed-frequency, fixed-amplitude, square-wave voltage to the converter. When the synchronous rectifier (SR) switches Q_1 and Q_2 are both conducting, the transformer secondary winding is short circuited so that the current i_R in the resonant inductor L_R has a pure triangular waveform. Then, switches Q_1 and Q_2 are alternatively turned off for a fixed amount of time, thus allowing the resonance between L_R and C_1 (C_2) to occur. The amplitude of the resonant voltages V_{C1} and V_{C2} is controlled by changing the delay of the SR turn off interval as respect to the primary switch drive signal, while the mean value of the voltage across the resonant capacitors is equal to the output voltage. From [1], the voltage conversion ratio is given by:

$$M = \frac{V_o}{V_s} = \frac{f_{sw}}{f_0} \frac{1}{\pi} \left(\frac{\pi}{2} + a \tan \left(\frac{V_s}{Z_c \Delta I} \right) + \frac{Z_c \Delta I}{V_s} \right) \quad (1)$$

where $Z_c = \sqrt{\frac{L_R}{N^2 C}}$ is the characteristic impedance,

$f_0 = \frac{1}{T_0} = \frac{N}{2\pi\sqrt{L_R C}}$ is the resonant frequency and

$V_s = V_{IN}/2N$. The quantity ΔI in (1) is defined as:

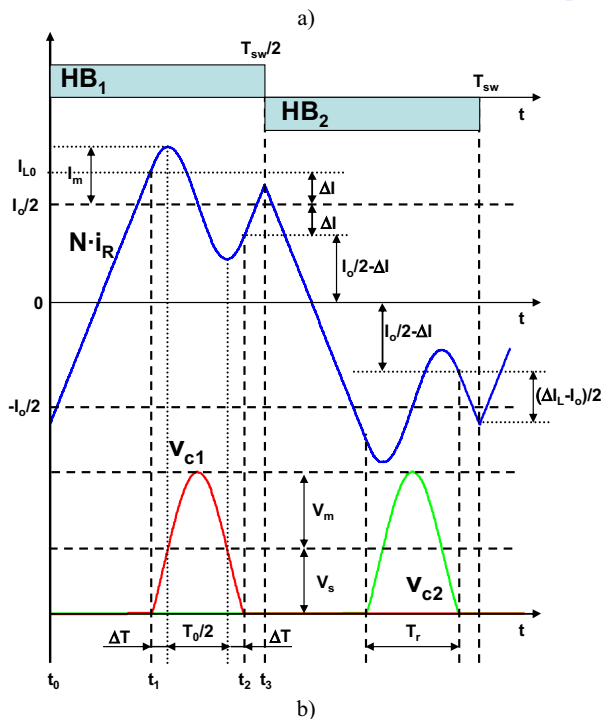
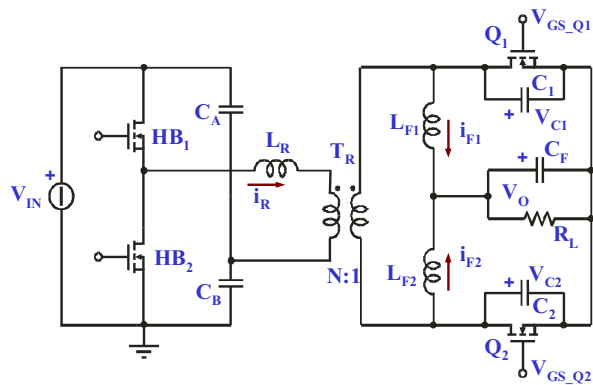
$$\Delta I = I_{L0} - \frac{I_o}{2}$$

where I_{L0} is the value of the resonant current reflected to the transformer secondary side at the SR's turn off instant, while I_o is the load current. From (1), it is possible to see that, in order to maintain the same voltage conversion ratio when the load is varying, it is sufficient to keep ΔI constant, by controlling the delay between the primary switch driving signal and the SR turn off instants.

For further details on the converter behavior and on the design criteria the interested reader should refer to the original paper [1]. Here, what we want to discuss, are some issues related to the physical realization of the converter prototype mainly related to the control of the parasitic components and to the thermal management. Moreover, no

TABLE I. CONVERTER SPECIFICATIONS AND COMPONENT VALUES

$V_{in} = 48 \text{ V} \pm 10\%$	$V_o = 1.3 \text{ V}$	$I_o = 50 \text{ A}$
$N = 5$	$L_R = 390 \text{ nH}$	$L_F = 100 \text{ nH}$
$C_1 = C_2 = 4 \times 10 \text{ nF} + 2 \times 4.7 \text{ nF}$	$C_F = 16 \times 10 \text{ }\mu\text{F}$	$C_A = C_B = 2 \times 470 \text{ nF}$

Figure 1. a) Scheme of the half-bridge resonant VRM described in [1]; b) main waveforms in a switching period ($V_s = V_{in}/2N$)

electrical isolation between primary and secondary circuits was kept in order to simplify the control signal management.

III. CONTROL OF PARASITIC COMPONENTS

The key parameters for any high-frequency resonant converter are the resonant components, especially the resonant inductance. The latter, in fact, depends on parasitic components like the transformer leakage inductance, and the PCB trace inductance. The problem is exacerbated by the very high switching frequency that enhances skin and

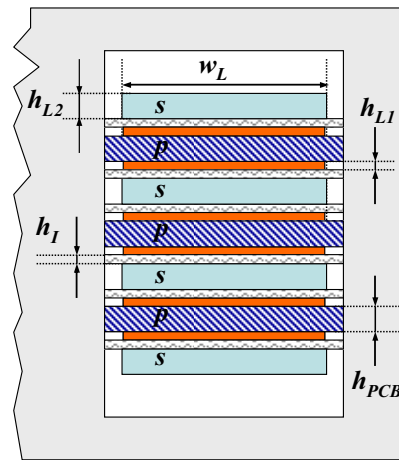


Figure 2. Transformer layer arrangement: p = primary layer, s = secondary layer (ER14.5/3/7 core 3F4 material)

proximity effects (at 1.8 MHz, the skin depth in copper at 100 °C is only 57 μm). Thus, a low leakage transformer is mandatory, calling for a high interleaved structure. The core employed was a planar ER 14.5/3/7 3F4 material from Ferroxcube and the windings were constructed by stacking thin double layer PCB sheets, for the primary five turns, and copper stamps for the single secondary turn. The layer arrangement is shown in Fig. 2 (from top to bottom): 1 turn secondary (copper stamp), 2 turns primary (first PCB sheet), 1 turn secondary (copper stamp), 1 turn primary (second PCB sheet with parallel connected traces, each on one side), 1 turn secondary (copper stamp), 2 turns primary (third PCB sheet), 1 turn secondary (copper stamp). All the primary turns are series connected while the four secondary stamps are parallel connected in order to reduce both dc and ac resistances. The winding physical dimensions are:

Copper stamp thickness h_{L2} :	200 μm
PCB trace thickness h_{L1} :	100 μm
PCB thickness h_{PCB} :	220 μm
Isolation sheet thickness h_I :	80 μm
Stamp and trace width w_L :	2.49 mm

Such arrangement gave a total leakage inductance of 61 nH, while the magnetizing inductance was 21 μH .

As far as the PCB trace inductances are concerned, they depend on both primary and secondary current paths, just like the losses associated to the PCB trace routing. One of the first layout we have experimented, used four SR MOSFETs parallel connected for each Q_1 and Q_2 all located on the same side of the PCB (see Fig. 3), with a ground plane on the opposite side of the PCB. Such arrangement gave high secondary losses mainly due to the strong proximity effect that causes a non uniform current distribution in the transformer secondary traces. Moreover, the strong vertical magnetic field produced by the secondary current (35 A peak, almost triangular current at 1.8 MHz) is likely to induce eddy currents on the ground plane, with associated losses. After a time consuming trial and error process, it has been recognized

that the only way to reduce both secondary parasitic inductance and ac resistance was to force the secondary current to flow on opposite layers in order to minimize the volume of the high magnetic field region (this provision gives benefit also from the electromagnetic compatibility point of view, by reducing the leakage magnetic field). Moreover, in order to force the current to spread over a large area on the PCB, the SR MOSFETs have been distributed and interleaved with the resonant capacitors C_1 and C_2 , each constituted by a parallel connection of four 10 nF and two 4.7 nF caps (5% tolerance).

As far as the position of the filter inductors L_{F1} and L_{F2} (one turn on a planar E14/3.5/5 core, 3F4 material from Ferroxcube) is concerned, they have been initially located on the edge of the PCB, as shown in Fig. 4 (prototype with two parallel connected SR MOSFETs for Q_1 and Q_2). Once again, such arrangement yield unacceptable performance in terms of power losses mainly due to a wrong current path (large area) and unequal current path length toward the resonant capacitors. The solution was to put the filter inductors in the middle of the SR MOSFETs in order to be equally displaced, as respect to the resonant capacitors, and to distribute symmetrically the filter capacitors C_F (eight 10 μ F caps on each side of the PCB).

Another crucial issue, strictly related to the converter losses, regards the techniques for removing the produced heat from the components in order to keep them at a reasonable maximum temperature. Having power components on both sides of the PCB, the only way to remove the heat was to

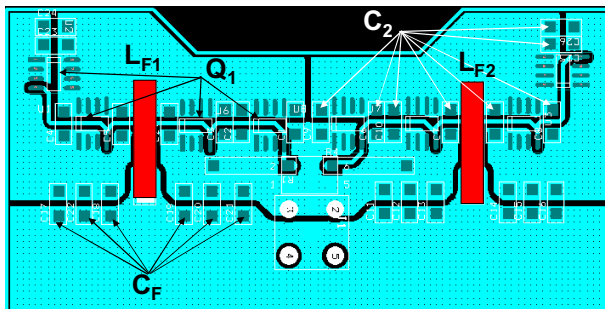


Figure 3. One experimented layout at the transformer secondary side with SR MOSFETs at the same PCB side (TOP view)

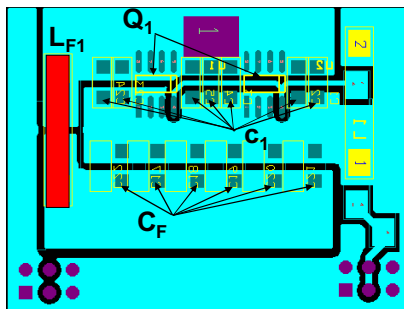


Figure 4. Other experimented layout showing one filter inductance located at the edge of the PCB (TOP view)

have a dissipating layer in between the two component layers, that was also used as ground connection at secondary side. Two different layouts were tested for the power stage: one using two layers of standard FR4 PCB (0.8 mm thickness) joined together to form an equivalent three layer PCB (see Fig. 5a) with an equivalent total inner layer thickness of 0.14 mm (PCB1), and the other built assembling two epoxy layers (0.5 mm thickness) on both sides of 0.7 mm thick copper baseplate shown in Fig. 5b (PCB2). As we can see, in the primary half bridge the layout employed followed the same philosophy used for the secondary circuit, i.e. the primary current follows a direct and return paths on different sides of the PCB (note the connection of the transformer to the capacitive node between C_A and C_B on the bottom layer). The resonant inductor was constructed with five turns of a Litz wire wound on a toroidal core (Micrometal T50-14 Powder Core).

Beside the components already mentioned above, the PCB includes the driver for the half bridge switches HB_1 and HB_2 (LM5101A from National) and a resonant driver for each SR MOSFET, different from the one proposed in [1], that was discussed in [2]. The latter employs a couple P-MOS and N-MOS on the same package (IRF7319) and exploits the internal 10 nH parasitic inductance (plus any external contribution from traces and layout) for charging and discharging in a resonant manner the SR MOSFET's gate equivalent capacitance.

The control signals, generated by a separate control circuit, are coupled with the power stage through the two connectors shown at the bottom edge of the PCB.

Finally, it is important to note that, even if the transformer secondary current loop has been minimized, the associated strong magnetic field could still cause significant losses due to eddy currents induced in the baseplate, whose thickness is not negligible (0.7 mm). In order to mitigate this problem, the baseplate was removed just inside the high field region.

IV. LOSSES DISTRIBUTION

In this section we want to discuss the converter power losses distribution that will be used for the thermal simulation of the PCBs. Due to the strong dependence on the layout, losses calculation is just an exercise, without any correlation with the reality. The only way is to measure them on the prototype, which is usually not an easy task. Fortunately, the resonant current resembles a triangular waveform, especially at nominal power: exploiting this similarity, we measured the losses of different components by operating the primary half-bridge with a short-circuit realized in different locations of the circuit (at the transformer's primary, at the transformer's secondary, by substituting the SR MOSFETs with copper strips, and by driving the SR MOSFETs with a constant V_{GS} voltage) and measuring the input power. The input voltage was adjusted any time in order to have a 7 A peak triangular resonant current i_R at primary side that roughly corresponds to the value measured at nominal power. The primary current has been measured with a small current transformer (6.4 mm

external diameter toroidal core with 1:10 turn ratio) with the secondary winding short circuited around a high bandwidth current probe. In this way, the 60 nH current probe inductance has been reduced by a factor of 100, becoming negligible as

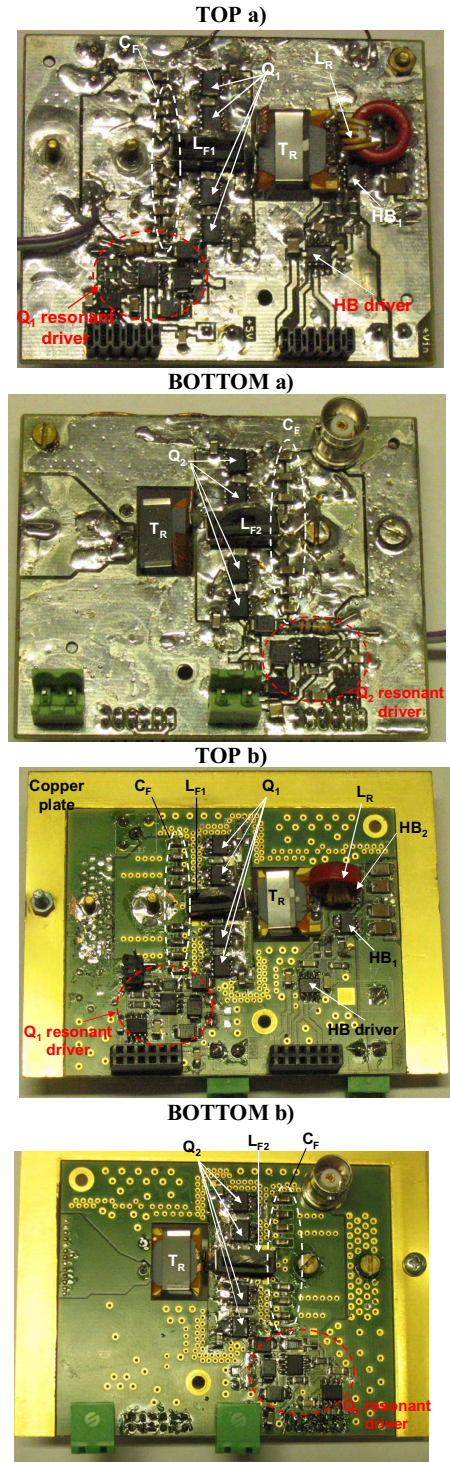


Figure 5. TOP and BOTTOM views of two prototypes: a) assembled two FR4 layers (PCB1); b) PCB with inner baseplate (PCB2)

compared to the resonant inductance L_R . Moreover, only a small loop was needed to accommodate for the current transformer. This procedure assumes that there is no dependence of the losses on the voltage, since all the switches operate with soft commutations. The short circuit at the transformer's primary allowed to estimate the total power dissipated by the resonant inductor L_R and the half bridge switches H_{B1} and H_{B2} (the individual contribution was then estimated calculating the MOSFET conduction losses from their R_{DS} value @ $t_j = 125^\circ\text{C}$). At the same time, it has been possible to measure the equivalent resonant inductance ($L_R + L_{\text{trace_primary}} = 285\text{ nH}$) from the knowledge of the input voltage needed to achieve the desired 7 A peak triangular resonant current. The short circuit at the transformer's secondary allowed to estimate the power dissipated by the transformer as well as its leakage inductance ($L_{\text{leak}} = 61\text{ nH}$). The short circuit created at the secondary side by substituting the SR MOSFETs with copper strips allowed to estimate the losses caused by the transformer secondary current loop (0.27 W) as well as its parasitic inductance (42 nH). Lastly, the short circuit created at the secondary side by driving the SR MOSFETs with a constant V_{GS} voltage, allowed to calculate their associated losses. As we can see, the overall resonant inductance was roughly 390 nH with the overall parasitic inductance weighting for almost 26% of the total value.

The results of the power loss measurements are summarized in table II in the case of PCB2 with IRF7836 SR MOSFETs: the resonant driver dissipation was simply measured thanks to the use of a separate power supply for them, while the power dissipation of the half-bridge driver was estimated from the MOSFET total gate charge ($Q_g = 28\text{ nC}$ extrapolated for $V_{GS} = 10\text{ V}$, $V_{DS} = 48\text{ V}$ for IRF7855)

TABLE II. DISSIPATED POWER FOR THE MAIN HEATING COMPONENTS ESTIMATED FROM MEASUREMENTS

Component	Ref. name	$I_{\text{out}}=30\text{A}$ Power [W]	$I_{\text{out}}=40\text{A}$ Power [W]	$I_{\text{out}}=50\text{A}$ Power [W]
Primary MOSFET 1	IRF7855	0.32	0.51	0.72
Primary MOSFET 2	IRF7855	0.32	0.51	0.72
Primary driver	LM5101A	1.0	1.0	1.0
Primary inductor	-	0.43	0.68	0.95
Transformer	-	0.9	1.5	2.1
Secondary inductor	-	0.18	0.32	0.5
Secondary traces	-	0.15	0.22	0.27
Secondary MOSFET 1	IRF7836	0.087	0.11	0.21
Secondary MOSFET 2	IRF7836	0.087	0.11	0.21
Secondary MOSFET 3	IRF7836	0.087	0.11	0.21
Secondary MOSFET 4	IRF7836	0.087	0.11	0.21
Secondary driver	IRF7319	1.0	1.0	1.0

and the well known formula:

$$P_{pd} = Q_g V_{GS} f_s$$

The described power loss analysis was not able to find all the contributions (resonant capacitors, output filter inductors and capacitors, output traces, etc.) so that the remaining power loss has been estimated by subtracting the total measured losses (6.4 W) from the total power loss measured at nominal conditions, i.e. with the converter delivering 65 W power at 1.3 V and 50 A (~ 12 W).

The converter efficiency of the power stage only (driver losses not included) measured at different output current values is reported in Fig. 6 for three different prototypes: PCB1 and PCB2 with IRF7836 SR MOSFETs and PCB2 with STS12NH3LL SR MOSFETs. As we can see, with IRF7836 SR MOSFETs the power stage efficiency at nominal power is 86% for PCB1 and 84% for PCB2 showing the influence of the thicker baseplate of PCB2 with associated eddy current losses, while with STS12NH3LL SR MOSFETs (lower total gate charge but higher $R_{DS(on)}$) the efficiency is close to 81% (in this case it was not possible to reach the nominal output current due to control saturation).

By including the driver losses, the overall efficiency drops of 3 points. It is important to mention that the efficiency measured at different times showed a uncertainty of $\pm 1\%$.

V. THERMAL SIMULATIONS

5.1 Single device model

The first step in the thermal modeling was to build-up a thermal finite element model (FEM) of the single SMD chip (see Fig. 7). We took, as a reference structure, that of bondless SO-8 STS12NH3LL power MOSFETs used as synchronous rectifiers, whose data were almost totally known either from literature or SEM (Scanning Electron Microscopy) inspection. Such a model was implemented using a commercial software tool (COMSOL

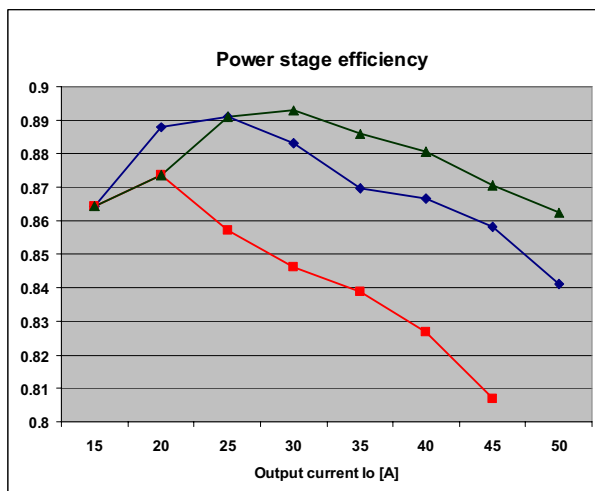


Figure 6. Comparison of the converter efficiency for three different prototypes: PCB1 (upper trace) and PCB2 (middle trace) with IRF7836 SR MOSFETs and PCB2 with STS12NH3LL SR MOSFETs (lower trace)

Multiphysics™), able to carry out multi-physics 3D simulations. The heat transfer module has been used, which includes Fourier conduction and convection equations [3].

As can be seen from Fig. 7, drain and source contacts are directly connected to the leads, by means of metal flanges and only the gate contact is wire bonded. The 3D structure of the packaged chip features elements with very different shapes (in particular, internal connections were done by thin metal layers), which required different meshing techniques for proper FEM treatment.

In this model the unknown parameters were the thermal resistance of the interface between the silicon die and the aluminum flanges (which is the sum of the thermal resistance of the solder layer plus the two Si-solder and solder-Al thermal contact resistances), the thermal conductivity of the package plastic lid, and the thermal convection coefficient. We estimate the values of these parameters by fitting experimental thermal data obtained from a suitable testing board, following the procedure explained in [4], until we obtained a worst-case difference of 10% between simulated and measured temperature variations on the test board.

5.2 Converter Thermal Model

The main scope of the model was to establish the maximum temperatures reached in the various board's layers and interfaces in thermal steady state, then the silicon die was treated as a uniform power source. Moreover, again following the procedure described in [4], from the accurate (and very complex, from the computational point of view) model of the chip, we built-up a simplified model, consisting in an homogeneous parallelepiped with the same external surfaces of the real package, without leads, with the power generated by an inner volume, properly placed inside the package, in order to obtain the same temperature distribution as calculated by the accurate model (see Fig. 8).

The other main heating components on the board were the MOSFETs at the primary section, the two MOSFET's

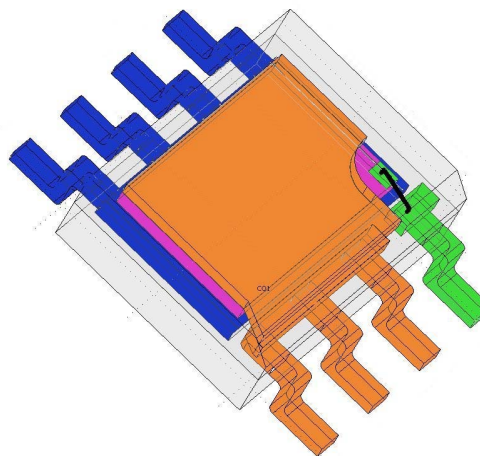


Figure 7. 3D FEM model of a the STS12NH3LL power MOSFET: drain and source metallization are directly connected to the leads, without wire bonding

drivers, the HF transformer, the three inductors and the filter capacitors. For SO-8 MOSFET and driver chips we used the same structure as well as the STS12NH3LL, with different thermally resistive layer between the inner volume where the heat is generated and the board, to account for different junction to ambient thermal resistance reported in the datasheets.

The inductors were designed with simplified structures (cores with same geometrical dimensions of the real ones, but simplified wounds). The transformer geometry was simplified as the SO-8 packages with three layers on each side of the PCB in place of the core and a trench in the PCB around the core. The capacitors were modeled as simple ceramic parallelepipeds with same geometrical dimensions of the real ones.

The secondary section of the circuit was replicated on the two sides of the board.

Heat transfers by conduction through the mounted packages to the board were modeled according to:

$$\nabla \cdot (-k \nabla T) = Q$$

where Q is the heat generated per volume unit and k is the thermal conductivity. Q was considered negligible in the circuit board, except that in the interconnection lines of the secondary section. The inductors were modeled to generate heat mostly in the copper wounds. In previous simulations of 3D FEM electro-thermal models of inductors operating with AC currents at 1.8 MHz, we observed that a little amount (5-10 %) of the total heat is produced by eddy currents in the core. Then, we considered a similar power dissipation in the inductors in the steady state simulations of the converters.

The thermal conductivities of the components were chosen to be similar to:

- IC epoxy resin (1.2 W/(m·K)), for the top layer of the chips;
- Al-Si (160 W/(m·K)), for the inner layer of the chips;
- FR4 (0.3 W/(m·K)), for the PCB1 board;
- Epoxy resin (0.5 W/(m·K)), for dielectric layers of the PCB2 board;
- Copper (400 W/(m·K)), for the ground plane (baseplate in the PCB2 board) and interconnection lines;

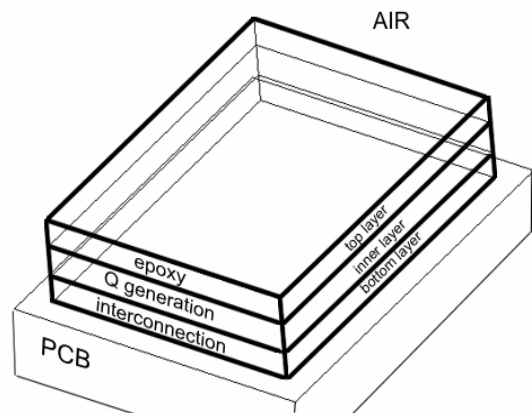


Figure 8. MOSFET simplified 3D model

- Copper, for the wound inductors;
- Ferrite (1 W/(m·K)), for magnetic cores;
- Ceramic (25 W/(m·K)), for capacitors.

The thermal conductivities of the chips bottom layers were chosen as fitting parameters to match the thermal resistances between junctions and ambient of each chip.

During thermal measurements, the board was clamped with a metal bench vise. The vise acted like heat sink with fixed temperature, then we set the temperature on the two edge in contact with the vise.

Heat dissipates from all air-exposed surfaces through natural air convection, which was modeled using a heat transfer coefficient, h :

$$q = h(T_{inf} - T)$$

where q is heat flux through the surface, T_{inf} is the external temperature and T is the point temperature on the surface. Fig. 9 illustrates the imposed boundary conditions.

To reduce the computational complexity, the thin conducting layers of the interconnection lines were modeled using a 2D shell approximation, according to:

$$\nabla \cdot (-d_s k \nabla_s T) = 0$$

where d_s is the layer's thickness (35 μm in our case), and ∇_s represents the nabla operator projected onto the direction of the plane. The model uses a general heat transfer application mode of Comsol Multiphysics to describe the 3D heat transfer as well as the 2D shell heat transfer in stationary state.

In order to consider Joule effect heat generation at 2D modeled interconnection layers, it is possible to set an heat flux at the boundaries representing these layers. We did this for secondary interconnection lines, although the electric measurements showed a little amount of power losses, if compared with the ones of other components.

We built-up two models, corresponding to the two versions of the converter, i.e. PCB1 and PCB2 previously described, with IRF7836 SR MOSFETs. As an example, Fig. 10 shows the simulated thermal distribution obtained on the upper side of the two models by imposing the same dissipated power for the components, as reported in table II, which were estimated

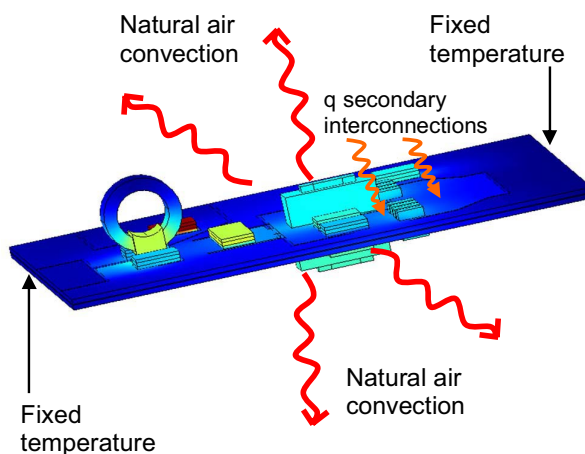


Figure 9. Thermal boundary conditions of the converter 3D FEM model

by the electrical measurements described in section IV.

The simulations were done first determining the fitting parameters for the PCB1 solution at $I_{out} = 50$ A. All other simulations were done using the same parameters.

The solution with integrated baseplate (PCB2) showed better behavior either in term of thermal uniformity and maximum temperatures.

VI. THERMAL MEASUREMENTS

A comparison between the two technological solutions of the converter was carried out from the thermal point of view, biasing them at different output current levels (30, 40 and 50 A) and detecting the thermal image of the board surfaces, by means of a Flir A20 infrared thermocamera.

A preliminary series of thermal measurements was carried out by means of k-thermocouples placed on the top of the heating components, to adjust in the thermocamera software the value of the emissivity of the various surfaces (the effect of the thermocouple itself was also estimated). The ambient temperature was 26 °C, input and output voltage were fixed at 48 V and 1.3 V, respectively.

Fig. 11 shows, as an example, the thermal map of the up-side of the converter measured with the IR camera for the two solutions (top: PCB1; down: PCB2) with 50 A of load current. Similar results were obtained for the downward surfaces.

It should be pointed out that the surface temperature is correctly represented by the color scale in the IR map only at

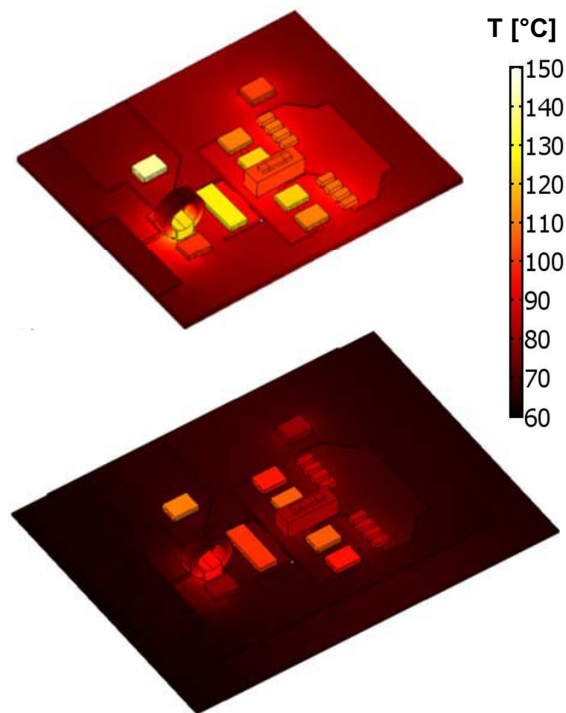


Fig. 10. Boundary thermal map of the up-side of the converter operating with 50 A load current (top: PCB1 solution; bottom: PCB2 solution)

the reference points, were a calibration of the emissivity was performed. This clearly appears, for instance, in the empty areas, which seem colder in the PCB1 than in PCB2, because the metallized surface (visible in Fig. 5a) is not passivated and has a very low emissivity.

Table III reports the measured and simulated temperatures at different points of the upper surface of the two boards for three different levels of load current (30, 40, and 50 A).

The measurement results confirm the better thermal behavior of the solution with integrated baseplate (PCB2) forecasted by FEM simulations: better thermal distribution over the board, a lower peak temperature of active and passive components and a lower mean temperature on the board.

The match between measured and simulated data is quite good: because some unknown parameters in the FEM thermal model were adjusted to fit the measured temperatures in the FR4 board at 50 A load current, the agreement for PCB1 is better than for PCB2. Nevertheless the differences in temperature increase over the ambient temperature are, in any

TABLE III. TEMPERATURES MEASURED (SIMULATED) AT THE SURFACE OF THE HEATING COMPONENTS IN THE TWO BOARDS AT DIFFERENT CURRENT LEVELS.

Component (test point)	T [°C] (PCB1)			T [°C] (PCB2)		
	I_{out} 30A	I_{out} 40A	I_{out} 50A	I_{out} 30A	I_{out} 40A	I_{out} 50A
Primary MOSFET 1	74 (72)	81 (80)	96 (102)	51 (54)	57 (60)	70 (75)
Primary MOSFET 2	75 (73)	82 (82)	96 (100)	51 (54)	57 (60)	70 (77)
Primary driver	123 (124)	129 (129)	143 (143)	97 (95)	102 (99)	114 (118)
Primary inductor wound	83 (82)	98 (98)	123 (122)	67 (62)	79 (73)	106 (94)
Primary inductor core	54 (53)	59 (60)	68 (69)	46 (47)	52 (55)	68 (67)
Transformer	82 (79)	96 (98)	121 (126)	68 (63)	81 (77)	108 (100)
Secondary inductor	73 (69)	84 (85)	104 (101)	63 (56)	74 (66)	96 (81)
Secondary MOSFET 1	72 (70)	85 (81)	107 (110)	59 (61)	70 (68)	93 (97)
Secondary MOSFET 2	76 (75)	90 (88)	116 (121)	64 (65)	77 (73)	103 (106)
Secondary MOSFET 3	78 (75)	93 (88)	118 (121)	64 (66)	77 (74)	102 (105)
Sec. MOSFET 4	75 (71)	88 (82)	110 (111)	60 (62)	70 (69)	91 (96)
Sec. driver	80 (79)	86 (86)	99 (102)	64 (63)	71 (67)	84 (80)
Board primary region	59 (58)	62 (62)	71 (73)	46 (48)	51 (50)	62 (64)
Board secondary region	59 (60)	67 (70)	83 (86)	48 (49)	54 (54)	68 (67)
Corner of the board	53 (53)	59 (59)	71 (74)	46 (47)	51 (51)	64 (64)

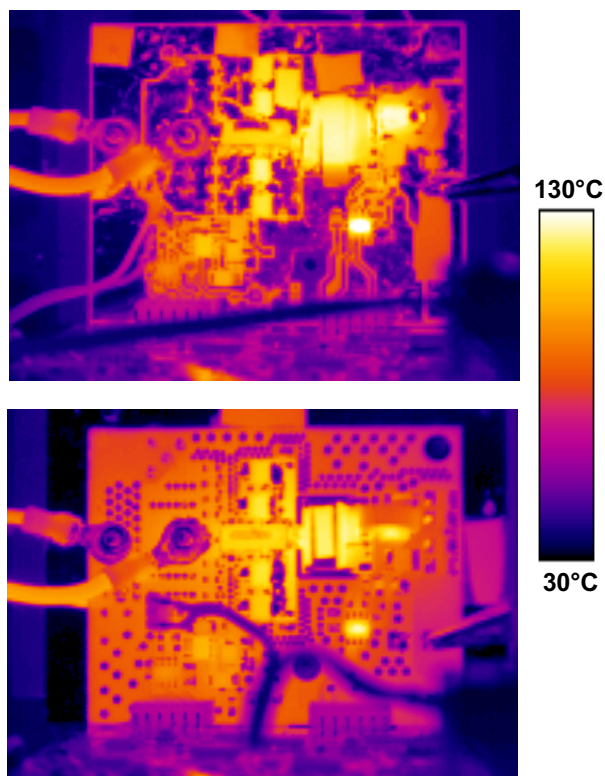


Figure 11. Thermal map of the up-side of the converter measured with the IR camera for the two solutions (top: PCB1; bottom: PCB2) with 50 A load current.

case, lower than 10% on the whole board, except for some points of magnetic components, probably due to the approximated models adopted for these elements.

This results confirm the validity of our simulation approach for thermal analysis and design of new power converter layouts and demonstrated the suitability of the final solution for the considered 1.8 MHz VRM.

The version of PCB2 mounting STS12NH3LL SR MOSFETs was also thermally characterized: we found a temperature distribution similar to that of the version with IRF7836, but about 15 °C higher (in the case of 50 A load current) in the SR MOSFET area. This higher heating was likely due to the lower efficiency, caused by the higher R_{DSon} of these MOSFETs.

CONCLUSIONS

In this paper, practical issues regarding the physical realization of a 1.8 MHz VRM described in [1] have been discussed in detail. The objective was to gain control on the layout-dependent parasitic components as well as to efficiently manage the dissipated power. In order to forecast the critical component temperature a FEM model of the whole converter has been developed. The complete model was based on a detailed thermal model of the single chips, which was validated by a comparison with measured temperatures on an *ad-hoc* designed and fabricated test board. The converter model was then simplified to meet a reasonable computational dimension.

Thermal measurements, by infrared thermocamera, allowed us to adjust some unknown model parameters, so that a mismatch within 10% in temperature variation between simulations and measurements was reached in the whole converter. The thermal model was built for the two PCBs with different technology. Thermal measurements were performed at different load current levels for both the PCBs and, in the case of PCB2 (the one with integrated copper baseplate), with different SR MOSFETs. The comparison shows that the PCB with integrated baseplate has a better thermal distribution over the board, a lower peak temperature of the active and passive components and a lower mean temperature on the board, confirming the results of FEM simulations.

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