

EXTENSION OF AIR COOLING FOR HIGH POWER PROCESSORS

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ABSTRACT

Air cooling limits for a high power CPU with high local power density were explored through a thermal model. The thermal model included a 20 mm × 20 mm die that was assumed to have power dissipation of 160W and a local power density of 100W/cm². Package size is assumed to be 50 mm × 50 mm, and the heat sink volume is 100 mm (flow length) × 100 mm (width) × 45 mm (height). The heat sink base is 5 mm thick. The effects of various package materials and configurations; thermal interface material between package and heat sink; heat sink base configurations, parallel plate fin geometries; and air flow conditions on the overall thermal performance have been investigated. Analytical methods are used to predict heat transfer and pressure drop for the parallel plate fin heat sink. Entropy generation rate minimization is applied in the optimization of the fin geometries and flow conditions. Finally, numerical model and heat sink performance results are used to predict air cooling limit.

KEY WORDS: Thermal model, heat sink, electronic package, air-cooling, vapor chamber, entropy generation, optimization

NOMENCLATURE

A_b	Heat sink base area, m ²
A_t	Total heat transfer area, m ²
c_p	Specific heat of air, J/kgK
D_h	Hydraulic diameter of parallel plate channel, m
h	Average fin heat transfer coefficient, W/m ² K
h_{eff}	Effective heat transfer coefficient of the heat sink base, W/m ² K
H_f	Fin height, m
k	Thermal conductivity, W/mK
m	Mass flow rate of air, kg/s
N	Total number of fins
Pr	Prandtl number
Q	Power dissipation on CPU, W
R_{ba}	Thermal resistance between top of heat sink base and ambient, °C/W
R_{die}	Thermal resistance from die, °C/W
R_{cs}	Thermal resistance between top surface of package and bottom surface of heat sink, °C/W
R_{ja}	Total thermal resistance between junction and ambient, °C/W

R_{jc}	Package thermal resistance, °C/W, = $R_{die} + R_{TIM1} + R_{Lid}$
R_{js}	Thermal resistance between junction and bottom surface of heat sink base, °C/W, = $R_{jc} + R_{cs}$
R_{jb}	Thermal resistance between junction and top surface of heat sink base, °C/W, = $R_{js} + R_{sb}$
R_{Lid}	Lid thermal resistance, °C/W
R_{sa}	Heat sink thermal resistance, °C/W, = $R_{sb} + R_{ba}$
R_{sb}	Heat sink base thermal resistance from bottom surface to top surface of heat sink base, °C/W
Re	Reynolds number, = $\rho U_{ch} D_h / \mu$
s	Fin gap, m
$S_{gen,H}$	Thermal entropy generation rate, W/K
$S_{gen,pp}$	Hydrodynamic entropy generation rate, W/K
$S_{gen,T}$	Total entropy generation rate, W/K
t	Thickness, m
t_f	Fin thickness, m
T	Temperature, K
U_{ch}	Air velocity between parallel plate fins, m/s
U_f	Approach air velocity, m/s
V	Volume flow rate of air, m ³ /s
W_{pp}	Fluid pumping power, W, = $\Delta P \times G$

Greek symbols

η_o	Overall surface efficiency
ΔP	Total pressure drop across the heat sink, Pa
ρ	Air density, kg/m ³
μ	Dynamic viscosity, N.s/m ²

Subscripts

b	top surface center of heat sink base
$inlet$	air inlet
j	junction
die	die
Lid	Lid material as heat spreader
$TIM0$	Thermal interface material between die and heat sink base for lidless package
$TIM1$	Thermal interface material between die and lid
$TIM2$	Thermal interface material between lid and heat sink base

INTRODUCTION

The power dissipation of the high performance CPUs increasing over time in high end server platforms. The 900 MHz Sun UltraSPARC III dissipates approximately 80W [1],

the IBM Power 4 single chip power level has been above 120 W [2], and the Intel Itanium 2 is about 130W [3]. According to the International Technology Roadmap for Semiconductors (ITRS) [4], power for high performance CPUs is projected to exceed 160 W in the near future as shown in Fig. 1. Meantime, local power density on a chip is increasing as the functional integration level is increasing. Hence larger temperature gradients across the die will be expected. The local power density has been reported to be near 100 W/cm² in the Power 4 chip [5]. In order to maintain the junction temperature below 90°C for the high performance CPU [4], improvement in package materials, package configuration, process, and heat sink technologies will be required. Maintaining an air-cooled design is becoming more challenging for future processors. Understanding air-cooling limits and associated costs are essential. Improvement in one single area will not be sufficient to meet overall thermal requirements. Therefore, having an integrated approach for the die, package and the air-cooled heat sink is critical.

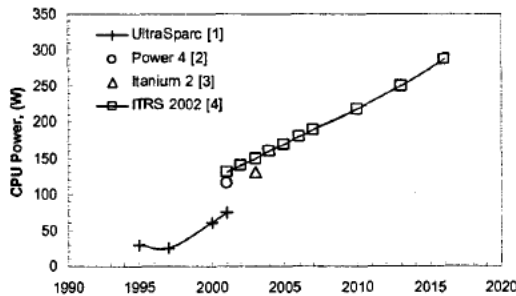


Fig. 1 High performance processor power trend

The objective of this study is to predict the air cooling limit through the development of an integrated numerical model. The integrated model included the die, package, and air cooled heat sink. A 3-D finite element method is used to perform the numerical model. Analytical methods for parallel plate fin are used for heat transfer and pressure loss calculation. Then, the heat transfer coefficient from the analytical method is employed as a boundary condition in the 3-D finite element model. The effects of a non-uniform power map, package material thermal conductivity, package configuration, heat sink base configuration, fin structures and air flow on the overall thermal performance are examined. Maximum allowable CPU power versus pumping power is estimated for a given power map on the die.

MODELING APPROACH AND SIMPLIFICATIONS

A commercial finite element method software ANSYS is used in this study [6]. A three dimensional model for the entire package was created. Computational domain includes Flip Chip package and heat sink base as shown in Fig. 1. The heat sink fin structure is not included in the computational domain and the model approach is described below. The package consists of a substrate, solder bumps with underfill, die, thermal interface material (TIM1) and Lid (heat spreader).

Geometry parameters and material properties for the package materials are listed in Table. 1. All of the thermal interface material conductivities in this Table are effective thermal conductivities. The effective thermal conductivity for thermal interface material k_{TIM} is given by

$$\frac{t_{TIM}}{k_{TIM}} = \frac{t_{TIM}}{k_{bulk,TIM}} + \frac{2}{h_{contact}} \quad (1)$$

Where t_{TIM} is thermal interface material thickness, $h_{contact}$ is heat transfer coefficient between surfaces which represent the contact thermal resistance. Both TIM bulk thermal conductivity $k_{bulk,TIM}$ and $h_{contact}$ can be determined experimentally by changing TIM thickness. In the baseline study, thermal interface material conductivity is assumed as 3 W/mK for conventional material such as silver epoxy and thermal grease. A wide range of thermal conductivity is used to study the effect that the different materials have on the thermal performance. Bond line thickness is fixed at 100μm for all cases. Typical lid material such as copper tungsten with thermal conductivity around 180W/mK is employed in the base line study.

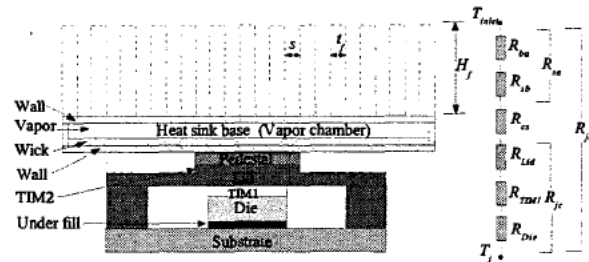


Fig. 2 Modeling configuration (not scaled) and thermal resistance network

As part of the parametric study, the size of the pedestal was varied in order to characterize the effect on the overall thermal performance. The dimensions of the passive phase-change heat sink base (vapor chamber) is 100 mm (W) × 100 mm (L) × 5 mm (H) is used in the model. Assumptions of vapor chamber construction and parameters used in this study are cited from the literature [7]. The 5 mm thick vapor chamber consists of 1 mm thick copper base, 1 mm thick wick structure, 2 mm vapor space and 1 mm copper wall. Effective thermal conductivities of wick structure and vapor space are assumed to be 40 W/mK and 50000 W/mK respectively in the baseline study. Vapor chamber base provides very effective heat spreading from relative small heat input area at the top of the package to the larger heat sink base area. Detail description of the vapor chamber can be found in the reference [7].

To simplify the modeling geometry, heat sink fins are not the part of simulation. Rather, an effective heat transfer coefficient is imposed as a boundary condition on the heat sink base. The effective heat transfer coefficient and pressure loss across the heat sink are calculated from analytical

methods [8, 9] for parallel plate fin structure in fully-ducted flow channel. The effective heat transfer coefficient on the heat sink base [8] is given by

$$h_{eff} = \frac{mc_p}{A_b} \left(1 - e^{-hA_f \eta_o / mc_p} \right) \quad (2)$$

where A_f is total surface area of heat sink base and fin exposed to air flow, η_o is overall surface efficiency [10], h is the average convective heat transfer coefficient. h is calculated from Nusselt number [11] for high aspect ratio of fin height to fin gap, as follows

$$Nu = \frac{hD_h}{k_{air}} = \max(7.54, 0.024 Re^{0.786} Pr^{0.45}) \quad (3)$$

where D_h is the hydraulic diameter of parallel plate channel, $= 2SH_f / (s + H_f)$. The air velocity U_{ch} in the parallel plate channel is used to define Reynolds number, $Re = \rho U_{ch} D_h / \mu$.

Assuming zero contact thermal resistance at the fin-to-heat sink base connection, a thermal resistance R_{ba} from top surface of the heat sink base to air flow can be defined as:

$$R_{ba} = \frac{T_b - T_{inlet}}{Q} = \frac{1}{h_{eff} A_b} \quad (4)$$

Table.1 Modeling parameters

Model configuration	Parameters	Baseline input	Range
Boundary condition	T_{inlet} (°C)	30	30
	h_{eff} (W/m ² K)	840	500 - 1600
Heat sink Base (Vapor chamber) [7]	Size (mm)	100x100x5	100x100x5
	t_{wall} (mm)	1	1
	k_{vapor} (W/mK)	50000	5x10 ⁴ - 377 (Cu base)
	t_{vapor} (mm)	2	2
	k_{wick} (W/mK)	40	20 - 80, 377 (Cu base)
	t_{wick} (mm)	1	1
	k_{wall} (W/mK)	377	377
	t_{wall} (mm)	1	1
	k_{ped} (W/mK)	377	377
	t (mm)	0	0 - 2
Pedestal	Size (mm)	N/A	20 x 20 - 35 x 35
	k_{TIM2} (W/mK)	3	1 - 20
TIM2	t_{TIM2} (mm)	0.1	0.1
	Size (mm)	50x50	50x50
Lid	t_{Lid} (mm)	2	1 - 3, Lidless
	k_{Lid} (W/mK)	180	180 - 1000
TIM1	k_{TIM1} (W/mK)	3	2 - 20
	t_{TIM1} (mm)	0.1	0.1
Die	Size (mm)	20 x 20	20 x 20
	t_{die} (mm)	0.6	0.6
	k_{die} (W/mK)	90	90
	Power (W)	160	160
C4 bump and Underfill	k (W/mK)	1	1
Substrate	Size (mm)	50 x 50	50 x 50
Boundary condition	h_{sub} (W/m ² K)	10	10

where T_b is the maximum temperature at the upper surface of heat sink base, T_{inlet} is the air inlet temperature and Q is total power dissipation from the die. Total pressure loss across heat sink includes entrance pressure loss, friction loss and exit pressure loss, is calculated from the Copeland's correlation [9]. In the baseline simulation, R_{ba} is calculated to be 0.12°C/W per Eq. (4). The associated heat sink fin material for the baseline simulation is aluminum ($k = 220$ W/mK), and the flow passage gap between fins is 2mm with 0.4 mm fin thickness. Per Eq. (2), the effective heat transfer coefficient is approximately 840 W/m²K at the flow rate through the heat sink of 0.015 m³/s. The corresponding pressure loss is predicted to be 37 Pa.

In addition to the boundary condition at the top of heat sink base as described above, a heat flux source is applied to the bottom of the die, and a convective heat transfer boundary condition is applied to the bottom of substrate. Sides of package and heat sink base are assumed to be adiabatic.

The thermal resistance network shown in Fig. 1 is utilized to define the individual components. The thermal resistance of the individual components in this paper is defined as

$$R_{xy} = (T_{x,max} - T_{y,max}) / Q \quad (5)$$

Where $T_{x,max}$ is the maximum temperature at the lower surface, and $T_{y,max}$ is the maximum temperature at the upper surface for each individual component.

The total thermal resistance is defined as

$$R_{ja} = (T_j - T_{inlet}) / Q \quad (6)$$

where T_j is the maximum junction temperature on the die. The junction-to-air overall thermal resistance can be separated into a package-level thermal resistance R_{jc} , thermal interface material (TIM2) resistance R_{cs} , and heat sink thermal resistance R_{sa} as follows

$$R_{ja} = R_{jc} + R_{cs} + R_{sa} \quad (7)$$

The package thermal resistance R_{jc} can be further divided into die thermal resistance R_{die} , TIM1 thermal resistance R_{TIM1} , and lid thermal resistance R_{Lid} , and given by

$$R_{jc} = R_{die} + R_{TIM1} + R_{Lid} \quad (8)$$

Normally, R_{jc} is defined as difference of maximum die temperature and upper lid surface temperature at the geometric center divided by the total power dissipation. This definition is a convenient approach used in engineering application and measurement. In most cases, the maximum upper lid surface temperature is approximately located at the center of the package. This has been verified through numerical model in

this study. The predicted difference between the maximum temperature of the upper lid surface and the temperature located at the surface center of the lid is less than 0.2°C. However, the maximum junction temperature typically is not located at the geometric center of the die for a non-uniform power map.

The heat sink to air thermal resistance is defined as

$$R_{sa} = (T_s - T_{inlet}) / Q = R_{sb} + R_{ba} \quad (9)$$

where T_s is the maximum heat sink base temperature, and is located at the geometric center of heat sink base bottom surface. To be better understanding of the sink to air thermal resistance, R_{sa} is divided into heat sink base thermal resistance R_{sb} and fin-to-air thermal resistance R_{ba} .

Mesh sensitivity study was carried out prior to the parametric study. Mesh sizes of 0.25 mm, 0.5 mm and 1 mm were examined. The variation of the maximum junction temperature is found to be less than 0.3°C at total power of 160W. Therefore, 1 mm mesh size was used in the model. Total number of elements in the model is approximately 10^5 .

RESULTS AND DISCUSSIONS

Baseline study and the effect of hot spot

To understand the effect of the local power density on the package performance, a uniform power map and a non-uniform power map with two local hot spots were simulated. As shown in Fig. 3 for the non-uniform power map, two individual local hot spots each dissipates 4W over a 4 mm² area, thus the power density is 100 W/cm². The remaining area on the die has a uniform power density of 38.8 W/cm². Total power dissipation on the 20 mm x 20 mm die is 160W for both uniform and non-uniform power maps.

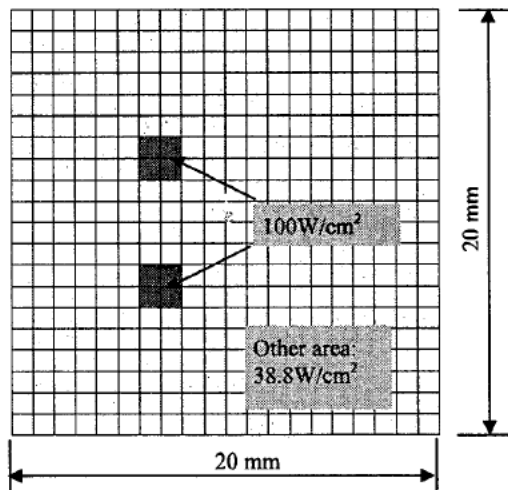


Fig. 3 Non-uniform power map on the die

Modeling results shown in Fig. 4 indicate the total thermal resistance increased by 0.045°C/W for the non-uniform power map as compared to the uniform power map. The most of increase is from package-level R_{jc} . Referring to Eq. (8), it is found that local hot spot increased the die thermal resistance R_{die} by 0.017°C/W and increased the TIM1 thermal resistance R_{TIM1} by 0.025°C/W, but has minimal increase for R_{lid} and R_{cs} . This indicates that the TIM1 performance has a dominant role for the non-uniform power map. Other parameters including local hot spot power density, hot spot size and location will affect the package thermal resistance, although evaluation of these parameters is not within the scope of this paper. Simulation data in the following sections are based on the non-uniform power map as shown in Fig. 3.

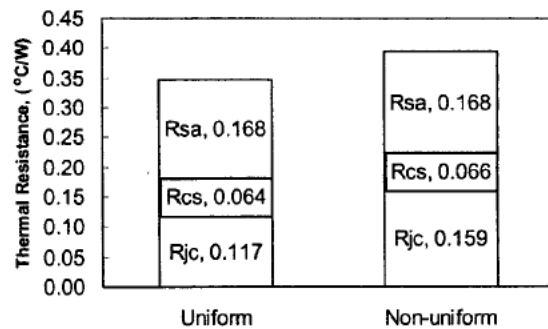


Fig. 4 Effect of power distribution on the thermal resistance

Effect of TIM1 thermal conductivity

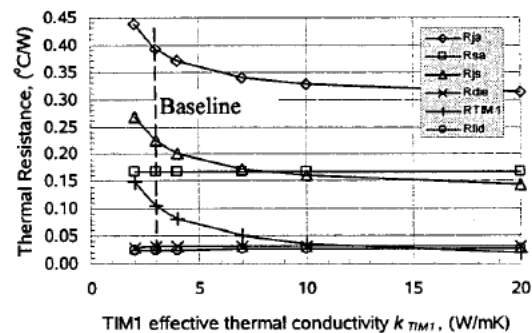


Fig. 5 Effect of TIM1 thermal conductivity

As improved TIMs become available to the marketplace, it is essential to understand gain from TIM performance improvement. The effective TIM1 thermal conductivity in this study ranged from 2 to 20 W/mK. It is shown in Fig. 5 that TIM1 only affects the TIM1 thermal resistance itself, does not affect the remaining thermal resistances including R_{die} , R_{lid} , R_{cs} and R_{sa} . As TIM1 thermal conductivity increases from 2 W/mK to 7 W/mK, it improves package thermal performance by 0.1°C/W, however as thermal conductivity increases from 7 to 20 W/mK, the improvement is approximately 0.03°C/W.

Thermal resistance of TIM1 reaches 0.02°C/W at an effective thermal conductivity of 20 W/mK . The increase in the TIM1 thermal performance becomes limited as TIM1 effective thermal conductivity goes beyond 20 W/mK .

Effect of lid material

Figure 6 shows the effect of lid material on the heat sink and also the individual package thermal performances when the lid thickness is 2 mm . It is found that a lid with increased thermal conductivity reduces the thermal resistance of R_{lid} , R_{TIM2} , and R_{sa} . Fig. 6 also shows an improved lid thermal performance has minimal impact on R_{die} and R_{TIM1} . It should be noted that heat sink base thermal performance is assumed to be independent of surface heat flux in this simulation. In reality, the vapor chamber base or other passive phase change heat sink base thermal resistance may increase as surface heat flux decreases at a fixed heat source area [7]. Therefore, it needs to be cautious about thermal resistance improvement from high thermal conductivity lid for the passive phase change heat sink base.

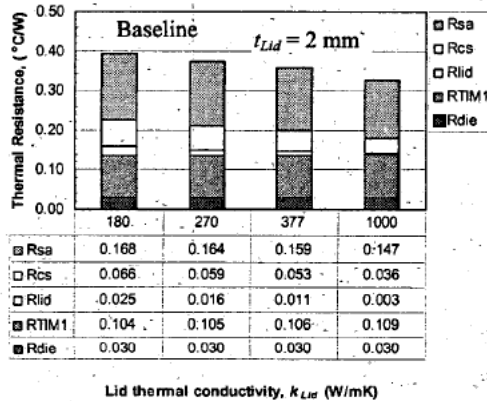


Fig. 6 Effect of lid thermal conductivity

The lid material and thickness effects on the overall thermal resistance are shown in Fig. 7. The results indicate that the impact of lid thickness is greater when the lid thermal conductivity is high than 200 W/mK . The total reduction in the overall thermal resistance R_{ja} is 0.07°C/W when increasing k_{lid} from 180 to 1000 W/mK at a lid thickness of 3 mm .

As an alternate package configuration, lidless package may be considered in order to improve thermal performance by eliminating lid material and one layer of thermal interface material. Thermal performance was also evaluated for the lidless package. The comparison between two package configurations is listed in Table 2. For the lidded package, a lid thickness of 2 mm is assumed. For the lidless package, thickness of thermal interface material (TIM0) between die and heat sink is assumed to be $100 \mu\text{m}$. Thermal conductivity of TIM1 in lidded package and TIM0 in lidless package is varied from 3 W/mK to 10 W/mK while TIM2 is a fixed value of 3 W/mK . When compared to the lidded package results for

$k_{\text{lid}} = 370 \text{ W/mK}$ and 180 W/mK , the lidless package yielded the total thermal resistance reduction of approximately 0.03°C/W and 0.07°C/W respectively, as the TIM0 thermal conductivity in the lidless package is equal to the TIM1 thermal conductivity for the lidded package. Model results indicate that as the lid thermal conductivity and the lid thickness increase, the thermal performance gain from lidless package will be diminished although results are not shown in Table 2. If the TIM0 thermal conductivity in the lidless package is less than the TIM1 thermal conductivity in the lidded package, the thermal performance of lidless package may be less than the lidded package performance. Therefore, the thermal interface material adjacent to the die plays a critical role for both lidded package and lidless package configurations.

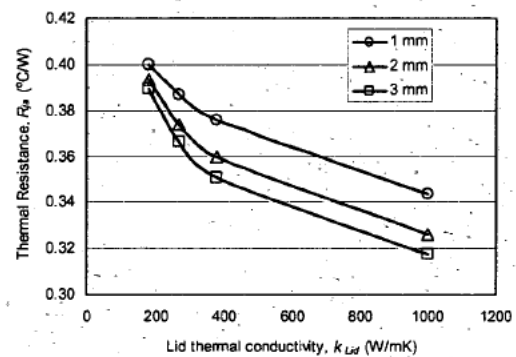


Fig. 7 Effect of lid thickness on overall thermal resistance

Table 2 Lidded package vs. lidless package

Package Config.	K_{lid}	K_{TIM1}	K_{TIM2}	R_{ja} ($^{\circ}\text{C/W}$)	R_{sa} ($^{\circ}\text{C/W}$)	R_{js} ($^{\circ}\text{C/W}$)
Lidded	180	3	3	0.225	0.168	0.393
	180	10	3	0.160	0.168	0.328
	377	3	3	0.197	0.153	0.351
	377	10	3	0.133	0.159	0.293
Lidless	N/A	3	N/A	0.139	0.187	0.327
	N/A	10	N/A	0.071	0.188	0.260

Effect of TIM2 thermal conductivity

The effect of TIM2 was also studied in this paper, although the impact of TIM2 on thermal performance might not be as significant as TIM1, since TIM2 is two layers away from die in the lidded package. As shown in Fig. 8, the thermal resistance of TIM2 decreases significantly when the TIM2 thermal conductivity increased from 1 to 7 W/mK . The thermal resistance will become 0.02°C/W when $k_{\text{TIM2}} = 10 \text{ W/mK}$. Data results from 1-D calculations which use the die area is provided in the same figure for comparison. It is shown that the 3-D model thermal resistance results are less than the results predicted by the 1-D calculation. As TIM2 thermal conductivity increases, the difference between model and 1-D calculation becomes minimized.

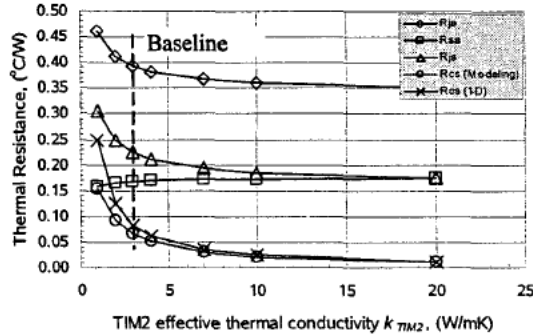


Fig. 8 Effect of TIM2 conductivity on thermal resistances

Effect of heat sink base configuration

The pedestal size investigated ranged from the size of the die at 20 x 20 mm to an upper limit of 35 mm x 35 mm, while the thickness of the pedestal is fixed at 2 mm. The model results in Fig. 9 indicate that the negative impact on the overall thermal performance provided by the pedestal will be less for increased pedestal size.

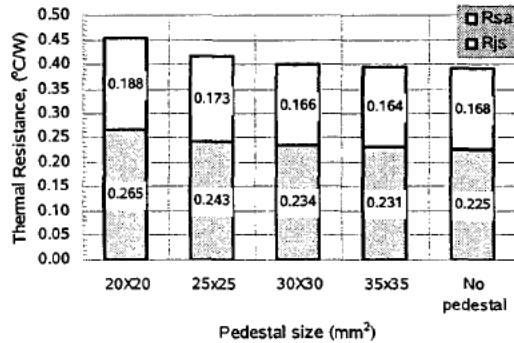


Fig. 9 Effect of pedestal configuration on the overall thermal resistance

As shown in Fig. 2, using vapor chamber as the heat sink base provides two dimensional heat spreading. As the heat is transferred through the evaporator wall to the wick structure, liquid within the saturated wick evaporate, vapor flows and then condenses in the upper condenser wall which has fins attached on the other side of air-cooling. Conduction through the evaporator wall and wick could dominate the vapor chamber base thermal resistance. In the model, wick structure is simplified as a solid material with effective thermal conductivity. The wick effective thermal conductivity is not only dependent on wick structure such as sintered powder metal, but also dependent on power density applied at the vapor chamber base. The impact of various effective thermal conductivities of wick structure is shown in Fig. 10. The overall thermal resistance can be improved by 0.013 C/W as the wick conductivity is double from base line value of 40

W/mK. The solid Cu model result is also shown in this figure for comparison. The results show that the vapor chamber heat sink base thermal performance is greater than the predicted performance for the solid Cu base heat sink. It needs to be noted that the thermal performance improvement from the vapor chamber could be less as the ratio of heat source area to the heat sink base area decreases, although this parameter was not included in this investigation. It also can be found from this figure that heat sink configuration has very little impact on package thermal resistance.

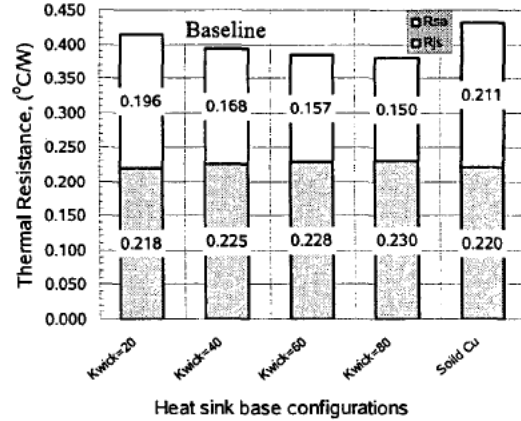


Fig. 10 Effect of heat sink base configuration

Parallel plate fin optimization

All of the model results discussed in the previous sections are based on a heat sink plate fin structure that has a fin flow passage 2 mm gap, a fin thickness of 0.4 mm which yields a total fin count of 42 fins. It was also assumed that a 0.015 m³/s air flow rate in a fully ducted channel flow. Optimization of the fin structure is essential to improve the thermal performance while attaining the required fan pumping power. The entropy generation minimization method developed by Bejan [12] is applied for parallel plate fin optimization in this paper. The total entropy generation rate $S_{gen,T}$ for external flow [13,14, 15] is given by

$$S_{gen,T} = S_{gen,H} + S_{gen,pp} = \frac{Q(T_b - T_{inlet})}{T_{inlet}^2} + \frac{V\Delta P}{T_{inlet}} \quad (10)$$

where $S_{gen,H}$ and $S_{gen,pp}$ are the entropy generation rates from thermal and hydrodynamic components respectively. Where, T_b is the temperature at the center of the top surface in the heat sink base, V is volume air flow rate, and ΔP is the total pressure loss across the heat sink. $V\Delta P$ is the fluid pumping power W_{pp} . Using the definition of R_{ba} in Eq. (4), the above equation can be expressed as:

$$S_{gen,T} = S_{gen,H} + S_{gen,pp} = \frac{Q^2 R_{ba}}{T_{inlet}^2} + \frac{W_{pp}}{T_{inlet}} \quad (11)$$

It can be seen from Eq. (11) that the total entropy generation rate is dependent on fin thermal resistance and fluid pumping power. As an example for this optimization approach, variation of only one parameter, the fin gap or the fin number was studied, while the overall heat sink size, fin thickness, air flow rate, fin thermal conductivity of 220 W/mK are held constant. The thermal resistance and overall pressure loss are calculated from Eq. (4) and Copeland's correlation [9] respectively. Detail optimization procedure for multiple parameters can be found in Culham and Muzychka [15].

The effect of fin number on total entropy generation rate is illustrated in Fig. 11. It indicates that the total entropy generation reaches the minimum value at fin number of approximately 63. Thermal entropy generation rate dominated the overall entropy generation rate when fin number is less than 40. On the other hand, pumping power increases with increased fin number, therefore, it is anticipated that the entropy generation rate from the hydrodynamic component will exceed that of the thermal component for fin numbers beyond approximately 90.

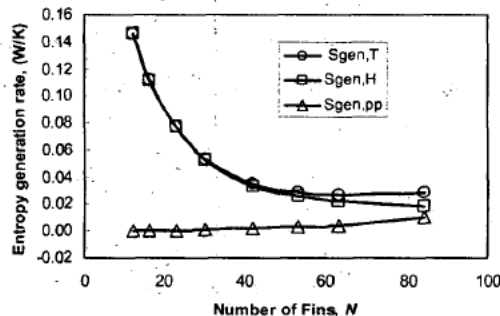


Fig. 11 Heat sink optimization at given fin thickness and air flow rate

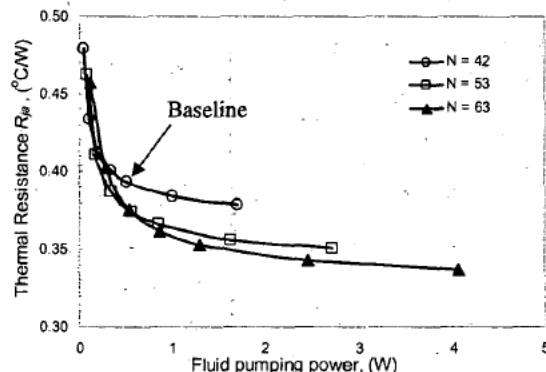


Fig. 12 Effects of pumping power and fin configuration

Figure 12 shows the effect of pumping power on the overall thermal resistance for three fin configurations at air flow rates ranging from 0.005 to 0.025 m³/s. It is shown that the overall

thermal resistance is reduced as the number of fins increases when the pumping power exceeds 0.5W. As pumping power increases from 0.1 to 1W, thermal performance can be improved by approximately 0.1°C/W. The reduction in the overall thermal resistance becomes minimized as the pumping power increases for a fixed fin configuration. This indicates the heat sink performance is approaching the air-cooling limit.

Allowable CPU power with air cooling

The parametric study investigated the impact on the thermal performance provided by the die, package material, configuration, heat sink base, and fin structure. Allowable CPU power can be determined from:

$$Q_{\max} = \frac{(T_{j,\max} - T_{\text{inlet}})/(R_{jc} + R_{cs} + R_{sa})}{(T_{j,\max} - T_{\text{inlet}})/(R_{jb} + R_{ba})} \quad (12)$$

Assuming a power map, package material, configuration, and heat sink base are given, thus only variable parameter is R_{ba} which is dependent on air flow rate and the fin design. As an example, the predicted R_{jb} thermal resistance is 0.177°C/W when $k_{TMM1} = 10$ W/mK, $k_{Lid} = 270$ W/mK, lid thickness of 2 mm, $k_{TMM2} = 4$ W/mK, and $k_{wick} = 80$ W/mK. If maximum allowable junction temperature $T_{j,\max}$ and air inlet temperature T_{inlet} are specified as 90°C and 30°C respectively, the maximum allowable power versus pumping power can be plot in the Fig. 13 for heat sink containing 63 parallel plate fins at varied air flow rates. In this example, the maximum allowable power will be 250W with $R_{ba} = 0.064$ °C/W, $R_{sa} = 0.108$ °C/W at fluid pumping power of 4 W. The system fan pumping power will be much higher than heat sink fluid pumping power due to dependency on the fan efficiency and total pressure drop in a computer system.

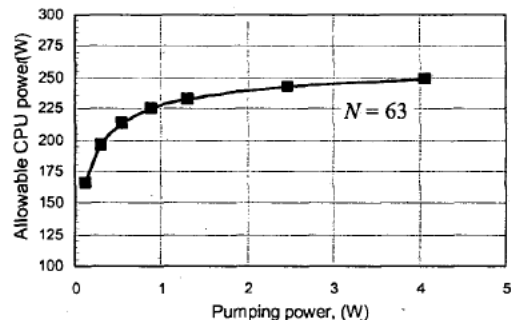


Fig. 13 Allowable CPU power vs. fluid pumping power

Figure 14 shows the maximum allowable power as a function of total thermal resistance. Maximum allowable power is approximately 150W for the baseline case with non-uniform die power map, 42 air fins, a 0.015 m³/s flow rate, and a 0.5W fluid pumping power. The maximum allowable power can be increased by 50W as the package materials performance is improved. Furthermore, increasing air fin number from 42 to 63, while also increasing the air flow rate from 0.015 m³/s

($W_{pp} = 0.5W$, $R_{sa} = 0.168^{\circ}C/W$) to $0.024 \text{ m}^3/\text{s}$ ($W_{pp} = 4W$, $R_{sa} = 0.108^{\circ}C/W$) will increase the allowable CPU power from 200W to 250W. The thermal resistance of R_{ba} may approach zero by maximizing the air flow rate and heat transfer coefficient, thereby reaching the air cooling limit. The maximum allowable power will not be higher than 340W. Therefore, the maximum allowable power is not only dependent on heat sink air flow performance, but also dependent on die power map, package material set and configurations.

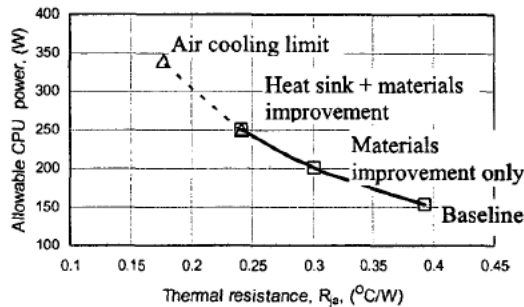


Fig. 14 Allowable CPU power vs. total thermal resistance

CONCLUSIONS

An integrated thermal model for CPU package and heat sink is performed using a 3-D finite element method. The computational domain included package, thermal interface material and heat sink base. An analytical method for air flow in plate fin heat sink is used to complete the overall model. The effects from package material thermal conductivity, package configuration, heat sink base, and fin geometry on the overall thermal performance have been discussed. The definition for die-level thermal resistance was introduced in order to study the affect of the local hot spot. Die-level thermal resistance is found to be independent of other parameters except the power map. The power map also affects the thermal resistance of TIM1. TIM1 material conductivity only impacts its own thermal resistance. Lid material conductivity potentially only affects the lid and other components thermal resistances above the lid. However, heat sink configuration and air flow have very little effect on the package thermal resistance. Based on the model investigation and heat sink prediction results, an approach to estimate the air cooling limited has been demonstrated.

From the model results, it is indicated that every individual resistance layer from die to air-cooled heat sink is equally important to meet thermal requirements for the air cooling regime. Concurrent efforts from silicon-level circuit design and layout, package material development, to heat sink design, and air flow optimization are recommended to manage the growing thermal challenge for cooling high powered processors that may also contain high local power density spots.

REFERENCES

- [1] UltraSPARC III Cu User's Manual, Version 2.2, page 1-3, May, 2003, Sun Microsystems Inc., U.S.A
- [2] J. D. Warnock et al., "The Circuit and Physical Design of the Power4 Microprocessor," IBM J. Res. & Dev., Vol. 46, No. 1, pp. 27-51, 2002
- [3] Intel Itanium 2 Processor Datasheet, page 2-3, 2003, Intel Inc., U.S.A
- [4] ITRS, International Technology Roadmap for Semiconductors, 2002
- [5] J. U. Knickerbocker et al., "An Advanced Multichip Module (MCM) for High-Performance UNIX Servers," IBM J. Res. & Dev., Vol. 46, No. 6, pp. 779-804, 2002
- [6] ANSYS, Version 6.0, ANSYS Inc., U.S.A
- [7] K. Grubb, "CFD Modeling of a Thermo-Base™ Heat Sink," 8th International Flotherm User Conference, Las Vegas, USA, 13-14 May, 1999
- [8] M. Saini and R. L. Webb, "Validation of Models for Air Cooled Plane Fin Heat Sink Used in Computer Cooling," Proc. of I-THERM, pp. 243-250, 2002
- [9] D. Copeland, "Optimization of Parallel Plate Heatsinks for Forced Convection," Proc. 16th IEEE SEMI-THERM Symposium, pp. 266-272, 2000
- [10] F. P. Incropera and D. P. DeWitt, "Fundamentals of Heat and Mass Transfer," 5th Ed., John Wiley and Sons, New York, 2001
- [11] Flotherm Reference Manual, Version 3.2, p. 15-47, Flomerics, 2002
- [12] A. Bejan, Entropy Generation Minimization. Boca Raton, FL: CRC Press, 1996
- [13] W. W. Lin and D. J. Lee, "Second Law Analysis on a Flat Plate-Fin Array under Crossflow," Int. Commun. Heat Mass Transfer, Vol. 27, No. 2, pp. 179-190, 2000
- [14] M. Iyengar and A. Bar-Cohen, "Least-Energy Optimization of Forced Convection Plate-fin Heat Sinks," IEEE Trans. on Components and Packaging Technologies., Vol. 26, pp. 62-70, 2003
- [15] J. R. Culham and Y. S. Muzychka, "Optimization of Plate Fin Heat Sinks Using Entropy Generation Minimization," IEEE Trans. on Components and Packaging Technologies., Vol. 24, pp. 159-165, 2001