MODERN DC-TO-DC SWITCHMODE POWER CONVERTER CIRCUITS

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MODERN DC-TO-DC SWITCHMODE POWER CONVERTER CIRCUITS

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FOR
JOY AND DIANA
AND
THE UNSUNG HERO
OF
ELECTRONIC DESIGN,
THE POWER SUPPLY ENGINEER

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Foreword

As each area of technology with a potential for significantly impacting any major segment of the electronics industry evolves, it often is accompanied by the development of a succession of new circuits. Each new circuit indeed appears different, employing different components in differing configurations, and claims an assortment of distinct features of "improved performance." Without a considerable investment of laboratory time to construct, evaluate, and compare each candidate circuit, it usually is difficult to realistically appraise the relative merits of one approach over another. It often is even more difficult to identify the underlying principles which point up basic similarities and differences. Such is the situation in the new and rapidly expanding area known as *electronic power processing* or *switching mode power supplies.*

The area of switching power supplies has been spurred by the need for power sources of higher performance, smaller volume, and lighter weight in order to achieve compatibility with the shrinking size of all forms of communication and data handling systems, and particularly with the portable battery-operated equipment in everything from home appliances and handtools to mobile communication equipment. Static dc-to-dc converters and dc-to-ac inverters provide a natural interface with the new direct energy sources such as solar cells, fuel cells, thermoelectric generators, and the like, and form the central ingredient in most uninterruptable power sources. Such solid-state power conditioners operating with internal conversion frequencies of tens to hundreds of kilohertz are emerging as the new mainstay of most power supplies for computers and communication systems, as they have already served over the last two decades for the space programs of the world.

A vast amount of circuit technology for switching power supplies has been generated in the past decade, and reported in numerous technical journals, conference proceedings and trade magazines. Our understanding of this rapidly evolving technology can be greatly enhanced by the introduction of some meaningful classification technique which assists in recognizing and focusing on fundamental elements and characteristics. In this way, the most important but often subtle aspects of a particular subject are brought to the surface so as not

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to become lost in the less important details. It has been found that such a classification scheme is indeed beneficial when working with the host of dc-to-dc converters which have evolved over the past two decades.

The authors have shown, for the first time, that a large class of the static dc-to-dc converters which are widely used in power processing applications fall within one of two families, namely, the buck-derived family and the boost-derived family. Each family is characterized by an equivalent averaged circuit model which exposes quite clearly the fundamental properties essential to the respective classes of converters. For example, the control-to-output transfer property of the boost-derived family of converter circuits exhibits non-minimum phase properties, i.e. a right-half S-plane zero, and two moving poles as the duty-cycle control signal is varied. The buck-derived converters, on the other hand, exhibit a zero and a double-pole which are both stationary. The differences in the fundamental properties that divide these two converter families are essential to the determination of a control strategy that assures loop stability and optimizes the dynamic responses.

Based on this classification scheme, a third class of hybrid converters that share the properties of both buck and boost converters has become evident. The familiar buck/boost converter and Ćuk converter, for example, belong to the hybrid family. Through the introduction of the principle of duality relationship and bilateral inversion, a framework is established which makes evident natural relationships between converter families and enables a methodical transfer of knowledge gained about one family of converters to its dual counterpart. As a result of this classification structure and the duality relationships revealed through it, many new converter topologies are suggested.

Further, the authors present the idea of integrated magnetics and show that various magnetic components in a converter can be integrated in a simple magnetic core structure. It is demonstrated that the integrated magnetic concept can be applied in a generalized fashion to all converter circuits. The simplified magnetic circuits may have a profound impact in future converter design.

I am very pleased to see that the authors have successfully brought together a vast amount of circuit technology in a refreshing and well organized manner. This book, with its emphasis on switching mode power supply design and topology selection, will assist experienced design engineers and help to bring novices up to speed. Congratulations, Rudy and Ed, for a job well done.

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Preface

From the everyday tools of science and business to the toys our children play with, no modern electronic product today goes untouched by the enormous strides made in microelectronic design technology over the past two and one-half decades. However, with each significant advance in micro-miniaturization of electronic systems has come a serious challenge to the designer of associated power processing networks to follow suit. These challenges are particularly difficult for those of us who must answer their call, for power processing techniques, as we know them today, are inherently discrete, by necessity physically larger than a user electronic system, and often wasteful in energy required to perform the processing or conditioning needed. This latter fact is especially true of those power processing schemes which utilize linear dissipative circuit approaches.

As the sizes of electronic systems began to shrink twenty years ago, it soon became very clear that bulky dissipative methods for power processing and conditioning would have to be replaced by more efficient and space-saving design techniques if overall product miniaturization was ever to be optimized. As a result, a new power electronics design specialty began to evolve, which has come to be known as the design of power conversion equipment using switch-mode power processing in conjunction with modern power semiconductors.

While the antecedents of this electronic design specialty clearly go back much earlier in time, it was the development of modern power semiconductors and the need for lightweight and efficient power processing equipment for space exploration programs that provided the initial impetus to explore and develop switch-mode conversion techniques. As is so often the case, it wasn't very long before military and, finally, commerical applications were being found for these switch-mode converter circuits (SPCs). In fact, today, in both dollar volume and unit numbers, the commercial use of SPCs has completely eclipsed their application in military and space electronic systems.

As a result of the widespread acceptance of SPCs, significant numbers of electronic engineers are now engaged in their design and application. It is not very surprising, given the ingenuity of the average electronic engineer, that literally

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hundreds of SPC circuit variations exist, all of which can be used for electrical power processing. In addition, much has been learned about the fundamental behavior of these circuits. Most of their basic behavior can be presented rather simply, and in a manner which is of great practical interest to circuit designers.

A basic educational problem facing an electronics engineer new to this field has been the scattering of information concerned with the design of SPCs in hundreds of publications, patents, technical papers, correspondence internal to electronic firms, private memoranda, and other scientific reporting media. As a result, only a small portion of the practical information related to this specialty is common knowledge and in general use.

Because there is such a limited pool of public knowledge in this design art, 95% of SPC designs now in service use one of six topologies, or variations thereof, to perform the desired power processing. While these conventional circuit approaches have served well and are useful for many applications, they represent only a few out of literally hundreds of possibilities. Also, these few circuits are not necessarily the best choice for many of the applications in which they are being used.

Another effect of limited knowledge is the poor transient response of many converter systems to both input line and output load changes. This is frequently due to a less than complete understanding by designers of small-signal modeling and analysis methods for SPC circuits. This problem is so widespread that many SPC system designers and their users automatically assume that poor transient response is an inherent characteristic of these circuits when, in actuality, nothing could be further from the truth. Significant improvements in the methods of modeling and small signal characterization of SPC circuits have been made in the last ten years and highly accurate and easily applied representations are now possible. The combination of good dynamic system models, multi-loop control schemes, and high frequency switching can provide SPCs with transient response characteristics that rival conventional linear dissipative circuits.

The wide acceptance of SPC technology has led to an incredible variety of applications, many of which impose severe requirements. More often than not, today's SPC designer is faced with performance requirements that can only be fulfilled by circuit designs which fully exploit state-of-the-art technology. The old "business-as-usual" approach, employing one or two SPC circuit variations for all applications, is no longer viable. Increasing the output power level quickly brings the designer face-to-face with component stress limitations in conventional SPC topologies. The seemingly endless quest for physically smaller SPC systems often forces designers to use power switching rates in the hundreds of kilohertz to reduce size, a practice generally unheard of until the late 1970s. When properly and thoughtfully applied, the use of alternate circuit topologies can be a powerful tool for circumventing the problems presented by circuit component limitations as well as by operation at extraordinarily high frequencies.

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New and more energy efficient power components continue to be developed and are finding widespread acceptance by SPC designers. The metal oxide semiconductor field effect transistor (MOSFET) is a prime example of a new circuit element. While power MOSFETs can be successfully used in any conventional SPC circuit, alternative circuit topologies exist that take full advantage of the capabilities of these new semiconductors.

The motivation for this book is to gather as much of the current design knowledge concerning SPC circuits as possible in one place, and to present that knowledge in a direct and unified manner. Because the amount of available information is really quite voluminous, it is neither possible nor practical to restrict it to the contents of a single book. Therefore, in this text, we will restrict the discussion to the fundamental behavior and characteristics of SPCs and the many topological possibilities. The information presented herein is, in our opinion, that which is of the greatest utility to the designer of SPC circuits and systems. Therefore, we have deferred detailed discussion of component selection and the comprehensive design aspect of related system regulatory control to future texts in this power electronics series.

If we examine the present state of our understanding of SPC circuits, many gaps are readily discernible. In particular, a quantitative and accurate means for modeling and characterizing the large signal dynamic behavior of these circuits is still very much missing, although a concerted research and development effort is now in process to fill this void in our knowledge. It is very tempting to delay writing a book such as this one until all pieces of the SPC design puzzle have been found and put into place. No doubt, in a few years when the design art of SPCs has reached a level of considerable maturity, some excellent and highly definitive texts will be written on the subject. Unfortunately, many of us cannot afford to wait that long. So, despite its shortcomings, this text will still provide a broad introduction into the basic operation and characteristics of SPCs as well as into many of the more advanced aspects of SPC design.

This book is intended to be used both by electronics engineers just beginning to design SPC circuits and the old hands who have many years of experience in the field. Each will find much information which is useful for solving practical design problems. The text of the book is divided into two major sections. Section I (Chapters 1 through 11) presents the basic theory of SPC circuits as we understand them at this point in time. The presentation is straightforward with a minimum use of mathematics throughout, although some mathematical exercise is required in Chapters 2, 3, and 10 to support the ideas therein.

The discussions of Section I begin with the detailed exploration of two elementary SPC circuits to determine their large and small signal characteristics, and then builds progressively from these basic circuits to much more complex ones by using combinations of the basic circuits in conjunction with synthesis techniques.

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The discussions of Section I assume the point of view that the desired power processing is voltage-related, that is, a voltage converter. This point of view could have just as well been current conversion-oriented and, in fact, we will see in Chapter 9 that these two points of view are duals electrically. The reason we have selected to pursue the voltage option is simply that this is by far the most common electrical conversion requirement encountered by SPC designers. The reader who has a need for a current converter should read Chapter 9 carefully, keeping in mind that the principles presented in that chapter can be applied to his requirement by the use of simple electrical duality relationships. Section I ends by discussing methods for comparing the relative merits of the multitude of SPC circuit topologies.

Section II (Chapter 12) is devoted to the examination of a variety of unique SPC circuits that fall into a special category of designs. This particular category encompasses converters whose primary inductive and transformer elements have been integrated (i.e., combined) into single physical assemblies. In many cases, the designs shown in Chapter 12, along with the methods behind the magnetic integration process, have never been shown or discussed before in any publication. Also contained in Chapter 12 is a brief review of magnetic fundamentals important to the understanding by the reader of the integration methods presented.

To further assist the reader, an extensive bibliography and lists of suggested reading materials has been included at the end of the book for reference and research purposes. We would like to acknowledge that only a portion of this book represents original contribution by the authors to the art of SPC design, with much of the information presented derived from the efforts of many others. The bibliography and reading list are attempts to acknowledge this fact. Of course, no practical reference list can ever be complete and, no doubt, many original contributions have been overlooked. To those individuals we have unintentionally omitted in this listing, we offer our sincere apologies for the oversight.

There are many individual researchers in the power electronics sciences who have distinguished themselves through their efforts to expand the design art of SPCs. In particular, we would like to acknowledge the work of Professor R. D. Middlebrook and his colleagues in the Power Electronics Group at the California Institute of Technology in Pasadena, California. Because of their dedicated research efforts, practical modeling and analysis of SPC systems is now feasible. Also, they have been instrumental in providing power electronics engineers with measurement tools and design techniques that have led to new SPC circuits and to a higher level of understanding of control techniques for SPCs than thought possible ten years ago.

A great deal of individual research into the science of power converter technology was required to write this text, including countless trips to the archives of many technical libraries and to facilities nationwide who maintain up-to-date records of SPC patents. Without the aid and assistance of Joy Bloom in the

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preparation of this material, including over a year's effort of manuscript editing and processing, this book would not have been completed in a timely manner. We are certainly in debt to this very special lady.

Both of us are practicing electronic design engineers and the creation of this book has been an education and often a revelation on the overwhelming possibilities of SPC circuit variations. If reading this book opens up for you the new vistas and possibilities which we have discovered in writing it, then we will feel our efforts have been well spent.

G. E. Bloom
R. P. Severns

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MODERN DC-TO-DC SWITCHMODE POWER CONVERTER CIRCUITS

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1. Introduction to Switchmode Power Converters

In a general sense, a power converter can be defined as a device which converts one form of energy into another on a continuous basis. Any storage or loss of energy within such a system while it is performing its conversion function is usually incidental to the process of energy translation. There are many types of devices which can provide such a function with varying degrees of cost, reliability, complexity and efficiency.

The mechanisms for power conversion can take many basic forms, such as those which are mechanical, electrical, or chemical in processing nature. We will be concerned here only with power converters which perform energy translation electrically and in a dynamic fashion, using the limited variety of components collectively illustrated in Fig. 1.1. How these circuit components are interconnected will be determined by the power translation desired. We restrict our choice of electrical components to include only inductors, capacitors, transformers, and switches, intentionally omitting resistors because they introduce undesirable power losses. High efficiency is usually an overriding requirement in most applications for electronic switchmode power converter (SPC) circuits, so resistive circuit elements must be avoided. This is not to say that resistances do not exist in SPCs. In their physically realizable forms, none of our chosen circuit components are ideal and all will introduce some resistive loss in the conversion process. However, every effort is made by SPC designers to minimize these parasitic resistances so that their presence and influence on SPC efficiency and conversion performance will not be significant. Only on rare occasions and for very special reasons are power consuming resistances introduced into the main power control paths of an SPC circuit. In auxiliary circuits, such as sequence, monitor, and control electronics of a total SPC system, high value resistors are commonplace, since their loss contributions are usually insignificant.

In SPC circuits, the semiconductor switches controlling the dynamic transfer of power from input to output are either fully ON or fully OFF, with very short transition times from one of these states to the other. Component voltage wave-

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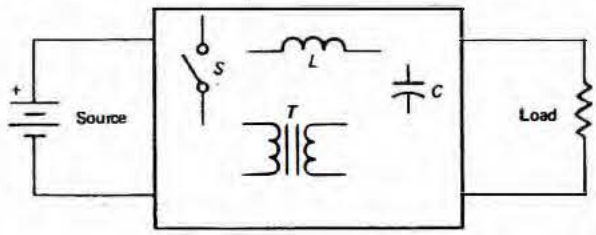


Fig. 1.1. Switchmode power converter components.

form shapes take the forms of either periodic pulse-width-modulated (PWM) rectangles, square waves, or combinations thereof. The associated current waveform shapes are usually triangular to trapezoidal. Semiconductor parts normally employed as switching elements in SPCs are fast recovery diodes, bipolar junction transistors (BJT), metal oxide semiconductor field effect transistors (MOSFET) and gate turn-off thyristors (GTO).

The most general form of the conversion function would be the transformation of a source of polyphase AC potential of one magnitude, phase, and frequency to another magnitude, phase, or frequency. With this concept, a DC input or output of an electrical power converter system can be viewed as AC with zero frequency and phase.

The discussions in this book will be limited to those circuits which perform a dynamic DC to DC (DC-DC) power conversion function. This is not nearly as restrictive a view as it might first appear, since there are a great many applications for a DC-DC SPC. There are also a large number of applications for AC to DC (AC-DC) conversion. This latter function is usually implemented by preceding a DC-DC converter circuit with a simple rectifier-filter network, a typical example of which is shown in Fig. 1.2. DC to AC and AC to AC power converter systems frequently use AC-DC and DC-DC networks as subsystem elements working together to obtain the desired output characteristics.

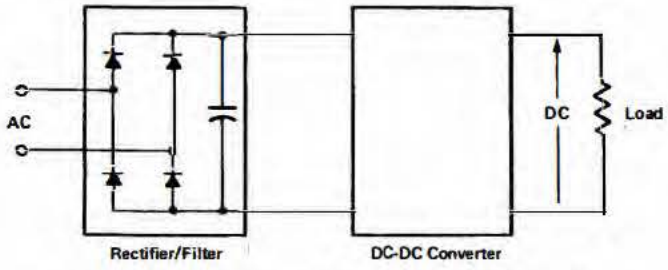


Fig. 1.2. Typical implementation of AC-to-DC conversion.

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It is also interesting to note that many motor control systems use circuit components and topologies that closely resemble DC-DC converters. If we consider the uniform rotary and, in some cases, linear output from a motor to be equivalent to a DC output, then the motor and its controller network can be viewed as a DC-DC or AC-DC converter. It follows then that a great deal of the design technology related to DC-DC converters is directly applicable to motor control electronics. For reasons such as this, a study of DC-DC converters using SPC techniques is very worthwhile and has wide applicability to other related power control disciplines.

Many virtues are expected of electrical power converters. They must be highly efficient, occupy little volume, be low in cost and weight, and have a long service life with no failures. Often their outputs must be regulated to close tolerances, even though their inputs may vary over a very wide range of values. The family of SPC circuits, which we will explore in this text, are able to fulfill these requirements remarkably well, provided their designs are well executed.

Depending on application needs, a DC-DC SPC circuit could be very simple in form, using only one SPDT switch, one inductor, and one capacitor. On the other hand, it may be very complex, utilizing many components to accomplish the required DC conversion function. Regardless of the complexity of a particular SPC circuit, the following key idea always applies:

Key Idea #1

THE INDUCTORS AND CAPACITORS OF A DC-DC SPC MUST, IN SOME MANNER, FORM A LOW-PASS FILTER NETWORK.

The justification for this idea is the need for a DC output voltage with a minimum of superimposed AC ripple from the switching action of an SPC. Since the internal nodal or branch waveforms of an SPC are at some point pulsating with both AC and DC components, a low-pass filter is required to prevent the undesirable AC components produced by SPC switching action from appearing at the output terminals of the converter.

It is not always easy to isolate the low-pass inductive and capacitive filter elements of an SPC from a casual inspection of its circuit diagram, since the effective filter inductor element (or elements) is often separated from the filter capacitor element (or elements) by switches and/or transformers. In the modeling processes to be discussed in Chapters 2, 3, and 10, we will invariably derive an equivalent low-pass filter network for each converter type. The most common circuits have a single-section low-pass filter. However, there are some special SPC circuits (such as the Ćuk SPC) which contain multiple-section equivalent filter networks.

Two of the simplest SPCs are shown in Figs. 1.3 and 1.4, along with physical realizations for their SPDT switch functions (Figs. 1.3B and 1.4B). The circuit

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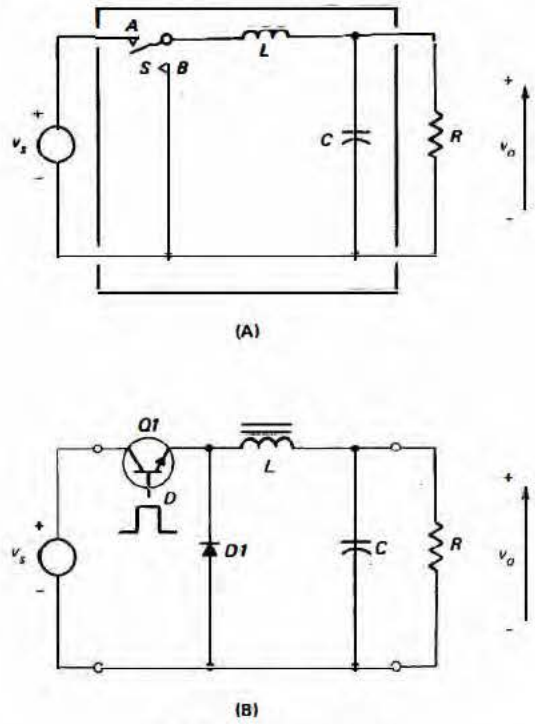
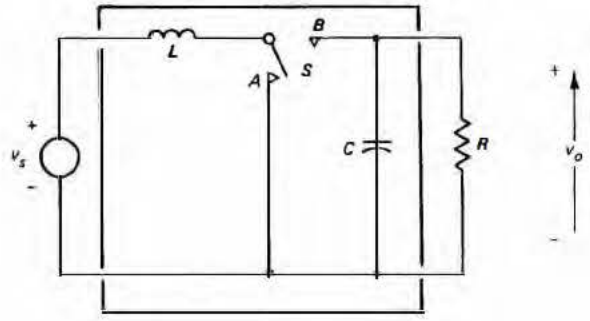


Fig. 1.3. The buck converter.

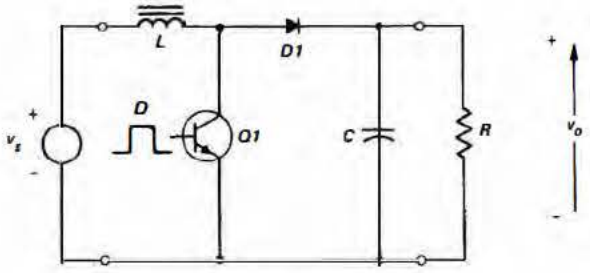
in Fig. 1.3 is called a buck (step-down) converter because the output voltage is always less than the input voltage. The circuit of Fig. 1.4 is referred to as a boost (step-up) converter because its output voltage is always greater than the input voltage.

One point should be made here. The output capacitor (C) in the buck converter is not absolutely essential for the circuit to function properly, since its inductor (L) and load resistor (R) form a low-pass filter by themselves and, in theory at least, L can be made arbitrarily large in value to produce a small ripple current in R. However, even the presence of a small amount of output capacitance will greatly reduce the size of L required to obtain a DC output voltage across R with a minimal AC ripple. In actual practice, C is rarely omitted. For this reason, we will assume that the basic buck converter will usually possess an output filter capacitor. On the other hand, the output capacitor of the boost converter cannot be omitted, since the output current will always be pulsating even if the inductor is infinitely large. Thus, to obtain a low-ripple output voltage,

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(A)



(B)

Fig. 1.4. The boost converter.

a filter capacitor is always necessary across the output terminals of a boost converter.

We will now put forward a number of additional key ideas regarding SPCs in general.

Key Idea #2

ALL KNOWN DC-DC SPC CIRCUITS CAN BE DERIVED FROM COMBINATIONS OF BUCK AND/OR BOOST CONVERTERS ALONG WITH SOME FORM OF TRANSFORMATION FUNCTION.

The transformation function is shown in a general fashion in Fig. 1.5A, and can be characterized as an ideal transformer element, as illustrated in Fig. 1.5B. Because of its ideal properties, such an element can transform DC as well as AC.

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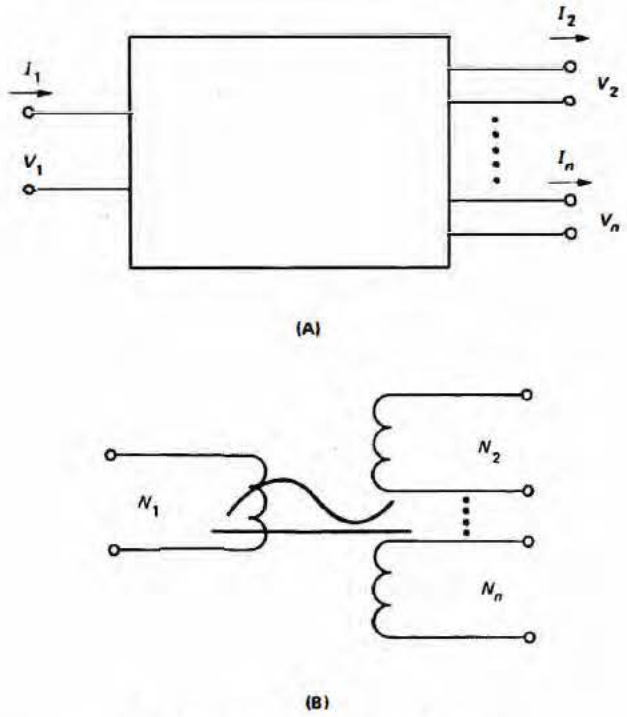


Fig. 1.5. The ideal transformation function.

Obviously, an ideal transformer element would be very difficult to realize in actual practice. Fortunately, perfection is not usually required in transforming voltages and currents within SPCs, and there are many practical design approximations which serve quite well. This subject of both DC and AC transformation will be treated in more detail in Chapter 4.

The justification for the assertion in Key Idea #2 is strictly empirical, i.e., no SPC circuit known at this point in time is so complex that it cannot be reduced to a combination of these elementary circuits. In the discussion that follows, the truth of this key idea is assumed and the structure of this book is organized in accordance with this premise. Chapters 2 through 4 will examine the two basic SPC converter circuits and transformation elements in great detail. That material will then be used in later chapters to examine more complex converter structures.

A third key idea is directly related to the second one:

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Key Idea #3

THE PROPERTIES OF BASIC CONSTITUENT CONVERTERS (i.e., buck and/or boost) ARE RETAINED IN ANY COMPLEX DERIVATIVE CONVERTER SYSTEM.

This key idea holds for the majority of complex SPCs, with the exception of a few converter circuits which use tapped inductors and transformers with equal turns ratios between windings. In some of these special converters, basic behavior patterns are modified to some extent. This subject is discussed in Chapter 10. Except for these special exceptions, the above idea is sound and the general properties of a complex SPC can be readily predicted from a knowledge of its basic constituents. This ability to directly relate circuit properties of many SPCs is a valuable tool in comparing the merits of more complex circuits.

For example, if one needs an SPC with inrush and short-circuit current control capabilities like those exhibited by a buck SPC, he must use an SPC topology that is buck-derived. By its very nature, an unmodified boost-derived converter cannot provide such current-control features. When one attempts to modify a boost-derived converter to include these features, one of two things will happen. The modified circuit will either become a buck-derived SPC or it will exhibit either buck-derived or boost-derived characteristics, depending on input voltage and output current magnitudes. Examples of SPCs which can have this type of dual personality are discussed in more detail in Chapter 9.

A fourth key idea which is of practical importance to an SPC designer is:

Key Idea #4

NO SINGLE SPC CIRCUIT TOPOLOGY IS ELECTRICALLY IDEAL FOR ALL APPLICATIONS. IT IS THE PARTICULAR APPLICATION WITH ITS INDIVIDUAL REQUIREMENTS THAT DETERMINES WHICH CIRCUIT WILL BE THE BEST TO USE.

This may seem to be a very obvious, almost trivial statement. However, even a brief look at the claims (and often the practice) within the power electronics industry will reveal that this simple truth is not universally appreciated nor accepted. If this key idea were not true, then this book would be dedicated to the discussion of the one most perfect circuit for all situations.

SPC circuits do exist which have been very carefully synthesized to have as many desirable and as few undesirable characteristics as possible. The Ćuk SPC circuit and its variations discussed in Chapter 7 are good examples. To an amazing degree, concerted efforts such as these have succeeded in producing designs

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which are near optimum for many applications. Despite these successes, however, SPC circuits such as the Ćuk versions are still not optimum for *all* applications.

What makes Key Idea #4 so important is the fact that even relatively small changes in SPC circuit topology often lead to significant alterations in component stresses, or changes in dynamic control-related characteristics, such that desired conversion properties might be severely compromised. On the other hand, SPC circuit topology alteration can be an effective tool for circumventing design difficulties created by the limitations and nonideal properties of components. Therefore, it is up to the designer to make the proper choice of alteration, always keeping in mind the pros and cons of his actions.

SPCs may be categorized by their general output characteristics. Sometimes, this can be most helpful to the user in defining the application requirements that must be met by an SPC. Fig. 1.6A shows a general converter system in block form, along with output voltage (V) and current (I) defined as illustrated. Fig 1.6B gives the possible directional combinations of V and I, where each quadrant

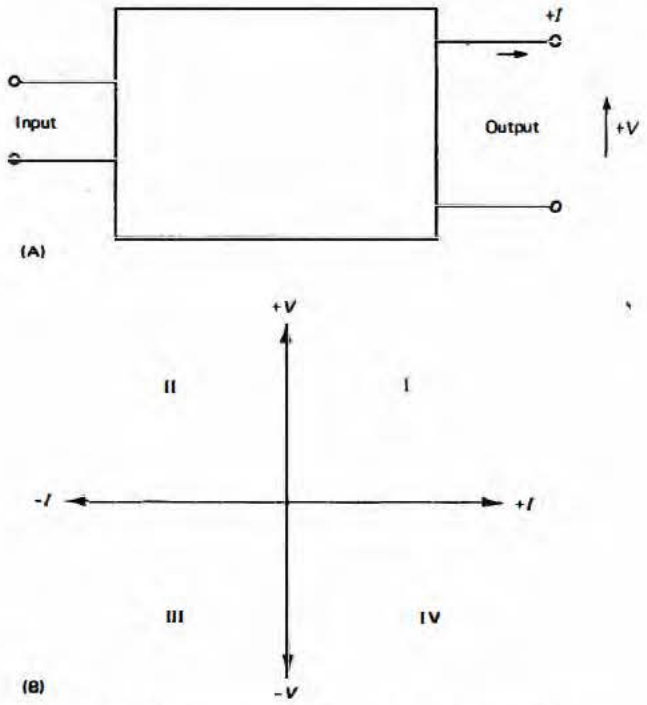


Fig. 1.6. The converter output operating quadrant concept.

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is identified by sign. In a simple DC-DC converter with unidirectional power flow (input-to-output), the output is constrained to lie in either quadrant I or quadrant III of Fig. 1.6B, depending on the desired output voltage and current polarity. This is an example of single-quadrant operation. In battery charger/discharger applications, the polarity of the converters' output potentials are fixed in sign, but their output currents may be either positive or negative in directional flow. Thus, their output characteristics must lie either in quadrants I and II or quadrants III and IV of Fig. 1.6B. This is an example of two-quadrant operation, where the power flow must be bidirectional. AC output of an SPC would also be a two-quadrant operational system. In the most general case, a converter with AC output and bidirectional power flow capability must operate in all four quadrants of Fig. 1.6B.

Before proceeding to the detailed circuit discussions of the next chapters, let us pause and review the terminology that we will be using in the text. Unfortunately, even among power electronics engineers, there is no universally accepted terminology for SPC circuit names and their operational modes, much less their origins. The present authors have taken the liberty of adopting terminology for this text which pleases us, and admittedly some of our choices are arbitrary. If the reader has adopted other conventions of terminology, he should have little difficulty in interpreting the descriptions to follow.

SPCs are often referred to as switching regulators, especially by their users. Most SPC *systems* do contain auxiliary control or regulating electronics to provide a constant output voltage with varying output load and input voltage—hence, the appellation *switching regulator*. In this text, we will discuss the power stages of switching regulators and refer to them as SPCs.

The word *converter* is used here in its general sense, referring to a physical system that is capable of converting electrical power of one form to another form, regardless of whether its inputs and/or outputs are AC or DC in nature. This same term is sometimes used in a more restricted sense to indicate that its input and output characteristics are the same form of power, i.e., AC-AC or DC-DC. The name *inverter* is used when DC-AC or AC-AC power conversion is implied. Since we are restricting the discussions of this text to DC-DC SPCs, these latter distinctions will not be needed.

Alternative names exist for the *buck* SPC. It is not uncommon to hear this basic SPC circuit referred to as a *voltage step-down converter*, *buck regulator*, or a *chopper converter*. The term *chopper* comes from the dynamic action of the SPDT switch within the converter which produces a "chopped" voltage at the input to its low-pass filter network.

Boost converters and their basic first-order derivatives also have other names by which they are known. These names include *ringing choke*, *flyback* or *voltage step-up* converters. The term *flyback* is particularly confusing, since the same term is often applied indiscriminately by designers in discussing three very

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different SPC circuits–the basic boost converter structure, a converter system which combines a buck and a boost converter in cascade, and a transformer-coupled version of a cascaded buck and boost converter network. In this text, the name *flyback* will be applied only to the last of the three alternative SPC circuits.

Buck and boost SPCs are frequently referred to as buck and boost regulators, respectively, since they are primarily used as the power stages of such regulation systems. For simplicity, we have chosen not to include these names as terms of the discussions of this text as was stated earlier in this chapter.

The adjectives *buck-derived* and *boost-derived* will be used quite frequently in the chapters to follow. When applied to a given circuit under consideration, they imply that it has been derived in some relatively direct manner from either a basic buck or a basic boost converter, respectively, and that the general properties of the parent converter have been retained. These descriptive terms will become very important as the process of evolution of large numbers of different converter topologies begins and the need to categorize them becomes evident in order to simplify the processes for application selection.

Lastly, the *switching frequency* (f_s) of an SPC circuit will be defined to mean the rate at which all of its circuit switches complete one full switching cycle of their operation. It is important that the switching frequency of an SPC not be confused with AC output voltage or *current ripple frequencies* (f_r) for, more often than not, f_r is an integer multiple of f_s. In the two basic SPC circuits to be examined in the next two chapters, their input, as well as output, ripple current frequencies are equal to the basic SPC switching frequency. However, in many other SPCs, the ripple frequencies of voltages and currents can be many times higher than the associated SPC switching frequency.

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2. The Buck Converter

The first of the elementary switchmode power converters (SPCs) that we will examine is the buck converter. The goal of the analyses of this chapter, as well as the next one, is to develop mathematical and equivalent circuit models that adequately represent circuit operation and to quantitatively determine essential electrical characteristics required for proper design. In the analysis process, we will derive most of the expressions from which numerical values for circuit performance and component stresses may be computed.

A highly desirable feature of any electrical circuit model is that it be readily manipulated using the techniques of linear circuit analysis and synthesis familiar to electrical engineers. Unfortunately, SPC circuits are nonlinear and discontinuous by their very nature, and, as such, are very cumbersome to analyze directly using standard linear circuit theory. A major part of this chapter is therefore devoted to "linearizing" the buck converter circuit model so that it can be easily analyzed. The linearizing process does involve a slight compromise in accuracy, but for most of the quantities we are seeking, the accuracy of the model is more than adequate for normal design purposes.

The models to be derived must possess many other virtues as well. An SPC is rarely used as a power processing system unto itself. There are usually additional networks such as sequence, monitor, and control electronics along with input and output filters for EMI noise suppression. Sometimes an SPC will be used in conjunction with other converter circuits. For reasons such as these, any SPC models of practical use must be able to accommodate any additional circuit elements as easily as possible.

Another constraint placed on our SPC models is the need to recognize the nonideal character of real circuit components, such as inductor winding resistance and core loss or the equivalent series resistance (ESR) of filter capacitors, and to be able to insert these parasitic elements into the models without undue complexity in the incorporation process.

Finally, our models must be sufficiently easy to use, so that they can be applied easily by the SPC designer in his work. A model, regardless of how accurate it may be, cannot be a general purpose design tool if many hours of calculation are

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required to generate the desired information. An SPC is expected to be efficient in its translation of power, and no less can be expected of its modeling abilities from a time viewpoint. The models that we will derive in this chapter and in Chapter 3 meet these requirements amazingly well.

The following modeling discussion tries to minimize the use of mathematics. As a result, some basic assumptions have been glossed over and most theoretical derivations have been omitted. For the reader who may be interested in these mathematical details, an excellent exposition of state-space averaging is given in Refs. 1 and 2 in the text bibliography of this book.

We begin by taking a very simple look in Section 2.1 at the circuit operation and waveforms for an ideal buck converter. Then, in Section 2.2, equations for the large-signal steady-state behavior for both conduction modes of this SPC will be presented. Section 2.3 will review the circuit's large-signal dynamic characterization. In Section 2.4, we will derive the small-signal characterization as well as a circuit model for the continuous mode of the buck SPC, using the state-space averaging technique. Parasitic elements will be included in this small-signal model. Finally, in Section 2.5, we will examine the operation of an ideal buck converter in a discontinuous mode situation and, once again using the methods of state-space averaging, derive the describing equations and a circuit model for this second operating mode.

The discussion of Section 2.4 is intended to demonstrate the procedure of state-space averaging. While this procedure is somewhat involved (and is really an overkill for the simple case of an ideal buck SPC), it is important to familiarize ourselves with these methods, as they are the only practical means for modeling both the discontinuous mode of a buck SPC and all modes of operation of a boost converter.

A basic assumption throughout the analysis to follow is that the output voltage ripple of the SPC is small. This is equivalent to saying that the output filter corner frequency (f_c) is much lower than the switching frequency (f_s). This assumption is one of the key means by which a linear SPC circuit model can be formulated and is fundamental to the principles of state-space averaging. Fortunately, the assertion that f_s is much greater than f_c is valid for any SPC producing a DC output with low AC ripple content.

2.1. BUCK CONVERTER OPERATION

An idealized circuit for the switch states of a buck SPC is shown in Figs. 2.1B and 2.1C, along with a practical realization for the SPDT switch in Fig. 2.1D. Corresponding typical waveforms for the ideal buck converter of Fig. 2.1A are diagrammed in Figs. 2.2 and 2.3.

During the switching cycle, the SPDT switch (S) moves between positions A and B, so that the circuit topology alternates states between that of Fig. 2.1B and that of 2.1C. At the beginning of a switching cycle (t_0), S is in position A, the

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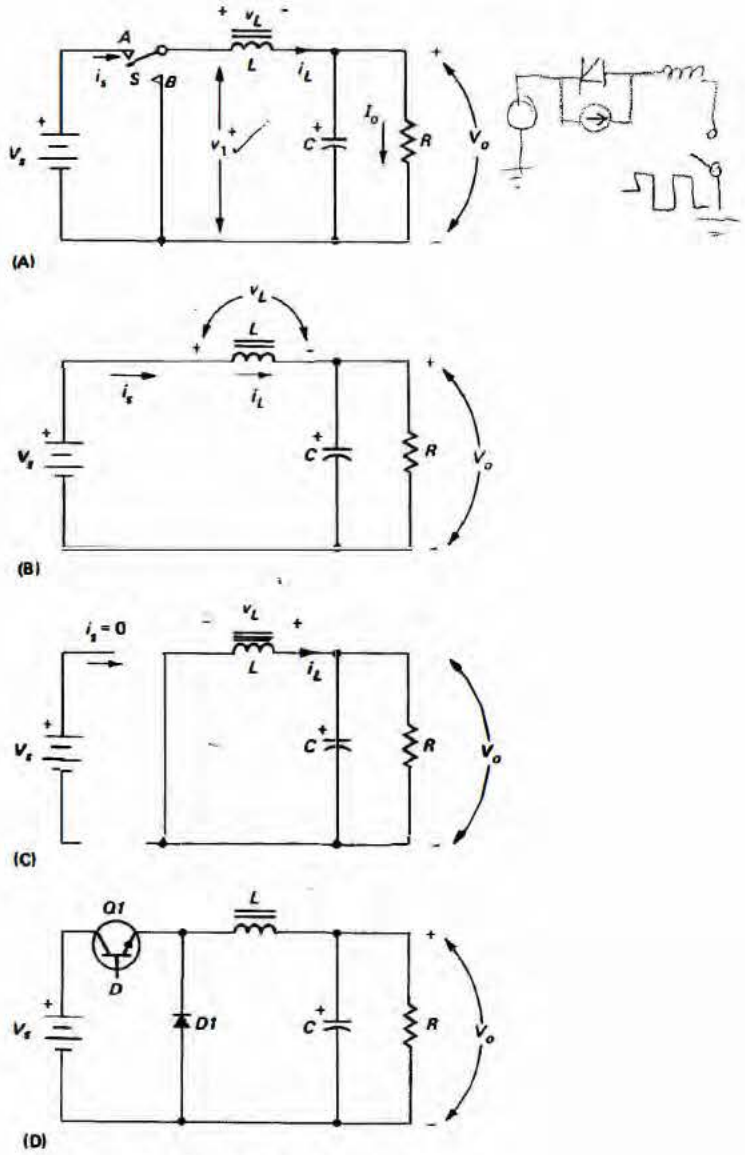


Fig. 2.1 The buck converter.

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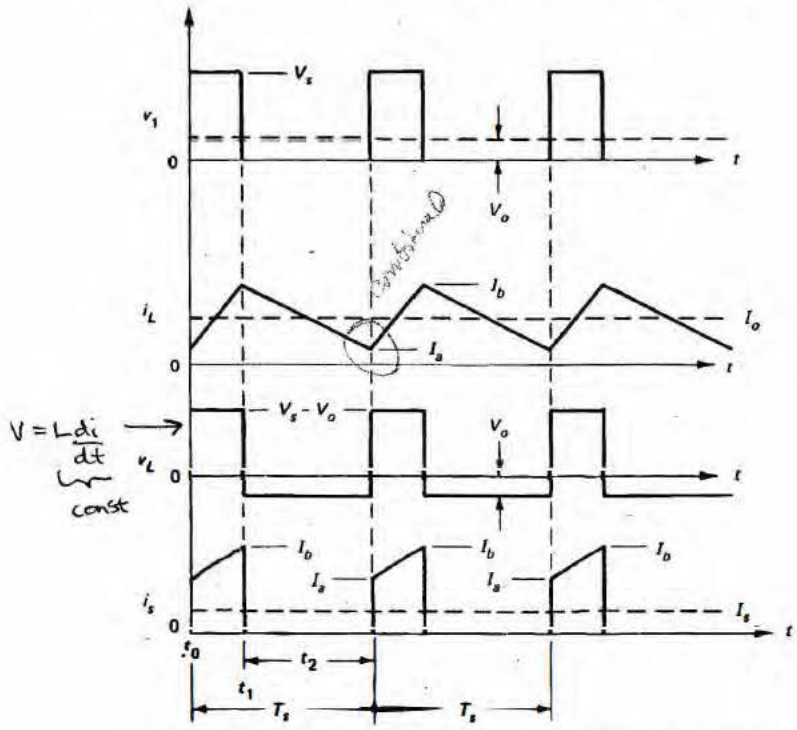


Fig. 2.2. Buck converter waveforms for the continuous mode of operation.

input voltage (V_s) is greater than the output voltage (V_o), and the current (i_L) in the inductor (L) ramps upward during the interval t_1, as shown in Fig. 2.2.

The inductor current will continue to ramp upward until S changes to position B. When S moves to position B, at $t = t_1$, $V_s = 0$ and the voltage across L changes sign with i_L ramping downward. Two inductor current possibilities now exist at the end of interval t_2; either $i_L = 0$ or $i_L = I_a$, some nonzero positive value. In other words, either all of the energy stored in L is delivered to the load between t_1 and t_2 or some energy remains as S moves back to position A.

This defines the two basic operating conditions for the buck SPC and leads to a key idea about SPC operating modes:

MODE 1. Continuous inductor current during the entire switching cycle (continuous mode operation).

MODE 2. Discontinuous inductor current during the switching cycle (discontinuous mode operation).

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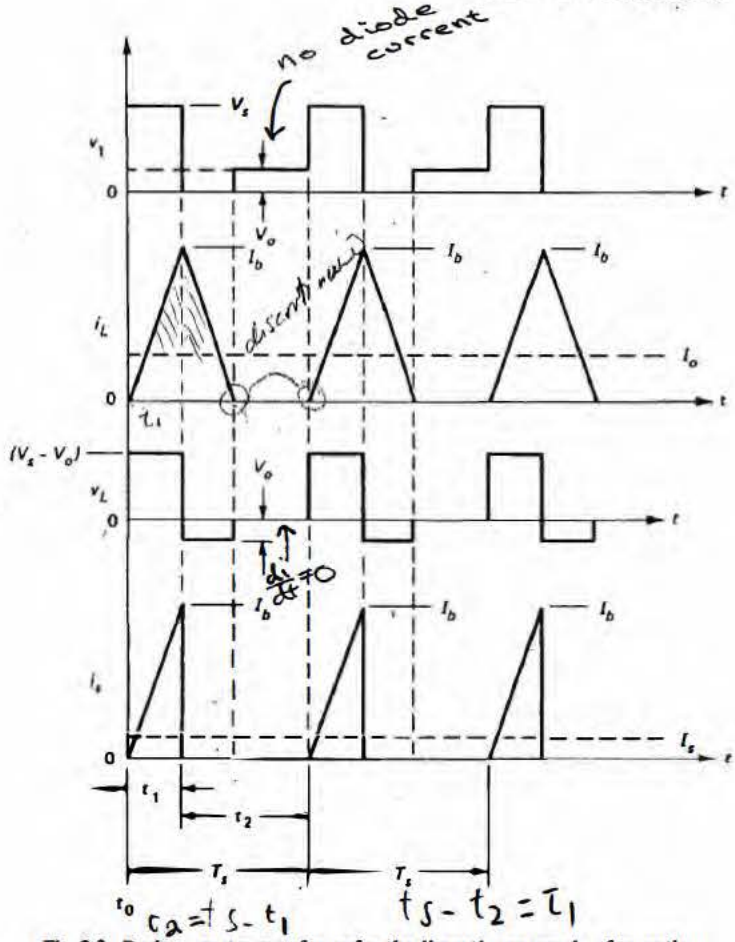


Fig. 2.3. Buck converter waveforms for the discontinuous mode of operation.

Key Idea #5

THE CONDUCTION MODE OF THE INDUCTOR CURRENT IS A FUNDAMENTAL FACTOR IN DETERMINING THE ELECTRICAL CHARACTERISTICS OF ANY SPC.

If one were to place two topologically identical SPCs in separate black boxes, the only difference between them being that the value of the inductor of one is chosen so the converter operates in the continuous mode and the other inductor chosen such that its SPC operates in the discontinuous mode, a series of

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tests on each SPC to determine output electrical characteristics would conclude that the two boxes contained entirely different converter circuits. The inductor current conduction modes of the basic SPCs (as well as any complex derivatives) have a profound effect on their conversion characteristics and are as important to know as their topological structures when determining circuit performance.

The *duty cycle* (D) is defined as:

$$D \equiv \frac{t_1}{T_s} = t_1 f_s \,. \tag{2.1}$$

For fixed values of L and D, the mode in which the buck converter operates is determined by the value of R. As R is increased in ohmic value, the operating mode will change from continuous to discontinuous. On the other hand, if R and D are fixed, the operating mode will change from continuous to discontinuous as the inductance of L is decreased. As f_s is increased, the minimum value of L to maintain the SPC in a continuous mode of operation will decrease in direct proportion to the change in f_s.

As this discussion proceeds, it will become apparent that, for many applications such as those where high-power or multiple outputs from an SPC are required, maintaining the SPC in a continuous mode of operation is very desirable, even for large variations in load resistances. To avoid using an excessively large value of L to maintain continuous current levels at light output loads, a "swinging" choke is sometimes employed. A swinging choke is an inductance whose value is a function of the current passing through it, being large at low current and getting progressively smaller as the current is increased. While this technique can be very useful, a swinging inductance will complicate the analysis of the SPC by making f_c of its associated filter variable with load resistance. This may make the stabilization of any associated regulatory control loop somewhat more difficult.

One can deduce many of the properties characteristic of a buck SPC and its more complex derivatives by examining its electrical waveforms, such as those plotted in Figs. 2.2 and 2.3.

V_o is the average voltage value of v_1 so this converter can be simply viewed as a voltage chopper followed by a low-pass filter. Voltage v_1 is composed of both AC and DC components. Since its DC voltage component is the desired output of the converter, the low-pass filter must remove any AC component of this time-varying potential. This implies that f_c of the output low-pass filter must be much less than f_s. Because V_o is the average of v_1, V_o must *always* be less than the input DC voltage (V_s) to this SPC.

Notice also that the waveform for v_1 differs in shape for each of the two modes of operation. In the continuous mode, $v_1 = V_s$ during t_1, and $v_1 = 0$ during the entire period t_2. The average value of v_1 (V_o) is determined by D only

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and, ideally, V_O would be independent of R in this mode. In the discontinuous mode, however, v_1 can be either zero or equal to V_o during time t_2. The length of time spent by v_1 in a zero-value condition during t_2 is determined by R. The value of V_O is now dependent on R as well as D. A close examination of the v_1 waveforms in Figs. 2.2 and 2.3 shows that, for the same value of V_s and D, V_o was increased in the discontinuous mode. Figs, 2.2 and 2.3 have been scaled so that both SPC output power levels are the same in value.

The input current (i_s) is always pulsating, regardless of the operating mode of the buck SPC. Most applications limit (often severely) the amount of pulsating current that can be drawn by an SPC from its source of power. In normal practice, some form of a low-pass filter network is inserted between the source of power and the input terminals of the SPC. As will be shown in Chapter 10, the presence of such a filter must be accounted for at an early stage of SPC design and modeling process. Failure to do so can result in a very unpleasant surprise in the form of self-oscillations when the SPC and the input low-pass filter circuit are united.

The average value of i_s is determined both by V_o and R. In an ideal buck converter with no power losses, efficiency (η) of power conversion is 100%. Therefore,

$$V_s I_s = \frac{V_o^2}{R}, \quad \eta = 100\%. \tag{2.2}$$

For the normal case with a constant value of V_o, $V_o^2 = K$.

In this instance,

$$I_s = \frac{K}{V_s R}. \tag{2.3}$$

Here, the average input current value is inversely proportional to both V_s and R. However, the pulsating value for i_s is determined by i_L, which, in turn, is a function of R, but *not* V_s. As V_s is varied and D altered to maintain a constant V_o, the width of i_s is altered, but *not* its maximum amplitude I_b.

The current i_s is the input switch current, and it can be seen from Figs. 2.2 and 2.3 that, for a constant value of input power, the peak magnitude of i_s is much higher when the buck SPC is operating in a discontinuous mode of operation. In a practical realization of the SPDT switch as shown in Fig. 2.1D, both the BJT ($S1$) and the diode ($D1$) must possess a much higher peak-power handling capability if SPC operation in the discontinuous mode is desired. For this and many other important reasons, continuous mode of operation of buck SPCs is normally preferred in high-power applications, even though their inductances must be larger and therefore, heavier and certainly more expensive.

The output filter cutoff frequency is defined as

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$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{2.4}$$

and it would appear that L can be chosen to be just large enough to maintain the SPC in a continuous mode, with C then selected to provide the degree of output filtering desired. Unfortunately, capacitors are not perfect electrical elements and some power will be dissipated in their ESR. The ESR voltage drop produces an output ripple voltage that can only be reduced by lowering ESR magnitude or the dynamic capacitor current causing the ripple. The size of C is more often determined by the ripple current magnitude than by the value desired for f_c. Making L larger reduces the output ripple current value which, in turn, reduces C. In actual design practice, there is usually a tradeoff made in selecting L and C for weight and size plus cost reasons. In high-power converters, such tradeoffs normally result in a value selection for L which places the SPC circuit operating well into the continuous mode at full load.

Ideally, the output current (I_o) of the buck SPC is not a pulsating quantity since the ripple content of i_L is small in the continuous mode. This is a convenient feature for many applications and, frequently, additional output filtering can be either dispensed with or made quite small.

2.2 STEADY-STATE LARGE-SIGNAL CHARACTERIZATION

To design a converter, it is necessary to quantify many of the circuit characteristics, such as the AC and DC currents flowing through its circuit elements, the voltages across these elements, the input-to-output voltage transfer ratio as a function of D, and many other factors.

The following discussion presents equations and graphs that describe the large-signal steady-state (DC) characteristics of a buck SPC. The analysis presumes an ideal buck SPC, i.e., no parasitic elements such as inductor series resistance (R_L) or capacitor ESR (R_c) are included. Despite this limitation, the equations presented still have more than adequate accuracy for practical design purposes. For an SPC to be efficient, R_L and R_c must be made small. Designers often go to great lengths to minimize lossy parasitic elements when engineering SPC circuits. Therefore, their omission from the following model derivation is justified as a matter of good design practice.

Figure 2.4 illustrates the buck SPC for which the equations in Tables 2.1 and 2.2 apply. An input filter network has been included (*L1*, *C1*), and it is presumed that *L1* possesses sufficient inductance so that I_s is essentially DC. On the output side, *C2* is assumed to be high in capacitance, so that the AC component of I_L flows only through this filter element. Both of these assumptions are consistent with practical application requirements of SPCs for both low input current ripple and small output voltage ripple.

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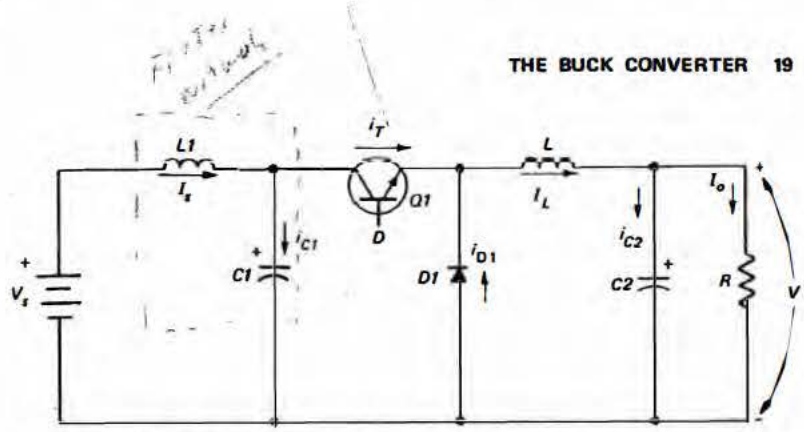


Fig. 2.4. Definition of the buck converter component currents.

For the equations shown in Tables 2.1 and 2.2, and later in Table 2.3, the following definitions apply:

$$D \equiv D_1 = \frac{t_1}{T_s} \text{ (switch conduction duty cycle)} \tag{2.5}$$

$$M = \frac{V}{V_s} \text{ (input-to-output DC transfer ratio)} \tag{2.6}$$

$$\tau_L \equiv \frac{L}{RT_s} \text{ (normalized inductor time constant)} \tag{2.7}$$

$$I_o = \frac{V}{R} \text{ (DC output current)} \tag{2.8}$$

TABLE 2.1A. Definitions of Variables for the Buck Converter Equations.

τ_L	L/RT_s
T_s	Switching period
τ_{LC}	L_c/RT_s
L_c	Critical inductance
τ_{LC}	$(1-M)/2$
D_1	Switch ON duty cycle
D_2	Diode conduction duty cycle
M	V/V_s
I_a	Minimum inductor current
I_b	Maximum inductor current

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TABLE 2.1B. Buck Converter Equations for Continuous Inductor Current.

Dependent Variable	$f(M, \tau_L, V, R)$	$f(D_1, \tau_L, V, R)$
M	M	D_1
D_1	M	D_1
D_2	$1 - M$	$1 - D_1$
I_a ($I_{L(\min)}$)	$\frac{V}{R}\left[1 - \left(\frac{1-M}{2\tau_L}\right)\right]$	$\frac{V}{R}\left[1 - \left(\frac{1-D_1}{2\tau_L}\right)\right]$
I_b ($I_{L(\max)}$)	$\frac{V}{R}\left[1 + \left(\frac{1-M}{2\tau_L}\right)\right]$	$\frac{V}{R}\left[1 + \left(\frac{1-D_1}{2\tau_L}\right)\right]$
$I_{L(\text{avg})}$	$\frac{V}{R}$	$\frac{V}{R}$
$I_{L(\text{rms})}$	$\frac{V}{R}\left[1 + \frac{1}{12}\left(\frac{1-M}{\tau_L}\right)^2\right]^{1/2}$	$\frac{V}{R}\left[1 + \frac{1}{12}\left(\frac{1-D_1}{\tau_L}\right)^2\right]^{1/2}$
$I_{C1(\text{rms})}$	$\frac{V}{R}\left\{M\left[(1-M) + \frac{1}{12}\left(\frac{1-M}{\tau_L}\right)^2\right]\right\}^{1/2}$	$\frac{V}{R}\left\{D_1\left[(1-D_1) + \frac{1}{12}\left(\frac{1-D_1}{\tau_L}\right)^2\right]\right\}^{1/2}$
$I_{C2(\text{rms})}$	$\frac{V}{R}\left(\frac{1-M}{\sqrt{12}\tau_L}\right)$	$\frac{V}{R}\left(\frac{1-D_1}{\sqrt{12}\tau_L}\right)$
$I_{T(\text{avg})}$	$\frac{VM}{R}$	$\frac{VD_1}{R}$
$I_{T(\text{rms})}$	$\frac{V}{R}\left\{M\left[1 + \frac{1}{12}\left(\frac{1-M}{\tau_L}\right)^2\right]\right\}^{1/2}$	$\frac{V}{R}\left\{D_1\left[1 + \frac{1}{12}\left(\frac{1-D_1}{\tau_L}\right)^2\right]\right\}^{1/2}$
$I_{D1(\text{avg})}$	$\frac{V}{R}(1-M)$	$\frac{V}{R}(1-D_1)$
$I_{D1(\text{rms})}$	$\frac{V}{R}\left\{(1-M)\left[1 + \frac{1}{12}\left(\frac{1-M}{\tau_L}\right)^2\right]\right\}^{1/2}$	$\frac{V}{R}\left\{(1-D_1)\left[1 + \frac{1}{12}\left(\frac{1-D_1}{\tau_L}\right)^2\right]\right\}^{1/2}$
$I_{s(\text{avg})}$	$\frac{VM}{R}$	$\frac{VD_1}{R}$

$$D_2 \equiv \frac{t_2}{T_s} \quad \text{(diode conduction duty cycle).} \tag{2.9}$$

The equations in these tables have been stated in two different ways–first as a function of D_1 for closed-loop calculations, and second as a function of M for open-loop operation. For the continuous mode, $D_1 = M$, so that the two columns

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TABLE 2.2A. Buck Converter Equations for Discontinuous Inductor Current.

Dependent Variable	$f(M, \tau_L, V, R)$	$f(D_1, \tau_L, V, R)$
M	M	$\frac{2}{1+\sqrt{1+8\tau_L/D_1^2}}$
D_1	$M\sqrt{\frac{2\tau_L}{1-M}}$	D_1
D_2	$\sqrt{2\tau_L(1-M)}$	$\left(\frac{4\tau_L}{D_1}\right)\left(\frac{1}{1+\sqrt{1+8\tau_L/D_1^2}}\right)$
I_a (hi freq)	0	0
I_b ($I_{L\,MAX}$)	$\frac{V}{R}\sqrt{\frac{2(1-M)}{\tau_L}}$	$\left(\frac{V}{R}\right)\left(\frac{4}{D_1}\right)\left(\frac{1}{1+\sqrt{1+8\tau_L/D_1^2}}\right)$
$I_{L(avg)}$	$\frac{V}{R}$	$\frac{V}{R}$
$I_{L(rms)}$	$\frac{V}{R}\left[\left(\frac{8}{9}\right)\left(\frac{1-M}{\tau_L}\right)\right]^{1/4}$	$I_b\left[\frac{D_1+D_2}{3}\right]^{1/2}$
$I_{C1(rms)}$	$\frac{V}{R}\left[M\sqrt{\frac{8}{9}\left(\frac{1-M}{\tau_L}\right)-M^2}\right]^{1/2}$	$I_b\sqrt{\frac{D_1}{3}-\frac{D_1^2}{4}}$
$I_{C2(rms)}$	$\frac{V}{R}\left[\sqrt{\frac{8}{9}\left(\frac{1-M}{\tau_L}\right)-1}\right]^{1/2}$	$I_b\left[\frac{D_1+D_2}{3}-\frac{(D_1+D_2)^2}{4}\right]^{1/2}$
$I_{T(avg)}$	$\frac{VM}{R}$	$\frac{VD_1}{R}$
$I_{T(rms)}$	$\frac{V}{R}\left[\frac{8}{9}M^2\left(\frac{1-M}{\tau_L}\right)\right]^{1/4}$	$I_b\sqrt{\frac{D_1}{3}}$
$I_{D1(avg)}$	$\frac{V}{R}\sqrt{2\tau_L(1-M)}$	$\frac{V}{R}\left(\frac{4\tau_L}{D_1^2}\right)\left(\frac{1}{1+\sqrt{1+8\tau_L/D_1^2}}\right)^2$
$I_{D1(rms)}$	$\frac{V}{R}\left[\frac{8}{9}\frac{(1-M)^3}{\tau_L}\right]^{1/4}$	$\left(\frac{V}{R}\right)\left(\frac{1}{\tau_L\sqrt{3}}\right)\left[\left(\frac{4\tau_L}{D_1}\right)\frac{1}{1+\sqrt{1+8\tau_L/D_1^2}}\right]^{3/2}$
$I_{r(avg)}$	$\frac{VM}{R}$	$\frac{VD_1}{R}$

of equations result in identical values. In the discontinuous mode, however, the closed and open-loop equations are quite different. Notice also that, between the continuous and discontinuous modes, the tables show equations that are distinctly different.

In order to select the correct equation set for use, it is necessary to know the

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TABLE 2.2B. Equations Normalized to τ_{LC}.

$\frac{I_a}{I_o} = 1 - \frac{\tau_{LC}}{\tau_L}$	Continuous Mode
$\frac{I_b}{I_o} = 1 + \frac{\tau_{LC}}{\tau_L}$	
$\frac{I_{L(rms)}}{I_o} = \left[1 + \frac{1}{3}\left(\frac{\tau_{LC}}{\tau_L}\right)^2\right]^{1/2}$	
$\frac{I_{C2(rms)}}{I_o} = \frac{1}{\sqrt{3}}\left(\frac{\tau_{LC}}{\tau_L}\right)$	
$\frac{I_b}{I_o} = 2\left(\frac{\tau_{LC}}{\tau_L}\right)^{1/2}$	Discontinuous Mode
$\frac{I_{L(rms)}}{I_o} = \left[\frac{16}{9}\left(\frac{\tau_{LC}}{\tau_L}\right)\right]^{1/4}$	
$\frac{I_{C2(rms)}}{I_o} = \left[\frac{4}{3}\left(\frac{\tau_{LC}}{\tau_L}\right) - 1\right]^{1/2}$	

mode in which the converter is operating. As was pointed out earlier, for a given value of M, the conduction mode is determined by L as well as R. For this reason, we have chosen to use the normalized time constant τ_L in the equations since it is a function of the ratio of L to R. As τ_L becomes smaller, the SPC's conduction mode will eventually change from continuous to discontinuous. The critical boundary value of τ_L (τ_{LC}) for the transition between modes is:

$$\tau_{LC} = \frac{1 - M}{2}. \tag{2.10}$$

If $\tau_L > \tau_{LC}$, then the continuous mode will prevail. On the other hand, if $\tau_L < \tau_{LC}$, then the converter operates in the discontinuous mode. This relationship of Eq. (2.10) is shown in graphic form in Fig. 2.5 for ease of determination of boundaries for various values of τ_L. Keep in mind that as R and V_s are varied, a mode change in SPC operation may occur. It is always prudent to evaluate the mode boundaries over the full range of R and V_s for a particular application if single mode operation is desired.

While Tables 2.1 and 2.2 are very useful for calculating specific numerical values,

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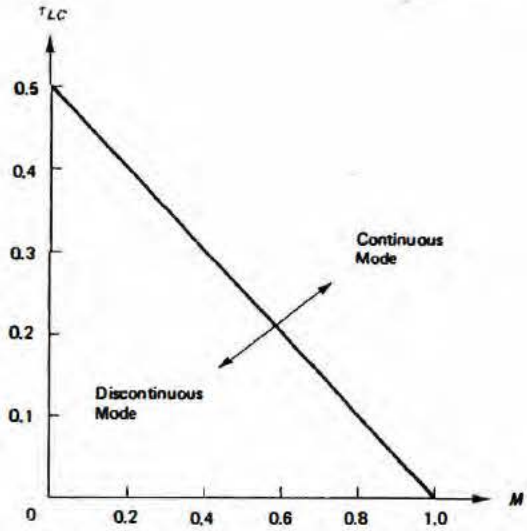


Fig. 2.5. Inductor current conduction mode boundaries.

greater visibility of buck SPC operation can be obtained by graphing the equations. For example, the relationship between M and D_1 is of great interest, and a graph of this relationship is given in Fig. 2.6.

Here we see that the DC control-to-output transfer characteristics are very different between the two modes of operation. In the continuous mode, M is a linear, monotonically increasing function of D_1, and V is not a function of circuit elements L, R, or C. In an ideal converter, V would be independent of load changes and, as such, would be self-regulating from a loading standpoint. A practical SPC converter, however, does not have perfect self-load regulation characteristics because of the presence of R_L. But if this resistance is small (the practical case), then it is reasonable to expect that a practical buck converter will display a high degree of output self-regulation for load variations, when operating in the continuous mode.

Conversely, when the buck SPC is operating in the discontinuous mode, its output is anything *but* self-regulating, with output voltage a function of D_1, R, L, and V_g. As the converter moves deeper into the discontinuous mode of operation, the control range can become quite small.

The control function DC gain (G_1) is:

$$G_1 = \frac{\partial V}{\partial D_1}. \tag{2.11}$$

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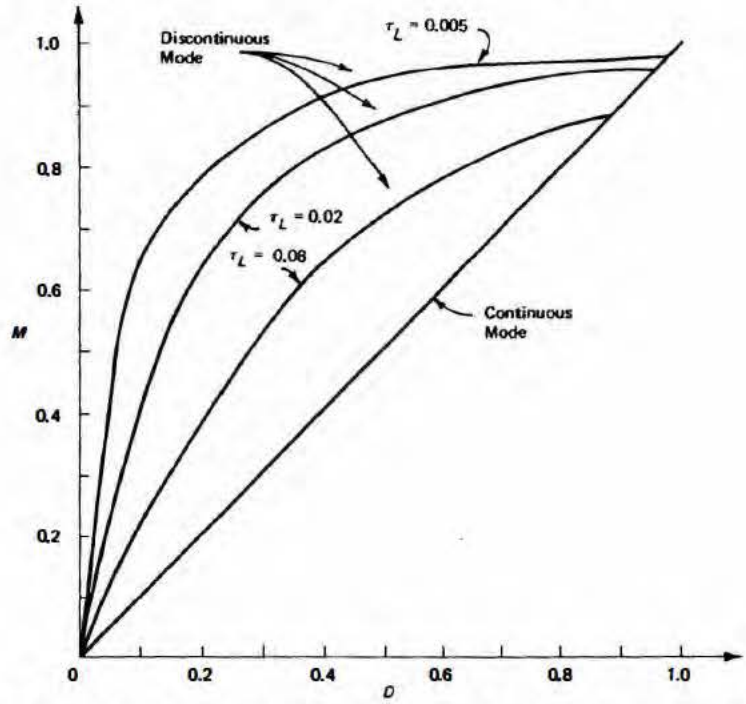


Fig. 2.6. Buck converter voltage gain (M) as a function of D for both continuous and discontinuous modes.

For the continuous mode:

$$G_1 = V_s. \tag{2.12}$$

However, in the discontinuous mode:

$$G_1 = V_s \left\{ \frac{16\tau_L}{(\sqrt{D_1^2 + 8\tau_L})(D_1 + \sqrt{D_1^2 + 8\tau_L})^2} \right\}. \tag{2.13}$$

From Eq. (2.12) we see that G_1 is a simple linear function of V_s. But in the discontinuous mode G_1 is a much more complex function and dependent on all the circuit quantities as shown in Eq. (2.13).

Of particular interest to a designer are the rms, average, and peak currents which occur within the branches of an SPC circuit. Figs. 2.7-2.13 are graphic

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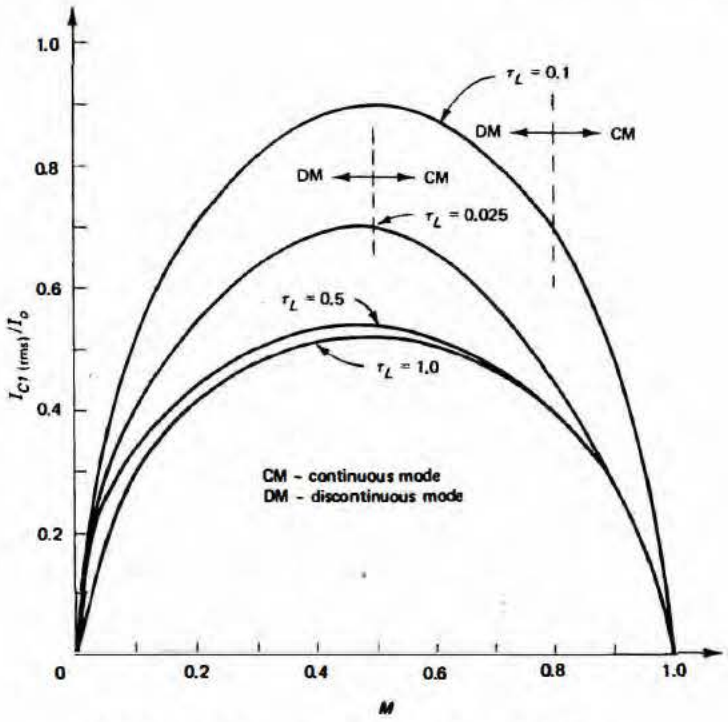


Fig. 2.7. A graph of $I_{C1(rms)}/I_o$ versus M for the buck converter.

representations of various current relationships for the buck SPC, all of which can be easily used as tools in component selection processes.

For example, to select the correct value for the input filter capacitor *C1* of Fig. 2.4, it is necessary to know the maximum rms current that this capacitor will experience. Looking at Fig. 2.7, we see that $I_{C1\,(rms)}$ varies widely with the value of M. If the range of M includes 0.5, then the maximum $I_{C1\,(rms)}$ will occur at or near 0.5. If the range of M does not include 0.5, then by inspection of Fig. 2.7, we can see whether to use the maximum or the minimum values of M to calculate $I_{C1\,(rms)}$. Besides M, the value of L will effect $I_{C1\,(rms)}$. From Fig. 2.8 we see that if L is large compared to L_c then variations in L will have little effect on the rms current in *C1*. But, as we reduce L, $I_{C1\,(rms)}$ increases, slowly at first, and then quite rapidly as the discontinuous mode is entered.

Variations in output capacitor current of the buck SPC with M and L_c/L are shown in Figs. 2.9 and 2.10, respectively. For *C2*, the maximum value of current always occurs at the minimum value of M and we again see the rapid increase

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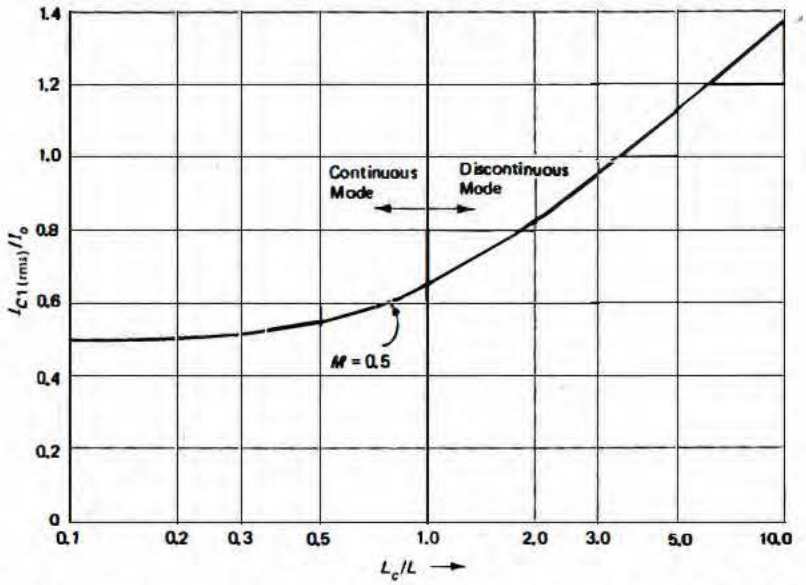


Fig. 2.8. Input capacitor rms ripple current as a function of inductor size for the buck converter.

in current as L is reduced. Figs. 2.11, 2.12, and 2.13 provide additional graphical examples of the variation of the circuit currents within an ideal buck circuit.

It is instructive to compare buck circuit component currents when L is altered to produce a conduction mode change. Such a comparison is given in Table 2.3 for $L = 2L_c$ (continuous mode) and $L = 0.5\ L_c$ (discontinuous mode). When the value of L is reduced, one would expect L to become smaller in proportion. However, $I_{L\,(rms)}$ is increasing rapidly and, since the copper losses in the inductor windings are proportional to wire turns (N) with L proportional to N^2, the copper loss increases. The larger value of AC current produced by a smaller L will also increase the core losses within the inductor. Even though the value of L has been reduced by a factor of four, the peak energy stored ($I_p^2 L/2$) has dropped only by 13%. The net result is that the physical size of L, assuming equal losses, does not drop nearly as rapidly as its inductance value. Meanwhile, the power dissipation in *C1* has more than doubled in the discontinuous case and the power dissipation in *C2* has risen nearly 20 times! To handle such losses, both *C1* and *C2* must be made larger and their increase in size can easily offset any volume gain as a result of reduction in the size of L. For such reasons, as buck SPC output power levels go beyond 75–100 watts, discontinuous modes of operation are rarely satisfactory. At low power levels, however, circuit component sizes are

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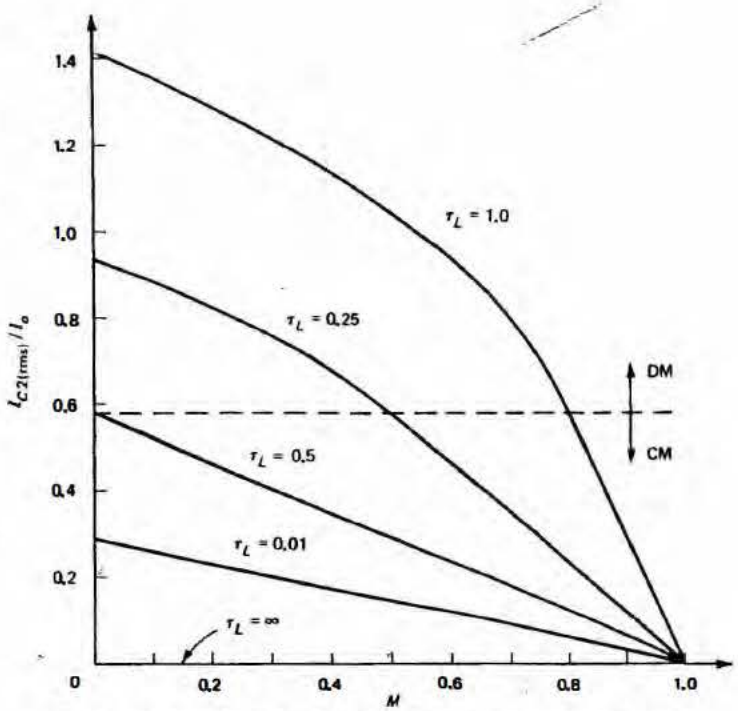


Fig. 2.9. Output capacitor rms ripple current amplitude as a function of M.

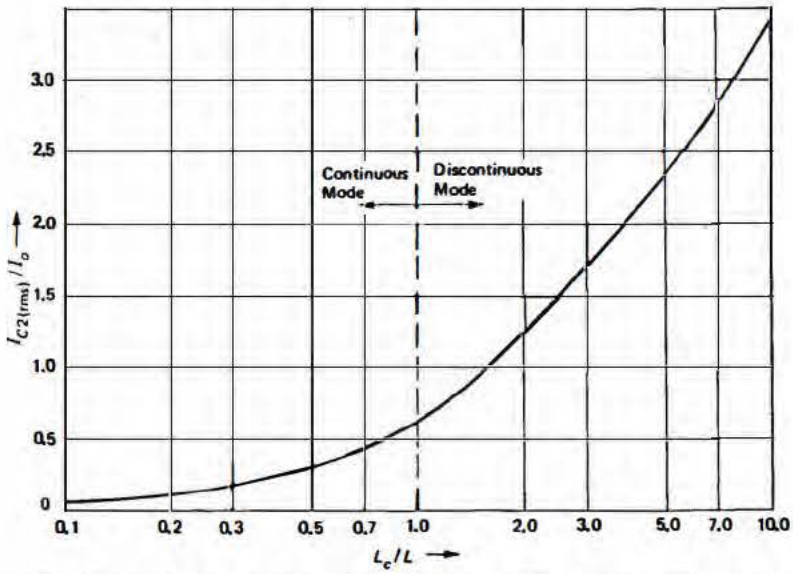


Fig. 2.10. Output capacitor rms ripple current amplitude as a function of inductance value.

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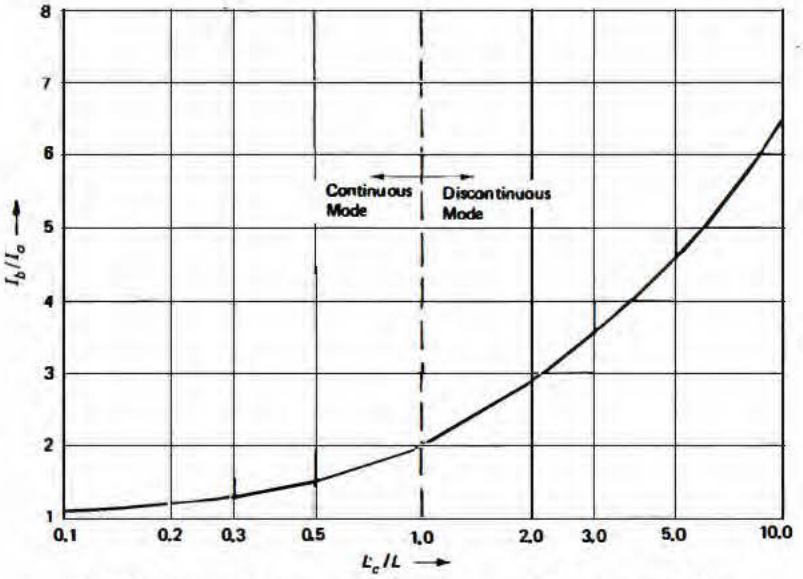


Fig. 2.11. Inductor peak current amplitude as a function of inductance value.

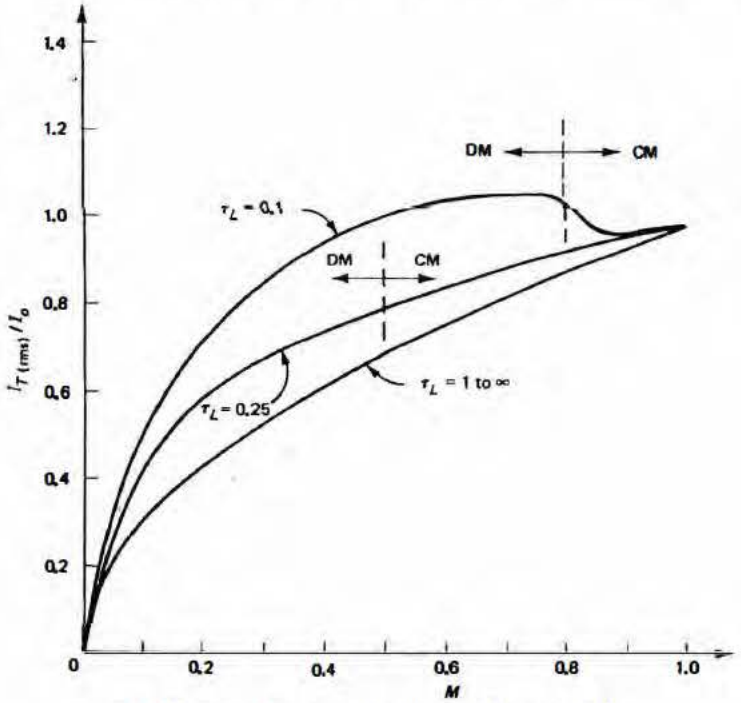


Fig. 2.12. Switch rms current amplitude as a function of M.

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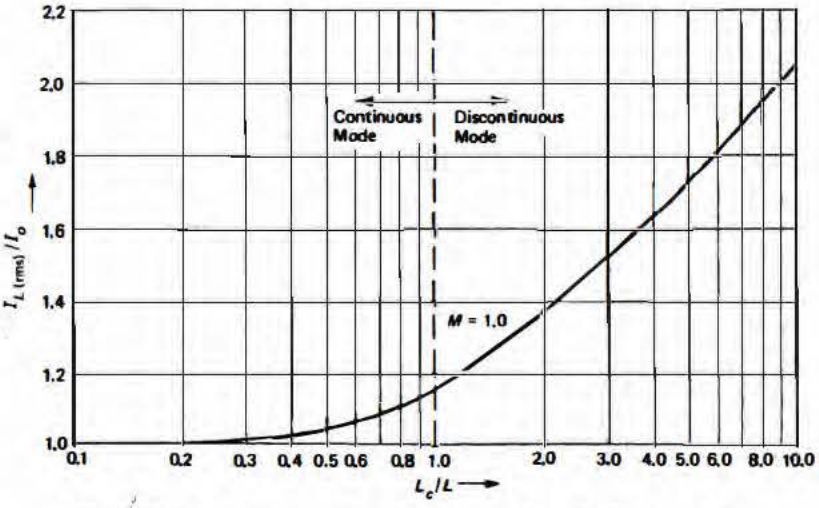


Fig. 2.13. Inductor rms current amplitude as a function of inductance value.

TABLE 2.3. Effect of Changing L_C/L.

Current	$L = 2L_c$	$L = 0.5L_c$	Ratio	Ratio^2
I_b	1.50	2.83	1.87	3.49
$I_{L(rms)}$	1.04	1.37	1.32	1.73
$I_{C1(rms)}$	0.54	0.83	1.54	2.36
$I_{C2(rms)}$	0.29	1.29	4.45	19.8

not so directly related to their current-handling capabilities. Here the discontinuous mode is frequently used, especially where large output load ranges are possible, to avoid conduction mode changes and corresponding effects on small-signal response functions important for regulation stability.

2.3. LARGE-SIGNAL DYNAMIC CHARACTERISTICS

A major concern of the designer is how an SPC circuit will respond to step-changes in input voltage and output load current, especially when such variations are produced by open circuit or overload situations.

If input/output variations are small, then excellent analytical tools are available to the SPC designer to predict corresponding circuit responses. These small-

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signal models will be examined in detail in later sections of this book. However, if these variations are large, currently available analytical means for predicting the SPC circuit response are quite limited and are far from accurate. Large-signal modeling and analysis of SPCs are problems that are now beginning to receive a good deal of research attention by power electronics scientists. Unfortunately, at this writing, we will have to restrict our discussions to some fairly general observations, unsatisfactory though that may be.

If the load of a buck SPC is removed, then $r_L = 0$ and the output voltage V will rise toward a value of V_s. V can be limited by providing auxiliary protection elements to sense the output voltage rise and to turn off the switching elements. Following such a sequence, V will fall to zero with a time constant dependent on the values of $C2$ and any leakage resistance inherent in the circuit.

When the output of the buck SPC is short-circuited, I_L will begin to rise with its rate limited by V_s, f_s, and L. Therefore, it will normally take several switching cycles of the SPC before I_L becomes excessive. If a current sensor is used in series with L, there is usually sufficient time for auxiliary electronics to turn off the switch before I_L can produce circuit damage.

If V_s is applied rapidly to the circuit of Fig. 2.4 and $Q1$ is initially OFF, then the inrush current into the SPC is limited by the value of $C1$. By increasing the duty cycle of $Q1$ slowly, V can increase gradually and the inrush current at SPC turn-on limited to that required to charge $C1$ of the input filter. This is referred to as "soft-starting" and is an auxiliary control feature included in most SPC applications.

Conversely, when the SPC is turned off, the duty cycle of $Q1$ can be slowly reduced by auxiliary electronics to produce a gradual reduction of the output voltage. However, there is a limit to the degree of shutdown control possible using such means. The turn-off time constant of the control circuit must be longer than the time constant formed by R and $C2$. If this condition is not satisfied, the effective load-plus-filter network time constant will determine the turn-off characteristics of the system.

One of the advantages of the buck SPC and its more complex derivative converters is the ability to easily control output voltages and currents during turn-on and turn-off and under output fault conditions. As we shall see in the next chapter, the boost converter does not possess such advantageous properties.

2.4 STATE-SPACE AVERAGE MODEL FOR THE CONTINUOUS MODE

One of the most important advances of the past ten years in characterizing SPCs has been the development of accurate small-signal models for them, and a variety of modeling methods are now available. We have chosen to present only the state-space averaging technique, since it is very general, relatively easy to comprehend, and straightforward in its application in solving practical SPC modeling problems.

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State-space averaging provides the SPC designer with a choice of either a mathematical or equivalent circuit model for his use. The mathematical model is very useful, since it permits the designer to calculate the values for SPC circuit voltages, currents, small-signal transfer functions, and much more. However, the mathematical model for an SPC does not readily expose the electrical processes occurring in the circuit. A deeper and more rapid understanding of the circuit functions can be gleaned from examination of an equivalent circuit model. In general, both types of models are usually needed to solve practical design problems. Two independent routes are available to the designer for developing each model. In the first, the circuit equations are manipulated until a satisfactory mathematical model is developed, and from that model, one proceeds to synthesize an equivalent circuit model. Alternatively, we could start with an equivalent circuit model, manipulate it into a satisfactory circuit form, and then generate related circuit equations. The two approaches just described are equivalent and the choice of which route to follow is really a matter of practical convenience. In the discussions to follow, we have elected to take the first route since it will be relatively easy for the reader to follow if this is his first exposure to state-space modeling. Again, for the researcher who is interested in a more complete exposition of the technique, the work by R. D. Middlebrook and his colleagues [1, 2] is highly recommended.

The procedure will follow these steps:

STEP 1. Draw the linear equivalent circuit for each state of the converter. In the case of the continuous mode, there are two states, each corresponding to one switch position.

STEP 2. Write the circuit equations for each equivalent circuit model of Step 1 in a state-variable format.

STEP 3. Average each set of equations by using the duty cycle of the switch as a weighting factor and then combine the two sets of state equations into a single set by summation.

STEP 4. Perturb the averaged equation set of Step 3 to produce DC and small-signal terms and eliminate any nonlinear cross products.

STEP 5. Transform the small-signal or AC terms from Step 4 into complex frequency domain (the so-called s domain).

At this point we will have a mathematical model and the final step of the procedure is:

STEP 6. Draw the equivalent circuit model corresponding to the mathematical equations formed by the earlier steps.

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As an example of the above procedure, we will now go through the step-by-step process for the case of a simple buck SPC operating in the continuous mode.

The circuit to be studied is shown in Fig. 2.14A. When the switch (S) is in position A, the circuit assumes the topology shown in Fig. 2.14B, and when S is in position B, the network assumes the topology illustrated in Fig. 2.14C.

We continue the process by writing the equations in state-variable form for each of these two networks. The form of the equation is:

$$\dot{x} = A_{11}\,x + A_{21}\,y + b_1\,v_s \tag{2.14}$$

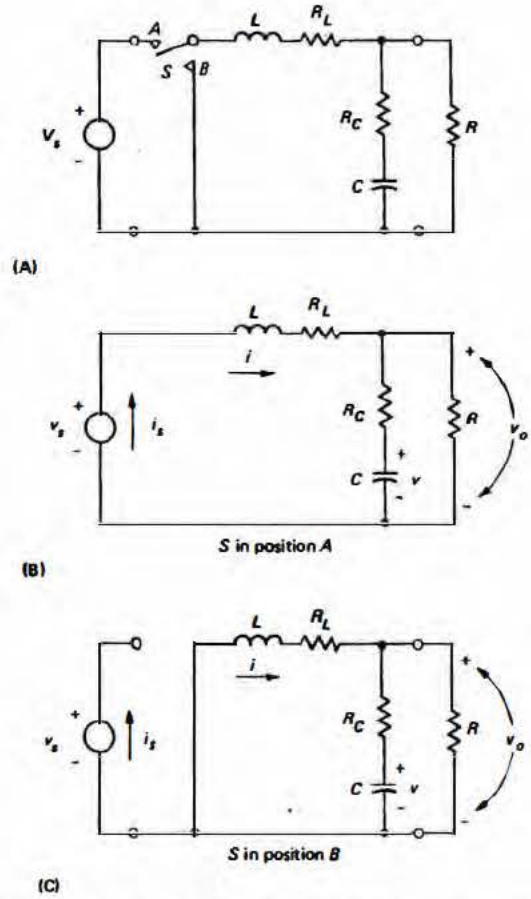


Fig. 2.14. Equivalent circuits for the buck converter in the continuous mode.

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$$\dot{y} = A_{21}x + A_{22}y + b_2 v_s \tag{2.15}$$

$$z = C_1 x + C_2 y. \tag{2.16}$$

Because of their dynamic behavior, it is normal to choose inductor currents and capacitor voltages as the state variables in the equations. Alternately, inductor flux (ϕ) and the capacitor charge (q) can also be used as state variables. For the network in Fig. 2.14B:

$$\frac{di}{dt} = -\frac{1}{L}\left(\frac{R R_L + R R_C + R_C R_L}{R + R_C}\right) i - \frac{1}{L}\left(\frac{R}{R + R_C}\right) v + \frac{v_s}{L} \tag{2.17}$$

$$\frac{dv}{dt} = \frac{1}{C}\left(\frac{R}{R + R_C}\right) i - \frac{1}{C}\left(\frac{1}{R + R_C}\right) v \tag{2.18}$$

$$v_o = (R \| R_C)\, i + \left(\frac{R}{R + R_C}\right) v \tag{2.19}$$

$$i_s = i \tag{2.20}$$

and for the network in Fig. 2.14C:

$$\frac{di}{dt} = -\frac{1}{L}\left(\frac{R R_L + R R_C + R_C R_L}{R + R_C}\right) i - \frac{1}{L}\left(\frac{R}{R + R_C}\right) v \tag{2.21}$$

$$\frac{dv}{dt} = \frac{1}{C}\left(\frac{R}{R + R_C}\right) i - \frac{1}{C}\left(\frac{1}{R + R_C}\right) v \tag{2.22}$$

$$v_o = (R \| R_C)\, i + \left(\frac{R}{R + R_C}\right) v \tag{2.23}$$

$$i_s = 0. \tag{2.24}$$

Notice that we have included expressions for the input and output quantities, i_s and v_o, as these quantities will be needed to form the final equivalent circuit model.

Each of the above sets of equations is valid for a particular switch position during an operating cycle. These equations are exact and, along with boundary conditions and element values, completely describe the corresponding network of Fig. 2.14 during each portion of its switching cycle. Unfortunately, it is a very cumbersome process to derive the SPC circuit parameters directly from these two sets of equations. In addition, one rarely needs exact answers for every

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parameter of these state equations. To combine the two networks into a single network which can be easily analyzed using linear circuit theory, we need to *average* the equations over one cycle. The weighting factor for averaging will be the proportion of time spent by the switch S (Fig. 2.14A) in each of its two states.

For switch position A, $\Delta t = t_1$, and for position B, $\Delta t = t_2$. The weighting factors for averaging then become:

$$\frac{t_1}{T_s} = d \tag{2.25}$$

$$\frac{t_2}{T_s} = \frac{T_s - t_1}{T_s} = 1 - d = d' \tag{2.26}$$

By averaging the state equations, we will lose some information about the SPC, but the results will be more than adequate in accuracy, especially if the output voltage ripple of the SPC is minute. Since low output ripple is normally a desirable characteristic of a DC-DC SPC, this restriction is of little analytical consequence.

The state-space averaging of a particular state variable will take the following form:

$$\langle \dot{x} \rangle = (A_{11}x + A_{12}y + b_1 v_s)\, d + (A'_{11}x + A'_{12}y + b'_1 v_s)\, d' \tag{2.27}$$

where the primed quantities represent the circuit constants associated with the state in Fig. 2.14C.

If we now apply this averaging process to Eqs. (2.17) through (2.24) the following set of equations for the state-space averaged network is obtained:

$$\frac{di}{dt} = -\left(\frac{R_L + R \| R_C}{L}\right) i - \frac{1}{L}\left(\frac{R}{R + R_C}\right) v + \frac{v_s d}{L} \tag{2.28}$$

$$\frac{dv}{dt} = \frac{1}{C}\left(\frac{R}{R + R_C}\right) i - \frac{1}{C}\left(\frac{1}{R + R_C}\right) v \tag{2.29}$$

$$v_o = (R \| R_C)\, i + \left(\frac{R}{R + R_C}\right) v \tag{2.30}$$

$$i_s = di. \tag{2.31}$$

We have now arrived at a single set of equations and a single model that represents the average characteristics of both states. However, the equations are not yet

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linear, since in Eq. (2.28) we see the term $v_s d$ and in Eq. (2.31) di, which are the products of two variables. As a practical matter, it is usually desirable to have separate solutions for AC and DC characteristics. In this equation set, both AC and DC characteristics are lumped into a single variable.

The standard technique for solving these problems is to assume that the AC terms can be made arbitrarily small compared to the DC terms. We do this by making the following assumptions:

$$v_s = V_s + \hat{v}_s \tag{2.32}$$

$$v = V + \hat{v} \tag{2.33}$$

$$i = I + \hat{i} \tag{2.34}$$

$$d = D + \hat{d} \tag{2.35}$$

$$v_o = V_o + \hat{v}_o \tag{2.36}$$

$$i_s = I_s + \hat{i}_s \tag{2.37}$$

where V_s, V, I, I_s, D, and V_o are the DC values for the circuit variables and $\hat{v}_s$, $\hat{v}$, $\hat{i}$, $\hat{i}_s$, $\hat{d}$, and $\hat{v}_o$ are the corresponding small-signal or perturbed values for the variables.

The small-signal assumption implies that:

$$\frac{\hat{v}_s}{V_s} \ll 1 \tag{2.38}$$

$$\frac{\hat{v}}{V} \ll 1 \tag{2.39}$$

$$\frac{\hat{i}}{I} \ll 1 \tag{2.40}$$

$$\frac{\hat{d}}{D} \ll 1 \tag{2.41}$$

$$\frac{\hat{v}_o}{V_o} \ll 1 \tag{2.42}$$

$$\frac{\hat{i}_s}{I_s} \ll 1. \tag{2.43}$$

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Since all small-signal quantities are minute, any cross-multiplied terms, such as $\hat{v}\hat{d}$, are even smaller and may be ignored. If we incorporate these assumptions into Eqs. (2.28) through (2.31) and separate the small-signal and DC portions of each, the following set of equations results:

DC

$$0 = [-R_L + (R \| R_C)]\, I - \left(\frac{R}{R + R_C}\right) V + V_s D \tag{2.44}$$

$$0 = \left(\frac{R}{R + R_C}\right) I - \frac{V}{R + R_C} \tag{2.45}$$

$$V_o = (R \| R_C)\, I + \left(\frac{R}{R + R_C}\right) V \tag{2.46}$$

$$I_s = DI \tag{2.47}$$

AC

$$\frac{d\hat{i}}{dt} = -\left(\frac{R_L + R \| R_C}{L}\right) \hat{i} - \frac{1}{L}\left(\frac{R}{R + R_C}\right) \hat{v} + \left(\frac{D}{L}\right) \hat{v}_s + \left(\frac{V_s}{L}\right) \hat{d} \tag{2.48}$$

$$\frac{d\hat{v}}{dt} = \frac{1}{C}\left(\frac{R}{R + R_C}\right) \hat{i} - \frac{1}{L}\left(\frac{1}{R + R_C}\right) \hat{v} \tag{2.49}$$

$$\hat{v}_o = (R \| R_C)\, \hat{i} + \left(\frac{R}{R + R_C}\right) \hat{v} \tag{2.50}$$

$$\hat{i}_s = D\hat{i} + I\hat{d}. \tag{2.51}$$

The small-signal relationships of Eqs. (2.48) through (2.51) can be more easily manipulated if they are transformed into the complex frequency domain using Laplace transformation methods. These four equations will now become:

$$V_s \hat{d}(s) + D\hat{v}_s(s) = (sL + R_L + [R \| R_C])\, \hat{i}(s) + \left[\frac{R}{R + R_C}\right] \hat{v}(s) \tag{2.52}$$

$$0 = \left[\frac{R}{R + R_C}\right] \hat{i}(s) - \left[sC + \frac{1}{R + R_C}\right] \hat{v}(s) \tag{2.53}$$

$$\hat{v}_o(s) = (R \| R_C)\, \hat{i}(s) + \left[\frac{R}{R + R_C}\right] \hat{v}(s) \tag{2.54}$$

$$i_s(s) = D\hat{i}(s) + I\hat{d}(s). \tag{2.55}$$

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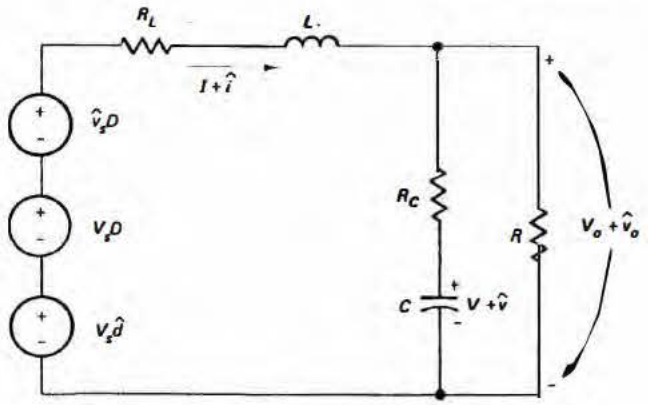


Fig. 2.15. A state-space averaged model for the buck converter.

The electrical network represented by these equations is illustrated in Fig. 2.15. For the time being, we will not elaborate on the methods of its construction. In Chapter 10, we will illustrate a general procedure for deriving the averaged circuit model of an SPC from its mathematical equations. While the circuit model in Fig. 2.15 is both simple and linear in nature, it still leaves much to be desired as a practical small-signal model. For example, the model contains generators whose values are functions of more than one variable, making it difficult to embed the model within a total power processing system, which normally includes regulation control electronics as well as input noise reduction filter networks.

The next step in practical model development is to separate the DC control function from the source voltage value. One way to accomplish this is shown in Fig. 2.16A, where a variable ideal turns-ratio transformer element (*T1*) has been introduced. This transformer element has some marvelous properties, since its frequency response extends down to zero so as to pass AC and DC signals with equal facility. We indicate this transformation capability by the combination of a sinusoidal and a straight line through the transformer symbol. Also, the primary-to-secondary turns ratio of this transformer model is variable and equal to $D + \hat{d}$.

Obviously, an ideal transformer such as this one is not physically realizable. Nevertheless, it is a very useful modeling concept for our purposes.

The small-signal dependency of the variable turns-ratio of the transformer element in Fig. 2.16A can be removed if desired, and for our modeling purposes it is highly desirable to do so, as many SPC circuits have small-signal models where the generators associated with d have a complex variable dependency.

If the turns-ratio dependency of *T1* on $\hat{d}$ is to be removed, then the model must include generator elements that account for the $I\hat{d}$ and $V_s\hat{d}$ changes in the

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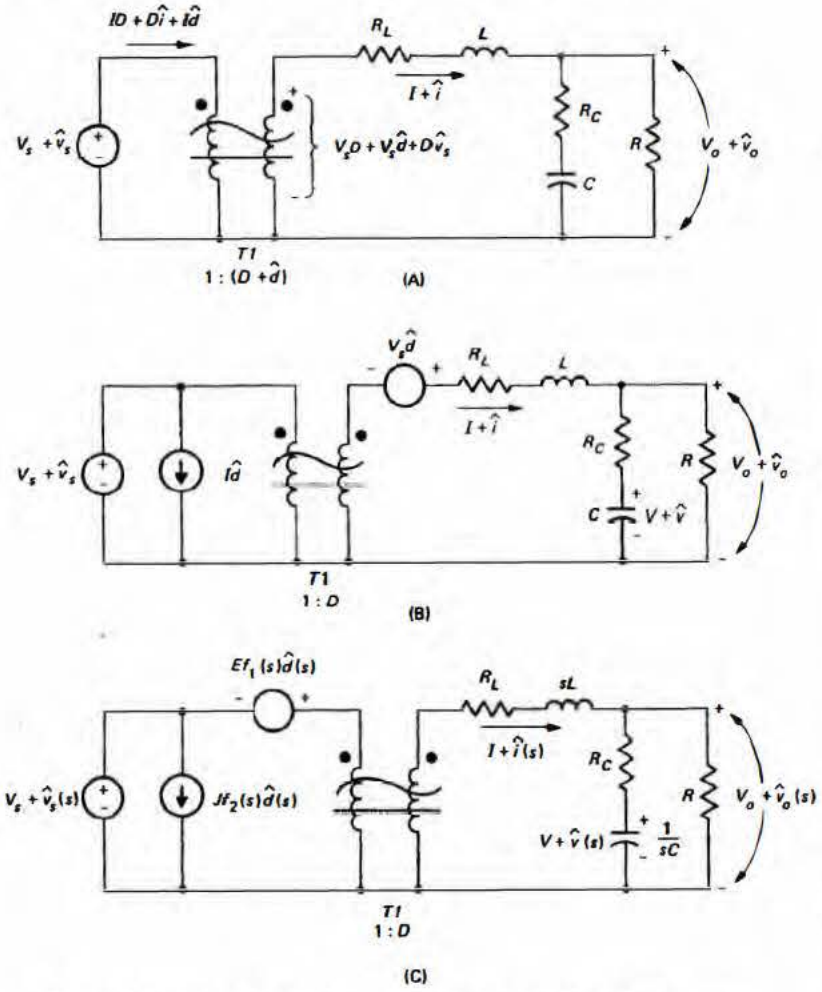


Fig. 2.16. Evolution of the final state-space averaged model for the buck converter.

primary and secondary, respectively, of the transformation element. This can be done, as shown in Fig. 2.16B, by placing appropriate voltage and current generators in the primary and secondary of *T1*. We can further simplify the model of Fig. 2.16B by translating the $V_s\hat{d}$ voltage generator to the primary side of the transformer. The resulting SPC model is illustrated in Fig. 2.16C, where:

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$$Ef_1 = \frac{V_o}{D^2} = \frac{V_s}{D} \tag{2.56}$$

$$Jf_2 = \frac{V_o}{R} = I \tag{2.57}$$

The model of Fig. 2.16C has the properties we have been seeking. All of the variables (V_s, $\hat{v}_s$, D, $\hat{d}$, etc.) have separate control elements and can be individually varied. The source and the load are clearly separated from the SPC model so as to facilitate the addition of an input filter or additional output filter circuits. The structure of the model permits its inclusion into a total power processing system with regulation controls that can alter D as a function of changes in SPC input voltage or output load. We will examine all these possibilities in more detail in Chapter 10.

The model we have evolved is somewhat arbitrary in that the primitive models we began with could have been manipulated in a different manner with the final result exposing a completely different model topology. In any case, the chosen circuit model must still conform to the constraints of Eqs. (2.44) through (2.47) and Eqs. (2.52) through (2.55), so that any model must be electrically equivalent to all others. Thus, one may choose between them as a matter of analytical convenience. The model of Fig. 2.16C meets all of our modeling needs very nicely and is now beginning to be accepted as a standard model for examining the effects of small-signal changes in control as well as input/output conditions.

Now that we have both a circuit model and a mathematical model for a buck SPC, we can begin to examine some of the circuit relationships important to small-signal operation.

For a start, we solve Eqs. (2.44) through (2.47) to obtain expressions for V_o as a function of V_s:

$$\frac{V_o}{V_s} = \underbrace{D}_{\text{ideal}} \cdot \underbrace{\left[\frac{R}{R+R_L}\right]}_{\substack{\text{correction} \\ \text{factor}}} \tag{2.58}$$

We see that V_o/V_s, when the parasitic resistance of the inductor is included, is simply the product of the ideal voltage transfer function of the buck SPC and a correction factor that accounts for the series parasitic resistance.

This correction factor is not normally very large if the buck converter is reasonably power-efficient, and is always less than one. From the small-signal equations, one can solve for the open-loop input-to-output transfer function or the control-to-output transfer function as shown below.

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$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \left(\frac{V_o}{D}\right)\left[\frac{1 + sR_C C}{1 + s\left(R_C C + [R \| R_L]\, C + \frac{L}{R + R_L}\right) + s^2 LC\left(\frac{R + R_C}{R + R_L}\right)}\right] \quad (2.59)$$

$$\frac{\hat{v}_o(s)}{\hat{v}(s)} = \left[\frac{DR}{R + R_L}\right]\left[\frac{1 + sR_C C}{1 + \left[R_C C + (R \| R_L)\, C + \frac{L}{(R + R_L)}\right]s + LC\left[\frac{R + R_C}{R + R_L}\right]s^2}\right] \quad (2.60)$$

Figure 2.17 is a logarithmic graph of the magnitude and phase angle of Eq. (2.59) using asymptotic approximations. As shown, the equation represents a conventional two-pole low-pass filter with a zero introduced by the presence of output capacitance ESR. The magnitude of Eq. (2.59) is obviously dependent on the value of SPC duty cycle D, which will change the position of the magnitude plot, but *not* its shape.

The open-circuit input impedance (Z_{io}) of the SPC is:

$$Z_{io} = \left.\frac{\hat{v}_s(s)}{\hat{i}_s(s)}\right|_{\hat{d}(s)=0} \quad (2.61)$$

To determine Z_{io} we could manipulate Eqs. (2.52) through (2.55) with $\hat{d} = 0$, but it is simpler to use the circuit model for the determination. Looking at Fig. 2.16C, we see that Z_{io} is the input impedance of the output filter network (including R) reflected through $T1$. From this observation we can write:

$$Z_{io} = \left[\frac{R + R_L}{D^2}\right] \cdot \left[\frac{1 + s\left[\frac{L}{R + R_L} + (R_C + (R \| R_L))\, C\right] + s^2 LC\left[\frac{R + R_C}{R + R_L}\right]}{1 + s(R + R_C)\, C}\right] \quad (2.62)$$

The open-loop output impedance (Z_{oo}) is defined as:

$$Z_{oo} = \left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{d}(s)=\hat{v}_s(s)=0} \quad (2.63)$$

However, our analysis has implicitly assumed that $\hat{i}_o(s) = 0$. We can alter our model to cope with this situation by adding an external generator (i_g) in parallel with R, as shown in Fig. 2.18 A. Then:

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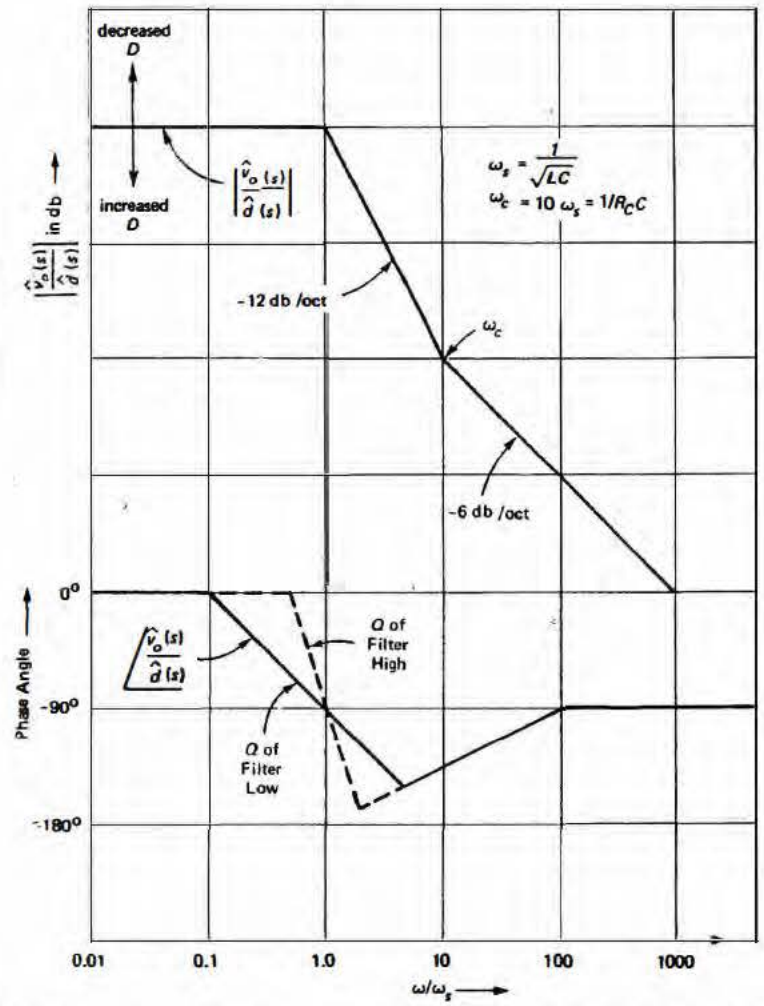


Fig. 2.17. Asymptotic gain and phase approximations for the control-to-output transfer function of a typical buck converter.

$$Z_{oo} = \left.\frac{\hat{v}_o(s)}{\hat{i}_g(s)}\right|_{\hat{d}(s)=\hat{v}_s(s)=0} \tag{2.64}$$

Given that $\hat{d} = \hat{v}_s = 0$, one can now redraw our circuit model to look like that shown in Fig. 2.18B. Since we are interested only in small-signal AC terms, the

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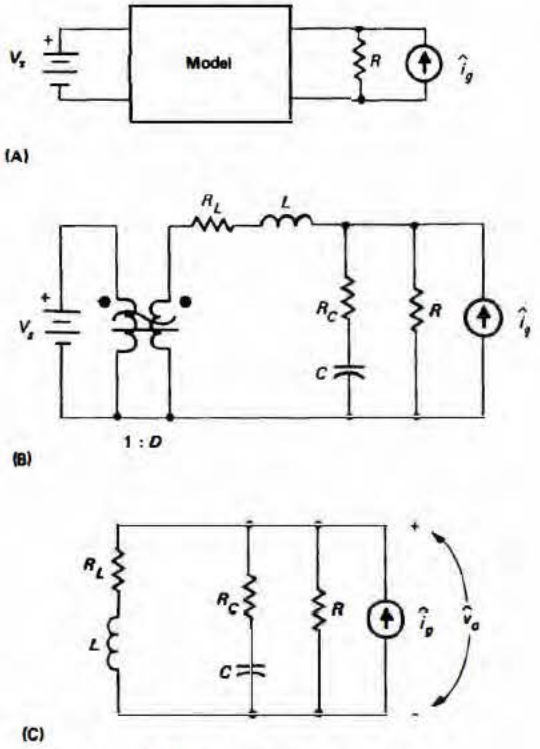


Fig. 2.18. Methods for determining Z_{00}.

model can be further simplified as shown in Fig. 2.18C. From this latter network, we can readily determine Z_{oo} to be:

$$Z_{oo} = (R \| R_C) \left\{ \frac{(s + R_L/L)(s + 1/R_C C)}{s^2 + \left[\frac{R_L + (R\|R_C)}{L} + \frac{1}{(R + R_C)\,C}\right] s + \left[\frac{R + R_L}{R + R_C}\right] \frac{1}{LC}} \right\}. \tag{2.65}$$

An alternative method for finding Z_{oo} would be to add $\hat{i}_g$ to our original circuit of Fig. 2.14A and then derive our averaged models with its effect included; i_g could then be extracted directly from the mathematical descriptions of the resulting averaged models.

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2.5. STATE-SPACE AVERAGED MODEL FOR THE DISCONTINUOUS MODE

The definition of the discontinuous mode requires that the inductor current of the buck SPC go to zero during each switching cycle. As a result, the discontinuous circuit model must assume three different states during each switching cycle in contrast to only two states for the continuous mode. In the analysis to follow, we will use an ideal buck converter circuit for simplicity.

The three networks (A, B, and C) corresponding to the three different states are shown in Fig. 2.19. By examination of each state, we can write the following state-variable network equations:

$$\text{A} \begin{cases} \dfrac{di}{dt} = -\dfrac{v}{L} + \dfrac{v_s}{L} & (2.66) \\ \dfrac{dv}{dt} = \dfrac{i}{C} - \dfrac{v}{RC} & (2.67) \end{cases}$$

$$\text{B} \begin{cases} \dfrac{di}{dt} = -\dfrac{v}{L} & (2.68) \\ \dfrac{dv}{dt} = \dfrac{i}{C} - \dfrac{v}{RC} & (2.69) \end{cases}$$

$$\text{C} \begin{cases} \dfrac{di}{dt} = 0 & (2.70) \\ \dfrac{dv}{dt} = -\dfrac{v}{RC} & (2.71) \end{cases}$$

Network A exists during time interval t_1, network B during time t_2, and network C during the remainder of the switching cycle. It is now possible to define the duty cycle values to be used for averaging the above equations:

$$d_1 \equiv \frac{t_1}{T_s} \tag{2.72}$$

$$d_2 \equiv \frac{t_2}{T_s} \tag{2.73}$$

$$d_3 \equiv 1 - d_1 - d_2. \tag{2.74}$$

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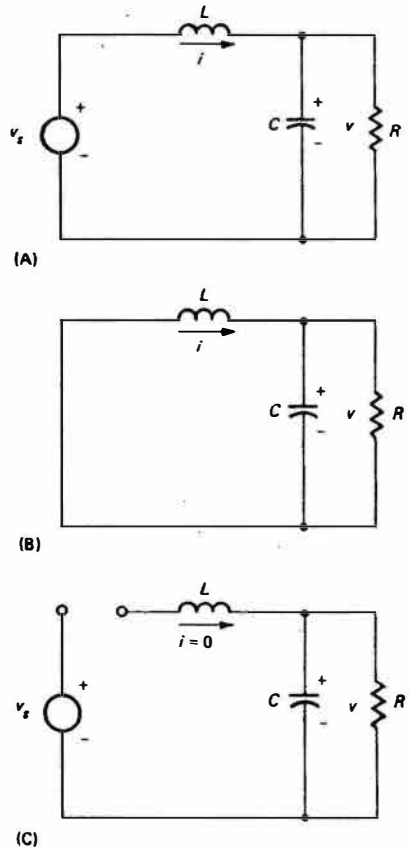


Fig. 2.19. Equivalent circuits for the buck converter in the discontinuous mode.

Before proceeding with the averaging step, a look at an additional circuit constraint is necessary because of the discontinuous conduction nature of the SPC.

For a converter operating in the continuous mode, at the beginning of each switching cycle, $I_L = i_L(0)$, and, at the end of each cycle, $I_L = i_L(T_s)$. In general, $i_L(0)$ and $i_L(T_s)$ do not equal zero. If we perturb i_L during the switching cycle, then $i_L(0) \neq i_L(T_s)$. As a consequence, the *average* value for the rate of change of inductor current *over one cycle does not equal zero* and, must be retained in the circuit equations under continuous current flow conditions.

However, in the discontinuous mode, the very definition of this operating mode requires that:

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$$i_L(0) = i_L(T_s) = 0. \tag{2.75}$$

Eq. (2.75) implies that any upward rate of change of inductor current must be exactly compensated for by a corresponding downward rate of change so that the average current magnitude over one complete cycle becomes:

$$\left\langle \frac{di}{dt} \right\rangle = 0. \tag{2.76}$$

The above relationship holds even if i_L is perturbed, as can be seen in Fig. 2.20, where t_1 is extended by Δt. The average value of the perturbation must still be zero.

If we now average Eqs. (2.66) through (2.71), using the definitions given in Eqs. (2.72) through (2.74), and keeping in mind the condition stated by Eq. (2.76), the following results are obtained:

$$0 = -(d_1 + d_2)v + d_1 v_g \tag{2.77}$$

$$\frac{dv}{dt} = \left(\frac{d_1 + d_2}{C}\right) i - \frac{v}{RC}. \tag{2.78}$$

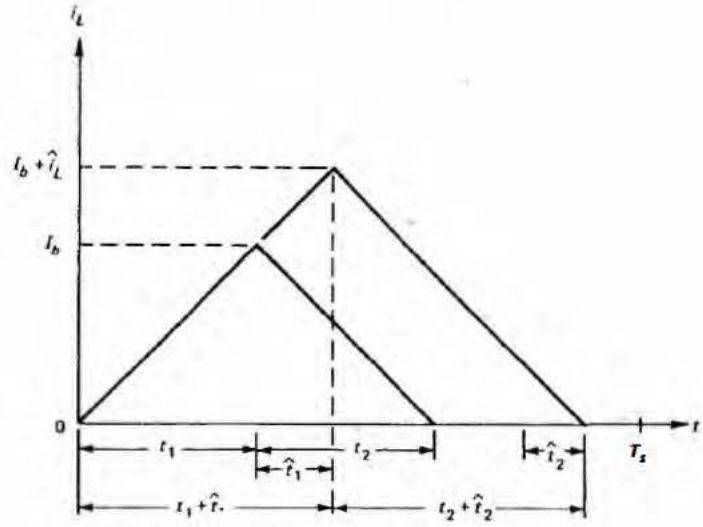


Fig. 2.20. The effect on i_L of perturbing t_1.

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Once again, a mathematical model has been derived consisting of a single set of differential equations which can be easily manipulated using conventional linear circuit theory.

We can now form a circuit model using Eqs. (2.77) and (2.78), and the result is shown in Fig. 2.21A. However, the utility of this model can be improved by modifying it slightly. In Fig. 2.21B, we employ an ideal transformer to isolate v and i as separate variables. In Fig. 2.21C, the dependent generators of Fig. 2.21B are replaced with another ideal transformer. For most design purposes, the current (i) circulating in the inner loop is of no particular interest. Therefore, the two transformers of Figs. 2.21B and 2.21C can be combined to arrive at the relatively simple circuit model of Fig. 2.21D.

This intermediate discontinuous model suffers from the same problems as the continuous mode model at this point in the analysis. All of the externally controlled variables have not been separated and another variable (d_2) has been introduced which is a function of the circuit elements as well as d_1. For these reasons, the process of model refinement must be continued and, as before, we have the option of either manipulating the associated circuit equations and then determining the circuit model, or manipulating the circuit model followed by equation derivations. As was the case of the continuous model derivation, the former option will be pursued here.

However, before continuing with the model development process, we note that the model of Fig. 2.21D does have one very interesting feature--*the inductor has disappeared!* As a result, we can conclude that the second-order nature of the output filter network has been reduced to first order. The disappearance of L from the model is a direct consequence of the constraint stated in Eq. (2.76).

Because of the altered nature of the model, one of the state variables (di/dt) has been lost. We can replace this loss with another equation related to the average current, i, defined as:

$$i = \frac{i_b}{2} = (v_s - v)\left(\frac{d_1}{2R\tau_L}\right). \tag{2.79}$$

If we now perturb Eqs. (2.77) through (2.79) using the same conventions and assumptions employed in Section 2.4, and then separate them into DC and small-signal sets, the following relationships are obtained:

$$\text{DC}\begin{cases} 0 = -(D_1 + D_2)V + D_1 V_s & (2.80) \\ 0 = (D_1 + D_2)I - \dfrac{V}{R} & (2.81) \\ I = (V_s - V)\left[\dfrac{D_1}{2R\tau_L}\right] & (2.82) \end{cases}$$

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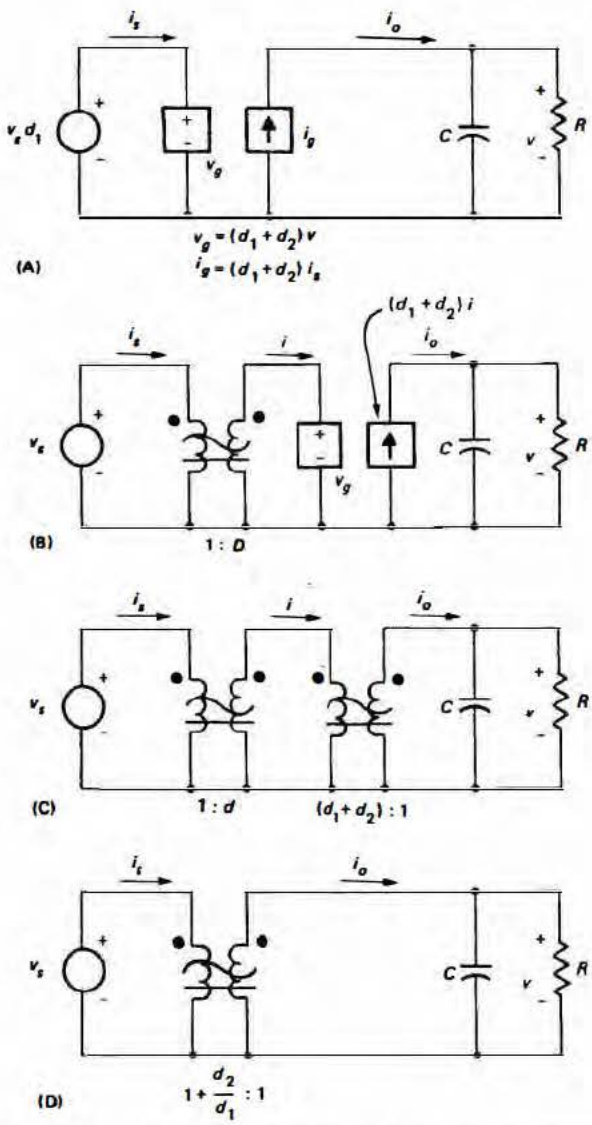


Fig. 2.21. Derivation of the state-space averaged model for the buck converter in the discontinuous mode.

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$$\text{AC}\begin{cases} 0 = -(D_1 + D_2)\hat{v} + (V_s - V)\hat{d}_1 - V\hat{d}_2 + D_1\hat{v}_s & (2.83) \\ C\dfrac{d\hat{v}}{dt} = (D_1 + D_2)\hat{i} - \dfrac{\hat{v}}{R} + I\hat{d}_1 + I\hat{d}_2 & (2.84) \\ \hat{i} = \left(\dfrac{1}{2R\tau_L}\right)[-D_1\hat{v} + (V_s - V)\hat{d}_1 + D_1\hat{v}_s]. & (2.85) \end{cases}$$

Unfortunately, the above equations still contain terms that include D_2 and $\hat{d}_2$. These can be eliminated by further manipulation of these same relationships, from which the following expressions evolve:

$$\text{DC}\begin{cases} I = \dfrac{V}{R}\sqrt{\dfrac{1-M}{2\tau_L}} & (2.86) \\ V = MV_s & (2.87) \end{cases}$$

$$\text{AC}\begin{cases} \hat{i} = \left[\dfrac{M}{R\sqrt{2\tau_L(1-M)}}\right]\hat{v} + \left(\dfrac{V}{2R\tau_L}\right)\left(\dfrac{1-M}{M}\right)\hat{d}_1 + \left[\dfrac{M}{R\sqrt{2\tau_L(1-M)}}\right]\hat{v}_s & (2.88) \\ C\dfrac{d\hat{v}}{dt} = \left(\dfrac{1}{R}\right)\left(\dfrac{M-2}{1-M}\right)\hat{v} + \left[\left(\dfrac{V}{R}\right)\left(\dfrac{2}{M}\right)\sqrt{\dfrac{1-M}{2\tau_L}}\right]\hat{d}_1 + \left[\left(\dfrac{M}{R}\right)\left(\dfrac{2-M}{1-M}\right)\right]\hat{v}_s & (2.89) \end{cases}$$

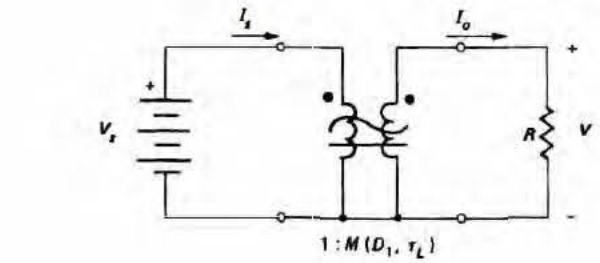
$$\hat{d}_2 = \left(-\frac{1}{V}\sqrt{\frac{2\tau_L}{1-M}}\right)\hat{v} + \left(\frac{1-M}{M}\right)\hat{d}_1 + \left(\frac{M}{V}\sqrt{\frac{2\tau_L}{1-M}}\right)\hat{v}_s \qquad (2.90)$$

These equations are defined in terms of M. If it is desirable to state them in terms of D_1, then the following relationship from Table 2.1 can be substituted:

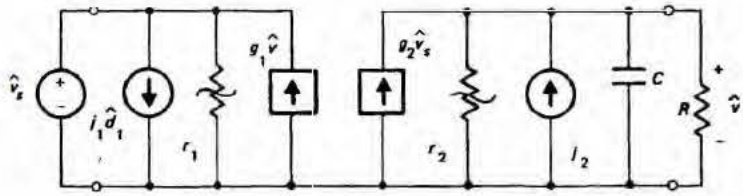
$$M = \frac{2}{1 + \sqrt{1 + 8\tau_L/D_1^2}} \qquad (2.91)$$

Equations (2.86) through (2.90) provide the basis for a mathematical model. From them, one can now proceed to find an equivalent circuit. Since the parameters I and $\hat{i}$ are not of any direct interest for most SPC designs, we will develop

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(A)



(B)

Fig. 2.22. The final state-space averaged models for the buck converter in the discontinuous mode.

a circuit model which does not include these two terms, much in the same manner as we followed to generate the circuit model in Fig. 2.21D.

The DC circuit model corresponding to the conditions of Eq. (2.87) is shown in Fig. 2.22A.

For convenience, Eq. 2.84 can be placed into the complex frequency domain by using Laplace transformation methods. Eliminating I and $\hat{i}$ and transforming this equation, we get:

$$\hat{v}_s(s) = \frac{1}{M}\left[sRC\left(\frac{1-M}{2-M}\right)+1\right]\hat{v}(s) - \left[\frac{2V}{M^2}\left(\frac{1}{2-M}\right)\sqrt{\frac{(1-M)^3}{2\tau_L}}\right]\hat{d}_1(s). \tag{2.92}$$

A circuit model which corresponds to Eq. 2.92 is illustrated in Fig. 2.22B, where:

$$j_1 = \frac{2V}{R}\sqrt{\frac{1-M}{2\tau_L}} \tag{2.93}$$

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$$j_2 = \frac{2V}{MR}\sqrt{\frac{1-M}{2\tau_L}} \tag{2.94}$$

$$r_1 = R\left[\frac{1-M}{M^2}\right] \tag{2.95}$$

$$r_2 = R(1-M) \tag{2.96}$$

$$g_1 = \frac{1}{R}\left(\frac{M^2}{1-M}\right) \tag{2.97}$$

$$g_2 = \frac{M}{R}\left(\frac{2-M}{1-M}\right). \tag{2.98}$$

Note that the resistive elements for r_1 and r_2 have a sinusoidal line drawn through their symbols. This is done to indicate that they are AC resistances *only* and they do not physically exist under DC conditions.

To conclude, a mathematical and a circuit model for the buck SPC have been evolved, both of which can be used as small-signal modeling aids when the converter is operating in a discontinuous mode. These circuit models can easily be inserted into more complex power processing networks, keeping in mind the AC and DC models for the discontinuous mode are not identical and, therefore, it will be necessary to solve for AC and DC quantities separately. In practice, such model changeover is not a great analysis inconvenience. From the mathematical model described by Eq. 2.92, one can easily derive the important small-signal transfer characteristics of the buck SPC operating in a discontinuous mode of operation.

$$\frac{\hat{v}(s)}{\hat{v}_s(s)} = M\left[\frac{1}{1+sRC\left(\frac{1-M}{2-M}\right)}\right] \tag{2.99}$$

$$\frac{\hat{v}(s)}{\hat{d}_1(s)} = \left[\left(\frac{2V}{M}\right)\left(\frac{1-M}{2-M}\right)\sqrt{\frac{1-M}{2\tau_L}}\right]\left[\frac{1}{1+sRC\left(\frac{1-M}{2-M}\right)}\right] \tag{2.100}$$

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3. The Boost Converter

In this chapter, we will examine the second of the two fundamental converter circuits, namely, the boost converter. The discussion will proceed in very much the same manner as it did in Chapter 2, but the end results will be quite different because the boost converter has very different properties from those of the buck converter. Even though the same components are used, the change in topology has a profound effect on how the converter operates.

In the case of the continuous-mode buck converter, the use of state-space averaging was admittedly an overkill because most of the characteristics could have been determined by viewing the circuit as a pulsed voltage source followed by a conventional low-pass filter. If that approach is used in the case of the boost converter, the answers derived would be wrong and would not include the movement of filter cutoff frequency as a function of SPC duty cycle and the nonminimum phase control-to-output transfer functions which are demonstrably present in real boost converters. The state-space averaging technique, however, does provide a very accurate model.

3.1. BOOST CONVERTER OPERATION

An ideal boost SPC circuit is shown in Fig. 3.1 with the waveforms for each operating mode established by the position of the SPDT switch (S) shown in Figs. 3.2 and 3.3.

During one complete switching cycle, S moves between positions A and B and the circuit topology changes from that shown in Fig. 3.1B to the network of Fig. 3.1C. At the beginning of the switching cycle, S is in position A. During time t_1, the inductor current (i_L) ramps upward from its value at $t = 0$ (I_a) towards a maximum value of I_b at $t = t_1$. At t_1, S moves to position B and the energy stored in L during time t_1 is now delivered to the output network (R and C). Consequently, i_L ramps downward during time t_2. If the converter is operating in the continuous mode, inductor current ramps down to a value of I_a at the end of the switching cycle, T_s. However, if the converter is operating in the discontinuous mode (Fig. 3.3), i_L at time t_2 is zero, since all of the stored energy

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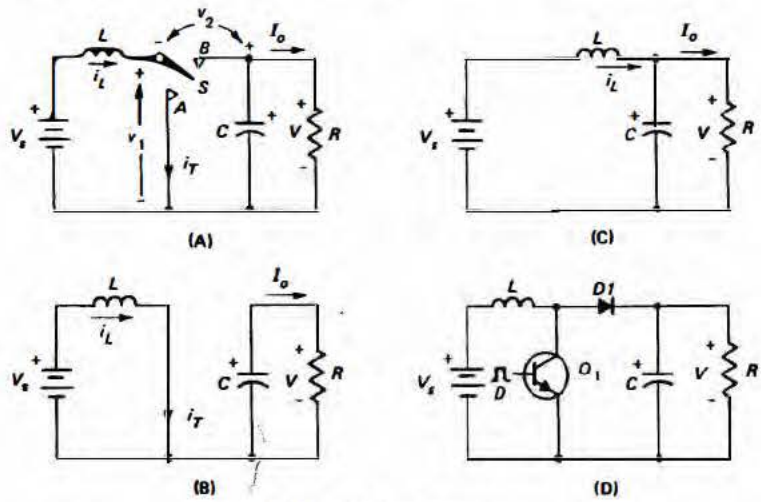


Fig. 3.1. The boost converter.

of the inductor has been delivered to the output. As was the case for the buck SPC, the operating mode of the boost SPC is of fundamental importance in determining the circuit characteristic waveforms and associated power transfer functions.

We can deduce many of the properties of the boost converter by examining the waveforms of Fig. 3.3. First, the output voltage must be greater than the input voltage. If this voltage relationship were not true, L would not discharge into the output network. In the continuous mode, the input current is non-pulsating, and its ripple magnitude can be made arbitrarily small by increasing the inductance of L. However, the input current during the discontinuous mode of operation is pulsating. The output current is always pulsating regardless of the mode of operation.

During intervals t_1 and t_3, when L is disconnected from the output, load energy needs are supported completely by C. Depending on operating mode and output power requirements, it may be necessary to make C quite large to meet the usual requirement of small output voltage ripple.

Current i_T is the collector current of the transistor switch (Q_1) in Fig. 3.1D. Comparing its waveform in Fig. 3.2 and that in Fig. 3.3, we see that its peak value is much higher in the discontinuous mode for a constant output voltage and load. It is evident that Q_1 must switch higher peak currents when it is turning off.

The DC input current (I_s) is the average value of i_L. For a given input power:

$$P_s = I_s V_s \tag{3.1}$$

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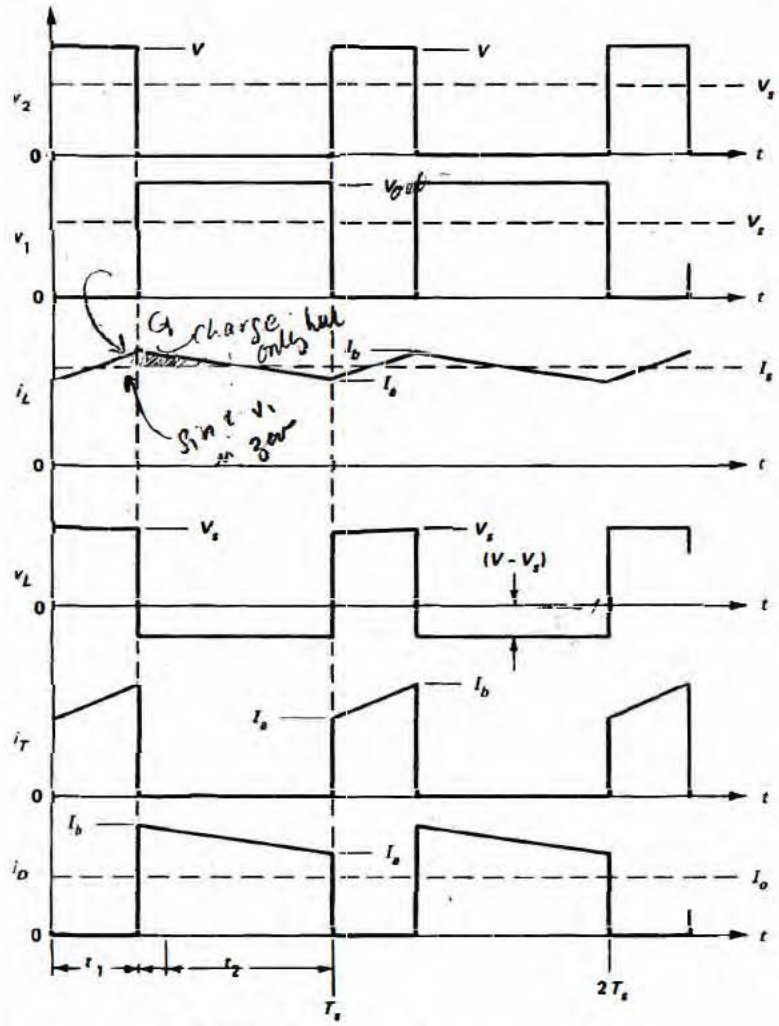


Fig. 3.2. Boost converter continuous mode waveforms.

Since I_a and I_b do not vary greatly with changes in V_s for a constant output voltage (V), the peak values for I_T and I_b in Fig. 3.3 are primarily functions of I_s. This dependency in the boost SPC has a counterpart in the buck SPC, where the peak values of I_T and I_b are determined by average output current (I_o). Therefore, in the boost SPC, as V_s increases, values of $I_{T(avg)}$, $I_{T(rms)}$ as well as I_b decrease.

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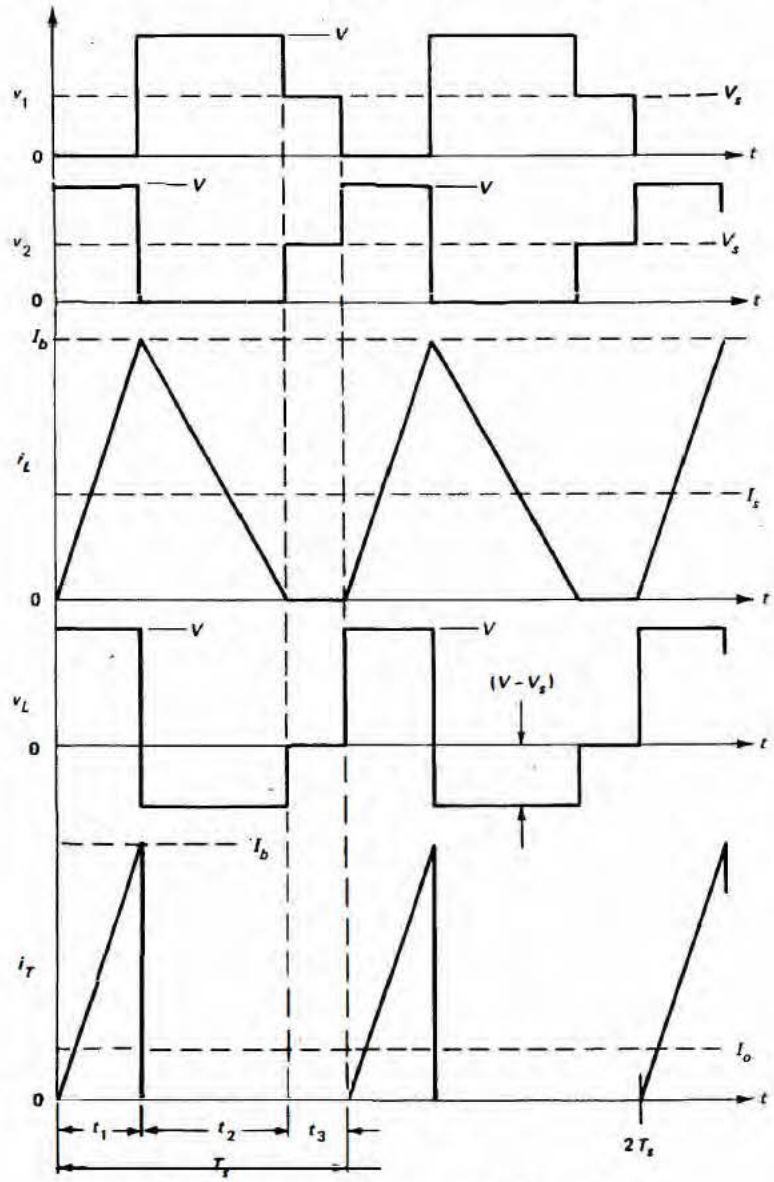


Fig. 3.3. Boost converter discontinuous mode waveforms.

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3.2. LARGE-SIGNAL STEADY-STATE CHARACTERIZATION

In this section, the characterization procedure will presume the ideal boost SPC of Fig. 3.4 for simplicity. In a high efficiency converter, the parasitic resistances must be small so that their omission will have only a small effect on the accuracy of the analysis.

As shown in Fig. 3.4, an input filter network ($L1$, $C1$) has been added to reflect a practical SPC. Equations defining the currents indicated in this circuit are summarized in Tables 3.1 and 3.2, where:

$$D_1 = \frac{t_1}{T_s} \tag{3.2}$$

$$D_2 = \frac{t_2}{T_s} \tag{3.3}$$

$$M = \frac{V}{V_s} \tag{3.4}$$

$$\tau_L = \frac{L}{RT_s} \tag{3.5}$$

$$I_o = \frac{V}{R} \tag{3.6}$$

$$I_s = I_{L(\text{avg})} \tag{3.7}$$

Considerable insight can be gained into the characteristics of the boost SPC by graphing some of the equations from Tables 3.1 and 3.2; however, we must first

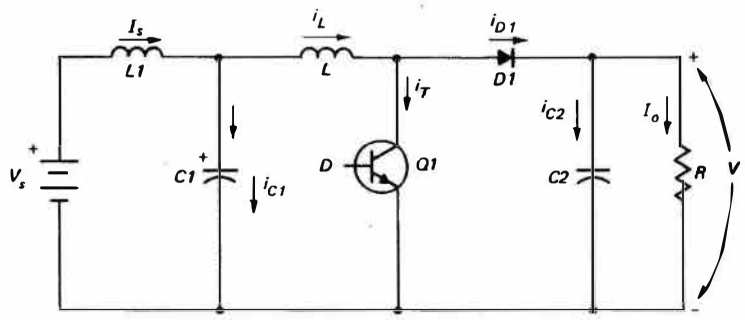


Fig. 3.4. Definition of the boost converter component currents.

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TABLE 3.1A. Definition of Variables for Boost Converter Equations.

τ_L	L/RT_s
T_S	Switching period
τ_{LC}	L_c/RT_s
L_c	Critical inductance
τ_{LC}	$(M-1)/2M^3 = D_1(1-D_1)^2/2$
D_1	ON duty cycle of switch
D_2	Diode conduction duty cycle
M	V/V_s
I_a	Minimum inductor current
I_b	Maximum inductor current

define the regions of operation where each set of equations will be valid. The boundary between the continuous and discontinuous modes is defined by τ_{LC}, where:

$$\tau_{LC} = \frac{M-1}{2M^3} \tag{3.8}$$

or alternatively:

$$\tau_{LC} = \frac{D_1(1-D_1)^2}{2}. \tag{3.9}$$

Graphs of Eqs. (3.8) and (3.9) are given in Figs. 3.5 and 3.6, respectively. We see that if $\tau_L > 2/27$, or approximately 0.075, then the converter will always remain in the continuous mode. Another interesting condition shown is the fact that, if $\tau_L < 0.075$, then an upper *and* a lower boundary condition exist, at which a mode change will occur. For example, if $\tau_L = 0.025$ the operating mode will change from continuous to discontinuous for $D_1 = 0.05$, and back to continuous when $D_1 = 0.73$. As τ_L is made larger, the range of D_1 over which the discontinuous mode exists will become progressively smaller.

With the areas of validity for the equations of Tables 3.1 and 3.2 established, graphical examination of one of them can now proceed. Fig. 3.7 shows the variation of M versus changes in D_1. For the continuous mode, this relationship

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TABLE 3.1B. Boost Converter Equations for Continuous Inductor Current.

Dependent Variable	$f(M, \tau_L, V, R)$	$f(D_1, \tau_L, V, R)$
M	M	$\frac{1}{1-D_1}$ *
D_1	$\frac{M-1}{M}$ *	$D_1 = D$
D_2	$\frac{1}{M}$	$1-D$
I_a	$\frac{V}{R}\left[M-\left(\frac{1}{2\tau_L}\right)\left(\frac{M-1}{M^2}\right)\right]$	$\frac{V}{R}\left[\frac{1}{1-D}-\left(\frac{1}{2\tau_L}\right)D(1-D)\right]$
I_b ✓	$\frac{V}{R}\left[M+\left(\frac{1}{2\tau_L}\right)\left(\frac{M-1}{M^2}\right)\right]$	$\frac{V}{R}\left[\frac{1}{1-D}+\left(\frac{1}{2\tau_L}\right)D(1-D)\right]$
$I_{L(\text{avg})}$	$\frac{V}{R}M$	$\left(\frac{V}{R}\right)\left(\frac{1}{1-D}\right)$
$I_{L(\text{rms})}$	$\frac{V}{R}\left[M^2+\frac{1}{3}\left(\frac{1}{2\tau_L}\right)^2\left(\frac{M-1}{M}\right)^2\right]^{1/2}$	$\frac{V}{R}\left[\left(\frac{1}{1-D}\right)^2+\frac{1}{3}\left(\frac{1}{2\tau_L}\right)^2D(1-D)\right]^{1/2}$
$I_{C1(\text{rms})}$	$\frac{V}{R}\left(\frac{1}{12\tau_L}\right)\left(\frac{M-1}{M^2}\right)$	$\frac{V}{R}\left[\frac{D(1-D)}{12\tau_L}\right]$
$I_{C2(\text{rms})}$	$\frac{V}{R}\left[(M-1)+\frac{1}{3}\left(\frac{1}{2\tau_L}\right)^2\left(\frac{1}{M}\right)\left(\frac{M-1}{M^2}\right)^2\right]^{1/2}$	$\frac{V}{R}\left[\frac{D}{1-D}+\frac{D}{12}\left(\frac{1-D}{\tau_L}\right)^2\right]^{1/2}$
$I_{T(\text{avg})}$	$\frac{V}{R}(M-1)$	$\left(\frac{V}{R}\right)\left(\frac{D}{1-D}\right)$
$I_{T(\text{rms})}$	$\frac{V}{R}\left[M(M-1)+\frac{1}{3}\left(\frac{1}{2\tau_L}\right)^2\left(\frac{M-1}{M^2}\right)^3\right]^{1/2}$	$\frac{V}{R}\left[\frac{D}{(1-D)^2}+\frac{1}{3}\left(\frac{1}{2\tau_L}\right)^2D^3(1-D)^3\right]^{1/2}$
$I_{D1(\text{avg})}$	$\frac{V}{R}$	$\frac{V}{R}$

*For $M > 3$, see equation 3.34 in text. 3.34 * $D' = 1-D$; $M = \frac{D'R}{R}$,

is quite nonlinear, with the value M rising rapidly as D_1 is increased. In contrast, in the discontinuous mode, the graphical relationship between M and D_1 is very nearly a straight line. This latter situation is surprising when one looks casually at the defining equation of this graph:

$$M = \frac{\sqrt{1+2D_1^2/\tau_L}}{2}x + \frac{1}{2} \tag{3.10}$$

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TABLE 3.2A. Boost Converter Equations for Discontinuous Inductor Current.

Dependent Variable	$f(M, \tau_L, V, R)$	$f(D_1, \tau_L, V, R)$
M	M	$\frac{1+\sqrt{1+2D_1^2/\tau_L}}{2}$
D_1	$\sqrt{2\tau_L M(M-1)}$	D_1
D_2	$\sqrt{\frac{2\tau_L M}{M-1}}$	$\left(\frac{\tau_L}{D_1}\right)(1+\sqrt{1+2D_1^2/\tau_L})$
I_a	0	0
I_b	$\frac{V}{R}\sqrt{\frac{2(M-1)}{\tau_L M}}$	$\frac{V}{R}\left[\frac{\sqrt{1+2D_1^2/\tau_L}-1}{D_1}\right]$
$I_{L(\text{avg})}$	$\frac{V}{R}M$	$\frac{V}{R}\left(\frac{1+\sqrt{1+2D_1^2/\tau_L}}{2}\right)$
$I_{L(\text{rms})}$	$\frac{V}{R}\left[\frac{8}{9}\frac{M(M-1)}{\tau_L}\right]^{1/4}$	$\frac{V}{R}\left[\frac{2}{3}\frac{D_1}{\tau_L}\right]^{1/2}$
$I_{C1(\text{rms})}$	$\frac{V}{R}\left[\sqrt{\frac{8}{9}\frac{M(M-1)}{\tau_L}}-M^2\right]^{1/2}$	$\frac{V}{R}\left[\frac{1+\sqrt{1+2D_1^2/\tau_L}}{2}\right]\left[\sqrt{\frac{8}{9}\frac{D_1(1-D_1)^2}{\tau_L}}-1\right]^{1/2}$
$I_{C2(\text{rms})}$	$\frac{V}{R}\left[\sqrt{\frac{8}{9}\frac{M-1}{\tau_L M}}-1\right]^{1/2}$	$\frac{V}{R}\left[\frac{2}{3}\left(\frac{\sqrt{1+2D_1^2/\tau_L}-1}{D_1}\right)-1\right]^{1/2}$
$I_{T(\text{avg})}$	$\frac{V}{R}(M-1)$	$\frac{V}{R}\left[\frac{\sqrt{1+2D_1^2/\tau_L}-1}{2}\right]$
$I_{T(\text{rms})}$	$\frac{V}{R}\left[\frac{8}{9}\frac{(M-1)^3}{\tau_L M}\right]^{1/4}$	$\frac{V}{R}\left[\frac{\sqrt{1+2D_1^2/\tau_L}-1}{\sqrt{3D_1}}\right]$
$I_{D1(\text{avg})}$	$\frac{V}{R}$	$\frac{V}{R}$

However, in most of the area where Eq. (3.10) is valid, we can state:

$$\frac{2D_1^2}{\tau_L} \gg 1. \tag{3.11}$$

Using the condition of Eq. (3.11) the value of M set by Eq. (3.10) can be approximated as:

$$M \approx \frac{1}{2} + \frac{D_1}{\sqrt{2\tau_L}}. \tag{3.12}$$

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TABLE 3.2B. Equations Normalized to τ_{LC}.

$\frac{I_a}{I_s} = 1 - \frac{\tau_{LC}}{\tau_L}$	Continuous Mode
$\frac{I_b}{I_s} = 1 + \frac{\tau_{LC}}{\tau_L}$	Continuous Mode
$\frac{I_{L(\text{rms})}}{I_s} = \left[1 + \frac{1}{3}\left(\frac{\tau_{LC}}{\tau_L}\right)^2\right]^{1/2}$	Continuous Mode
$\frac{I_b}{I_s} = 2\sqrt{\frac{\tau_{LC}}{\tau_L}}$	Discontinuous Mode
$\frac{I_{L(\text{rms})}}{I_s} = \left[\frac{16}{9}\left(\frac{\tau_{LC}}{\tau_L}\right)\right]^{1/4}$	Discontinuous Mode

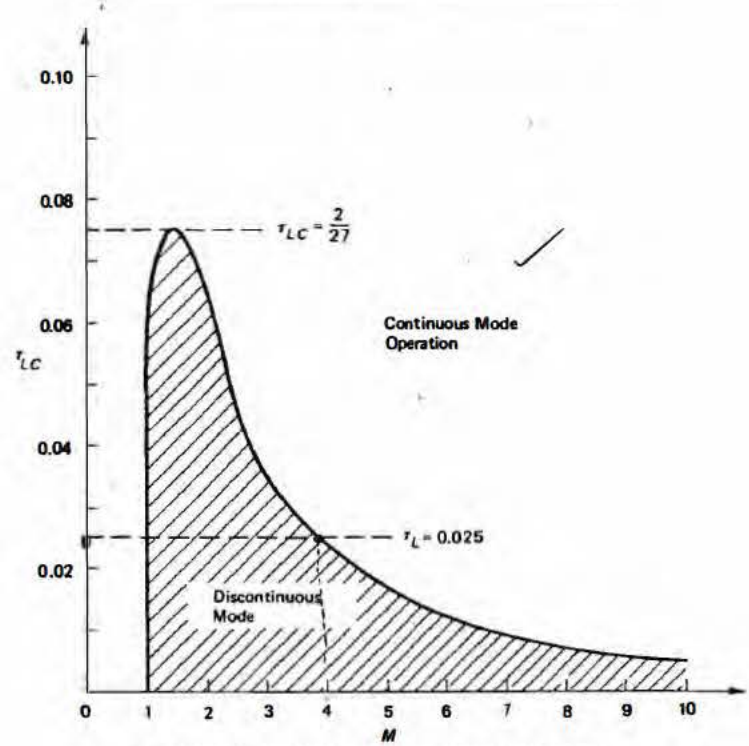


Fig. 3.5. Operating mode boundaries as a function of M.

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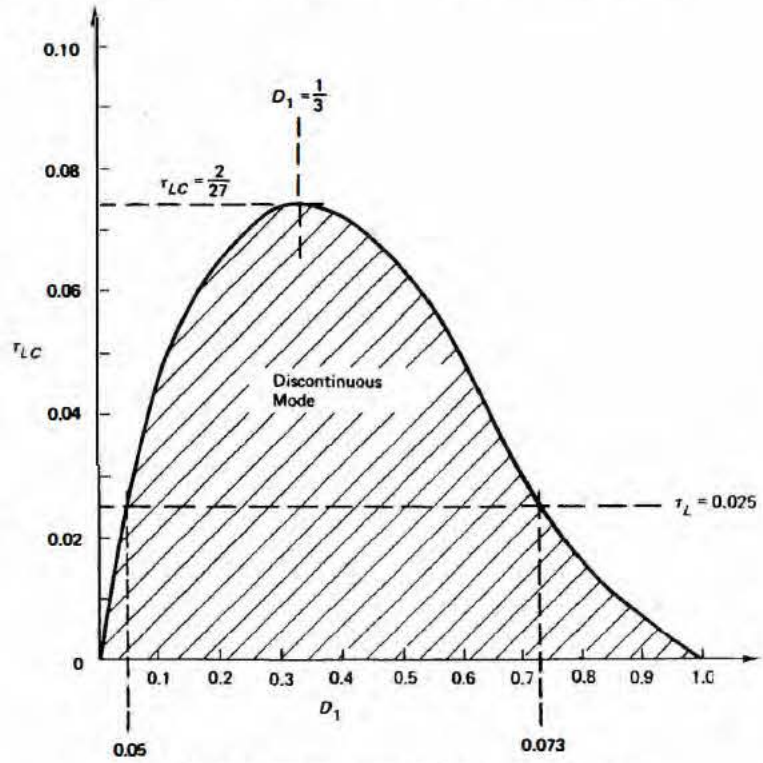


Fig. 3.6. Operating mode boundaries as a function of D_1.

If we compare the results of Eqs. (3.10) and (3.12) for values of D_1 and τ_L set at 0.5 and 0.01, respectively, an error of less than 1% will be found. Therefore, the simpler form of Eq. (3.10) will give results accurate for most analysis needs. Even if the value of τ_L is increased by a factor of ten, the error introduced by the use of Eq. (3.10) is only 3%.

As was the case for the buck SPC of the last chapter, the voltage control characteristics of Fig. 3.7 differs greatly between the two conduction modes. Although the conditions of this graph apply to an ideal boost SPC, the graph is a good representation of the control characteristic for practical boost converters, where M is less than three. For continuous-mode M values larger than three, the effects of any component parasitic resistances become quite noticeable. The associated plot of Fig. 3.7 does not continue its exponential climb, but actually reaches a peak and then begins to fall. This change will be demonstrated in Section 3.4, when component parasitics are added to the ideal boost SPC model.

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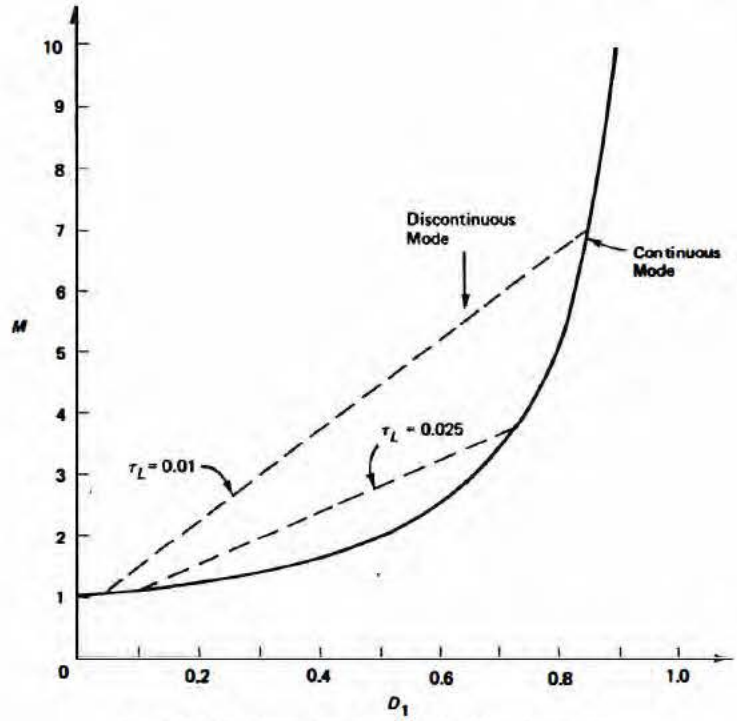


Fig. 3.7. DC control characteristic for the boost converter.

The variations in I_b and $I_{L\,(\mathrm{rms})}$ as τ_L is varied are shown in Figs. 3.8 and 3.9, respectively. From these graphs, the effect of τ_L on the amplitude of these particular currents can be clearly seen. In very much the same manner as was observed in the buck SPC, the amplitudes of these currents are always higher in the discontinuous mode and, in some cases, they can be very large. Thus, the use of the discontinuous mode for boost SPC operation is not advantageous for high output power.

3.3. LARGE-SIGNAL DYNAMIC CHARACTERIZATION

If the output load of a boost SPC is removed, or short-circuited, the converter reacts in a manner unlike that observed in the buck SPC of Chapter 2 under similar conditions.

In an output short-circuit condition, reducing the duty cycle of the switch to zero will not limit the amount of current drawn from the source, because the

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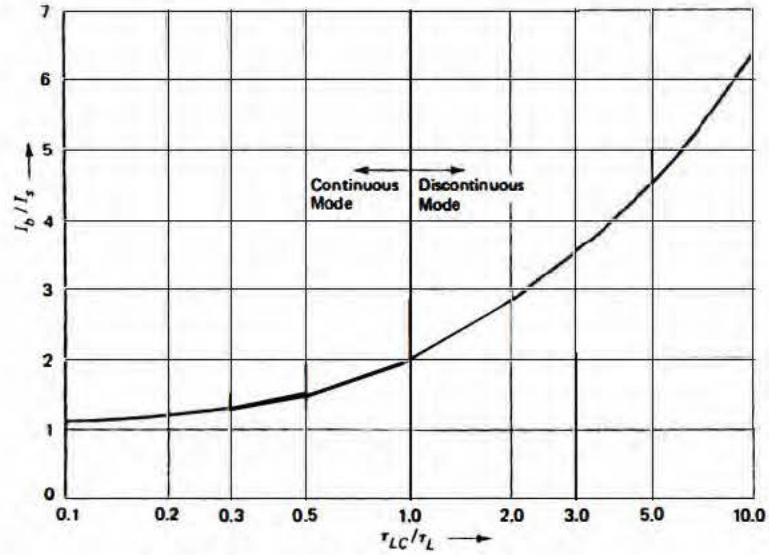


Fig. 3.8. Inductor peak current amplitude as a function of inductance value.

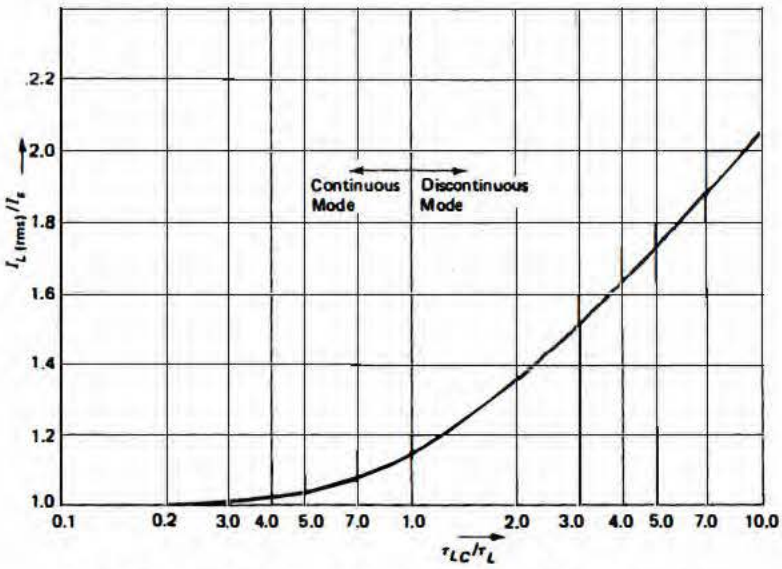


Fig. 3.9. Inductor rms current amplitude as a function of inductance value.

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switch is *not* in series with it. Reducing the duty cycle of switch will provide output overload protection only until the output voltage equals the source voltage. At that point, there is no inherent mechanism for output current limiting, other than parasitic inductor resistance and diode impedance, both of which are normally very small. If output current overload must be tolerated, then an additional switch in series with the source must be added. This is a fundamental problem common to all boost-derived converters. Fortunately, the problem can be resolved fairly simply. Practical solutions are treated in Chapter 9.

If the boost SPC output is open-circuited, another serious problem arises. If the switching action of the SPC is continued in the absence of an output load, the energy stored in C will increase. The output voltage will rise until a component fails.

A short anecdote will serve to emphasize the potential seriousness of the problem. Some years ago, one of the authors was familiarizing a young electronics engineer with the design of SPCs. One of his job assignments was to design and build a basic boost SPC, and he was forewarned never to operate the boost SPC without proper loading. This admonition apparently was not taken seriously, for shortly afterwards, a loud bang was heard at the engineer's work bench. Upon investigation by co-workers, he was found to be bleeding from his forehead, almost exactly between the eyes, where the inside portions of an electrolytic capacitor had struck him. Apparently, the output filter capacitor had exploded when the load of the converter was removed. He finally got the point (no pun intended) and, we trust you do too, from this account of a very unfortunate experience.

Applications where the output loading of a boost SPC could be removed are frequently encountered by designers. In these instances, overvoltage or stress problems from unloading can be eliminated by adding auxiliary circuitry in the SPC control system to sense an overvoltage condition and then reduce switch duty cycle D to zero.

When V_s is first applied to the boost SPC of Fig. 3.1D, and the shunt switch is OFF, the input inrush current is limited only by the characteristics of a low-pass filter network formed by R, L, and C. The shape of the inrush source current transient is one-half cycle of a damped sinusoid, as shown in Fig. 3.10. The maximum value of this transient may be many times that of the steady-state average value of I_s. This high peak current can produce damage to filter elements or to the source. For these reasons, SPC input specifications often call for limiting the amplitude of inrush current.

An additional complication may arise if the inrush current reaches a value large enough to cause the core of L to saturate. Should this happen, the waveforms in Fig. 3.10 will no longer apply, and even higher values of inrush current will occur, limited only by source impedances and parasitic resistances of L, D, and C.

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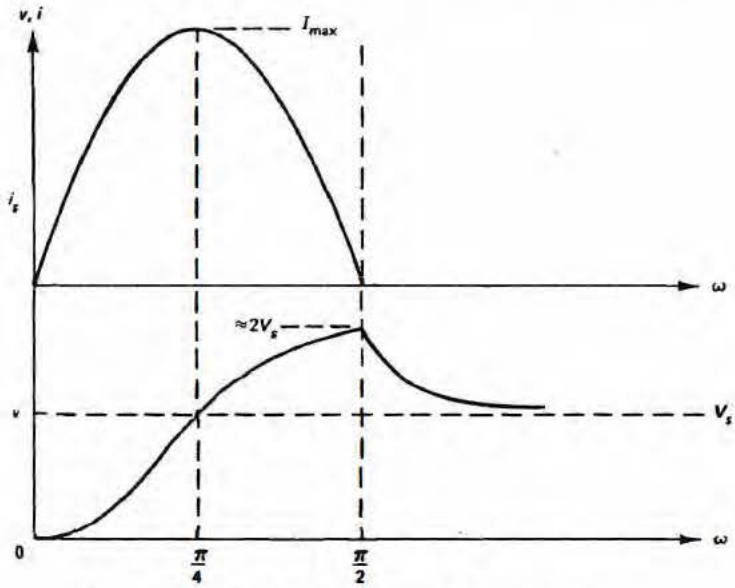


Fig. 3.10. Inrush current waveform at source turn-on.

In addition to potentially high inrush currents at turnon, there is another problem peculiar to the boost SPC relative to starting sequence. Some boost designs are structured so as to begin SPC switching action with the application of V_s. When V_s is first applied, the output voltage (V_o) will be initially zero and begin to rise toward the desired output voltage value. During this build-up interval, the auxiliary voltage control circuitry will push the value of D to a maximum and decrease it as output voltage increases. If the maximum value of D is too large, the circuit will lock up and V_o will not be built up. This situation is usually accompanied by both excessive input inductor as well as switch current values. It is normal practice, therefore, to limit the maximum value of D to a value slightly larger than that required for normal output voltage. An analytical determination of the maximum duty cycle is presented in Section 3.4.

It is well to remember that these potentially damage-producing properties of the basic boost SPC are retained in their more complex derivative topologies. In boost-derived SPCs which contain a DC transformation element, the inrush current occurs at the onset of SPC switching action, rather than at the time when V_s is first applied. Nevertheless, the potential stress problems discussed earlier are still possible.

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3.4. STATE-SPACE AVERAGED MODEL FOR THE CONTINUOUS MODE

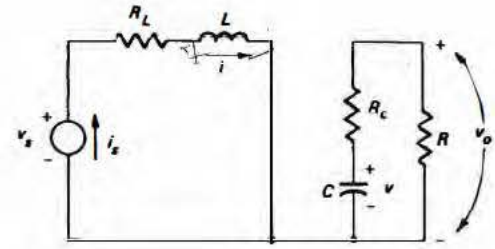
The same processes that were used in Chapter 2 for deriving general small-signal models for the buck SPC can be repeated here for the boost SPC.

Figure 3.11 shows the equivalent circuits for each of the two possible states of the boost SPC in the continuous mode. We have now included the parasitic resistances of the inductor and output capacitor to make our models practical in nature.

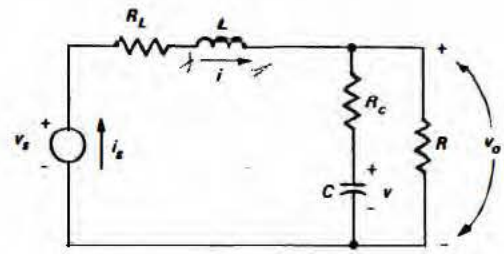
The corresponding circuit equations, in state-variable form, for the network of Fig. 3.11A are:

$$\frac{di}{dt} = -\left[\frac{R_L}{L}\right] i + \frac{v_s}{L} \tag{3.13}$$

$$\frac{dv}{dt} = -\frac{v}{(R + R_c)C} \tag{3.14}$$



(A)



(B)

Fig. 3.11. Boost converter equivalent circuits.

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$$v_o = \left[\frac{R}{R + R_c}\right] v \tag{3.15}$$

$$i_s = i. \tag{3.16}$$

For network B of Fig. 3.11, the describing circuit equations are:

$$\frac{di}{dt} = -\left[\frac{R_L + (R \| R_c)}{L}\right] i - \frac{1}{L}\left[\frac{R}{R + R_c}\right] v + \frac{v_s}{L} \tag{3.17}$$

$$\frac{dv}{dt} = \left[\frac{R}{(R + R_c)C}\right] i - \frac{v}{(R + R_c)C} \tag{3.18}$$

$$v_o = (R \| R_c) i + \left[\frac{R}{R + R_c}\right] v \tag{3.19}$$

$$i_s = i. \tag{3.20}$$

Using the same assumptions for averaging that were established in Chapter 2, the state-space averaged circuit equations for the boost SPC are:

$$\frac{di}{dt} = -\left[\frac{R_L + (1 - d)(R \| R_c)}{L}\right] i - \left[\frac{(1 - d)R}{L(R + R_c)}\right] v + \frac{v_s}{L} \tag{3.21}$$

$$\frac{dv}{dt} = \left[\frac{(1 - d)R}{(R + R_c)C}\right] i - \frac{v}{(R + R_c)C} \tag{3.22}$$

$$v_o = (1 - d)(R \| R_c) i + \left[\frac{R}{R + R_c}\right] v \tag{3.23}$$

$$i_s = i. \tag{3.24}$$

A circuit model corresponding to the above equations is shown in Fig. 3.12. In this model, an output low-pass filter network is evident as was the case for the buck SPC model in the continuous mode. However, the values for L and its series resistances are now modulated functions of the switch duty cycle. It follows then that the output filter network characteristics will change as a function of d. This was not the case in the buck SPC model and represents an important difference between these two converters.

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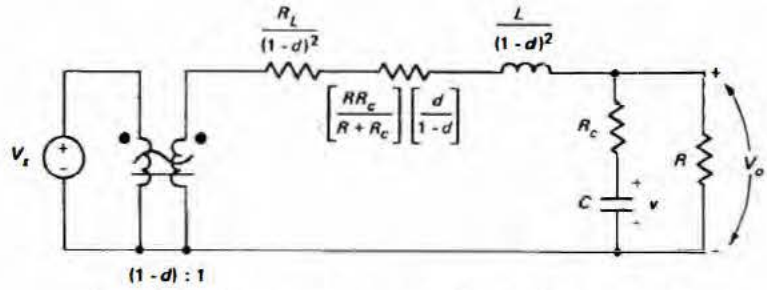


Fig. 3.12. Initial state-space averaged model for the boost converter.

Continuing the process of model development, we can now perturb Eqs. (3.21) through (3.24) using the same small-signal conventions that were employed in Chapter 2. As a result of these perturbations, the following relationships are established:

DC

$$0 = -[R_L + (R\|R_c)D']I - \left(\frac{RD'}{R+R_c}\right)V + V_s \tag{3.25}$$

$$0 = (RD')I - \frac{V}{(R+R_c)} \tag{3.26}$$

$$V_o = (R\|R_c)D'I + \left(\frac{R}{R+R_c}\right)V \tag{3.27}$$

$$I_s = I \tag{3.28}$$

AC

$$\frac{d\hat{i}}{dt} = -\left[\frac{R_L + (R\|R_c)D'}{L}\right]\hat{i} - \left[\frac{RD'}{(R+R_c)L}\right]\hat{v} + \left(\frac{V_o}{D'L}\right)\left(\frac{D'R+R_c}{R+R_c}\right)\hat{d} + \frac{\hat{v}_s}{L} \tag{3.29}$$

$$\frac{d\hat{v}}{dt} = \left[\frac{RD'}{(R+R_c)C}\right]\hat{i} - \left[\frac{I}{(R+R_c)C}\right]\hat{v} - \left[\frac{V_o}{D'(R+R_c)C}\right]\hat{d}, \qquad \hat{i}_s = \hat{i} \tag{3.30}$$

$$\hat{v}_o = (R\|R_c)D'\hat{i} + \left(\frac{R}{R+R_c}\right)\hat{v} - \left[\frac{V_o R_c}{D'(R+R_c)}\right]\hat{d}. \tag{3.31}$$

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From the DC equations, we can readily derive expressions for V, I, and M as:

$$I = \frac{V_o}{D'R'} \qquad D' = 1 - D \tag{3.32}$$

$$V = V_o \tag{3.33}$$

$$M = \frac{D'R}{R'} \tag{3.34}$$

where

$$R' = R_L + (R \| R_c)D' + \frac{R^2(D')^2}{R + R_c}. \tag{3.35}$$

Equation (3.34) can be rearranged so that it takes the form of the voltage gain function of an ideal boost SPC multiplied by a correction factor produced by the SPC's parasitic resistances:

$$M = \underbrace{\left(\frac{1}{D'}\right)}_{\text{IDEAL}}\underbrace{\left[\frac{(D')^2R}{R'}\right]}_{\text{CORRECTION FACTOR}}. \tag{3.36}$$

Figure 3.13 shows a graph of Eq. (3.34) comparing an ideal M versus D characteristic ($R_L = R_c = 0$) to one in which $R_L = R_c = 0.01R$. As shown, for M values less than 3, the difference between actual and ideal relationships is very small. For M values greater than 3, the two curves diverge from one another rapidly and the effect of the correction factor in Eq. (3.36) becomes apparent in the nonideal case. Values of parasitic resistances for an efficient conversion process are usually less than 1% of the converter's maximum load value, and, frequently, even smaller parasitic values can be realized by proper filter component selection.

The departure of Eq. (3.36) from the ideal curve of Fig. 3.13 at high duty cycles poses a problem in SPC applications. In this example, for $R_L = R_c = 0.01R$, the maximum value for M is 4.7 and occurs at a duty cycle of 0.88. Should the source voltage (V_s) drop in value, any output voltage regulation control electronics of the converter would attempt to increase D, and therefore M, to maintain a constant output voltage. If the SPC's regulation controls were designed so as to allow a duty cycle of 0.88 to be exceeded under these circumstances, then the output voltage would drop, resulting in a further increase in the value of D. This increase in D would continue until a maximum control limit value is

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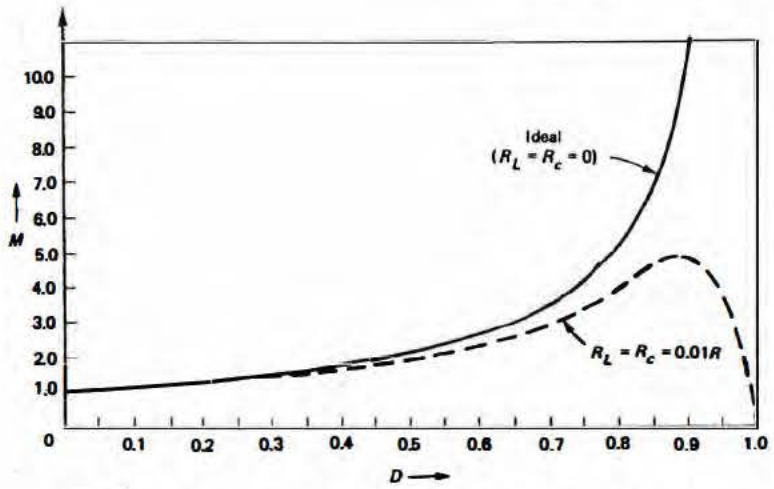


Fig. 3.13. A comparison between ideal and practical DC control functions.

reached. Therefore, in our practical example, it is possible for related voltage control electronics to produce a *latch-up* condition, wherein the SPC switch would be placed in a full conduction condition. This is a primary reason that all boost SPC systems should be designed so that their maximum duty cycle is limited to prevent latch-up. For a more detailed discussion of this lock-up problem, the reader should examine the contents of Ref. 4 given in the text bibliography.

We can now complete our mathematical model by transforming Eqs. (3.28) through (3.31) into the complex frequency domain:

$$\frac{V_o}{D'}\left[\frac{D'R + R_c}{R + R_c}\right]\hat{d}(s) + \hat{v}_g(s) = [sL + R_L + D'(R \| R_c)]\hat{i}(s) + \left[\frac{RD'}{R + R_c}\right]\hat{v}_g \tag{3.37}$$

$$\left(\frac{V_o}{D'}\right)\hat{d}(s) = (D'R)\hat{i}(s) - [1 + s(R + R_c)C]\hat{v}(s) \tag{3.38}$$

$$\hat{v}_o(s) = D'(R \| R_c)\hat{i}(s) + \left[\frac{R}{R + R_c}\right]\hat{v}(s) - \left[\frac{V_o R_c}{D'(R + R_c)}\right]d(s) \tag{3.39}$$

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$$\hat{i}_s(s) = \hat{i}(s). \tag{3.40}$$

Examination of the mathematical model equations shows that they have exactly the same form as the model for the buck converter derived in Chapter 2. Only the proportionality constants produced by the circuit element values are different. This implies that any equivalent circuit model topology established by the above equations will be *identical* to that of the buck SPC, and differ only in element values. From this observation and a little bit of equation manipulation (see Chapter 10), we can formulate the small-signal continuous circuit model of the boost SPC as shown in Fig. 3.14, where:

$$E = V_o\left[\frac{R}{R+R_c} - \frac{R_L}{(D')^2 R}\right] \tag{3.41}$$

$$f_1(s) = 1 - s\left[\frac{L}{\dfrac{(D'R)^2}{R+R_c} - R_L}\right] \tag{3.42}$$

$$J = \frac{V_o}{(D')^2 R}, \qquad f_2(s) = 1 \tag{3.43}$$

$$R_e = \frac{R_L + (R \| R_c)DD'}{(D')^2} \tag{3.44}$$

$$L_e = \frac{L}{(D')^2}, \qquad f_c = \frac{1}{2\pi\sqrt{L_e C}}. \tag{3.45}$$

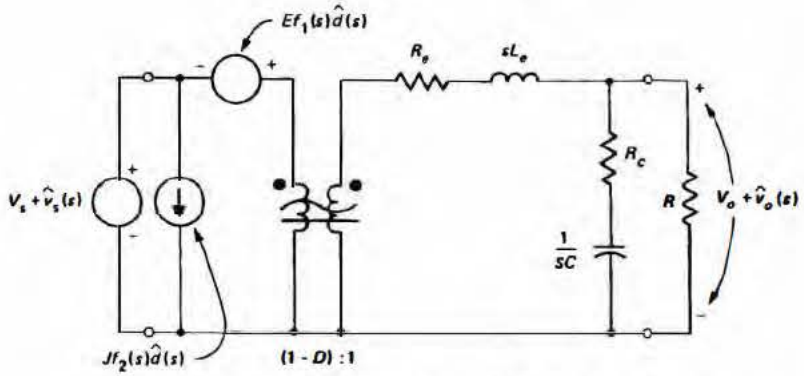


Fig. 3.14. Final state-space averaged model for the boost converter.

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Once again, the output network of the model in Fig. 3.14 takes the form of a low-pass filter; however, some filter elements (R_e and L_e) are functions of D. In a closed-loop voltage control application, these variations will cause f_c to change as a function of D. Obviously, this will complicate the design of the SPC voltage control electronics from stability and bandwidth standpoints.

We see also that the $\hat{d}(s)$ voltage generator has a complex amplitude $f_1(s)$ and that $f_1(s)$ has a *right* half-plane zero! The right half-plane zero appears as a consequence of the switching action, and seriously complicates the problem of stabilizing the control loop.

A simple physical explanation for the presence of this zero can be found by considering boost control circuit reaction to a step increase in $D(\Delta D)$, which is equivalent to commanding a step increase in output voltage. The initial reaction of the boost SPC system would be to keep its shunt switch on for a corresponding period, $D + \Delta D$. During this interval, V_o will drop slightly, since the output voltage must be sustained by the energy in $C2$ for a slightly longer time than was necessary on the immediate preceeding switching cycle of the SPC. The initial slope of the output response (dv_o/dt) is therefore negative for a positive input change. This phenomenon is characteristic of a system with a zero in the right half of the complex frequency plane. The negative rate of change of v_o exists only momentarily, and then becomes positive in value as output voltage rises in response to control increases in converter duty cycle D.

From the small-signal equations, we can now derive some SPC transfer functions of interest:

$$\frac{\hat{v}_o(s)}{\hat{v}_s(s)} = \left[\frac{D'R}{R'}\right] \cdot \left\{ \frac{(1 + sR_cC)}{s^2LC\left(\frac{R + R_c}{R'}\right) + s\left[\frac{L}{R'} + \left(\frac{RR_L + R_cR_L + D'RR_c}{R'}\right)C\right] + 1} \right\} \tag{3.46}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \left[\frac{V_o}{D'R'}\right]\left[\frac{(D'R')^2}{R + R_c} - R_L\right] \cdot \left[\frac{(1 + sR_cC)\left[1 - s\left(\frac{L}{\frac{(D'R)^2}{R + R_c} - R_L}\right)\right]}{s^2LC\left[\frac{R + R_c}{R'}\right] + s\left[\frac{L}{R'} + \left(\frac{RR_L + R_cR_L + D'RR_c}{R'}\right)C\right] + 1} \right] \tag{3.47}$$

In both of these equations, a zero appears because of the presence of output capacitor ESR (R_c) as well as a complex pole that moves as a function of D.

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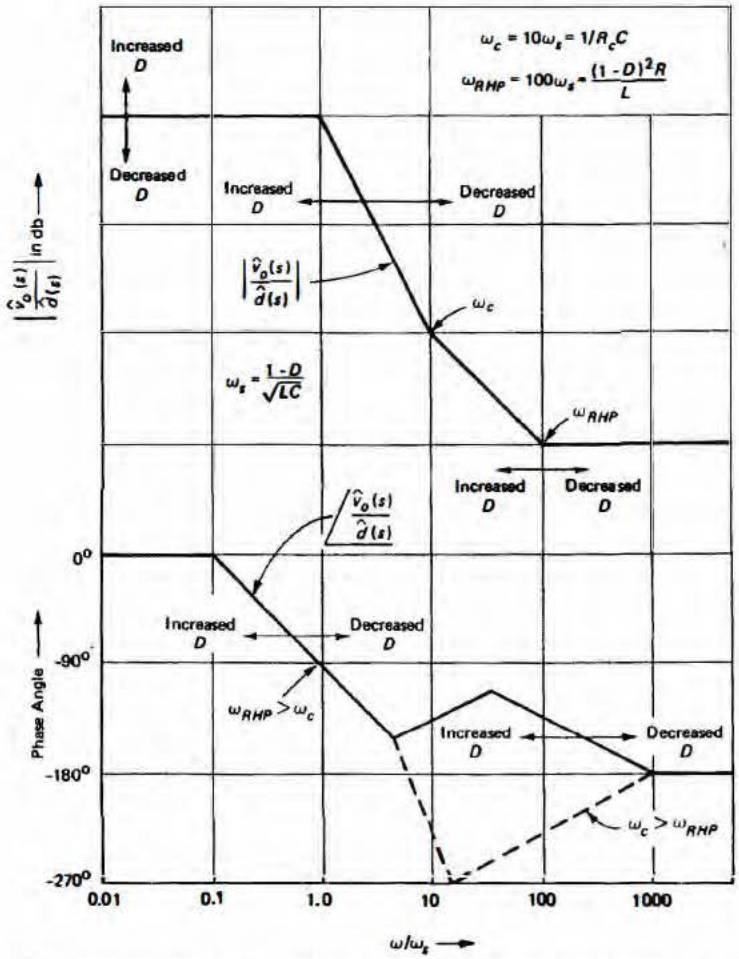


Fig. 3.15. Asymptotic gain and phase approximations for the small-signal control-to-output transfer function of a typical boost converter.

However, the right half-plane zero discussed earlier appears only in the control-to-output transfer function. An asymptotic gain and phase approximation for this latter function is shown in Fig. 3.15, where the deleterious effect of the right half-plane zero on system stability is very apparent when compared to the same graph for the buck SPC (Fig. 2.17). In Fig. 3.15, it has been presumed that the ESR effect of the output capacitor results in a break frequency lower

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than that caused by the right half-plane zero. If the frequency relationships of these two zero break points are interchanged, the gain plot will remain unchanged, but the phase angle plot (as shown by the dashed line) will move in a direction so as to even more severely complicate control measures for system stability.

3.5. STATE-SPACE AVERAGED MODEL FOR THE DISCONTINUOUS MODE

Like its counterpart SPC of Chapter 2, the boost converter assumes three different states during the discontinuous mode of operation. These are shown in Fig. 3.16. For each of the networks of Fig. 3.16, a set of equations can be written:

$$\text{A}\begin{cases} \dfrac{di}{dt} = \dfrac{v_s}{L} & (3.48) \\ \dfrac{dv}{dt} = -\dfrac{v}{RC} & (3.49) \end{cases}$$

$$\text{B}\begin{cases} \dfrac{di}{dt} = -\dfrac{v}{L} + \dfrac{v_s}{L} & (3.50) \\ \dfrac{dv}{dt} = \dfrac{i}{C} - \dfrac{v}{RC} & (3.51) \end{cases}$$

$$\text{C}\begin{cases} \dfrac{di}{dt} = 0 & (3.52) \\ \dfrac{dv}{dt} = -\dfrac{v}{RC}. & (3.53) \end{cases}$$

The duty cycle periods associated with the three networks of Fig. 3.16 are defined as follows:

$$\text{A:} \quad d_1 = \frac{t_1}{T_s} \tag{3.54}$$

$$\text{B:} \quad d_2 = \frac{t_2}{T_s} \tag{3.55}$$

$$\text{C:} \quad d_3 = 1 - d_1 - d_2. \tag{3.56}$$

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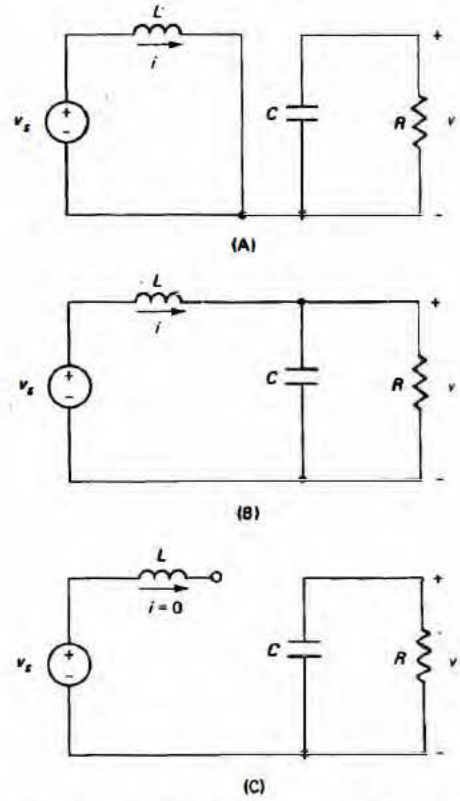


Fig. 3.16. Equivalent circuits for the boost converter operating in the discontinuous mode.

We can now perform the state-space averaging step, keeping in mind that di/dt is zero for the same reasons that were evident in the buck SPC during the discontinuous mode. The resulting averaged equations are:

$$0 = -d_2 v + (d_1 + d_2) v_s \tag{3.57}$$

$$\frac{dv}{dt} = \left(\frac{d_2}{C}\right) i - \frac{v}{RC}. \tag{3.58}$$

Again, the lost state variable, i, can be replaced by:

$$i \equiv \frac{i_b}{2} = \left[\frac{d_1}{2R\tau_L}\right] v_s. \tag{3.59}$$

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Construction of the circuit topology corresponding to Eqs. (3.57), (3.58), and (3.59) would reveal that the inductor does not appear in the resulting circuit.

Perturbation of Eqs. (3.57) through (3.59) and separation of AC and DC components result in the following expressions:

$$\text{DC}\begin{cases} 0 = -D_2V + (D_1 + D_2)V_s & (3.60)\\ 0 = D_2I - \dfrac{V}{R} & (3.61)\\ I = \dfrac{D_1V_s}{2R\tau_L} & (3.62)\end{cases}$$

$$\text{AC}\begin{cases} 0 = -D_2\hat{v} + V_s\hat{d}_1 - (V - V_s)\hat{d}_2 + (D_1 + D_2)\hat{v}_s & (3.63)\\ \dfrac{dv}{dt} = \left[\dfrac{D_2}{C}\right]\hat{i} - \dfrac{\hat{v}}{RC} + \left[\dfrac{I}{C}\right]\hat{d}_2 & (3.64)\\ \hat{i} = \left[\dfrac{V_s}{2R\tau_L}\right]\hat{d}_1 + \left[\dfrac{D_1}{2R\tau_L}\right]\hat{v}_s & (3.65)\end{cases}$$

The mathematical model described by the above relationships has terms including the dependent variables D_2 as well as $\hat{d}_2$. With a bit of manipulation, these dependent terms can be eliminated and the model then becomes:

$$\text{DC}\begin{cases} I = \dfrac{V}{R}\sqrt{\dfrac{M-1}{2\tau_L M}} & (3.66)\\ V = MV_s & (3.67)\end{cases}$$

$$\text{AC}\begin{cases} \hat{i} = \dfrac{V}{R}\left[\dfrac{1}{2\tau_L M}\right]\hat{d}_1 + \dfrac{1}{R}\left[\sqrt{\dfrac{M(M-1)}{2\tau_L}}\right]\hat{v}_s & (3.68)\\ C\dfrac{dv}{dt} = -\dfrac{1}{R}\left[\dfrac{2M-1}{M-1}\right]\hat{v} + \left[\dfrac{2V}{R}\right]\dfrac{\hat{d}_1}{\sqrt{2\tau_L M(M-1)}} + \dfrac{M}{R}\left[\dfrac{2M-1}{M-1}\right]\hat{v}_s & (3.69)\\ \hat{d}_2 = -\dfrac{1}{V}\left[\sqrt{\dfrac{2\tau_L M^3}{(M-1)^3}}\right]\hat{v} + \dfrac{\hat{d}_1}{M-1} + \dfrac{1}{V}\left[\dfrac{M}{M-1}\right]^2[\sqrt{2\tau_L M(M-1)}]\hat{v}_s & (3.70)\end{cases}$$

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The above equations are stated in terms of M. If one would rather have them expressed in terms of D_1, then a substitution is possible:

$$M = \frac{1 + \sqrt{1 + 2D_1^2/\tau_L}}{2}. \tag{3.71}$$

For convenience, we will transform Eq. (3.69) into the complex frequency domain, obtaining:

$$M\hat{v}_s(s) = \left[1 + sRC\left(\frac{M-1}{2M-1}\right)\right]\hat{v}(s) - \left[\frac{2V}{2M-1}\right]\left[\sqrt{\frac{M-1}{2\tau_L M}}\right]\hat{d}_1. \tag{3.72}$$

If we compare Eqs. (3.67) and (3.72) with their buck SPC counterparts of Chapter 2 in the discontinuous mode [Eqs. (2.87) and (2.92), respectively], the equation form is identical and each set differs only in the proportionality constant. This allows the use of the buck circuit model with different element values, as shown in Fig. 3.17, where:

$$j_1 = \frac{2V}{R}\sqrt{\frac{M}{2\tau_L(M-1)}} \tag{3.73}$$

$$j_2 = \frac{2V}{R\sqrt{2\tau_L M(M-1)}} \tag{3.74}$$

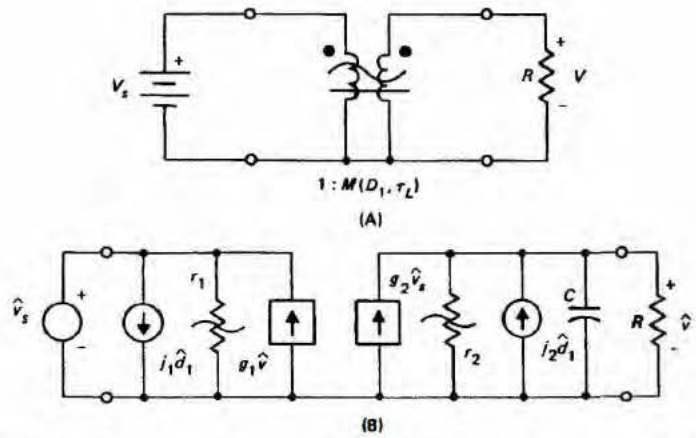


Fig. 3.17. Final state-space averaged models for the boost converter operating in the discontinuous mode.

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$$r_1 = \left[\frac{M-1}{M^3}\right]R \tag{3.75}$$

$$r_2 = \left[\frac{M-1}{M}\right]R \tag{3.76}$$

$$g_1 = \frac{1}{R}\left[\frac{M}{M-1}\right] \tag{3.77}$$

$$g_2 = \frac{1}{R}\left[\frac{M(2M-1)}{M-1}\right]. \tag{3.78}$$

From the models of Figs. 3.17A and 3.17B, the input-to-output and control-to-output transfer functions can easily be derived as:

$$\frac{\hat{v}(s)}{\hat{v}_s(s)} = \frac{M}{1 + sRC\left(\frac{M-1}{2M-1}\right)} \tag{3.79}$$

$$\frac{\hat{v}(s)}{\hat{d}(s)} = \left[\frac{2V}{2M-1}\right]\left[\sqrt{\frac{M-1}{2\tau_L M}}\right]\left[\frac{1}{1 + sRC\left(\frac{M-1}{2M-1}\right)}\right]. \tag{3.80}$$

By inspection, we see that both of these transfer functions have a single-pole characteristic, which will move as input voltage changes, thus altering the value of M. Also note that the right half-plane zero, which was present in the continuous mode, is *not* present in the discontinuous mode model for the boost SPC.

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4. DC Transformers

The buck and boost SPCs are fundamental building blocks from which more complex power processing systems can be constructed. However, both of these fundamental SPCs have practical conversion limitations that can only be overcome by the use of another SPC element–*the DC transformer*. Recall that each of the basic converters can only accommodate one input and provide only one output with input and output sharing a common return reference point. Definite limits on their output voltage ranges relative to their input voltage values are evident. All of these limitations can be overcome by the use of additional DC transformation functions, the ideal form of which is depicted in Fig. 4.1. An ideal transformer element would pass all signal frequencies from DC to light with no power loss, provide any selected transformation ratio of voltage or current, provide complete isolation between its input and its output, process power in either direction with equal facility and, finally, provide for additional inputs or outputs if required.

Obviously, such a perfect transformation device does not physically exist and, fortunately, perfection is rarely required. Many circuits which approximate the characteristics of an ideal transformation element do exist and are quite practical, especially if unlimited bandwidth of signal processing is not required.

4.1. TYPICAL CONFIGURATIONS

One of the most common SPC circuits used as a DC transformer element in a power processor is shown in Fig. 4.2A. This circuit topology is often called a "push-pull" converter, or *parallel DC transformer*, in reference to the alternating conduction actions of the two primary-side switches (S1 and S2) and the secondary-side rectifier elements (D1 and D2). In Fig. 4.2A, the secondary rectifier connection is commonly called a *full-wave center-tapped* connection. However, there are other rectifier connections, such as the one shown in Fig. 4.2B. Here, this particular form is in a *full-bridge* connection. Regardless of their output rectifier connection, both circuits of Fig. 4.2 are classified as parallel DC transformers.

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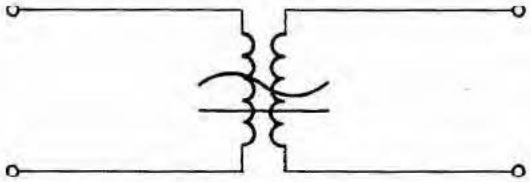


Fig. 4.1. The ideal transformer.

Switches S1 and S2 operate alternately, with conduction duty cycles of 50% during one complete switching cycle. These switching actions generate a symmetrical and alternating voltage across the primary of T1. Transformer T1 is a normal high-frequency AC transformer designed to operate at the switching rates of S1 and S2. Due to the AC voltage applied to N_p on each switching half

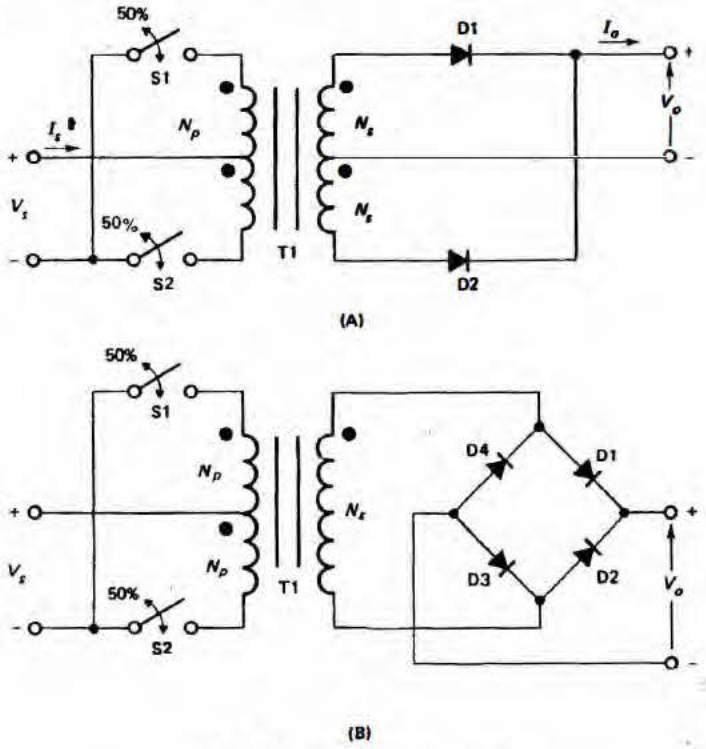


Fig. 4.2. The parallel DC transformer.

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cycle, an AC voltage will appear on N_s such that:

$$V_o = V_s\left[\frac{N_s}{N_p}\right] \tag{4.1}$$

Transformer T1 provides desired voltage transformation ratio as well as input-to-output ground return isolation, if so desired. The corresponding AC voltages across the secondary windings of T1 are rectified by D1 and D2 so as to produce a DC voltage determined by Eq. (4.1). The circuits of Fig. 4.2 thus perform two series conversion steps, (DC-to-AC and AC-to-DC, respectively) to realize a DC-DC transformation function.

The voltage which appears across a nonconducting primary switch in this DC-DC transformer system is $2V_s$, as the voltage across one half of the total primary winding of T1 (N_p) must be reflected into its other half. The peak current in each of the two primary switches is equal to the input average current, I_s, when each is ON.

In addition to this parallel DC transformer circuit, three other primary switch variations are in general use today. These forms are commonly called *half-bridge*, *full-bridge*, and *single-ended* DC transformers and are shown in Figs. 4.3A through 4.3C, respectively, less associated secondary networks. There are many other primary switch connections possible for DC transformation, but the four variations just discussed represent the majority of schemes normally encountered in practice. More complex variations will be discussed in Chapter 9.

In the half-bridge circuit of Fig. 4.3A, switches S1 and S2 conduct alternately, i.e., when S1 is ON, S2 is OFF, and vice versa. The voltage appearing across any open switch is equal to the source voltage, and the peak current through any conducting switch is twice the average source current. Because of the reduced switch OFF voltage stress, this half-bridge primary connection is usually preferred over the parallel connection of Fig. 4.2A in offline applications since in the latter case, any open switch must ideally sustain twice the source voltage. On the other hand, for low source voltage values, the parallel connection is usually chosen, since any conducting primary switch sees only I_s rather than $2I_s$ in the case of a half-bridge DC transformer.

Notice that, in the half-bridge primary connection, the voltage across the primary of the transformer is ideally one-half the value of V_s. Therefore, for a given N_p, V_s, and V_o, the primary winding must have half as many turns.

In the full-bridge circuit of Fig. 4.3B, switches S1 and S4 are closed simultaneously during the first half-cycle of the conversion process, and then S2 and S3 are closed simultaneously during the second half-cycle. The voltage appearing across any open switch is equal to the source voltage and the peak current through any conducting switches is equal to the average source current. Because the full-bridge DC converter provides minimum switch voltage as well as minimum current stress, this approach is popular in high-power (>750 W) converters.

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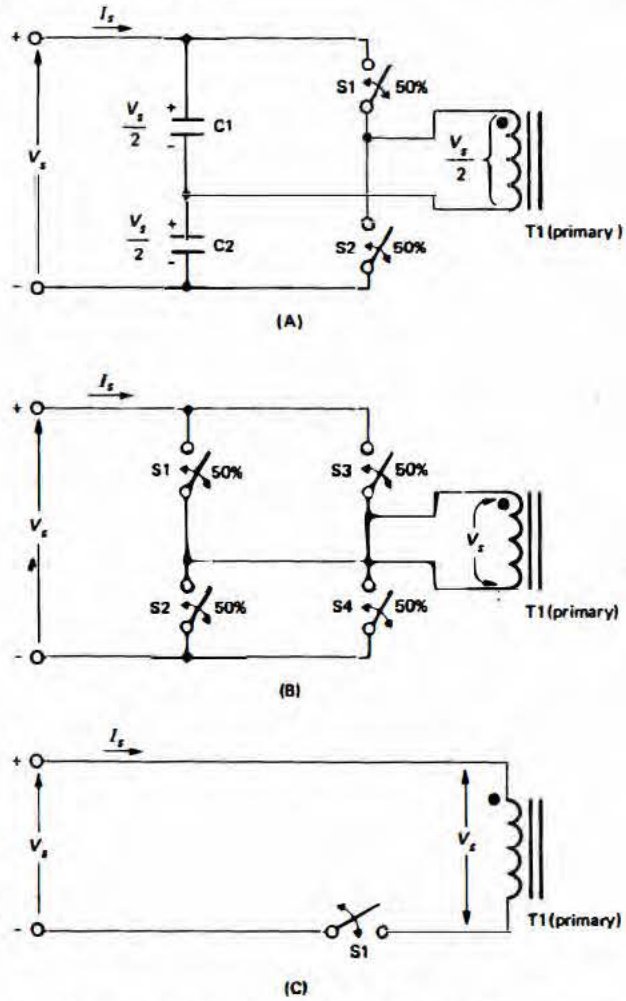


Fig. 4.3. Alternative primary switch connections for a DC transformer.

The single-ended approach to DC transformation (Fig. 4.3C) is simpler than all the others discussed, and is a very popular technique for low and medium output power applications. The circuit does, however, have some drawbacks. Its input current is pulsating, with an amplitude determined by the average value of I_s and the duty cycle of S1. Consequently, some form of input low-pass filter is usually needed to smooth out these current pulsations. When S1 is not con-

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ducting, its open-circuit voltage is equal to the source voltage plus the voltage reflected through the transformer from its secondary. In many cases, the switch open-circuit voltage will be greater than double the source voltage, while its closed-circuit peak current may well be more than twice the average input current. For these reasons, the single-ended DC transformer circuit is usually restricted to applications below 500 watts.

Finally, some means must be provided to reset the core of the transformer in this circuit when S1 is in an OFF state. This reset means is needed to prevent core saturation and subsequent high current in the switch when it is turned ON. Many transformer core reset schemes exist and may be divided into two general categories–those which allow the core energy to dissipate naturally, and those which force the reset of the core by external means. Which reset category is the best to use for a particular application is dependent on the core *B-H* loop characteristics, two extremes of which are shown in Fig. 4.4. The core material associated with the loop in Fig. 4.4A is characterized by a low remnant flux density (B_r) when its magnetizing force (H) is zero. When the magnetizing force is removed, this type of core can have a relatively large amount of energy stored. Here, an external means of core reset is desirable to quickly dissipate the large energy stored. The core characteristic of Fig. 4.4A is typical of some ferrite or powdered iron materials, or *any* core with an air gap. The characteristic shown in Fig. 4.4B is typical of cores composed of grain-oriented nickel-iron alloys, with no air gaps. Because of its "square-loop" *B-H* characteristic, this type of core material stores little energy and has a high B_r at zero excitation.

Comparing the two *B-H* characteristics, we see that each has advantages and disadvantages. With a low B_r core, the reset scheme can be very simple which is a significant advantage. The disadvantages of a low B_r core include the need for substantial core area and/or winding turns to keep the magnetizing current within reasonable bounds and the fact that less than half the available core flux can be used. A high B_r core, on the other hand, may require a more complex reset arrangement but, in exchange, will have a smaller core and/or less copper in the windings. As a general rule for the same power level, the forced reset high B_r core will provide the smallest complete transformer.

In practice, gapped low-B_r cores are most frequently used in single-ended DC transformer converters. The reason for this choice is not necessarily that this core characteristic is superior for this application, but rather due to a general lack of appreciation by designers of how simply forced-current reset can be implemented as well as the advantages of so doing.

A wide variety of reset schemes are possible, with simple clamp methods as shown in Fig. 4.5. In theory, the diode-zener clamp may be added to any winding of the transformer to provide core reset, provided that the associated volt-seconds/turns factor is sufficiently large that the core is indeed reset during the *minimum* time period that the switch is OFF. In practice, however, the clamp is usually placed on the primary winding (Fig. 4.5A), since any practical transformer

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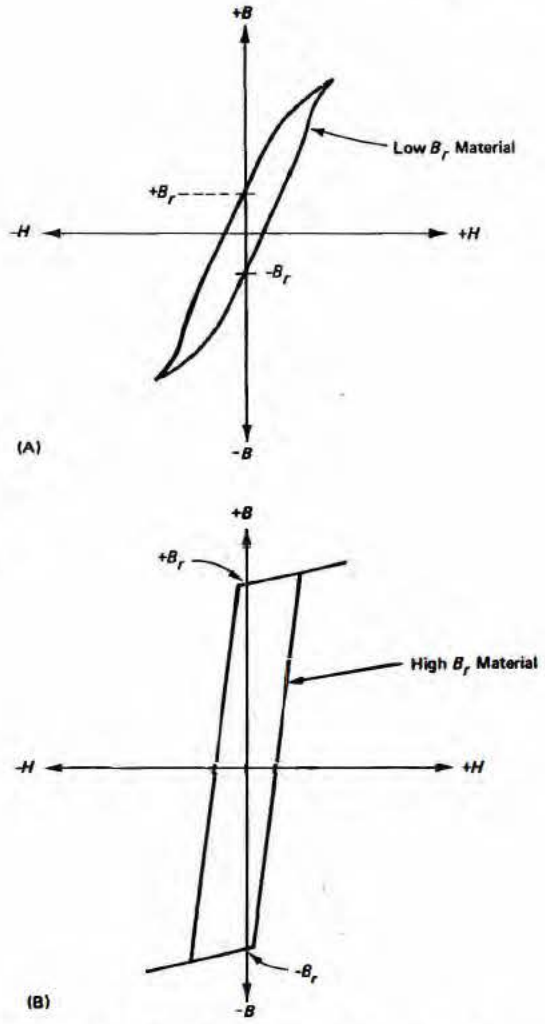


Fig. 4.4. Typical core *B-H* loop characteristics.

will have some primary-to-secondary leakage inductance. This parasitic inductance will also store energy and can damage the switch element if not dissipated safely. By placing the clamp circuit across the primary winding, both core reset and switch protection against parasitic transformer leakage inductance effects are accomplished simultaneously. Of course, in this type of core reset circuit,

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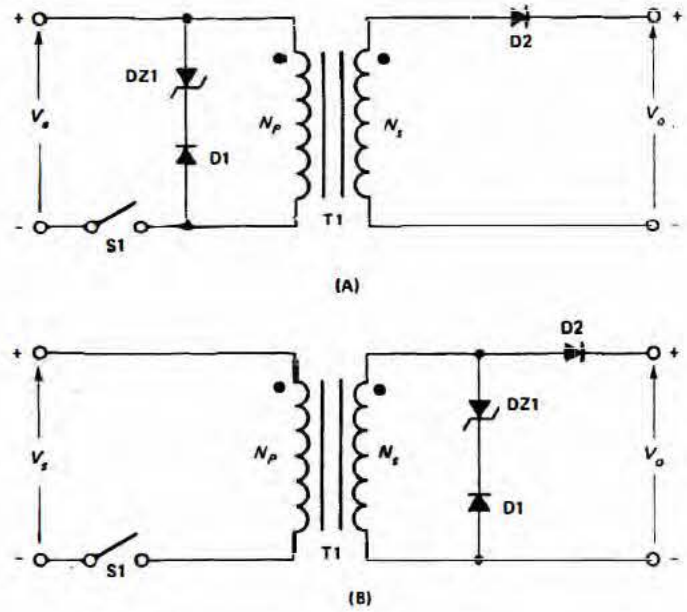


Fig. 4.5. Dissipative core reset schemes.

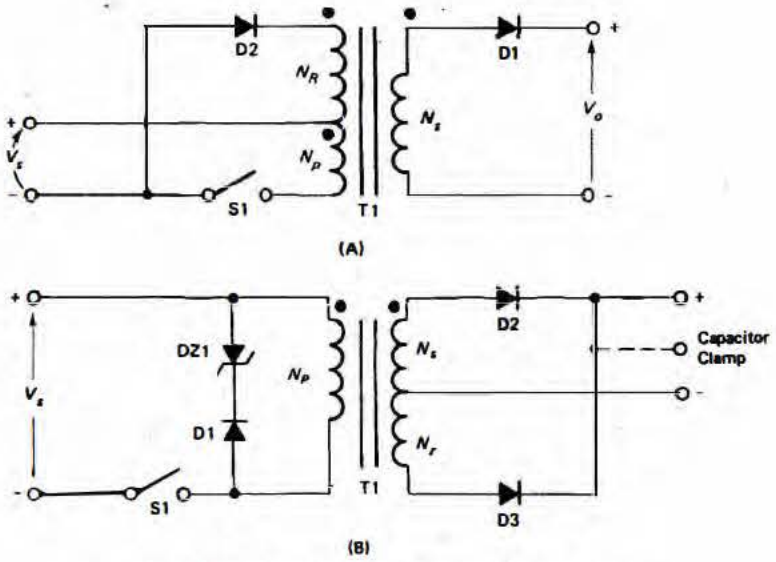


Fig. 4.6. Core reset schemes that recover the core energy.

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all of the stored core energy is lost within the clamp network. For this reason, this simple reset scheme is suitable for low-power applications.

For higher power applications, the stored energy of the transformer's core may be either returned to the source voltage (Fig. 4.6A) or to the load (Fig. 4.6B). In this manner, only a small portion of the stored core energy is lost, and the input-to-output power conversion efficiency is high. There is no requirement that N_R be equal to N_P or N_s. In fact, by making N_R small compared to N_P, the duty cycle of S1 can be increased with a reduction in the peak current it must handle. Unfortunately, as N_R is made smaller, the open-circuit voltage (V_a) across S1 will increase. The expression for V_a versus V_s is:

$$V_a = V_s \left[1 + \frac{N_P}{N_R}\right]. \tag{4.2}$$

In practice, the maximum switch duty cycle (D) of the single-ended transformer is usually limited to 0.7 or 0.8. For example, if the reset scheme of Fig. 4.6A is used with a maximum duty of 0.8, the number of turns on the primary must be more than *four* times the number of turns on the reset winding. From Eq. (4.2), the ideal switch voltage stress when it is in an OFF state will then be at least *five* times the source voltage.

In Fig. 4.6B, notice that a dissipative clamp circuit is shown on the primary of the transformer. This voltage clamp is needed to protect S1 from the harmful effects of parasitic primary leakage inductance and does not play a major role in the core reset operation. Power dissipation in this clamp circuit is normally quite small. When the core energy is discharged into the secondary as shown in Fig. 4.6B via diode D3 it will be necessary to connect D3 to a low-impedance load, such as the capacitor of any associated low-pass filter network. Connecting the energy commutation diode to a high-impedance load (such as an inductor) will cause a large voltage spike to appear on both primary and secondary windings of the transformer.

When a core of a single-ended DC transformer has a high value of B_r, mechanisms can be provided for reset. Two possibilities are shown in Fig. 4.7, the first of which uses an auxiliary winding and a current source and the second a permanent magnet. Ferrite cores having an integral permanent magnet are now available, but are rarely employed (primarily because of cost of customization) despite the simplicity of the reset scheme. The current reset scheme of Fig. 4.7A is not often used in practice because of the need for an additional transformer winding and an external current source. However, in many SPC circuits, there is a built-in current source–the filter inductor of any associated output low-pass network! In these instances, current reset may be realized by simply tapping the secondary of the transformer, as shown in Fig. 4.8, and routing the inductor current through the tap via a diode. This method costs little to implement–a tap on the transformer. In most circuits the diode will already be present.

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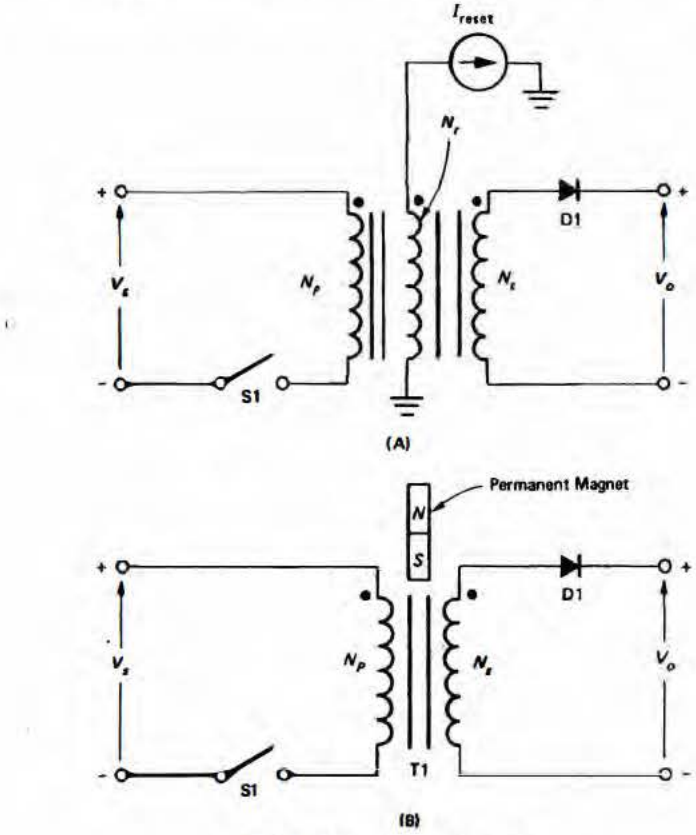


Fig. 4.7. Forced core reset schemes.

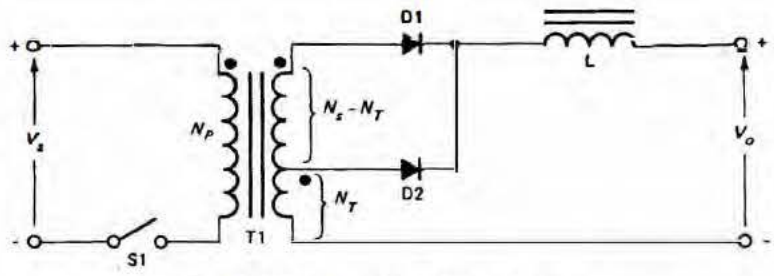


Fig. 4.8. Current reset using an output inductor.

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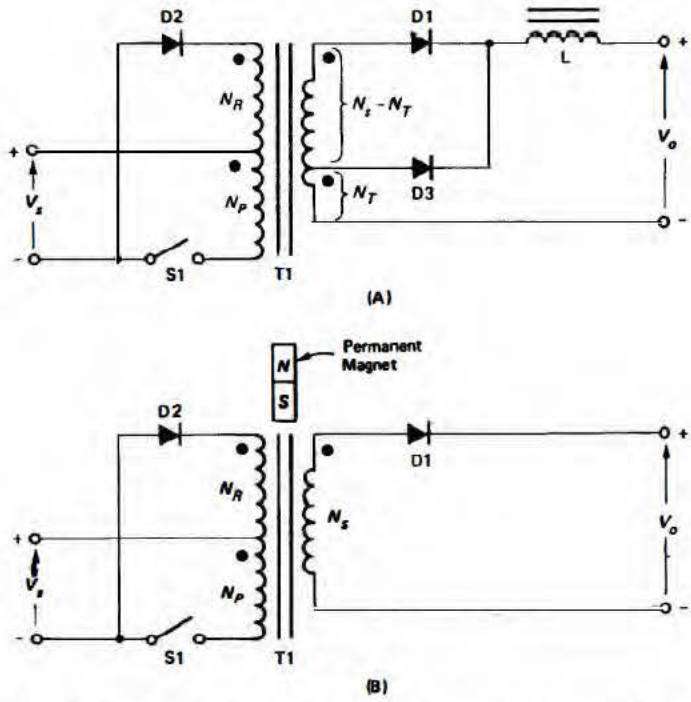


Fig. 4.9. Practical realizations for current and permanent magnet reset schemes.

The reset schemes of Figs. 4.7 and 4.8 lack one important feature, namely, a means for limiting the amplitude of the OFF voltage stress on S1 (V_a) during core reset. This feature can be easily added by the use of the primary clamping scheme of Fig. 4.6A. The resultant circuit structures are shown in Fig. 4.9.

In converter applications which have a high-voltage source, V_a can become substantial, as Eq. (4.2) predicts. A means to minimize V_a in these applications is shown in Fig. 4.10A. In this scheme, two primary switches are used and are driven ON and OFF simultaneously. Here, V_a for each switch will be equal to V_s, and the maximum duty cycle is 0.5, since the primary winding is also the reset winding. The duty cycle limit may be increased, again at the expense of increasing V_a, by tapping the primary winding as shown in Fig. 4.10B.

4.2 UNIDIRECTIONAL DC TRANSFORMERS

As we have just seen, there are a wide variety of circuits that can approximate the properties of an ideal DC transformer element. Here, we will look at SPC DC

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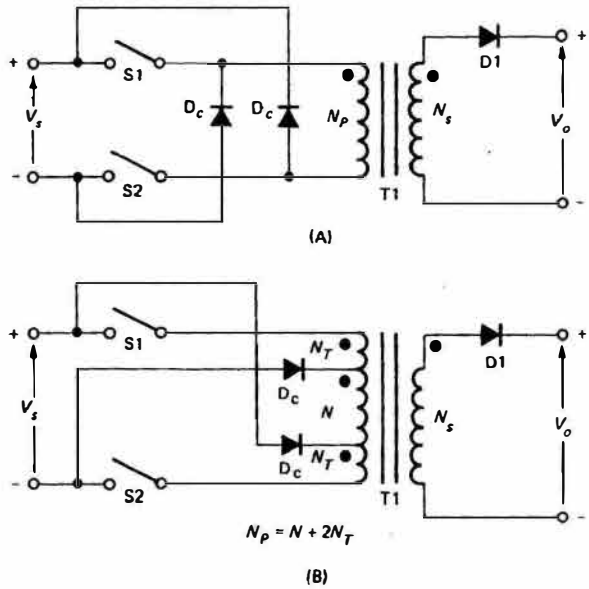


Fig. 4.10. Double-switch, single-ended reset schemes.

transformer circuits in which the input-to-output power flow is *unidirectional.* Then, in the next section, similar circuits in which *bidirectional* power flow is possible will be examined.

When comparing the DC transformer circuits to follow, one must take into consideration more than just topology concepts. As a practical matter, both the choice of switch arrangements and the means for driving them must be considered. There are several choices to be made in switch-drive arrangements alone, i.e., external drive or self-oscillating, voltage or current-drive, and many more.

One of the simplest (and oldest), unidirectional DC transformers is the *Royer* circuit shown in Fig. 4.11A. This is a self-oscillating BJT circuit, in which the transistors are driven from positive-feedback auxiliary windings on T1. For the circuit to be self-oscillating, it is necessary that the transformer core saturate at the end of each half cycle, removing the base drive from the switch in conduction. Residual energy in the transformer's core changes the polarity of the voltage across its transformer windings when a switch turns OFF, turning on the opposing switch. The alternate switch remains in conduction until the core saturates once again, and the process repeats. The primary advantage of the Royer circuit is its simplicity, but it does have a number of practical drawbacks which

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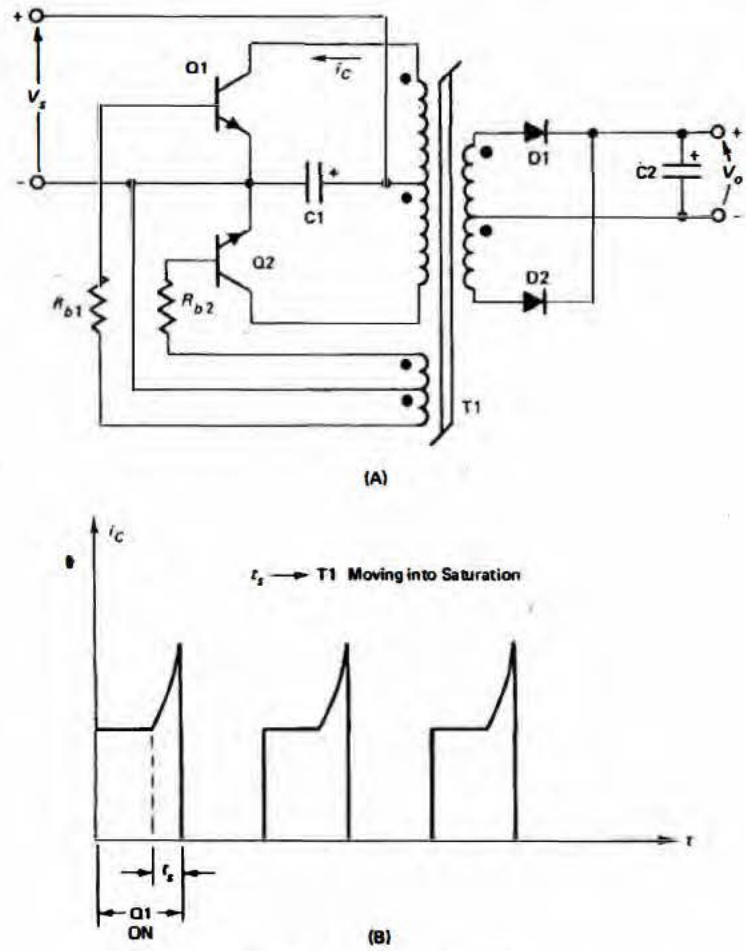


Fig. 4.11. The Royer circuit.

limits its use to low-power applications. One major problem occurs when the core goes into saturation reducing the primary impedance to a low value. This causes a large increase in i_C during the interval when the switch is turning OFF, as shown in Fig. 4.11B. This current transient causes high peak power to be dissipated in the transistor. For this reason, the Royer circuit is preferred for low-power DC transformer applications where such peak transient currents are small.

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The oscillation frequency of the Royer approach is more or less a linear function of the source voltage. It will also change as a function of temperature since the core flux saturation level, V_{CE} (sat) and the winding resistances of the transformer are all directly related to the environment. An additional problem is that the core flux excursion must go from $+\phi_s$ to $-\phi_s$, thus limiting the maximum self-oscillating frequency due to core power dissipation.

Another topology similar to the Royer circuit, which removes the switch drive functions from the main power transformer, is shown in Fig. 4.12A. This circuit is called the self-oscillating *Jensen* converter. In this approach, converter oscillation frequency and base-drive functions are performed by the saturable

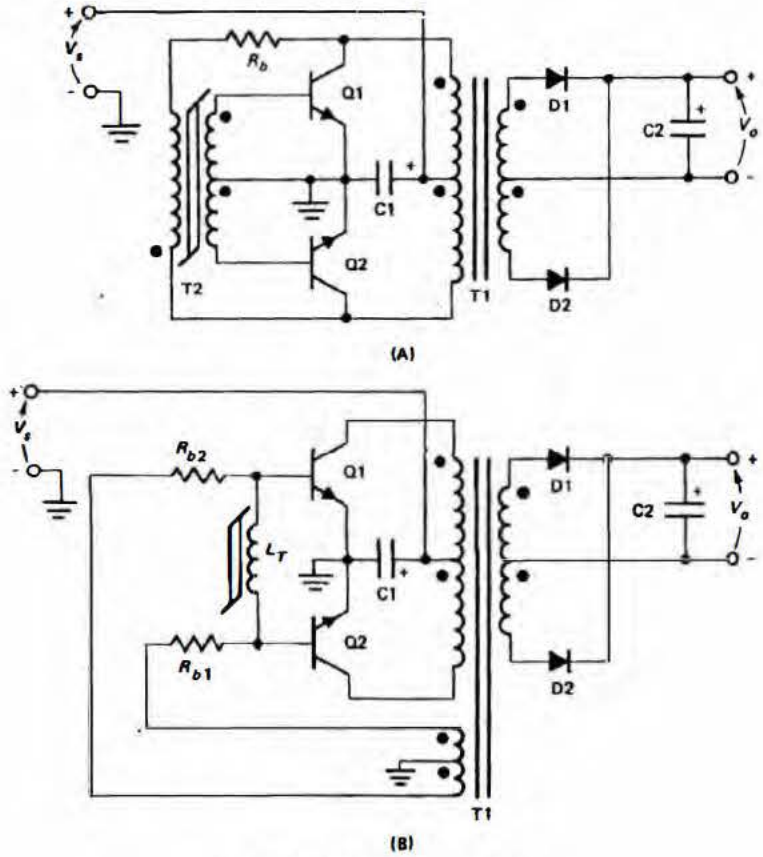


Fig. 4.12. The Jensen circuit.

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transformer element, T2. Therefore, Tl can be optimized for power tranfer alone. The oscillating frequency of the Jensen approach is determined by the core characteristics of T2 and the base-emitter voltage of the transistor switches. These voltages will vary with both converter load and ambient temperature, but normally not enough to have a large effect. The oscillation frequency of the Jensen converter is relatively stable with line, load, and temperature changes when compared to similar conditions in a Royer circuit. The primary switching current waveforms of the Jensen converter are also more uniform, with little or no current spiking due to core saturation. The price paid for this improvement is the need for an additional transformer. The Jensen circuit can be simplified as shown in Fig. 4.12B, where the timing function is accomplished by a single-winding saturating reactor (L_T), with the base drive power for the switches provided by an auxiliary winding on the power transformer, T1.

If the load and/or source voltage of the Jensen converter varies over a wide range of values, the transistor base drive approaches of Fig. 4.12 may be unsuitable, since they provide for drive magnitudes which are proportional to the source voltage. To provide sufficient base drive under worst-case input/output line and load conditions, (minimum V_s, with maximum load current), the base resistance (R_B) must be selected to provide enough current to maintain the switch in a fully saturated condition. Thus, when V_s is at its maximum and the converter load current is at a minimum, the switches are grossly overdriven. Long transistor storage times result. To maintain a base drive proportional to load demand, a current-drive network must be employed, as shown in Fig. 4.13A. In this circuit:

$$i_b = i_C \left[\frac{N_2}{N_1}\right] - I_{m2} \tag{4.3}$$

where I_{m2} is the magnetizing current in winding N2 of T2. By using a proportional base current drive such as this, the switches are always operating at a fixed β except when the converter has low output currents. Under light load conditions, i_C is small, and I_{m2} may become large enough to make the resultant i_b small. A low i_b value could result in inadequate base drive to maintain transistor saturation, and produce high power dissipation in these semiconductors. To overcome the light-load drive problem, an additional winding may be added to T2 to compensate for I_{m2}, as shown in Fig. 4.13B.

Besides providing excellent switching characteristics, the proportional base drive network of Fig. 4.13 is very efficient. For these two reasons, these forms of self-oscillating parallel DC transformers can work well at power levels up to several hundred watts. However, proportional current drive does have a disadvantage to keep in mind. If the output of a Royer converter is short-circuited, the circuit will cease oscillation and remain quiescent with both of its primary switches OFF. To a large degree, the Royer circuit is self-protecting in this

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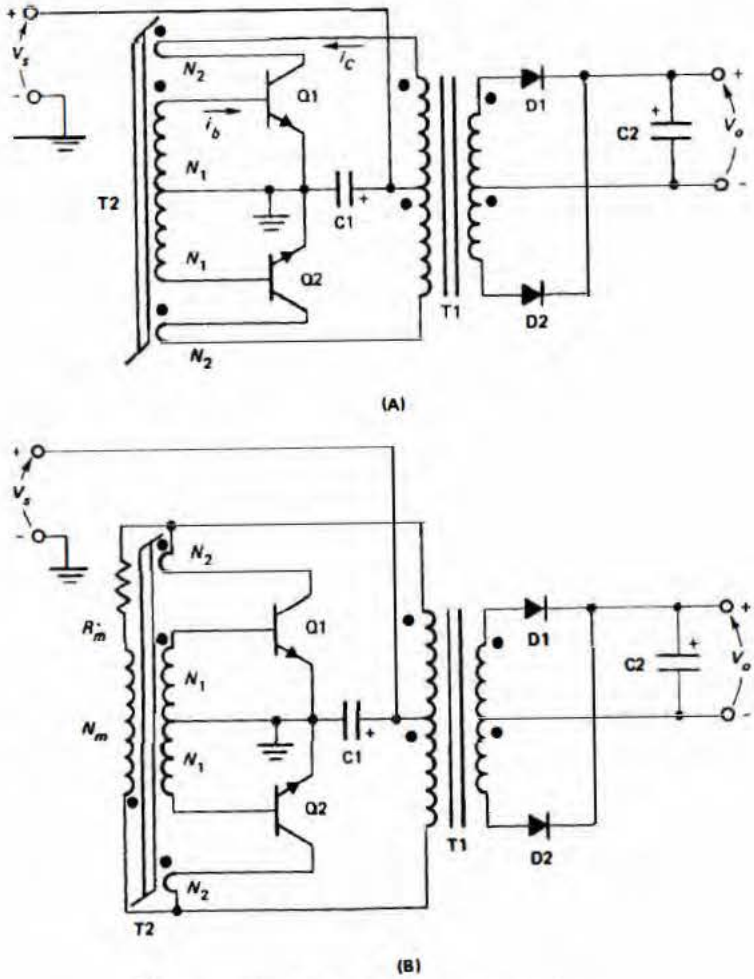


Fig. 4.13. A current-driven Jensen circuit.

regard. Similarly, the voltage-driven Jensen converters of Fig. 4.13 are also somewhat self-protecting in overload situations. This is not to imply that for all conceivable conditions of output current overload that the circuits of Figs. 4.11 and 4.12 will always be self-protecting by nature but, in general, the degree of self-protection is very good. However, in the current-driven circuits of Fig. 4.13, the feature of self-protection from output overloads is notably absent except,

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perhaps, for a complete short circuit condition on their outputs. As the output load increases in value, I_b increases proportionately in these schemes. Therefore, the proportionality feature of current drive will then cause the collector currents of the switches to reach peak stress levels, usually resulting in damage, unless the transistors are turned OFF by external protective means.

When efficient high power processing at a controlled frequency of conversion is desired, an externally driven DC transformer is usually used. For example, the circuit in Fig. 4.13A could be externally controlled by simply adding another center-tapped winding to T2 and connecting two drive switches as shown in Fig. 4.14. At the beginning of the switching cycle, S3 and S4 are both ON, disabling the transformer action of T2. This prevents S1 and S2 from turning ON. Driver switch S3 is then turned OFF and the residual energy stored in T2 (by I_D) is discharged into the base of primary switch S2 turning it ON. S2 conduction will then be maintained by the proportional base current supplied by the positive current feedback winding (N_2) of T2. At the end of this half cycle, S3 again turns ON, shorting the drive winding of T2, and disabling the proportional base drive mechanism for S2. One switching cycle is completed when similar actions are accomplished with S1 and S4. Although we are concerned here with 50% conduction cycles, the conduction periods of S1 and S2 could be pulse-width-modulated (PWM) if a low-pass LC filter is provided on the output of this converter for energy storage when switches S1 *and* S2 are both OFF.

Both full-bridge and half-bridge externally-driven DC transformer variations are frequently used in practice. An example of a half-bridge version is shown in Fig. 4.15. Here, only a single positive feedback winding on T2 is needed to accommodate proportional base drive for both S1 and S2.

DC transformer drive schemes abound in practice. Unfortunately, we cannot present them all in this text. The ones covered do represent the major schemes

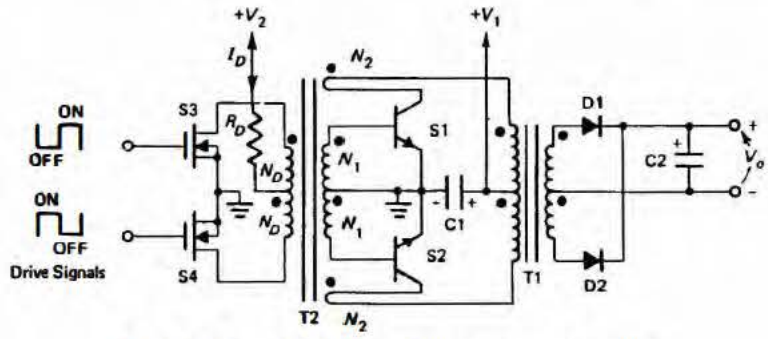


Fig. 4.14. A driven parallel circuit with proportional base drive.

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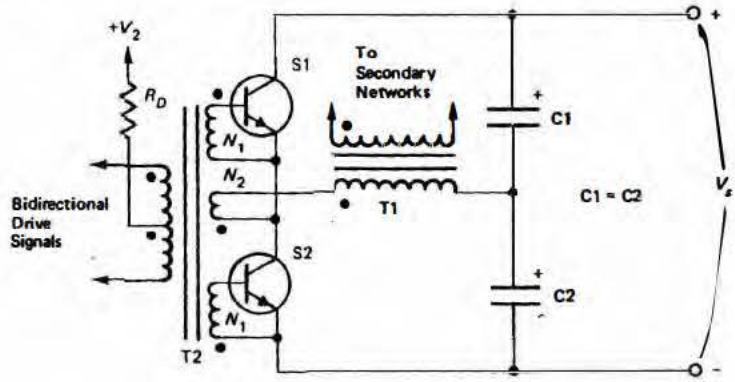


Fig. 4.15. A half-bridge version of Fig. 4.14.

found in today's conversion systems. Which scheme will be the best for a particular application is a function of conversion needs, size, and, of course, cost.

4.3. BIDIRECTIONAL POWER FLOW

For some power conversion applications, such as battery charging and discharging, it is desirable for the DC transformer to have bidirectional power flow capability. These features can readily be achieved by making appropriate converter switch elements bidirectional with corresponding drives for directional states. An example of adding this feature to the parallel transformer of Fig. 4.2 is shown in Fig. 4.16. Here, we have chosen MOSFETS as switch elements, as they possess diodes as an integral part of their structure. The direction of power flow will depend on the values of V_s, V_O, N_P, and N_s, as indicated by the following relationships:

$$V_s > \left[\frac{N_P}{N_s}\right] V_o \Rightarrow \text{power flow from input to output} \tag{4.4}$$

$$V_s < \left[\frac{N_P}{N_s}\right] V_o \Rightarrow \text{power flow from output to input.} \tag{4.5}$$

By making the switches bidirectional in handling currents, the discontinuous mode of operation is *not* possible. As the inductor current approaches zero during a switching cycle, it will continue on, becoming *negative* rather than remaining at a zero value. This means that at $t = T_s$, $I_a \neq 0$ but may have some negative value. Therefore, the continuous mode of SPC operation and small-

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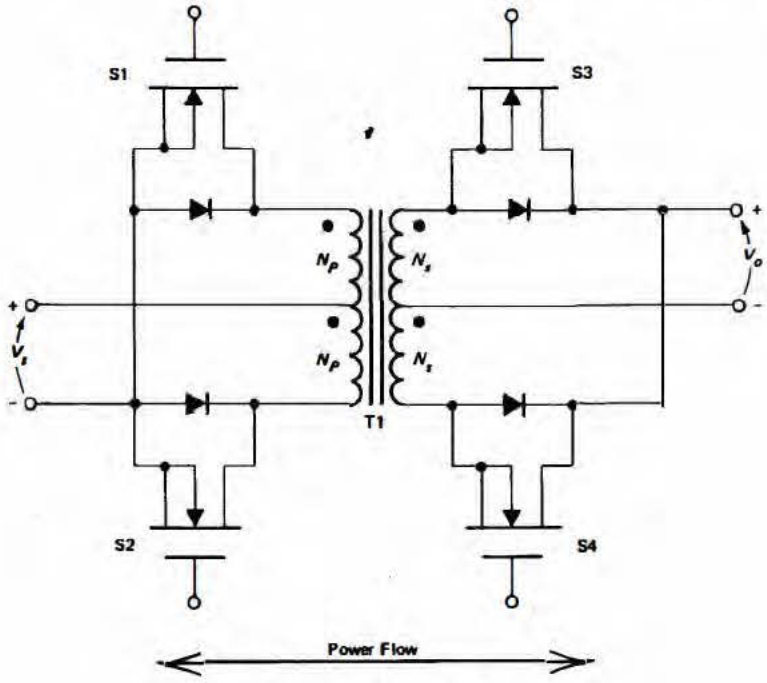


Fig. 4.16. A bidirectional parallel DC transformer.

signal modeling associated with it discussed in Chapters 1 and 2 will *always* prevail in a converter with bidirectional power flow capability.

4.4 PROBLEMS AND LIMITATIONS OF PRACTICAL DC TRANSFORMERS

Obviously, practical DC transformers can not exhibit ideal electrical characteristics and, as such, have performance limitations and operational problems. Fortunately, most of the circuit problems can be overcome and the functional limitations minimized.

The most fundamental performance limit is bandwidth of signal processing. For practical purposes, the bandwidth can be assumed to be less than one-half of the maximum switching frequency of the converter. It follows that, to achieve wide bandwidth of power processing, high switching frequencies must be used. At the present time, conversion switching frequencies up to 500 kilohertz are not uncommon and, by using MOSFET switch elements, frequencies of several

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megahertz are possible. For most applications, converter bandwidth is not a problem if associated active and passive circuit elements are properly chosen or designed.

Any practical switch element requires some finite period of time to change state. In the BJT, the delay in turnoff is primarily due to minority carrier storage time. One example of the effect of BJT storage time is conduction time overlap in the switches of a DC transformer. The result of finite switching times and conduction overlap in a parallel DC transformer (Fig. 4.17B) is shown in Fig. 4.17A, where its output secondary waveform appears much like that shown somewhat exaggerated in Fig. 4.17A. Two design approaches can be followed to reduce the effects of these "breaks" in output voltage. First, reduce the con-

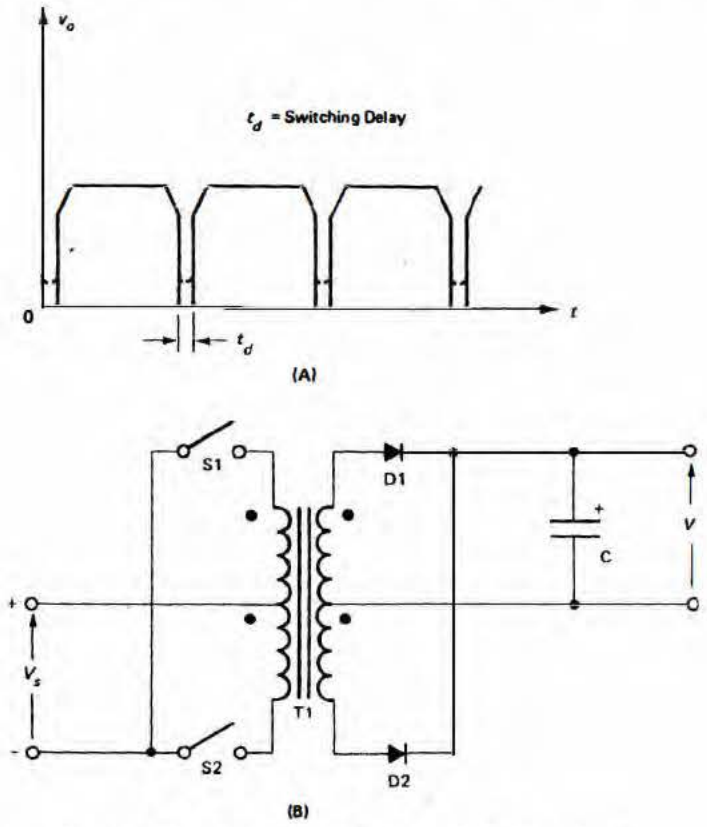


Fig. 4.17. Typical output waveform in a practical DC transformer.

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duction overlap to acceptable intervals and, second, add a small capacitor (Fig. 4.17B) across the output terminals of the circuit to smooth out the waveform pulsations.

Conduction overlap of primary switches also causes another problem discussed earlier, namely, high current spikes during such intervals. If the transformer is supplied from a "stiff" voltage source and both switches are ON simultaneously, there is very little impedance to limit the switch current amplitudes and they could very well be damaged or destroyed as a result. If converter drives are externally provided, their signal intervals may be shortened to provide a *dead time* when neither primary converter switch is being actively driven. The amount of dead time required will be determined by maximum storage time of the primary switches. Because the storage time of a BJT is a function of base drive magnitude, collector current level, junction temperature and normal variations in the manufacturing processes of the semiconductor, the required dead time intervals are difficult to predict and, to satisfy the worst case, may have to be a significant portion of the switching cycle of the converter. Any output filter capacitor for energy storage (Fig. 4.17A) also will end up being fairly large.

In a self-oscillating DC transformer circuit, automatically inserting an adequate dead time interval to prevent conduction overlap of primary switches is often unrealistic. Usually, some form of in-line primary current-limiting is added instead to reduce the amplitudes of any potentially destructive current spikes to safe levels. A simple means for limiting instantaneous primary current is the insertion of an inductor in series with the source voltage as shown in Fig. 4.18. In Fig. 4.18A, the energy stored in L following any overlap interval of S1 and S2 is dissipated in resistor R_o and diode D_C. In Fig. 4.18B, the stored energy in L is returned to the source via diode D_C.

Large current spikes in the primary switches can also occur should the transformer core saturate when either one is conducting. In an ideal converter, the volt-seconds applied to both the primary and the secondary windings will average to zero over one switching cycle and the corresponding flux excursions of the transformer core will be symmetrical about the origin of its hysteresis loop. Therefore, no core saturation problems will occur as long as maximum flux capability of the core is not exceeded. In practical terms, however, perfect volt-second balance is never achieved for a number of reasons. First of all, the conduction interval of the primary switches may not be exactly identical and their conduction voltage drops may not be equal. Also, conduction voltage drops as well as conduction time intervals of rectifier diodes on the secondary side of the transformer may not be equal because of parasitic inductances. This problem will be addressed in more detail in Chapter 8.

There are many ways to minimize or eliminate transformer core saturation from unbalance and its resultant undesirable side effects. Some techniques are simple in concept while others can be very complex to implement. The simplest

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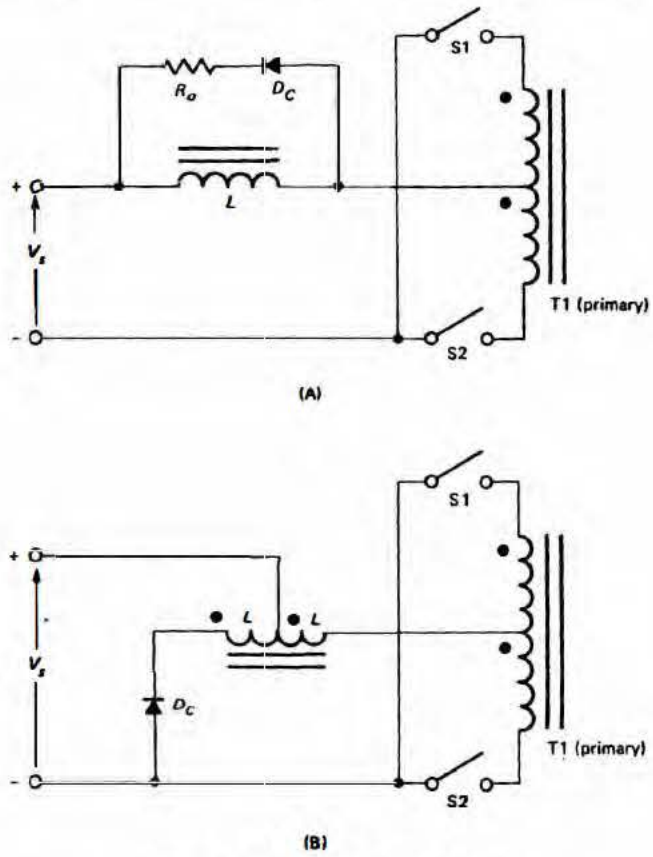


Fig. 4.18. Primary current-limiting circuits.

method is the selection of a core material for the transformer that has relatively low permeability and low residual flux density (such as is shown in Fig. 4.4A) which will tolerate some DC offset without saturation. This solution brings with it relatively high magnetizing current levels for small core area dimensions or low numbers of turns on windings. Increasing core area and winding turns to reduce magnetizing current levels increases the size and cost of the transformer. A better alternative would be the use of a core with a characteristic like that shown in Fig. 4.19A. In this type of core characteristic, the effective permeability is very high in the normal operating region (about the origin of the *B-H* loop). If some DC imbalance is present and the operating loop moves off to one side of the core

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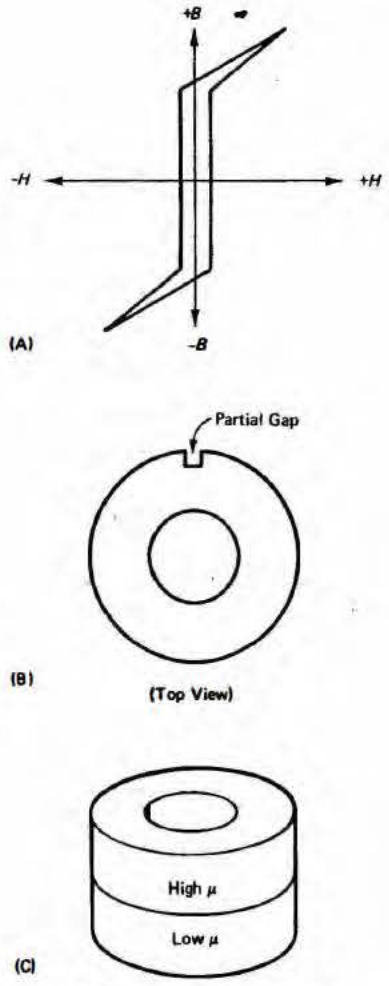


Fig. 4.19. Composite core structures.

characteristic, the core does not go into hard saturation, but moves into the upper region of the characteristic, where the permeability is lower. Thus, sufficient inductance will exist to limit peak switch currents to safe levels. While there is no known single core material with the desirable characteristic of Fig. 4.19A, modified or composite core structures can be built which can emulate it. Two examples, using toroidal structures, are illustrated in Figs. 4.19B and C. In

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Fig. 4.19B, a partial air gap is placed on the outer part of the core so that nearly all of the core flux is contained in its inner ungapped section during normal operation. If the inner section should saturate, the core flux will move to the outer air-gapped portion which has a lower but still significant permeability. A stacked two-core composite configuration is shown in Fig. 4.19C, where two cores with the same inner and outer diameters but composed of different permeability materials are used. The methods of primary current-limiting (shown in Fig. 4.18) for overlapping conduction will also provide switch protection for core saturation.

For those DC transformation circuits which use a bridge or half-bridge primary switch connection, a particularly simple means is available for eliminating transformer core saturation due to primary volt-second imbalance. In these two converter circuits, the primary winding of their transformers can be DC-isolated by the insertion of a series capacitor (C_s) as shown in Fig. 4.20. Notice that for the half-bridge version (Fig. 4.20B), the series DC-blocking capacitor function is accomplished inherently by the presence of the voltage-division capacitors, C1 and C2. The value chosen for C_s cannot be arbitrary, for as C_s is made smaller, the output voltage waveform (Fig. 4.20C) will become more tilted because of the AC voltage drop across this series capacitor. On the other hand, if C_s is made too large and the source voltage is subject to rapid changes, the DC voltage across C_s may not change quickly enough to prevent momentary transformer core saturation. The time constant (τ_C) for the rate of change of DC voltage across C_s is approximately:

$$\tau_C \cong R_r C_s \tag{4.6}$$

where R_r is the reflected output load resistance of the converter seen by the primary of the transformer.

If possible, the value of τ_C should be made small in comparison to the maximum slew rate of expected changes in V_s.

A variety of active circuits are possible that will electronically sense the condition of impending core saturation and turn off primary switch networks. The price paid for any electronic approach is additional SPC complexity as well as cost.

The possibility of transformer core saturation can be reduced if converter switches are closely matched in thermal as well as electrical characteristics. Matching can greatly improve the protective effectiveness of the passive methods discussed earlier. For MOSFET switches, matching is not difficult or unreasonable from a cost standpoint. However, matching BJTs requires that several parameters (V_{CE} (sat), V_{BE}, t_s, etc.) be controlled over the ranges of junction temperatures and load currents encountered in an application. BJT matching is

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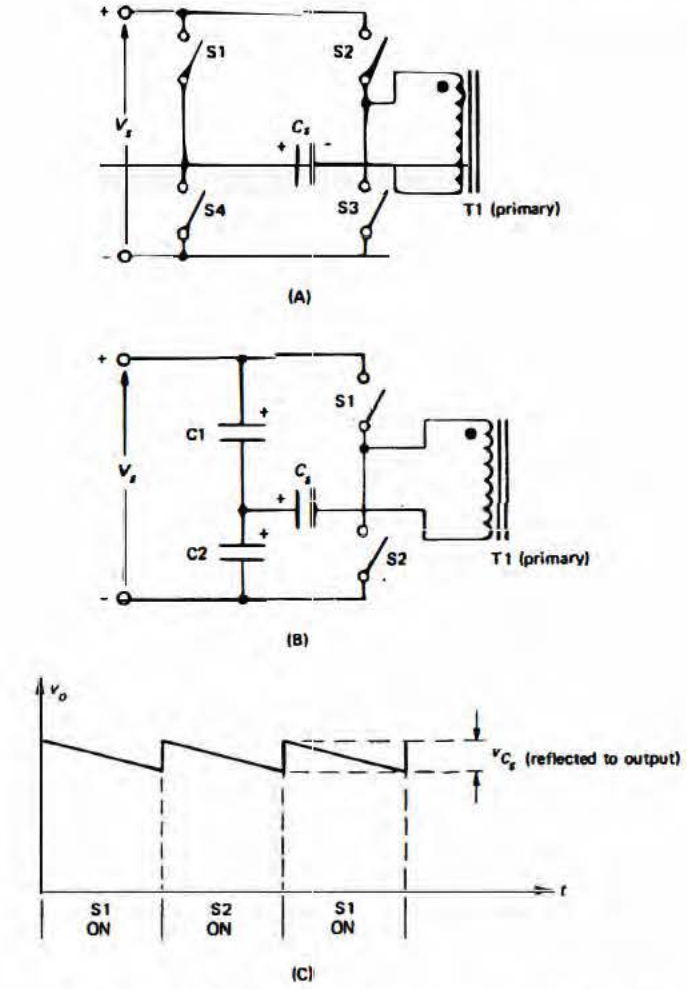


Fig. 4.20. A DC-blocking capacitor in series with the primary winding.

rarely economically practical, although pair matching for some parameters will always be to the designer's advantage.

When a DC transformer circuit is shut down by rapidly removing its source of power or its drive, the transformer core may not have zero residual flux but instead be left with a large value of residual flux. When the converter is reactivated,

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the core material of the transformer may saturate on the first half-cycle of operation, resulting in a potentially destructive current spike in one of the primary switches. Since there is no means in most SPC circuits to determine the actual initial value of the core flux at converter turn-on, this particular problem has destroyed more than a few converters. Both inductive primary current-limiting methods or active core state flux-sensing schemes are effective approaches in solving this turn-on core saturation dilemma.

The self-oscillating transformer circuits shown in Figs. 4.11 through 4.13 work very well, once oscillation has begun. However, all of these circuits suffer from a lack of reliable "starting." Since both primary switches are initially OFF, there is no inherent mechanism (other than leakage paths) to start oscillation at power application. Therefore, it is necessary to include auxiliary starting electronics which momentarily place one (or more) of the DC transformer switches in an active conduction mode. A commonly used starting circuit for the Royer system of Fig. 4.11 is shown in Fig. 4.21. Many other starting networks exist. Interested readers are referred to text reference 5 in the bibliography of this book.

In the parallel circuit of Fig. 4.2, if the two primary windings of the transformer are not tightly coupled, it is possible to generate switch voltage spikes from leakage inductances. The effect is equivalent to placing a small discrete

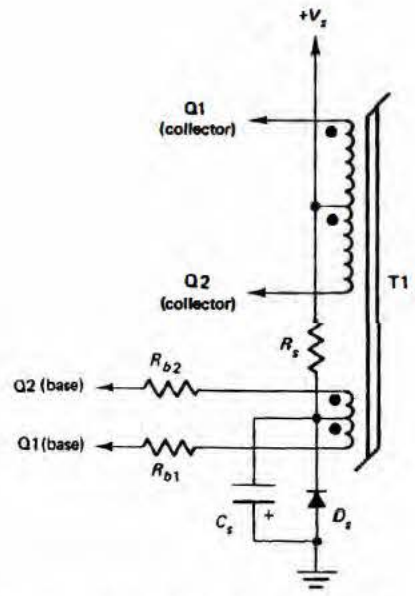


Fig. 4.21. A typical starting circuit for self-oscillating converters.

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inductor (L_ℓ in Fig. 4.22) in series with each primary switch. When a switch is turned OFF, the energy in the associated parasitic leakage inductance must be dissipated. For this reason the voltage across the OFF switch will continue to rise until this energy is eliminated, usually as a result of switch breakdown. If the transformer leakage inductances are made very small, then any parasitic capacitance in parallel with the OFF switch will limit the resultant transient voltage amplitude, often protecting the switch from voltage breakdown and producing a damped ringing waveform which can contribute to the electromagnetic (EMI) noise generated by the converter. Winding the primary windings of the transformer either bifilar or interleaved is a common design method used to maximize coupling between the windings. Adding a transient-damping network (R_s, C_s) across the primary winding, as illustrated in Fig. 4.22, is also recommended.

When the output load of a practical DC transformer is made very light, voltage

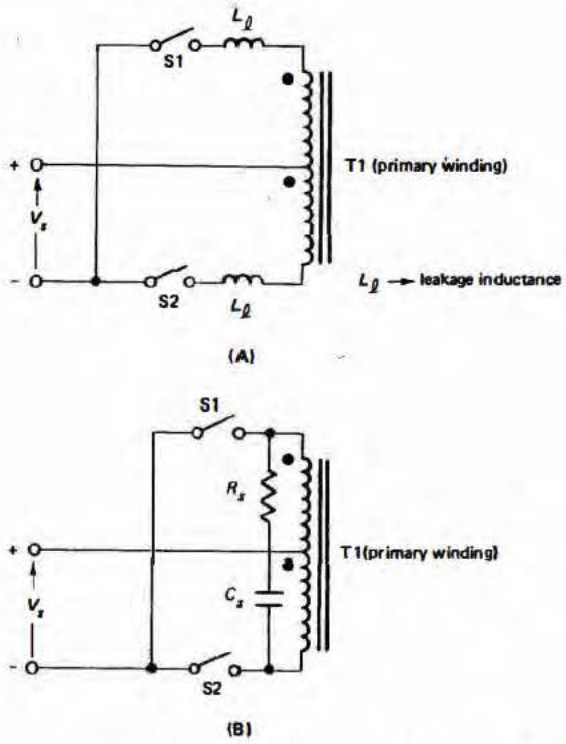


Fig. 4.22. Primary-to-primary leakage inductance with a damping network.

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transients resulting from winding and circuit layout parasitic inductances can appear as a dynamic part of the output voltage, altering its average voltage value, independent of the value of V_s. This transient-produced output problem is best resolved by careful design of the transformer, good physical layout of converter power electronics and appropriate damping networks across parasitic inductive elements.

The magnetizing inductance of a practical transformer of a converter must be finite, and therefore contributes to the primary current waveform. A general representation of the AC waveform of the magnetizing current waveshape is shown in Fig. 4.23A. Since i_m is an inductive current, it does not represent an inherent conversion power loss. However, from earlier discussions, it can increase the converter switching losses and the resistive losses in the winding of the transformer. At full load, I_m is normally small in amplitude when compared to I_s (as shown in Fig. 4.23B), so that their composite waveform is always positive. However, at light output loads, I_m may exceed I_s and cause the composite current waveform to reverse polarity. A typical solution to this light-load problem is to make the primary switches bidirectional. For BJT switches, anti-parallel diodes can be added as shown in Fig. 4.24. During light loading when the diodes are conducting, the effective duty cycle of the switches may be different from that applied to the switch element alone. If the switch is PWM controlled, then the voltage transfer function will be altered.

In a practical single-output circuit, each half section of the transformer secondary winding is not perfectly coupled to either the primary winding or to its other half section. In addition, physical connections to output rectifiers will always have some series inductance associated with them. These parasitics can affect the output voltage regulation and ripple of the converter. The equivalent circuit of an SPC output secondary winding with rectifier connections can be drawn with these parasitics, with leakage inductances drawn as lumped inductors in series with each rectifier. The resultant circuitry is shown in Fig. 4.25A. Note that there are two types of inductances illustrated–that which is common to both halves of the secondary winding and that which is due to imperfect transformer coupling between these secondary windings plus their rectifier connection inductance (L_a and L_b). For the purposes of this discussion, the presence of the common inductances will be ignored and the equivalent circuit of Fig. 4.25B used. These parasitic inductances do affect converter circuit operation, becoming more significant as either the switching frequency or the output current level is increased.

The voltage and current waveforms within the equivalent circuit of Fig. 4.25B are given in Fig. 4.26, for the case of 50% duty cycle on each secondary. During time t_1, a current i_1 is flowing through D1 and L_a. At $t = t_1$, the polarity of v_1 and v_2 relative to the centertap of the transformer secondary changes, but, because of the presence of inductors L_a and L_b, i_1 will fall gradually and i_2 will increase gradually. The average value relationship,

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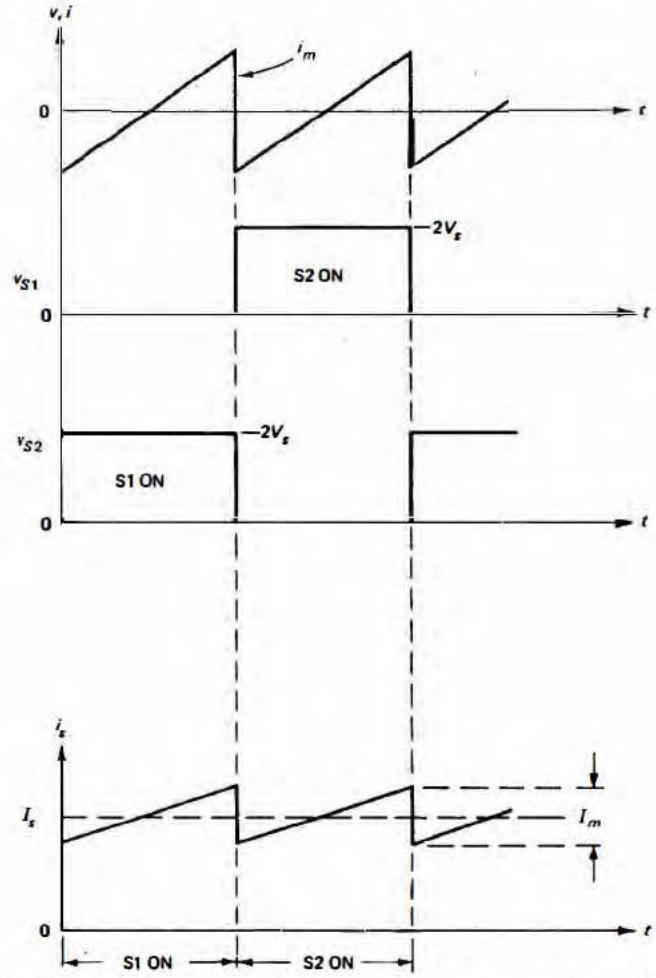
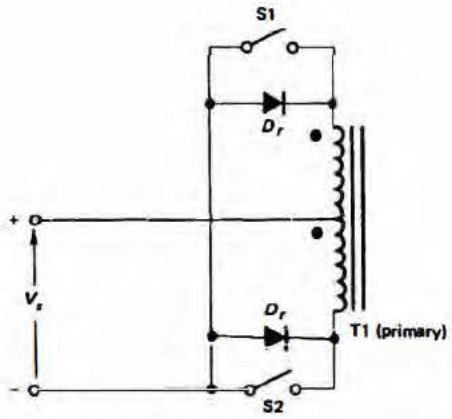


Fig. 4.23. Primary voltage and current waveforms showing the effect of the magnetizing current.

$$I_1 + I_2 = I_3 \tag{4.7}$$

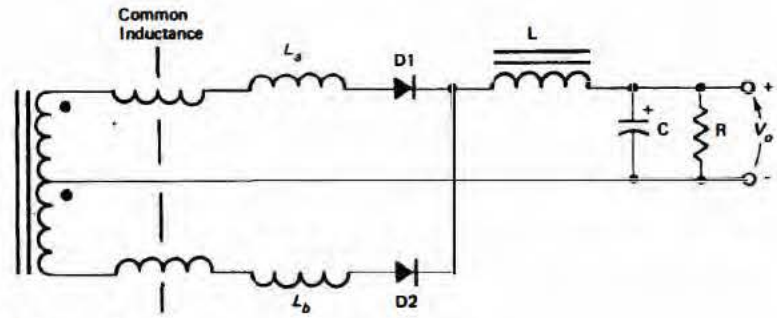
must be preserved throughout the converter's operating cycle. During the interval Δt, when both i_1 and i_2 are flowing, D1 and D2 must be in conduction simultaneously, so that $v_3 = 0$. This "notch" in v_3 reduces the average output

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S1, S2 → undirectional switch elements

Fig. 4.24. Primary free-wheeling diodes.



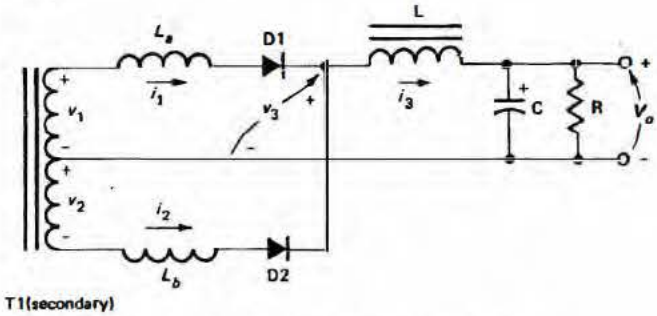


Fig. 4.25. Secondary equivalent circuits.

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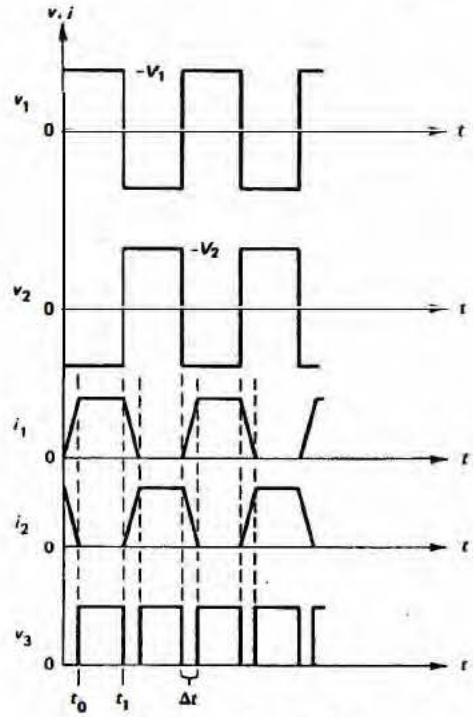


Fig. 4.26. Secondary waveforms.

voltage of the converter and increases associated AC ripple magnitudes, both of which are undesirable.

The overlap time interval (Δt) is:

$$\Delta t = \frac{L_a i_1}{V_1}. \tag{4.8}$$

It is obvious from Eq. (4.8) that low-voltage high-current transformer secondary windings are most likely to produce a significant value of Δt. The "delay" interval will also vary with the converter's load current. This time interval can be related to a change of conversion duty cycle, ΔD, and ripple frequency ($f_r = 2f_s = 2/T_s$) by:

$$\frac{\Delta t}{T_s} = \Delta D = \frac{L_a i_1 f_r}{2V_1}. \tag{4.9}$$

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For conversion duty cycles less than 50%, the "notch" effect is still evident, even though v_1 goes to zero prior to change in secondary voltage polarity. Therefore, i_1 must continue to flow to satisfy the requirements of Eq. (4.7). In practical circuits, i_2 may not remain zero during the Δt time interval and i_1 is thus reduced. This situation can reduce ΔD to some degree, but the basic result is still evident. Voltage v_3 will be zero during Δt only if $L_a = L_b$. Usually, this latter condition is not satisfied. Therefore, voltage v_3 usually has some positive value during Δt. The net result of all of the above actions is a reduction in effective duty cycle of the v_3 waveform when compared to that of the transformer secondary voltages. The change is dependent on load current.

In a DC-DC converter with multiple secondary outputs, transformer cross-regulation between secondaries is degraded by this effect as well as by parasitic resistances of rectifier diodes, winding resistance voltage drops, and other leakage inductance effects. For good transformer winding cross-regulation, it is imperative that parasitic series inductances be minimized.

So far we have been dealing with symmetric output converter circuits with equal parasitic inductances, i.e., $L_a = L_b$. Now consider a single-ended DC transformer output circuit, such as that shown in Fig. 4.27A. Here, L_a will most likely be different in value than that of L_b. The resulting waveform shape of v_3 will be very similar to that shown in Fig. 4.27B. The corresponding equation for Δt_1 and Δt_2 are:

$$\Delta t_1 = (L_a + L_b)\frac{i_1}{V_1} \tag{4.10}$$

$$\Delta t_2 = (L_a + L_b)\frac{i_1}{V_1'} \tag{4.11}$$

and, because v_1 is usually asymmetrical, $\Delta t_1 \neq \Delta t_2$. The equations for v_3 during Δt_1 and Δt_2 are, respectively:

$$v_3 = \frac{L_b i_3}{\Delta t_1} \tag{4.12}$$

$$v_3 = \frac{L_b i_3}{\Delta t_2} . \tag{4.13}$$

4.5 SOURCE IMPEDANCE EFFECTS

So far in the discussions of this chapter, we have tacitly assumed that a voltage source was being used at the input to the DC transformer, as shown in Fig. 4.28A. This is referred to as a *voltage-fed* transformer. Often the power source

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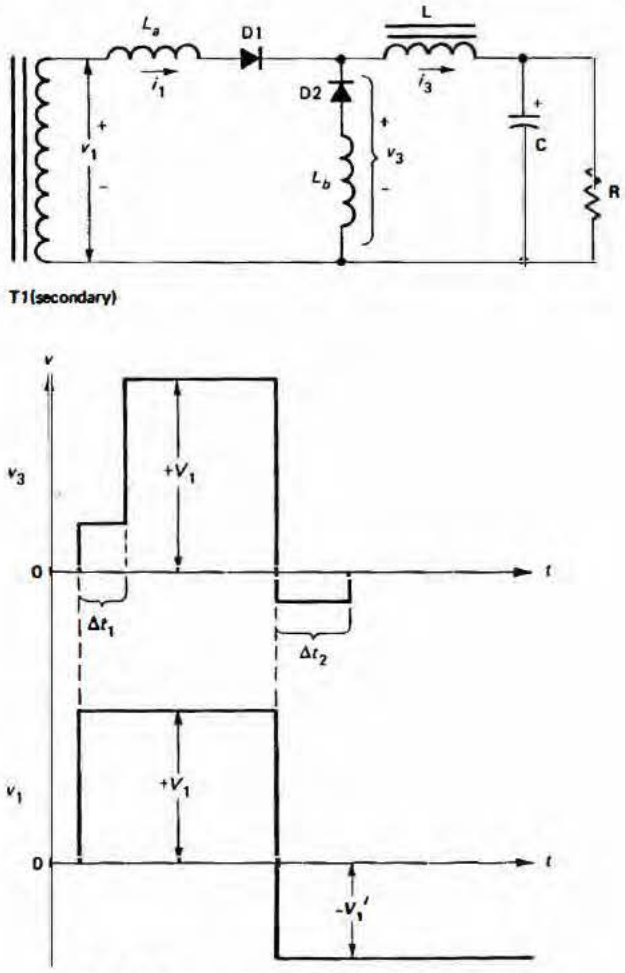


Fig. 4.27. Asymmetrical converter secondary waveforms.

is high in impedance value, and as such could be characterized as a current source, as shown in Fig. 4.28B. One practical and common form of a "current" power source is shown in Fig. 4.28C. In this instance, the transformer system is said to be *current-fed*.

In the case of voltage-fed DC converters, voltages appearing across the transformer windings are determined by source voltage and the winding currents by

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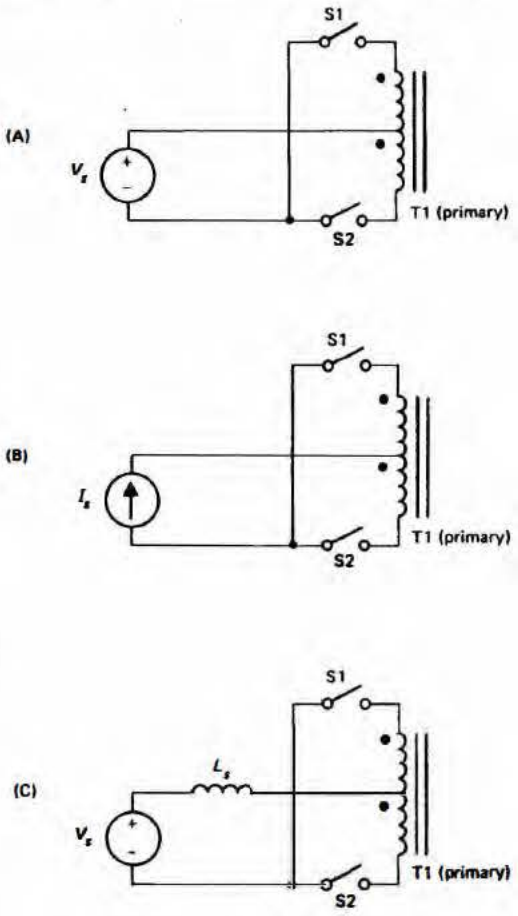


Fig. 4.28. Voltage- and current-fed transformers.

the converter load. In the case of current-fed converters, transformer currents are determined by the impedance of the source and winding voltages by the load of the converter. Obviously, a dual source relationship exists between these types of converter feed.

Taking into account the parasitic effects, such as switch conduction overlap and others discussed earlier in this chapter, a current-fed converter has many desirable features, since it automatically limits primary currents. Also, the current-

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fed converter is less prone to output capacitor charging under light output load conditions. On the other hand, the current-fed converter does have its disadvantages. For example, any practical transformer will have some leakage inductance between primary and secondary windings which, can produce large voltage spikes across converter switches when they are turning OFF. Again, good magnetics design and liberal use of appropriate transient damping networks are the best defenses. Also, when a self-oscillating converter is operated from a current-limited source, a starting problem can exist because of starting-voltage dependdency on output load magnitude.

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5. Buck-Derived Circuits

In Chapter 1, we asserted that complex SPC circuits could be reduced to equivalent forms of one or more combinations of the buck, boost, and the DC transformer element. Because of that assumption, Chapters 2, 3, and 4 were devoted to detailed examinations of the characteristics of these three basic converters. Now the time has come to test our original premise and to see if this evolutionary point-of-view is valid and useful in practical SPC design.

In this chapter, we begin by examining the family of SPC circuits which can be derived from the basic buck converter by the insertion of different DC transformers into its topology at various points. In the pursuit of these combinational investigations, opportunities to reduce the switch count will arise, whereby other SPC circuit changes will become apparent that, in turn, will reveal further offspring of the buck SPC family.

The first combinations we will examine are those which use the parallel DC transformer of Fig. 4.2A, followed by similar circuit variations using bridge, half-bridge, and single-ended DC transformers. We will digress a bit in the related discussion on the single-ended transformer variation to point out the consequences of using the different transformer core reset schemes of Chapter 4 on SPC circuit performance.

5.1 BUCK SPC AND PARALLEL TRANSFORMER COMBINATIONS

Figure 5.1 shows the two basic circuits under consideration—the buck converter (A) and the parallel DC transformer (B). In Fig. 5.1A, we have indicated five circuit locations (A-A′ through E-E′) where insertion of a DC transformer is feasible so as to be in series with the flow of input-to-output power. Other insertion areas within the buck SPC topology for DC transformers are conceivable but, in general, yield converter systems that are not functional, as the DC transformer would not be in series with the power flow path.

If we insert the DC transformer at location A-A′, the converter shown in Fig. 5.2A is obtained. Here the buck converter usually serves as a regulated voltage source for the DC transformer. This system is usually referred to by

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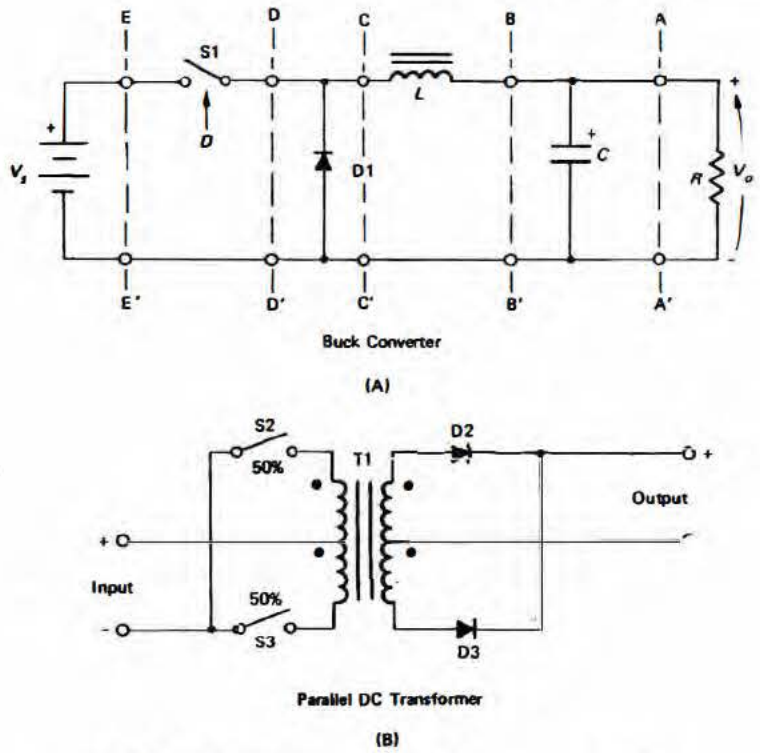


Fig. 5.1. The basic constituents of buck-derived converter circuits.

SPC designers as a *DC-DC converter with a pre-regulator* and can be altered to include multiple-output capability, as shown in Fig. 5.2B. Control of the conduction duty cycle of S1 is usually maintained by auxiliary voltage control electronics associated with either the output of the pre-regulator (the buck converter portion) or one of the outputs of the DC transformer. Keep in mind that the DC transformer is voltage-fed, and one may experience the unbalance and conduction overlap problems discussed in Chapter 4.

Even though the circuit of Fig. 5.2 uses a buck converter as a pre-regulator, the addition of the DC transformer allows the output voltage(s) to assume a value(s) higher or lower than the source voltage (V_s). DC isolation between input and output is now possible and, as shown in Fig. 5.2B, a number of different output voltages can be provided simultaneously. The output voltages are related to the output voltage of the pre-regulator buck SPC by the corresponding turns ratio of the transformer windings.

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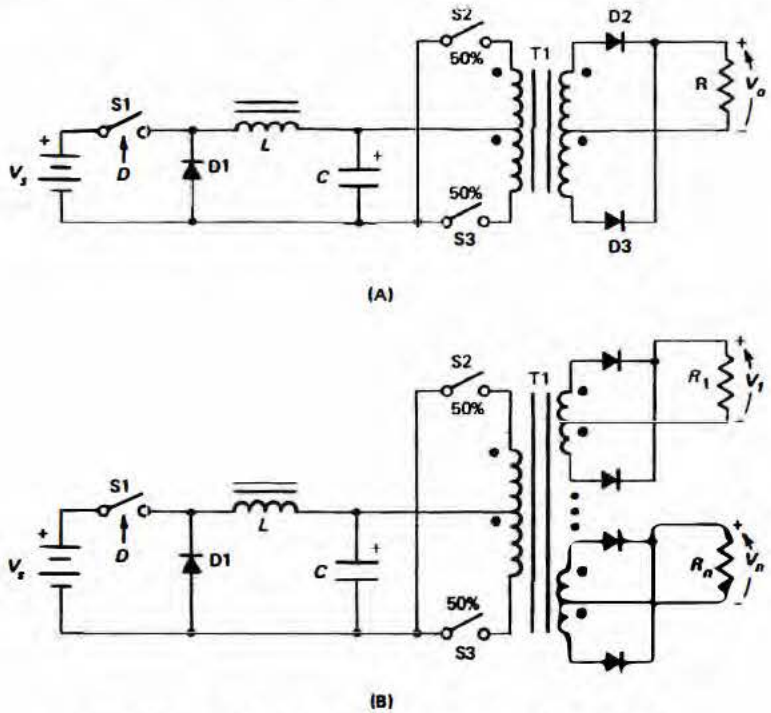


Fig. 5.2. The DC transformer inserted at location A-A′ in Fig. 5.1.

Even though the range of voltage gain (M) is no longer restricted to less than one and input-to-output DC isolation has been achieved, the converter of Fig. 5.2A (and those to follow in this chapter) still retains the basic properties of a buck SPC.

When the DC transformer insertion point is moved to position B-B′ of Fig. 5.1A, the converter shown in Fig. 5.3A results. This system also can have multiple outputs (Fig. 5.3B), but each output must now include a filter capacitor sized in proportion to its load. Since a practical DC transformer would have a small filter capacitor on any output as shown in Fig. 4.17B, its value need only be increased to meet the requirement just mentioned. Total effective filter capacitance seen on the primary side of the transformer will appear to the buck SPC as if a single-output were being provided. Also, the load appearing at the output of the buck SPC is simply the parallel combination of the secondary loads reflected to the primary side of the DC transformer.

In the converters of Fig. 5.3, the DC transformer is current-fed and we realize

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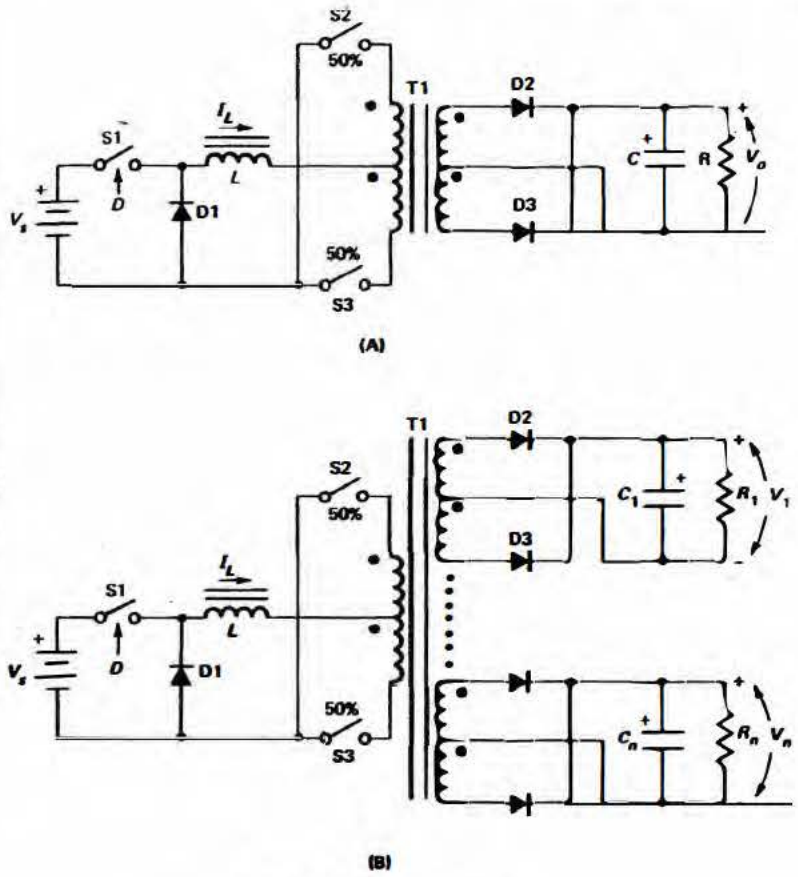


Fig. 5.3. The TRW converter.

the advantages of this type of source as outlined in Chapter 4. The well-controlled component stresses in these circuits make them particularly attractive for high power, multiple output applications.

There is no inherent requirement in the SPCs of Fig. 5.3 for the switching action of S1 to be synchronized with those of S2 and S3. They can be operated asynchronously, both in phase and frequency if desired. However, if S1 is operated at twice the switching frequency of S2 and S3 and locked in time phase with them, some advantage from a component stress standpoint can be gained, as shown by the circuit waveforms of Fig. 5.4.

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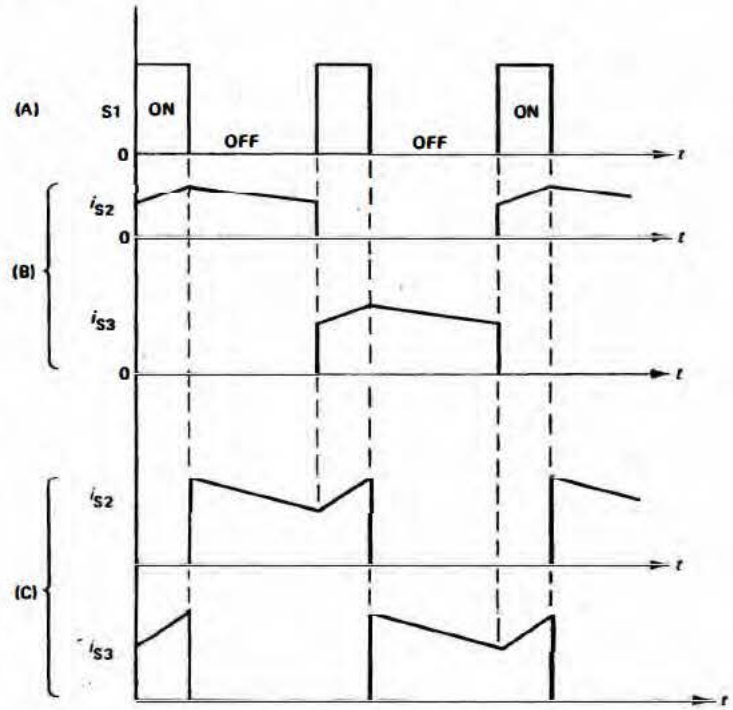


Fig. 5.4. Current waveforms for synchronized switching in the TRW converter.

Two synchronized possibilities are illustrated, switches S2 and S3 may be turned ON when S1 is turned ON or they may be turned ON when S1 is turned OFF. The resulting switch current waveforms are shown in Figs. 5.4B and C, respectively. The most desirable waveform is that shown in Fig. 5.4B, since this method of synchronization allows S2 and S3 to switch when the inductor current is at a minimum. If τ_L is not much greater than τ_{LC}, then the current stresses and corresponding switching losses in S2 and S3 can be quite small. This reduction in stress can be very helpful for applications where high output power is needed, or when high-frequency switching rates are required.

A small refinement could be added to the idealized waveforms of Fig. 5.4 so as to reflect potential overlaps in S2 and S3 conduction times. When both of these switches are ON, inductor current (I_L) divides between them. In this way, current levels are close to $I_L/2$ when the switches turn ON and OFF, which further reduces their switching losses.

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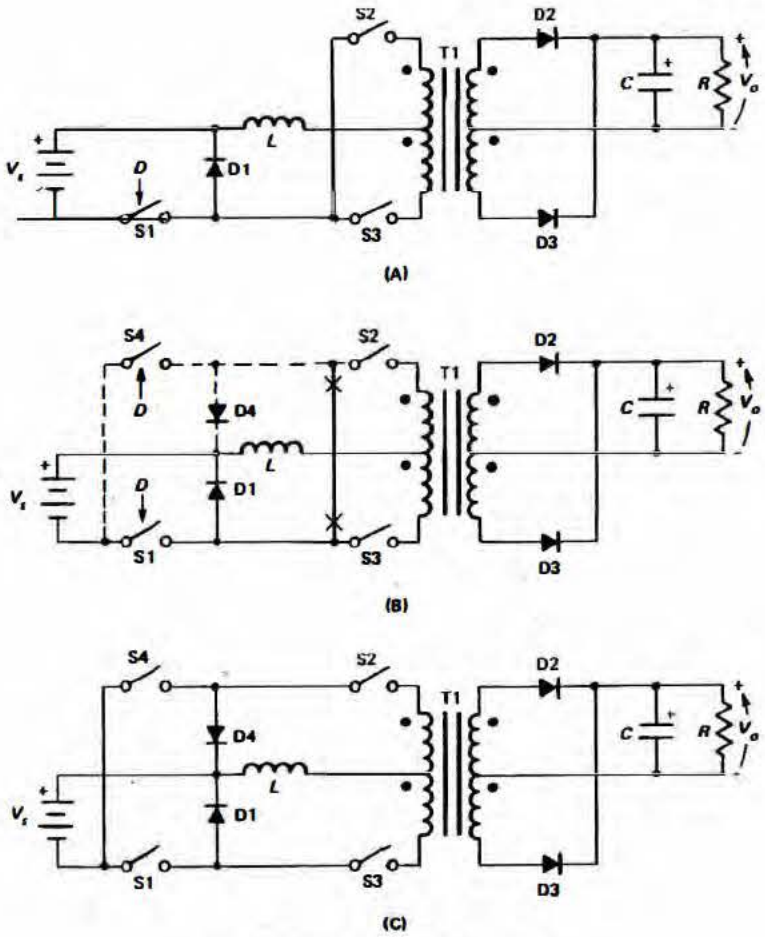


Fig. 5.5. Evolution of the IBM circuit.

The buck-derived converter of Fig. 5.3A can be modified in a number of interesting ways. One modification is shown in Fig. 5.5C, with intermediate evolutionary steps illustrated in Figs. 5.5A and B. In Fig. 5.5A, S1 is moved to the return point of the source voltage. Obviously, this move does not alter the switch or SPC function. The second step, shown in Fig. 5.5B, duplicates the original switch functions of S1 and D1 with the addition of S4 and D4. This

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step is completed by the removal of the connection between S2 and S3, which results in the converter system of Fig. 5.5C. Superficially, this "new" SPC would not seem to offer any advantages over that of the one shown in Fig. 5.3A, but a closer examination of it reveals that there are some operational differences, particularly in how the current in D1 and D4 commutates during a switching cycle of the system.

At the beginning of a switching cycle, S1 and S3 in Fig. 5.5C are both ON. Energy is stored in the inductor L and also delivered to the output load of T1 via diode D2. Part way through the switching period, S1 is turned OFF and the inductor current commutates to diode D1. Halfway through one complete switching cycle, the inductor current is then transferred from S3 and D1 to switches S2, S4, and diode D4. Because this is a current-fed converter system and the current through inductor L must be continuous (if operating in the continuous mode), switches S2 and S4 are closed before turning S3 OFF (remember—S1 is already OFF). The resulting reverse voltage appearing across D1 at this time will be smaller than that seen in the commutating diode of a normal buck SPC or its offspring shown in Fig. 5.3A. Lower reverse voltage will reduce the recovery time current transients through D1 as well as diode D4 on the next half cycle of converter operation. In a high-frequency or high-power converter application, these reduced current transient levels can significantly reduce electrical stresses on contemporary switch elements, lower commutating diode losses, and increase overall efficiency.

The SPC circuits in Figs. 5.2, 5.3, and 5.5 are very useful if their source voltage values are above 50 VDC. However, for lower source voltages, the conversion efficiency suffers because the inductor current must flow through two series switch elements during a substantial part of the switching cycle. This particular power loss problem can be eliminated by modifying the converter circuit of Fig. 5.5C, as shown in Fig. 5.6A. Here, circuit connection points for switches S1 and S4 are changed to the opposite ends of S2 and S3. The resultant switching sequence remains as described earlier, except that inductor current flows through only one switch element at any time in the switching cycle. The price paid for the elimination of one series element voltage drop is an increase in the peak OFF voltage across S1 and S2 from V_s to $(V_s + 2V_r)$, where V_r is the reflected load voltage through transformer T1. Since the SPC Fig. 5.6B is intended for low input voltage applications, this increased switch voltage stress is seldom a problem and represents a good trade.

The converter system of Fig. 5.6B is very useful, but it does have design drawbacks. First of all, it is relatively complex, using four switch elements and two primary commutating diodes. Second, the inductor current flows through both a switch and a diode during a portion of the switching cycle, which increases the power losses for low values of source voltage. As will be shown in Chapter 8, these losses can be reduced by using a tapped winding on transformer T1. How-

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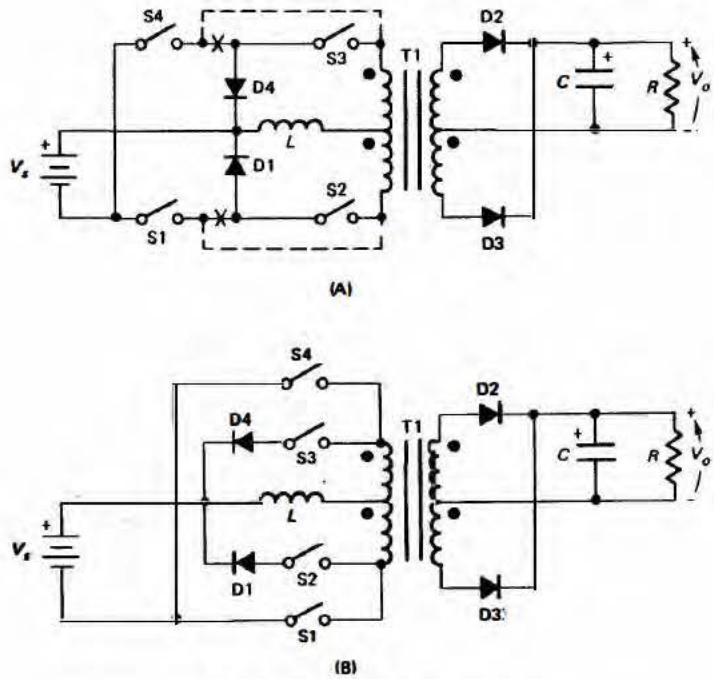


Fig. 5.6 Evolution of the Cronin circuit.

ever, a much better solution would be a reduction in the number of switches and commutation diodes.

Another buck-derived circuit exists which is very similar in structure to the one in Fig. 5.6B. This variation is illustrated in Fig. 5.7. Note that primary diode and switch connections are the same, but now a series inductor has been added on the secondary side of the converter. For multiple outputs from this converter, it is necessary to use a similar inductor on each individual output, as will be necessary for the quasi-squarewave converter to be discussed later in this chapter. This SPC circuit variation does not appear to have any advantages over the one shown in Fig. 5.6B and, in fact, has some significant disadvantages, the most serious one being the need for a multiplicity of inductors for multi-output applications. All such inductors must remain in a continuous current mode if reasonable cross-regulation of converter outputs is to be realized.

By making the inductor a two-winding element and repositioning the converter switches, the converter of Fig. 5.8 can be derived from the one shown in Fig. 5.6. This new circuit does not appear to have any advantages over its predecessor,

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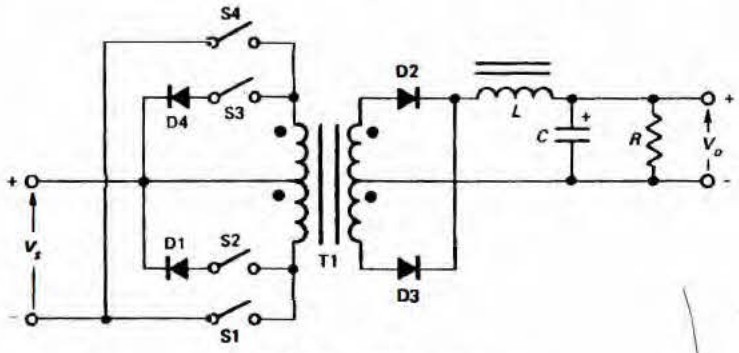


Fig. 5.7. The Hunter circuit.

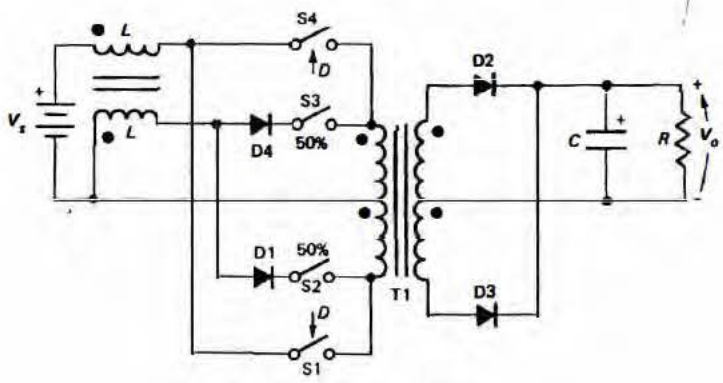


Fig. 5.8. The Severns circuit.

except that its structure is not patented and therefore lies in the public domain. It does, however, provide a conceptual stepping stone to another quite useful buck-derived converter, shown in Fig. 5.9A.

If S2, S3, and the secondary winding of inductor L in Fig. 5.8 are connected to the secondary side of T1 and the turns ratio of the windings on L made equal to the turns ratio of T1, then it is apparent that switches S2, S3 and diode D4 will no longer be needed and can be eliminated, as indicated in Fig. 5.9A.

We have now arrived at a current-fed converter circuit which uses only two primary switch elements with the inductor currents flowing through either a primary switch *or* a secondary diode D1, but *not* both simultaneously.

For low input voltage ranges, moderate winding transformation ratios and one or two outputs, the converter circuit of Fig. 5.9A is both simple and efficient.

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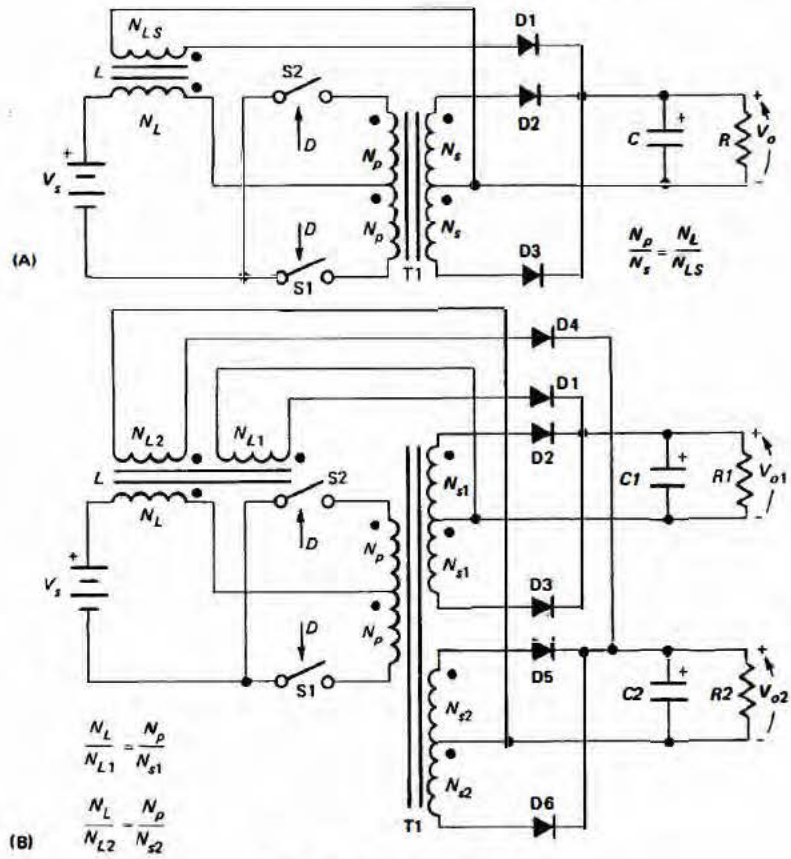


Fig. 5.9. The Weinberg circuit.

However, if large turns ratios are necessary between the windings of T1 and L, then switch voltage stress problems will arise from inherent primary-to-secondary leakage inductances. This can be a very serious problem at high output power levels for reasons mentioned in Chapter 4. To accommodate multiple outputs from this converter, inductor L must also have multiple windings and associated diodes as illustrated in Fig. 5.9B. When more than two outputs, high power delivery, or large transformation ratios are required, the converter circuit of Fig. 5.7 may be a better application choice.

There is another potentially serious problem which can occur in the converter circuit of Fig. 5.9A. Non-ideal transformers have finite magnetizing inductances.

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Therefore, during the intervals when both primary switches are OFF, the voltage across both primary transformer windings cannot be zero because transformer magnetizing current is discharging through one of the output diodes, thus clamping the secondary winding voltage to that of the output load. This implies that during concurrent OFF intervals of the primary switches, an additional voltage above that of the source *plus* the reflected output voltage from L will appear across one of the switches, raising the OFF voltage level across one and reducing the OFF voltage level across the other. In addition, the residual flux in transformer T1 may increase because of the impressed secondary voltage, in turn increasing the chances of core saturation. Fortunately, there is a rather simple cure for this problem, which is shown in Fig. 5.10. Here, an additional secondary diode is added in series with the inductor. Both inductor commutating diodes are then connected so as to force the transformer secondary voltage to zero during the interval when both primary switches (S1 and S2) are in an OFF state.

When input-to-output DC isolation is not required and when the converter output voltage is higher than its input voltage, a direct-coupled version of the circuit of Fig. 5.9A may be used. Two examples of this type of converter circuit are given in Fig. 5.11. Note that the primary inductor is now tapped, and for different values of transformer turns and inductor connections, boost voltage gain can be obtained. Adding the transformer demagnetization feature shown in Fig. 5.10 to the converters of Fig. 5.11 is accomplished by a separate winding on the transformer, as illustrated in Fig. 5.11C.

We can now return to Fig. 5.1 and insert the DC transformer at positions C-C′ and D-D′. The result is shown in Fig. 5.12A and B, respectively. From an inspection of these two SPC circuits, it can be seen that the commutating diode (D1) is no longer required in either case, since diodes D2 and D3 will pro-

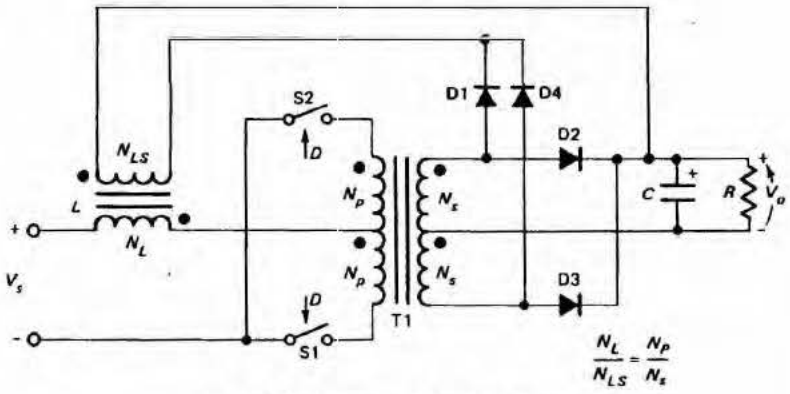
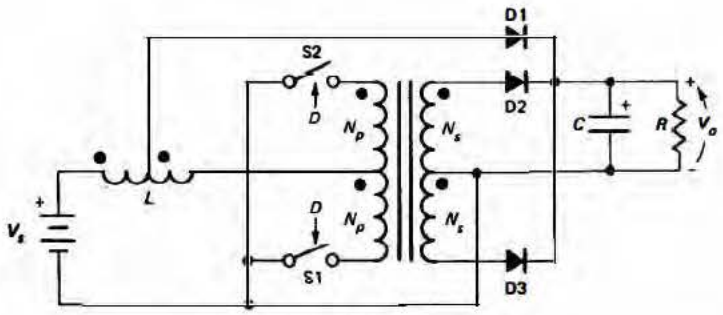


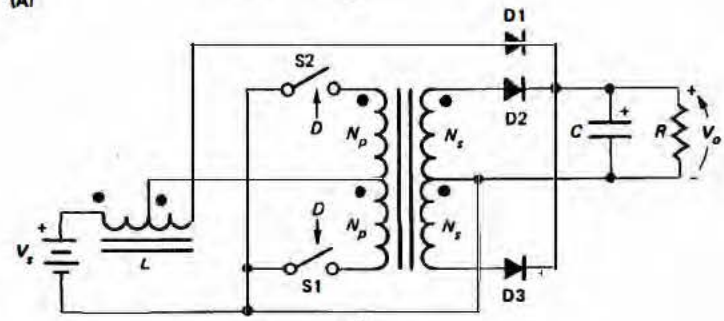
Fig. 5.10. An improved Weinberg circuit.

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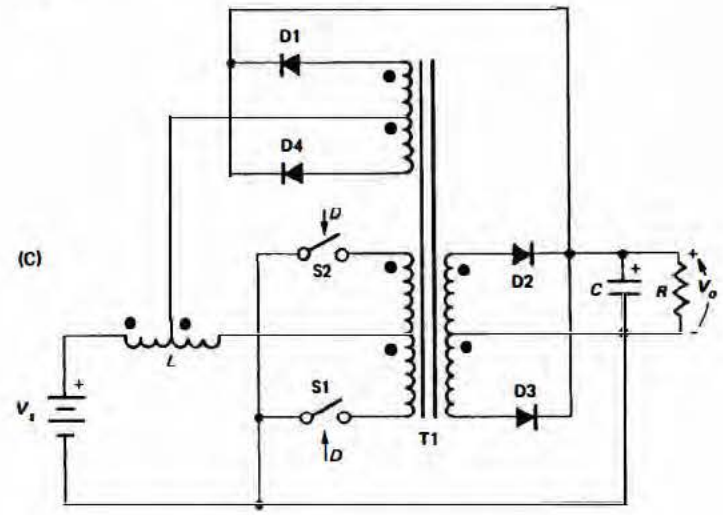
Boost Only If $\frac{N_p}{N_s} < 1$

(A)



Boost Only If $\frac{N_p}{N_s} > 1$

(B)



(C)

Fig. 5.11. Non-isolated Weinberg circuits.

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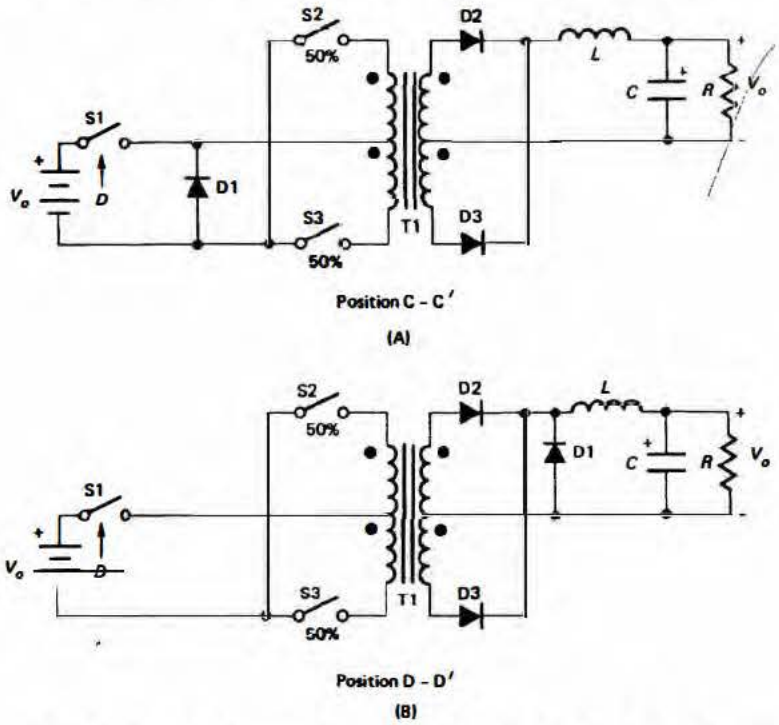


Fig. 5.12. The DC transformer inserted at locations C-C' and D-D' in Fig. 5.1.

vide this function of assuring continuous inductor current when switches S2 and S3 are both OFF. The two converters are therefore equivalent in operation. Occasionally, D1 is not removed from Fig. 5.12B in high output current applications. The reason for not removing D1 in this case lies in the fact that, during the converter intervals when S2 and S3 are OFF, the inductor current may commutate through D1 instead of through the two halves of the center-tapped transformer secondary winding via diodes D2 and D3. Therefore, the associated power losses in the secondary winding are reduced during inductor current commutation intervals.

Looking again at Fig. 5.12 we can see that the duty cycle control function of S1 could be performed by primary switches S2 and S3, since these latter switch elements are directly in series with S1 on alternating half-cylces. If duty cycle control of power conversion is moved to S2 and S3 (with S1 removed), the circuit in Fig. 5.13A emerges. The common name given to this circuit is the *parallel quasi-squarewave converter* and it is one of the most popular DC-DC conversion

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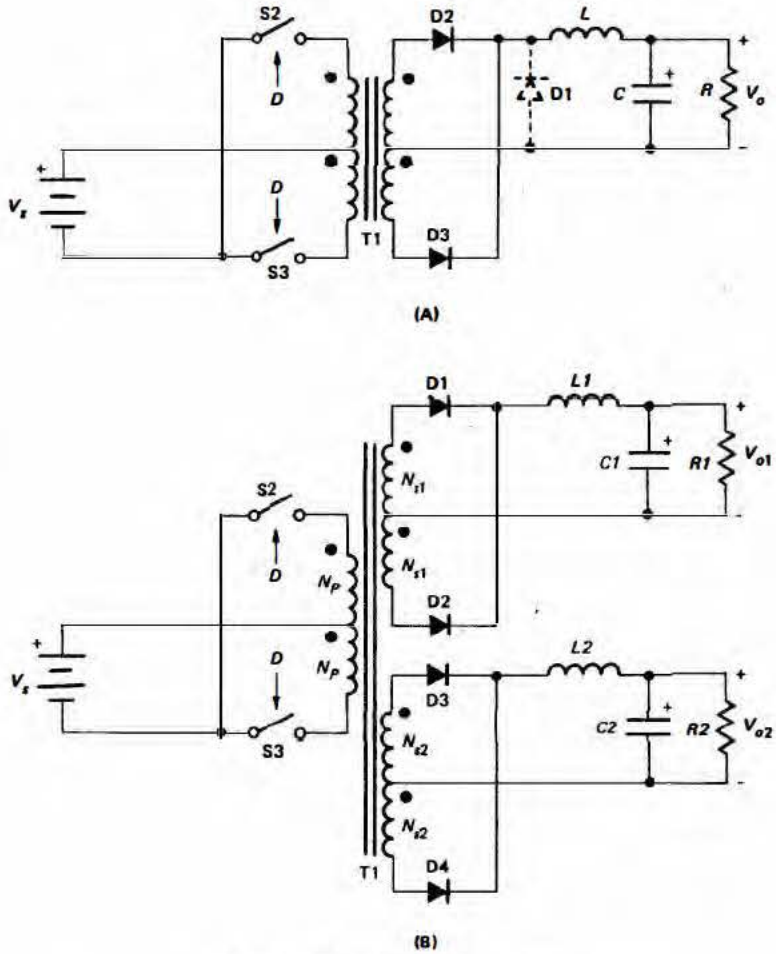


Fig. 5.13. The quasi-squarewave converter.

systems in use today. In applications requiring multiple DC outputs, additional transformer windings and filter networks can be added, as shown in Fig. 5.13B for a two-output case. Notice here that each DC output must have low-pass output filter. In this circuit, it is very possible for one output inductor to be operating in the continuous mode, with the other operating in the discontinuous mode! The character of any associated small-signal model of this SPC will depend on which converter output is being regulated. In normal operation,

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all filter inductors are usually maintained in the continuous mode to assure good cross-regulation between the regulated output and other unregulated ones. Any output of this SPC that drops out of the continuous mode will lose this highly desirable cross-regulation action. The problem of cross-regulation, as well as the number of output inductors required for multiple-output applications, are major draw-backs of this particular circuit approach. Another potential disadvantage is the fact that the DC transformer is now voltage-fed and therefore subject to transient currents produced by primary switch conduction overlap, transformer core saturation, and the other problems discussed in Chapter 4.

The final step in our evolutionary process is to insert the DC transformer at position E-E′ in Fig. 5.1. The resulting SPC is shown in Fig. 5.14A for a single-output application, and in Fig. 5.4B for multiple-output situations.

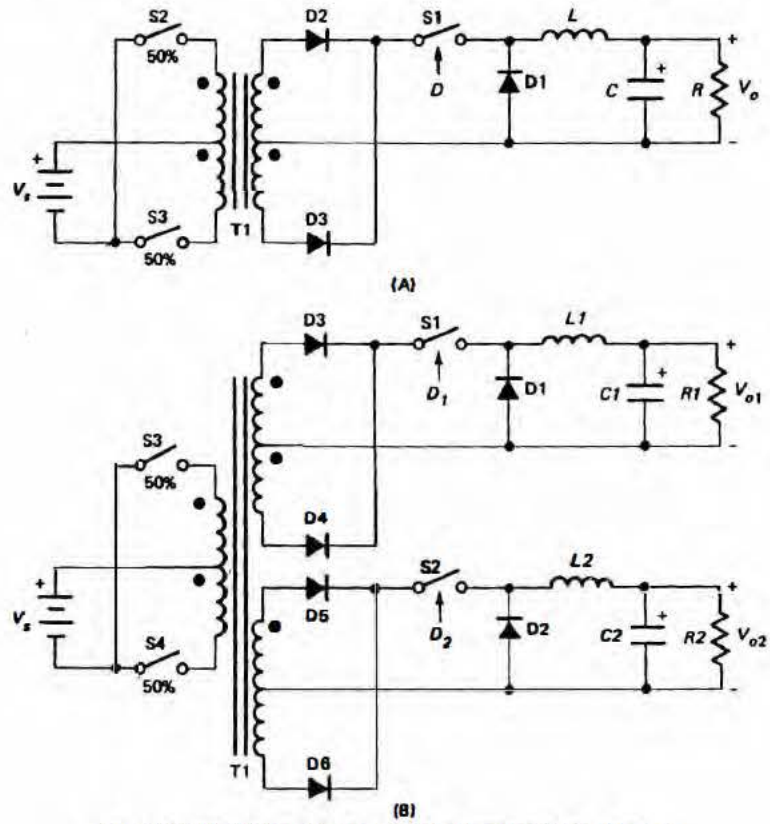


Fig. 5.14. The DC transformer inserted at location E-E′ in Fig. 5.1.

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This particular converter circuit is occasionally used and allows each of the outputs to be individually regulated by proper duty cycle control of the secondary switches (S1, S2 in Fig. 5.14B). The disadvantage of this circuit is the multiplicity of output switch elements. Because of their presence, the output switches add additional power losses in the converter, especially if the outputs are required to deliver high currents at low DC voltages.

A very common requirement encountered by designers today is the need for an SPC with one low-voltage (2-5 VDC) high-current output along with one or more higher-voltage (10-28 VDC) outputs with lower output current levels. If good voltage regulation and efficient conversion of power are required for all outputs, then the converter in Fig. 5.14B can be combined with the quasi-squarewave system of Fig. 5.13A. This possibility is shown in Fig. 5.15 for a two-output SPC. Here, the primary switch control loop is closed around the low-voltage high-current output, (V_{o2}). A separate switch (S1) and associated controls are used in the remaining secondary network to provide good regulation of the second DC voltage (V_{o1}). For this SPC to work properly, AC voltages

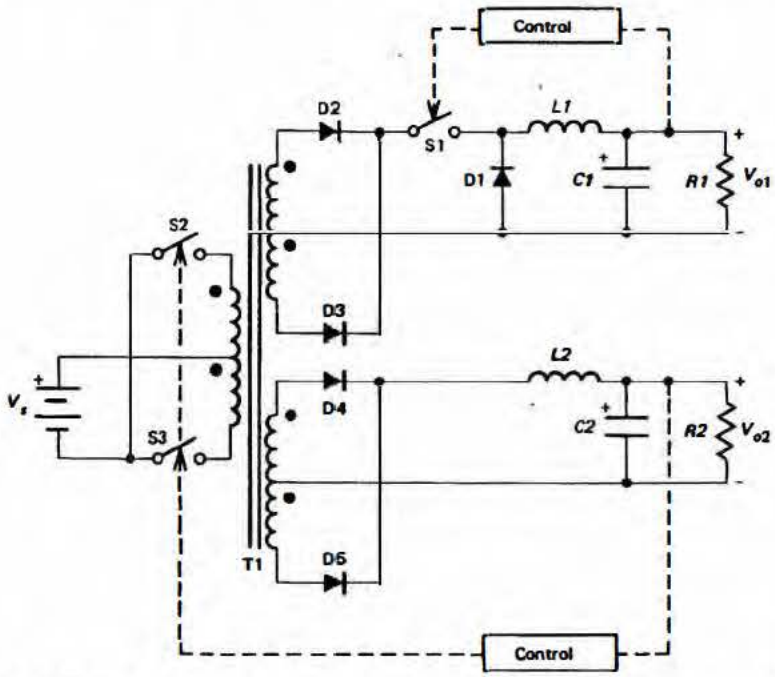


Fig. 5.15. The quasi-squarewave converter with an auxiliary post-regulator control system.

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across the second output winding of the transformer must be made large enough so as to give the second control switch (S1) reasonable duty cycle range for regulation of voltage V_{o1}. Since the SPC's primary switches are also duty cycle controlled, the AC voltages across the secondary of the second winding are regulated by control of V_{o2}; therefore, the duty cycle of S1 will remain close to 90% or better as the SPC's source voltage (V_s) changes as long as the inductors remain in the continuous mode.

5.2 FULL- AND HALF-BRIDGE DC TRANSFORMERS IN THE BUCK SPC

A problem common to all of the converters in Figs. 5.12 through 5.15 is that all primary switches (S2 and S3) will see a peak OFF voltage stress of twice the source voltage value (or greater, when transients are considered). These voltage stress levels can be reduced by using either a full or half-bridge DC transformers, rather than the parallel DC converter were used up to this point.

In the previous section, if a full-bridge DC transformer had been chosen in our evolutionary investigations, we would find that identical manipulations could be applied and similar circuits derived. Figs. 5.16 and 5.17 show the full-bridge

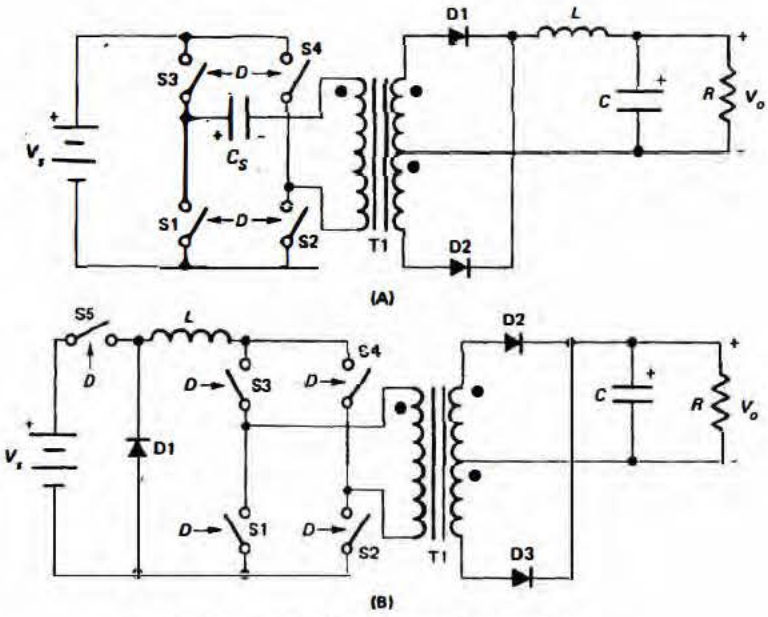


Fig. 5.16. Full-bridge buck-derived variations (1).

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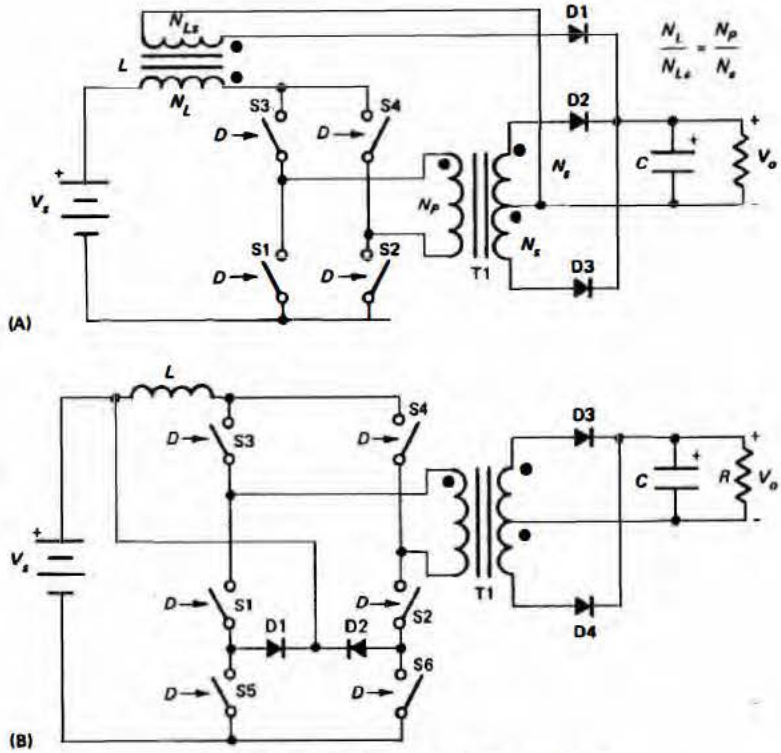


Fig. 5.17. Full-bridge buck-derived variations (II).

equivalent for the circuits of Figs. 5.16, 5.12, 5.9A, and 5.5C, respectively. Full-bridge versions of circuits are used when the need arises for high output power levels (>500 W) at high values of source voltage. From our full-bridge discussions in Chapter 4, the switches see a reduced peak voltage stress when they are in an OFF state. Here again, the presence of additional voltage stresses from inherent parasitic circuit elements has been ignored.

For lower power levels and high source voltages, the half-bridge versions, such as those shown in Fig. 5.18, are preferred.

Both the full and half-bridge SPCs call for an untapped single primary winding on their transformers. From a copper utilization standpoint, a single primary winding is advantageous and helps to reduce transformer manufacturing cost and increase its efficiency. In addition, the need to obtain good magnetic coupling between the two halves of the primary winding of a parallel transformer is eliminated.

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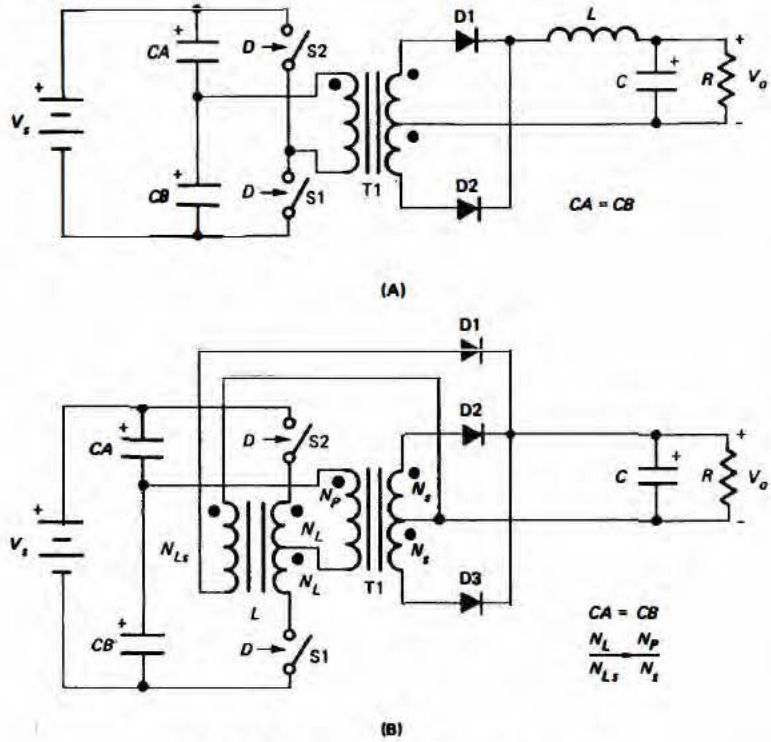


Fig. 5.18. Half-bridge buck-derived variations.

In Figs. 5.16 and 5.17, all of the primary switch elements are shown to be modulated in duty cycle. This is a usual mode of operation but not a mandatory one. Switches S1 and S2 or their counterparts S3 and S4 could be operated with fixed conduction duty cycles of 50%, with variable duty cycle modulation applied to the remaining switch pair. In some SPC applications, a simplification of switch drive circuitry will result. Alternatively, switches S1 and S3 or S2 and S4 may be operated at fixed 50% conduction duty cycles and duty cycle control applied to the other two switch elements.

5.3 THE SINGLE-ENDED DC TRANSFORMER IN THE BUCK SPC

Simplicity of topology is a very great virtue in a converter since it usually reduces cost and weight while increasing reliability. For this reason, converter circuits which use only one switch element are very popular among designers.

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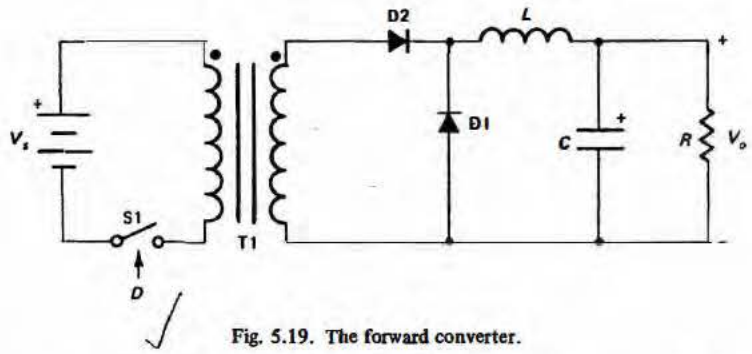


Fig. 5.19. The forward converter.

The single-ended form of the quasi-squarewave converter is shown in Fig. 5.19. This circuit is commonly known as the *forward converter* and is widely used in Europe. Applications of the forward converter using a single BJT switch and having an output power of 2 kW or more do exist, although this SPC is normally used at much lower output power levels. It is debatable for many practical reasons if this SPC is really advantageous at very high power levels.

As was pointed out in Chapter 4, a practical single-ended DC transformer circuit must have some provision for transformer core reset. If we apply the reset schemes developed in Section 4.2 to the forward converter of Fig. 5.19, a wide variety of related circuits can be evolved. A few of the resulting converter possibilities are shown in Figs. 5.20 through 5.24.

If a physically smaller transformer with better core utilization properties is desired, then current reset schemes can be used. Three possible methods are illustrated in Fig. 5.22. Reset using a tertiary winding and a current source (Fig. 5.22A) is fairly common; however, this approach can be readily accomplished by using the current source of the output filter, namely, inductor L!

As shown in Fig. 5.22B, the current in inductor L may be used as a means of core reset by simply providing a tap on the transformer secondary and a diode (D1) for connection to the inductor. The transformer core may also be reset by using a field bias from a built-in permanent magnet, as shown in Fig. 5.22C. Biased cores are commercially available and usually made of ferrite materials with inherent permanent magnets.

There is one mechanism missing from the SPC circuits in Fig. 5.22, namely, a means for controlling the amplitude of the primary voltage during core reset intervals. Some limits must be placed on these amplitudes to protect the SPC switch element from possible voltage breakdown. Any of the voltage clamp schemes of Chapter 4 may be used, one example of which is shown in Fig. 5.23.

It might appear that the choice of reset schemes is an arbitrary one, but such is not the case. The reset scheme chosen will determine the maximum duty cycle

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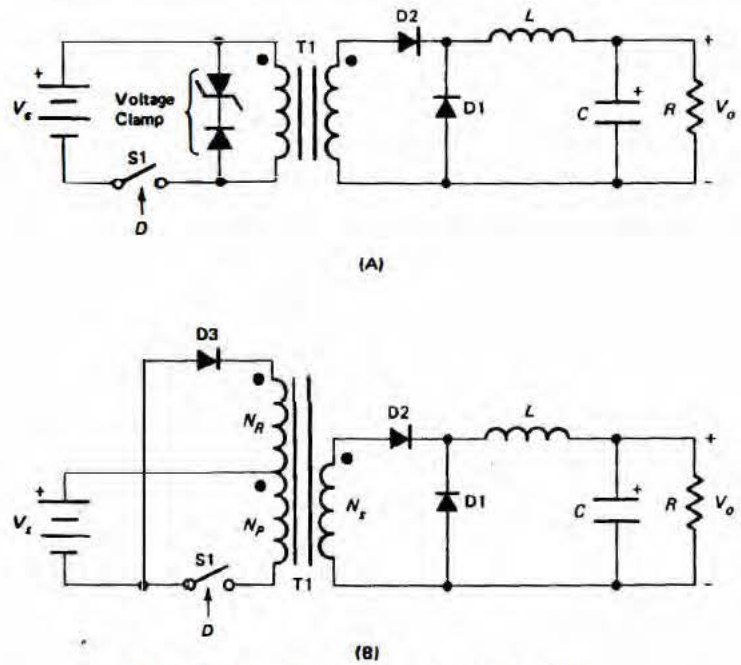


Fig. 5.20. Forward converter core reset variations (1).

limit of primary switch control which, in turn, determines the peak switch OFF voltage level and ON current value.

Since the forward converter of Fig. 5.19 is buck-derived and therefore has the properties of a buck SPC, the maximum value of switch duty cycle will occur at the lowest source voltage and highest load value. As V_s increases, the duty cycle (D) of the primary switch (S1) will decrease. The larger D can be made, the smaller the peak switch current will be, and the power level which can be controlled by a given switch will be greater.

Other reasons for maximizing switch duty cycles are the resulting reductions in the physical size of inductor L and the rms current in any input filter capacitor across the source voltage. In an elementary buck SPC, as its source voltage approaches minimum value, the switch duty cycle could approach unity in order to maintain output voltage regulation. However, in the forward converter, some time is always required to reset the core of its transformer. We can make D larger by making V_s larger, but we must be careful not to exceed the breakdown rating of the switch when V_s goes to its highest value. An ideal voltage

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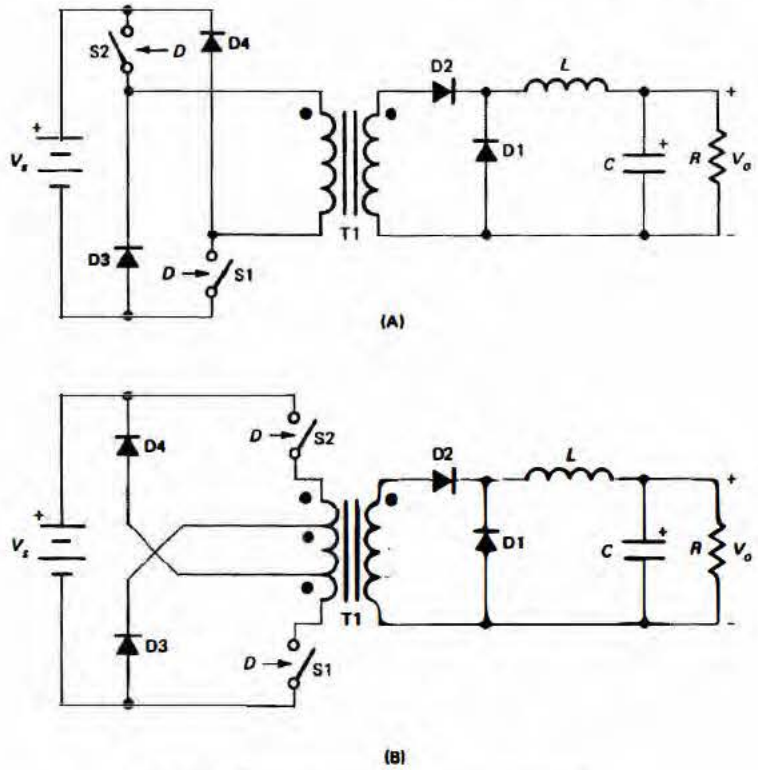


Fig. 5.21. Forward converter core reset variations (II).

reset scheme would provide a high reset voltage when V_s is low and a lower reset voltage when V_s is high. This would allow the maximum possible value for D at the lowest value for V_s for a given voltage rating of the switch. Unfortunately, this ideal reset scheme is not easily realized and most circuits are a compromise. The best compromise is to use a constant reset voltage such as that shown in Figs. 4.5 and 4.6B. The variable reset scheme given in Fig. 4.6A is the worst, since the *lowest* reset voltage occurs at the *lowest* value of V_s–just the opposite of what is desired.

In practice, limit values of D from 60 to 70% are quite common. Compared to a parallel DC transformer quasi-squarewave converter (Fig. 5.13A), the forward converter topology uses only one switch element and requires fewer windings on its transformer. On the other hand, the inductor and transformer of the

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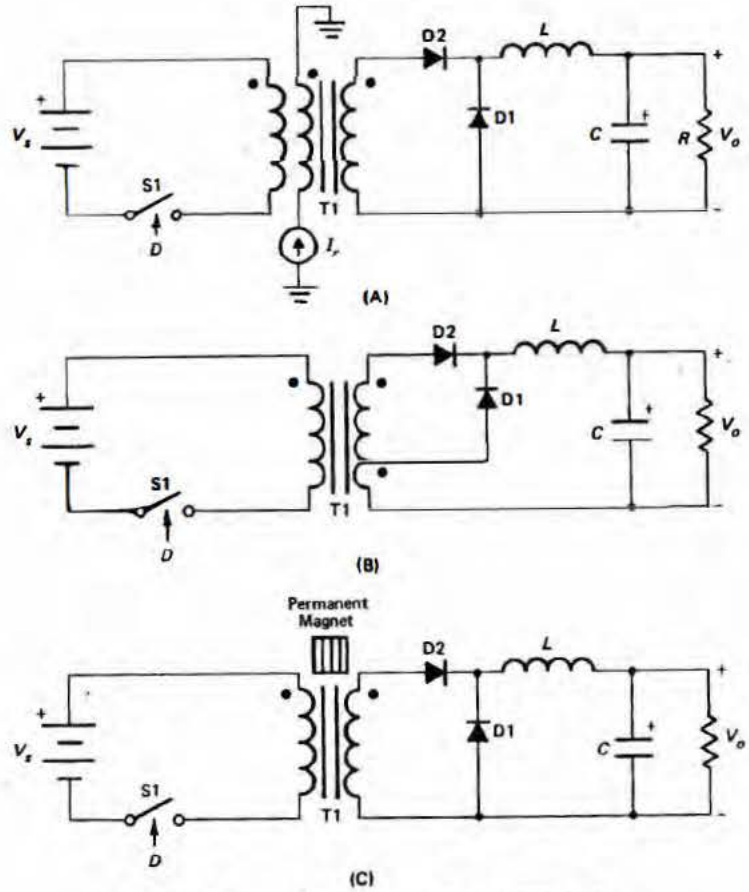


Fig. 5.22. Forward converter core reset variations (III).

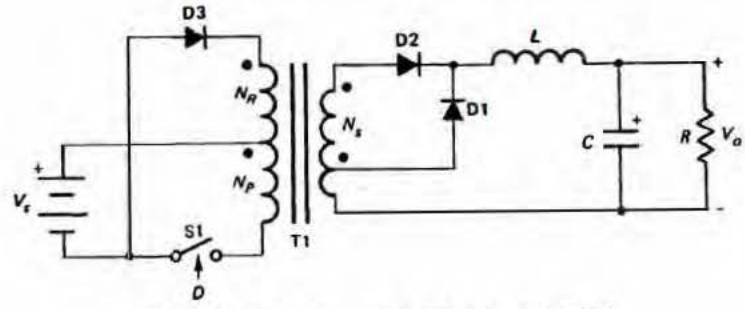


Fig. 5.23. Forward converter core reset variations (IV).

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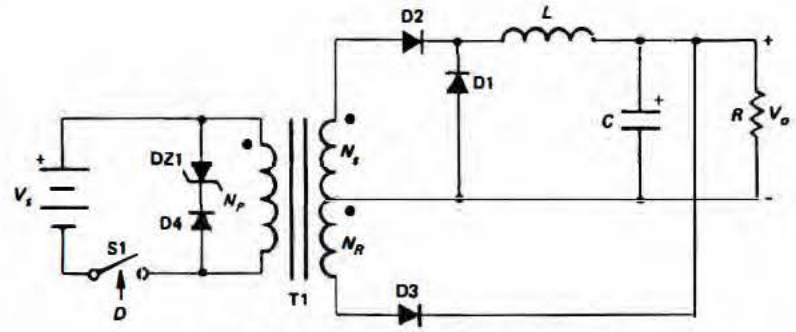


Fig. 5.24. Forward converter core reset variations (V).

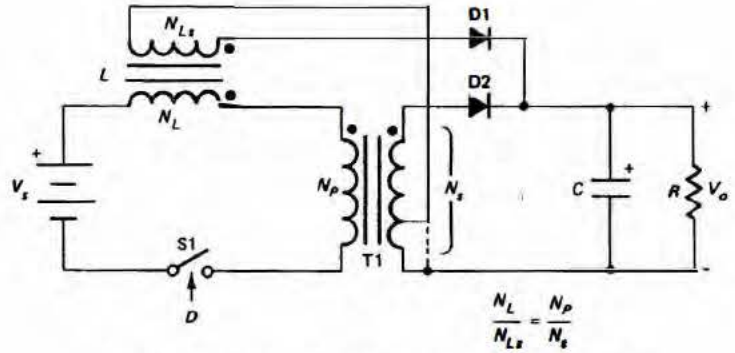


Fig. 5.25. An example of a single-ended Weinberg converter.

forward SPC are usually physically larger than their contemporaries in a symmetrical quasi-squarewave SPC.

Single-ended transformer equivalents are not limited to reduced forms of the quasi-squarewave SPC, although the forward converter just discussed is the most popular and in wide use today. A single-ended version of the SPC circuit of Fig. 5.9A is shown in Fig. 5.25, as an example of another circuit form which uses a different parent. By applying the various core reset schemes described for the forward converter, another generation of single-ended SPC's based on the converter of Fig. 5.25 would result.

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6. Boost-Derived Circuits

In this chapter, we will essentially repeat the evolutionary processes of Chapter 5, using the basic boost SPC of Chapter 3 as our starting point. As a result, a large family of boost-derived SPC circuits will be created.

It is interesting to note that most of the buck-derived circuits of Chapter 5 were developed independently by many individual designers over the past twenty year period. However, the processes used to demonstrate electrical relationships between them were developed after many buck-derived converters were in more or less popular use. Such was not the case for boost-derived SPCs with relatively few examples of derivative converters to be found only in recent literature. In this chapter, the procedures which we used to show the relationships among buck-derived SPC circuits become synthesis tools to develop new boost-related SPCs. In many cases, the resulting SPCs will be unusual and interesting in form. Many of the boost-derived circuits to be discussed arise from repeating simple manipulation techniques that were applied to the buck-derived circuits of Chapter 5.

All of the circuits to be developed in this chapter retain the basic properties of the elementary boost converter with the exception that DC isolation, arbitrary input-to-output voltage ratio, and multiple-output capability are now possible.

6.1 PARALLEL DC TRANSFORMERS WITHIN BOOST CONVERTERS

Five logical points to insert a DC transformer element into the basic boost SPC are shown in Fig. 6.1.

Insertion of the DC-DC transformer at A-A′ results in the converter of Fig. 6.2, a pre-regulated DC-DC converter with a boost SPC as the pre-regulation circuit. This converter can be advantageous if its source voltage has a low value (e.g., 12 VDC mobile applications) because the DC transformer switches can operate at higher voltage and lower current levels. In general, for low values of input voltage, this circuit will be more efficient than its buck-derived counterpart of Chapter 5.

When the DC-DC transformer is inserted at location B-B′ or C-C′ of Fig. 6.1,

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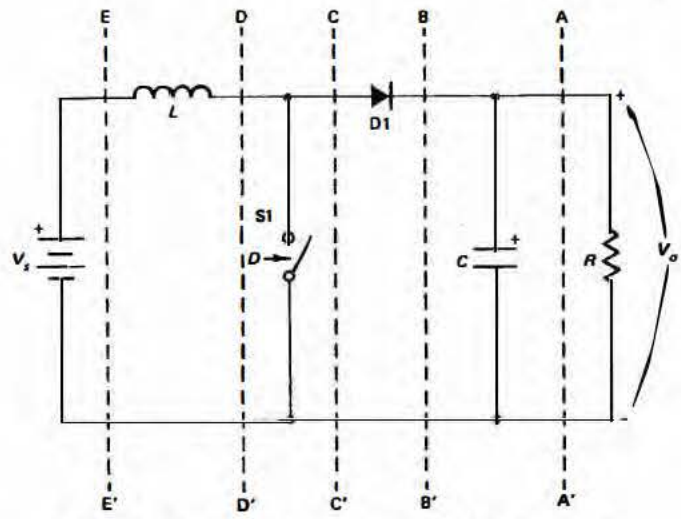


Fig. 6.1 DC transformer insertion points in the boost converter.

the equivalent converters of Fig. 6.3 appear. Again, we have a case where D1 is not required for the circuits to function properly, and therefore can be omitted, as illustrated in Fig. 6.4A.

The SPC circuit in Fig. 6.4A is a viable conversion approach, but it does use three switch elements. If the duty cycles of S2 and S3 are made variable and always greater than 50% (i.e., if S2 and S3 have *overlapping* conduction intervals)

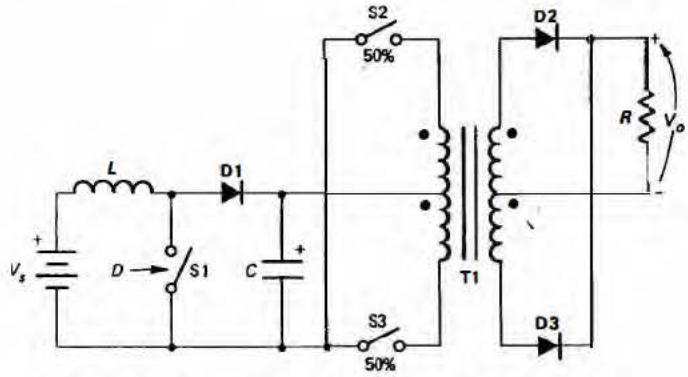


Fig. 6.2 The DC transformer inserted at location A-A' in Fig. 6.1.

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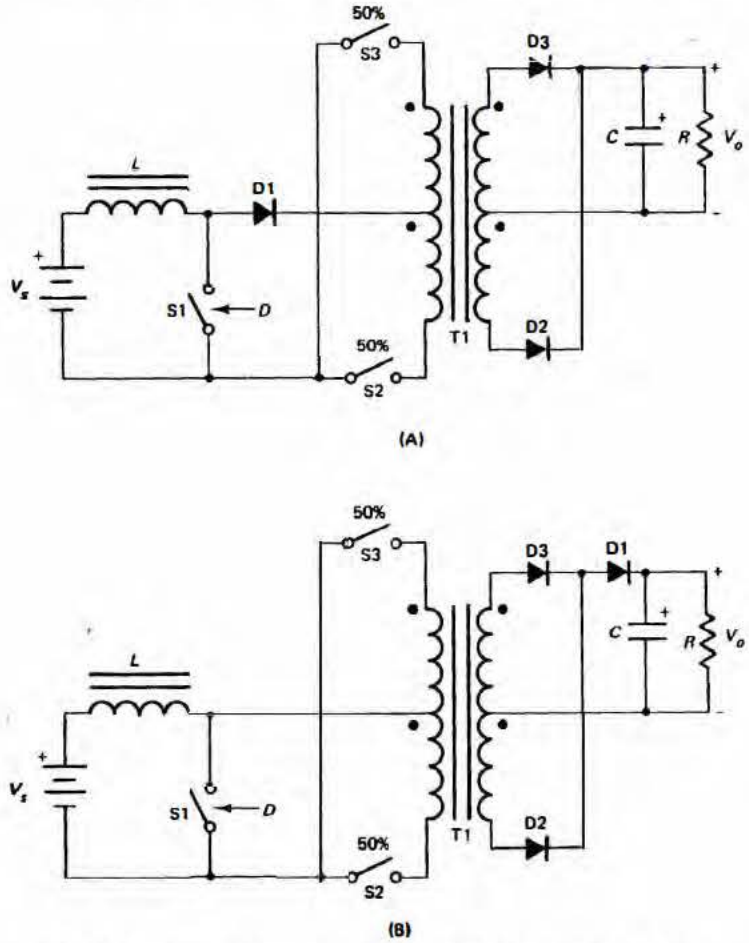


Fig. 6.3 The DC transformer inserted at locations B-B' and C-C' in Fig. 6.1.

so as to permit the primary of the transformer T1 to present a short circuit to inductor L for a portion of each half cycle), then S1 is no longer needed and it can be eliminated as shown in Fig. 6.4B. Fig. 6.4B also gives an indication of how easily a need for multiple outputs can be accommodated. One of the advantages of the overlapping primary switch conduction is the equal division of inductor current between S2 and S3, thus reducing their average and rms current

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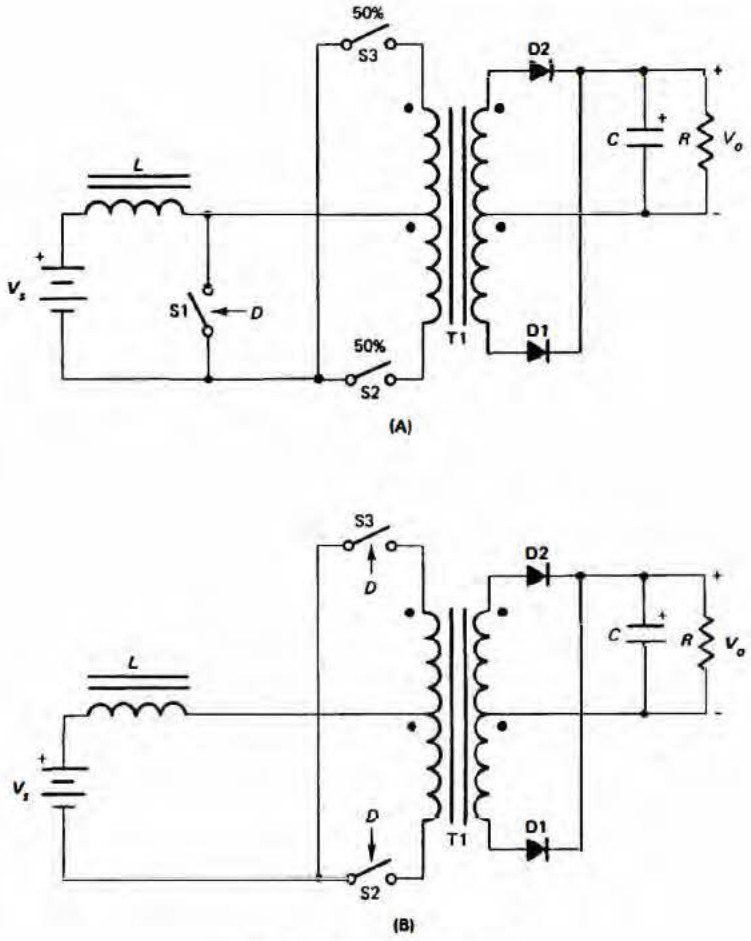


Fig. 6.4. The Clarke circuit.

levels as well as the primary winding rms current magnitude. When MOSFET devices are used as the switch elements, a significant improvement in conversion efficiency can be achieved here.

Proceeding to position D-D′ of Fig. 6.1 and inserting the DC transformer produces the converter circuit of Fig. 6.5A, in which the shunt switch now appears on the secondary side of the transformer. Having this duty-cycle modu-

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lated switch in this position can be very advantageous, if strict DC isolation is required between primary and secondary circuits as well as for associated voltage regulation controls. Here, any regulation control circuitry can share a common reference with the output voltage being monitored.

The converter in Fig. 6.5A does have one potential problem. If the SPC's output is required to deliver a low DC voltage at high current levels, then having D1 in series with the rectifiers (D3 and D2) can cause unacceptable power losses. In addition, the ON current of S1 will be large, further increasing such losses. This problem can be fixed quite easily, as shown in Fig. 6.5B, where the clamp diodes (D1, D2) along with the secondary switch are operated at higher voltage and lower current levels, with the converter's output current flowing only through each of the rectifier diodes (D3, D4).

This idea of secondary-referenced duty cycle control can be extended, as shown in Fig. 6.5C, by placing S1 on a separate auxiliary winding. This provides not only DC isolation between the primary and both secondaries, but also between any voltage regulation control switch element! The auxiliary winding also allows the voltage and current levels in S1 to be optimized to suit the capabilities of the device used to realize the switch function. As shown earlier for the converter of Fig. 6.4B, auxiliary transformer windings can also be added to produce multiple outputs if desired.

In the converters of Fig. 6.5, it is not mandatory that S1, S2, and S3 operate synchronously, but it is definitely advantageous. If S1 operates at twice the switching frequency of S2 and S3, and if S1 and S2 or S1 and S3 are turned ON simultaneously, then S2 and S3 will turn ON and OFF at inductor current minimum points, much as was observed for the current-fed buck converters in Fig. 5.3.

If the core of the transformer is made from a material with a high-B_r characteristic (often termed a "square-loop" material), then a number of additional boost-derived circuits become possible. In the converter shown in Fig. 6.6A, the conduction of duty cycle of S1 and S2 is fixed, usually just over 50% for slight overlaps. The switching frequency (f_s) is the control variable for regulation and is adjusted so that transformer T1 goes into saturation on each half cycle of the switching sequence. Saturation of T1 emulates to a great degree the same "shorting" function as the shunt control switch of Fig. 6.4. As f_s is made lower, the time spent by the transformer primary in a "shorted" condition over a half-cycle interval ($T_s/2$) will become greater. Therefore, the output voltage (V_o) is inversely proportional to the value of f_s. The converter of Fig. 6.6A works very well as long as switching frequency is kept low enough so that the transformer core can be driven from $+\phi_s$ to $-\phi_s$. As the switching frequency is raised, a point will be reached where core temperature rise from power losses may become excessive, at which time $\Delta\phi$ must be reduced. Keep in mind that the trans-

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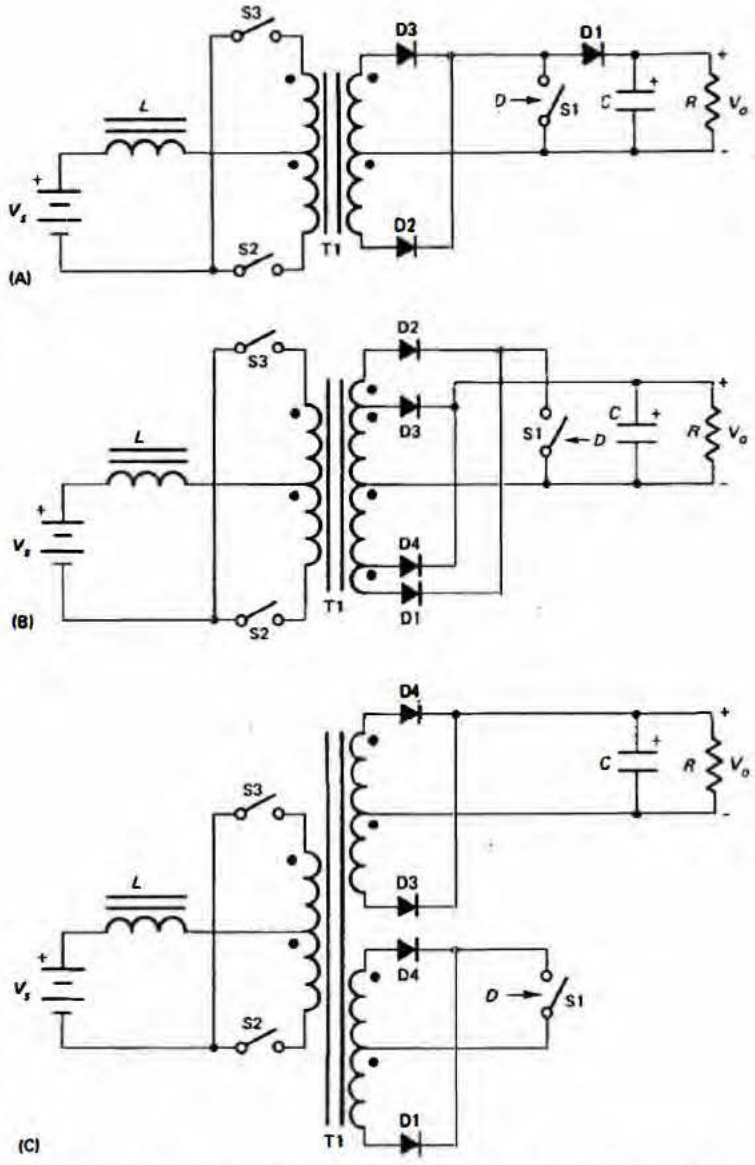


Fig. 6.5. The DC transformer inserted at locations D-D' in Fig. 6.1 with variations.

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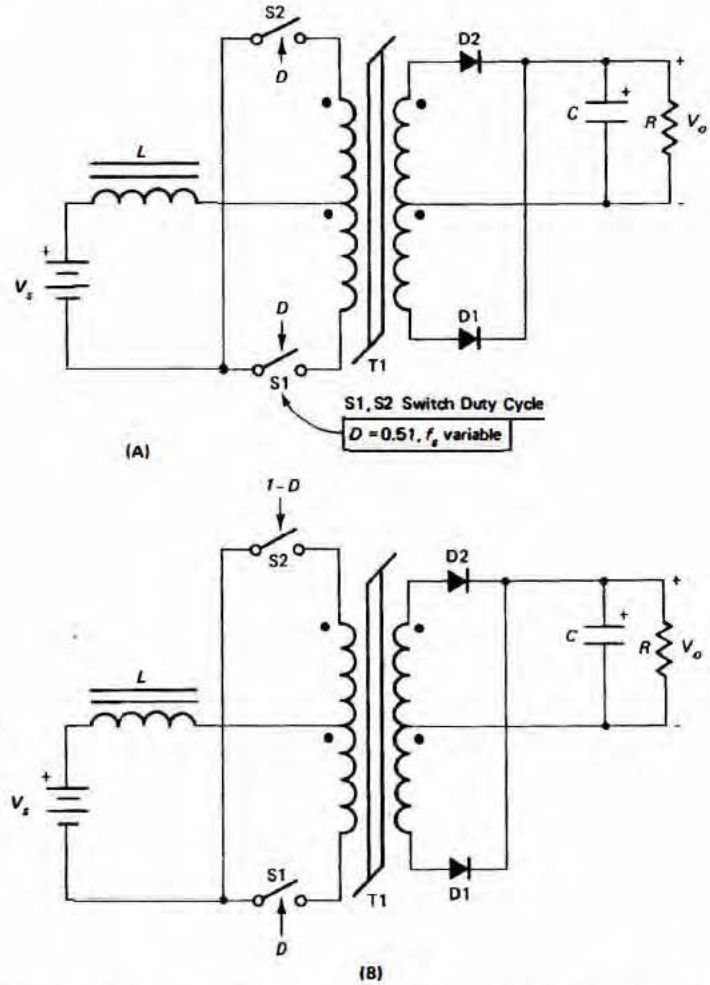


Fig. 6.6. Fixed duty cycle, variable-frequency and asymmetrical duty cycle boost-derived converters.

former core material chosen will place an upper boundary on the switching frequency.

Alternative converter circuits which exploit the saturable properties of a square-loop core material allow for arbitrary changes in flux and operate at a fixed switching frequency, as shown in Fig. 6.6B and Fig. 6.7. In the SPC of Fig. 6.6B,

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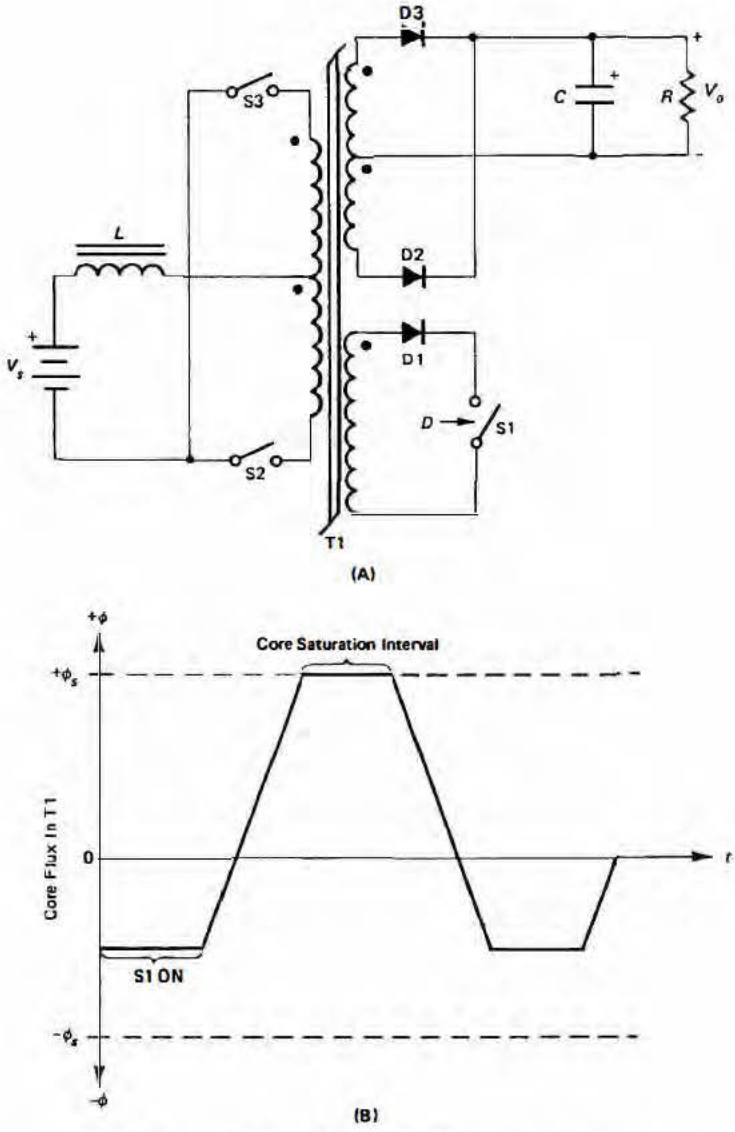


Fig. 6.7. A secondary shunt-switch saturable-core converter circuit.

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the duty cycles of S1 and S2 are deliberately made asymmetrical so that during each full switching cycle the transformer core saturates, as it cannot support any significant asymmetry in primary volt-second levels. Here it is not necessary that both primary windings be identical in number of turns, but reasonably good magnetic coupling between them is still highly desirable. By making the windings asymmetrical, the two switch duty cycles of conduction can be altered to more favorably distribute the conversion power losses between them.

The circuit in Fig. 6.7A is rather unusual in that, on alternating half cycles, the primary "shorting" action is provided first by the closure of switch S1 and then by saturation of the core of T1. A diagram showing typical core flux excursion as a function of switching times is illustrated in Fig. 6.7B.

One of the simpler boost-derived SPCs from an overall circuit point of view is shown in Fig. 6.8. Here, switches S1 and S2 are operated at a fixed duty cycle and the saturation time of transformer T1 is controlled by the magnitude of the bias current source, I_c. This converter eliminates the need to modulate the primary switch conduction intervals. The modulation action is performed by the transformer alone, lending considerable simplification to the SPC's control circuitry. To adjust the gain due to I_c, N_c can be varied. It may also be advantageous to make the fixed duty cycles of S1 and S2 asymmetrical. Alternatively, transformer turns N_1 and N_2 may be made asymmetrical. Both of these alter-

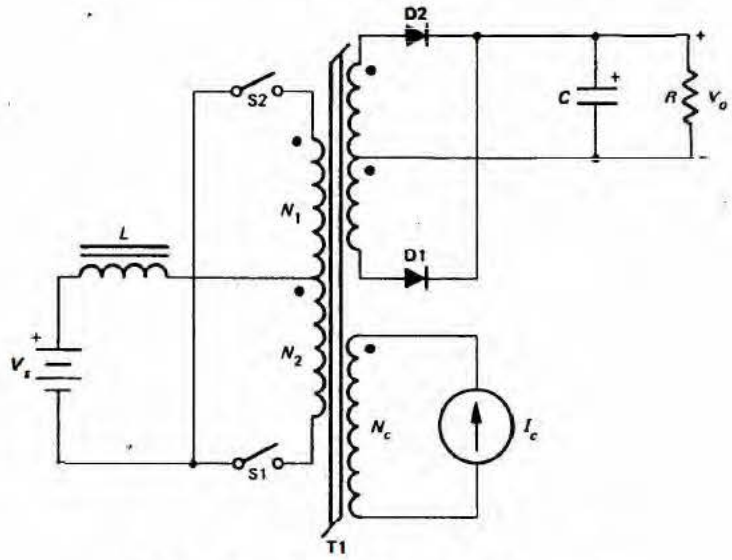


Fig. 6.8. A current-controlled boost-derived converter.

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natives would have the effect of supplying a fixed DC bias for T1 and allowing the operating point of I_c to be adjusted accordingly in an optimum fashion.

Many boost-derived current-fed converters have an inherent problem when their switching action is shut down. For example, if drive power is suddenly removed from all converter switches, what happens to the stored energy in the inductor L? In many cases, in the absence of protective circuit arrangements, this energy will be dissipated by avalanche breakdown of the converter's switch elements. For BJTs, in particular, this can be a fatal situation. Two commonly used methods to circumvent this energy removal problem are shown in Fig. 6.9.

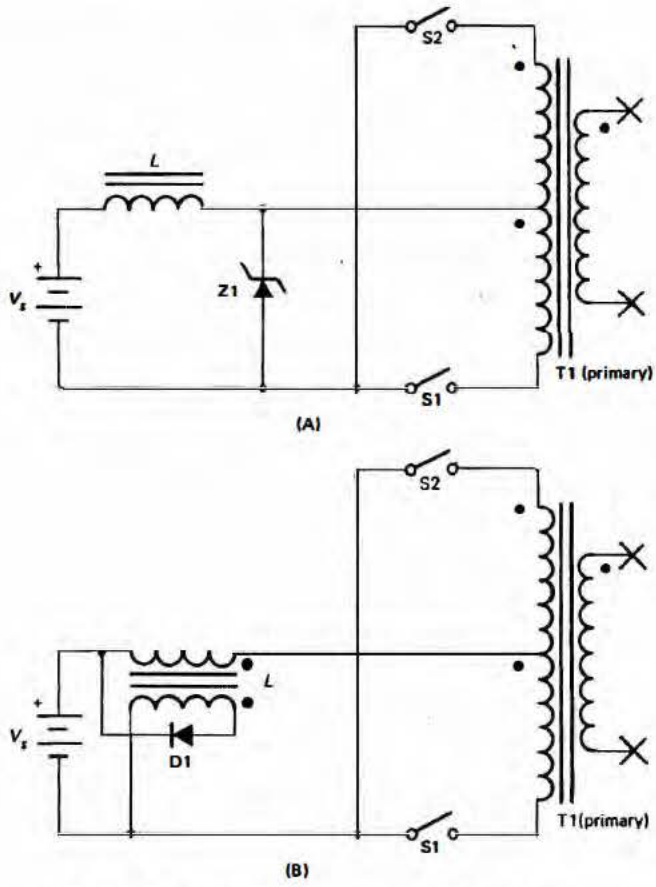


Fig. 6.9. Boost-derived converter switch protection schemes.

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In Fig. 6.9A, residual energy of the inductor at converter shutdown is dissipated in a shunt power zener diode. Since this zener needs to absorb only the energy in L on a one-time basis (at converter turnoff), it does not have to dissipate much average power and can be quite small. An alternative measure is shown in Fig. 6.9B, where a secondary winding has been added to inductor L. Thus any residual energy will be returned to the SPC's voltage source. The turns ratio of this auxiliary winding relative to the primary is adjusted so that the commutating diode (D1) does not conduct during normal converter operation. This condition usually implies that voltage magnitudes across converter switches could be higher than that produced by the clamp of Fig. 6.9A, especially if the source voltage is large at the instant of SPC system shutdown.

6.2 BRIDGE AND HALF-BRIDGE DC TRANSFORMERS WITHIN BOOST CONVERTERS

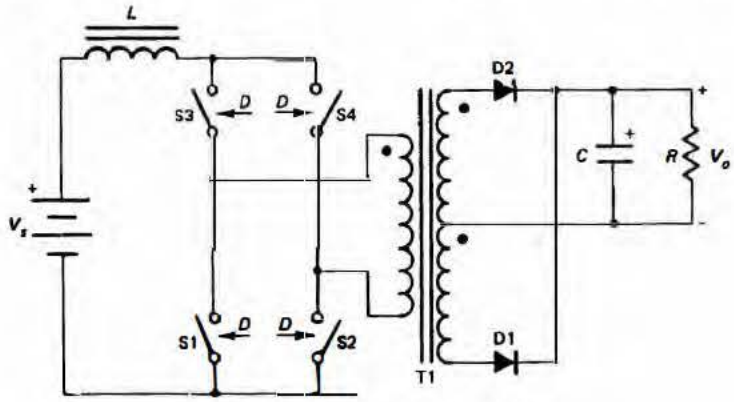
We can insert full and half-bridge DC-DC transformers within basic boost SPCs just as easily as was possible for the buck-derived converters of Chapter 5. Two circuit examples are shown in Fig. 6.10A and 6.10B.

Examination of the SPC circuit in Fig. 6.10A reveals that a variety of switch sequences can be accommodated without compromising conversion performance. Three of these sequencing possibilities are shown in Fig. 6.11. In Fig. 6.11A, all four switch elements have conduction duty cycles greater than 50%. Here, twice each switching cycle, all four switches are ON simultaneously. If MOSFETS are used as switch elements, then the inductor current will divide relatively equally between switch sets S1 and S3 and S2 and S4. This current-sharing feature reduces primary switch rms current levels, especially at low input voltages when switch overlap interval and inductor current are at their maximum values. When BJT switches are used, current-sharing may not be equalized to the same degree. Therefore, one pair of BJT switches may take more load current than the other pair.

In a full-bridge converter, at least two of the primary switches will require DC-isolated drives. The simplest and most common means for providing an isolated drive network is to use transformer-coupling between the drive source and the associated power switch element. In a buck-derived bridge converter, a single drive transformer with multiple-output windings (e.g., see the circuit of Fig. 4.15) can be used since switch duty cycle (D) of conduction is always less than 50%. However, in boost-derived bridge converters, D is greater than 50% and a separate drive transformer will be necessary for each DC isolated switch element. Additional drive networks complicate overall design and their number should always be minimized.

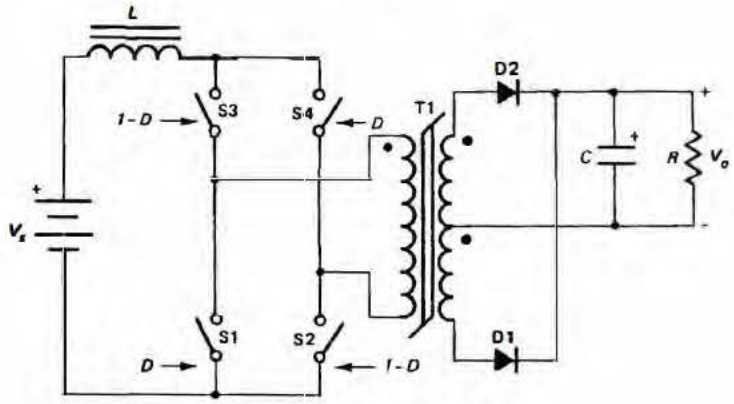
The switch drives can be simplified by using the timing sequence shown in Fig. 6.11B, where S3 and S4 are operated at a fixed D of 50% and duty cycle

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Primary Switch Overlapping Conduction

(A)



Asymmetrical Switch Modulation

(B)

Fig. 6.10. Full-bridge boost-derived converter variations.

control applied only to S1 and S2. This sequence simplifies the drive problem, but now only two SPC switches are ON during conduction overlap periods.

A further drive simplification is shown in Fig. 6.11C. Here all four SPC switches are operated with a conduction duty cycle of 50%, with the conduction phase of S1 and S2 varied relative to that of S3 and S4. This sequence produces a conduction overlap twice each complete switching cycle, once by S1 and S3

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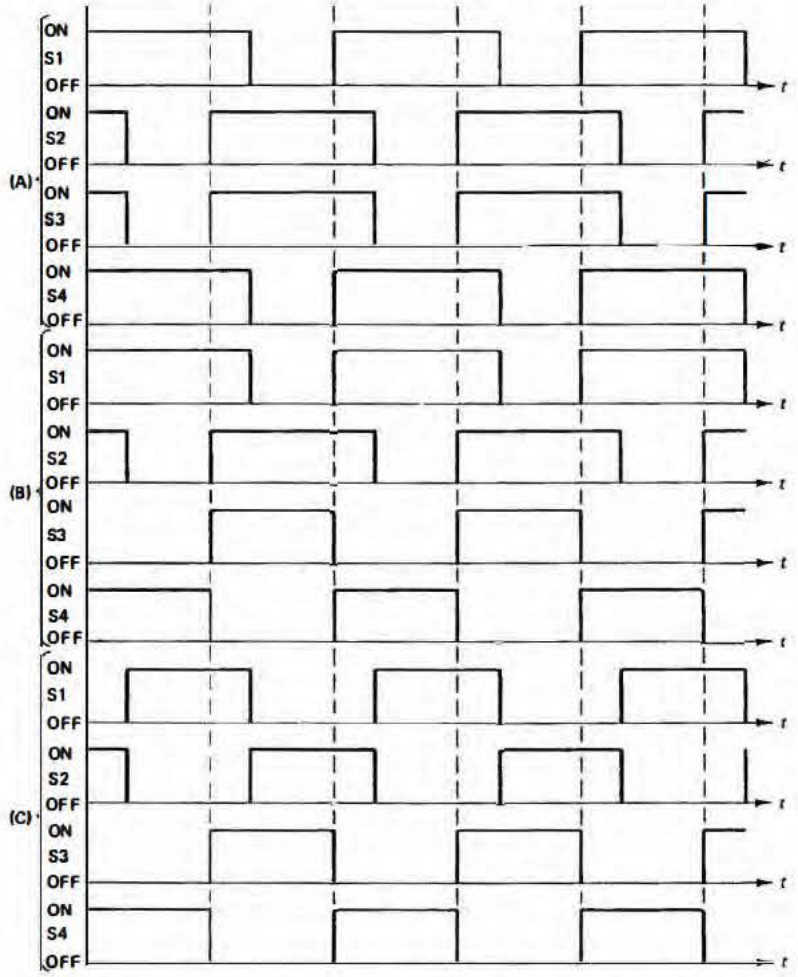
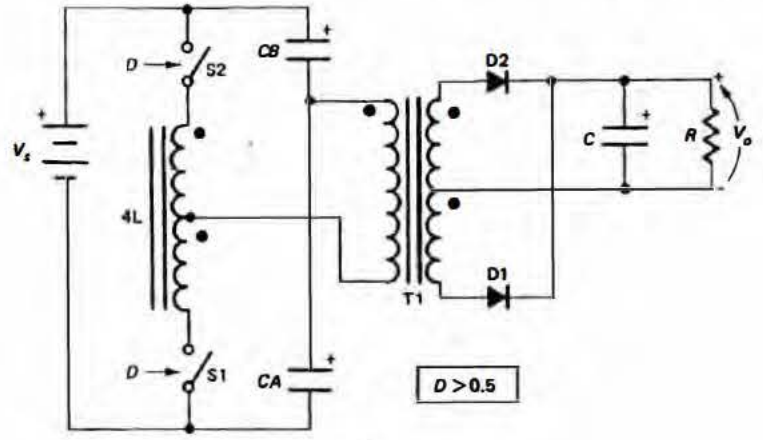


Fig. 6.11. Possible switch conduction sequences in the overlapping conduction boost converter.

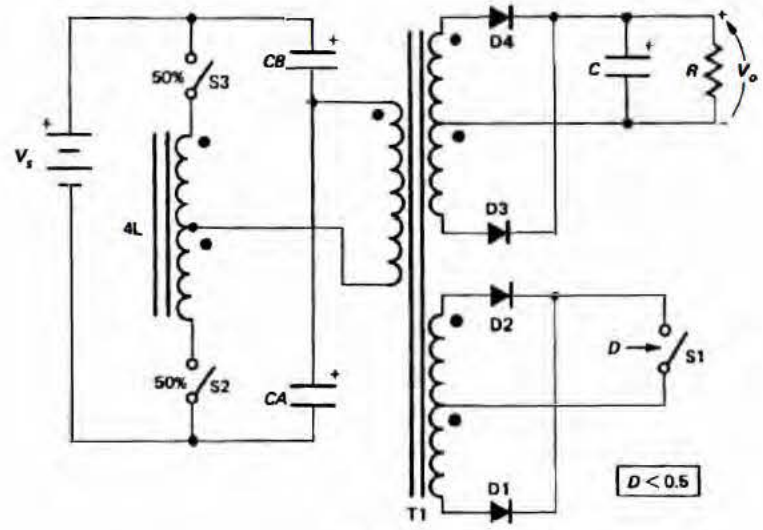
and once by S2 and S4. Complete DC isolation of drive power for the four SPC switches can be achieved by using two transformers, each with two output windings. These drive transformers handle only low-power symmetrical signals, and are usually very small in physical size.

As shown by the examples in Fig. 6.12, half-bridge boost converters can be

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(A)



(B)

Fig. 6.12. Half-bridge boost-derived converter variations.

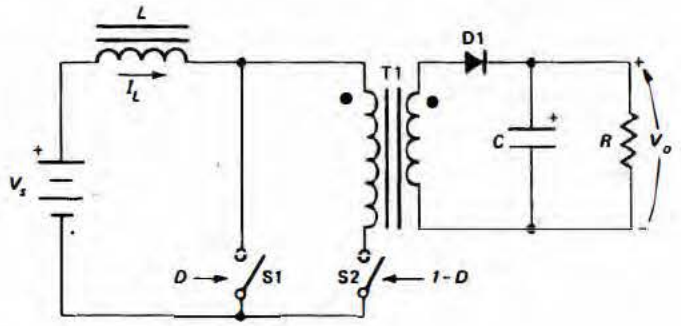
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readily derived, but it is necessary that the input inductor L be center-tapped and inserted between the SPC switches.

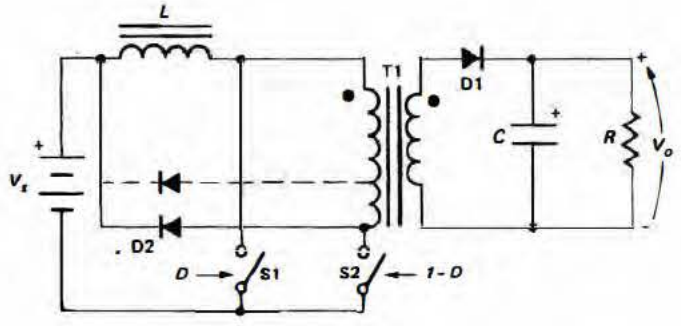
6.3 SINGLE-ENDED DC TRANSFORMERS WITHIN BOOST CONVERTERS

A single-ended DC-DC transformer can be combined with a basic boost SPC. Such combinations, however, result in converters that require *two* primary switch elements, rather than only one as was the case for buck-derived single-ended transformer designs.

The boost-equivalent of the buck-derived forward converter is shown in Fig. 6.13A. At the beginning of a switching cycle, S1 is ON and S2 is OFF. Inductor



(A)



(B)

Fig. 6.13. A single-ended boost-derived converter.

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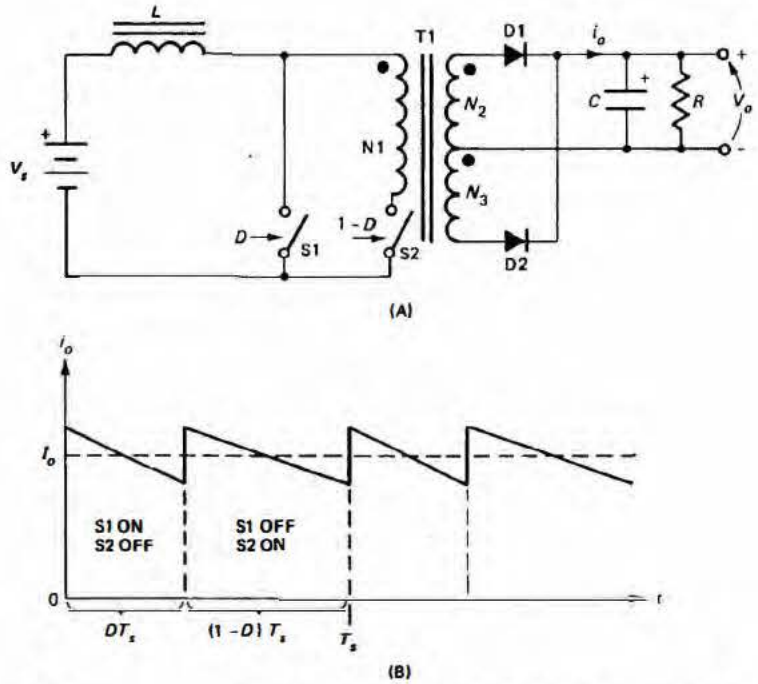


Fig. 6.14. A method for reducing the output current ripple in the single-ended boost converter.

current therefore flows through S1. With S2 open, energy to sustain the output voltage load comes from the filter capacitor C. When S1 turns OFF and switch S2 closes, it now allows the inductor current to flow through the primary of T1 and to deliver its stored energy to the output of the converter. As long as inductor current is flowing in a continuous fashion, one switch must always be closed for proper converter operation. A simple transformer core reset scheme for the converter of Fig. 6.13A is shown in Fig. 6.13B. Of course, other reset schemes discussed in Chapter 4 could also be used. The current of the inductor could also be used to reset the core of T1 by adding a small tertiary winding in series with switch S1.

Another interesting SPC circuit can be derived from the single-ended boost converter of Fig. 6.13A. Normally, the magnetizing inductance of T1 is made as large as possible to minimize the amount of energy stored in its core. However, if this magnetizing inductance is deliberately made relatively small and the stored energy of the core discharged into the secondary (as shown in Fig. 6.14A),

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then it is possible to greatly reduce the converter's output ripple current by judicious choice of the values of the inductor and T1's magnetizing inductance. The resultant output current waveform is illustrated in Fig. 6.14B. As shown, discontinuities in the waveform still exist at switching points but can be made smaller by optimizing the value of the magnetization inductance of T1. Another variable for controlling output ripple current magnitude is the turns ratios between N2 and N3.

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7. Combinations of Converters

Up to this point, we have been discussing the two basic DC-DC converters and combinations of each with a single DC transformer. Despite these restrictions, many unusual and different SPC circuits were derived as well as some converter topologies that are in popular use today.

However, there are many useful SPC circuits that are combinations of more than one elementary converter. Some of the more complex SPCs also include a DC transformer or even a simple AC transformer to further enhance their utility. As we will see, the number of SPC circuit variations is limited only by the imagination and persistence of the designer, although the point of vanishing returns from increased circuit complexity inevitably puts a practical boundary on innovation.

The SPC building blocks available at this point in the discussion are the basic buck and boost converters, AC and DC transformers, plus the many buck and boost-derived circuits developed in Chapters 5 and 6. For simplicity in the discussions to follow, we will attempt to treat each of the combinational as interconnections of separate two-port electrical networks. A few of the interconnection possibilities of two-port networks are shown in Fig. 7.1. Obviously, a multi-output SPC or DC transformer system could be viewed as a multiport network. However, we will find plenty of complexity in the circuits of this chapter without including such viewpoints.

7.1 CASCADING IDENTICAL CONVERTERS

Perhaps the simplest combination of SPC's would be the cascade connection of identical converter topologies, such as the two buck converters shown in Fig. 7.2A. For this SPC operating in the continuous mode, its ideal overall voltage gain (M) will be:

$$M = D_a \cdot D_b. \tag{7.1}$$

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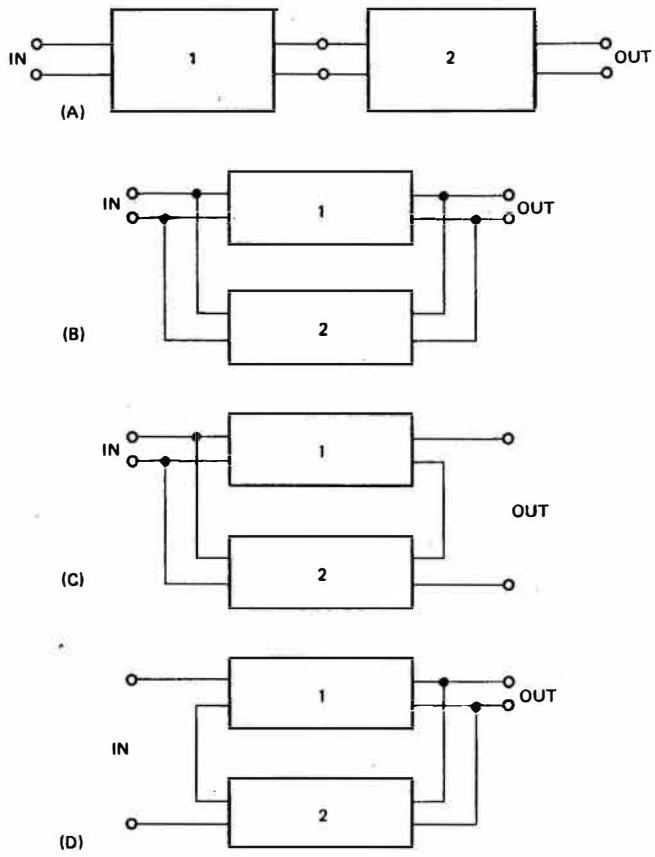


Fig. 7.1. Typical connections of two-port networks.

In some applications, D_a (or D_b) is held at a fixed value, while the other switch is varied to maintain output voltage regulation. In many cases, for simplicity of drive circuitry, duty cycle control of S1 and S2 are generated from a single source. In such cases, D_a will be equal to D_b so that

$$D = \sqrt{M}. \tag{7.2}$$

Remember that for a single-stage buck SPC:

$$D = M. \tag{7.3}$$

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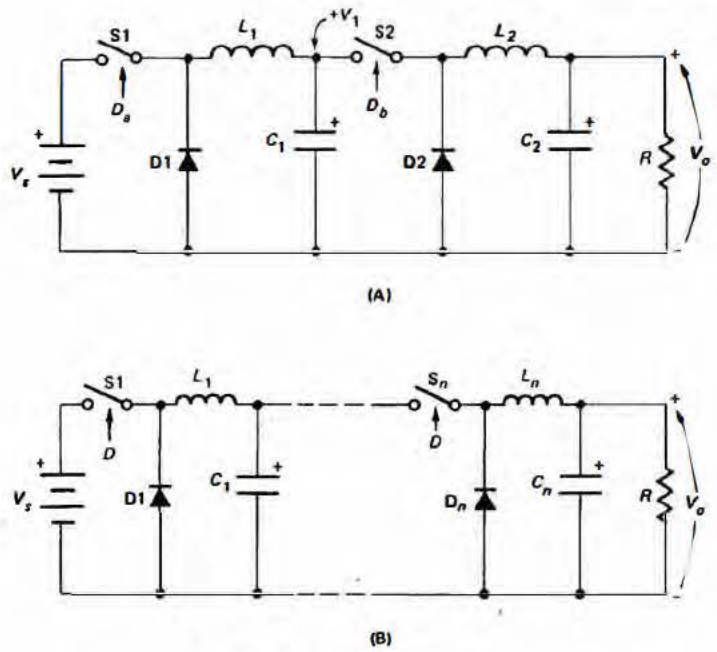


Fig. 7.2. Cascaded buck converters.

Since

$$M \leqslant 1 \tag{7.4}$$

the switch duty cycle for two buck stages in tandem will *always* be greater than that of a single stage for a given value of M. Several benefits become evident– first, since the average source current (I_s) through S1 must remain the same (same V_s and input power levels), then the peak current (I_b) through S1 must go down as D is increased. For example, if $M = 10$, then $I_b = 10I_s$ for a single-stage buck converter operating in a continuous mode. However, for a comparable two-stage buck system, $I_b = \sqrt{10}I_s$. This implies that peak current levels of S1 will be much lower in the two-stage case and, therefore, it can control more power than an equivalent single-stage counterpart. Switch S1 and diode D1 will still see OFF voltage stresses equal to V_s, but S2 and D2 only have to sustain an OFF voltage (V_1) given by:

$$V_1 = \sqrt{V_o \cdot V_s} \tag{7.5}$$

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for $D_a = D_b$. Since V_1 is always less than V_s in value, the OFF voltage capabilities of S2 and D2 are reduced accordingly.

If M is small (in the range of 0.4 or less), there is no real advantage in cascading the two converters. It would be better to simply implement the function of S1 with paralleled switch components for higher current-handling capability and remove the second low-pass filter network (L_2, C_2). On the other hand, if M is large, then the cascade connection of two buck SPCs should be considered for component stress reduction reasons.

This cascade principle can be extended to any number (n) of buck SPCs as shown in Fig. 7.2B. The ideal voltage gain of a complete system is then:

$$M = D^n \tag{7.6}$$

assuming all switches are operated at an identical duty cycle, D. From a practical standpoint, it is questionable that more than two buck stages in cascade offer any advantages. Nevertheless, cascade arrangement of many stages is still a viable concept.

For a number (n) of cascaded boost SPCs operating in the continuous mode, at same duty cycles of conduction, ideal voltage gain is given by

$$M = \frac{1}{(1 - D)^n}. \tag{7.7}$$

7.2 CASCADING DISSIMILAR CONVERTERS

Several useful and popular SPC circuits can be obtained from cascade combinations of buck and boost converters. For example, one can precede a boost converter with a buck converter as shown in Fig. 7.3A. This circuit can be greatly simplified by a bit of topology manipulation as illustrated in Figs. 7.3 and 7.4.

First, in Fig. 7.3B, we presume that S1 and S2 are synchronized and have identical duty cycles. Therefore, the functions of S1, S2, D1, and D2 can be replaced with an equivalent DPDT switch as indicated. Notice that capacitor C1 has been deliberately omitted in Fig. 7.3B. Up to this point in our discussion, the buck converter has always been shown with an output filter capacitor but, strictly speaking, it is not required. In theory, the inductor of a buck SPC can be made arbitrarily large so as to reduce load ripple current amplitudes without the need for additional capacitive filtering. In actual practice, however, it is much easier to add an output filter capacitor to keep the physical size of the inductor small. The output capacitor of the boost converter cannot be eliminated because its output current is always pulsating, regardless of how large its inductor is made. In the example of Fig. 7.3B, considerable ripple in L1 can be tolerated since L2 and C2 provide a second stage of low-pass filtering.

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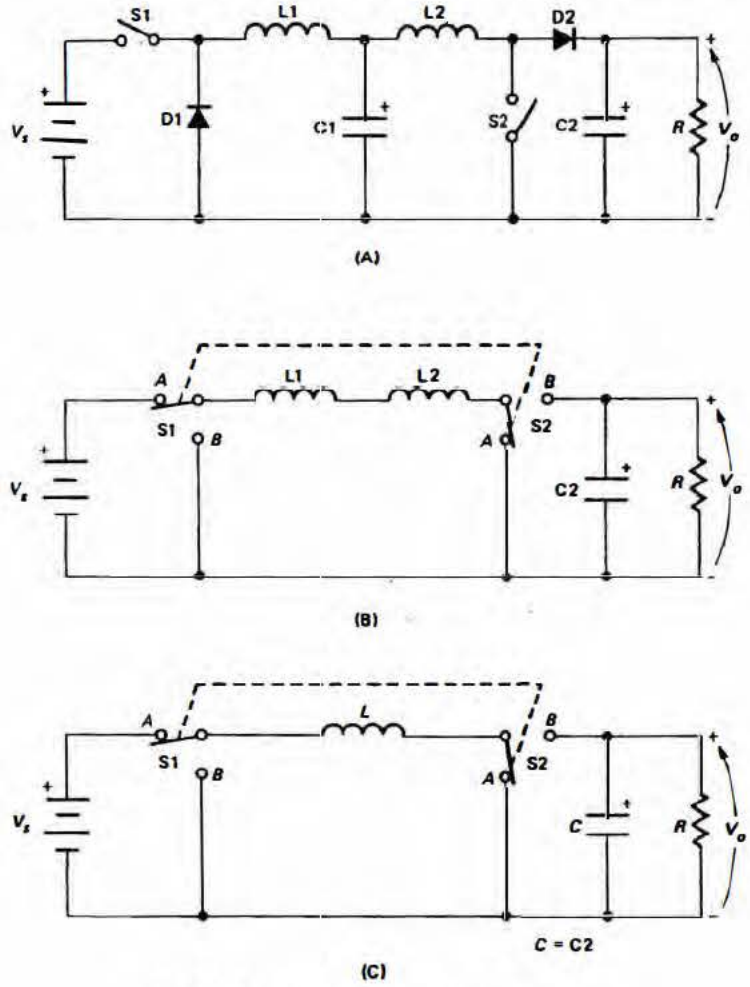


Fig. 7.3. Evolution of the buck-boost converter (I).

Having eliminated C1, inductors L1 and L2 can now be combined into a single element, as shown in Fig. 7.3C, since they are series-connected in one branch of the topology.

If we are willing to accept a polarity inversion of the output voltage, the circuit can be further simplified by rearrangement of the DPST switch/inductor network of Fig. 7.3C to that shown in Fig. 7.4A. A practical realization for this

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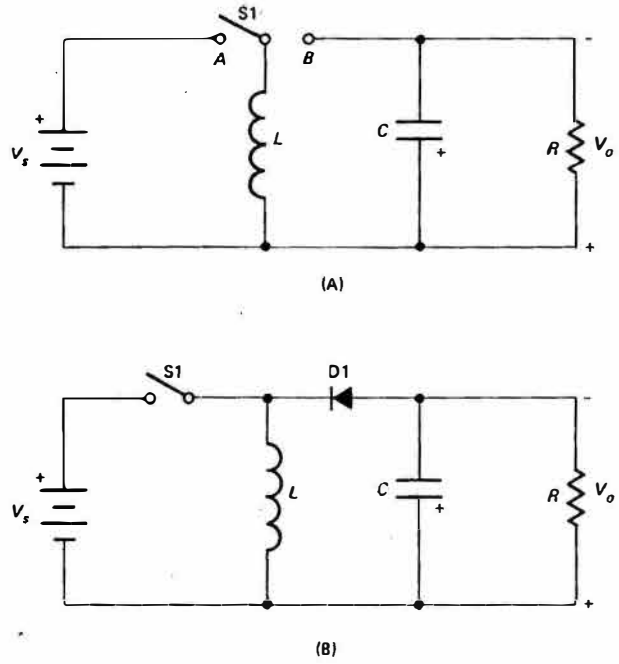


Fig. 7.4. Evolution of the buck-boost converter (II).

latter circuit is given in Fig. 7.4B and is commonly called a *buck-boost converter*. The buck-boost converter uses the same number of circuit components as does a buck or boost SPC and has an ideal voltage gain equal to $D/(1 - D)$. Therefore it is possible to have output voltage magnitudes that are either greater or less than that of the converter's input voltage.

However, there is a price to be paid for this versatility in voltage gain. The buck-boost SPC has the input properties of the buck converter and the output properties of the boost converter. Both the input and output currents of this converter are pulsating, which increases the sizes of additional input and output filters used for EMI reduction. In addition, its switch and diode currents are greater (for a given power level and voltage gain) than those of the basic buck or boost converters. For these reasons, the buck-boost SPC is rarely used in high DC power processing applications.

The buck-boost converter is considered by many SPC design engineers to be an elementary SPC form. As we have seen, this SPC uses the same number of circuit components as do buck or boost converters, and certainly is a viable DC conversion scheme. Also, it is possible to treat the network formed by S1, D1,

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and L in Fig. 7.4A as an essential SPC feature and, by processes of rotation and mirror-imaging, used to logically evolve buck or boost SPC topologies.

As we have seen, it is possible by a simple manipulation to derive the buck-boost converter topology from the cascade connection of the two elementary converters. The derivation of the buck-boost SPC small-signal model given in Chapter 10 also supports this view. For these reasons, we have chosen here to classify the buck-boost converter as a special combination of buck and boost SPCs, rather than an elementary converter unto itself. Since this assumption has proven to be self-consistent, we have retained it throughout the discussions of this text, but certainly the point of origin of this converter topology is an arguable one.

When multiple outputs and/or DC isolation from input to output are desired in a buck-boost converter, it is not necessary to incorporate a DC transformer, as we will see. Consider the buck-boost circuit of Fig. 7.5A, where the inductor L now has two identical windings in parallel. This winding addition does not alter the basic converter operation. Next, the links connecting the two inductor windings are removed, as shown in Fig. 7.5A. Again, circuit operation remains the same except that DC isolation between the input and the output has been achieved. The final step in this process is shown in Fig. 7.5C, where additional secondary windings have been introduced in the inductor assembly with arbitrary turns ratios relative to the inductor "primary." This transformer-isolated multiple-output form of the buck-boost SPC is called the *flyback converter* and is probably the most popular circuit in use today for output power levels below 50 W. Its primary advantage is simplicity, particularly in that only one magnetic component is needed, even when input-to-output DC isolation and/or multiple outputs are required from the converter. The primary difficulty associated with this SPC is the design of inductor L, which now assumes the roles of both an energy-storage device and a transformer element. Its design becomes even more difficult when multiple outputs with good cross regulation are required. Successful flyback SPC design examples with as many as 25 isolated outputs do exist, but their magnetics designs were very complicated.

Besides the pulsating input and output current characteristic and the high switch currents mentioned earlier, the control-to-output small-signal transfer function of the buck-boost has a *right* half-plane zero, as we will see in Chapter 10. The presence of this troublesome zero should come as no surprise since one of the elementary constituents of the buck-boost converter has a similar control-to-output transfer function.

When a buck SPC is preceded by a boost SPC, as shown in Fig. 7.6A, quite a different, and in many ways a more useful converter can be derived in much the same manner as was followed to evolve the buck-boost and flyback SPCs. In Fig. 7.6B, the two switch-and-diode sets are replaced by a single DPDT switch. In this case, C1 cannot be omitted since it is required for energy storage. As was

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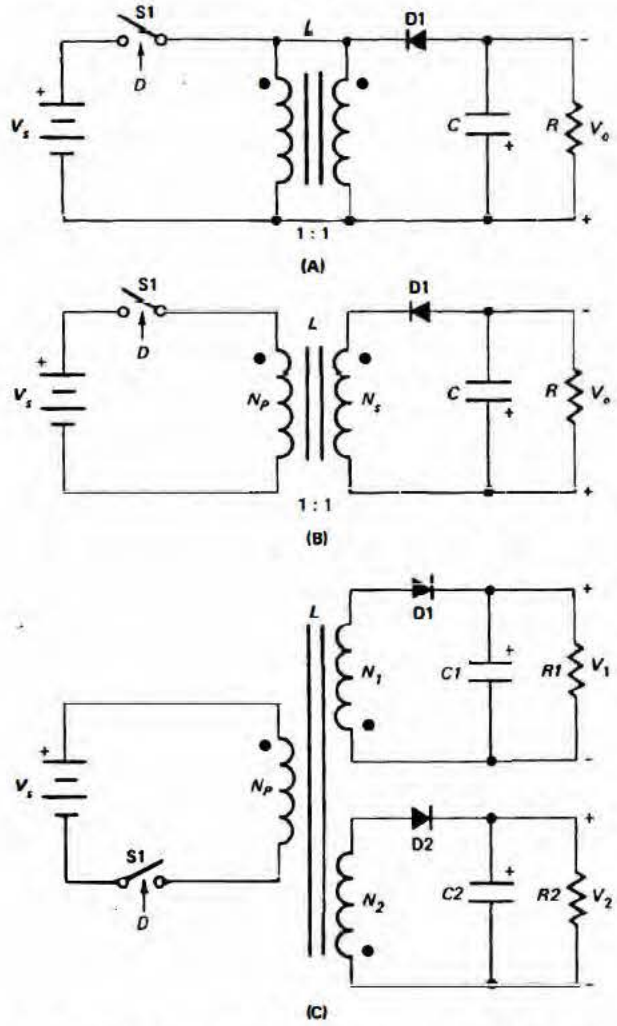


Fig. 7.5. Derivation of the flyback converter from the buck-boost converter.

the case for the buck-boost, if a polarity inversion of output voltage is permitted, the circuit can be further simplified. As indicated in Fig. 7.6C, the DPDT switch and shunt capacitor network can be replaced by a SPDT switch and a series capacitor. A practical realization of this new circuit is shown in Fig. 7.6D. This

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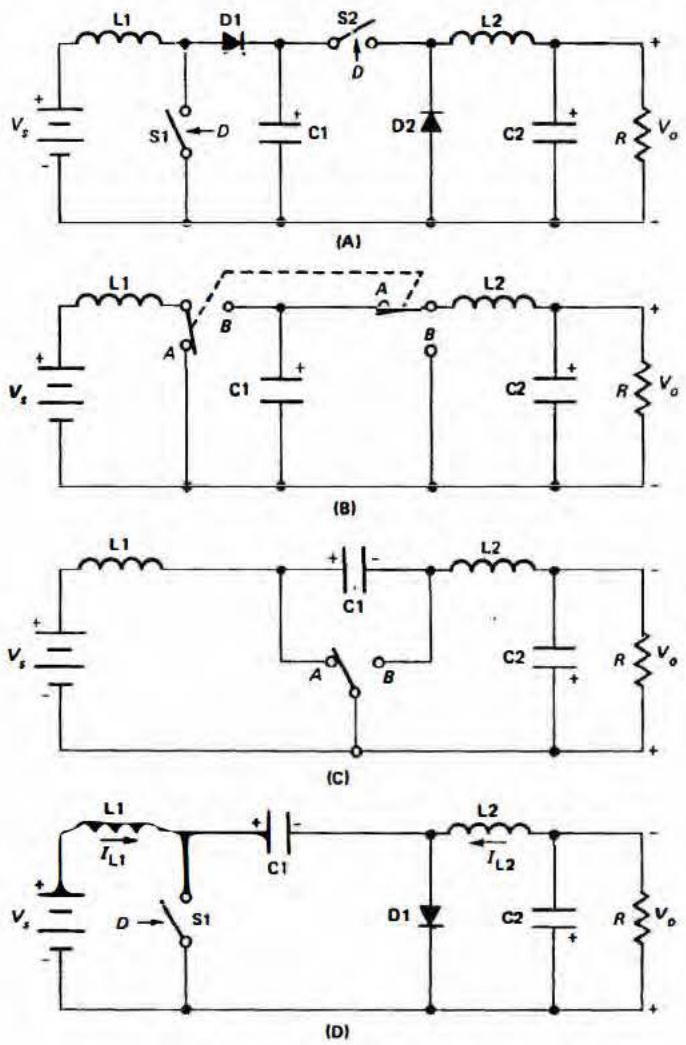


Fig. 7.6. Evolution of the Cuk converter.

SPC is known as the Ćuk (pronounced "Chook") converter after its inventor, Dr. Slobodan Ćuk of the California Institute of Technology [Ref. 6].

From a historical point of view, it is interesting to note that many popular SPC circuits were conceived more or less at random, and often the same SPC

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topology was invented by many different people at different points in time. SPC invention processes historically have been anything but orderly. The Ćuk converter is very much an exception to this development tradition. The topology was the result of a deliberate and logical effort by Dr. Ćuk to synthesize an SPC circuit with as many desirable conversion properties as possible. To the best of our present knowledge, *no* other independent invention of the basic Ćuk SPC topology has yet been claimed, although patents held by other power electronics engineers do exist which add further enhancements to the Ćuk topology.

Looking at the basic Ćuk SPC of Fig. 7.6D, we see that it requires only a ***single*** switch and a ***single*** commutation diode, with C1 serving as the main energy transfer link between input and output. When operating in the continuous mode, the input ***and*** the output currents of the Ćuk SPC are non-pulsating and associated AC ripple currents can be made arbitrarily small by increasing the values of inductors L1 and L2. This particular converter property often eliminates the need for additional input/output EMI filters in an application. Recall that both the boost and buck SPCs frequently require an additional output and input low-pass filter, as shown in Fig. 7.7A and 7.7B, respectively, to minimize conducted noise from SPC switching actions. Comparing the number of circuit components in the SPCs of Figs. 7.7A and 7.7B to that of the Ćuk converter in Fig. 7.7C, one finds that all three use the same number.

The Ćuk SPC, like the buck-boost converter, can provide an output voltage magnitude either above or below the value of its source voltage, depending on the duty cycle of S1 in Fig. 7.7C. Ideally the relationship between input and output voltages is simply $D/(1 - D)$. Switch, diode, and capacitor currents are comparable in the Ćuk converter to those of their counterparts in the buck-boost SPC operating with the same voltage transformation ratio and input power level. If input and output EMI filters are added to the buck-boost converter, the resultant conversion system becomes more complex than the Ćuk approach.

Like the cascaded buck SPC of Fig. 7.2A, the basic Ćuk converter has two inductors. It is readily possible to operate the converter so that one inductor is operating in the continuous current mode and the other in a discontinuous mode. This particular possibility is usually avoided in practice, since it leads to rather peculiar power conversion transfer characteristics!

DC isolation and multiple outputs can be added to a basic Ćuk converter by insertion of an AC transformer within its topology, as shown in Fig. 7.8. Here, the energy transfer capacitor (C1 of Fig. 7.7C) is divided into two series capacitors, C1A and C1B, whose total series capacitance value is equal to that of C1. A large inductor, such as that represented by the magnetization inductance of a transformer's primary, can be placed from the junction of C1A and C1B to the return point of source voltage *without* significantly affecting the converter operation. With the addition of secondary windings on this "inductor" along with associated output filter circuitry on each winding, the multi-output transformer-

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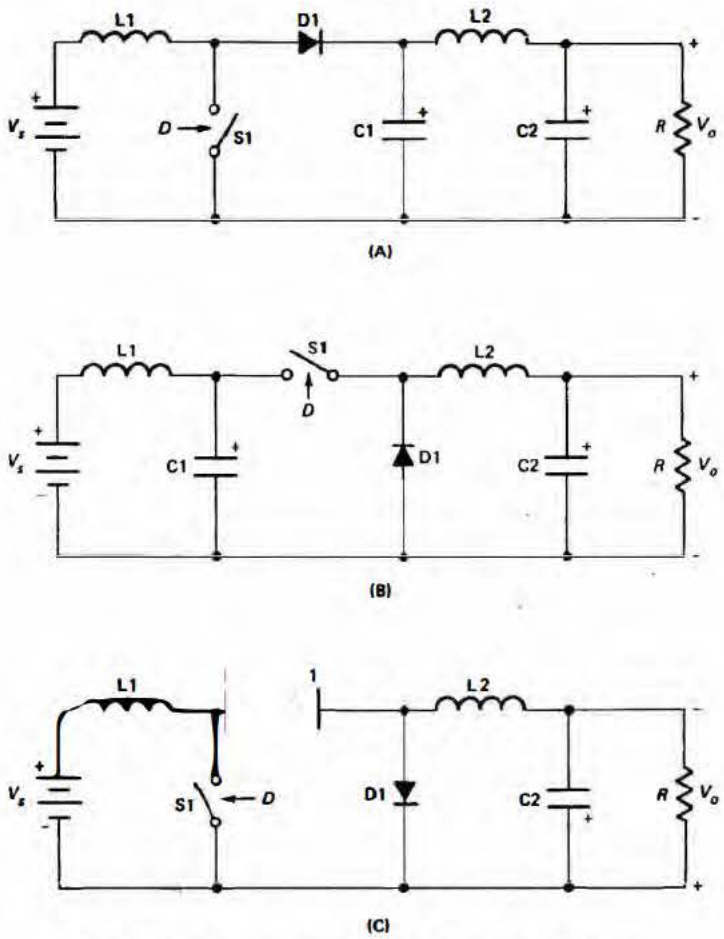


Fig. 7.7. Circuit comparisons of the boost, buck, and Ćuk converters.

isolated Ćuk converter results, as illustrated in Fig. 7.8B for a two-output case. Note that T1 does not store energy as part of the converter action. Because of the presence of capacitors in series with each winding, no DC can appear across the transformer windings. This allows full utilization of core flux capability. For these reasons, T1 is much easier to design, has better cross-regulation properties between outputs, and is usually smaller in physical size than the transformer of a flyback converter.

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