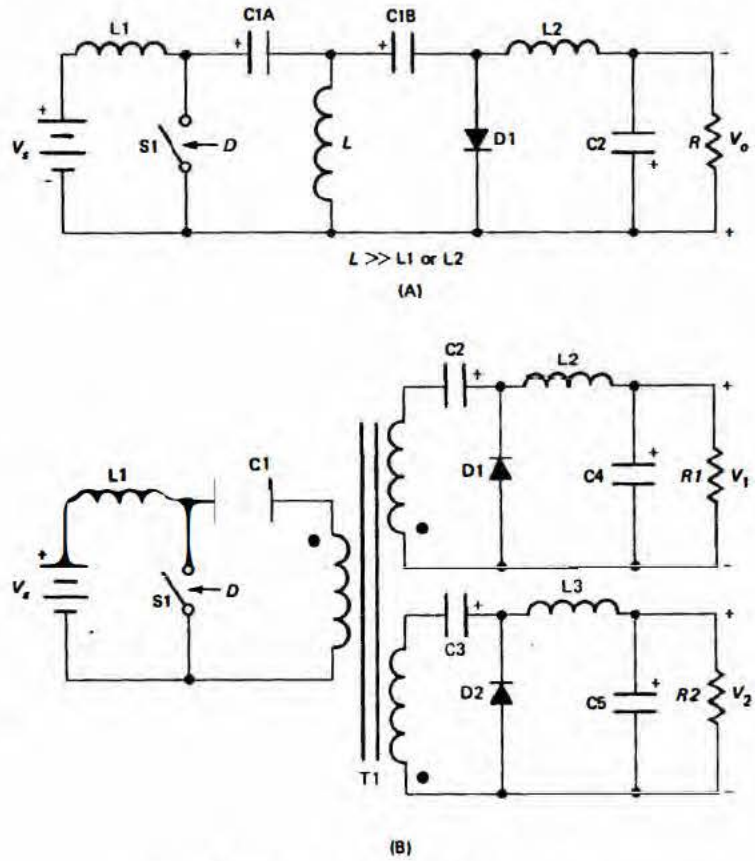


Fig. 7.8. The transformer isolated Ćuk converter.

Another unique enhancement can be added to the Cuk converter, if desired. It is possible to have mutual inductive coupling (k) between L1 and L2, as shown in Fig. 7.9A. This can be achieved by placing L1 and L2 on a *common* core and controlling the value of k to reduce either input or output current ripple magnitudes. In fact, for properly selected values of coupling and turns ratios between the two inductor windings, input *or* output current ripple can actually be reduced to *zero*! This unusual effect is a function of the value of leakage inductances between the windings on L. However, in a practical sense, it is very difficult to build multi-winding inductances with closely controlled mutual-coupling properties, especially if the leakage inductances must be quite small.

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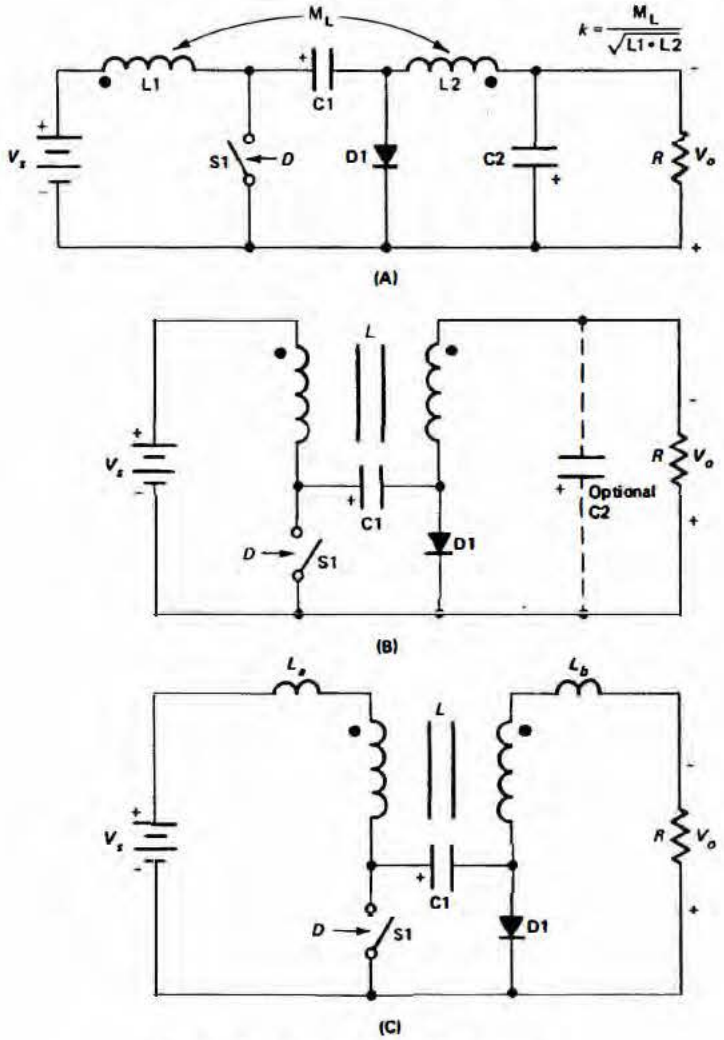


Fig. 7.9. The coupled inductor Ćuk converter.

So, as a practical expedient, L is usually built with tight coupling ($k \approx 1$) between windings and a small trimming inductor added on either the primary or secondary for current ripple reduction, as shown in Fig. 7.9C.

An interesting single-inductor version of the Ćuk converter is shown in Fig.

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7.10B. In Fig. 7.10A, L has been moved from its original position above S1, D1, and C1 in Fig. 7.9B to one below these circuit elements. By making the turns ratio of the inductor in Fig. 7.10A one-to-one it can be reduced to a single-winding inductor as shown in Fig. 7.10C. This later circuit topology is simply a buck-boost circuit with its energy storage capacitor C1 connected directly to the positive side of the input source rather than to the return side.

The Ćuk converter has a multitude of variations, a few of which are shown in Fig. 7.11. Some of these unusual variations allow *both* input and output ripple current magnitudes to be made zero *simultaneously* using the magnetic coupling methods discussed earlier.

The process of cascading buck and boost SPCs can be carried another step farther by cascading a boost and a buck-boost converter, or a buck-boost converter, or a buck-boost converter and a buck converter. The results of performing the same network simplifications developed earlier on these combinations are shown in Figs. 7.12 and 7.13, respectively.

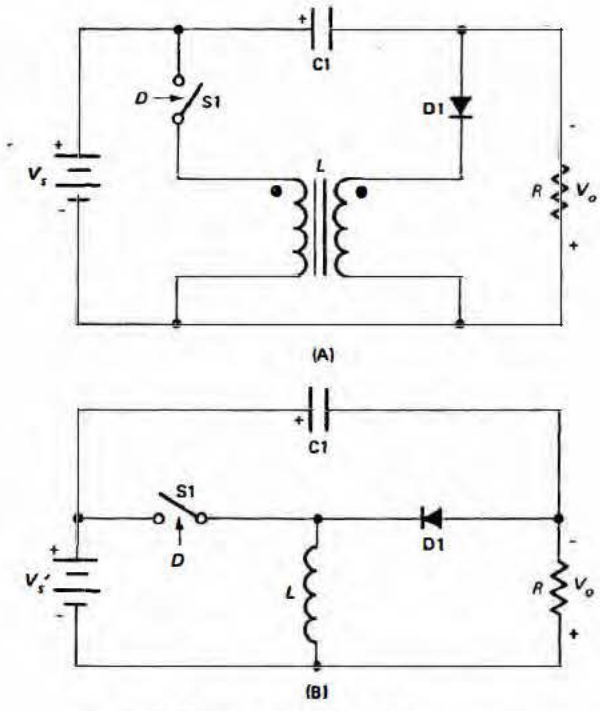
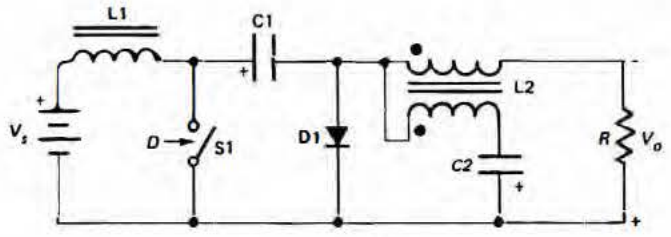
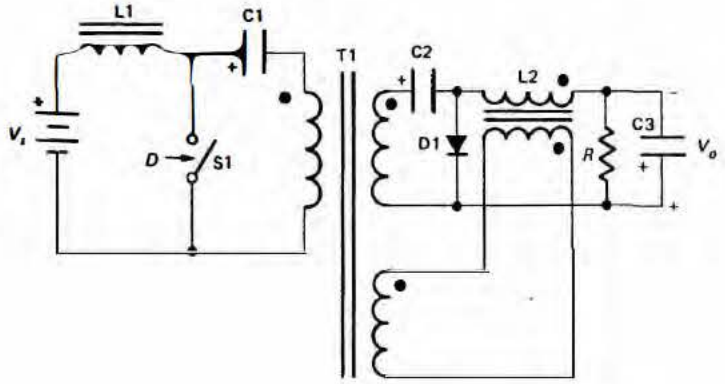


Fig. 7.10. The single inductor Ćuk converter.

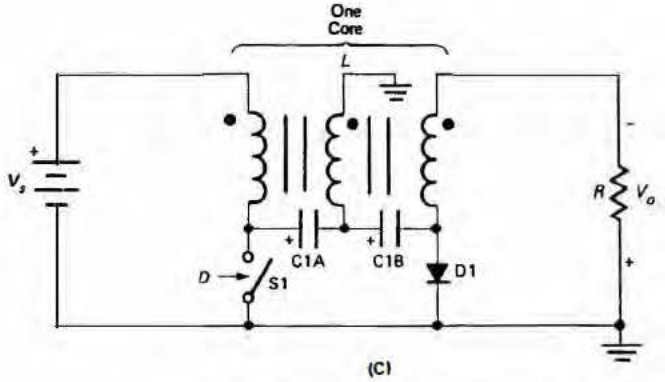
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(A)



(B)



(C)

Fig. 7.11. Ćuk converter circuit variations.

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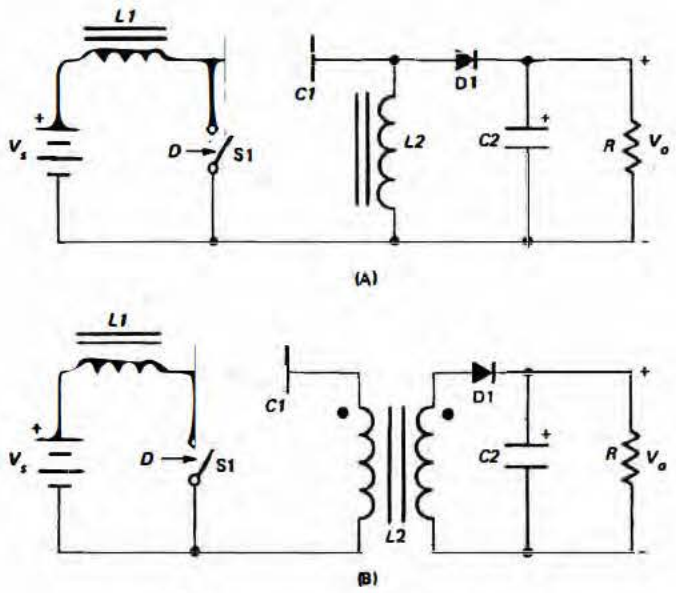


Fig. 7.12. Cascaded boost and buck-boost converters.

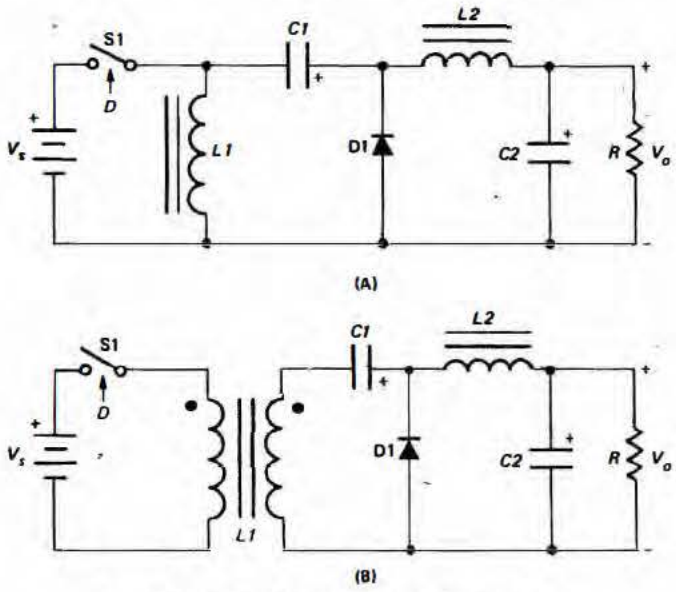


Fig. 7.13. Cascaded buck-boost and buck converters.

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Even though we have essentially cascaded three converters in the last examples, the final circuit form of the simplified SPCs contain only a *single* switch and a *single* commutating diode. Based on these experiences, it appears that any SPC system formed by a number of cascaded, alternating buck and boost converters can be reduced to a topology consisting of one switch and one diode. From a practical standpoint, the need for more than two stages in cascade is rare.

7.3 PARALLELING CONVERTERS

There are a number of reasons for paralleling two or more converters, the most common being the need to provide higher output power levels. Given the practical limitations of circuit components (in particular, semiconductor switches), there will always be a maximum power output for any given converter design. Of course, it is possible to parallel multiple switches and commutating diodes to extend the output power capabilities of a single converter. However, this process usually involves derating individual device capabilities since exact sharing of current or voltage stresses is usually not achievable in a practical sense. Achievable power output from a single SPC with paralleled circuit elements may well be less than that possible from a conversion system composed of paralleled SPCs using single circuit elements. Unfortunately, there is no simple means for deciding which conversion system design approach will be the best for a particular output power need, other than to generate a fairly detailed design of each approach and then compare the results. At the present time, SPCs with power output levels above 10 KW usually use two or more converters operating in a parallel fashion.

Another reason for paralleling converters is higher system reliability as a result of operational redundancy. For example, if three converters are paralleled, any two of which can supply the full load power, the probability of two failures occuring in two of them that would disable the entire conversion system is much less than that of single failure in a conversion system composed of only one converter. Systems using five converters in which any three can fulfill full output load demands are not uncommon. Although complex in circuitry, very high functional reliability can be achieved by well-designed paralleled SPCs in a high power application.

Converters are often paralleled to increase the frequency and lower the magnitude of the input and/or output current pulsations. Potentially, this allows a reduction in the size and the weight of input and/or output EMI filter networks. An example of ripple current reduction by paralleling is shown in Fig. 7.14. Here, the switches (S1 through S3) of three paralleled flyback converters are operated sequentially, one-third of a complete switching cycle apart from one another. This timing sequence results in input and output current ripple frequencies three times that of the overall converter switching frequency. Another

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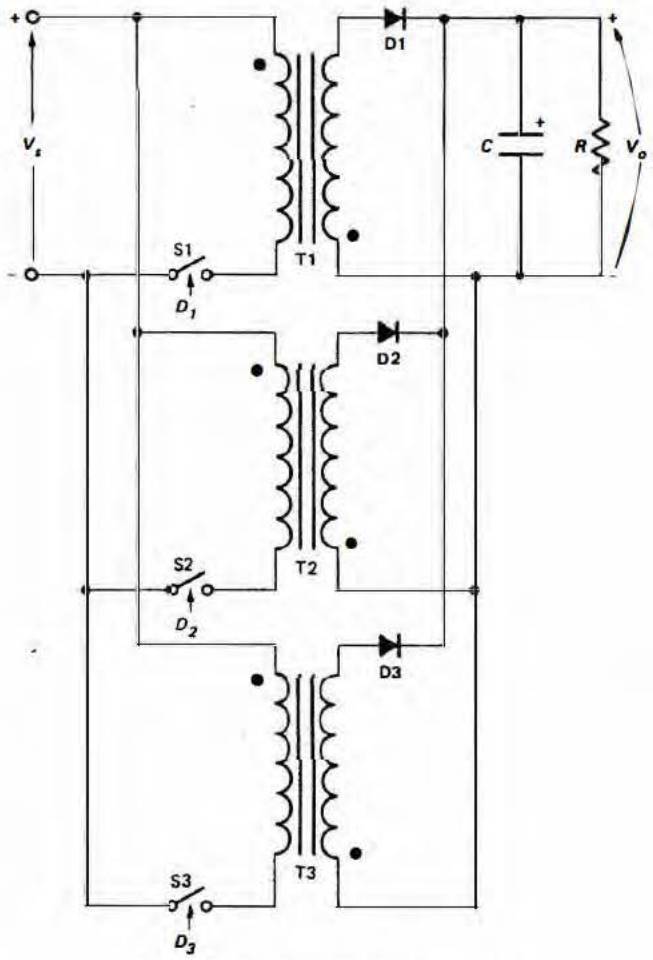


Fig. 7.14. Phased parallel flyback converters.

benefit of sequenced switching is an increase in the duty cycle of input/output current waveforms and a decrease in their peak currents. For example, in Fig. 7.14, for $D_1 = D_2 = D_3 = 0.3$, the input current duty cycle will be 0.9 with output current duty cycle unity, since the output current pulses from each converter will overlap. This overlap results in a nearly continuous output current waveform. Also, the peak value of the input current will be one-third that of a single flyback converter of comparable output power level.

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Production power supplies using SPCs must meet the requirements of widely varying applications and still be low in cost. A common product approach adapted by many power supply companies is to design a single medium-power converter and to produce this single design in quantity. Customer requirements for higher power outputs than possible from the single converter are met by paralleling two or more of the basic designs and adding necessary auxiliary control electronics. This product design philosophy results in low nonrecurring engineering costs as well as lower recurring manufacturing expenses.

There is one problem which is common to all parallel converter schemes, namely how to share the output load demands equally among each SPC. Other than potential similarities in circuit and component impedances, there is no inherent mechanism to force current-sharing between paralleled converters. Therefore, large imbalances in load sharing can occur if several converters are simply wired in a parallel fashion. The usual solution to this problem is the use of regulatory current sensors to maintain balance in load sharing among the converters. Control schemes which compare individual switch currents against an error voltage related to total output load are viable methods to insure current sharing among SPCs.

7.4 OTHER SPC COMBINATIONS

As shown in Figs. 7.1C and D, the inputs and/or the outputs of converters can be connected in a series fashion. An example using two parallel quasi-squarewave converters with their inputs tied in parallel and their outputs connected in series is shown in Fig. 7.15.

If the required output voltage is high enough that the additional voltage drop of one more rectifier diode can be tolerated, the SPC system of Fig. 6.15 has some definite advantages. Because both transformer output windings are connected in series, their currents must be the same. This current relationship is reflected to transformer primary circuitry so as to force equal input currents in each converter. This automatic power-sharing feature eliminates any need to incorporate auxiliary electronics to insure balance. The output diodes of Fig. 7.15 will also see equal and lower reverse voltage stresses than a single SPC of this type. Here, again, equal voltage stresses on these diodes are results of the current-sharing feature mentioned earlier.

The advantages of automatic sharing of reverse diode voltages could be gained by using series multiple connections of windings on a single transformer. But, for very high output voltages on the order of 20 kV or greater, a single transformer with multiple windings for voltage-sharing can be very difficult to build. On occasions, it may be simpler to use separate transformers for each winding and increase the insulation on windings in the string that see higher voltages.

Input power sharing can be obtained by connecting the inputs of SPCs in series.

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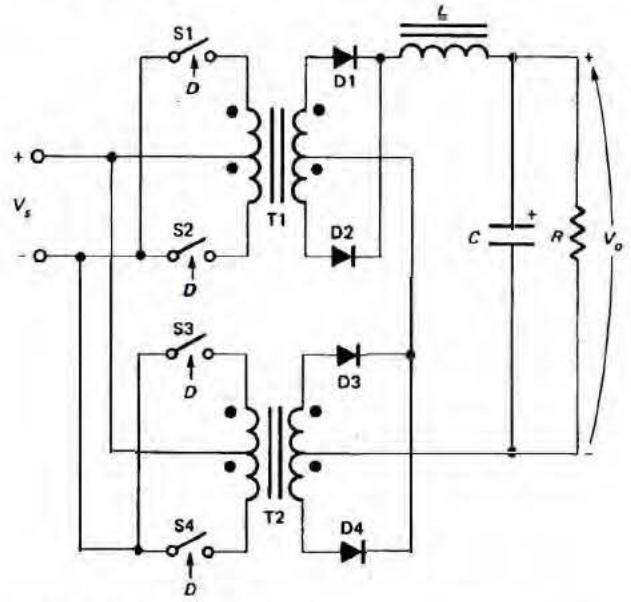


Fig. 7.15. A parallel-input, series-output converter connection.

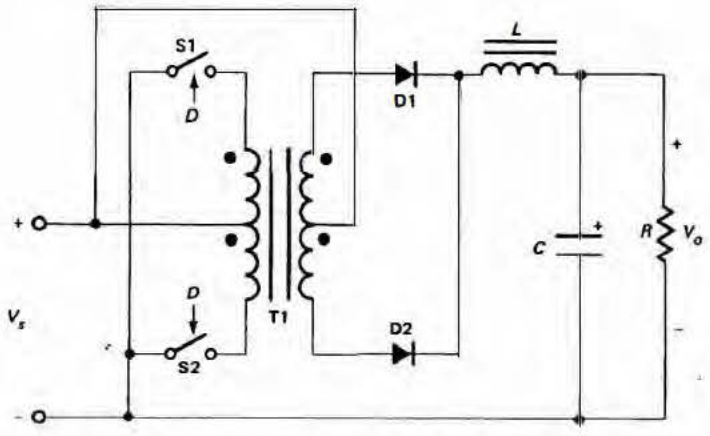


Fig. 7.16. A boost circuit using a buck converter.

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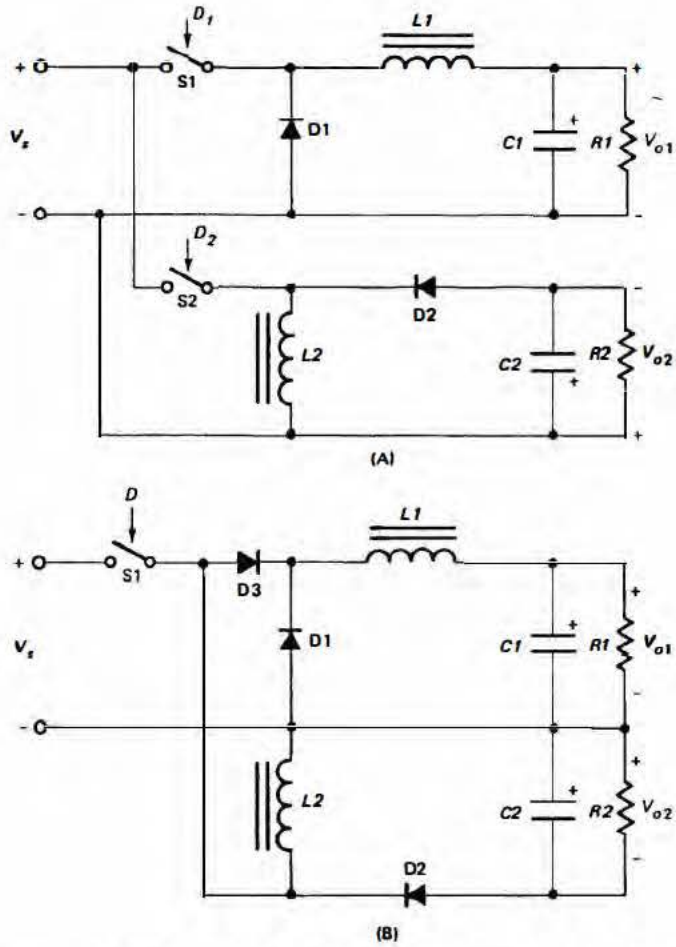


Fig. 7.17. A scheme for combining duty cycle and frequency modulation to provide two regulated outputs with one switch.

Again, automatic input current balance is provided and applications with very high input source potentials can be met with little difficulty by an input series arrangement of two or more SPCs with lower input voltage capability.

In the converter of Fig. 7.15, the voltage waveform present at the input of the output low-pass filter is the algebraic sum of the potentials of the individual

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transformer windings. Therefore, it is quite possible with this SPC to synthesize a "stepped" voltage waveform with a predetermined harmonic content. This can be accomplished by using different winding turns ratios in T1 and T2 and by phasing switch conduction duty cycles between the two converters. The number of voltage "steps" can be increased by connecting more converters in this series fashion—properly phased, of course. This phasing method can be used to reduce the size of the output low-pass filter network or to synthesize an output waveform that closely approximates a sinusoid in its shape.

Many other SPC combinations are possible and are occasionally seen in practice. For example, if the desired SPC output voltage magnitude is somewhat greater than the highest value of input voltage and DC isolation is not required, then the converter shown in Fig. 7.16 can be used. In this SPC, the input voltage is in series with the converter's output. The duty cycle controls for the primary switches are then set to allow most of the input power to the system to "bypass" the converter when the input voltage is at its maximum. As input voltage is reduced, more power is processed by the SPC. Since only a small portion of the total output power is controlled, the size and cost of the converter is reduced while improving overall efficiency of power conversion. This converter performs a voltage-boost function, even though it is a buck-derived SPC.

A very unusual SPC system is shown in Fig. 7.17, which has recently been reduced to practice. The object of the converter in Fig. 7.17A is to provide two separate, well regulated output voltages. However, one converter switch and any associated drive networks can be eliminated, as shown in Fig. 7.17B, if one converter is operated in the continuous mode and the other in the discontinuous mode. The output voltage of the converter operating in the continuous mode is determined by D and is relatively insensitive to variations in switching frequency. However, the output voltage of the converter operating in the discontinuous mode is a function of both D and switching frequency.

By using a variable duty cycle control to regulate the continuous mode output and a variable-frequency control to regulate the discontinuous mode output, simultaneous regulation of both outputs can be achieved. Note in Fig. 7.17B that a blocking diode (D3) is required to prevent the two converter modes from interacting with one another.

Obviously we can continue the combinational exercises of this chapter indefinitely. The examples presented, however, should serve to illustrate the many possibilities and utility of converter aggregation processes.

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8. Magnetic Component Tapping

Rarely do the needs of a particular power processing application require that a new SPC be created, especially since many variations are already known, as we have just seen in the last two chapters.

However, occasions do arise when available SPC topologies are almost but not quite good enough for an application and some small changes in their electrical characteristics are necessary. One of the simplest means to enhance performance is the tapping of the windings of the inductor and transformer elements. Many beneficial results can be realized and include circuit simplification, improved cross-regulation properties, lower EMI noise levels, component stress reductions and, in some special cases, the elimination of moving left half-plane poles as well as right half-plane zeros in the small-signal transfer functions. Most converter circuits are amenable to magnetic tapping for specific improvements such as those just described.

We will begin this chapter by discussing inductor-tapping methods in SPCs, followed by examining related tapping of any associated transformer windings. Finally, techniques will be covered whereby combinations of inductor and transformer tapping methods can be useful in SPCs.

8.1. INDUCTOR TAPPING

One of the simplest and most common examples of inductor tapping is shown in Fig. 8.1A, where the switch in a boost converter is connected to a tap on the winding of the inductor.

A brief comparison between important tapped and untapped boost converter electrical characteristics is given in Table 8.1. Ideal components are assumed and the converters are both operating in the continuous mode. We see that as the switch is moved to a tap on the inductor, switch OFF voltage stress is reduced, (remember V_o is always greater than V_s) which allows one to have a higher output voltage for a given switch breakdown rating. However, there is a price to pay for this improvement. The diode reverse voltage increased over that seen in the untapped converter and, as shown in Fig. 8.1 B, the input current will now have

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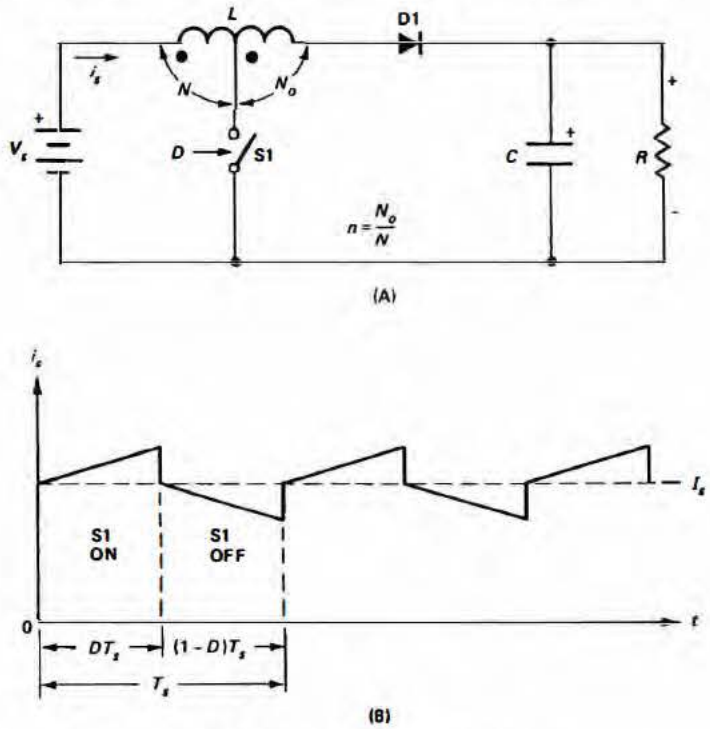


Fig. 8.1 A tapped-inductor boost converter.

discontinuities in its waveshape. Since power diodes with large reverse voltage ratings are usually much easier and cheaper to obtain than switches with high OFF voltage capabilities, a reduction in switch voltage stress by tapping can certainly be advantageous.

From Table 8.1, the value of n in the tapped inductor converter will always be greater than zero; therefore:

$$M = \frac{1 + Dn}{1 - D}. \tag{8.1}$$

In the case of the converter with an untapped inductor:

$$M = \frac{1}{1 - D}. \tag{8.2}$$

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TABLE 8.1. Boost Converter Comparisons—Continuous Mode.

Parameter	Untapped	Tapped
V_T	V_o	$(V_o + nV_s)/(n + 1)$
V_{DR}	V_o	$V_o + nV_s$
D	$(M - 1)/M$	$(M - 1)/(M + n)$

V_T = peak switch off voltage
V_{DR} = diode reverse voltage
M = ideal voltage transfer factor
n = tap factor (≥ 0)

From Eqs. (8.1) and (8.2), it is apparent that, to achieve a given value of M in both converters, a *smaller* value of D will be needed in the case of the tapped inductor SPC. This reduction factor is equal to $1/(1 + (n/M))$.

In a similar fashion, the diode of the boost SPC can be connected to a tap on its inductor as shown in Fig. 8.2A. In contrast to the previous tapping method, this movement reduces diode reverse voltage at the expense of increasing the OFF voltage of the switch. In the buck converter, inductor tapping as shown in Fig. 8.2B and C can also be used to alter the component stresses and voltage gains.

During the time intervals when all primary switches in a quasi-squarewave converter (Fig. 5.13) are OFF, the current in the primary windings will ideally be zero. However, the inductor current in the secondary must commutate through D1 (if present) and/or through diodes D2 and D3 during such intervals. To maintain ampere-turn balance in the secondary winding of T1, the commutating current must split equally in each half of this winding (assuming D1 is not present). Because there will be small differences in the conduction characteristics of diodes D2 and D3 as well as in secondary winding impedances, it is very probable that the average currents (I_1 and I_2 in Fig. 8.3A) will not be equal. As a result, an unbalanced DC bias on the transformer core will occur and can cause core saturation. This particular problem is especially severe if ungapped tape cores are used in the transformer. The addition of a third commutation diode (D1) does not guarantee that saturation will not occur, as it only provides another potentially imbalanced impedance path for a portion of the inductor current. However, if D2 and D3 are connected to a tap on the output inductor as shown in Fig. 8.3B, then both secondary diodes can be reverse-biased during the intervals when the primary switches are OFF. Diode D1 now must commutate the entire inductor current, and therefore, no DC core bias can occur as a result of imbalance in rectifier diode impedances. Reverse-bias voltage levels for D2 and D3 need only be 0.5 to 1.0 V, so that the tap ratio can be very small. There will be a discontinuity in the inductor current due to the tap. However, except for

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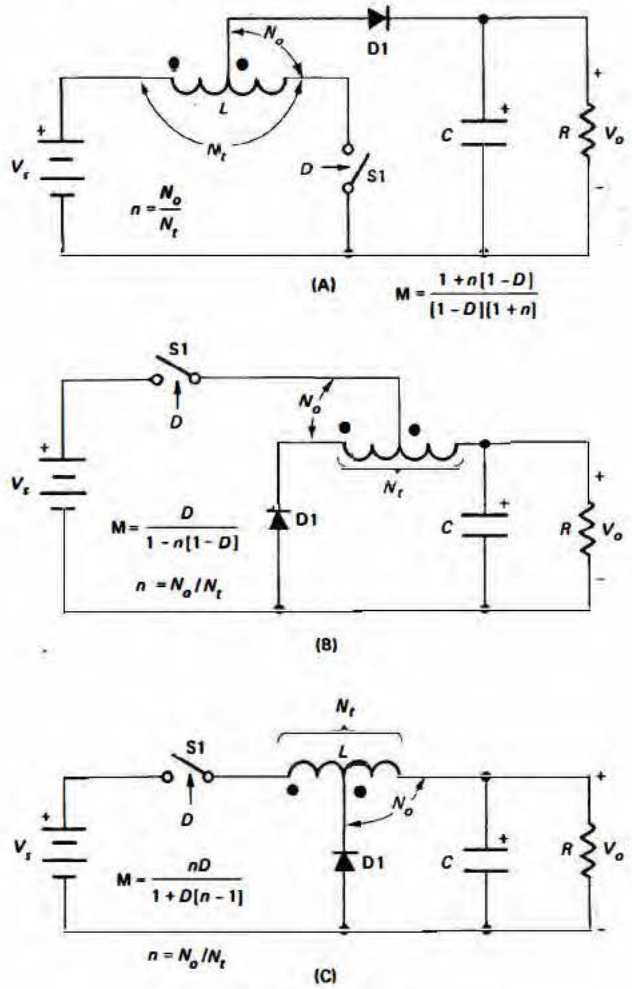


Fig. 8.2. Other tapped-inductor variations.

very low output voltages, this discontinuity will be quite small with little contribution to the rms value of the inductor current.

Although transformer core imbalance from the effects of secondary commutating currents is eliminated by the inductor-tapping technique just described, a potential problem could arise from its use. With diodes D2 and D3 in Fig. 8.3 now reverse-biased at times when the SPC's primary switch networks are OFF,

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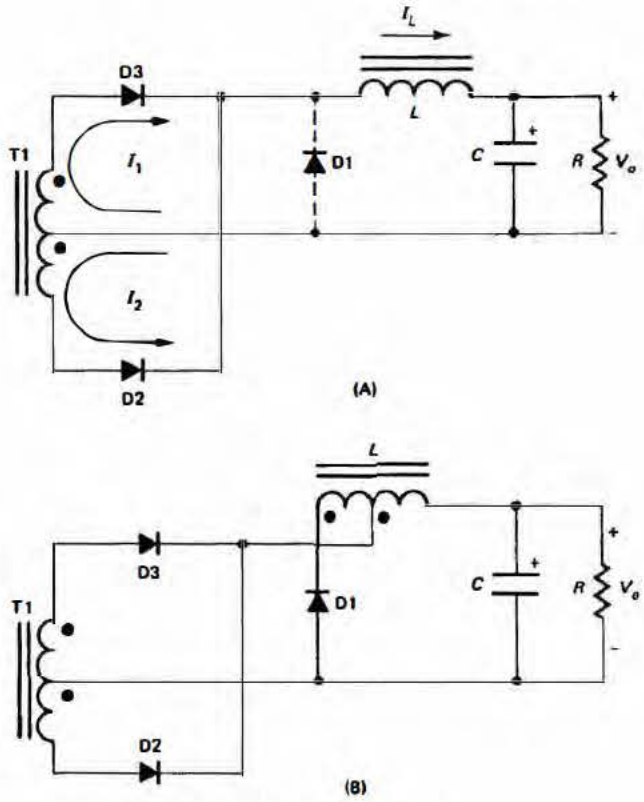


Fig. 8.3 The McLyman circuit.

magnetization energy within T1 is still present and must be eliminated. This is usually accomplished by adding dissipative energy clamps across primary switch elements. If this energy is large, overall SPC system efficiency can suffer from its loss in protective circuitry.

The concept of tapping can be extended to the use of multiple windings on the inductor. Recall that one of the disadvantages of a multi-output quasi-squarewave converter is the need for a separate energy storage inductance for each output. Also, if reasonable cross regulation between outputs is to be maintained, each output inductor must remain in the continuous mode. Both of these disadvantages can be circumvented by using a *single* multiwinding inductor assembly as shown in Fig. 8.4. Here, the turns ratios of the inductor's windings are chosen to be the same as the ratios of corresponding transformer windings.

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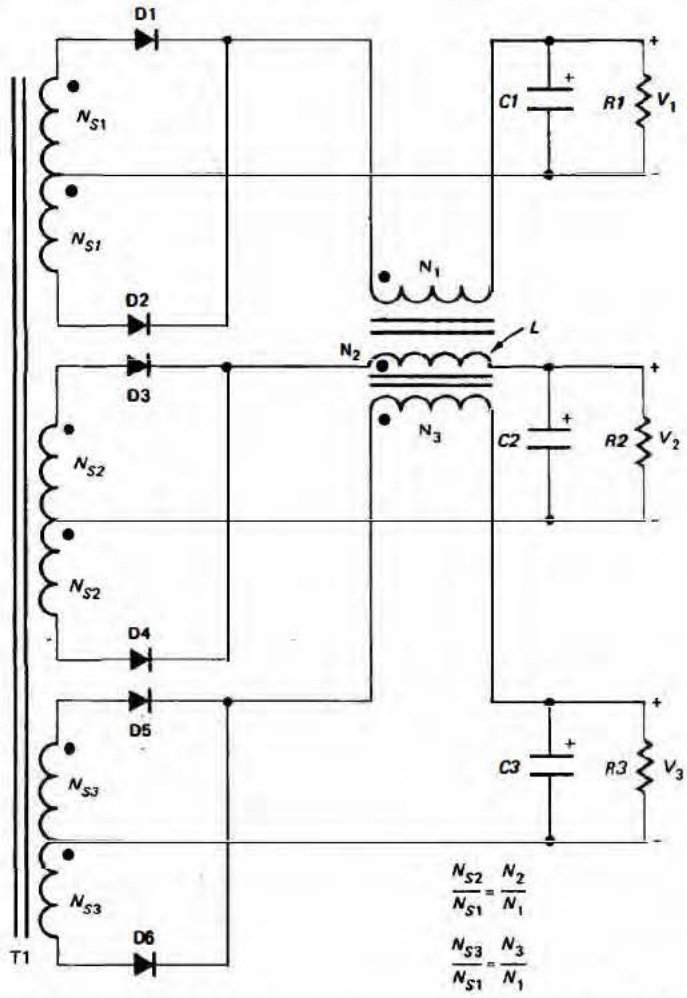


Fig. 8.4. A multiple-output quasi-squarewave converter using a single multi-winding inductor.

The advantages of this common arrangement are several. First, the inductor operating mode is determined by the sum of the ampere-turns of all its windings. Therefore, the inductor can remain in the continuous mode even if one or more output currents fall to a small value. This allows reasonable regulation of all SPC outputs regardless of load. Since each low-pass filter does not need to have a

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separate inductor, a significant reduction in number magnetics is achieved. Also, commonality of core permits less total energy to be stored in the inductor to maintain continuous conduction, thus reducing the physical size of L. Even if the total stored energy were the same, the weight of the multiwinding inductor assembly would still be less than the sum of weight of separate inductors.

The design of the multiwinding inductor is a straightforward procedure. We know that for a single output to maintain continuous conduction mode:

$$L_1 \geq \frac{R_{L1}(1 - D)\, T_s}{2} \tag{8.3}$$

where T_s is total converter switching period, R_{L1} is the minimum load expected, and D is the conduction duty cycle of the SPC primary switches. In the multi-output case, R_{L1} is the sum *total* of all output loads transformed to a single output for reference. For example, if we chose the first output of the SPC in Fig. 8.4 as our reference, then:

$$R_{L1} = \frac{V_1^2}{P_1 + P_2 + P_3} = \frac{V_1^2}{P_T} \tag{8.4}$$

where P_1 through P_3 are the individual minimum output power levels. The inductance associated with the first secondary is then calculated from Eq. (8.3) as:

$$L_1 \geq \left[\frac{V_1^2}{P_T}\right]\left[\frac{1 - D}{2}\right] T_s. \tag{8.5}$$

Allowing for the rectifier diode forward conduction voltage (V_o) and resistive voltage drop in secondary windings (V_w), the turns required for the other windings must be:

$$N_n = \left[\frac{V_n + V_{Dn} + V_{wn}}{V_1 + V_{D1} + V_{w1}}\right] N_1, \qquad n = 2, 3. \tag{8.6}$$

With L_1 and the turns ratios between windings known, the inductor design can proceed in a normal fashion. One word of caution is needed here—maintaining an equality of balance in inductor turns ratios to corresponding transformer secondary values is essential to prevent "circulating" currents in output filter networks. Severe unbalance can produce high ripple currents and potential damage to output filter capacitors.

A multiwinding or tapped inductor can also be used to alter the ripple current in a filter capacitor (C) as shown in Fig. 8.5A. The average DC voltage appearing on the capacitor will remain the same. The use of the auxiliary winding (or tap)

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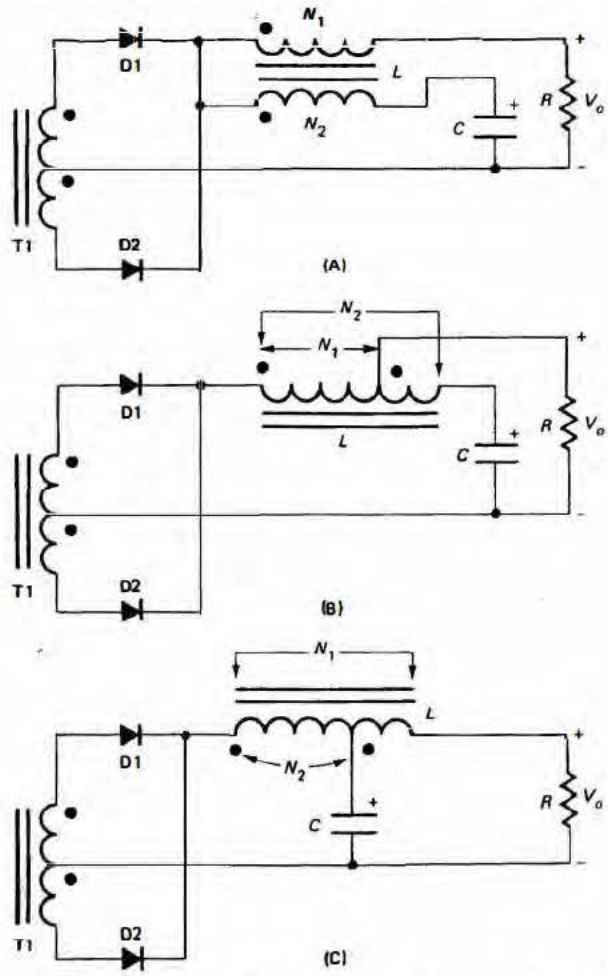


Fig. 8.5. Schemes for increasing the effective value of the output filter capacitor.

allows a selection of C that often results in a smaller and less expensive part. If the impedance of the filter capacitor at high frequencies is dominated by internal parasitics (resistive or inductive), then the scheme of Fig. 8.5A may not be advantageous. The companion circuit of Fig. 8.5B is equivalent to that of Fig. 8.5A when $N_2 > N_1$, while the circuit in Fig. 8.5C is equivalent to that of Fig. 8.5 A when $N_2 < N_1$.

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Further discussions of integrating inductor as well as transformer windings on single core structures are contained in Chapter 12.

8.2. TRANSFORMER WINDING TAPS

Provision for a multiplicity of output voltages is a very common requirement for an SPC. Traditionally, this requirement is met by providing multiple transformer windings, as shown in the example of Fig. 8.6A. Normally, one output is chosen to be directly regulated and voltage regulation of the other winding outputs may suffer as a result. One of the key ingredients that determine cross-regulation properties between SPC windings is winding-to-winding coupling. If windings are tightly coupled, then good cross regulation is possible. Coupling between windings can be greatly improved by using a single secondary winding, tapped as shown in Fig. 8.6B. However, DC isolation between windings is lost using this technique. In addition to improving the winding coupling properties, copper utilization factors are usually better. Voltage drops due to winding resistance are somewhat self compensating because the resistance is common to both windings, which further improves the cross regulation. Another factor determining cross regulation is the variation of the forward voltage drops (V_f) of the rectifier diodes. For silicon diodes, the temperature coefficient of V_f is about -2 mV/°C. In applications where extreme changes in circuit temperatures are present, definite changes in V_f will occur and cross regulation will suffer as a result.

For example, assume that one output (V_2) is +5 V and the other (V_1) is +10 V in the circuit of Fig. 8.6B. Further, we will assume that the +5 V output is tightly regulated by the control loop. If the forward voltage drops of D2 and D3 were to increase by 50 mV resulting from a 25°C drop in temperature, the voltage control electronics would respond by increasing the winding voltages associated with D2 and D3 by 50 mV to maintain a constant +5 V output. Since the ratio of N_1 to N_2 is 10/5, the winding voltages at D1 and D4 will increase by (10/5) (50 mV), or 100 mV. Presumably, the voltage drops of D1 and D4 will also increase by 50 mV due to the temperature change. Therefore, a net 50 mV increase of the +10 V winding will occur. In this example, it is possible to compensate for the +10 V output change by adding a series diode (D5 in Fig. 8.6B). The presence of D5 adds further power loss to the SPC and could reduce efficiency significantly if loads on the +10 V output are large.

The primary windings of an SPC's transformer can also be tapped to enhance performance. Fig. 8.7A shows a quasi-squarewave converter (Fig. 5.13), in which two more switch elements (S3, S4) with corresponding taps on the transformer have been added. Note also that each of the two new switches are operated at a 50% duty cycle. The result of this change in topology is an alteration of the input current and output voltage waveforms as shown in Fig. 8.8. For illustration purposes, we have assumed an average output voltage of 5 VDC and an average

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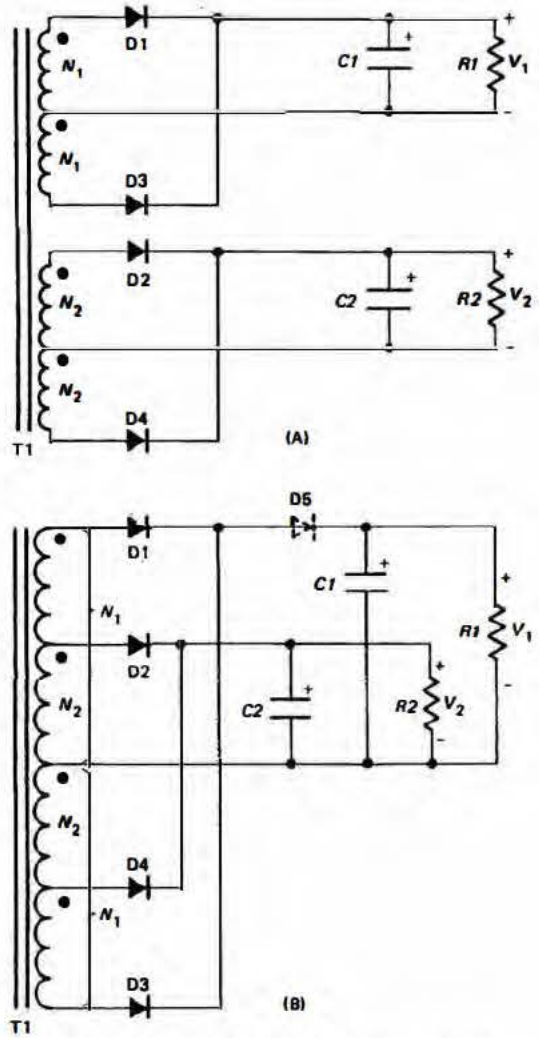
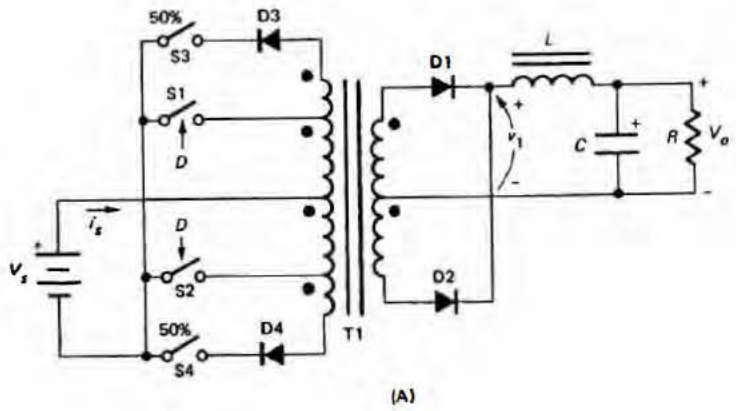


Fig. 8.6. Multiple-output secondary winding variations.

input current magnitude of 2 ADC. Fig. 8.8A and C are the waveforms for an "untapped" converter (Fig. 5.13) and Figs. 8.8B and D are corresponding waveforms for the tapped converter of Fig. 8.7A. Note that the primary-to-secondary turns ratios have been adjusted so that D is the same in both converters. By

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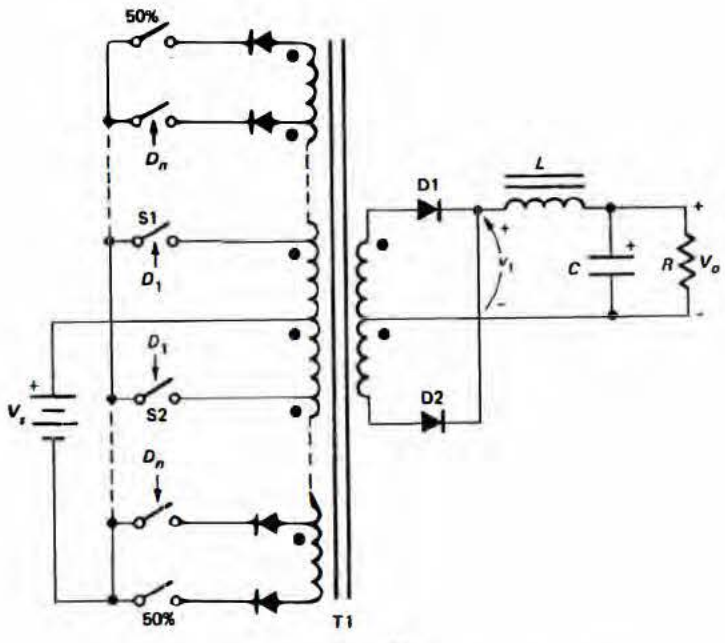


Fig. 8.7. A tapped-primary quasi-squarewave converter.

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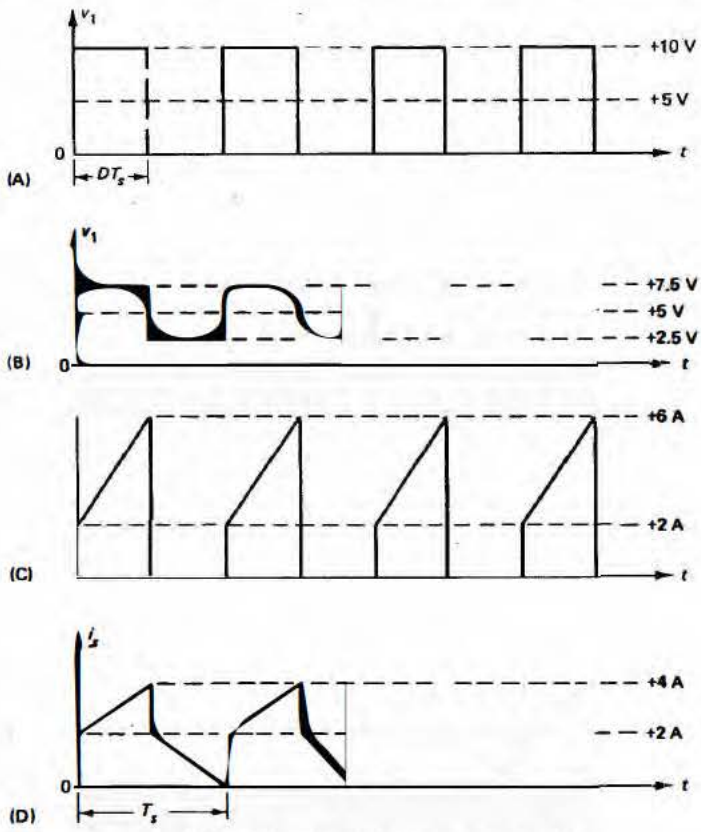


Fig. 8.8. Voltage and current waveform comparisons.

inspection of the waveforms of Fig. 8.8, several benefits become evident. First, the rms value of v_1 is lower in the tapped case, which will result in the output filter being smaller in size. Also, the peak reverse voltage on output rectifier diodes is reduced. In the tapped example, the rms value of input ripple current as well as peak switch current is smaller, resulting in a smaller input filter network.

However, these improvements are not without penalty. The converter of Fig. 8.7A is now more complex, with twice as many primary switches and a multitap transformer primary winding. In the standard quasi-squarewave converter of Fig. 5.13, a lower limit on input voltage value is reached where its primary switches are operating at their maximum duty cycle. Also, there is no inherent upper limit on input voltage value other than the stress limitations of the circuit

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components. By reducing the switch duty cycle, a very wide range of input voltages can be accommodated by the conventional quasi-squarewave SPC. In the tapped version of this SPC in Fig. 8.7A, there will be an inherent upper limit on input voltage with its magnitude determined by transformer tap locations. To realize the benefits as outlined above for this converter, the range of input voltages is usually constrained to 2 to 1 or less.

Multiple transformer taps can be used, as shown in Fig. 8.7B, to synthesize an output voltage (v_1) with as many "steps" in level as there are taps. This approach is sometimes used by SPC designers to generate outputs that closely approximate sinusoids. Primary diodes in series with all but the innermost switches are necessary since the voltage appearing across the outside switches will reverse polarity when an inside switch is closed. Therefore, these diodes prevent any reverse tap currents which might damage switch components or produce converter malfunction.

The idea of using primary taps has many variations, some of which are shown in Fig. 8.9. Here, the number of switches or diodes can be reduced by altering the topology slightly (e.g., see Figs. 8.9A and C) or by moving the return reference point (Figs. 8.9B and D).

Primary transformer taps with additional switch elements can also be used in other circuits. For example, Fig. 8.10 shows a tapped version of the boost-derived converter of Fig. 6.4B. Bridge versions of the converter in Fig. 8.7A are shown in Figs. 8.11 and 8.12. If the input voltage range is 2 to 1 or less, then only one additional switch is needed, as illustrated in Fig. 8.11B. When using a full-bridge primary circuit, there are several alternate ways in which transformer taps and switch elements can be interconnected. Two of these possibilities are shown in Fig. 8.12.

In a similar fashion, primary transformer tapping can be applied to half-bridge SPC circuits. One example is shown in Fig. 8.13.

Secondary-tapping with auxiliary switch networks is also possible. Fig. 8.14A shows a tapped secondary version of the post-regulated buck-derived converter developed in Chapter 5 (Fig. 5.14A). This SPC has exactly the same electrical properties as the tapped primary quasi-squarewave circuit of Fig. 8.7A, except that voltage regulation control (S3) is performed on the secondary and three switches are needed for a single output rather than four in the circuit of Fig. 8.7A. If multiple regulated SPC outputs are desired, then each output will still need a separate control switch, as was the case in Fig. 5.14B.

A boost-derived circuit using a tapped secondary is shown in Fig. 8.14B. It's untapped counterpart was developed in Chapter 6 (Fig. 6.4B).

When an SPC's output rectifier network uses a bridge configuration, then several other tapped variations are possible, two of which are shown in Fig. 8.15.

Very high frequency or very high power SPCs frequently have very few turns on the transformer windings associated with low-voltage outputs. If multiple-

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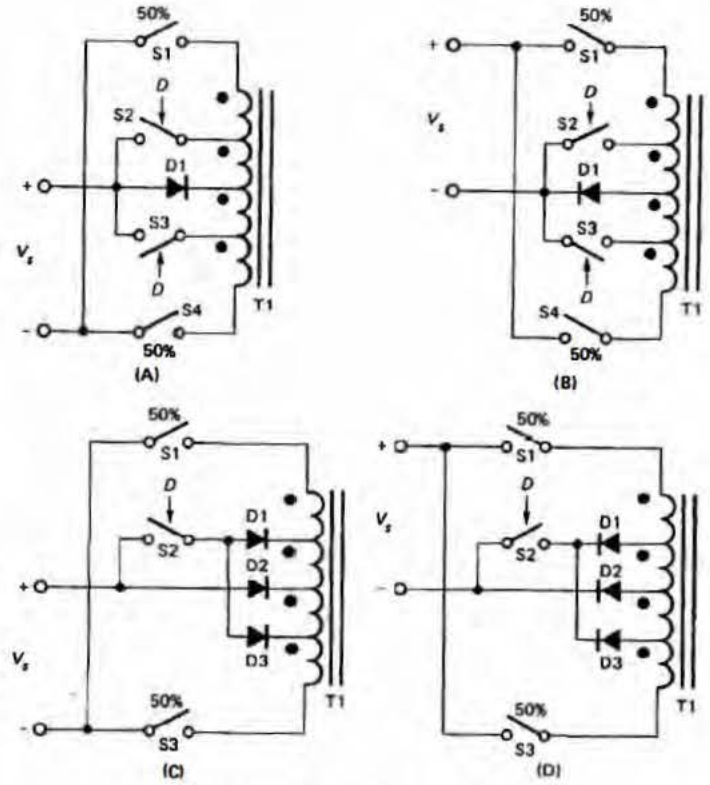


Fig. 8.9. Primary tapping variations.

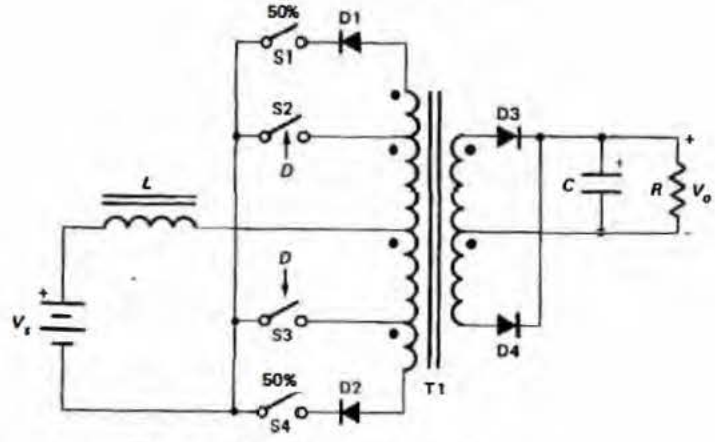


Fig. 8.10. A tapped primary boost-derived converter.

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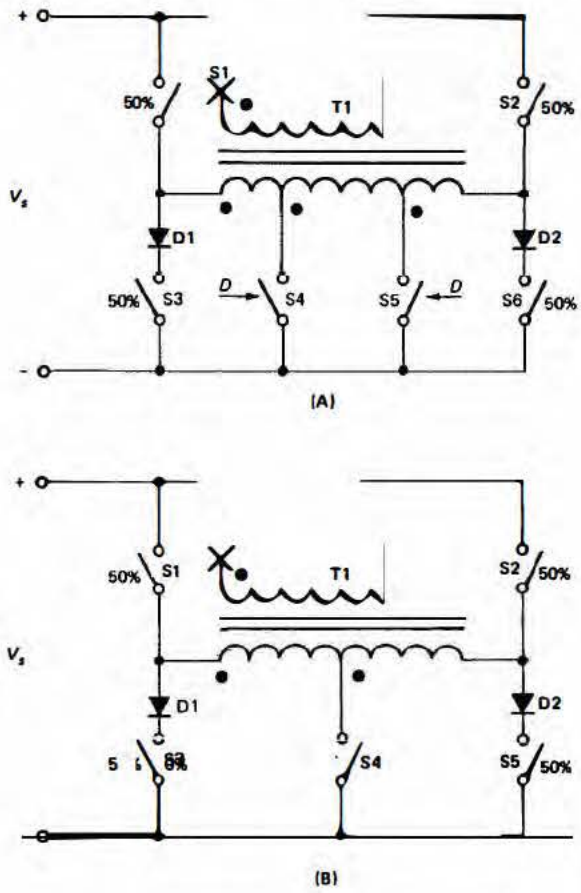


Fig. 8.11. Tapped primary full-bridge switch connection variations (I).

output voltages are required of such SPCs, a problem can exist in obtaining sufficient resolution and cross-regulation between all outputs since secondary volts-per-turn factors may be quite high. One means to alleviate this particular problem is the addition of a small transformer (T2) to provide a trimming voltage in series with the output rectifiers, as shown in Fig. 8.16. This trimming voltage may be either aiding or opposing in its contribution. Voltage amplitudes presented by these trimming windings are determined by the turns ratio of N_1 to N_2 and N_3. The primary turns (N_1) on T2 can be made arbitrarily large so as to provide as

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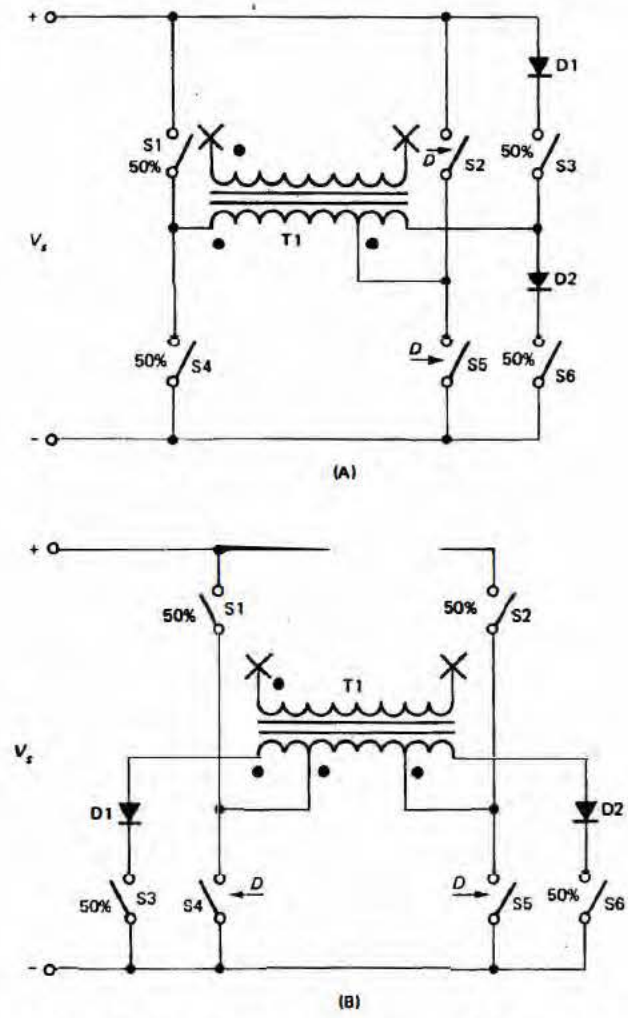


Fig. 8.12. Tapped primary full-bridge switch connection variations (II).

small a trimming voltage as desired. Therefore, corresponding resolution of output voltage (V_1) is very good. The addition of transformer T2 is not desirable for cost and size reasons; however it usually is a small transformer and relatively inexpensive. If improvements in resolution of several output windings are desired, transformer T2 can be designed to accommodate multiple trimming

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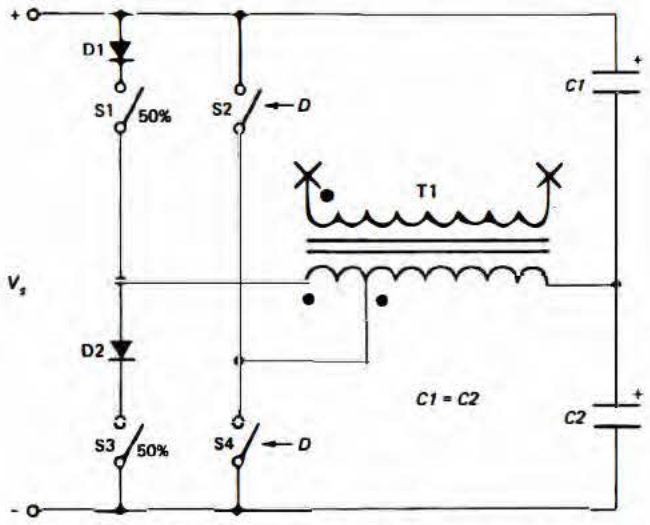


Fig. 8.13. Tapped primary half-bridge switch connection.

windings. Therefore, a separate "trimming" transformer will not be required for each output in such cases.

Like taps, multiple transformer windings can be very useful in a DC-DC converter. For example, in the circuit of Fig. 5.8, DC-isolated drives are required for all of primary switch elements. By using extra primary windings as shown in Fig. 8.17, all switch drives can be referenced to the same return point. This can permit (in many cases) the elimination of the drive transformers. Although the design and construction of Tl will be slightly more complex, overall system component count is reduced with corresponding savings in space and cost. This particular technique can be applied to many of the SPCs discussed in earlier chapters of this book to obvious advantage.

Another beneficial application of multiple primary windings in SPCs is shown in Fig. 8.18. Here, two separate primary windings are used, each with its own set of switches and one isolation diode. This arrangement allows the converter to operate from either of two different power sources. As an application example, V_{s1} could be a low voltage battery source and V_{s2} could be an AC-rectified source of high voltage DC. The primary turns ratios of the transformer could then be adjusted so that power is normally taken from V_{s2} until its voltage value drops to:

$$[V_{s2} - V_{Ds2}] = \frac{N_2}{N_1} [V_{s1} - V_{Ds1}]. \tag{8.7}$$

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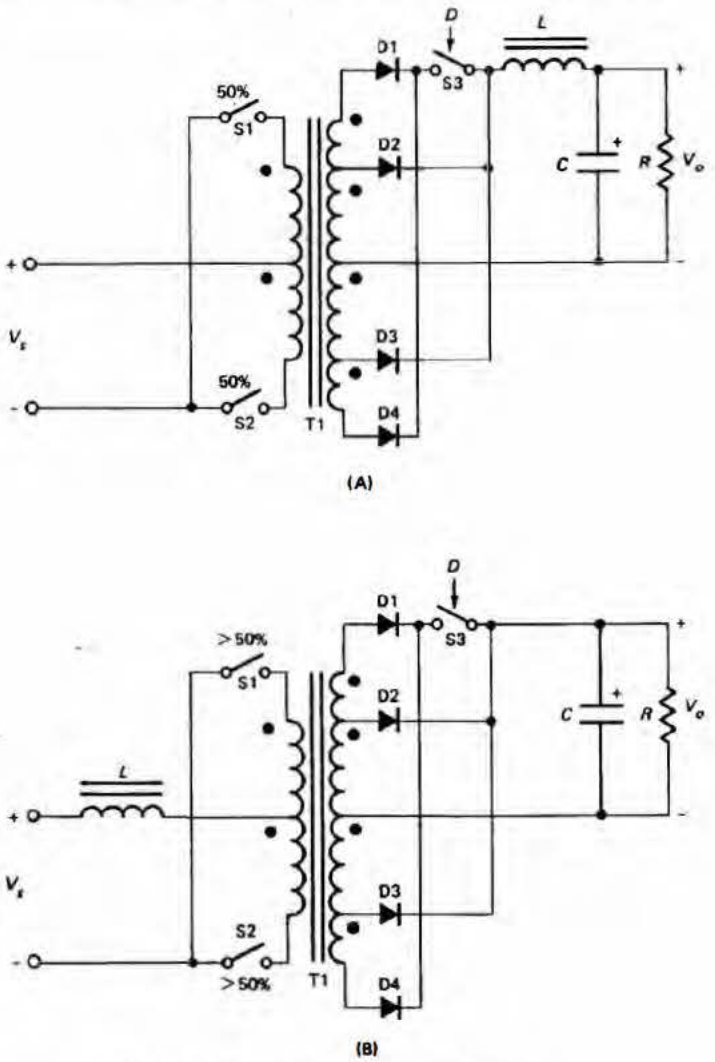
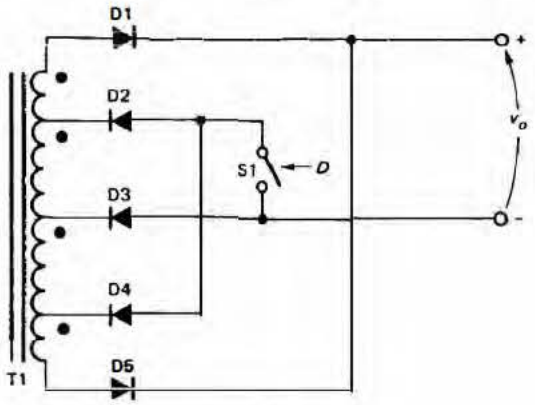


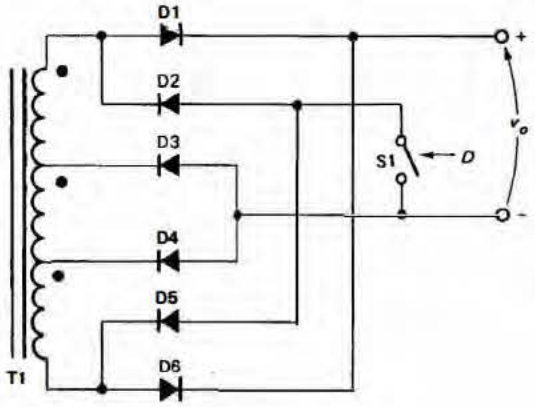
Fig. 8.14. Tapped secondary converters.

At this point, the converter's load power source isshifted to V_{s1} automatically with no interruption of output voltage during transition. As an additional refinement, a battery charger could beadded across D_{s1} to charge V_{s1} during normal

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(A)



(B)

Fig. 8.15. Tapped secondary variations.

operation. Additional diodes (shown dotted in Fig. 8.18A) will be needed across S1 and S2 to provide a bidirectional path for charging current if switches S1 and S2 are *not* operated in phase with S3 and S4, respectively.

8.3. COMBINING TRANSFORMER AND INDUCTOR TAPPING METHODS

It is evident from earlier discussions that tapping of either the inductor or the transformer windings of an SPC can produce useful and beneficial results. Both

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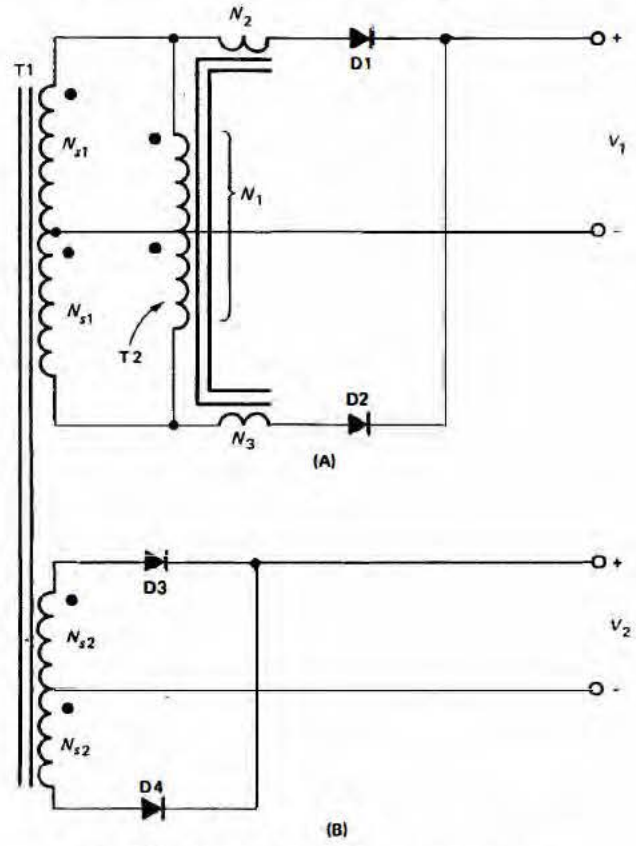


Fig. 8.16. Auxiliary output voltage-trimming scheme.

of these tapping techniques can be combined in a single converter so as to produce additional benefits. As a general rule, when both the transformer and the inductor are tapped, the turns ratio of both taps will have the same value.

The SPC circuit of Fig. 5.6 in Chapter 5 was developed to provide high conversion efficiency when operating from a low voltage source of power. Conversion power losses due to conduction voltage drops in S2, S3, D1, and D4 of Fig. 5.6 can be reduced even further if both the inductor and the transformer primary are tapped. The resultant topology is as shown in Fig. 8.19. In this circuit modification, the average current flowing through primary diodes (D1, D2) is reduced by the equal tap turns ratios of L and T1. Therefore, the overall ef-

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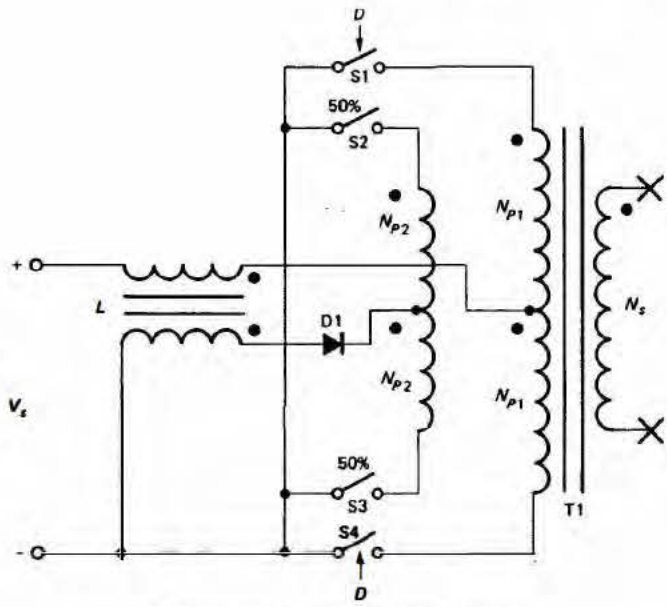


Fig. 8.17. Multiple primary winding example.

ficiency of power conversion will be much improved when a low voltage source is present.

In order for the output current to remain continuous, the turns ratios of the taps on the transformer and the inductor of a buck-derived SPC must be the same. If they are not equal, the inductor current waveform will have discontinuities with a corresponding increase in output voltage ripple. In addition, a small-signal analysis of an unbalanced tapped SPC of this kind will show that the cut-off frequency of the converter's equivalent output low-pass filter becomes a function of converter duty cycle, D. Therefore, without equal tap ratios, any buck-derived SPC will begin to display boost-like electrical properties.

The tapped transformer boost-derived SPC illustrated in Fig. 8.10A can have an alternate common connection point for its switches. This connection change is shown in Fig. 8.20A. The SPC's gain function is still the same even though its topology looks somewhat different. It is still a boost-derived converter with a discontinuous output current waveshape, moving low-pass filter poles, and a right-half-plane zero in its control-to-output transfer function. If the input inductor is tapped with the same turns ratio as the primary windings of the transformer, and two of its switches connected to the inductor tap as shown

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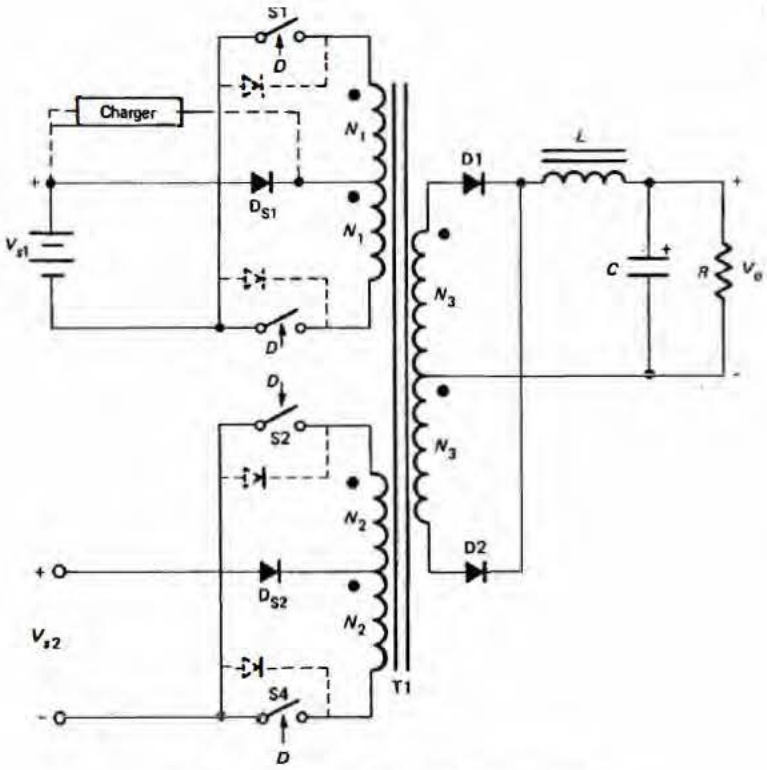


Fig. 8.18. A converter with multiple input sources.

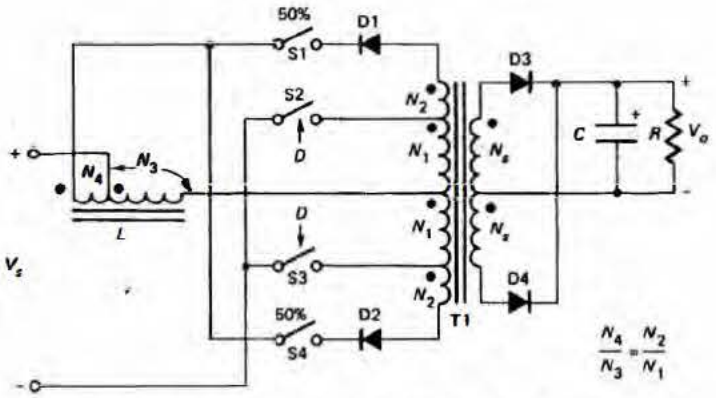


Fig. 8.19. A tapped inductor-and-transformer version of the Cronin converter.

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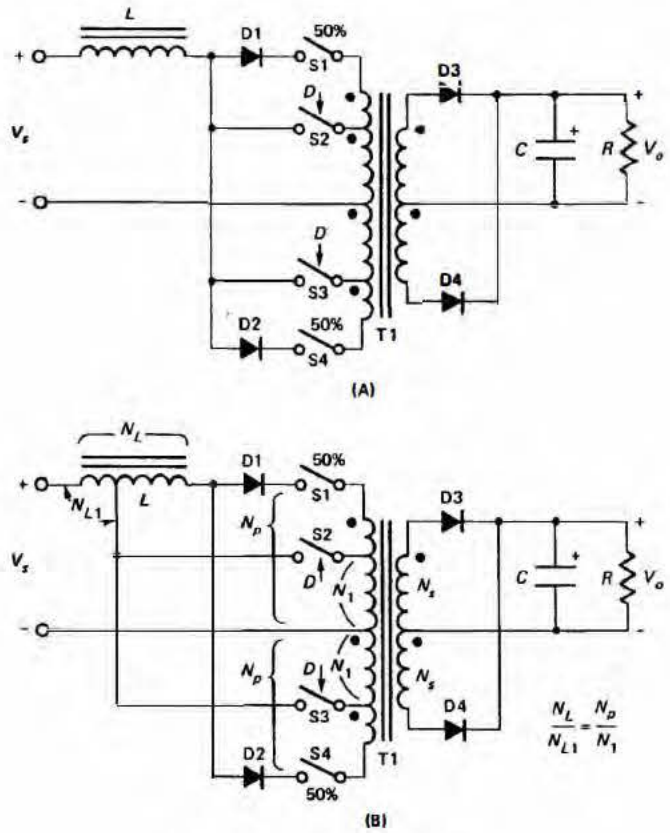


Fig. 8.20. Derivation of the Hughes circuit.

in Fig. 8.20B, a rather remarkable change in circuit properties occurs. The ampere-turns product in the primary winding of T1 is now constant and independent of switch conduction duty cycle, D. The output current waveform is now continuous, just as it would be for a buck-derived converter. Further, a small-signal analysis of the SPC topology will show that the effective value for output filter inductance is constant. As a result, the output filter poles do not move with duty cycle and the control-to-output right-half-plane zero, characteristic of a boost-derived converter, has disappeared! Despite the fact that this particular SPC circuit was clearly derived from a boost topology, it has many of the properties of a buck-derived converter. However, some properties characteristic of a boost SPC are still retained. For example, magnitudes of output

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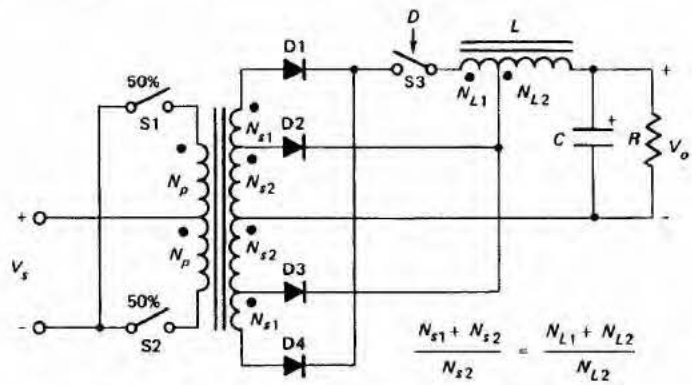


Fig. 8.21. A tapped transformer secondary and inductor circuit.

short-circuit and turnon inrush currents (see Chapter 3) cannot be controlled by control of switch duty cycles. Also, some circuit provisions must be made to safely dissipate the energy stored in the input inductor as well as in the transformer when all four switches in Fig. 8.20B are turned OFF.

In a similar fashion, the buck-derived converter of Fig. 8.14 can be equipped with tapped inductor and transformer elements as shown in Fig. 8.21. As was the case in the last example, SPC circuit properties are radically altered. If the transformer and the inductor are tapped equally, the input current of this SPC will be continuous just as it would be in a boost-derived converter. Output current is now discontinuous and the output filter transfer function will change as a function of the conduction duty cycle of switch S3. In contrast to the SPC of Fig. 8.20B, this converter topology has become boost-like in nature!

In this latest group of complex SPC circuits, it is interesting to observe that pulsating current characteristics of input or output terminals can be interchanged by adding or removing taps on internal inductors and transformers. From an EMI point of view, these design alternatives can be very useful in directing and controlling the major conduction noise sources of an SPC, especially if the converter must be designed to meet tough conducted EMI specifications such as those imposed by European countries on power supply systems.

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9. Duality Among SPC Circuits

After examining a multitude of SPC topologies in preceding chapters, one might be led to believe at this point that all variation possibilities have been exhausted. Such is not the case.

Recall that the tools we used to build the more complex SPCs of past chapters were essentially combinational in nature. In this chapter, we will turn to evolutionary methods that employ deductive reasoning based on duality.

Duality is a fundamental electrical circuit principle and discussions of its application in linear network analysis are found in most basic electrical engineering textbooks. Although SPCs are *nonlinear* electrical systems by their very nature, we saw in Chapters 2 and 3 that we could formulate *linear* small-signal models for the buck and boost converters, using state-space averaging methods. Therefore, it is logical to assume that *linear* duality analysis and synthesis principles can be applied to SPCs.

In this chapter, we will conduct duality investigations of SPC topologies to generate new circuit variations and, perhaps more importantly, to show functional relationships between them that will enhance our understanding of their unique properties. As a part of these duality discussions, the concept of varying the SPC circuit properties by changing the switch operating sequences will be introduced.

9.1. BILATERAL INVERSION

In Chapter 4, it was demonstrated that bidirectional power transfer could be achieved in a DC transformer if switch elements were placed across the output diodes and antiparallel diodes placed across the primary switches (Fig. 4.16). This same technique can be used to provide bilateral power flow in any SPC, regardless of its complexity. An example of its application using a boost converter is shown in Fig. 9.1. Fig. 9.1A shows the elementary topology of the converter. In Fig. 9.1B, a switch (S2) is placed across the output diode (D1) along with another diode (D2) across the input switch (S1). The direction of power flow will now depend on switch conduction duty cycle (D) and the relative amplitudes

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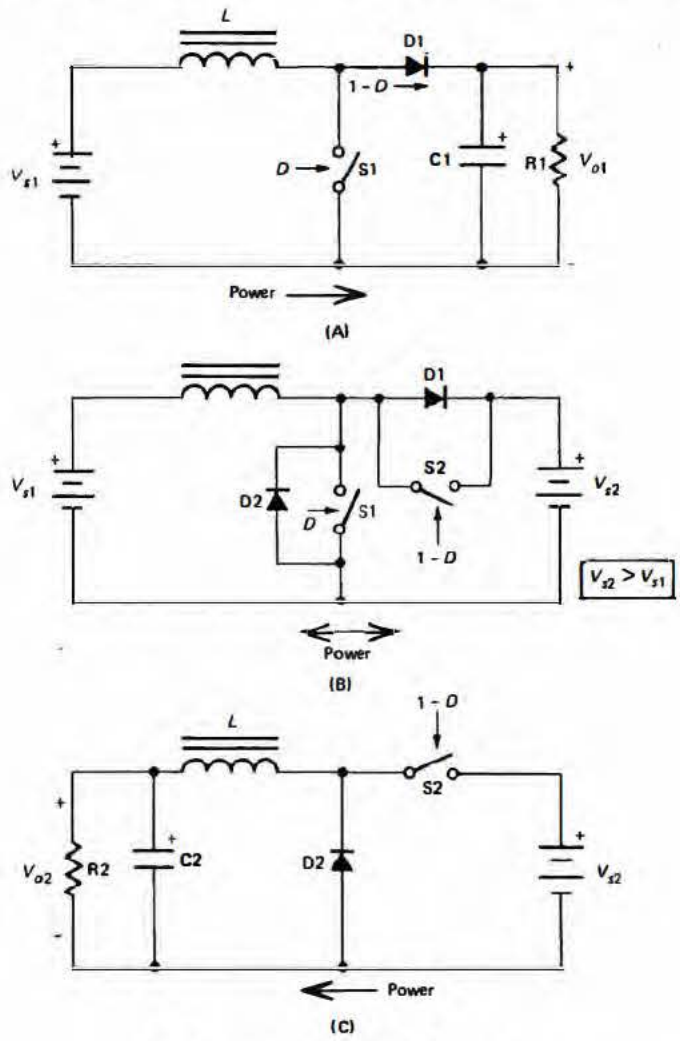


Fig. 9.1. An example of bilateral inversion.

of voltage sources V_{s1} and V_{s2}. If V_{s1} and V_{s2} are maintained relatively constant in their values, then the direction of power flow will be controlled by D. As D is made larger, the power will begin to flow from V_{s1} to V_{s2}. Conversely, as D is made smaller, direction of power flow will reverse and flow from V_{s2} to V_{s1}.

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Continuing the bilateral process, the original switch (S1) and diode (D1) in Figs. 9.1A and B are now removed, resulting in the SPC of Fig. 9.1C. This converter circuit is now unidirectional in its power flow; however, in contrast of the original SPC of Fig. 9.1A, the power flow direction is from right to left. The original source V_{s1} is then replaced by the load R2. Looking at the circuit in Fig. 9.1C, we see that it is nothing more than a mirror image of a buck converter topology! The process steps illustrated in Fig. 9.1 are a special case of duality and are referred to as *bilateral inversion.*

From this simple exercise, it becomes readily evident that boost and buck topologies are dual converter structures. It is interesting to observe that the boost converter circuit could have been easily "created" by applying the above processes to a buck converter circuit. For this reason, it is tempting to inquire which of these two SPCs is "more" fundamental than its counterpart. This particular question, when asked, often leads to much discussion with no definitive answer. For our purposes, we will assume that *both* are fundamental DC-DC power converters with duality relationships evident in their electrical characteristics.

The general rules for applying bilateral inversion can be stated as follows:

STEP 1. Each switch element is replaced by a diode phased to conduct current in the opposite direction from that seen by the switch element to be replaced.

STEP 2. Each commutating diode is replaced by a switch element phased to conduct current in the opposite direction from that seen by the diode to be replaced.

STEP 3. Conduction duty cycle of replacement switches is the inverse of that of original SPC switch elements (i.e., $D' = 1 - D$).

STEP 4. Assuming the input voltage to the original SPC circuit is V_s and its output voltage is V_o for a given value of D, the source voltage is replaced by a load with a potential V_s and the original load replaced by a source voltage with a potential V_o.

STEP 5. For the same value of D in Step 4, the replacement load and any output capacitance becomes:

$$R2 = R1\left[\frac{V_o}{V_s}\right]^2, \quad C2 = C1\left[\frac{V_s}{V_o}\right]^2.$$

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STEP 6. For given values of V_s, V_o, D, and output power levels, the dual circuit will *not* change operating mode (i.e., continuous or discontinuous) over that of the original converter circuit.

9.2. INVERSION OF RECTIFIER NETWORKS

The principles behind bilateral inversion can be applied with equal facility to rectifier networks. For example, in Fig. 9.2, we have taken four common rectifier networks and applied the rules delineated earlier for bilateral inversion. As shown, the duals of these output rectifier circuits are the four common primary switch connections found in SPC's.

It is also interesting to note that the four rectifier connections shown in Fig. 9.2 represent only a few possibilities, with many other circuit arrangements in common use. This observation leads directly to the idea of applying bilateral inversion principles to all known rectifier connection arrangements to derive new and potentially useful switch connections.

Let us now explore this idea. The rectifier connection given in Fig. 9.2C is called a *voltage doubler*. Another circuit form of a single-winding voltage doubler exists and is shown in Fig. 9.3A. Applying the rules of bilateral inversion, the switch network of Fig. 9.3B results. This arrangement is an alternative to the common half-bridge connection and allows one side of the primary of T1 to be connected to the common return point of the source voltage. Although the need for capacitor C2 may not be apparent from Fig. 9.3A, practical SPC circuits seldom are designed to permit pulsating currents to flow in their power sources; therefore, C2 will normally be added to "smooth" out such current pulsations.

Voltage multipliers with gain ratios greater than 2 are possible and their networks can be inverted to evolve switch connections which exhibit the voltage and current characteristics of the multipliers. Fig. 9.4 shows a voltage quadrupler network (A) and its dual switch connection (B). In this switch network, the average voltage appearing across any open switch will be equal to 50% of the input source voltage (V_s)! As an example, the network of Fig. 9.4A would allow switch elements with breakdown ratings of 400 V to be used when operating from a 700 V source (some derating of breakdown voltage is assumed here). Therefore, series connection of switch elements to increase voltage breakdown capability is not required, as might be the case in conventional SPC primary switch connection schemes. Lin and Chua have demonstrated that this type of quadrupler (Ref. 3) has nine possible variations each of which will produce a switch connection with slightly different properties. A 7-times multiplier would have 115 variations, which should be enough to keep even the most ambitious analyst busy for some time.

There are other, and in some ways, better means for providing voltage multiplication by rectification and capacitive energy storage. One of the problems

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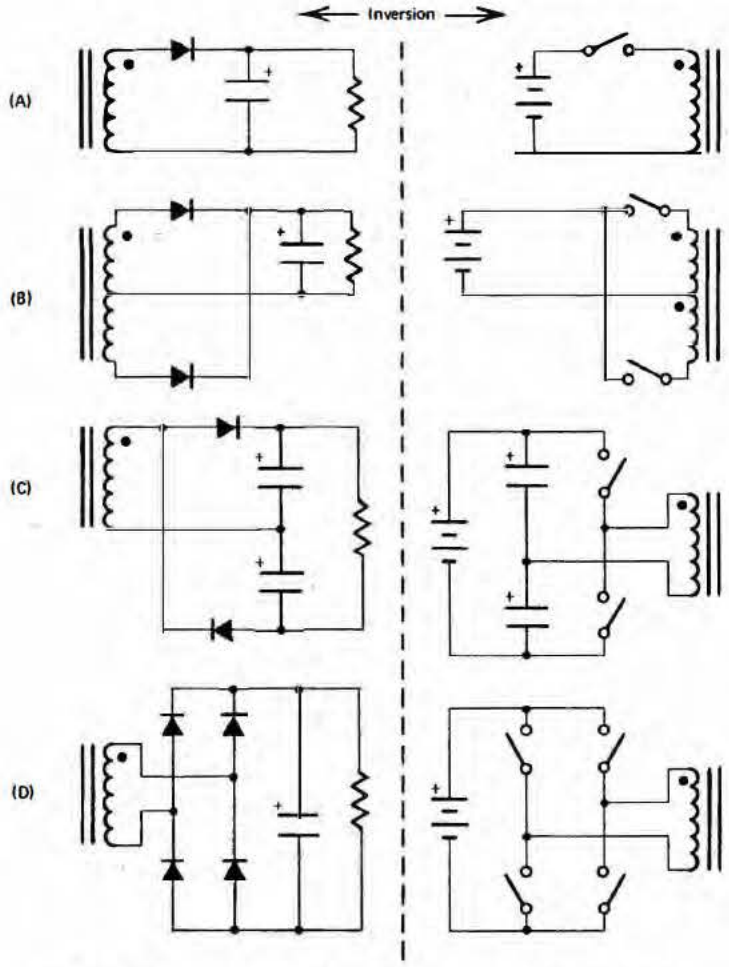


Fig. 9.2. Bilateral inversion applied to four common rectifier connections.

with the multiplier circuits just shown is the high output impedance and the large diode currents, both properties of which are transferred to their dual switch circuits. Other forms of voltage multipliers exist, some of which have much lower output impedances. The voltage doubler form of one of these rectifier connections is shown in Fig. 9.5A, with the dual switch connection in Fig. 9.5B. This latter circuit is a double-bridge switch connection in which each switch

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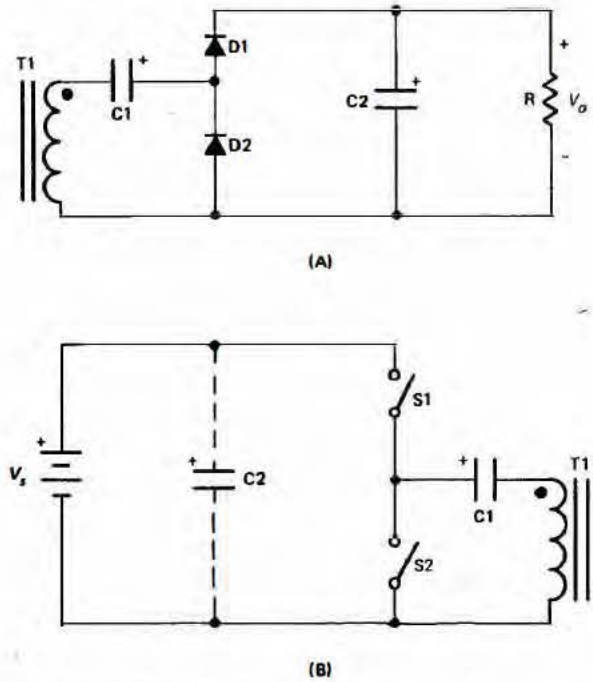


Fig. 9.3. Bilateral inversion of an alternate voltage-doubler rectifier connection.

sees a maximum OFF voltage of $V_s/2$ and a peak ON current equal to that of I_s. The transformer's peak-to-peak primary voltage will be equal to V_s. In this type of multiplier-derived switch connection, the switch currents do not increase in direct proportion to the multiplication number, as was the case for the connections in Figs. 9.2C, 9.3B, and 9.4B. The correct timing sequence for the SPC circuit of Fig. 9.5B is to close switch set S2, S3, S6, and S7 or switch set S1, S4, S5, and S8 simultaneously. In other words, each bridge set of Fig. 9.5B is operated with identical switching sequences.

Multipliers can be extended to even higher orders. Two examples of voltage triplers are illustrated in Fig. 9.6. In higher-order multiplier networks, there is a choice to be made in arrangement of energy storage capacitors. These capacitors may be connected in series (Fig. 9.6A), in which case each capacitor will see nearly the same value of DC bias. However, to keep the output impedance of the network low, the capacitors are usually large in value. In Fig. 9.6A, capacitors C1 and C2 should have values at least twice that of capacitors C3 and C4. Lower output impedance can be obtained if the energy storage capacitors

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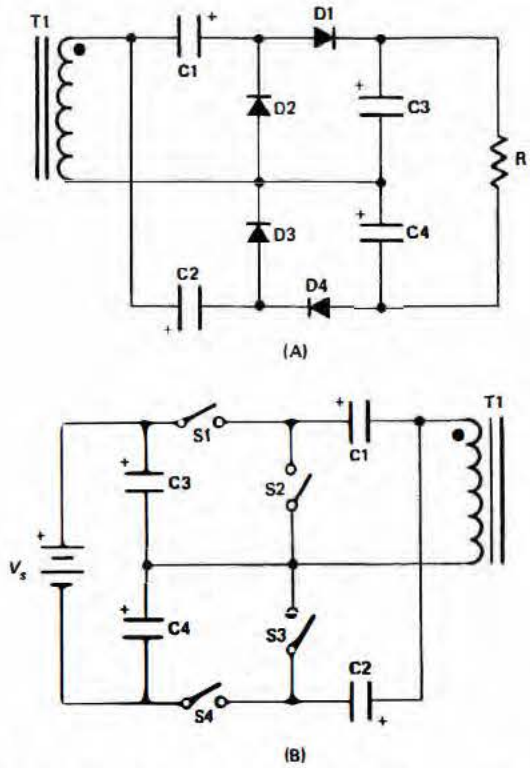


Fig. 9.4. Bilateral inversion of a quadrupler rectifier connection.

are connected in a parallel fashion as shown in Fig. 9.6B. Here, capacitors C3 and C4 will experience a DC bias of twice that appearing across C1 and C2. In a voltage-tripler network, high DC voltage across its capacitors is not usually a problem. However, in higher-order multipliers, capacitor sizes can become very large, since their stored energy is proportional to the square of the voltage appearing across their terminals. When multipliers of this variety are used for very high voltage gain, combinations of series and parallel capacitor methods are normally employed. Typically, these combinations consist of groups of parallel capacitor triplers or quadruplers stacked to form a series-parallel network system.

Another form of a low impedance voltage-doubler circuit is shown in Fig. 9.7A, where two separate transformer windings and associated rectifier bridge networks are tied in a series fashion. Since there are no series capacitance elements in this doubler, output impedance can be made very low at the expense of additional

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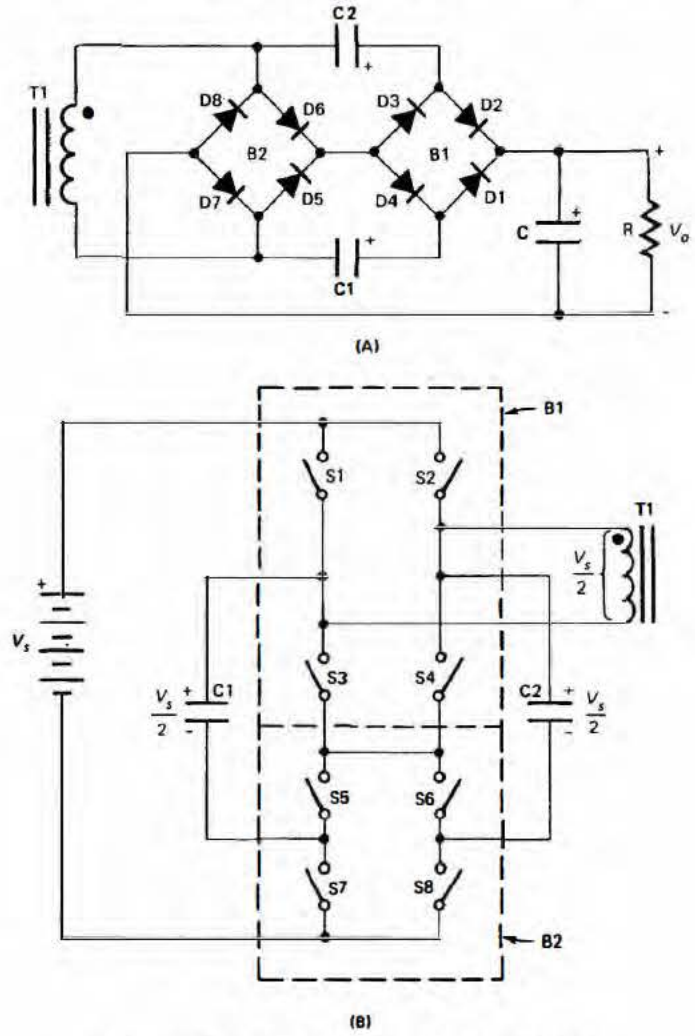


Fig. 9.5. Inversion of low impedance voltage multipliers (*I*).

transformer complexity. The output voltage of this system can be made even higher in value by adding more transformer windings and bridge networks without the loss of the low output impedance characteristic. For this reason, this particular voltage multiplier approach is very frequently used by designers in converters that must have high voltage output capability.

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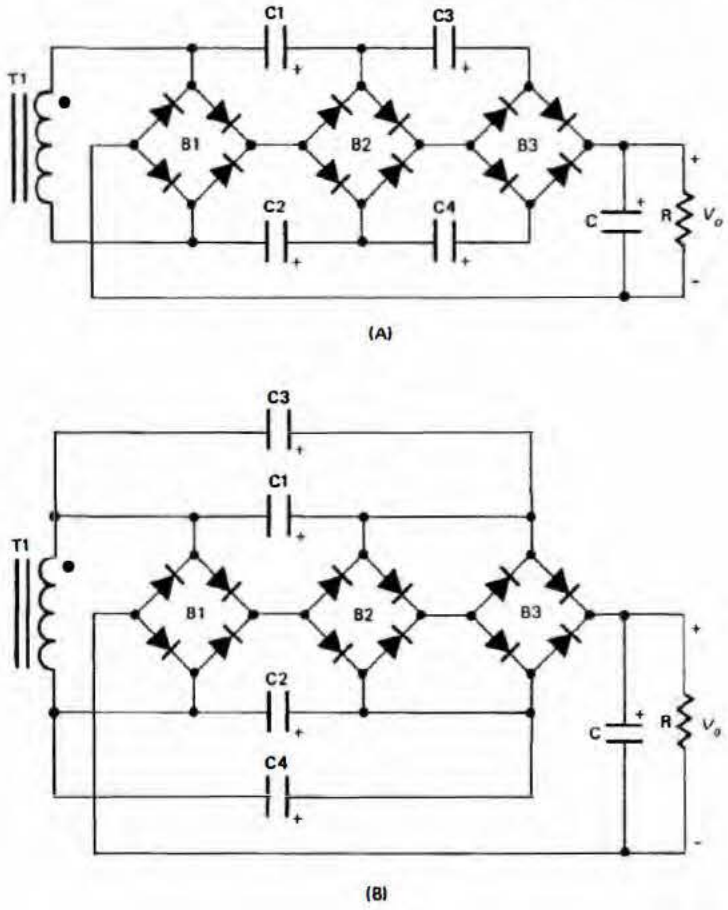


Fig. 9.6. Extension of the multiplier in Figure 9.5A to tripler arrangements.

The corresponding dual switch connection of this multiplier is illustrated in Fig. 9.7B. This is another double-bridge scheme (B1, B2) in which the maximum OFF voltage of each switch is $V_s/2$, with peak switch ON currents equal to that of the average source current. This switch connection would be particularly useful in an SPC which must operate from a 1000 to 1200 V voltage source and process tens of kilowatts of output power. Semiconductor switch elements exist today that could be used in the circuit of Fig. 9.7B to easily provide 50 kW or more output power. Even higher source voltage values and output power levels could be accommodated by stacking additional switch bridges and transformer

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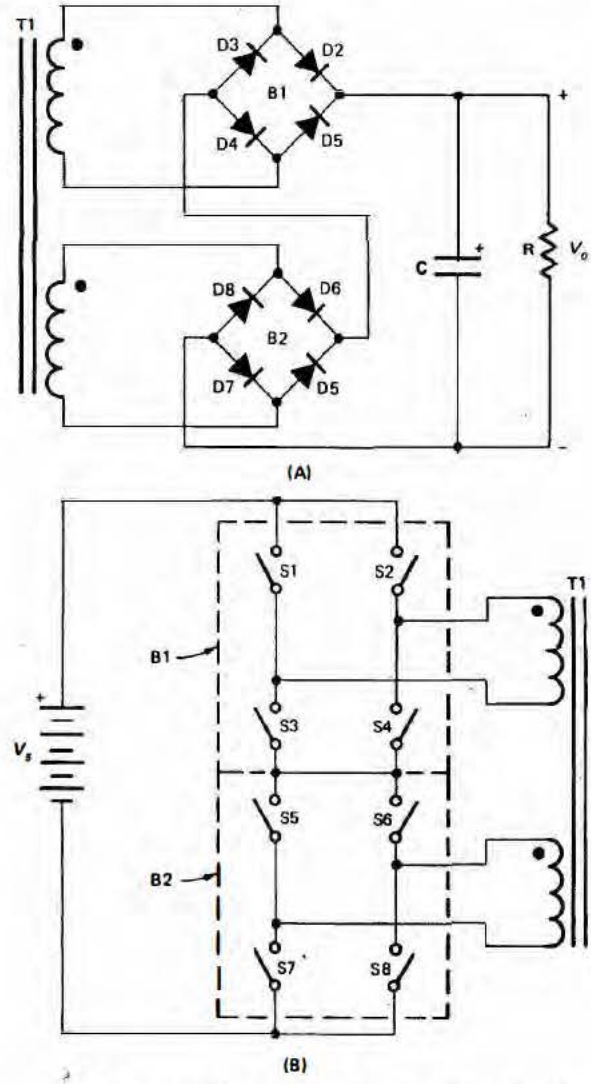


Fig. 9.7. Inversion of low impedance voltage multipliers (II).

windings to the extent that an SPC could conceivably be designed to provide hundreds of kilowatts of output power.

In addition to the vast number of voltage-multiplier connection possibilities, there are an equally large number of networks associated with polyphase rectifica-

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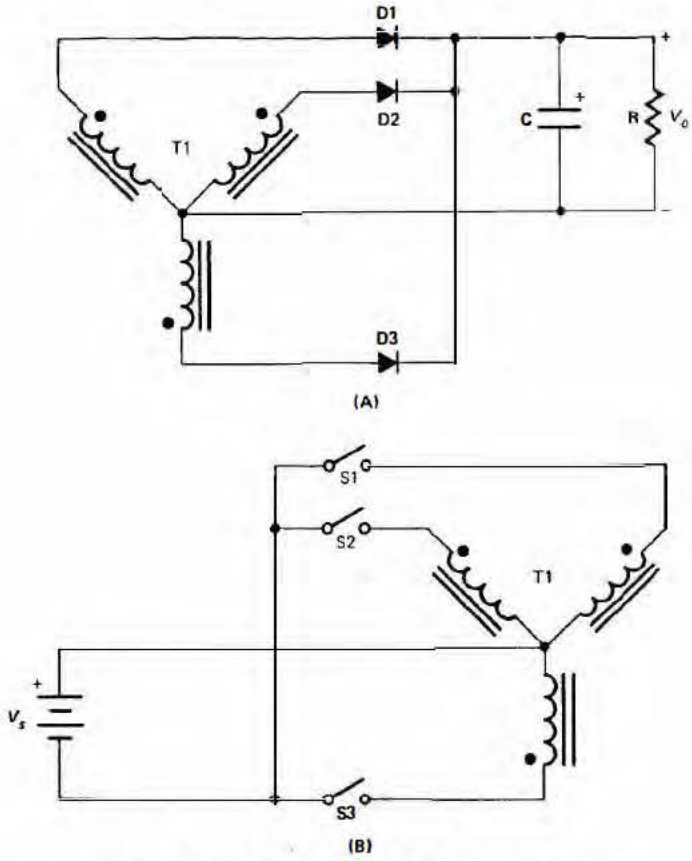
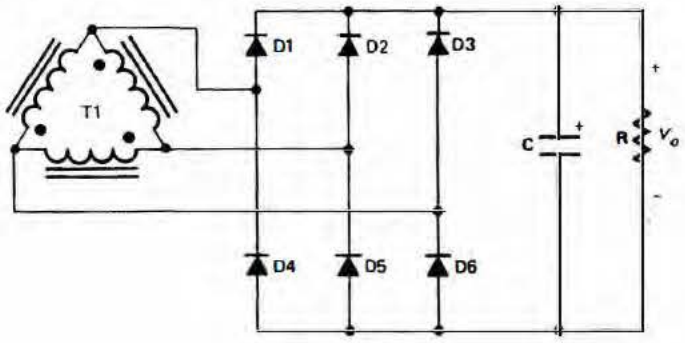


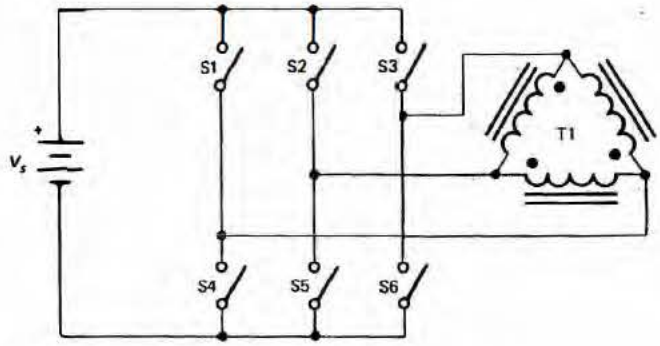
Fig. 9.8. Inversion of the three-phase star rectifier connection.

tion to which the principles of bilateral inversion can be applied. Two circuit examples and their duals are shown in Fig. 9.8 and 9.9. Polyphase rectifier networks provide many electrical benefits, especially at high power-processing levels. These benefits include higher ripple frequency, automatic current-sharing among multiple devices, better copper utilization of associated transformer windings, and many more. To a great extent, these desirable electrical properties are retained in the dual polyphase switch connections. For example, if the primary switches shown in Fig. 9.9B are operated at a switching rate of 20 kHz, the output voltage ripple frequency of any transformer secondary winding will be (6) (20 kHz), or 120 kHz. Obviously, any low-pass output filter will be smaller in size because of the higher ripple frequency. The timing sequence of switching

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(A)



(B)

Fig. 9.9. Inversion of the three-phase bridge rectifier connection.

for this polyphase converter is diagrammed in Fig. 9.10. We observe that maximum duty cycle of any switch is approximately 33%, whereas, in a single-phase full-bridge connection, the duty cycle limit would be 50% Also evident is the fact that *only* one switch at a time will turn on if $D < \frac{1}{6}$. This would imply that the output voltage from the converter must be zero; thus, the required range of the duty cycle of any switch is $\frac{1}{6}$ to $\frac{1}{3}$ in order to produce zero-to-full output voltage. In the polyphase full-bridge connection, inherent delays in switching actions (such as storage time in BJTs) do not pose conduction overlap problems under converter overload conditions (i.e., small values of D). As we have just seen, such delays can be as long as one-sixth of the entire switching interval (T_s) and still be tolerated.

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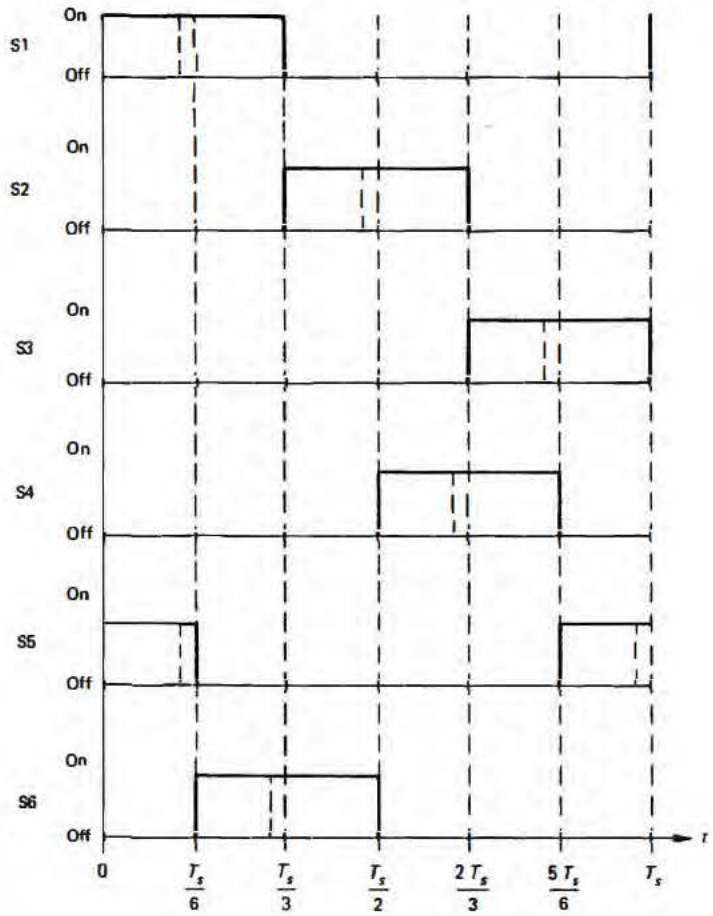


Fig. 9.10. The three-phase bridge switching sequence.

By equipping the polyphase switch connection of Fig. 9.9B with the multiple bridge approach of Fig. 9.7, very high power converters are possible and practical.

9.3. TOPOLOGY MODIFICATION BY SWITCHING SEQUENCE VARIATIONS

Up to this point, we have assumed that each SPC topology has individual and distinguishable sets of electrical characteristics, i.e., buck, boost, or some combination thereof. Now we will look at SPCs whose topologies are still fixed in circuit form, but whose conversion characteristics can be drastically altered by

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changing the sequence in which their switches are opened or closed. As an example of such systems, the circuit of Fig. 5.8 will be used. In Fig. 9.11, we see the two "normal" switching states of this converter. At the beginning of the switching cycle, switches S1 and S2 are closed (State I) and the current flows from the source through inductor L1 and switch S1 to the ouput via the transformer, T1. Part way through the first half-cycle of switching operation, S1 is opened (State II) and energy stored in L discharges through D1 and S2 into the output. This two-state sequence is then repeated using S3 and S4 to complete one switching cycle of operation. As was shown in Chapter 5, the SPC of Fig. 9.11 is a buck-derived converter.

An alternative two-state switching sequence is shown in Fig. 9.12. At the beginning of a switching cycle, S1, S2, and S3 are closed (State I). Once again, current flows from the input source through L. However, now the average inductor current divides equally between S1 and S3 and effectively places a "short circuit" across the primary of T1. Therefore, no energy is delivered to the out-

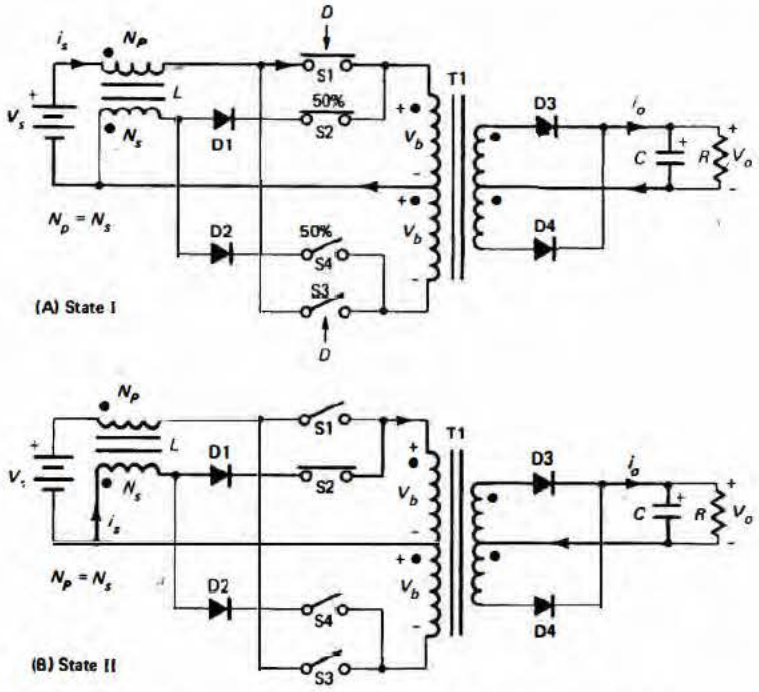


Fig. 9.11. Operation of the Severns circuit in the buck-derived mode.

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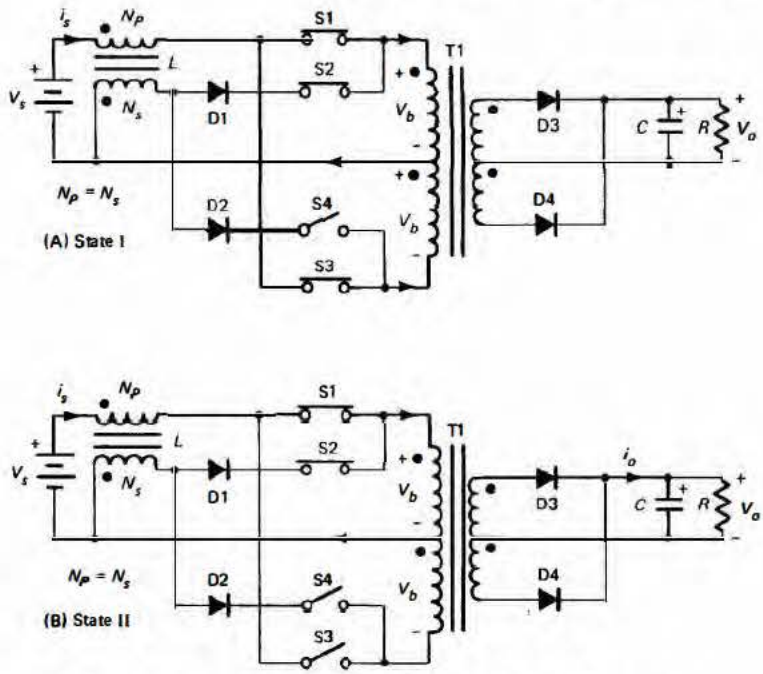


Fig. 9.12. Operation of the Severns circuit in the boost-derived mode.

put during State I. Part way through this half-cycle of conversion action, S3 opens (State II) and all of the energy in L is delivered to the output through S1. Notice that the secondary winding of inductor L, as well as S2, S3, D1, and D2 play *no* part in conversion operation using this timing sequence. Therefore, this SPC operates in much the same manner as did the boost-derived converter shown in Fig. 6.4B.

The difference between the converter switching sequences of Fig. 9.11 and Fig. 9.12 lies in switch duty cycle D. In Fig. 9.11, D is always less than 50% while in Fig. 9.12, it is always greater than 50% Thus by simply altering switch duty cycle, this SPC can operate either as a buck or a boost converter! Another circuit variation that would provide a similar type of operation with proper sequencing of switches is the full-bridge SPC of Fig. 5.17A.

This is a rather peculiar and interesting capability and one may wonder if sequence changes in SPC timing have any practical application. To demonstrate the utility of this technique, an illustration is in order. Some time ago, one of the authors was asked to design a high power off-line (i.e., source voltage is de-

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rived from high-voltage rectified AC) unity-power-factor converter with a very high quality input current waveform. The unity power factor requirement clearly indicated that a boost-derived SPC was needed, since all buck-derived converters have pulsating input currents. The SPC circuit topology chosen was the full-bridge overlapping-conduction converter of Fig. 6.10A. The converter worked very well for normal steady-state operation. However, because it was a boost-derived SPC, it could not, by its very nature, provide inrush and overload current-limiting, as was pointed out in Chapter 3. To circumvent these turnon and overload problems, the SPC topology circuit was modified to that shown in Fig. 9.13. Here, an auxiliary winding was added to the input inductor L and connected to the center tap of the primary on T1 through a diode (D1). This modification allowed the converter to operate in a "buck" mode when overload or turnon inrush current control protection was required. The circuit is affectionately called the *shower converter* because the changes in topology were evolved early one morning while one of the authors was standing under a hot shower, with its warm water apparently acting as a catalyst in the innovation process.

The moral of this story brings us to another key idea relative to SPC design.

KEY IDEA #6

IF YOU WANT THE PROPERTIES OF A BUCK CONVERTER, THEN THE SPC *MUST* BE BUCK-DERIVED. IF THE PROPERTIES OF A BOOST CONVERTER ARE REQUIRED, THEN THE CIRCUIT CHOSEN *MUST* BE BOOST-DERIVED. IF *BOTH* BUCK AND BOOST PROPERTIES ARE DESIRED OF AN SPC, THEN *EITHER* THE CIRCUIT MUST BE EVOLVED FROM A COMBINATION OF BUCK

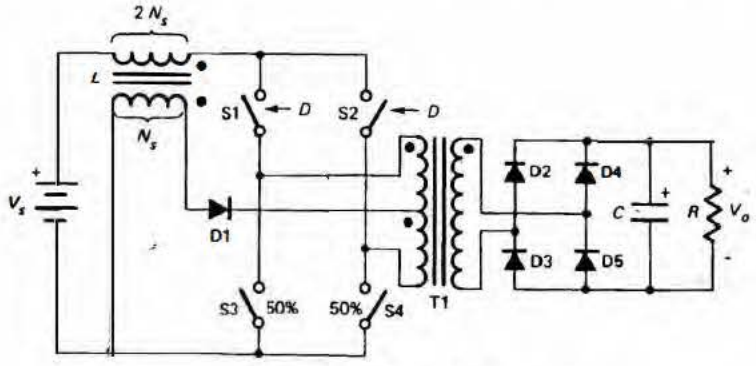


Fig. 9.13. The Shower circuit.

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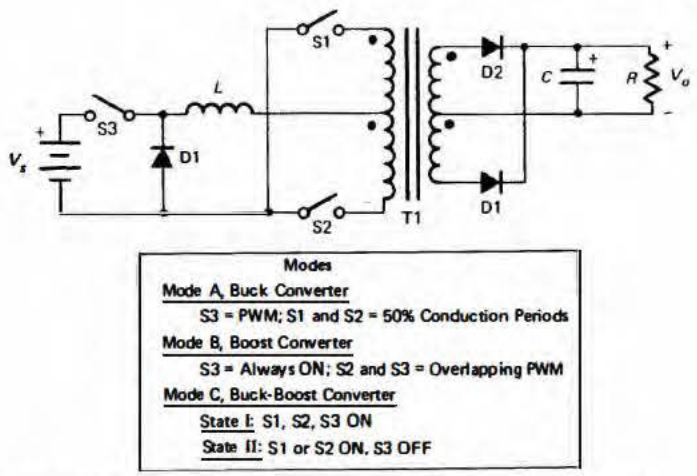


Fig. 9.14. The TRW converter operating in three different switching modes.

AND BOOST-DERIVED CONVERTERS *OR* THE SPC *MUST* BE ABLE TO ALTERNATE BETWEEN BUCK AND BOOST-DERIVED MODES OF OPERATION.

We can carry the process of altering the timing sequence even further to provide three modes of conversion operation as shown in Fig. 9.14. Here, by varying the switching sequence, a converter, shown earlier in Chapter 5 (Fig. 5.3A) can assume the characteristics of a buck, a boost or a buck-boost SPC.

9.4 APPLYING BILATERAL INVERSION TO COMPLEX CONVERTERS

The rules for bilateral inversion can be applied directly to more complex SPCs to evolve their duals and, in some cases, new converter structures will result. For example, Fig. 9.15A shows the parallel quasi-squarewave converter circuit of Chapter 4. Applying the rules of bilateral inversion to this SPC, the topology shown in Fig. 9.15B evolves and, by inspection, is the parallel overlapping-conduction boost converter of Chapter 5. Again, the existence of duality between contemporary buck and boost-derived converters becomes apparent.

In Fig. 9.16, we see that the dual of another buck-derived converter of Chapter 5 (Fig. 5.9A) is a flyback SPC in series with the output of a DC transformer (Fig. 9.16B). The input current of this dual topology is continuous in form, while its output current is discontinuous. These properties are to be expected since the dual of the SPC in Fig. 9.16A must be a boost-derived converter.

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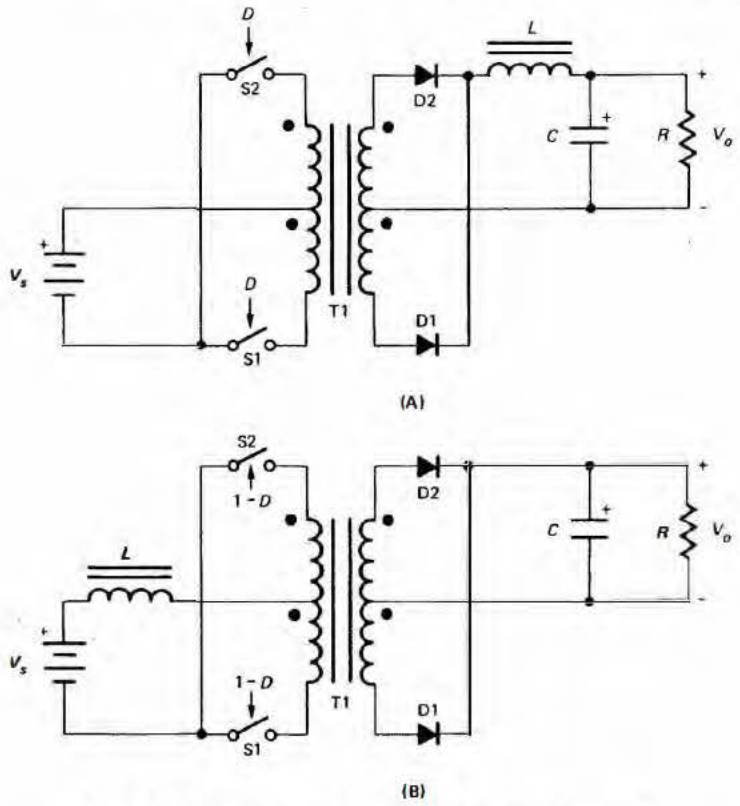


Fig. 9.15. Bilateral inversion of the quasi-squarewave converter.

Finally, in Fig. 9.17, we see that the dual to a boost-derived converter with a tapped primary winding (Fig. 8.20B) is a tapped secondary winding buck-derived SPC system as shown in Fig. 9.17B.

At this point, it is evident that, *for every known buck-derived converter, there exists a dual boost-derived converter, and vice versa*. Therefore, should new SPC topologies be conceived, their dual structures can easily be evolved using the methods of bilateral inversion. However, in some cases, a bilaterally-inverted network is identical to the original parent circuit. The Ćuk and buck-boost converters are prime examples of such exceptions. While these two particular converters have identically dual SPCs that result from bilateral inversion manipulation, we will soon see that applying general duality principles to these two SPCs will finally reveal the dual nature of their topologies.

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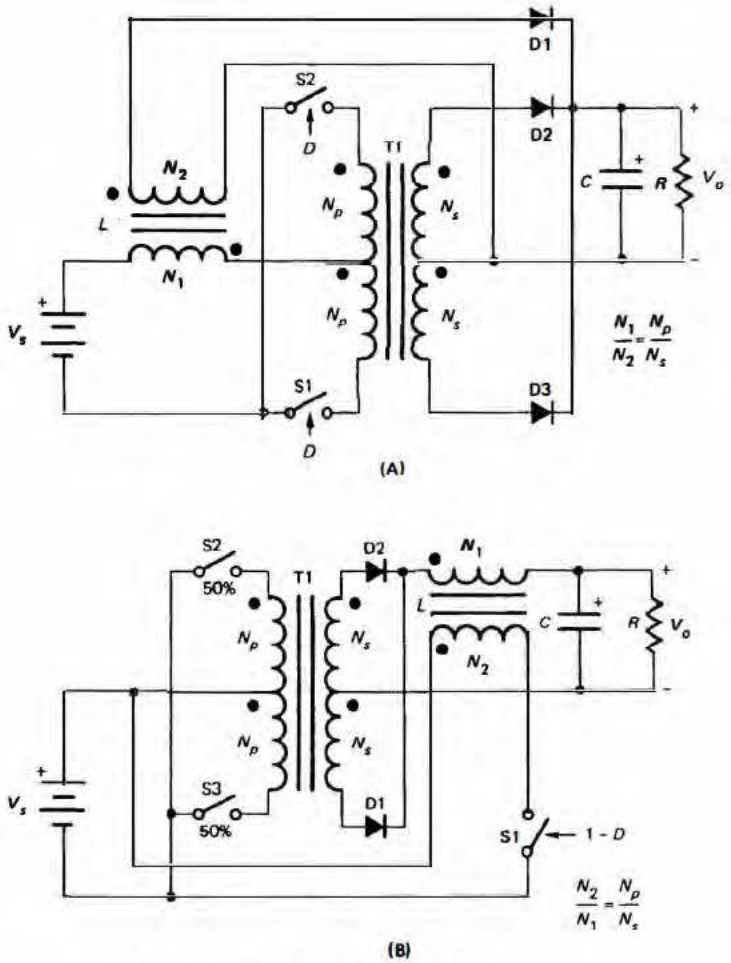


Fig. 9.16. Bilateral inversion of the Weinberg converter.

The previous three examples of this discussion concerned themselves with single-output converter structures. When bilateral inversion principles are applied to single-input multiple-output converter systems, the resultant dual SPCs will have a single-output and a multiple-input capability.

While converters with the capability of accepting inputs from more than one source of power are occasionally useful, the general rule for effective application of the principle of bilateral inversion is to reduce the SPC circuit to a single in-

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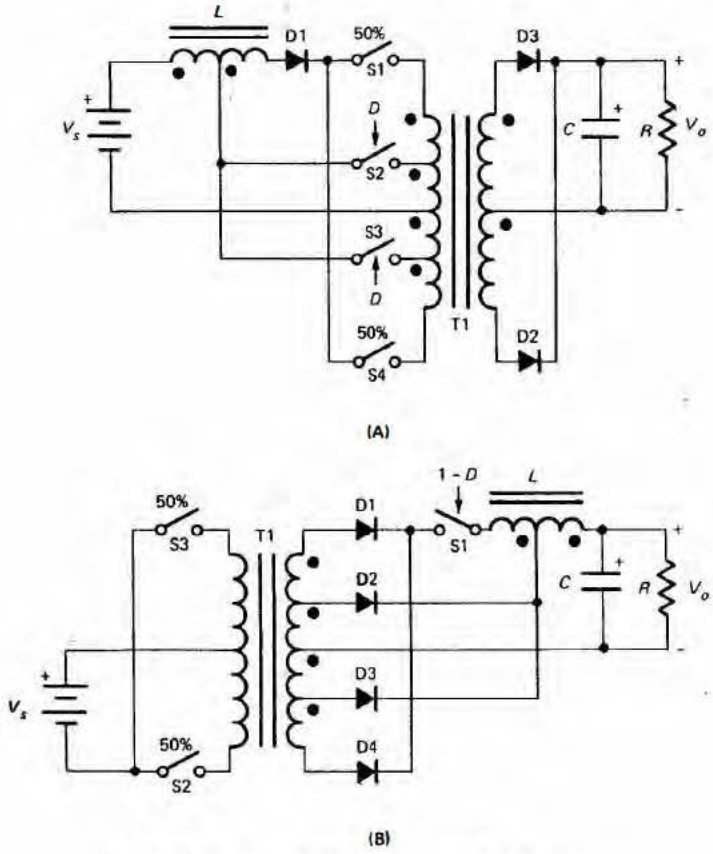


Fig. 9.17. Bilateral inversion of the Hughes circuit.

put and a single output, perform the inversion processes, and then arrange the number of inputs and outputs to suit the application need.

9.5 APPLYING THE GENERAL DUALITY PRINCIPLE TO SPC CIRCUITS

In the first four sections of this chapter, we have been discussing a very special and limited case of duality namely, bilateral inversion. In this section, we will expand our discussions to include the general concept of duality and how to apply it to SPC circuits.

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The duality principle is a fundamental concept in our understanding of nature and its application to electrical circuits is well established. However, most discussions of duality are limited to linear circuits or those with rather simple nonlinearities. Until the work by Ćuk [5], it was not clear how, or even if, it was possible to apply duality to SPC circuits, which are highly nonlinear. As we shall see, duality in its general sense can be applied to this class of circuits. Applying duality will provide us with an analytical method of simplifying the derivation of the properties of many converters. The insight gained into the relationships between SPC circuits will enable us to better judge the applicability of different converters.

Basically, Dr. Ćuk's approach is to reduce a converter circuit to a series of linear equivalent circuits for each switching state, much as we did when deriving the averaged small-signal models of Chapter 2. A dual network for each circuit state is then developed, and the resulting networks recombined into a single circuit. For many of us (the authors included), the principles behind duality of electrical networks were subjects introduced briefly in a college sophomore or junior network analysis course with little or no application in subsequent day-to-day work. So, before charging into an exposition of using duality in SPC circuits, we will stop to review the duality principle and related procedures for generating circuit duals. Of necessity, the subject discussions to follow are limited in scope, but most basic electrical network analysis textbooks provide more rigorous treatments for those readers who wish to delve deeper into duality principles.

In electrical networks, duality is usually limited to those linear circuits whose graphs are planar. A *graph G* is said to be *planar* if it can be drawn on a plane in such a way that no two branches cross at a point which is *not* a node. For example, the graph in Fig. 9.18A is planar while that of Fig. 9.18B is not.

In a planar graph, any closed loop which has no branches in its interior is called a *mesh*. In Fig. 9.18A, loops *a-b-e-a*, *c-d-e-c*, and *b-c-e-b* are meshes. A loop which contains no branches in its exterior is called an *outer mesh*. With these basic definitions in mind, we can now move to define what is meant by duality in graphs and then extend it to electrical circuits.

A graph G^* is said to be the dual of another graph G if the following three conditions are satisfied:

CONDITION 1. There is a one-to-one correspondence between all meshes of G and the nodes of G^*.

CONDITION 2. There is a one-to-one correspondence between all nodes of G and the meshes of G^*.

CONDITION 3. There is a one-to-one correspondence between the branches of each graph such that, whenever two meshes of one graph have

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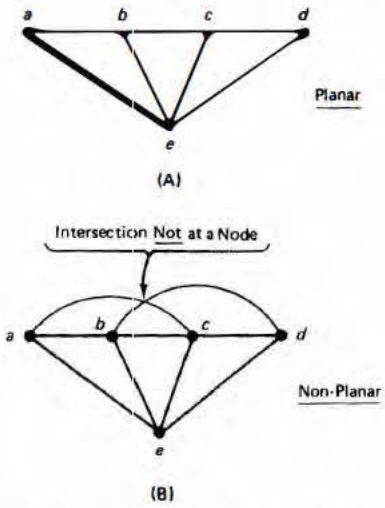


Fig. 9.18. Examples of planar and nonplanar graphs.

a branch in common, the corresponding nodes of the other graph have the corresponding branch connecting these nodes.

In analyzing electrical circuits, the direction of the assumed current flow in each branch is usually indicated. The graph of such a circuit is called an *oriented graph*, with a current direction indicated on each of its branches. For an oriented graph G, where each branch current has a reference direction, the orientation of the dual graph G^* can be obtained by rotating the current reference direction of each branch by 90° *clockwise* to obtain the current direction of the corresponding branch in G^*.

All of these rules sound very complex and formal, but as we see in Fig. 9.19, the actual process is quite simple. Here, an oriented graph is shown in Fig. 9.19 A. In Fig. 9.19B, we place a node inside each mesh including the outer mesh (nodes 1*, 2*, 3*, and 4*). Branches are then connected between the new nodes so that one branch of the new graph intersects each of the branches of the original one. We now have the dual graph as shown in Fig. 9.19C. From each intersection in the dual graph the orientation of the corresponding branch is then determined. For analysis convenience, it is common practice to draw similar circuits with the same layout format. In doing so, it is much easier for a designer to recognize the type of circuit being examined. It is quite possible to draw common converter circuits in a manner where their structures become unrecognizable. Sometimes, the process of generating the dual of a network results in a circuit

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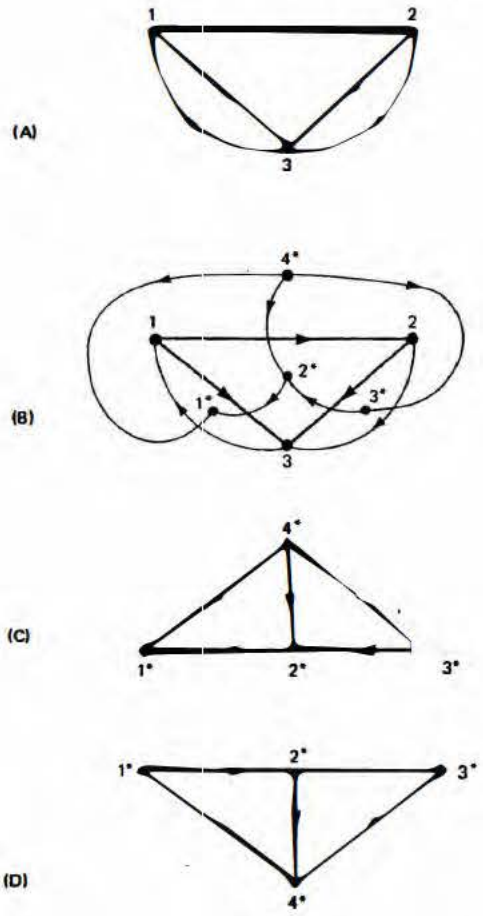


Fig. 9.19. Derivation of the dual of an oriented graph.

form which is not "standard" or easily recognizable. Usually simple drawing rotation or translation techniques will place the circuit in the proper perspective; however, it is often necessary to also mirror-image the circuit. An example of mirror-imaging is shown in Fig. 9.19D. Notice that the reference current direction of each branch of the mirror image must be reversed.

In an electrical network, each of its branches will contain circuit components with particular electrical characteristic, i.e., a resistor, an inductor, a current source, etc. Duality requires that the following transformations be made:

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$$v \rightarrow i^*, \quad i \rightarrow v^*, \quad q \rightarrow \phi^*, \quad \phi \rightarrow q^* \tag{9.1}$$

where v = branch voltage, i = branch current, q = branch charge, and ϕ = branch flux variation.

From elementary circuit theory, we know that for each branch:

$$\left\{ \begin{array}{ll} v = iR & v^* = i^*R^* \\ v = L\dfrac{di}{dt} & v^* = L^*\dfrac{di^*}{dt} \\ i = C\dfrac{dv}{dt} & i^* = C^*\dfrac{dv^*}{dt} \end{array} \right\} \tag{9.2}$$

From the relationships of Eq. (9.2), it can be shown that the corresponding branch duality relationships in Table 9.1 are true. The dual relationship for D^* is demonstrated in the next section of this chapter.

Let us now apply the relationships of Table 9.1 and the dual graphing procedure to the network N in Fig. 9.20A. The resulting dual network N^* (mirror-imaged) is shown in Fig. 9.20C.

The duality principle is actually much more general than the simple procedures outlined here would indicate. The principle of duality applied to dual networks can be stated as follows:

Consider an arbitrary planar network N and its dual N. Let S be any true statement concerning the behavior of N. Let S* be the statement obtained from*

TABLE 9.1. Branch Component Duality Relationships.

Quantity	Dual Element
v	i^*
i	v^*
q	ϕ^*
ϕ	q^*
R	$R^* = G = 1/R$
G	$G^* = R = 1/G$
C	L^*
L	C^*
Open circuit	Short circuit
Short circuit	Open circuit
D	$D^* = 1 - D$
Voltage generator	Current generator
Current generator	Voltage generator

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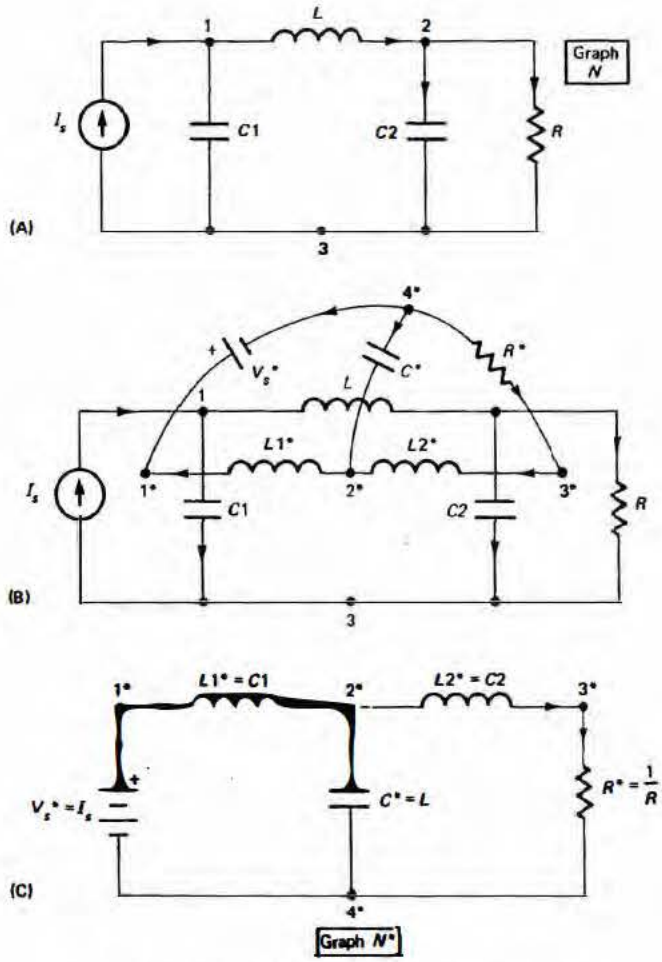


Fig. 9.20. Derivation of the dual of an electrical network.

S by replacing every graph-related word or phrase (node, loop, mesh, etc.) by its dual and every electrical quantity (voltage, current, impedance, etc.) by its dual. Then S is a true statement concerning the behavior of N*.*

Before proceeding to applying duality to SPC circuits, we need to take another look at the elementary buck and boost converter circuits. In Chapters 2 and 3, all of the basic converter circuits were shown with a voltage source at their in-

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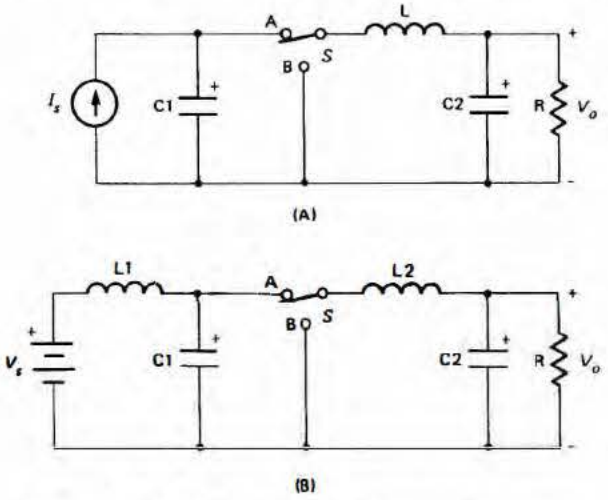


Fig. 9.21. The buck converter fed from a current source.

puts. We could also have used a current source as shown in Fig. 9.21A. Here, capacitor C1 has been added across the input current source so that the input voltage does not rise to infinity when switch S is in the B position. As a practical matter, SPCs very often have a "current source" at their inputs because of the common requirement for limiting the amount of conducted EMI noise seen by their input voltage sources. A typical example is shown in Fig. 9.21B where, to obtain a high degree of isolation from input current pulsations, an input low-pass filter (L1, C1) is added. The inductance of L1 is usually large and its current is essentially DC, since C1 provides the dynamic energy source for the SPC. This arrangement acts very much like a voltage-limited current-source. In Fig. 9.22, the four combinational possibilities of source and elementary converter topologies are indicated. Notice that we have tinkered a bit with the SPC circuits. In the buck converters (Fig. 9.22A and B), the output capacitors have been eliminated since their presence is not required for proper converter function, as was pointed out in Chapters 1 and 2. However, in the boost converters (Fig. 9.22C and D), the output capacitor (C2) is required and so it has been retained. Another change indicated is the addition of a capacitor (C1) across each of the voltage sources. From a circuit function point of view, this capacitor serves no real purpose, since the voltage sources are assumed to have zero impedance. The reason for adding C1 is a matter of practicality in the application of duality principles to SPC systems. As we will soon see, its presence will lend credibility to the existence of many dual SPCs. The reader may notice that, by removing

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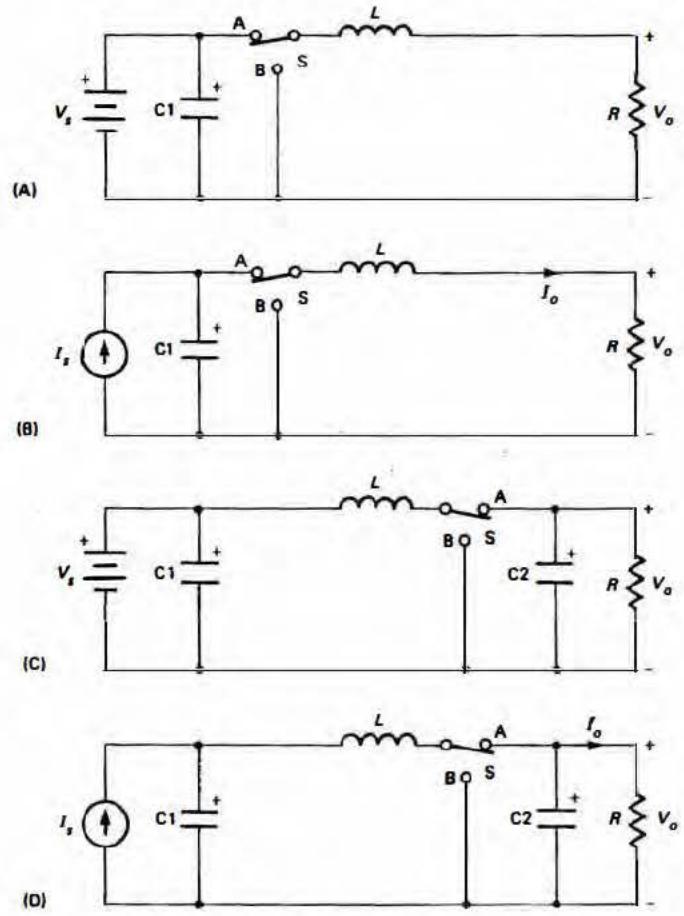


Fig. 9.22. Current and voltage source possibilities with the buck and boost converters.

the loads and sources from the circuits of Fig. 9.21, the buck circuits are mirror images of the boost circuits. In order to apply duality to SPC circuits and obtain meaningful results, it is necessary to manipulate the circuits in this manner.

Looking again at Fig. 9.22, we see that circuit A is a normal buck converter since $V_o/V_s < 1$, this SPC can be called a *buck-voltage* converter. For circuit B, $I_o/I_s > 1$, hence, we can call this SPC a *boost-current* converter. Circuit C is a *boost-voltage* converter, since $V_o/V_s > 1$, but circuit D is a *buck-current* converter since $I_o/I_s < 1$. We will use these four names in the duality discussions to fol-

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low, but we will not expand the number of basic converter types from two to four since there seems to be no practical or advantageous reason to do so, at this time at least. Nearly all converters in use today are voltage converters that provide regulated output voltages. Applications where the primary function of the converter is to provide a regulated output current do exist, but are relatively low in number. For such rare applications, it would be interesting and perhaps very useful to restate the voltage-converter-oriented presentations of this book in terms related to current conversion. The duality principle is the most convenient and efficient means to do this. However, because of our stated limitation of scope of subject matter, the authors leave current-conversion examinations as duality exercises for the reader.

We are now ready to apply duality methods to some of the common converter circuits of earlier chapters.

9.6 APPLYING DUALITY TO SPC CIRCUITS

Consider the circuit in Fig. 9.23A which is a current-boost converter or, if you prefer, a buck-voltage converter with a voltage-limited current input source. If we presume the continuous mode of operation, then there are two equivalent linear circuits that correspond with the two switch positions A and B. The circuits resulting from these two switch states are shown in Fig. 9.23B. Since these circuits are linear, we can apply the principles of duality directly using the rules and procedures developed in the previous section of this chapter. This is indicated in Fig. 9.23B, with the final results shown in Fig. 9.23C. The two dual linear circuits can now be reunited with switch S positioned as shown in Fig. 9.23D. Note that this SPC is a boost converter. Once again, it becomes apparent that the boost converter is the dual of the buck converter, just as we found when bilateral inversion techniques were applied. By convention, switch conduction duty cycle (D) in the buck converter is defined as the portion of the total switching interval (T_s) that switch S is in position A. However, for the boost converter, D is the portion of T_s that S is in the B position. From this observation, we can immediately see the origin of the dual transformation definition, $D^* = 1 - D$, given earlier in Table 9.1. These duty cycle conventions are simply the result of the normal realization of the SPDT switch by the use of a diode and a transistor and subsequently defining D as the ON time of the transistor.

For the current source buck regulator of Fig. 9.23A, it can be shown that:

$$\frac{I_o}{I_s} = \frac{1}{D} . \tag{9.3}$$

From the rules for duality developed earlier, we know that:

$$I_o \rightarrow V_o^* \tag{9.4}$$

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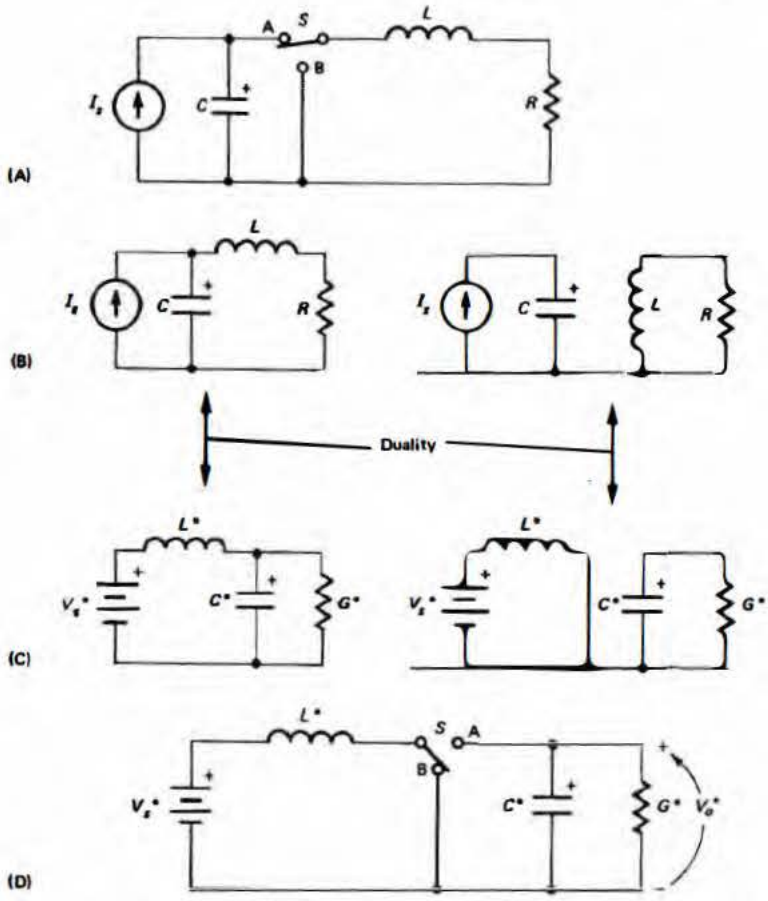


Fig. 9.23; The duality relationship between buck and boost converters.

$$D \rightarrow D^* = 1 - D \tag{9.5}$$

$$I_g \rightarrow V_g^*. \tag{9.6}$$

Therefore:

$$M = \frac{V_o^*}{V_g^*} = \frac{1}{1 - D}. \tag{9.7}$$

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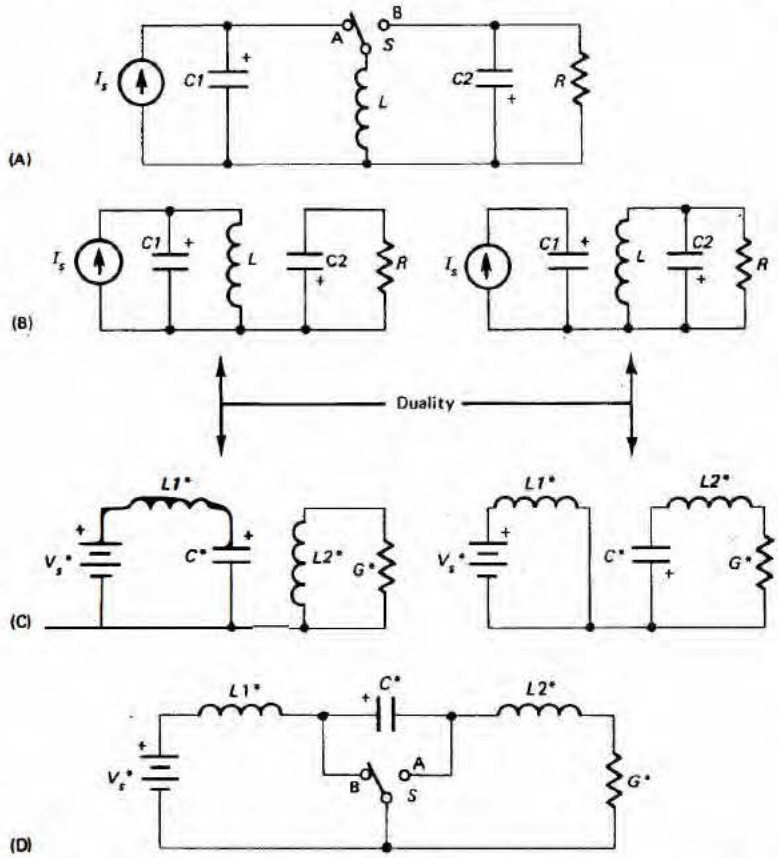


Fig. 9.24. The duality relationship between the Ćuk and the buck-boost converters.

We have already established the gain relationship indicated by Eq. (9.7) in Chapter 3 by a completely separate (and more involved) circuit analysis method. We could have applied the principle of duality to the buck converter of Chapter 2 and derived the characteristics of the boost converter directly with much less analysis effort. This example illustrates the power of the duality principle.

We can now introduce the following key idea related to SPC characteristics and duality:

KEY IDEA #7

IF WE KNOW THE PROPERTIES OF A GIVEN SPC CIRCUIT, WE CAN DERIVE THE PROPERTIES OF THE DUAL OF THE

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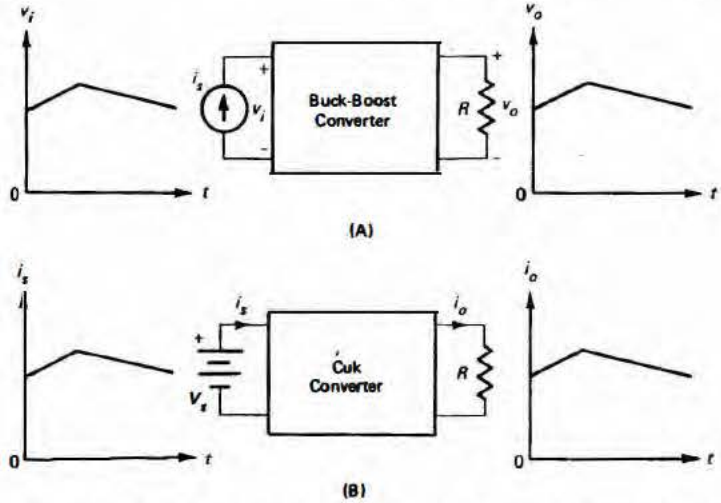


Fig. 9.25. Duality of the input and output voltages and currents in buck-boost and Ćuk converters.

SPC BY APPLYING THE RULES OF DUALITY TO THE ORIGINAL CONVERTER PROPERTIES. ALL OF THE PROPERTIES OF THE DUAL CONVERTER WILL BE DUALS OF THOSE OF THE ORIGINAL SPC.

Let us now apply duality to a more complex converter. Fig. 9.24A shows a buck-boost converter with a current source input. By following the duality steps indicated in Fig. 9.24B and C, we arrive at the dual converter of Fig. 9.24D, which is none other than the Ćuk converter. The Ćuk and the buck-boost are therefore dual SPCs. Interestingly enough, if the Ćuk converter approach had not been conceived by quite a different process (see Chapter 7, Fig. 7.6) it would have appeared quite naturally from the application of duality principles to the buck-boost converter.

In Fig. 9.25, note that the nonpulsating nature of input and output voltage waveforms in the buck-boost converter is transferred to the input and output currents in the dual Ćuk converter. The nonpulsating nature of the input and output currents is a major advantage of the Ćuk converter.

9.7 DUALITY IN INDUCTIVE AND CAPACITIVE ENERGY TRANSFER

In earlier chapters, we made much ado about the central role played by inductor current in determining the operating mode of an SPC. In most converters, it is

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the inductor which transfers the energy from the input to the output. The Cuk converter is unique in this respect in that it uses a capacitor to transfer energy from the input to the output as well as inductive energy storage. From the principle of duality, we know that the dual to an inductor current will be a capacitor voltage. In the Cuk converter, the capacitor voltage can be either continuous or discontinuous. Since the capacitor is an active part of this SPC's energy transfer mechanism, the conduction mode of the capacitor voltage is just as fundamental in determining the converter properties as its inductor's conduction modes. Readers interested in a more detailed discussion of the phenomena of discontinuous capacitor voltage in a Ćuk converter are referred to Ref. 5 in the bibliography of this text.

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10. Small-Signal Models of Complex Converters and Regulators

In Chapters 2 and 3, a great deal of effort was expended in the generation of equivalent circuit as well as mathematical models for the basic buck and boost converters. In subsequent chapters, a multitude of SPC circuits were derived, for the most part, from these two elementary converters. Throughout the development of these more complex SPCs, we have been very careful to keep track of their basic constituents, i.e., whether they were buck-derived, boost-derived, or some combination thereof. One of the many reasons for carefully identifying their basic constituents is that by doing so, we can quickly determine which of the basic SPC models of Chapters 2 and 3 apply to any given converter. As will be evident in this chapter, this recognition capability greatly reduces the effort in analyzing a given SPC circuit.

Up to this point, we have treated all of the SPC circuits by themselves and ignored the fact that most converters are normally used in conjunction with other electronic networks to realize a voltage-regulating system. An important exception to this viewpoint was the development of small-signal circuit models that provided for external dynamic control of duty cycle. In this chapter, we will present some SPC examples in which voltage regulation and EMI filter networks are included. These examples will serve to demonstrate the flexibility and the power of small-signal modeling techniques for SPC systems.

10.1. THE CANONICAL MODEL

In Chapters 2 and 3, small-signal models for the buck and boost converters were developed for two distinct conduction modes. The conduction modes were defined as continuous and discontinuous, and reflected the nature of the current waveform within the inductor of these SPCs. For each conduction mode, we found that the small-signal describing equations and the equivalent circuit models had the same form for both buck and boost converters. The differences between each SPC model were the component values of network elements of the circuit

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model and corresponding constants in the circuit equations. These observations bring us to a key generalization for modeling SPCs:

Key Idea #8

THE SMALL-SIGNAL CIRCUIT MODEL OF ANY SPC FOR A *GIVEN CONDUCTION MODE* CAN HAVE THE SAME TOPOLOGY AND TYPE OF CIRCUIT ELEMENTS. THE VALUES ASSIGNED TO EACH CIRCUIT ELEMENT OF THE COMMON MODEL TOPOLOGY ARE DEPENDENT ON INDIVIDUAL CONVERTER PROPERTIES.

This generalization allows us to make a rather spectacular simplification in the analysis of SPC circuits, since we will now know beforehand what the structure of the model will look like. The analysis problem then reduces to one of calculation of model element values using standard techniques of linear circuit theory.

Our general small-signal model will be called the *canonical model* and is patterned after that conceived by Drs. Middlebrook and Ćuk (Ref. 6). By necessity, separate canonical models for each conduction mode are required. The canonical model for the continuous mode is given in Fig. 10.1. For convenience, various element impedances or characteristics are expressed in terms of complex frequency, i.e., the s domain. To further simplify the equations of this presentation, we will omit the explicit expression of s in such instances and let it be implicit. For example, $d(s)$ will be written as d.

We see that the model of Fig. 10.1 is divided into three sections, each representing the functions inherent in an SPC. The first box represents the small-signal control properties due to $\hat{d}$, the second box represents the inherent DC

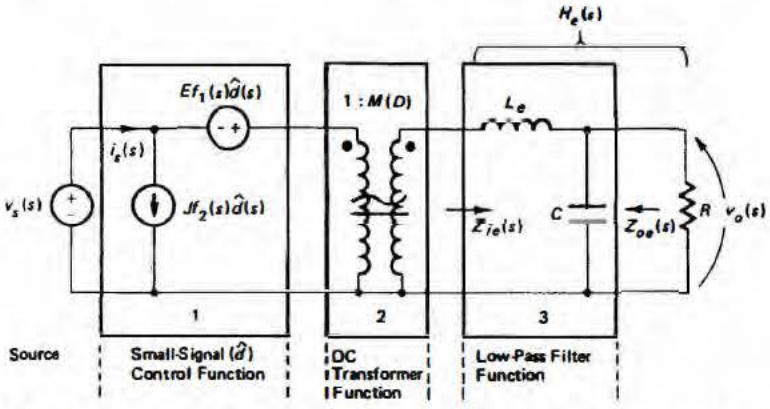


Fig. 10.1. The small-signal canonical model for converter operation in the continuous mode.

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transformation function of the converter to be modeled ($M(D)$), and the third box represents the effective output low-pass filter network of the SPC. As defined in Chapters 2 and 3, M is the ideal ratio of V_o/V_s for the SPC to be modeled. The correction factor that accounts for the *nonideal* value of M (i.e., efficiency of power conversion), is included in the transfer function, H_e. The filter network, shown in the third box of Fig. 10.1, represents only one of an infinite variety of possibilities. The only constraints placed on this filter network are the need to exhibit a *low-pass* characteristic and, of course, that it correctly represent the effective filter circuit elements of the converter under consideration. As we shall see in the next section of this chapter, this equivalent low-pass filter network can become quite complex. Like any linear filter circuit, it can be characterized by its input-to-output voltage-transfer ratio (H_e), its input impedance (Z_{ie}) and its output impedance (Z_{oe}). Note that the converter's load (R) must be included in the determination of H_e and Z_{ie}. Also, any source impedances must also be included in Z_{oe}, suitably transformed through the DC transformation function of the second box in Fig. 10.1. Having a single model such as this for *all* converters can be extremely useful in the day-to-day design of SPC circuits. The following analysis advantages come immediately to mind.

First of all, an ever-increasing number of designers are using computer-aided methods to perform circuit analyses. By using a single universal model topology like the canonical form of Fig. 10.1, it is only necessary to write one computer analysis program for the model topology, inserting different values for the circuit elements of the model to examine the small-signal characteristics of *any* converter desired.

Second, the differences in small-signal characteristics of converters can easily be examined by comparing associated canonical model element values. For example, the range of D can be derived directly from MH_e (0) (i.e., the product of M and the DC transfer function of the output filter), the range of input voltage (V_s), and variation in load resistance (R). Another example would be the comparison of control-to-output transfer functions of buck and boost SPCs. Here, the value of $f_1(s)$ in Fig. 10.1 will be equal to 1 for the buck converter. However, in the boost model, $f_1(s)$ will be complex and contain a *right* half-plane zero.

Thirdly, low-pass filter networks of SPC models can be compared in order to estimate their relative filtering capability for a given amount of signal attenuation desired.

There remains, of course, the analysis problem of determining canonical model element values for an SPC. There are two ways one can approach this problem. One method is to manipulate the equivalent circuit model and, very often, this can be done by simple inspection. In the next section of this chapter, we will give several examples of this inspection procedure. The second approach for determining model element values is to directly manipulate the circuit equations that describe features of an SPC. Looking at the canonical model in Fig. 10.1, we can write by inspection that:

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$$\hat{v}_o = (\hat{v}_s + Ef_1\,\hat{d})\,MH_e \tag{10.1}$$

$$\hat{i}_s = Jf_2\,\hat{d} + (Ef_1\,\hat{d} + \hat{v}_s)\,\frac{M^2}{Z_{ie}}\,. \tag{10.2}$$

Eqs. (10.1) and (10.2) can be rearranged so that:

$$\hat{v}_o = (MH_e)\,\hat{v}_s + (Ef_1\,MH_e)\,\hat{d} \tag{10.3}$$

$$\hat{i}_s = \left(\frac{M^2}{Z_{ie}}\right)\hat{v}_s + \left(Jf_2 + \frac{M^2 Ef_1}{Z_{ie}}\right)\hat{d}\,. \tag{10.4}$$

These equations can be further simplified by stating that:

$$\hat{v}_o = G_{vs}\hat{v}_s + G_{vd}\hat{d} \tag{10.5}$$

$$\hat{i}_s = G_{is}\hat{v}_s + G_{id}\hat{d} \tag{10.6}$$

Using Eqs. (10.3) through (10.6), we can derive expressions for the canonical model circuit elements:

$$Ef_1 = \frac{G_{vd}}{G_{vs}} \tag{10.7}$$

$$Jf_2 = G_{id} - Ef_1\,G_{is} \tag{10.8}$$

$$H_e = \frac{G_{vs}}{M}\,. \tag{10.9}$$

The ideal SPC voltage gain function has already been determined as:

$$M = \frac{V_o}{V_s}\ \text{(IDEAL)}\,. \tag{10.10}$$

Further, if we define f_1 and f_2 such that:

$$f_1(0) = f_2(0) = 1\,, \tag{10.11}$$

then expressions for both E and J in the model can be readily determined.

The procedure for determining the canonical model element values is quite straightforward and can be stated as follows:

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STEP 1. Derive the SPC equations using state-space averaging procedures, being careful to include $\hat{v}_o$ and $\hat{i}_s$ in any resulting expressions.

STEP 2. Rearrange the circuit equations of Step 1 so that they assume the form of those shown by Eqs. (10.5) and (10.6).

STEP 3. Solve for the element values of the small-signal model using Eqs. (10.7) through (10.11).

By way of an example of this three-step procedure, we will now develop the small-signal canonical model for the ideal buck-boost converter shown in Fig. 10.2A. Notice here the output voltage (v) has been defined as "positive" with respect to the common return of the SPC, even though the DC output voltage of the buck-boost converter is actually inverted (see Chapter 7). The "positive" convention is used here to be consistent with the format of the canonical model and, if our procedure is valid, the SPC's inversion property should appear in the final model as a natural consequence. The continuous mode will be assumed so that the converter must have two switching states, as shown in Figs. 10.2B and C. Applying the state-space averaging procedure to these two networks, we find from the DC relationships that:

$$M = -\frac{D}{D'} \tag{10.12}$$

which clearly indicates the inverting nature of the converter.

The small-signal equations of the averaged SPC are:

$$\frac{d\hat{i}}{dt} = \left[\frac{D'}{L}\right]\hat{v} + \left[\frac{D}{L}\right]\hat{v}_s - \left[\frac{V}{LD}\right]\hat{d} \tag{10.13}$$

$$\frac{d\hat{v}}{dt} = -\left[\frac{D'}{C}\right]\hat{i} - \left[\frac{1}{RC}\right]\hat{v} - \left[\frac{V}{D'RC}\right]\hat{d} \tag{10.14}$$

$$\hat{v}_o = \hat{v} \tag{10.15}$$

$$\hat{i}_s = \hat{i}D - \left[\frac{V}{RD'}\right]\hat{d}. \tag{10.16}$$

We can now transform these equations into the complex frequency domain and rearrange them into the forms of Eqs. (10.5) and (10.6). As a result of this transformation:

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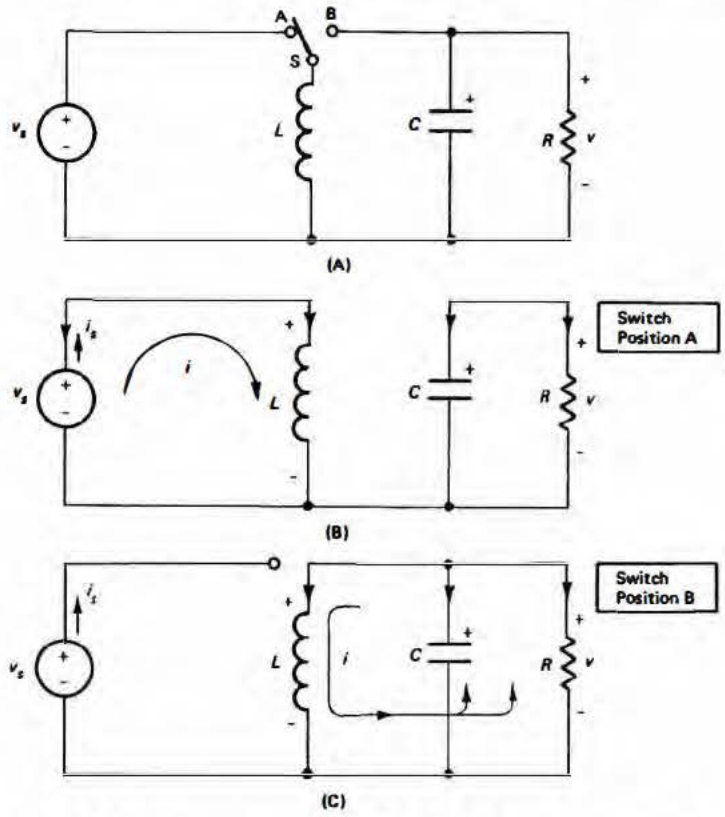


Fig. 10.2. Buck-boost converter equivalent circuits for the continuous mode.

$$\hat{v}_o = \left(-\frac{D}{D'}\right)\left[\frac{1}{1 + s(L_e/R) + s^2 L_e C}\right]\hat{v}_s + \left(\frac{V}{DD'}\right)\left[\frac{1 - s(L_e D/R)}{1 + s(L_e/R) + s^2 L_e C}\right]\hat{d} \qquad (10.17)$$

$$\hat{i}_s = \left[\frac{D^2}{R(D')^2}\right]\left[\frac{1 + sRC}{1 + s(L_e/R) + s^2 L_e C}\right]\hat{v}_s - \left[\frac{V}{R(D')^2}\right]\left[\frac{1 + D + sRC}{1 + s(L_e/R) + s^2 L_e C}\right]\hat{d} \qquad (10.18)$$

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where

$$L_e = \frac{L}{(D')^2} \tag{10.19}$$

By using Eqs. (10.7) through (10.12), the canonical circuit elements appear as:

$$E = \frac{-V}{D^2} \tag{10.20}$$

$$f_1 = 1 - \frac{sL_eD}{R} \tag{10.21}$$

$$J = -\frac{V}{R(D')^2} \tag{10.22}$$

$$f_2 = 1 \tag{10.23}$$

$$H_e = \frac{1}{1 + s(L_e/R) + s^2L_eC} \tag{10.24}$$

Looking at the expression for H_e in Eq. (10.24), it is very evident that this transfer function is characteristic of a single-section LC low-pass filter. Finally, the continuous mode small-signal model for the buck-boost converter is constructed, using the element values given above. The complete model is shown in Fig. 10.3, where the corresponding "negative" values of E and J are represented

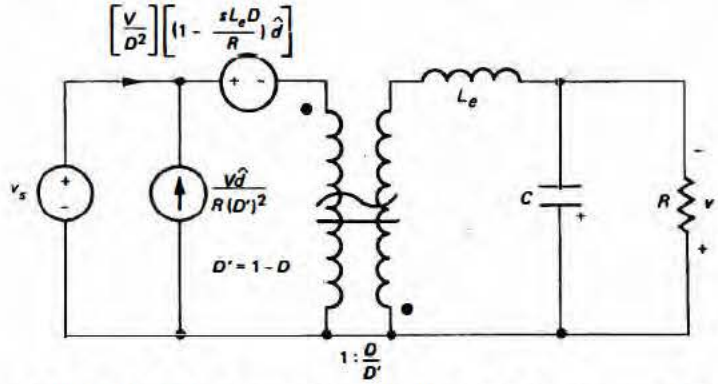


Fig. 10.3. The buck-boost converter small-signal model for the continuous mode.

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by voltage and current generators of reverse polarity. In a similar fashion, the "negative" nature of the value for M is represented by inverting the winding relationships of the transformer within the model.

In Chapter 7, we demonstrated that the buck-boost SPC could be derived from a cascade connection of a basic buck converter followed by a basic boost converter, if an inversion of the output voltage polarity was acceptable. Table 10.1 gives a comparison of the element values for the small-signal canonical models of the buck, boost, and buck-boost converters. Notice that the element properties of the buck and boost converters are clearly related to those of the buck-boost converter. This observation is another confirmation of Key Idea #3 given in Chapter 1.

In an analogous manner, we can use a canonical model to represent the small-signal characteristics of an SPC operating in the discontinuous mode. The general form of this model is shown in Fig. 10.4. The procedure to develop element values for the discontinuous model follows in much the same manner as that given earlier for the continuous mode.

Table 10.2 gives the discontinuous model element values for the buck, boost, and buck-boost converters. Note also that the values of j_1 and j_2 in the case of the buck-boost are dependent on output DC voltage *magnitude* only.

TABLE 10.1. Comparison of Buck, Boost, and Buck-Boost Model Element Values.

Element	Buck	Boost	Buck-Boost
M	D	$\frac{1}{D'}$	$-\frac{D}{D'}$
E	$\frac{V}{D^2}$	V	$-\frac{V}{D^2}$
J	$\frac{V}{R}$	$\frac{V}{R(D')^2}$	$-\frac{V}{R(D')^2}$
f_1	1	$1-\frac{sL_e}{R}$	$1-\frac{sL_eD}{R}$
f_2	1	1	1
L_e	L	$\frac{L}{(D')^2}$	$\frac{L}{(D')^2}$

$D' = 1 - D$

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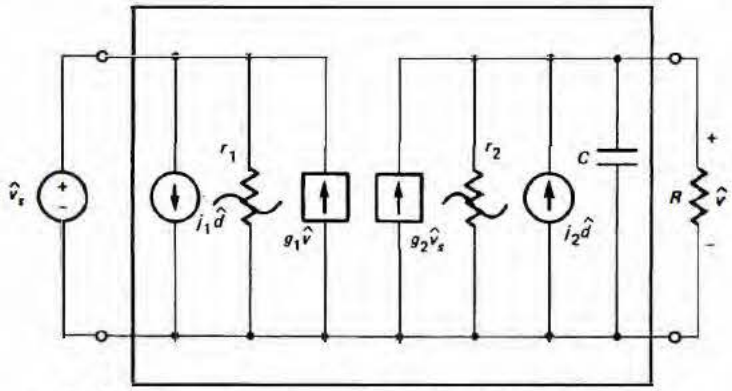


Fig. 10.4. The small-signal canonical model for the discontinuous mode.

10.2 MODELS FOR COMPLEX CONVERTERS

For most converter circuits, it is not necessary to go through the lengthy and somewhat complex mathematical derivations that were performed in the examples of the last section. The equivalent small-signal circuit model can usually be deduced from a knowledge of its derivative basic converter along with a little bit of manipulation of the canonical model to add any new circuit features of the SPC under analysis.

In Chapter 5, it was shown that the quasi-squarewave converter was derived by inserting a DC transformer into a basic buck converter (Figs. 5.12, 5.13). To derive the idealized small-signal canonical model for the quasi-squarewave converter, it is only necessary to add the DC transfer function to the canonical model for the buck converter. This addition is shown in Fig. 10.5A, where N represents the turns ratio of the DC transformer. This model can be simplified further by simply merging the two transformer functions into one element as shown in Fig. 10.5B.

The presence of a second transformer element in Fig. 10.5A will modify the E and J factors of the model by its turns ratio, N. These changes are needed as this second transformer will reflect the model's DC output voltage and load resistance by factors of $(1/N)$ and $(1/N)^2$, respectively.

Table 10.3 gives comparisons between model element values for the buck converter, its quasi-squarewave offspring, plus those for a two-output SPC of the same kind. For a quasi-squarewave converter with more than one output, the model development process is still basically the same but one additional step must be added. Fig. 10.6A shows an example of the development of a small-signal model for a dual-output quasi-squarewave SPC. The first step in reducing

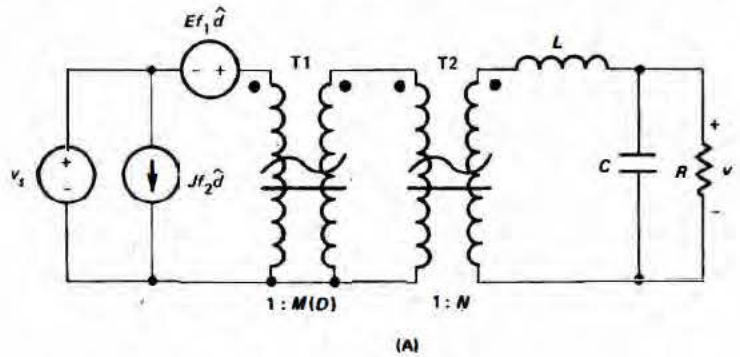
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TABLE 10.2. Element Definitions for Model of Fig. 10.4.

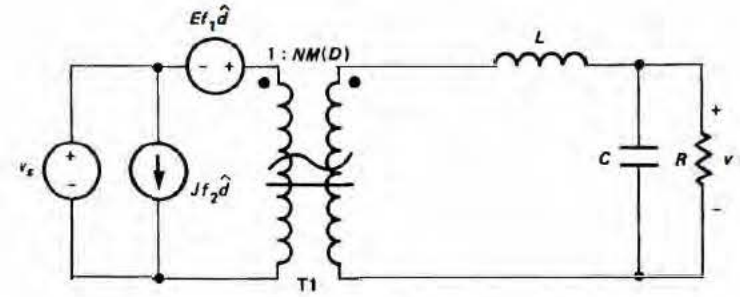
SPC Type	M	j_1	r_1	g_1	j_2	r_2	g_2
Buck	$\frac{2}{1+\sqrt{1+8\tau_L/D^2}}$	$\frac{2V}{R}$	$\left[\frac{1-M}{M^2}\right]R$	$\left[\frac{M^2}{1-M}\right]\frac{1}{R}$	$\frac{V}{RM}\sqrt{\frac{2(1-M)}{\tau_L}}$	$(1-M)R$	$\frac{M(2-M)}{(1-M)R}$
Boost	$\frac{1+\sqrt{1+2D^2/\tau_L}}{2}$	$\frac{V}{R}\sqrt{\frac{2M}{\tau_L(M-1)}}$	$\left[\frac{M-1}{M^3}\right]R$	$\left[\frac{M}{M-1}\right]\frac{1}{R}$	$\frac{V}{RM}\sqrt{\frac{2M}{\tau_L(M-1)}}$	$\left[\frac{M-1}{M}\right]R$	$\frac{M(2M-1)}{(M-1)R}$
Buck-Boost	$\frac{D}{\sqrt{2\tau_L}}$	$\frac{\sqrt{2}\lvert V\rvert}{R\sqrt{\tau_L}}$	$\frac{R}{M^2}$	0	$\frac{\lvert V\rvert}{RM}\sqrt{\frac{2}{\tau_L}}$	R	$\frac{2M}{R}$

$\tau_L = L/RT_s = Lf_s/R$
D = switch conduction duty cycle

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(A)



(B)

Fig. 10.5. Derivation of the small-signal continuous-mode model for the quasi-squarewave converter.

TABLE 10.3. Buck-Derived Model Element Comparisons.

Element	Basic Buck	Single-Output Quasi-Squarewave	Dual-Output Quasi-Squarewave
M	D	nD	n_1D
E	V/D^2	V/nD^2	V_1/n_1D^2
J	V/R	nV/R	$(n_1V_1)/(R1\|\|(n_1/n_2)^2R2)$
f_1	1	1	1
f_2	1	1	1

n, n_1, n_2 transformer turns ratios
$\|\|$ in parallel with.

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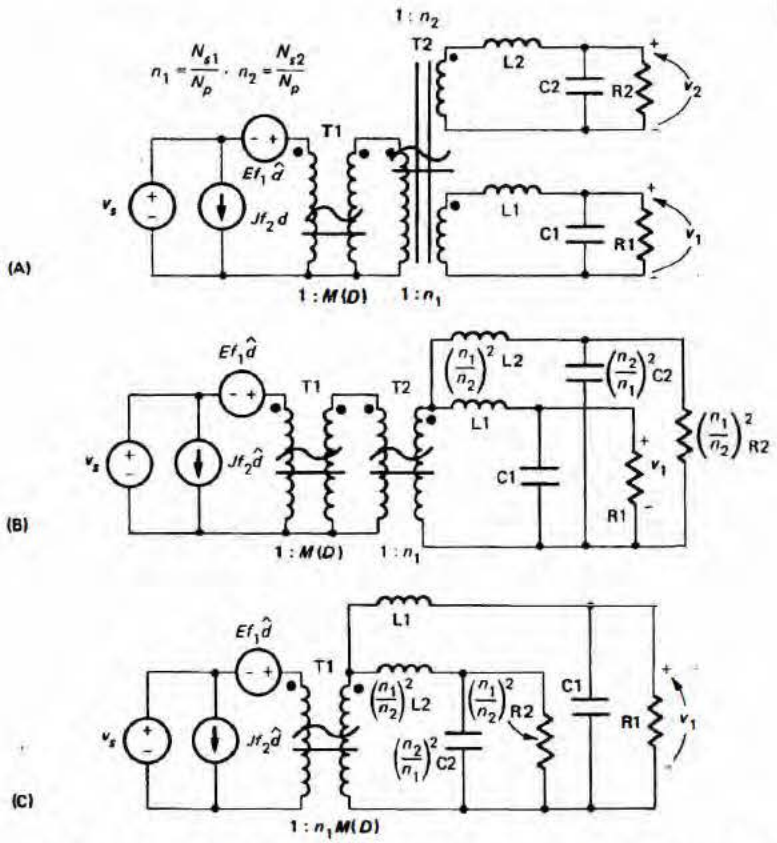


Fig. 10.6. Derivation of the small-signal continuous-mode model for a multiple-output quasi-squarewave converter.

the model of Fig. 10.6A is the transformation of the circuit elements on winding N_{s2} to winding N_{s1}, as is done in Fig. 10.6B. We can then combine the two transformer functions as was done in the last example in order to arrive at the final model in Fig. 10.6C. Normally, the reason for deriving the small-signal model of an SPC is to facilitate analyses that examine the stability effects of adding a voltage control feedback system associated with one of the outputs. To represent the power converter model as an element in an overall control system, Fig. 10.6C can be redrawn as shown in Fig. 10.7. In particular, notice here that the equivalent low-pass filter network is quite different from that of a single-output case as the low-pass filter elements associated with winding N_{s2} reflect

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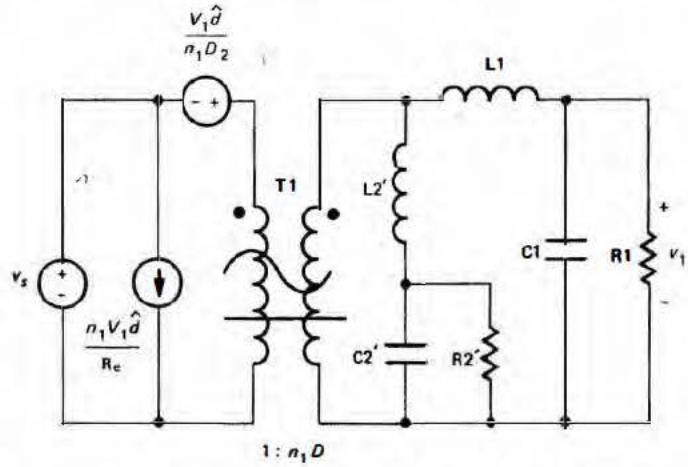


Fig. 10.7. Multiple-output quasi-squarewave converter model reorganized.

as shunt elements at the input of the low-pass filter connected to winding N_{s1}! The control-to-output transfer function of this multi-output SPC can be quite different from that of its parent, the buck converter, when a nonzero input impedance is present. This transfer function change must be taken into account if proper stability of output voltage control is to be achieved. This example points out once again the great power and utility of the canonical small-signal models.

The complexity of the low-pass filter in this example is not characteristic of all small-signal models of multi-output buck-derived circuits. As an example, the small-signal model for the dual-output converter of Fig. 5.6B in Chapter 5 is shown in Fig. 10.8A. Again, the number of windings on T2 are reduced by transforming the components of winding N_{s2} to positions associated with winding N_{s1}. Next, we move inductor L to the secondary of T2 and then combine the functions of T1 and T2. The final model of this SPC is shown in Fig. 10.8B. In this model, notice that its low-pass filter retains the simple single-section LC characteristic of the basic buck converter model.

Continuing the simple process of SPC model development, let us turn now to examples of boost-derived converters. It was demonstrated in Chapter 6 (Fig. 6.4) that the overlapping-switch-conduction family of SPCs were derived by inserting a DC transformer into a basic boost converter. Knowing this, we can immediately draw the model of Fig. 10.9A. This network can be further simplified as that shown in Fig. 10.9B by translating inductor L to the secondary

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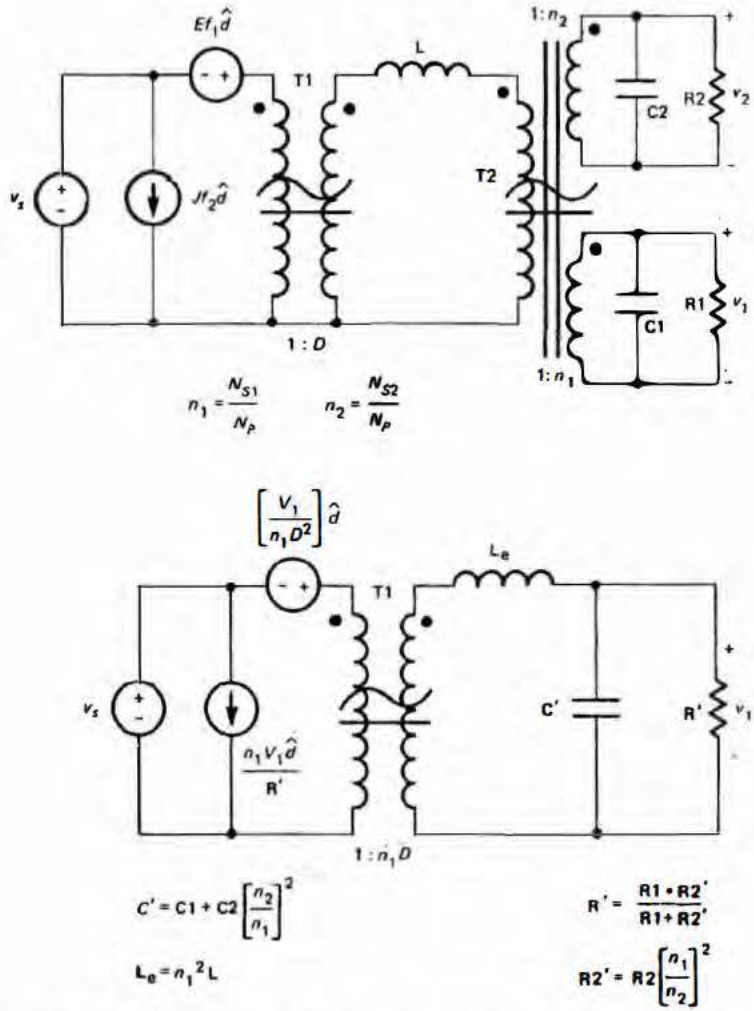
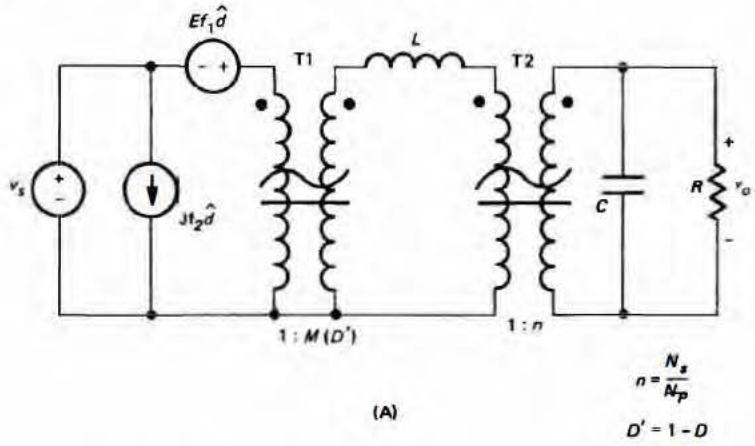


Fig. 10.8. Derivation of the small-signal continuous-mode model for a multiple output Cronin converter.

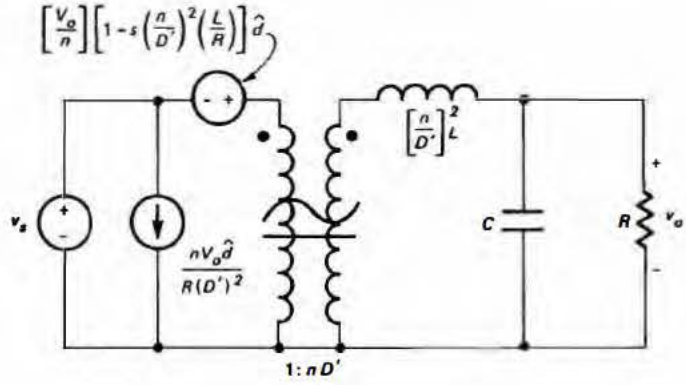
side of T2 and then combining the function of T1 and T2 into one transformer element.

When a converter circuit uses a tapped inductor or transformer, the derivation of its small-signal model can be somewhat more involved. For example, if a

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(A)



(B)

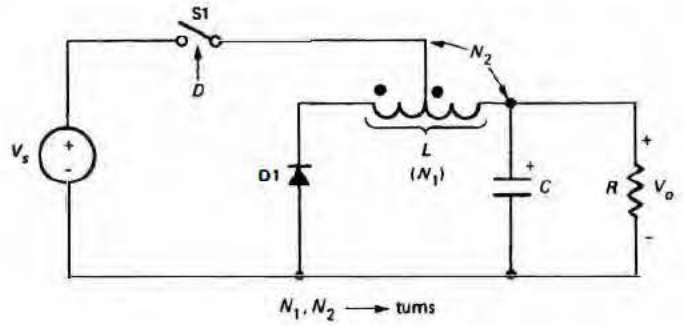
Fig. 10.9. The small-signal continuous-mode model for the Clark circuit.

tapped inductor is used in a buck converter as shown in Fig. 10.10A, the corresponding small-signal model will change as indicated in Fig. 10.10B, where:

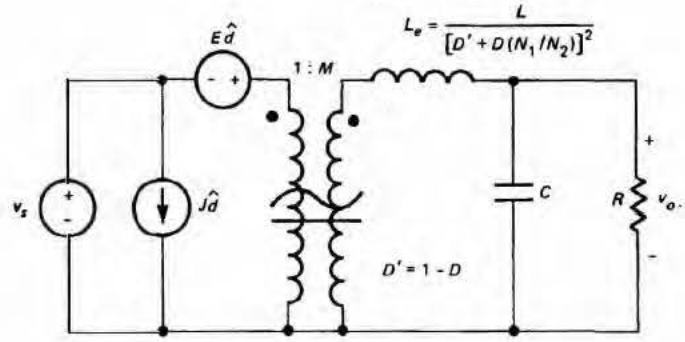
$$L_e = \frac{L}{[D' + D(N_1/N_2)]^2}. \tag{10.25}$$

In this example, in exchange for reducing the voltage across S1, the input voltage generator now has a zero dependent on R, L_e, and D. Also, the poles

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(A)



$$E = \left[\frac{V_o}{D^2}\right]\left[\frac{N_2}{N_1}\right]\left[1 + s\left(\frac{DL_e(N_1 - N_2)}{N_2 R}\right)\right]$$

$$J = \left[\frac{V_o}{R}\right]\left[\frac{N_1}{N_2}\right]\left[\frac{1}{[D' + D(N_1/N_2)]^2}\right]$$

$$M = \frac{D}{D + D'(N_2/N_1)}$$

(B)

Fig. 10.10. The small-signal continuous-mode model for a tapped-inductor buck converter.

of the model's low-pass filter will now vary as a function of D because of the dependence of L_e on switch duty cycle. This change in the cutoff frequency (Δf_c) is:

$$\Delta f_c \propto \frac{1}{\sqrt{\Delta L_e}}. \tag{10.26}$$

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Therefore, the effect of output filter cutoff frequency change or that of a zero in $E\hat{d}$ may not be a problem if the tap ratio (N_1/N_2) is not much greater than unity. Also, if the range of duty cycle D is not too great, changes in L_e will be small and could be neglected. If either of these two situations are not the case, reducing the switch voltage stress by tapping the inductor is probably a poor trade for increased control stabilization problems.

A second example of more complex model values is the tapped-transformer buck-derived converter shown in Fig. 10.11A. The small-signal model for this SPC variation is given in Fig. 10.11B, which shows quite clearly the effect of the variable turns-ratio of the transformer, T1.

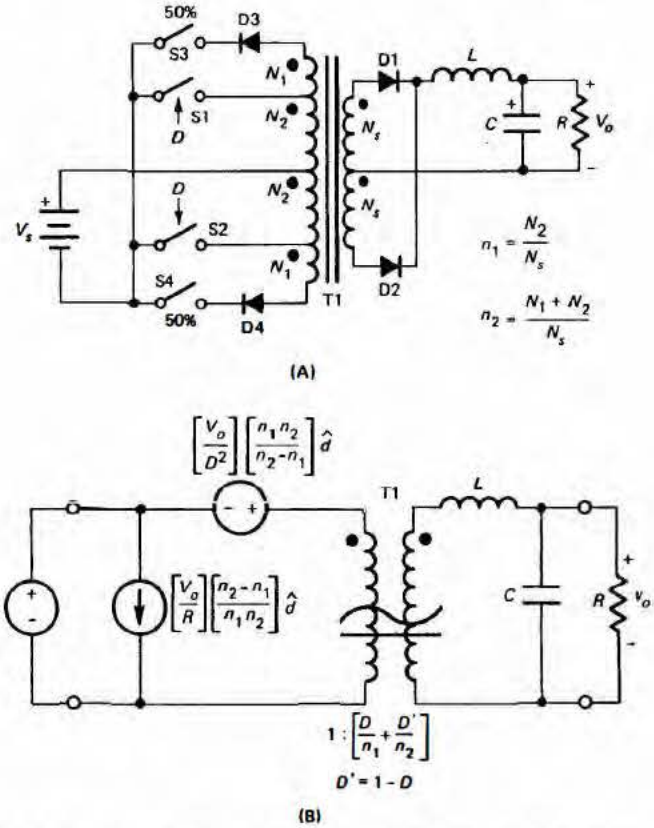


Fig. 10.11. The small-signal continuous-mode model for a tapped-primary buck-derived converter.

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10.3. CLOSING THE LOOP

Normally, the output from a power converter is required to be regulated against changes in its load and input voltage. Usually this control is accomplished by auxiliary electronics that compare the output voltage to that of a constant reference voltage. These electronic networks will in turn produce a control voltage (v_c) that is a function of this comparison. The control voltage magnitude is then converted to a value of d using a pulse-width-molulator (PWM) circuit. The PWM output is then employed to drive the switches of the power converter. This negative feedback arrangement is shown schematically in Fig. 10.12. There are many ways in which a PWM can be realized, but its general function can be rather succinctly stated as follows:

$$d = \left(\frac{f_m}{V_m}\right) v_c \tag{10.27}$$

where V_m is the DC range of v_c required to vary the value of D from 0 to 1 and f_m is the generalized AC transfer function characteristic of the particular PWM under consideration. For the purposes of this discussion, we will leave the small-signal PWM control-to-duty cycle gain function of Eq. (10.27) in the form shown.

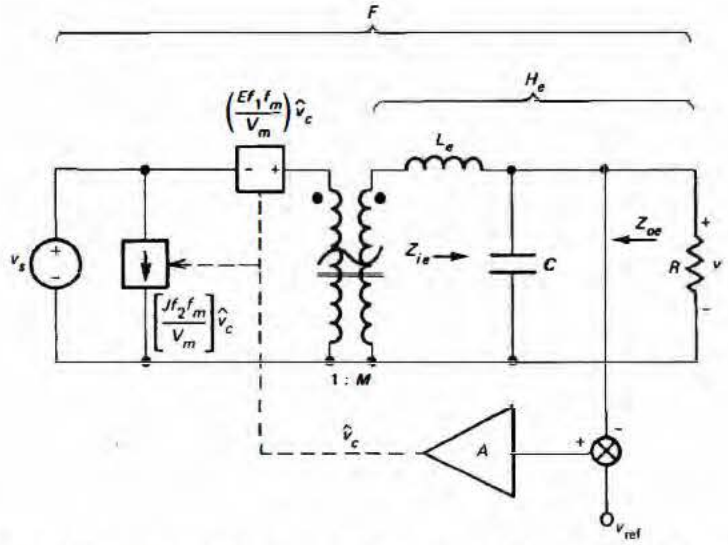


Fig. 10.12. The continuous-mode canonical model combined with an output voltage control system.

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In the model of Fig. 10.12, the small-signal portion of the PWM gain function has been merged with the voltage and current generator element values. Also notice that these generator symbols are now represented by "squares," indicating that they are *dependent* sources controlled by the small-signal value of $\hat{v}_c$. The methods of linear circuit analysis can now be applied directly to the model of Fig. 10.12 to derive the system's electrical characteristics in a straightforward manner. For example, the open-loop control loop gain (T) can be found by inspection of Fig. 10.12 as:

$$T = \frac{Ef_1 f_m AMH_e}{V_m}. \tag{10.28}$$

Notice that T does not contain a term for the dependent current generator of the canonical model (Jf_2). In this example, the model is driven from a zero-impedance voltage source (v_s). Therefore, this current generator plays no effective role in determining the various transfer functions of the system model. Usually, this is not the case, as we shall soon see when an input filter network is added between the voltage source and the input of the SPC model. From elementary control theory we know that:

$$Z_0 = \frac{Z_{00}}{1+T} \tag{10.29}$$

$$F = \frac{\hat{v}_o}{\hat{v}_s} = \frac{MH_e}{1+T}. \tag{10.30}$$

Finally, with a modest algebraic exercise, the closed-loop input admittance ($1/Z_i$) can be found to be:

$$\frac{1}{Z_i} = \left(\frac{1}{1+T}\right)\left(\frac{M^2}{Z_{ie}}\right) - \left(\frac{T}{1+T}\right)\left(\frac{M^2}{Rf_1}\right). \tag{10.31}$$

Looking at Eq. (10.31), we see that the input admittance of the system has two terms, one of which is negative! In any conventional control loop, the value of T will be very large at low frequencies, growing smaller as frequency is increased. Also, at low signal frequencies, the factor f_1 in our model will be close to unity. Therefore:

$$Z_i \approx -\frac{R}{M^2}. \tag{10.32}$$

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Under such conditions, the input impedance of the SPC is negative! This result is not very surprising when one considers a basic characteristic of any SPC regulator. The output voltage (V_o) is maintained constant; therefore, for a fixed value of R, the output power must also be constant. If we assume a highly efficient converter, then:

$$P_i \approx P_o = V_s I_s . \tag{10.33}$$

Since P_i is constant, I_s must decrease as V_s increases and vice versa. Therefore, the incremental input resistance (R_i) of the regulator system must be *negative*. At low frequencies, then:

$$Z_i \approx R_i = -\frac{R}{M^2} . \tag{10.34}$$

As signal frequency is increased, the real part of the complex impedance Z_i (Re $[Z_i]$), will at some point become positive in value; however, there is a substantial range of frequencies over which R_i is negative. This latter situation can be a problem if an input LC filter is used between the source voltage and the SPC regulator. When an LC filter is terminated in a negative resistance, self-oscillation can occur if the total effective damping resistance (i.e., the termination resistance plus any filter-damping resistances) becomes negative. Very few SPCs are built without an input filter for conducted EMI control. Therefore, this negative impedance problem can be very serious unless means are taken to circumvent self-oscillation due to the marriage of the input filter and the SPC.

To examine this particular problem in more detail, let us add an input filter to our system model, as shown in Fig. 10.13. Here, H_s is the *unloaded* voltage transfer function for the input filter network. To somewhat simplify our analysis, the voltage source and the input filter can be transformed into a Thevenin equivalent network, as shown in Fig. 10.14. Impedance Z_s represents the parallel combination of C1 and the series network consisting of R1 and L1. By applying some muscle to the crank of our algebra machine, we can derive the following new relationships, which now contain the effect of the input filter network:

$$T' = T\left[\frac{1 - \dfrac{M^2 f_1 f_2 Z_s}{R}}{1 + M^2(Z_s/Z_{ie})}\right] \tag{10.35}$$

$$F' = F\left[\frac{1}{1 + M^2(Z_s/Z_{ie})}\right]\left[\frac{1+T}{1+T'}\right] \tag{10.36}$$

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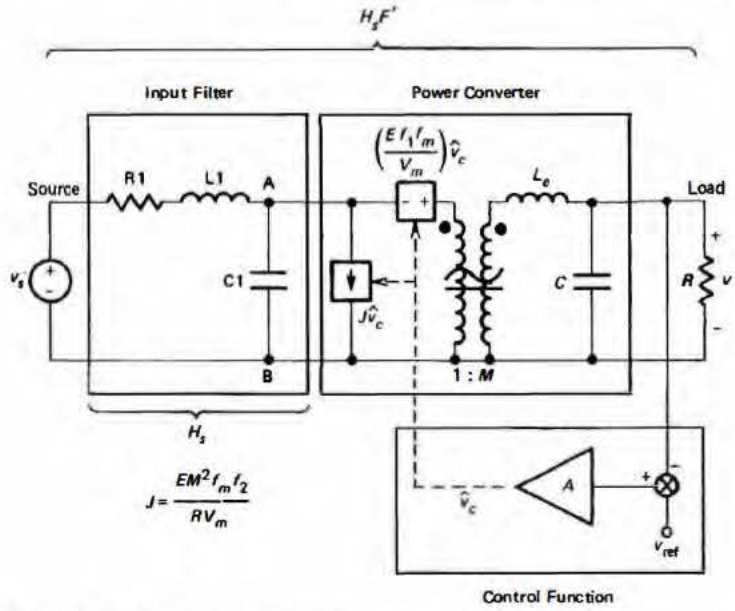
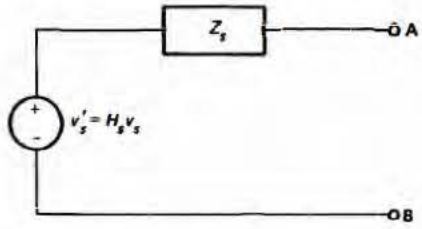


Fig. 10.13. The continuous-mode small-signal model for a complete converter circuit.



$$Z_s = \frac{\left[\frac{1}{sC1}\right]\left[R1 + sL1\right]}{R1 + sL1 + (1/sC1)}$$

$$H_s = \frac{(1/sC1)}{R1 + sL1 + (1/sC1)}$$

Fig. 10.14. Equivalent circuit representing the input source and low-pass filter.

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$$Z_0' = Z_0 \left[\frac{1 + M^2(Z_s/Z_a)}{1 + M^2(Z_s/Z_{ie})} \right]. \tag{10.37}$$

Here, Z_a is the value for Z_{ie} when the output of the system is short-circuited (i.e., $R = 0$). Therefore, in this particular example:

$$Z_a = sL_e. \tag{10.38}$$

The values of T, F, and Z_0 in Eqs. (10.35) through (10.37) are those obtained from the expressions of Eqs. (10.28) through (10.30), respectively (i.e., *without* an input filter present).

Equations (10.35) through (10.38) express a number of important features now evident in the SPC. First of all, the inclusion of the input filter network alters *all* of the essential SPC circuit properties. Unfortunately, these changes are for the worse. For example, output impedance (Z_0) and line-to-output transmission (F) are increased, while loop gain (T) is decreased. Looking at Eq. (10.35), we see that there is a negative term in the numerator of this equation. Therefore, the sign of the system's loop gain can change if:

$$\frac{M^2 f_1 f_2 Z_s}{R} > 1. \tag{10.39}$$

If the condition of Eq. (10.39) is satisfied, the regulatory system will probably become unstable and oscillate. Even if oscillation does not occur output transient response to changes in load and input voltage will be degraded to the point where serious "ringing" of output voltage will occur.

To assure stability of the SPC system with an input filter, two *necessary* and *more than sufficient* conditions must be met:

$$\frac{M^2 f_1 f_2 Z_s}{R} \ll 1 \tag{10.40}$$

$$\frac{M^2 Z_s}{Z_{ie}} \ll 1. \tag{10.41}$$

Placing the above conditions into the earlier expressions for T', Z_o', and F', we find that:

$$T' \approx T \tag{10.42}$$

$$Z_o' \approx Z_o \tag{10.43}$$

$$F' \approx F. \tag{10.44}$$

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It is apparent from these relationships that the input filter will not materially affect converter system performance if they are satisfied. The key factor is to make Z_s as small as possible (large C on the output). In some SPC regulator applications, such as high power operation with very restrictive EMI and weight requirements, it may not be practical to meet the criterion of Eqs. (10.40) and (10.41). In such instances, detailed modeling of the complete converter system using computer-aided analysis will probably be necessary to quantitatively evaluate the degradation in performance due to the presence of an input filter. Fortunately, the models we have developed in this chapter are well suited for such analyses. For further discussion of the input filter/SPC interaction problem, the reader is referred to Refs. 7 and 8 in the bibliography of this text.

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11. Comparative Techniques for SPC Selection

In the preceding chapters of this book, we have presented a large number of different SPC circuits. In addition, means by which even more SPC circuit variations can be created have been demonstrated. This overwhelming wealth of converter topologies is almost too much of a good thing because it creates a very basic problem, namely, how do we choose the best converter approach for a given application from the multitudes of options available to us?

Each individual circuit has many characteristics which must be considered for a particular application. Some of the more common application characteristics which must be compared are listed below:

1. Required control-loop and input-to-output dynamic transfer functions,
2. Component stress levels,
3. Circuit complexity (component count),
4. Efficiency of power conversion,
5. Weight of the converter system,
6. Volume of the converter system,
7. System filtering requirements for input and outputs,
8. Energy storage required (both capacitive and inductive),
9. Producibility and maintainability,
10. Cost of the conversion system,
11. Effect of nonideal components on desired performance, and
12. Unusual electrical or packaging needs.

One means for simplifying the selection problem is to arrange the circuits into groups that exhibit common properties. Once this is done, we can zero in on the general characteristics of the SPC quickly and then turn to considering the differences between a small number of circuit variations in greater detail.

As a practical matter, whatever process we choose to use must converge on the best choice relatively quickly. Engineering time is usually limited and expensive

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and designers can rarely afford to spend any great length of it trying to select the one most perfect SPC for a particular power conversion application need.

In this chapter we will examine means for categorizing and comparing SPC circuits. While these methods are helpful, keep in mind that they do not guarantee an optimum choice. You, the designer, will have to exercise a good deal of judgment to steer the selection process in the right direction to achieve an optimum solution. Like most engineering problems, there are often several solutions that are very nearly equal and viable with the final choice usually made as a result of personal preference.

11.1. FAMILIES OF CONVERTER CIRCUITS

The most obvious category scheme that comes first to mind is the grouping of SPC circuits on the basis of their basic parent converter (i.e., buck, boost, type of DC transformer, etc). As we have seen, the properties of the basic constituents are, for the most part, preserved in related converters. From a knowledge of basic SPCs, we can therefore predict in advance most of the conversion properties of any derivative.

We have chosen to group SPC circuits by the following criterion; first, the basic converter or combination thereof; second, by the choice of DC transformer if one is used and, finally, by whether or not the transformer is voltage-fed or current-fed.

This scheme makes a great deal of sense since, from the basic properties of a converter, we can quickly determine electrical transfer functions, switch duty cycles, component currents, etc. Then, from the DC transformer, we can rapidly determine the switch voltage and current stresses.

An example of this ordering scheme is shown in Fig. 11.1. Here we have developed a family tree for relating the circuits developed in earlier chapters of this text. The numbers shown in each portion of the tree relate to the figure number of this book.

The grouping begins with the buck and boost converters, which are dual in their electrical structures. From these two basic circuits, three major branches are delineated—those converters derived from the buck converter, those derived from the boost converter, and those derived from a combination of both buck and boost converters. Each main branch of the tree is further divided by the type of DC transformer (or the lack thereof) chosen. Notice that a hybrid branch has been included in Fig. 11.1 for the DC transformer category. The hybrid branch takes into account the possibility of a multiple input converter (Fig. 8.18) in which one input uses a different switch connection than the other input.

The next level of division is by the type of source at the input to the DC transformer (current or voltage-fed). By now, our family tree is looking pretty busy. Therefore, we have omitted cross linkage to indicate the duality relationships between some members of the buck- and boost-derived families. While de-

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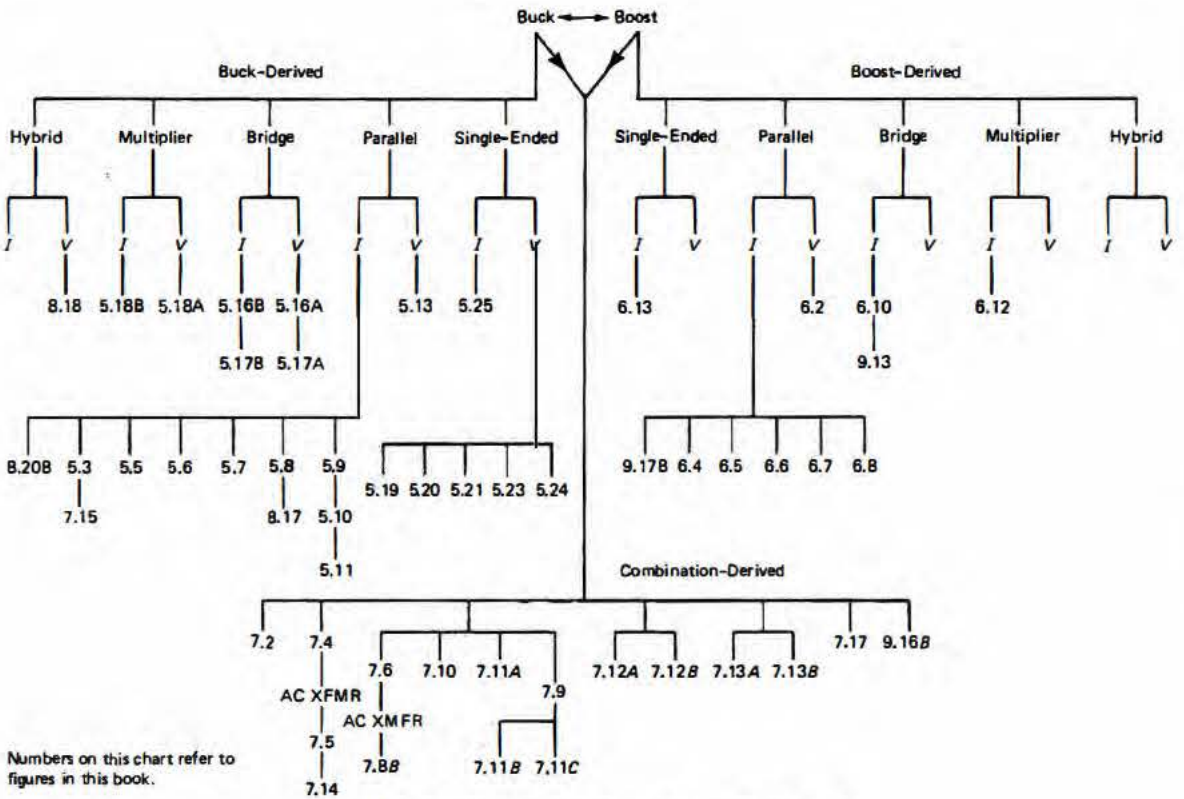


Fig. 11.1. Evolving a switchmode power converter family tree.

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sirable, addition of such duality relationships would render Fig. 11.1 completely illegible and perhaps unusable for some readers.

By way of an example of the use of this family tree, let us look at what it tells us about the quasi-squarewave converter of Fig. 5.13. In Fig. 11.1, we see immediately that it is a buck-derived converter and uses a voltage-fed parallel transformer. From these facts we can immediately infer that:

1. The input current is pulsating in nature.
2. The output current is nonpulsating in nature.
3. The input-to-output and the control-loop transfer functions have simple low-pass characteristics with fixed left-half-plane poles and zeros.
4. The ideal peak voltage that each of the converter switches will see when in an OFF state will be twice the supply voltage, V_s.
5. The average current of either switch will be equal to one-half of the average input current.
6. Because the transformer is voltage-fed, the switches may be subjected to current spikes should conduction overlap occur.

Thus, at a glance, we are able to define most of the important properties of a selected circuit. It is for this reason that this method of converter circuit grouping is so useful. By way of comparison, we could repeat the selection process with another circuit and then cancel out common characteristics leaving only the differences to compare if they are important for the application under consideration.

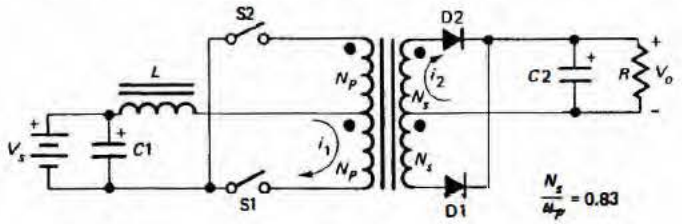
Of course, it would be impractical (unless you are willing to give up one wall of your office!) to include all possible circuits on a single diagram. So this type of diagram usually resides in the mind of the designer along with the information of the derivation of each circuit. When actually selecting a circuit, only portions of the family tree would need to be drawn by a designer as aids in converter selection.

11.2. QUANTITATIVE COMPARISONS

The qualitative comparison aided by family tree grouping is very helpful in narrowing the field of search for the right converter structure. However, sooner or later, a quantitative comparison must be conducted to determine actual circuit characteristics and the obtainable performance of each candidate circuit.

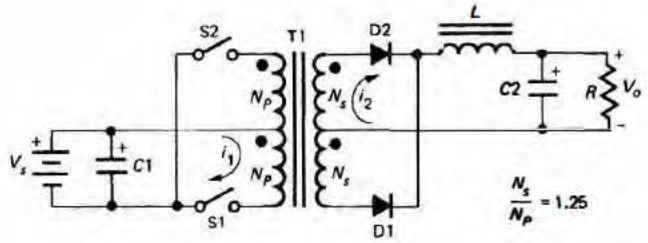
As a typical example of quantitative analysis at an intermediate level, we will examine a comparison between the buck-derived parallel quasi-squarewave converter of Fig. 5.13 and the boost-derived parallel overlapping-conduction converter as shown in Fig. 11.2. From the assumptions listed in Table 11.1 and the equations given in Tables 2.2A and 3.2A, we can derive the worst-case values for

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Boost-Derived

(A)



Buck-Derived

(B)

Fig. 11.2. Buck- and boost-derived circuits for comparison.

the circuit currents and voltages. The results of the derivations are delineated in Table 11.2.

From Table 11.2, we can make the following four observations:

1. If we assume that the size of L is proportional to the peak energy stored in it, then the buck inductor is physically larger by a factor of 1.5 over the inductor of the boost converter. Looking at $I_{L\,(\mathrm{rms})}$, we see that this current is larger in the boost converter, but since the inductance is lower in value, the boost in-

TABLE 11.1. Circuit Parameters for Performance Comparisons.

$V_g = 20 - 30$ V
$V_O = 25$ V
$R = 1\,\Omega$
$f_S = 50$ kHz
$\tau_L = 2\,\tau_{LC}$
Switch and diode voltage drop = 0

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TABLE 11.2. Continuous-Mode Buck and Boost Converter Comparison (see Table 11.1).

	Buck	Boost	Ratio (Ratio^2)
I_b	46.9 A	46.7 A	1.0
$I_{C1(rms)}$	16.5 A	2.6 A	–
$I_{C2(rms)}$	7.2 A	19.8 A	–
$(I_{C1} + I_{C2})_{(rms)}$	23.7 A	22.4 A	1.06 (1.12)
$I_{T(rms)}$	22.1 A	21.1 A	1.05 (1.10)
$V_{T(max)}$	60 V	60 V	1.0
L	3.3 μH	2.2 μH	1.5
$I_{L(rms)}$	26.1 A	31.2 A	0.84 (0.71)
Peak Energy ($\frac{1}{2}I_b^2L$)	3.6×10^{-3} J	2.4×10^{-3} J	1.5
Duty cycle range (S1 or S2)	0.33 to 0.5 (1.5:1)	0.5 to 0.665 (1.33:1)	1.13
$I_{1(rms)}$	22.1 A	21.1 A	1.05 (1.10)
$I_{2(rms)}$	18.4 A	22.6 A	0.81 (0.66)
$I'_{2(rms)}$ (I_2 reflected to primary)	23.0 A	18.8 A	1.22 (1.50)
$(I_1 + I'_2)_{(rms)}$	45.1 A	39.9 A	1.13 (1.28)

ductor will have fewer turns and its copper loss will be approximately the same as the inductor of the buck converter.

2. The total rms capacitor current is slightly larger in the buck converter. It is common design practice for the capacitor size to be determined more by current requirements than by the capacitance so that the buck converter requires a slightly greater volume of capacitors.

3. The total rms winding current reflected to the primary ($I_1 + I'_2$) is greater for the buck; but, since the primary winding in the buck will have a factor of 0.67 times the number of turns of the primary in the boost converter, the total copper loss in the buck transformer for the same wire size will be 85% that of the boost. For the same losses, the boost transformer will be slightly larger.

4. $I_{T(rms)}$ is 5% larger in the buck converter. If MOSFET switches are used where their conduction losses are proportional to $[I_{T(rms)}]^2$ and their ON re-

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sistances have a positive temperature coefficient, then the conduction losses could well be 20–30% higher in the buck converter depending on the thermal impedances of heat sinks used for the MOSFETs. The buck converter will need larger switches for the same power level.

From the preceding observation, it would appear from Table 11.2 that the boost circuit will be somewhat smaller or more efficient than the buck and therefore must be the logical choice. Unfortunately, this simple example has ignored some other practical considerations that make the choice not so clear cut. For example:

1. If an EMI specification such as MIL-STD-461A is imposed on the input to the converter, and the output noise specification is substantially wider in tolerance (a fairly common requirement), then the input filter for the buck converter will be much larger, since the input current is pulsating. On the other hand, if a low-noise EMI specification is required of the output, then the total buck converter system may very well be smaller in volume and weight.

Consider also that increasing L in the boost converter reduced $I_{C1\,(\mathrm{rms})}$, as opposed to the buck converter where increasing L above $2L_C$ doesn't change the value of $I_{C1\,(\mathrm{rms})}$ to a great degree. The dual argument applies to the output filter.

2. The control-to-output characteristic for the buck converter is very well behaved, but the boost converter has moving poles and a right-half-plane zero. As a result, efforts to provide unconditional stability usually result in the boost converter control loop having less bandwidth and, therefore, a slower transient response. The high-frequency output impedance of the boost converter will be lower since the output capacitor is so much larger (2.8:1), which compensates somewhat for the smaller bandwidth.

3. The boost-derived converter is current-fed by nature, as was pointed out in Chapter 4. The circuit will have much less of a problem dealing with transformer saturation and most other nonideal component behavior. An exception, of course, is the problem of high voltage spikes caused by transformer leakage inductances.

4. If overload, turn-on, and turn-off output voltage-ramping and inrush-current controls are required, then the buck converter is a much better choice. To exhibit these often necessary properties, the boost converter must be made more complex in topology in order to emulate a buck converter when called upon to do so.

11.3 THE PRACTICAL COMPARISON PROCESS

The preceding discussion has shown that both quantitative and qualitative considerations must enter into any decision process by which a particular SPC circuit is chosen for a given application.

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In practice, the decision process usually begins rather subjectively (with personal bias and experience playing an important role) with qualitative considerations using the family tree approach to narrow the number of alternatives. The process then becomes more objective as quantitative comparisons are made. The final converter choice is then made, based on a detailed quantitative comparison of a very few circuits. This final stage of comparison often requires the execution of very detailed circuit designs each using one candidate converter. Since this final step is very time-consuming, it is rarely possible to do such detailed comparisons between more than two or three circuit approaches. For this reason, the judgment (and intuition) exercised by a designer at the beginning of the selection process will be the major factor in determining final converter choice and its degree of acceptability. Like most human endeavors, such judgment comes with experience. Therefore, the inexperienced designer would be well advised to spend a good deal of effort at an intermediate level of quantitative comparison of many different converter approaches before choosing final candidates. Repeating this comparison process for several converter designs will bring familiarity and speed of selection for future applications.

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12. Converters with Integrated Magnetics

The continuing and seemingly never-ending quest by product designers to develop new techniques to integrate electronic circuit functions has motivated power electronics engineers to find ways whereby the physical size and parts count of SPCs can also be reduced. One part of these investigative efforts that has shown definite promise in recent years is the integration of the magnetic components of an SPC. Such methods provide for the combination, or "lumping," of inductors and transformers into *single* physical assemblies with little or no compromise in conversion characteristics.

As we have seen in past chapters, SPC inductors and transformers perform a variety of essential roles and are key to the dynamic power transfer and storage processes of these circuits. Unfortunately, and with few exceptions, inductors and transformers are also the major contributors to the total cost, weight, and size of a converter system. Therefore, it is not very surprising that SPC designers often go to considerable extremes to minimize the number and size of magnetic components required in a converter, and not uncommon that such extremes include the selection of a less-than-optimum SPC circuit approach that, in turn, calls for one or more undesirable concessions in electrical performance.

SPC topologies which inherently adapt well to the integration process of magnetic functions are very attractive to designers for reasons such as those just mentioned. Also, magnetic integration, if properly executed in the design of these converters, can bring added benefits in electrical performance, such as reduced stress on other SPC components or lower ripple currents on input and output lines. The Ćuk converter variations discussed in Chapter 7 (Fig. 7.11) and the multi-winding output inductor assembly proposed in Chapter 8 (Fig. 8.4) are excellent examples where integration of magnetic functions will not only reduce component count, but also will enhance the operational features of these converters. The flyback converter of Chapter 7 (Fig. 7.4B) is another example, wherein its singular magnetic serves as the primary energy storage component of this SPC as well as a means for providing electrical isolation between all input and output terminals.

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In this chapter, we will explore the unusual subject of integrating magnetic circuit elements of SPCs. In our exploration, we will take a more detailed analytical look at the single-magnetic Ćuk converter of Fig. 7.11C to better understand how it can be designed to have *both* zero input and zero output current ripple. Because the output section of a Ćuk converter is essentially that of a buck SPC, this look will also provide insight into the design principles of a multiwinding inductor assembly for use in the quasi-squarewave converters of Figs. 8.4B and 8.5A. Finally, magnetic design methods whereby the inductors and transformers of many other SPC circuits can be blended together will then be examined, followed by the evolution of new and unique converter circuits using these integration methods.

12.1. MAGNETIC CIRCUIT ANALYSIS–A REVIEW OF CONCEPTS

Magnetic circuit concepts are subjects usually found in basic electrical engineering textbooks dealing with topics related to electrostatic field theory. For the most part, these important concepts are usually presented in such books with little or no illustration of application in the practical design of inductors and transformers for SPCs.

While a complete review of the fundamentals of magnetic circuits is beyond the scope of this book, a brief review of those important to the proper understanding of ferromagnetic circuits is appropriate here, as a prelude to later discussions of SPC inductor and transformer integration methods. For those readers interested in a more thorough exposure, Ref. 9 cited in the bibilography of this text is highly recommended.

Recall that the similarity between Kirchhoff's voltage and current laws for linear electric circuits and Ampere's circuit laws related to magnetomotive force and flux continuity in *linear* magnetic circuits permit the use of electric circuit analogs for analysis purposes. These analysis methods make voltage analogous to magnetic potential, F, current analogous to magnetic flux, ϕ, and electrical resistance analogous to magnetic reluctance, $\mathcal{R}$. It follows also that any electrical circuit resulting from application of these analogous relationships will have the same topology as that of its magnetic circuit counterpart. Furthermore, because it is linear, this circuit model can be manipulated into even more useful forms by the use of the standard duality relationships explained in detail in Chapter 9. Conversion by duality will then provide a final model relating reluctance values to inductances, flux linkages in windings to voltages, and flux magnitudes in magnetic paths into currents.

The familiar relationship between the voltage appearing across an inductor L and the rate of change of current through it is simply:

$$v = L\frac{di}{dt} \tag{12.1}$$

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in accordance with Faraday's classic law of electromagnetic induction. This law, when applied to a single coil of wire with N turns, can also be restated as:

$$v = \frac{d\lambda}{dt} = N\frac{d\phi}{dt} \tag{12.2}$$

where λ is the measure of *flux linkage* within the coil produced by *self-induction*. In those instances where multiple coils of wire have common magnetic paths, the total flux linkage in any one coil would be the sum of that produced by self-induction plus those produced by *mutual induction*, i.e., caused by dynamic changes in the currents of the remaining coils. For the case of a single coil, its *self-inductance* can be determined by the equality of Eqs.(12.1) and (12.2) as:

$$L = N\frac{d\phi}{di}. \tag{12.3}$$

Magnetomotive force (F) of an excited coil of wire is defined as the product of the instantaneous current through it and the number of turns of the coil. In equation form, F can be directly related to *magnetizing force*, H, and its magnetic path length, l, as:

$$F = Ni = Hl. \tag{12.4}$$

Assuming that a linear relationship between ϕ and H is always maintained, the *reluctance* ($\mathfrak{R}$) of a magnetic path can be defined as the ratio of a change in magnetomotive force to the corresponding change in flux value. Therefore, it follows from Eqs. (12.3) and (12.4) that:

$$\mathfrak{R} = \frac{dF}{d\phi} = N\frac{di}{d\phi} = \frac{N^2}{L}. \tag{12.5}$$

Reluctance can be expressed in terms of related magnetic path length, cross-sectional area (A_C), and the permeability (μ) of the magnetic path. Assuming that the cross-sectional area is uniform,

$$\mathfrak{R} = \frac{l}{\mu A_C} = \frac{1}{\mathcal{P}} \tag{12.6}$$

where $\mathcal{P}$ is defined as material *permeance*, the reciprocal element of reluctance.

In magnetic circuits, arrows are used to indicate the assumed directions of currents rather than polarity marks for magnetomotive forces (mmfs). The best

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known method for relating the direction of current to that of the flux it produces is the "right-hand rule" illustrated in Fig. 12.1A.

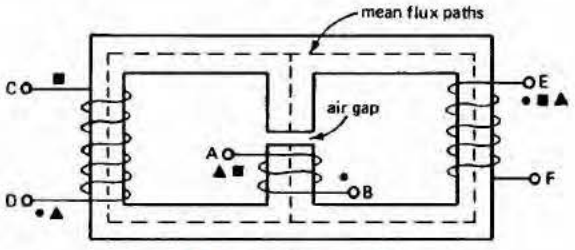
With the right hand positioned as shown, the flux direction will be indicated by the direction of curvature of the fingers. Note that the thumb must be aligned so as to point in the direction of the current. The fingers then point in the positive direction of flux produced by the current.

In representing transformers in electric circuit diagrams, it is customary to use *dot notation* to convey the voltage polarity relationships of windings relative to one another, as shown in Fig. 12.1B. Three basic rules are followed in establishing such relationships:

1) Voltages induced in any two windings due to changes in mutual flux will have the *same* polarity at "dot-marked" terminals.
2) If positive currents flow into the dot-marked terminals, the mmfs produced in the two windings will have *additive* polarity.



(A)



■ Relative to Winding A – B
▲ Relative to Winding E – F
• Relative to Winding C – D

(B)

Fig. 12.1. (A) Determining flux direction using the right-hand rule.
(B) Dotting of windings in a magnetic structure with multiple flux paths.

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3) If one of the two windings is open-circuited, and if the current flowing into the dot-marked terminal of the other winding has a *positive* rate of change, then the voltage induced in the open winding will be *positive* at dot-marked terminal.

When a magnetic assembly has more than two windings and contains multiple magnetic material paths, then multiple "dotting" of windings will be necessary. This is easily done using the right-hand rule and the three basic relationships given above. An example of multiple dotting is shown in Fig. 12.1B. Here, three sets of "dots" are needed to express the voltage polarities relative to each of the three windings.

Finally, to complete our review, we can relate the degree of mutual induction between two windings sharing a common magnetic path by the use of the following relationship:

$$M = k\sqrt{L_{o1}L_{o2}} \tag{12.7}$$

where k is defined as the *coupling coefficient*, M is the amount of *mutual inductance* that exists between the windings, and L_{o1} and L_{o2} are the *self-inductance* (open-circuit) values of the two windings.

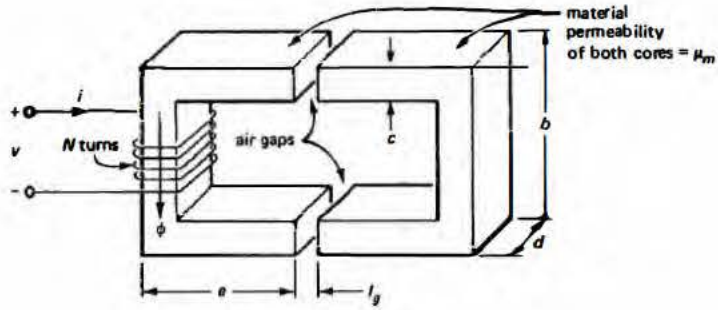
All of these fundamental definitions relating to magnetic circuits, when combined with the equivalent electric-circuit development methods described earlier for modeling, produce a powerful set of analysis tools for quick and accurate evaluation of any magnetic circuit system, regardless of its complexity. As demonstrations of their utility, we will now use them to develop realistic electric circuit models for an inductor and a dual-winding transformer. The reader is encouraged here to review the duality concepts of Chapter 9, for they are key to a proper understanding of these modeling examples.

12.2. EXAMPLES OF MAGNETIC CIRCUIT MODELS

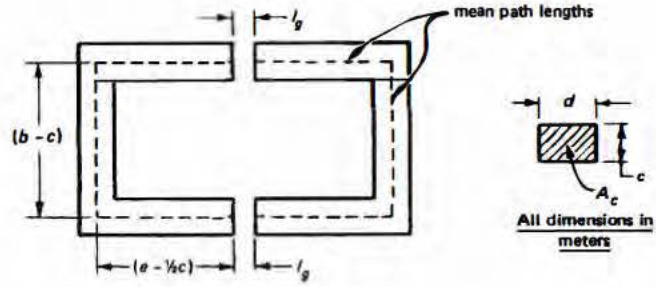
Consider now the single-winding magnetic structure shown in three-dimensional form in Fig. 12.2A. Here, we have joined two C cores of equal dimensions and cross-sectional areas and have inserted small air gaps of equal length at their junctions. A winding of N turns of wire has been placed on the outer leg of one of the C cores, into which a current (i) flows.

For our analysis purposes, we will assume that flux distribution within the cores as well as across each of the two gaps is uniformly distributed, and that both cores have the same permeability, μ_m. Also, mean magnetic path lengths will be used to estimate the reluctances of each portion of the cores and that presented by the air gaps, as diagrammed in Fig. 12.2B. Using standard international MKSA (Meter-Kilogram-Second-Ampere) magnetic units, the reluctances

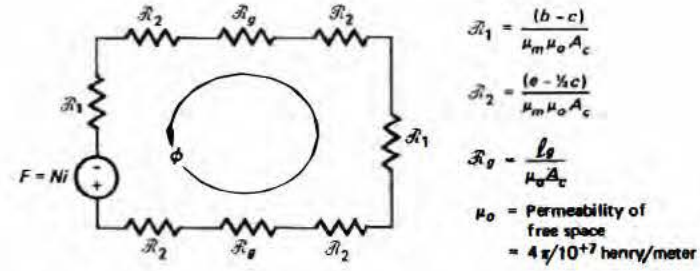
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(A)



(B)



(C)

Fig. 12.2. Setting up a reluctance and mmf model for a single-winding inductor.

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of each portion of the mean flux path can then be determined using the equations accompanying Fig. 12.2C. From our electric circuit analog, the flux magnitude is simply:

$$\phi = \frac{F}{\mathcal{R}_T} = \frac{Ni}{2\mathcal{R}_1 + 4\mathcal{R}_2 + 2\mathcal{R}_g} \tag{12.8}$$

where $\mathcal{R}_T$ is the sum total of all reluctances in the flux path.

Fig. 12.3A is the circuit model described by the conditions of Eq. (12.8). With an electric circuit analog established, we now determine its dual network

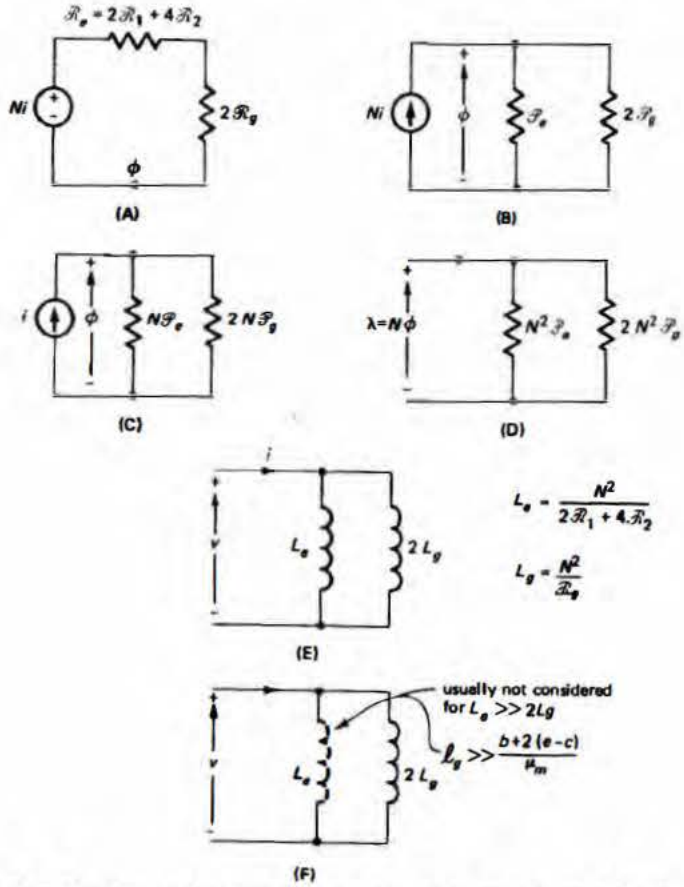


Fig. 12.3. Development of an electrical network model for the inductor of Fig. 12.2.

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as is done in Fig. 12.3B. It is now necessary to scale the dual circuit by the number of turns of the winding until it is in a form where permeances can be directly related to inductances. This operation is performed in Figs. 12.3C and D. From Eqs. (12.5) and (12.6), we see that inductance is equal to permeance times the number of winding turns squared. Using this relationship, we then convert the equivalent circuit of Fig. 12.3D to its final inductive form shown in Fig. 12.3E.

Our final model clearly shows that the inductances established by the core materials are in parallel with the inductances produced by the airgaps of the composite structure. If L_e is much greater than $2L_g$, then the equivalent circuit of Fig. 12.3E reduces to the single-component network of Fig. 12.3F. In most practical inductor designs for SPCs, this is usually the case. Air gaps will be the major factors in determining their winding inductance values, and increasing air gap length will decrease the inductance of a magnetic material. However, a larger air gap will also permit more DC bias to be tolerated by the core of an inductor, a situation frequently encountered in converter circuit applications. For this reason, most SPC inductors use core structures with external air gaps in the magnetic paths, or employ cores that have inherent gaps in the composition of their magnetic material.

This simple example, evolving a practical electrical circuit model for an inductor from its magnetic structure, serves to illustrate the ease of development when electric circuit analogs are used. In our next example, we will use the same procedure to derive a practical circuit model for a transformer with leakage inductances. The magnetic circuit (taken from Ref. 9) that we use for this particular example is shown in Fig. 12.4A.

As shown, three flux paths are indicated, two of which (ϕ_2 and ϕ_1) are *not* contained within the magnetic material of the toroid. These latter paths are called *leakages* and, as we will see, produce *leakage inductances* in the final electrical model for the transformer. The remaining material flux path links both windings and is designated as the mutual flux (ϕ_m). With a voltage source applied to the primary winding (N_P), with the polarity as shown in Fig. 12.4A, the resulting current direction will produce a counter-clockwise flux in the core. Using the dot notation with the primary winding as reference, the secondary winding (N_s) will have its dot at the top of the winding, and therefore will produce a load voltage with the polarity shown. Because the secondary current direction is "out of the dot," it will produce an mmf that *opposes* that of the primary winding.

Fig. 12.4B is the equivalent magnetic circuit diagram, with its dual network shown in Fig. 12.4C. Note that ϕ_m and ϕ_1 have the same polarity in the primary winding, since they are caused by i_s. However, in the secondary winding, ϕ_m and ϕ_2 have opposite polarity, since one flux produces i_o while the other is a consequence of i_o.

With a dual magnetic network established, we can now proceed to place it

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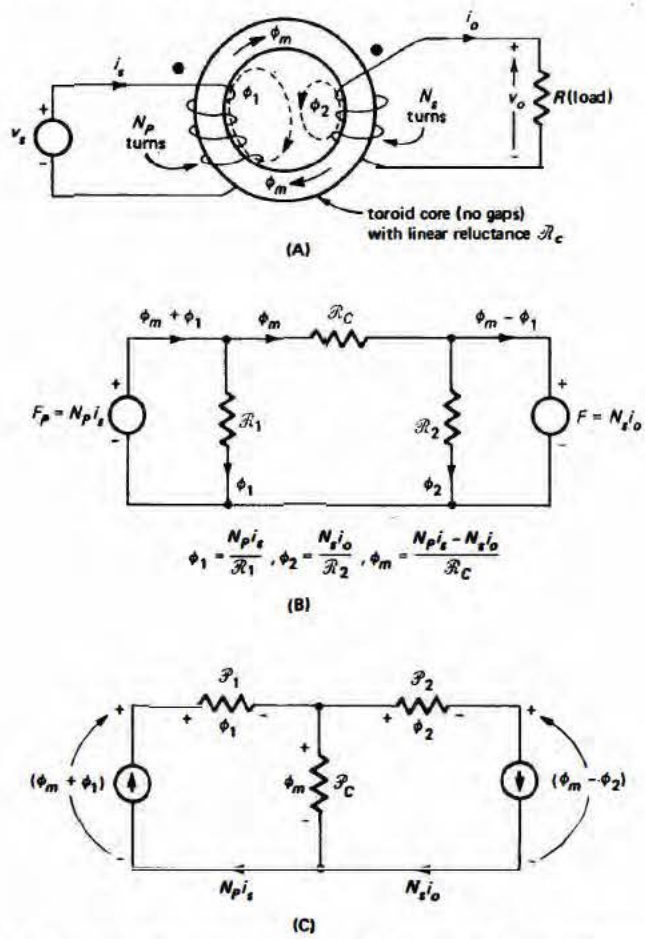


Fig. 12.4. Setting up a reluctance and mmf model for a two-winding transformer with leakage flux paths.

into an electrical form following the same steps that were used in the previous inductor example. First, we scale up the permeances of the model of Fig. 12.4C by the square of the turns of the winding that is selected as reference. In this case, the primary will be used as the reference winding. The results of this scaling operation is shown in Fig. 12.5A. Next, the scaled permeances are replaced by inductances in accord with Eq. (12.6) and flux linkages by voltage sources. This last step produces the final inductive circuit model illustrated in Fig. 12.5B.

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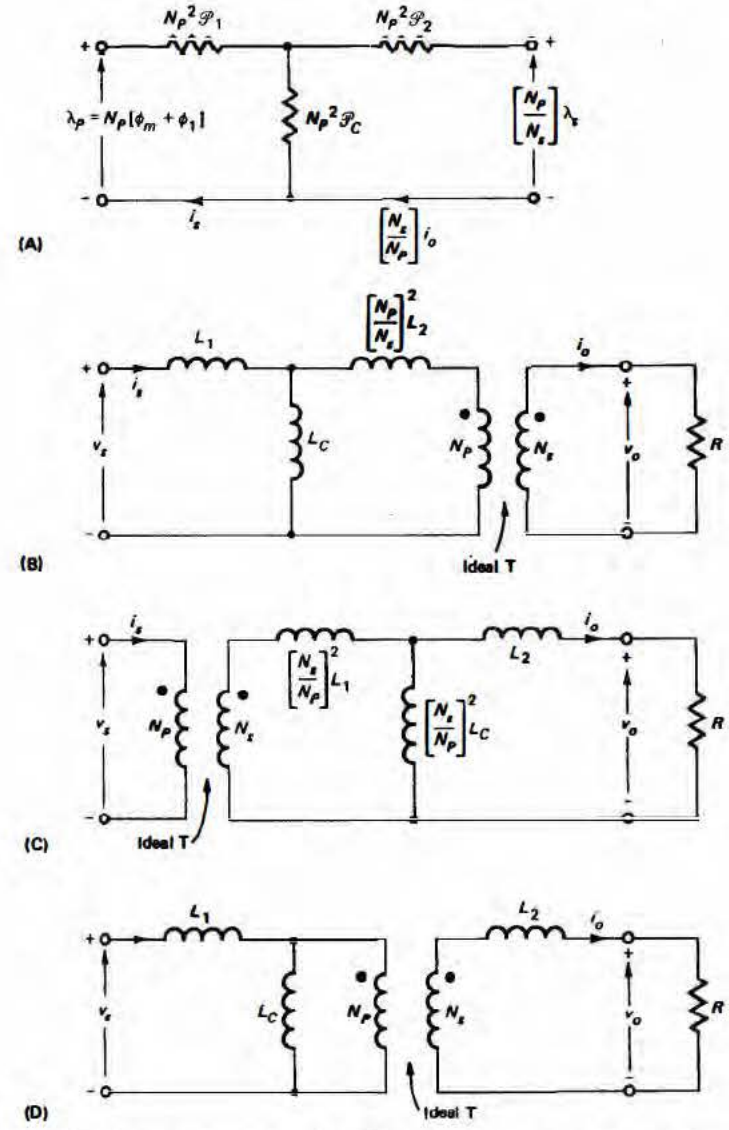


Fig. 12.5. Development of equivalent electrical circuits for the two-winding transformer of Fig. 12.4.

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If one desires to reference one or more inductances of this final model to the secondary side of the transformer instead of the primary, this can be easily accomplished using impedance transformation techniques. Two alternative circuit models developed in this fashion are shown in Figs. 12.5C and D.

The last circuit model in Fig. 12.5D is a classic form used frequently to design and analyze transformers for SPCs. Here, L_1 and L_2 represent the *leakage inductances* of primary and secondary windings, respectively, while L_C is often termed the *primary magnetizing inductance* of the transformer. In practice, designers will strive to minimize the value of L_1 and L_2 in a converter transformer. This is accomplished by winding the primary and secondary in very close proximity to one another. Also, to minimize core excitation current, L_C is usually made as large as possible. Therefore, in a transformer, core structures *without* air gaps are highly desirable, although most practical designs for SPCs do have small gaps to prevent core saturation from external imbalance effects (see Section 4 of Chapter 4).

It should be pointed out here that L_C in the transformer models of Fig. 12.5 is *not* the mutual inductance (M) shared by primary and secondary windings. However, M can be easily found by writing the two nodal circuit equations that relate input and output currents of the models and isolating the common inductance term. If we choose the model of Fig. 12.5D for this analysis, the value of M is found to be

$$M = \left(\frac{N_S}{N_P}\right) L_C . \tag{12.9}$$

From Eq. (12.7), the degree of coupling between the two windings of our model can then be determined as

$$k = \frac{(N_S/N_P)\, L_C}{\sqrt{(L_1 + L_C)(L_2 + [N_S/N_P]^2\, L_C)}} \tag{12.10}$$

Note that Eq. (12.10) correctly predicts that k will be equal to unity (perfect coupling of windings) when the two leakage inductances (L_1 and L_2) of the model are reduced to zero.

Once again, in four easy steps, an electrical circuit model that accurately represents its magnetic circuit counterpart has been found. The evolution of an electrical model by this procedure also gives much insight into the important relationships between physical core dimensions, material properties, and corresponding electrical performance. Although these two modeling examples were somewhat simplistic, the same steps of model formation can be followed in analyzing more complex and unusual magnetic circuits, as we will soon see in our discussions of SPCs with integrated magnetics.

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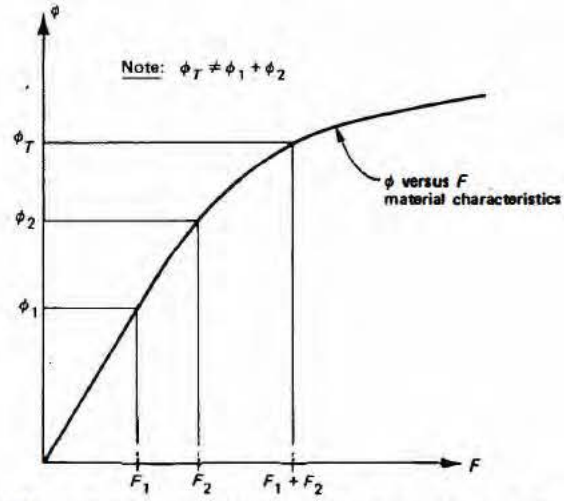


Fig. 12.6. Doubly-excited magnetic circuit operating in a nonlinear portion of the core material's characteristic curve.

Before moving into these discussions, one important modeling rule mentioned earlier needs to be re-emphasized. Always keep in mind that the electrical model analogs are based on the assumption that *linear* relationships exist between flux and exciting forces of windings. This assumption allows us to use linear circuit analysis methods in model development. If this assumption is not valid, the values of the inductive elements within the model will be inaccurate and erroneous results will be obtained from its use. As an illustration of a violation of this assumption, consider the ϕ versus F plot shown in Fig. 12.6.

Here, we have depicted a situation where a magnetic material with the indicated characteristic is excited by two mmfs which are additive. It is seen that the resulting flux caused by the total mmf does *not* equal the sum of individual flux magnitudes. Therefore, to insure that the linear principle of superposition of flux values will always hold true, operation well below the saturation limits of the magnetic material is always necessary. One is therefore cautioned to always check that the point of maximum core excitation does not fall in a nonlinear portion of the material's characteristic before attempting to construct any linear electric circuit analog.

12.3. TWO-WINDING INDUCTORS AND THE ZERO-RIPPLE CURRENT PHENOMENON

During lab experiments at the California Institute of Technology in 1977, Dr. Slobodan Ćuk decided to wind both of the inductors of his SPC on a com-

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mon magnetic core. The purpose of this particular experiment was to see if a savings in the weight and size of a basic Ćuk converter could be achieved without affecting its basic electrical properties. The experiment was successful, but an unexpected and potentially useful effect also occurred. While observing the input and output ripple current waveforms, Dr. Ćuk noted that they were very unequal, to the point where the magnitude in one was close to *zero* while the other remained near a value that would be expected if the two inductors were *not* coupled together on a common core. Also, the effect seemed to be *independent* of input and output voltage values, the switching frequency of the converter, switch duty cycle, and inductor current waveform (i.e., continuous or discontinuous)!

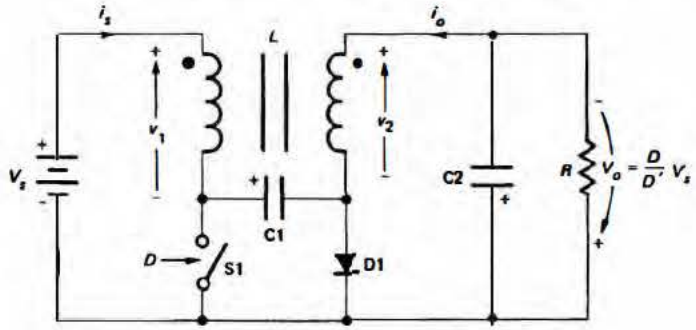
Since the time of these experiments, this peculiar effect that Dr. Ćuk observed has come to be known as the *zero-ripple current phenomenon*. Its appearance is dependent on the proper phasing of the voltages appearing across the terminals of the inductors as well as on certain details of the magnetic design of the dual-winding inductor. As it happens, the Ćuk converter inherently produces voltages across its inductors that are *always* proportional in magnitude and are *always* in phase. These waveform relationships are shown in Fig. 12.7, along with the schematic of a basic coupled-inductor Ćuk converter taken from Chapter 7 (Fig. 7.9B).

The voltage relationships of Fig. 12.7, along with the right choice of leakage inductances associated with the inductor windings, are the key factors in achieving zero-ripple current at *either* the input or the output of the Ćuk converter. Since a two-winding "coupled-inductor" is nothing more than a dual-winding transformer, the modeling example of Fig. 12.5D can be used to determine what values of leakage inductances are relevant to producing this unusual condition.

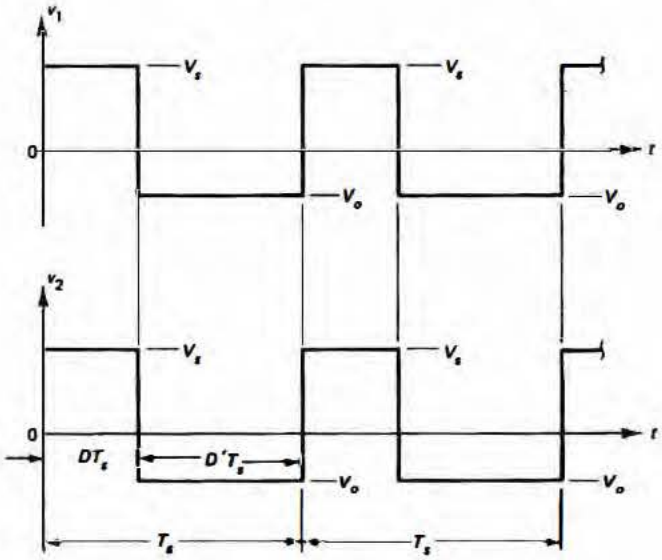
To make the following examination general, we will excite both the input and output of our transformer model with proportional voltage sources of like frequency and phase, as shown in Fig. 12.8. These conditions will be the only ones we will impose, and the waveform shapes of the voltage sources can take any form. For example, the shapes could be quasi-squarewave or sinusoidal as illustrated, differing only in amplitude by a factor defined here as a, where $a > 0$. For the Ćuk converter in Fig. 12.7, $a = 1$, as indicated by the accompanying voltage waveforms.

Let us now make the assumption that is possible to reduce the value of i_o to *zero* in our model of Fig. 12.8, and then examine the circuit currents and voltages that result from our assumption. If i_o is zero, then the AC voltage drop across L_2 must also be zero, as illustrated in Fig. 12.9A. The voltage appearing across L_C must therefore be equal to that of the secondary voltage source, av_s, reflected through the ideal transformer in the model. Also, the current through L_1 and L_C must be equal to that produced by the primary voltage source, v_s. These conditions lead to the simplified circuit model of Fig. 12.9B, where:

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(A)



(B)

Fig. 12.7. A coupled-inductor Ćuk converter with equal primary and secondary voltage waveforms.

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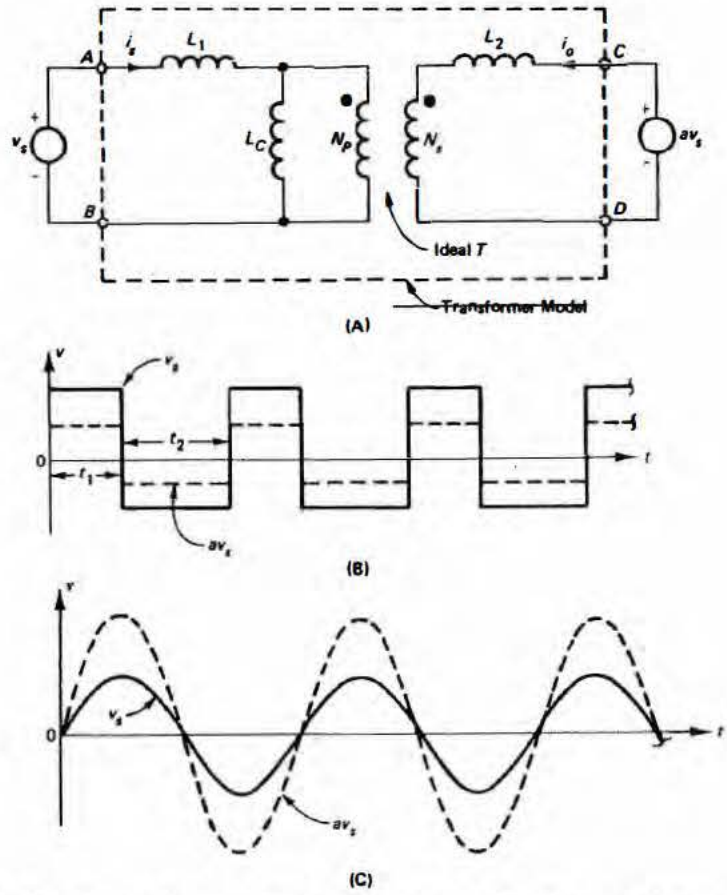


Fig. 12.8. Exciting the two-winding transformer model of Fig. 12.5D with similar voltage sources of equal frequency and phase.

$$v_s = (L_1 + L_C)\frac{di_s}{dt} \tag{12.11}$$

$$\left[\frac{N_P}{N_s}\right][av_s] = L_C\frac{di_s}{dt}. \tag{12.12}$$

Combining Eqs. (12.11) and (12.12) by the elimination of the common di_s/dt factor gives:

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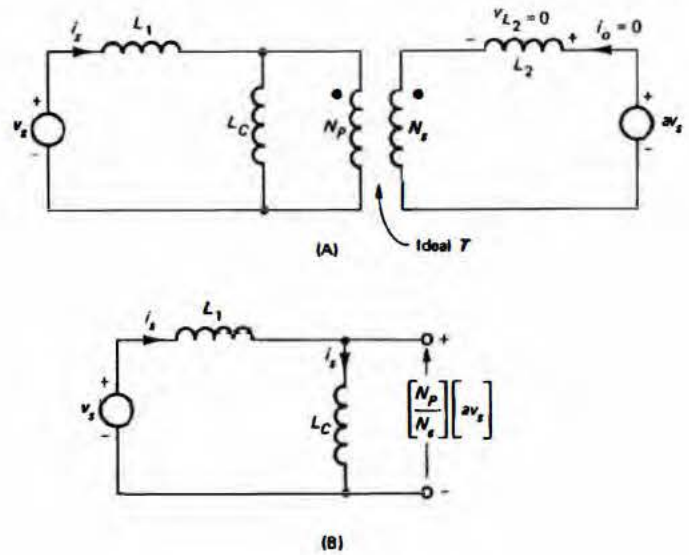


Fig. 12.9. Circuit model conditions for zero ripple output current.

$$L_1 = L_C\left[\frac{N_s}{aN_P} - 1\right]. \tag{12.13}$$

The relationship between primary leakage inductance and that of the core material set by Eq. (12.13) is important and worth dwelling on for a moment. First of all, recall that this equation was derived based on the premise that *no* output ripple current existed in our model and, if satisfied, must produce this condition. It also indicates that a similar relationship can be established between L_2 and L_C to permit the input rather than the output ripple current to be reduced to zero. Using a similar path of analysis as depicted in Figs. 12.10A and B, this condition should occur when:

$$av_s = \left[L_2 + \left(\frac{N_s}{N_P}\right)^2 L_C\right]\frac{di_o}{dt} \tag{12.14}$$

$$\left[\frac{N_s}{N_P}\right]v_s = \left[\frac{N_s}{N_P}\right]^2 L_C\,\frac{di_o}{dt} \tag{12.15}$$

$$L_2 = \left(\frac{N_s}{N_P}\right)^2 L_C\left[\frac{aN_P}{N_s} - 1\right]. \tag{12.16}$$

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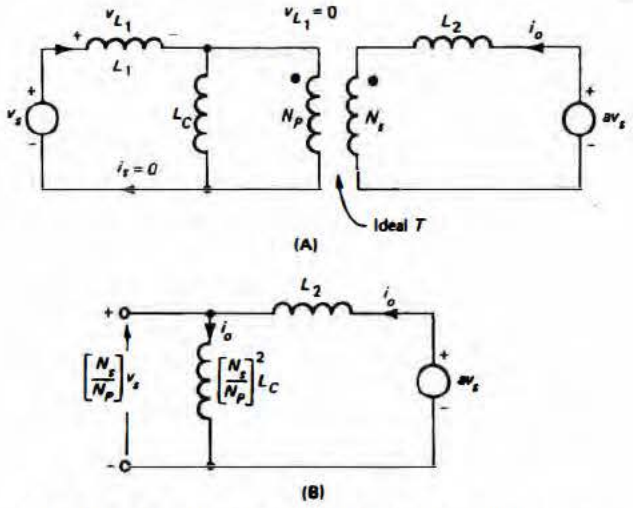


Fig. 12.10. Circuit model conditions for zero ripple input current.

Comparing the constraints imposed on the values of L_1 and L_2 by Eqs. (12.13) and (12.16), respectively, one finds that it is *not* possible to achieve zero input *and* output ripple currents simultaneously. For values of $N_s/aN_P > 1$, L_1 can be selected for zero output ripple. On the other hand, if $aN_P/N_s < 1$, then a value of L_2 can be found to reduce the input current ripple to zero.

Fig. 12.11 shows the current waveshapes that result when the conditions of either Eq. (12.13) or Eq. (12.16) are satisfied. Here, we have assumed that the input and output voltage sources take the form of quasi-squarewaves, such as those illustrated earlier in Fig. 12.8. Note from the equations accompanying Fig. 12.11 that the effective inductance seen at the primary side of the coupled-inductor is equal to its open-circuit value (i.e., secondary side open) when L_1 is selected for zero output current ripple. Conversely, the effective inductance seen at the secondary terminals will equal its open-circuit magnitude when L_2 is selected to achieve zero input current ripple.

In practice, it is difficult to design and consistently manufacture a transformer with specific values of leakage inductances to achieve the "matching" conditions specified by Eq. (12.13) or Eq. (12.14). One viable solution to this problem is to tightly wind primary and secondary turns together to reduce L_1 and L_2 to essentially zero, and then insert a small *external* "trimming" inductor in series with the input or output to emulate the desired value of L_1 or L_2.

This technique is shown in Fig. 12.12, where L_{ext} represents the external inductance needed for zero input (Fig. 12.12B) or output (Fig. 12.12A) current

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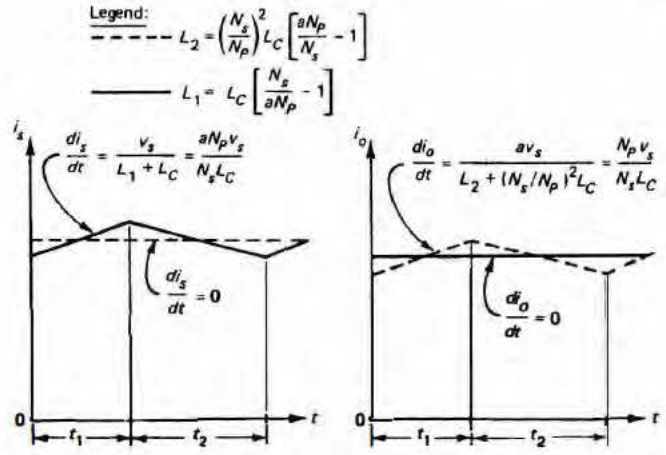


Fig. 12.11. Winding current waveshapes under zero ripple current conditions.

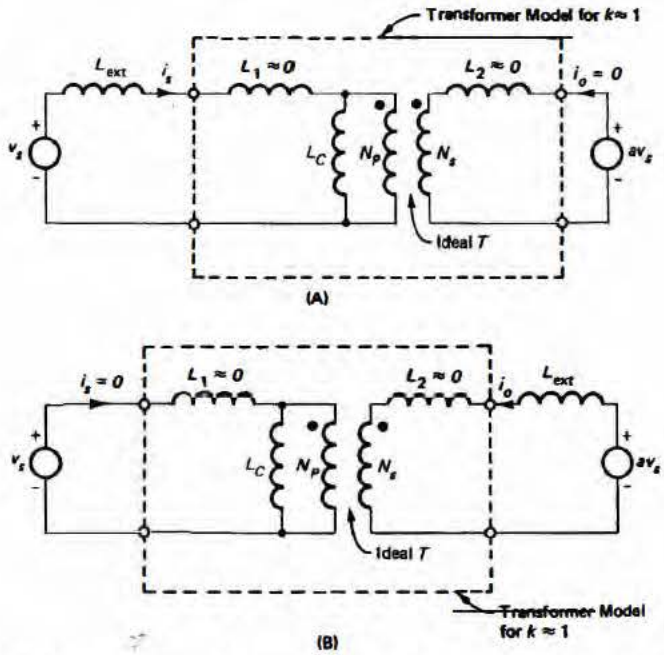


Fig. 12.12. Using external inductors to simulate leakage inductance required for zero current ripple.

VC00049713

ripple. Eqs. (12.13) or (12.16) can be used to calculate the ideal value of L_{ext} needed in either case. The actual contribution to this calculated value by the appropriate leakage inductance within the transformer can be found by empirical means. This entails measurement of the inductance of one winding while maintaining a low-inductance short across the other winding. Because the short will bypass the magnetization inductance of the transformer, only leakage inductance will be measured by this method.

12.4. APPLICATION IN BASIC CONVERTERS

At first thought, the zero-ripple current phenomenon may seem to be a scientific curiosity with little or no value in "real-world" SPC design. However, the ability to selectively reduce ripple currents of inductors within converters can be very advantageous when one considers that most SPC applications require low conducted noise on their input and output lines. Also, low ripple currents in SPC inductors reduce heating losses in associated converter capacitors, and often will decrease the values of capacitance needed for proper filtering of SPC input and/or output voltages.

From our generalized analysis of the last section, it is apparent that the zero-ripple current phenomenon can be produced in *any* converter whose inductances have proportional voltages of equal shape, frequency and phase, and is *not* just a special effect unique to the Ćuk converter circuit. To illustrate this point, let us pause and take a look at a few basic SPC design examples.

In Fig. 12.13, the output inductor of a basic buck converter has been replaced by one with two windings, N_s and N_P. Note that a second capacitor (C2) has been added to provide DC isolation for the "primary" winding of the inductor. Because of its position in the converter, this capacitance will see an average DC potential equal to that of the output voltage, V_o. Therefore, when S1 or D1 is conducting, both windings of L are forced to have *identical* voltage waveforms of *equal* magnitude. With a knowledge of the inductor's value (L_C), N_s, N_P, and L_{ext} can now be selected to reduce the dynamic "secondary" winding current to zero, using the criteria of Eq. (12.13) for $a = 1$.

The reader will recall that the converter of Fig. 12.13 was shown earlier in Chapter 8 (Fig. 8.5A) and can be implemented in a tapped form if desired. Although an output capacitor is shown (C1), it is not needed for ripple filtering. In practice, some capacitance is usually placed across the output of the converter to reduce second-order noise or to provide an instantaneous source of energy for dynamic loads.

Capacitor C2, on the other hand, is always required in this ripple reduction approach. Note that the elimination of the ripple current in N_s is produced by "steering" this dynamic current to the primary winding, N_P. Therefore, C2 can see significant dynamic current magnitudes and must be selected in size and value to properly handle them without excessive ESR power loss.

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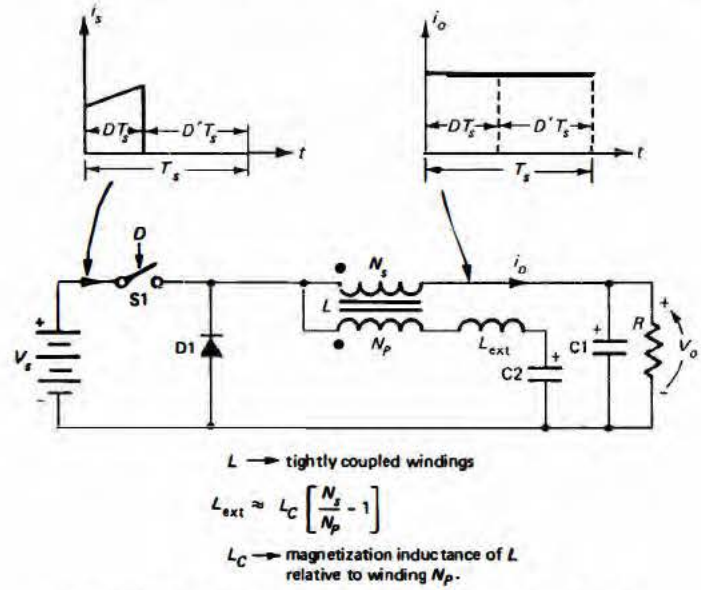


Fig. 12.13. Buck converter modified for zero output current ripple.

A basic boost converter can be altered in a similar fashion to achieve zero input ripple current. The resulting circuit is shown in Fig. 12.14. In this case, winding N_2 of the inductor is DC-isolated by capacitor C1, which sees a DC potential equal to that of the source voltage, V_s. Like the previous buck example, this isolation capacitor can see significant ripple current and its value and size must be chosen with care.

When two or more filter inductors of a converter see proportional equal voltages of equal frequency and phase, they can be placed on a common magnetic core and ripple currents adjusted so as to reduce one or more of them to essentially zero. Fig. 12.15 illustrates a coupled-inductor application in a two-output quasi-squarewave SPC. Here, the inductor of the second output, along with L_{ext}, is used to reduce the ripple current of the first output to zero. Again, we can use Eq. (12.13) to select L_{ext}; however, the proportionality constant, a, must now be set to approximately N_{s1}/N_{s2} of T1. The selection equation for L_{ext} accompanying Fig. 12.15 assumes that the four secondary diodes have negligible voltage drops and that T1 is an ideal transformer. Should either of these two assumptions not be valid, then the selection criteria for L_{ext} must be adjusted accordingly. The reader is referred back to Section 8.2 of Chapter 8 for further discussions of nonideal cross regulation of transformer windings and the effects of diode drops when dealing with SPCs with multiple unregulated outputs.

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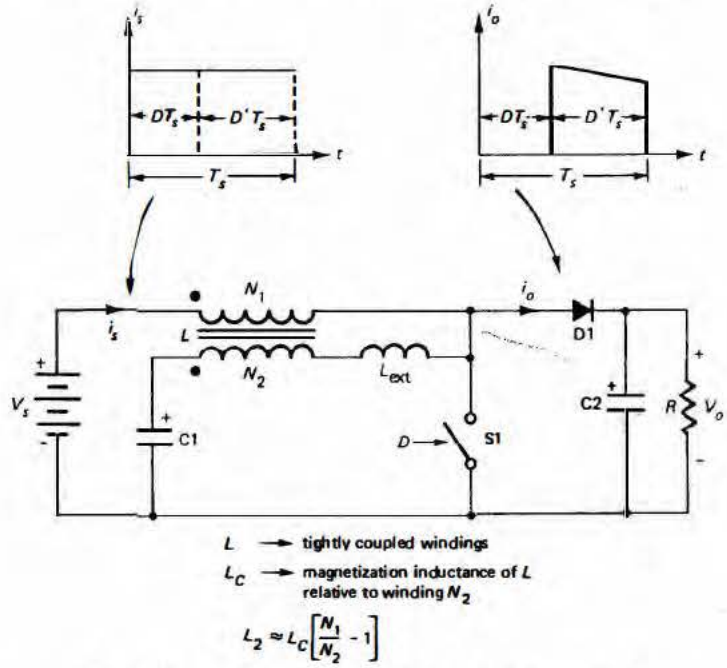


Fig. 12.14. Boost converter modified for zero input current ripple.

Fig. 12.16 shows one version of a basic Ćuk converter which uses two sets of coupled inductors to reduce *both* input and output ripple currents to zero. Here, both inductor assemblies require separate trimming inductances as well as decoupling capacitors. Another version of this same converter (Ref. 10) is shown in Fig. 12.17. In this case, by separating the energy transfer capacitance (C1 in Fig. 12.16) into two series parts, a common tie point for DC isolation of the secondary windings of both inductors is created. As a result, this zero-ripple Ćuk converter requires one less DC isolation capacitor than the circuit of Fig. 12.16.

12.5. THREE-WINDING INDUCTORS AND THE ZERO-RIPPLE PHENOMENON

Looking back at our examples of the last section, we see that a separate "tuning" winding was required to adjust the current ripple of a selected input or output inductor to zero. It is natural to inquire at this point if it is possible to devise a magnetic assembly whereby a *single* winding can *simultaneously* control the ripple current magnitudes in two other contemporary windings.

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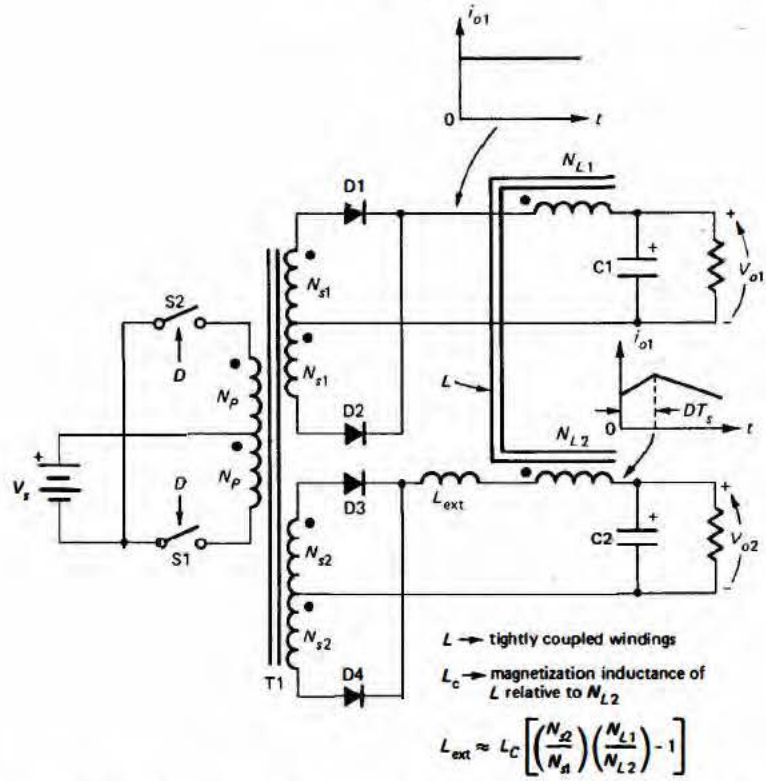
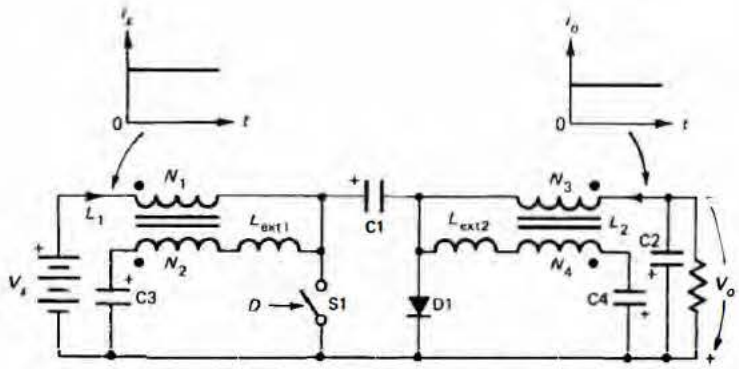


Fig. 12.15. Coupled-inductor quasi-squarewave converter with one output set for zero current ripple.

This combinational possibility is illustrated in a sequential fashion in Fig. 12.18. In part A, two separate magnetic assemblies are shown, each with two windings, with N selected as the ripple control winding in each case. A gap has also been placed into each core, as is the usual case for an inductor that will see a DC bias. In part B, we have placed the two cores from part A together with a common winding N. Finally, in part C, the two cores are combined into one structure, with winding N placed on its center portion.

Examination of the major flux paths illustrated in each part of Fig. 12.18 indicates that all three magnetic arrangements should be equivalent from an electrical standpoint, and that the single-core system of Fig. 12.18C is a viable scheme to permit winding N to control ripple current magnitudes in *both* winding N_1 and in winding N_2. To verify this idea, we will need to take a closer

VC00049717



L_1, L_2 → tightly coupled windings

L_{c1} → magnetization inductance of L_1 relative to N_2

L_{c2} → magnetization inductance of L_2 relative to N_4

$$L_{ext1} \approx L_{c1}\left[\frac{N_1}{N_2} - 1\right], \quad L_{ext2} \approx L_{c2}\left[\frac{N_3}{N_4} - 1\right]$$

Fig. 12.16. Ćuk converter variation using two sets of coupled inductors to achieve zero input and output ripple.

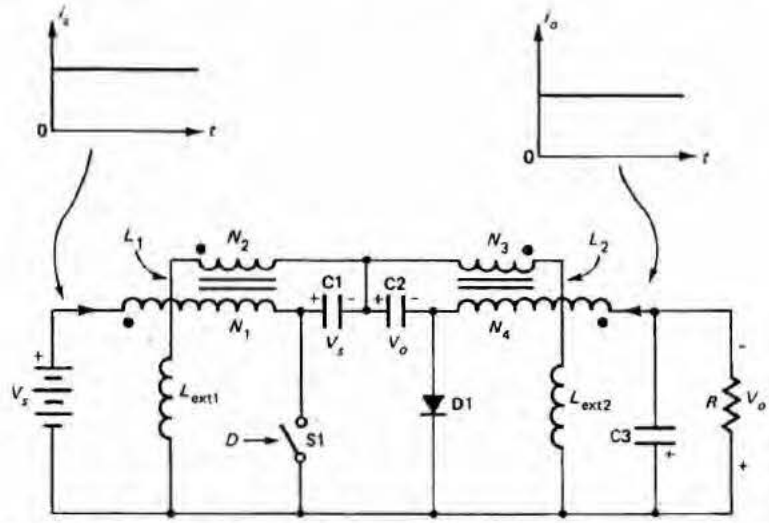


Fig. 12.17. Another variation of the Ćuk converter of Fig. 12.16 that uses one less decoupling capacitor.

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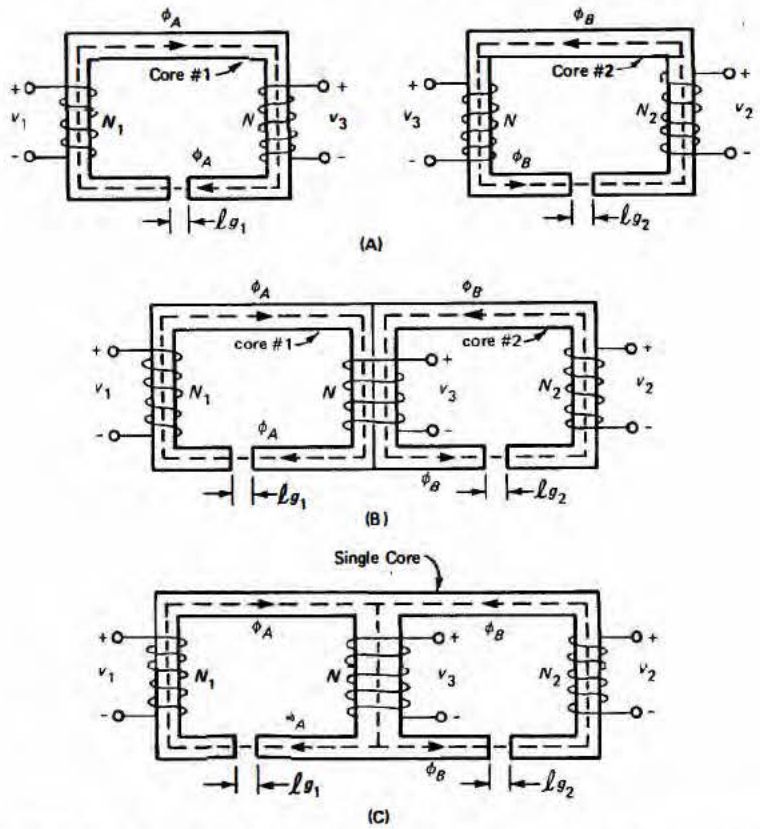
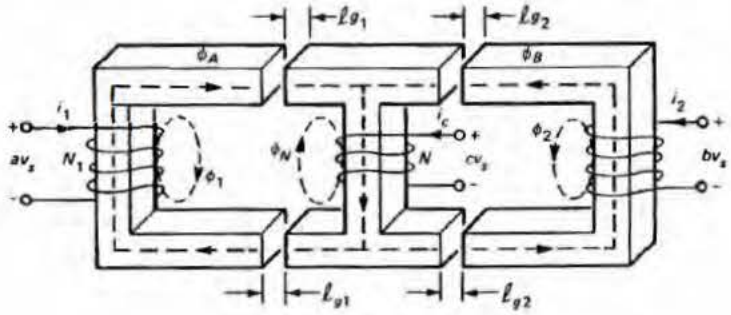


Fig. 12.18. Evolution of a single-core three-winding magnetic concept for zero current ripple control.

analytical look at the magnetic system of Fig. 12.18C in much the same manner that was followed for the two-winding inductor in Section 12.3.

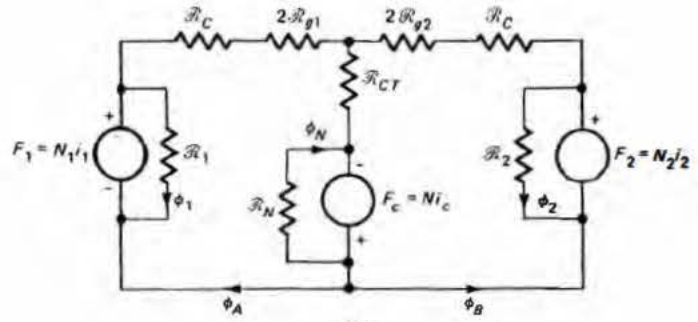
We begin by considering a similar three-winding magnetic assembly illustrated in Fig. 12.19A. In this instance, an I core is used as an interface between two C cores, with air gaps introduced at each of the four joints. For our analysis, we will assume that all three cores have identical permeability and cross-sectional areas, and that the two sets of air gap lengths are uniform with no fringing fluxes associated with them. Two major and three leakage flux paths are also assumed, with directions as shown, and each of the three windings is driven by a zero-impedance voltage source.

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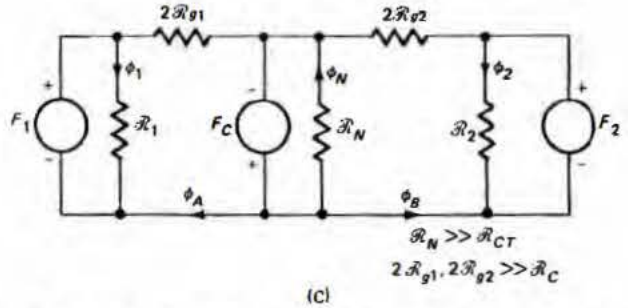


- material permeability of all cores = μ_m
- uniform cross-sectional area (A_C) throughout

(A)



(B)



(C)

Fig. 12.19. Developing a reluctance and mmf model for the magnetic of Fig. 12.18C.

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Again, we assume that all three voltage sources (av_s, bv_s, cv_s) are of similar shape, proportional in amplitude (set by constants a, b, and c), have the same frequency and phase, and constants $a, b, c > 0$.

With all important electrical and magnetic circuit conditions established, we now proceed as before to establish an equivalent circuit model. First, the basic reluctance and mmf topology is drawn with flux paths taken from Fig. 12.19A. This step is shown in Fig. 12.19B, with all series reluctances lumped together. $\mathcal{R}_C$ represents the total reluctance of each of two C core paths, with $\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_N$ as those to related winding leakage paths. $\mathcal{R}_{CT}$ is the reluctance of the I core material, with air gap reluctances designated by $\mathcal{R}_{g1}$ and $\mathcal{R}_{g2}$. For simplicity, we have omitted the actual equations here (as well as in future model developments of this chapter) for relating reluctance values to the mean dimensions of the cores and associated air gap lengths. For those interested in these details, they can be easily calculated using the rules followed earlier in the development of a circuit model for a simple inductor (see Figs. 12.2B and C).

To further simplify our work, we can also reasonably assume that the air gap reluctances will be much greater than those presented by the core materials. The elimination of $\mathcal{R}_C$ and $\mathcal{R}_{CT}$ from Fig. 12.19B results in the reduced reluctance model of Fig. 12.18C. Taking the dual of this simplified model produces the permeance network of Fig. 12.20A. Using the av_s winding as a reference, elements of this network are then scaled by N_1, resulting in a circuit model relating flux linkages to winding currents (Fig. 12.20B). Finally, all permeances are replaced by their corresponding inductance values and all flux linkages by voltage sources, scaled as necessary using ideal transformers with proper turns ratios (Fig. 12.20C).

We can further manipulate the electrical network model of Fig. 12.20C to place the leakage inductances associated with windings N and N_2 on the "primary" side of their respective ideal transformer. Performing this impedance translation results in the final network model shown in Fig. 12.21.

Once again, using the same simple procedure for model development, we have been able to reduce a rather complex magnetic circuit to a simplified electrically equivalent network. This network can now be used to establish the electrical conditions necessary to produce zero-ripple currents in the two outer windings, N_1 and N_2.

First, we see from the model of Fig. 12.21 that, if currents i_1 and i_2 have been reduced to zero, there can be *no* dynamic voltage drops across leakage inductances L_1 and L_2. This observation also implies that L_1 and L_2 could assume *any* values and still not be important in the determination of what model values are needed to produce zero ripple current conditions in their respective windings. It also can be deduced the values of the remaining model circuit elements, namely air gap inductances and the leakage inductance of the center winding, *will* be important in the production of the zero-ripple phenomenon.

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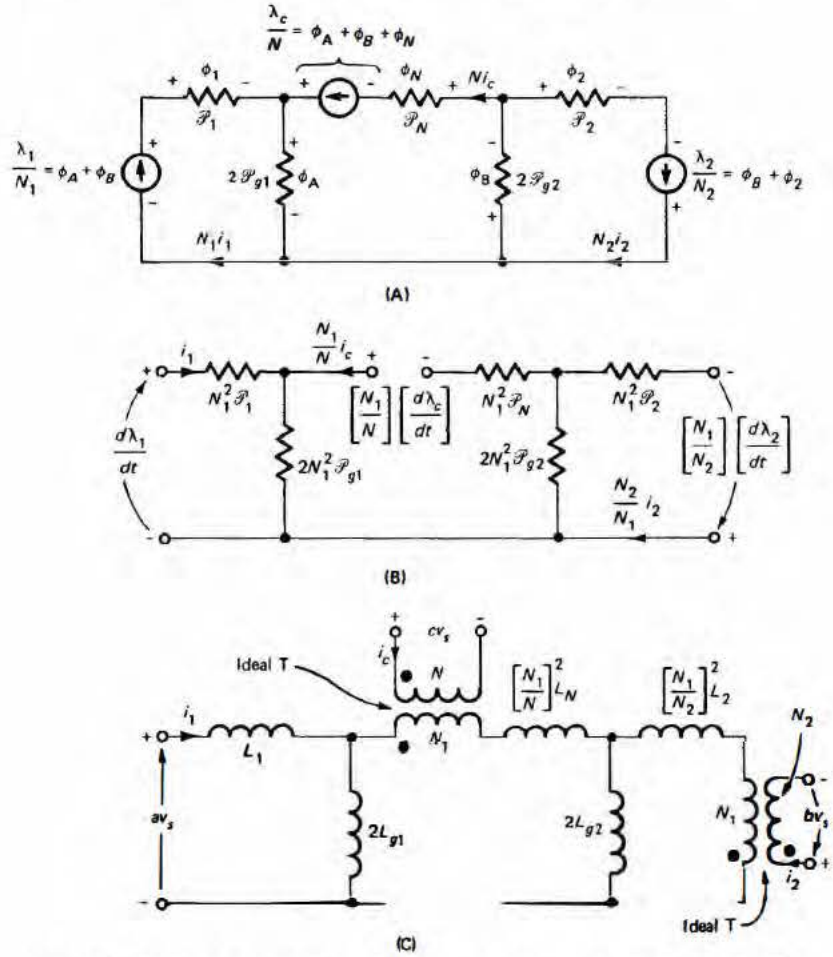


Fig. 12.20. Developing an electrical model from the reluctance network of Figure 12.19C.

With i_1 and i_2 equal to zero, we can redraw the model network of Fig. 12.21 to depict the circuit conditions that result from their absence. When this is done, the simplified model of Fig. 12.22 is obtained. Note that, with these currents set at zero, the voltages appearing across the gap inductances are, at most, simple reflections of associated winding voltages since their leakage inductance voltage drops must also be zero. We can now establish the relationships between L_N and that of the two gap inductances by simple network analysis as follows:

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$$av_s = \left(\frac{N}{N_1}\right)(2L_{g1})\frac{di_c}{dt} \tag{12.17}$$

$$b\left[\frac{N_1}{N_2}\right]v_s = \left(\frac{N}{N_1}\right)(2L_{g2})\frac{di_c}{dt} \tag{12.18}$$

$$cv_s - v_x = L_N\frac{di_c}{dt} \tag{12.19}$$

$$v_x = \frac{N}{N_1}\left[av_s + \left(\frac{N_1}{N_2}\right)bv_s\right]. \tag{12.20}$$

Combining Eqs. (12.17) and (12.18) with Eqs. (12.19) and (12.20) and eliminating the common di_c/dt terms gives:

$$\frac{L_N}{2L_{g1}} = \left(\frac{c}{a}\right)\left(\frac{N_1}{N}\right) - \left(\frac{b}{a}\right)\left(\frac{N_1}{N_2}\right) - 1 \tag{12.21}$$

$$\frac{L_N}{2L_{g2}} = \left(\frac{c}{b}\right)\left(\frac{N_2}{N}\right) \quad \left(\frac{a}{b}\right)\left(\frac{N_2}{N_1}\right) - 1. \tag{12.22}$$

Therefore, if the conditions set by Eqs. (12.21) and (12.22) are *simultaneously* satisfied, then the ripple currents in *both* windings N_1 and N_2 will be reduced to

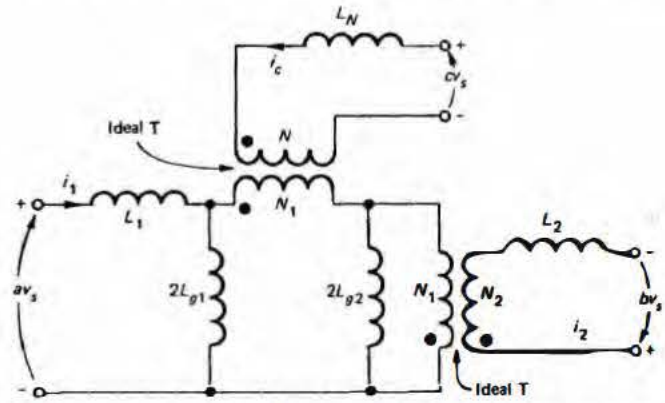


Fig. 12.21. Final equivalent electrical circuit for the three-winding magnetic system of Fig. 12.19A.

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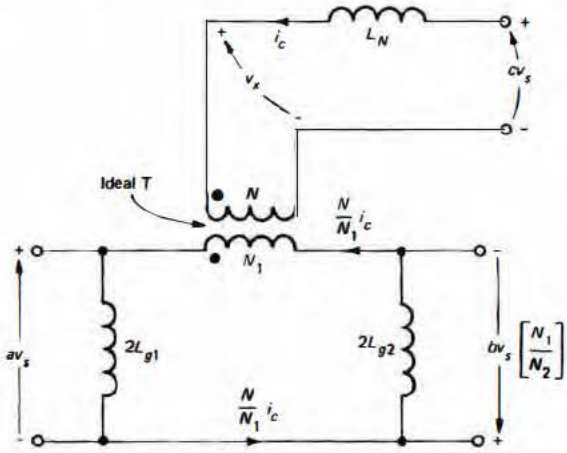


Fig. 12.22. Circuit conditions within the model of Fig. 12.21 when both i_1 and i_2 equal zero.

zero. Also, the effective inductance seen at the terminals of the center winding N will be equal to

$$L_e = L_N + \left(\frac{N}{N_1}\right)^2 [2L_{g1} + 2L_{g2}] \tag{12.23}$$

under these same conditions. Unlike the zero-ripple dual-winding inductor design criteria given in Section 12.3, note that Eqs. (12.21) and (12.22) are *not* interdependent. Therefore, assuming that winding turns and proportionality constants are known, values for the gap inductances L_{g1} and L_{g2} can be found that satisfy both of these equations for any fixed value of center leg leakage inductance, L_N.

For example, assume that we have a converter application where $a = 1$, $b = 2$, $c = 3$, and $N_1 = N_2$. Placing these values into Eqs. (12.21) and (12.22), one finds that gap inductance L_{g2} must be twice L_{g1}, and that the choice of N, N_1, and L_N will determine the actual gap inductance values needed to produce zero ripple currents in both N_1 and N_2.

Referring once again to the network of Fig. 12.22, we see that we can increase the effective value of the leakage inductance L_N by simply adding a small amount of *external* inductance in series with it, just as we did in the case of the two-winding inductor in Section 12.3. In actual design practice, it may be difficult to predict and maintain a constant value for L_N since it is essentially a parasitic component; therefore, supplementing it by external means could be very desirable, if not mandatory, for a production application.

VC00049724

With the conditions established to achieve current ripple reduction in two of the three windings of the assembly shown in Fig. 12.19A, let's take a look now at two applications of this unique magnetic in typical converter circuits.

12.6. MORE ZERO-RIPPLE CONVERTER APPLICATIONS

Figure 12.23 shows a three-output buck-derived quasi-squarewave converter with all output inductances wound on a common core. In this case, the ripple currents in the first and third outputs are controlled by the common inductance associated with the second output. Since the voltage waveforms across each of the three inductances are of the same shape, phase, and frequency, we can apply Eqs. (12.21) and (12.22) to select the air gap lengths and the leakage inductance of the center leg of the core to achieve zero ripple in the outer windings. In this application, the constants a, b, and c are established by the corresponding primary-

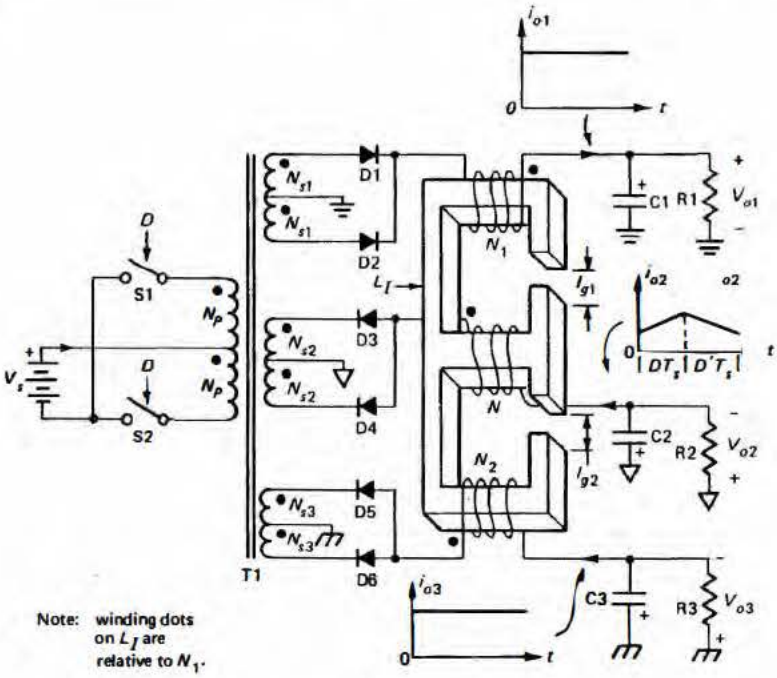


Fig. 12.23. A coupled-inductor three-output quasi-squarewave SPC with two outputs adjusted for zero current ripple.

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to-secondary turns ratio of T1 as:

$$a = \frac{N_{s1}}{N_P} \tag{12.24}$$

$$b = \frac{N_{s3}}{N_P} \tag{12.25}$$

$$c = \frac{N_{s2}}{N_P}. \tag{12.26}$$

Placing the above values for a, b, and c into Eqs. (12.21) and (12.22), and noting that we have only one air gap on each side of the center leg of the core in Fig. 12.23, gives:

$$\frac{L_N}{L_{g1}} = \left(\frac{N_{s2}}{N_{s1}}\right)\left(\frac{N_1}{N}\right) - \left(\frac{N_{s3}}{N_{s1}}\right)\left(\frac{N_1}{N_2}\right) - 1 \tag{12.27}$$

$$\frac{L_N}{L_{g2}} = \left(\frac{N_{s2}}{N_{s3}}\right)\left(\frac{N_2}{N}\right) - \left(\frac{N_{s1}}{N_{s3}}\right)\left(\frac{N_2}{N_1}\right) - 1. \tag{12.28}$$

The above equations assume that the various secondary diode drops are negligible and that the converter's transformer (T1) is an ideal circuit element. Therefore, it may be necessary to alter the values for a, b, and c to account for any deviation from this assumption, should these diode voltages or transformer parasitic contributions be significant. The reader is referred once again to Chapter 8 for more details of this particular problem.

Of all the various converter circuits, perhaps the Ćuk converter benefits the most from the use of an integrated magnetic design such as that shown earlier in Fig. 12.19. One such circuit variation (Ref. 11) is illustrated in Fig. 12.24. Here, the main energy transfer capacitance of the converter has been split into two series parts. Note that *two* isolated windings of equal turns (N) have been placed on the center leg of the magnetic assembly, with one winding tied to C1 and the other to C2. With these placements, both of the center-leg windings will *always* see a voltage waveform *identical* to that appearing across both outer windings (N_1 and N_2) of the magnetic assembly. Therefore, these two inner windings form a one-to-one transformer element, providing a means of DC isolation between V_s and V_o as well as ripple current control of both input and output lines.

The equations accompanying Fig. 12.24 give the criteria for selecting the two air gap lengths and are based on the conditions required by Eqs. (12.21) and (12.22). In many practical applications of this particular converter, the outer windings usually have the same number of turns ($N_1 = N_2$).

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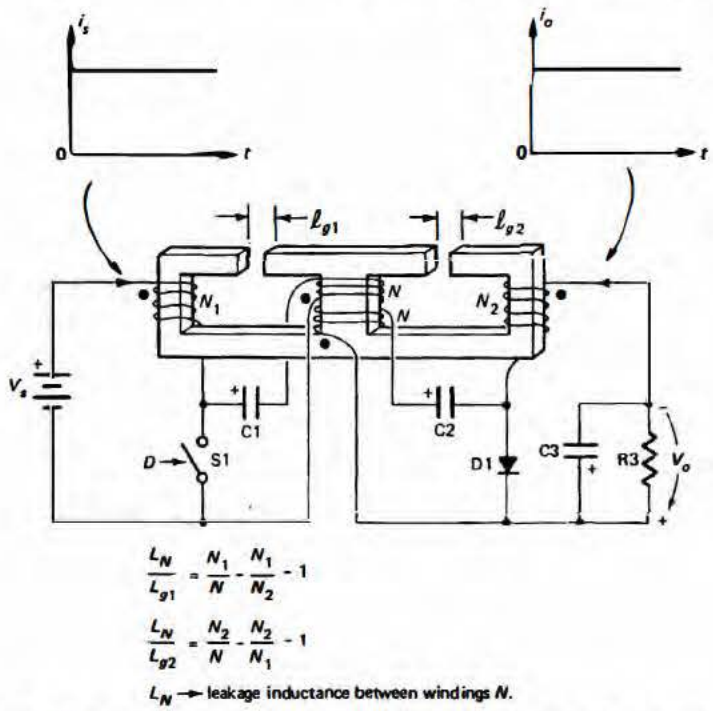


Fig. 12.24. Ćuk converter design that emulates a true DC transformer with turns ratio set by duty cycle D.

For this special case, our selection equations reduce to:

$$\frac{L_N}{L_{g1}} = \frac{N_1}{N} - 2 \tag{12.29}$$

$$\frac{L_N}{L_{g2}} = \frac{N_1}{N} - 2 \tag{12.30}$$

since $a = b = c = 1$. Therefore, it is apparent from Eqs. (12.29) and (12.30) that the two core air gap lengths will be *equal* for this particular case, again assuming that core cross-sectional areas are uniform and equal throughout.

Let us now pause for a moment and reflect on the significance of the Ćuk converter design of Fig. 12.24. Here, an SPC variation has been created which emulates a *true DC transformer*. The "turns ratio" of this DC transformer is set by the value of the switch duty cycle and is therefore *electronically variable*.

VC00049727

Both input and output currents can be made to be *nonpulsating* and will remain that way regardless of changes in converter switching frequency, switch or diode duty cycle, and load. In addition, all of its magnetics are contained within a *single* magnetic assembly, including a transformer for DC isolation of input and output voltages!

12.7. A FORWARD CONVERTER WITH INTEGRATED MAGNETICS

Up to this point, we have restricted our discussions of magnetic integration methods to those that directly relate to inductances with proportionally equal voltages impressed across them. With the single exception of the Ćuk converter variation just discussed (Fig. 12.24), we have excluded AC transformers from our design development of integrated magnetic SPCs. In the special case of this Ćuk-derived circuit, it was possible to fashion a single magnetic assembly which housed not only the two inductors of the converter, but also a 1:1 isolation transformer. All this was done with no compromise in conversion characteristics or performance.

The Ćuk converter is a unique SPC topology in that all inductor as well as any transformer windings must *always* have proportional voltages of equal shape, frequency, and phase. However, other converters are not as fortunate in this respect, and it is not readily apparent how one can magnetically combine inductive as well as AC transformer components in these circuits.

For example, consider the case of a buck-derived forward converter using the circuit variation shown in Fig. 5.20B of Chapter 5. Here, the windings of the isolation transformer T1 see voltages proportional to the source potential, V_s, while its inductor L sees voltages proportional to the difference between V_s and the output voltage, V_o. Since V_o is a function of switch duty cycle (D), the inductor's AC voltage will fluctuate in accord with changes in D. Similar observations can be made of transformer and inductor voltage waveforms in boost-derived converters, such as the single-ended design shown in Fig. 6.14 of Chapter 6.

However, we do know that the AC transformers and inductors of converters share a common dependency on flux change in ferromagnetic materials to perform their functions. Recall from the basic definition of inductance set by Eqs. (12.1) and (12.2) that flux change in any magnetic medium can be related to current variation as:

$$v = L\frac{di}{dt} = N\frac{d\phi}{dt} \tag{12.31}$$

or

$$d\phi = \frac{L}{N}di. \tag{12.32}$$

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We also remember from our previous modeling experiences of this chapter that many magnetic core structures have multiple flux paths. Depending on winding arrangements, it is therefore feasible to devise core structures wherein various components of flux add or substract from one another in some portions of its magnetic paths. Therefore, it would seem very probable that an integrated magnetic assembly could be conceived that would emulate as well as properly relate various flux changes one would expect in the inductors and transformers of an SPC.

Since it is possible by network analysis to formulate a set of equations that relate the various dynamic currents to circuit voltages for each conduction state of a converter, we can then modify them to relate currents to magnetic flux changes, using the conditions of Eq. (12.32). The modified equations then show how the flux changes of various magnetics of an SPC are interrelated and act as guides in constructing an integrated magnetic core system that satisfies the required relationships.

As an illustration of an SPC that was conceived using the above developmental method, let us examine the workings of a single-magnetic converter shown in Fig. 12.25. Here, two E cores have been joined with an air gap introduced only in the center leg section of the converter's magnetic component. At first glance, this SPC topology shows some resemblance to that of a forward converter; however, the output inductance used for energy storage when the switch (Q1) is in an OFF state is not readily discernable.

We can use the modeling tools of Section 12.1 to analyze the converter of

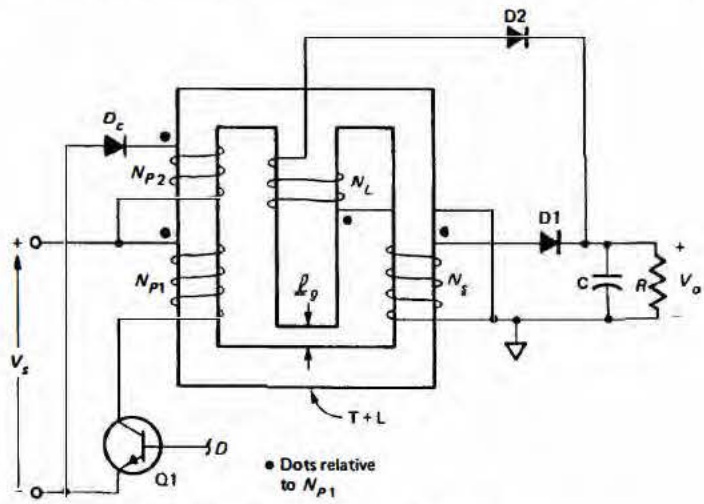


Fig. 12.25. An integrated magnetic forward converter.

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Fig. 12.25 to see if this inductor is "hidden" within its magnetic assembly. First, we isolate the magnetic and identify winding potentials and current directions. This is done in Fig. 12.26, with current directions corresponding to those that would result if the SPC switch and/or diodes were in a conducting state. Major flux paths and their directions resulting from the indicated winding currents are also identified, using the right-hand rule and the procedure given in Section 12.1 for "dotting" of the five windings relative to N_{P1}. Because we are interested only in the major flux paths for this investigation, secondary leakage flux paths are not considered here; however, they can be added at the expense of a more complicated model, just as was done for the examples in Figs. 12.4 and 12.19.

Next, the reluctance model for the magnetic assembly is drawn in Fig. 12.27A using the information contained in Fig. 12.26. Since the core structure is symmetrical and the air gap reluctance will be dominant in the center leg, the circuit model of Fig. 12.27A can then be simplified to that shown in Fig. 12.27B. Note also that the two left-hand mmfs can be combined into a single mmf because of their series connection in one leg of the core structure.

Once again, we can use duality relationships to convert the network of Fig.

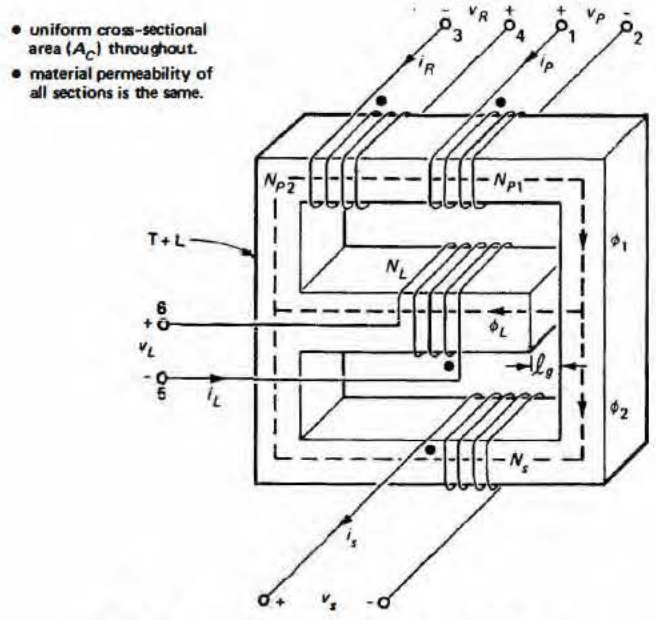


Fig. 12.26. Magnetic used in the SPC design of Fig. 12.25.

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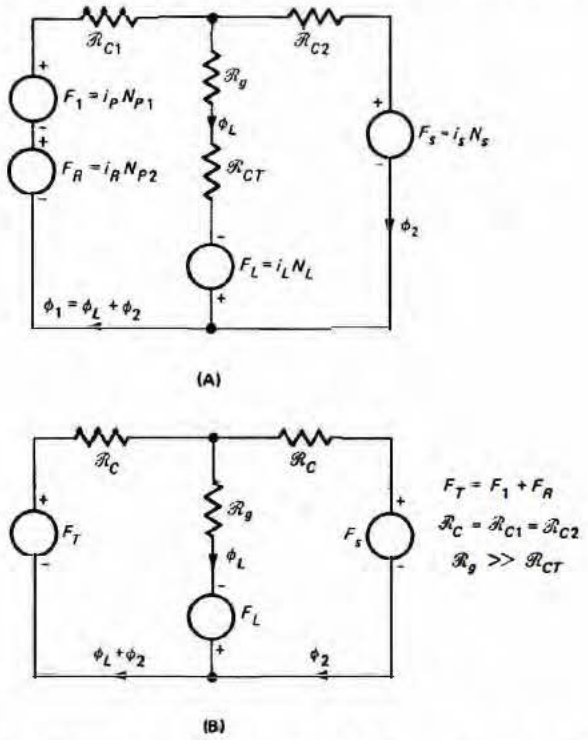


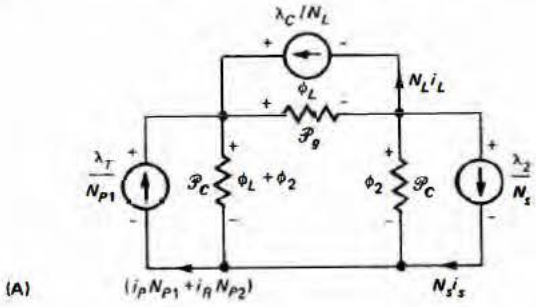
Fig. 12.27. Reluctance/mmf models for the magnetic of Fig. 12.26.

12.27B to one involving permeances, as is done in Fig. 12.28A. This new network is then scaled to the winding chosen as a reference. The circuit of Fig. 12.28B results from this scaling step, with N_{P1} designated as the reference winding. Finally, the scaled permeances are then replaced by inductances and ideal transformers added as required to refer winding currents to their terminal values, as shown in Fig. 12.28C.

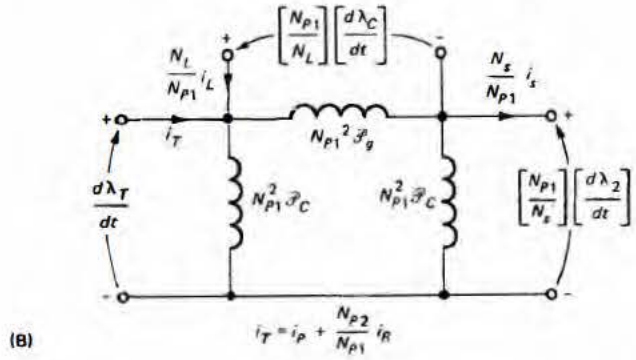
We now have an electrical model for the magnetic system of Fig. 12.26. Substituting this model into the converter of Fig. 12.25 results in the equivalent SPC circuit shown in Fig. 12.29. Note that, in making this substitution, we have also moved the gap inductance to the secondary side of the ideal transformer of turns ratio, $N_{P1}:N_s$. In making this impedance translation, the ideal transformer of turns ratio ($N_{P1}:N_L$) in Fig. 12.28C must also be moved and its ratio changed as indicated in Fig. 12.29.

The converter of Fig. 12.29 is now beginning to resemble a forward converter.

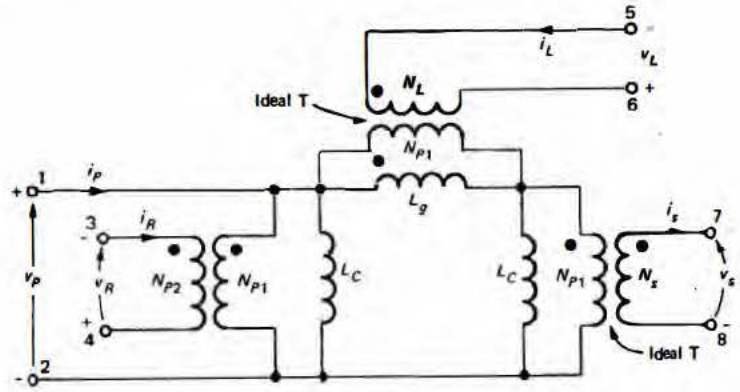
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(A)



(B)



(C)

Fig. 12.28. Development of an electrical circuit equivalent for the magnetic of Fig. 12.26 using the reluctance network of Fig. 12.27B.

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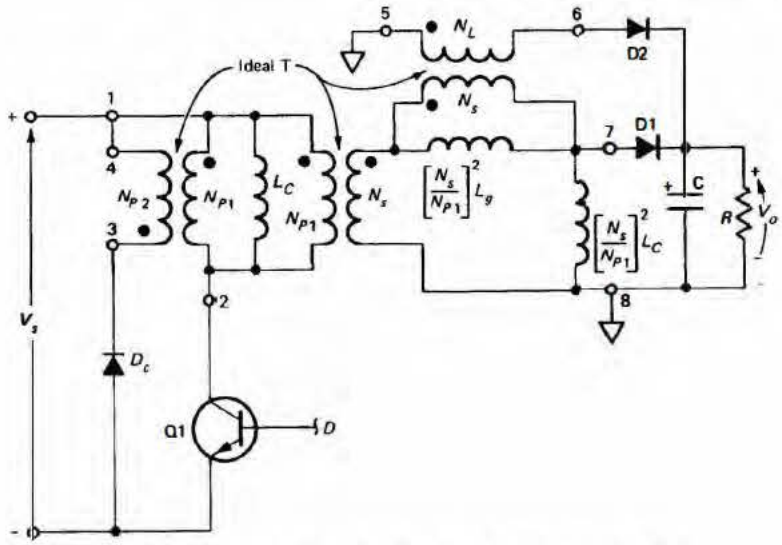


Fig. 12.29. Complete electrical circuit for the SPC of Fig. 12.25.

If we now assume that L_C is much greater than L_g and that $N_L = N_s$, the converter circuit can be further simplified to that of Fig. 12.30A. Note that we have also converted the ideal transformer of turns ratio (N_{P1}:N_s) in Fig. 12.29 to an imperfect one that has a finite value of magnetizing inductance set equal to L_c.

The topology of Fig. 12.30A can be reduced further by the elimination of the two remaining ideal transformers. The clamp winding on the primary side of the converter can be placed within T1 if N_{P1} and N_{P2} are wound tightly coupled. On the secondary side of the converter, the ideal 1 : 1 transformer associated with the reflected center leg inductance can be removed by manipulating the circuit positions of diodes D1 and D2 without compromising their conduction intervals.

The final converter structure that results from the elimination of all ideal transformers from the circuit of Fig. 12.30A is illustrated in Fig. 12.30B. Comparing this latter equivalent SPC to the forward design of Fig. 5.20B in Chapter 5, we find that the two topologies are identical!

Therefore, we can conclude that the SPC shown earlier in Fig. 12.25 is indeed an integrated-magnetic version of a buck-derived forward converter. It is also apparent from our analysis that the air-gapped center leg of this unusual magnetic assembly serves as an energy storage medium to supply output power when the primary switch (Q1) is in an OFF state. When Q1 is ON, energy in the center leg is replenished as well as transferred from the input source to the output via the outer legs of the core structure. Winding N_{P2} is used to return any energy stored in the outer legs to the source when Q1 is turned OFF.

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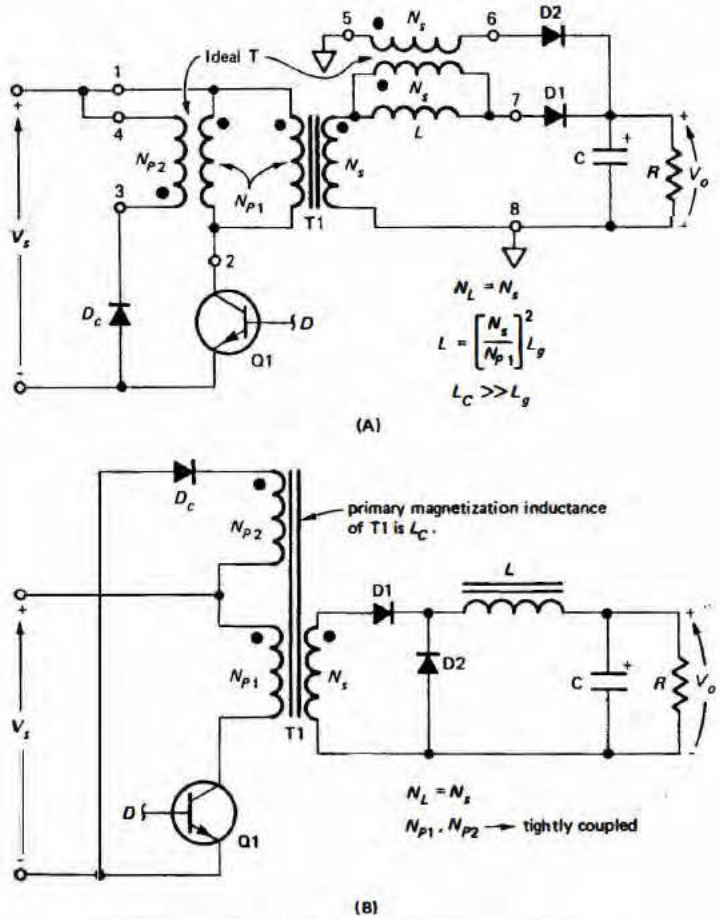


Fig. 12.30. Simplified versions of the converter in Fig. 12.29.

Assuming that the output current maintains a form that is continuous, the ideal voltage transfer function of this converter can be found by equating the volt-seconds experienced by the center leg winding during times DT and $D'T$. Ignoring all switch and diode voltage drops and assuming that conversion efficiency is 100%, the output-to-input voltage ratio is therefore found to be:

$$\frac{V_o}{V_s} = \frac{N_s}{N_{P1}} D, \quad N_L = N_s. \tag{12.33}$$

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Note that the ideal voltage transfer function of Eq. (12.33) is *identical* to that determined earlier in this textbook for a forward converter with discrete transformer and inductor magnetic elements.

Examination of the current waveforms in the switch and the diodes of this converter also confirms that is a buck-derived SPC. A typical set of these waveforms are shown in Fig. 12.31A. Note that the magnetization energy of the outer legs is returned to the source during $D'T$ intervals via diode D_c. Although the total output current (i_o) is shown to be continuous at the converter switching transitions, some discontinuity may be seen because of the loss of this magnetization energy. This discontinuity can be minimized by making the ratio of outer leg inductance to center leg inductance as large as possible (say 10 times) so that magnetization energy level will be small in comparison to that delivered to the load of the converter.

Contemporary voltage waveforms that would be observed in this converter are shown in Fig. 12.31B. Here, again, they are indicative of the dynamic potentials of a buck-derived forward design operating in a continuous mode. The waveform shown for the center leg winding assumes a measurement across N_L

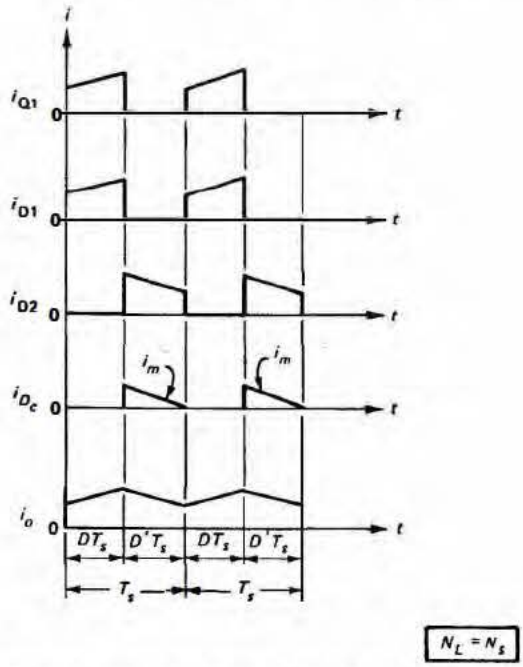


Fig. 12.31. (A) Typical current waveforms within the converter circuit of Fig. 12.25.

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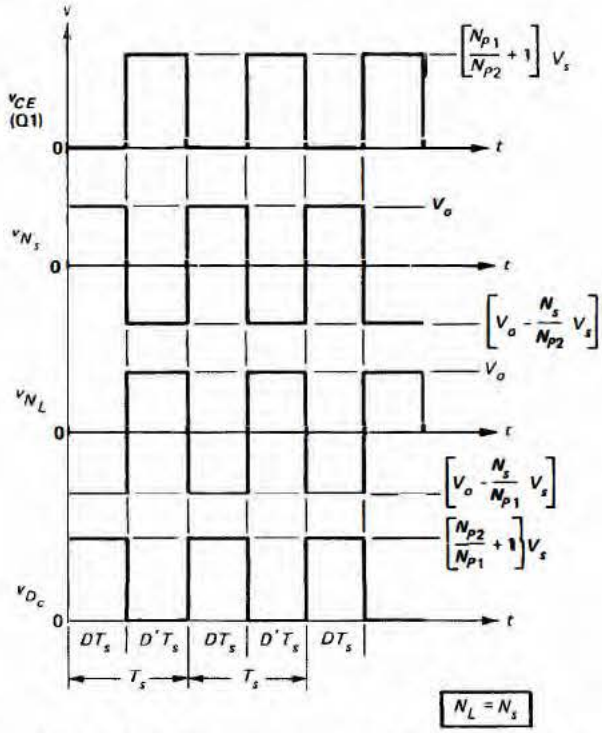


Fig. 12.31. (*Continued*) (b) Ideal voltage waveforms within the converter circuit of Fig. 12.25.

with ground reference at its "undotted" terminal, while that for diode D_c is taken at its cathode connection (terminal 3 in Fig. 12.29) with respect to the source voltage return.

Additional outputs can be accommodated by simply adding more inductor windings and commutating diodes on the center leg of the magnetic in Fig. 12.25, along with corresponding secondary windings and diodes placed on the outer leg. Also, in those applications where N_{P1} can be made equal to N_{P2}, then a single-primary version of the converter of Fig. 12.25 can be made. This SPC variation is shown in Fig. 12.32, where both switches (Q1 and Q2) are turned ON and OFF simultaneously. Diodes D3 and D4 then provide the path for return of magnetization energy to the source when both switches are OFF. The reader might recall that this particular core reset scheme was discussed previously in Chapter 4 (Fig. 4.10A). In fact, all of the core reset methods discussed in this earlier chapter are applicable to single-ended integrated magnetic SPC designs.

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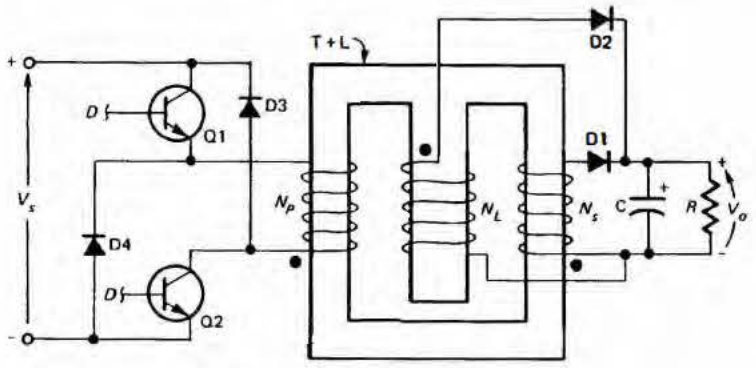
If we choose *not* to make N_L equal to N_s in the converter of Fig. 12.25, then the output current ripple will become somewhat discontinuous, just as might be expected in a forward converter with "tapped" inductor or transformer windings. The subject of magnetic tapping was covered in Chapter 8 and all alternatives discussed there for buck-derived SPCs apply as well to the integrated designs of Figs. 12.25 and 12.32.

12.8. AN ISOLATED BOOST SPC WITH INTEGRATED MAGNETICS

If we now apply the rules of bilateral inversion that we learned in Chapter 9 to the integrated forward design of Fig. 12.25, a dual boost converter approach can be derived. Fig. 12.33 shows the converter circuit that results from this duality exercise.

This particular SPC is an integrated magnetic version of a boost design shown earlier in Fig. 6.14A of Chapter 6. When switch Q2 is ON and switch Q1 is OFF, energy is stored in the air gap inductance of the center leg of the magnetic structure in Fig. 12.33. During these time intervals, the energy in the output capacitor C supplies load power needs. Also, any inductive energy stored in the outer legs of the structure is routed to the load via diode D3. When Q1 and Q2 reverse conduction states, the energy stored in the center leg is released to the output winding N through diode D1 and diode D3 turns OFF. With N_L set equal to N_P, the ideal voltage transfer function (continuous mode) for this converter is;

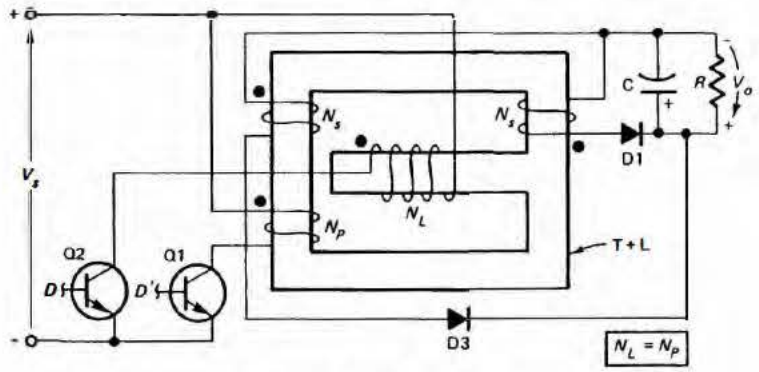
$$\frac{V_o}{V_s} = \frac{N_s}{N_P}\left[\frac{1}{1-D}\right] \tag{12.34}$$



Note: Dots relative to N_P.

Fig. 12.32. One variation of the integrated magnetic forward converter shown in Fig. 12.25.

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Note: Dots relative to N_p.

Fig. 12.33. An integrated magnetic boost converter.

which proves that this SPC is indeed a boost-derived design. This is to be expected, however, as the rules of bilateral inversion and duality must apply to all converter circuits, *including* those that have integrated magnetics.

12.9. RUDIMENTARY SYNTHESIS METHODS

Having established by analysis methods that the SPC circuits of Figs. 12.25 and 12.33 are integrated magnetic versions of basic buck and boost topologies with transformer isolation, let us now see if we can formulate an easy way to synthesize an integrated magnetic version of each of these SPCs, given the discrete-magnetic circuit arrangements as starting points.

To begin, we must first reconstruct the circuit schematics of these SPCs so as to detail the magnetic aspects of the transformer and inductor components. The schematics that result from this reconstruction process are illustrated in Figs. 12.34 and 12.35 for buck and boost versions, respectively. Note that a flux direction within each magnetic component has also been assigned, based on winding polarities produced by converter operation.

Next, for each of the two switching intervals of the converters (continuous mode of operation assumed), a set of equations defining the rate of change of flux in each magnetic component is established. These equations, of course, will be dependent on circuit voltage and the number of turns of related transformer and/or inductor windings. For this exercise, we can assume all semiconductors of the SPCs are ideal in order to simplify our work. Also, we will ignore potential leakage inductance effects between transformer windings for the same reason, and assume that fluxes are completely contained within its core structure.

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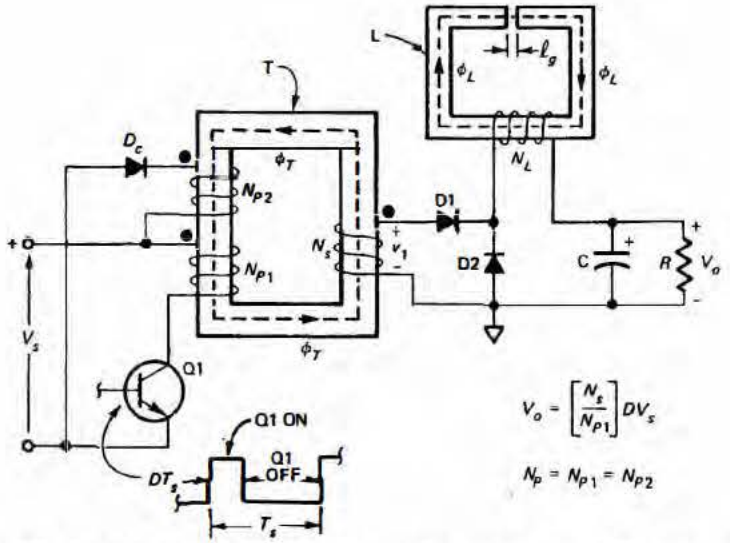


Fig. 12.34. The SPC of Fig. 5.20B redrawn to emphasize magnetic aspects of its transformer and inductor.

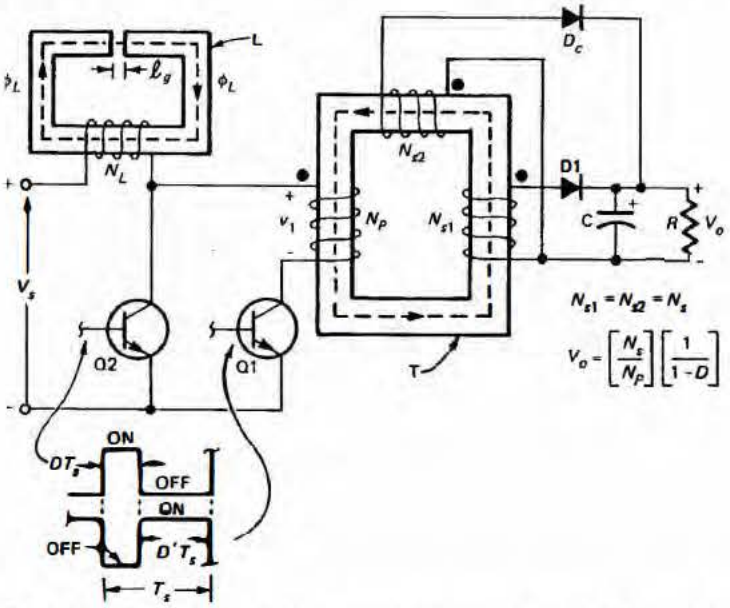


Fig. 12.35. The SPC of Fig. 6.14A redrawn to emphasize magnetic aspects of its transformer and inductor.

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Thus, for the buck converter of Fig. 12.34 during interval DT:

$$\frac{d\phi_T}{dt} = \dot{\phi}_T = \frac{V_s}{N_P} = \frac{V_1}{N_s} \tag{12.35}$$

$$\frac{d\phi_L}{dt} = \dot{\phi}_L = \frac{V_1}{N_L} - \frac{V_o}{N_L} \tag{12.36}$$

where $\dot{\phi}_T$ is the rate of flux change in the transformer core, $\dot{\phi}_L$ is the rate of change of inductor flux, and V_1 is the peak value of secondary voltage during DT. For the interval $D'T$:

$$\frac{d\phi_T}{dt} = \dot{\phi}_T = \frac{V_s}{N_P} \tag{12.37}$$

$$\frac{d\phi_L}{dt} = \dot{\phi}_L = \frac{V_o}{N_L}. \tag{12.38}$$

Referring back to Eqs. (12.35) and (12.36), we can combine them to eliminate the dependent variable, V_1. Performing this combination gives:

$$\dot{\phi}_T = \left[\frac{N_L}{N_s}\right]\dot{\phi}_L + \frac{V_o}{N_s}. \tag{12.39}$$

Note that the last term of Eq. (12.39) is of a form that could be considered as defining a flux change in a magnetic medium that is dependent on the output voltage, V_o, of the converter and the number of secondary turns on the converter's transformer, N_s. Also, it follows that, if we make this consideration, that the magnetic medium *must* be a part of the transformer assembly itself in order that the constraints on flux changes defined by Eq. (12.29) are satisfied. Therefore, we can rewrite Eq. (12.39) as:

$$\dot{\phi}_T = \left[\frac{N_L}{N_s}\right]\dot{\phi}_L + \dot{\phi}_o \tag{12.40}$$

where $\dot{\phi}_o = V_o/N_s$. Turning now to the first term of Eq. (12.39), we note that its contribution to $\dot{\phi}_T$ is dependent on a fraction, N_L/N_s, of the rate of change of flux in the SPC's inductor. Since our goal is to make the inductor a part of the same magnetic assembly that contains the transformer component, it is logical to assume that N_L should be made equal to N_s, so that *all* of this flux change is contained within one magnetic path or leg of this assembly. The reader may also recall that this same assumption permitted us to reduce the rather complex magnetic model of Fig. 12.29 to a form that facilitated recognition of this SPC as a

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buck-derived converter. Therefore, setting $N_L = N_s$ in Eq. (12.40), we arrive at an expression for $\dot{\phi}_T$ as:

$$\dot{\phi}_T = \dot{\phi}_L + \dot{\phi}_o . \tag{12.41}$$

Remembering our magnetic modeling experiences from earlier sections of this chapter, we can interpret Eq. (12.41) as defining a magnetic assembly in which there are three major flux paths. It also tells us that the flux change in an input source-related path (ϕ_T) contributes to the change in another path associated with the inductor portion of the magnetic assembly (ϕ_L), as well as to flux change in a third path (ϕ_o). From Eq. (12.40), this third leg must be related to output voltage value.

These general observations permit us now to sketch out a magnetic path arrangement that satisfies the needs of Eq. (12.41). This is done in Fig. 12.36A. Note that we have added a gap in the "inductor" path area because we expect this leg will have significant DC bias, just as a discrete inductor in a buck converter would experience.

Having found a magnetic arrangement that meets the flux change relationships for the interval DT, we now use Eqs. (12.38) and (12.39) to establish similar relationships for the interval $D'T$. This is done keeping in mind the core arrangement of Fig. 12.36A is still needed for the interval DT. The resulting magnetic system is shown in Fig. 12.36B.

To complete our synthesis effort, we now combine the two magnetic arrangements of Fig. 12.36 into a single magnetic element, adding surrounding switches

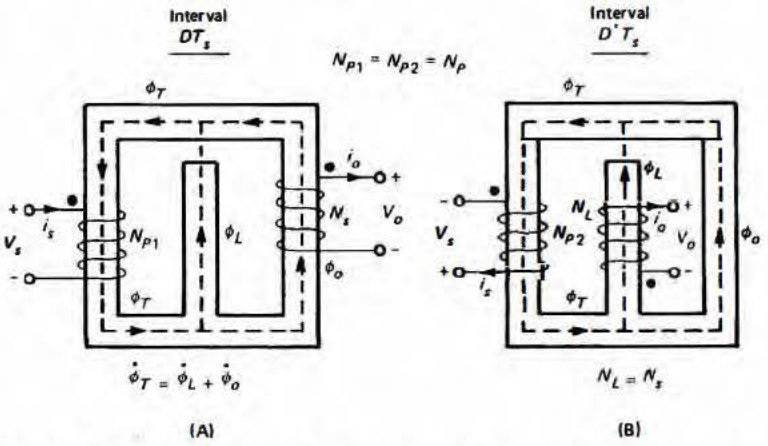


Fig. 12.36. Synthesizing the required magnetic paths for integration of transformer and inductor in a forward converter.

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and diodes to satisfy the needs of each of the two switching states of the SPC. This final step results in the integrated magnetic forward converter shown earlier in Fig. 12.25 of this chapter!

The total synthesis procedure can be repeated for the boost converter of Fig. 6.14A from Chapter 6. First, the converter is redrawn as shown in Fig. 12.35, emphasizing the magnetic aspects of its inductor and its transformer. Second, the idealized flux change rates for each magnetic are found using this schematic. For the interval DT:

$$\frac{d\phi_L}{dt} = \dot{\phi}_L = \frac{V_s}{N_L} \tag{12.42}$$

$$\frac{d\phi_T}{dt} = \dot{\phi}_T = \frac{V_o}{N_s}. \tag{12.43}$$

Repeating for the interval $D'T$:

$$\frac{d\phi_L}{dt} = \dot{\phi}_L = \frac{V_1}{N_L} - \frac{V_s}{N_L} \tag{12.44}$$

$$\frac{d\phi_T}{dt} = \dot{\phi}_T = \frac{V_1}{N_P} = \frac{V_o}{N_s}. \tag{12.45}$$

We now combine Eqs. (12.44) and (12.45) to eliminate the intermediate variable, V_1, and set $\dot{\phi}_s = V_s/N_P$:

$$\dot{\phi}_T = \left[\frac{N_L}{N_P}\right] \dot{\phi}_L + \dot{\phi}_s. \tag{12.46}$$

As was the case for the forward design just discussed, Eq. (12.46) indicates that N_L should be made equal to N_P to contain all inductor flux change within one path of the magnetic assembly under consideration. Therefore:

$$\dot{\phi}_T = \dot{\phi}_L + \dot{\phi}_s, \quad N_L = N_P. \tag{12.47}$$

Next, we use Eq. (12.47) as a guide in sketching a magnetic core arrangement for the interval $D'T$, adding a gap in the "inductor" leg for DC bias toleration. Another arrangement sketch is prepared for the interval DT, using the conditions of Eqs. (12.42) and (12.43) as guides. Finally, the two sketches are combined, along with SPC switches and diodes to set the magnetic states for each portion of the switching interval. The final circuit that results is (as we might expect at

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this point) identical to that shown in Fig. 12.33! The reader may recall that this particular integrated magnetic SPC was originally evolved by applying bilateral inversion to the SPC of Fig. 12.25.

This rudimentary synthesis procedure is fairly simple and straightforward to apply to any SPC circuit. While neither rigorous nor exact in results, it does yield an integrated magnetic version of any SPC quickly, and gives good insight as to the major magnetic aspects of the required core arrangements and construction needs.

12.10. MORE COMPLEX CONVERTERS WITH INTEGRATED MAGNETICS

The single-ended integrated magnetic forward converter of Fig. 12.25 can be modified so as to use two primary switch elements operating in a so-called "push-pull" manner. Two versions with this modification are shown in Fig. 12.37 (Ref. 12). In Fig. 12.37A, an additional set of primary and secondary windings have been added with "dot" polarities referenced to the primary winding controlled by switch Q1. In this version, when either of the primary switches is ON, energy is stored in the air gap of the magnetic's center leg. When Q1 is ON and Q2 is OFF, energy is also transferred from input to output via diode D1. When Q2 is ON and Q1 is OFF, D2 provides the input-to-output energy transfer path. When both primary switches are OFF, the energy stored in the center leg is routed to the output via diode D3. The ideal voltage transfer function for this push-pull version can be determined to be:

$$\frac{V_o}{V_s} = \left[\frac{N_L}{N_P}\right]\left[\frac{D}{1 - D\,[1 - (N_L/N_s)]}\right] \tag{12.48}$$

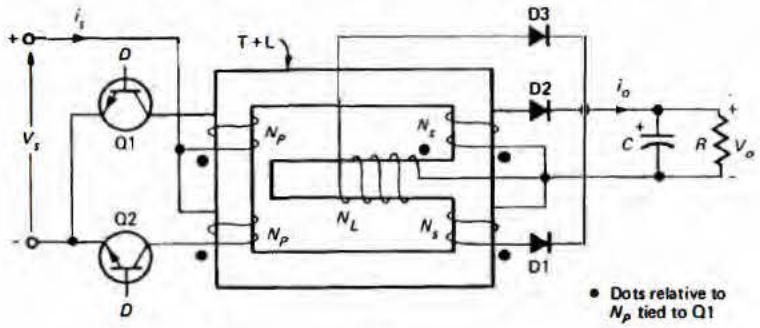
assuming that the converter is operating in a continuous output current mode. If N_L is made equal to N_s, Eq. (12.48) reduces to:

$$\frac{V_o}{V_s} = \frac{N_s}{N_P} D \tag{12.49}$$

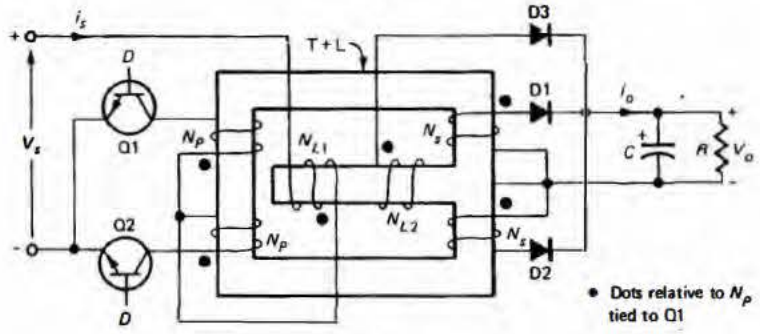
which is the transfer function of a quasi-squarewave buck converter, such as the circuit shown in Fig. 5.13A of Chapter 5.

In the second push-pull variation shown in Fig. 12.37B, secondary winding dot polarities are such that only magnetization energy would be stored in the center leg of its magnetic when either Q1 or Q2 is ON. Therefore, an additional winding tied to the primary source of power (N_{L1}) has been placed on the center leg to provide another source of energy storage during switch conduction

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(A)



(B)

Fig. 12.37. Push-pull versions of the integrated magnetic forward converter of Fig. 12.25.

intervals. The voltage transfer function for this converter variation is then determined to be:

$$\frac{V_o}{V_s} = \frac{1}{(N_P/N_s) + (D'/D)(N_{L1}/N_{L2})} \tag{12.50}$$

for the continuous mode of operation. If we choose to make:

$$\frac{N_P}{N_s} = \frac{N_{L1}}{N_{L2}} \tag{12.51}$$

then the transfer function set by Eq. (12.50) becomes:

$$\frac{V_o}{V_s} = \frac{N_s}{N_P} D. \tag{12.52}$$

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This is the same transfer function that one would expect from the buck-derived Weinberg converter shown in Fig. 5.9A in Chapter 5! Thus, we can conclude that the push-pull SPC variation illustrated in Fig. 12.37B is simply an integrated magnetic version of the Weinberg converter circuit.

The various current waveforms and their timing relationships that one would expect in *either* of these two converters is illustrated in Fig. 12.38. Note that, during the times when both switches are OFF, the magnetization energy stored in the outer legs of the magnetic structure causes either D1 or D2 to conduct, thus releasing this energy to the output. The output current into the converter load and capacitance thus will be the sum of the current produced by this energy (i_o) and that flowing in D3 during these times. As shown, the total output current will normally have a slight "step" because of this summation when the two switches are turning ON or OFF. Because this energy is usually small in comparison to that stored in the center leg of the magnetic, the magnitude of this "step" will be minute and can be neglected in most instances.

Fig. 12.38B illustrates the ideal voltage waveforms at various nodes within the converters of Fig. 12.37. The time sequence of these waveforms corresponds to that of the component currents shown in Fig. 12.38A. Note that the maximum OFF voltage appearing across either of the converter's primary switches is a function of primary-to-secondary turns ratio, as well as both input and output volt-

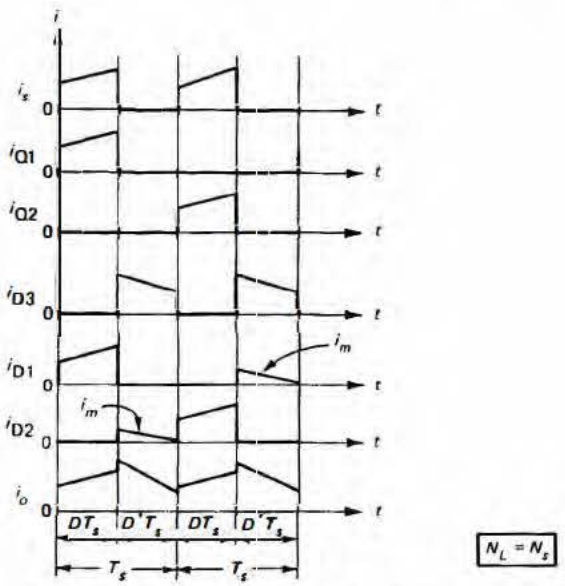


Fig. 12.38. Typical current waveforms within the converters of Fig. 12.37.

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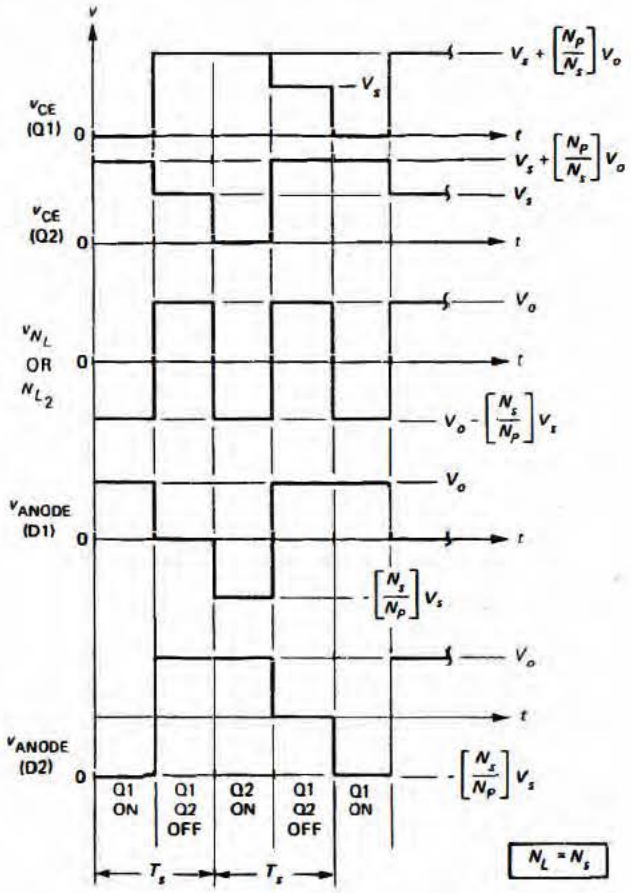


Fig. 12.38. (*Continued*)

age value. In contrast, comparable discrete-magnetic circuit counterparts, such as that shown in Fig. 5.13A in Chapter 5, will have an ideal OFF voltage stress on each primary switch that is *twice* that of the source voltage, V_s. Therefore, by judicious choice of turns ratio of transformer windings, the integrated converters of Fig. 12.37A can be purposely designed to impose *lower* OFF voltage stresses on their switches.

From a practical design standpoint, the converter version in Fig. 12.37B is preferred over that in Fig. 12.37A. Note that in version A, corresponding primary and secondary windings are on opposite sides of the core structure and therefore

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cannot be wound tightly together to minimize leakage inductances. By contrast, in version B just the opposite is true. Therefore, voltage transients produced by stored energy in leakage inductances during switching intervals will be much smaller in version B than in version A, thus reducing the electrical stress on converter primary switches and output diodes.

Since the converter magnetic of Fig. 12.37B contains an inductive winding in series with the outer leg primary winding, instantaneous current increase in either of the two primary switches due to conduction overlap is automatically prevented. However, this is not the case for its companion converter shown in Fig. 12.37A. Thus, the circuit of Fig. 12.37A can be considered a *voltage-fed* integrated magnetic converter, while the other version shown in Fig. 12.37B is a *current-fed* integrated magnetic converter. In fact, an integrated magnetic version of any converter circuit *must* retain *all* electrical properties of its discrete magnetic circuit counterpart to be truly contemporary in voltage and current transfer characteristics.

Using the magnetic modeling methods described earlier in this chapter, equivalent circuits for analyzing the electrical characteristics of the converters of Fig. 12.37 can easily be found. These equivalent networks are shown in Figs. 12.39 and 12.40, respectively. Note the similarity of the models of the magnetics to that shown earlier in Fig. 12.28 for the integrated forward converter. This similarity is to be expected, however, as the main inductive parts of the models should be the same; however, the basic model is changed to reflect the presence of additional windings on various legs of the magnetic cores in each instance.

Adding the provisions for two or more outputs from the two converters of Fig. 12.37 is a matter of adding more center leg and secondary windings, as is done in Fig. 12.41 for version B. This multi-output converter is an integrated

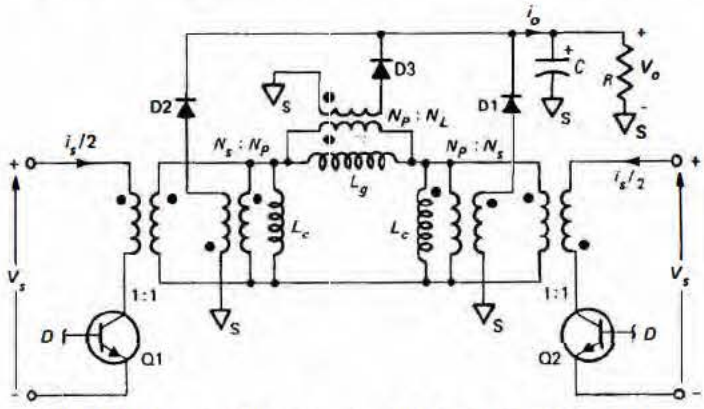


Fig. 12.39. Equivalent electric circuit model for the SPC of Fig. 12.37A.

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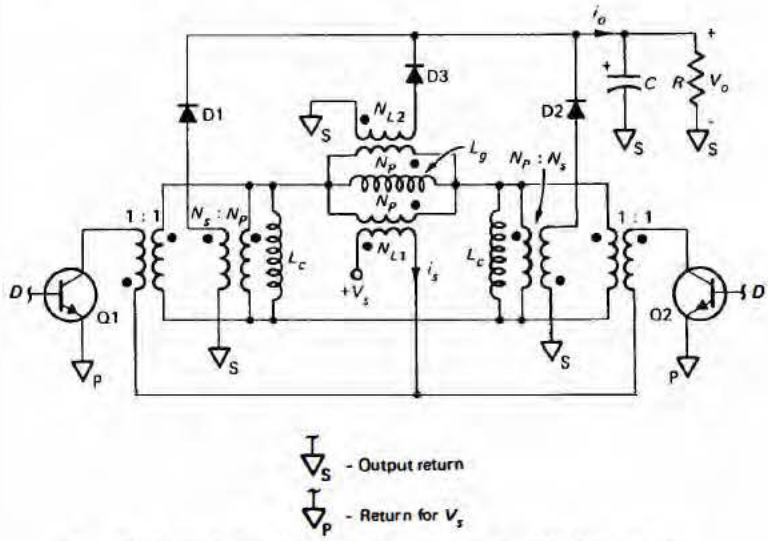


Fig. 12.40. Equivalent electric circuit model for the SPC of Fig. 12.37B.

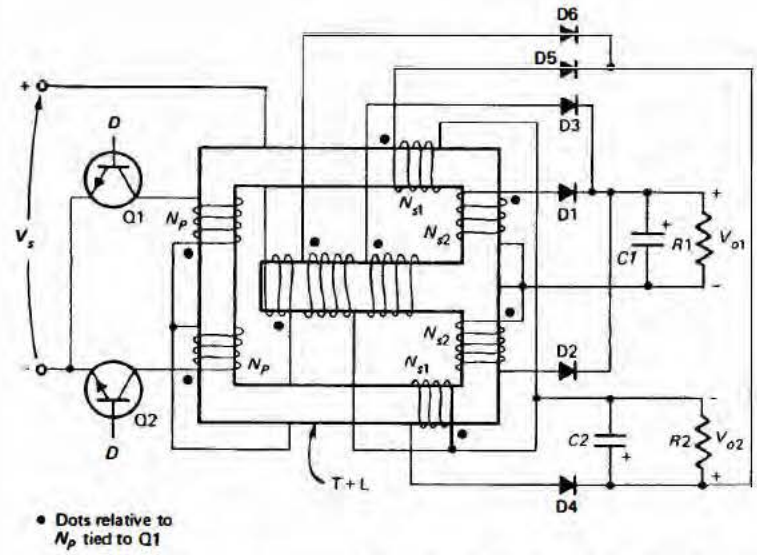


Fig. 12.41. A two-output version of the push-pull SPC shown in Fig. 12.37B.

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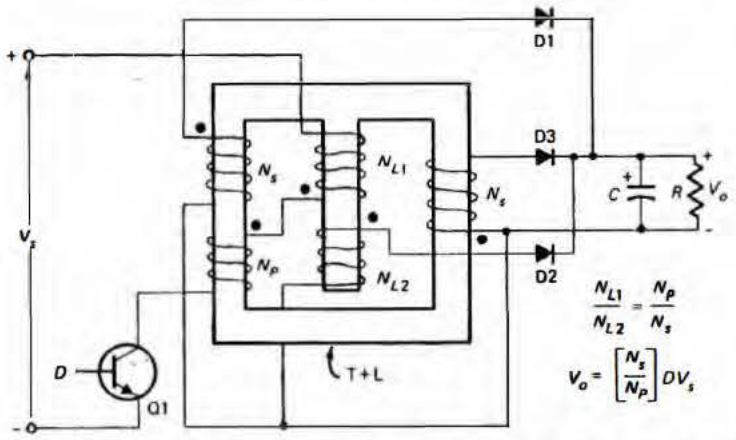


Fig. 12.42. An integrated magnetic version of the single-ended Weinberg converter shown in Fig. 5.25 of Chapter 5.

magnetic SPC whose discrete two-magnetic counterpart is the converter shown in Fig. 5.9B of Chapter 5.

With the extension of the integrated magnetic concept from single-switch to two-switch quasi-squarewave SPCs, it follows that we can apply it to other buck and boost-derived converters that have even more switches and diodes. Figs. 12.42 through 12.46 show five examples of more complicated possibilities, using

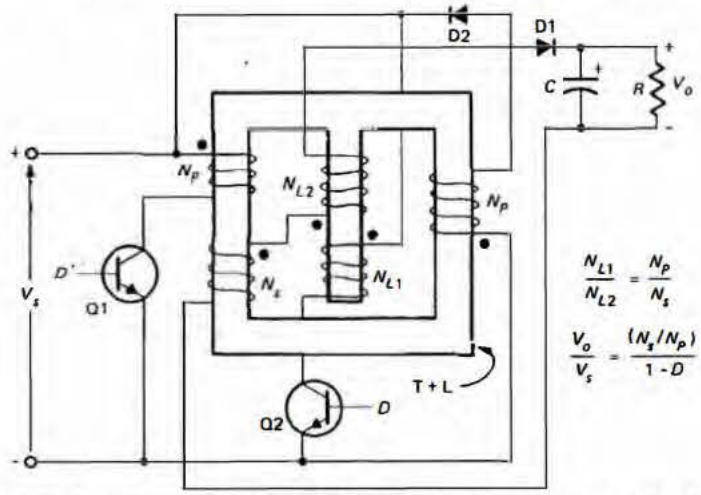


Fig. 12.43. Dual converter circuit to the integrated magnetic design of Fig. 12.42.

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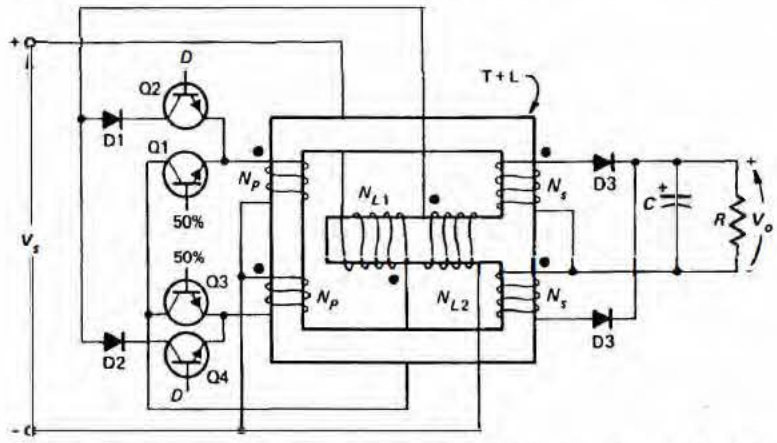


Fig. 12.44 An integrated magnetic version of the Severns converter shown in Fig. 5.8 of Chapter 5.

converter designs taken from Chapters 5, 8, and 9. Note that, in each of these five cases, even though the surrounding electronic circuit topology is more involved, the integrated magnetic structure is *still* a three-legged arrangement, with an air-gapped center leg performing the required inductive storage functions.

At this point in our work, it should be very evident that an integrated magnetic approach can be conceived for *any* buck or boost-derived SPC circuit. Although we have not specified a rigorous synthesis procedure here, evolution steps are

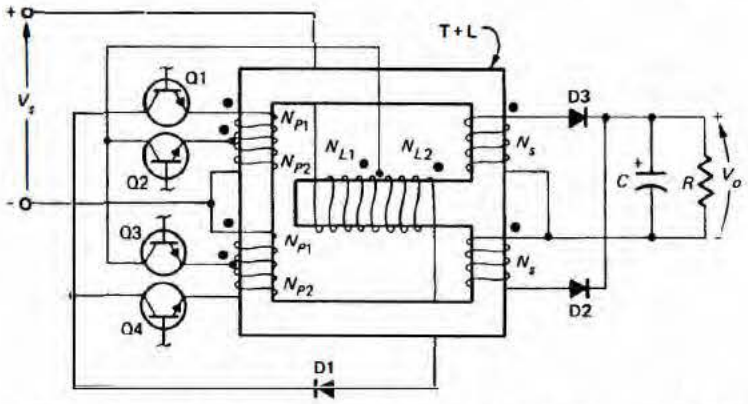


Fig. 12.45. An integrated magnetic version of the Hughes converter shown in Fig. 8.19 of Chapter 8.

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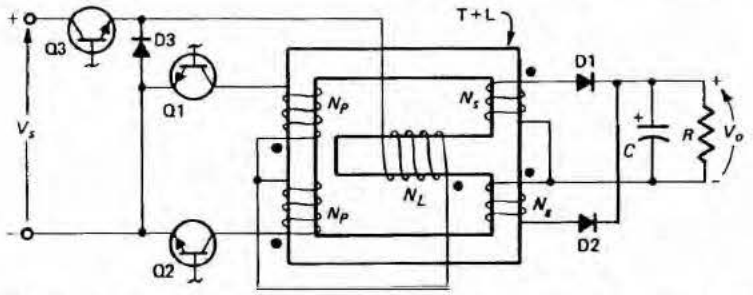


Fig. 12.46. An integrated magnetic version of the multi-mode converter shown in Fig. 9.14 of Chapter 9.

simply a matter of defining the flux relationships that exist in each magnetic component of a converter from a knowledge of the voltage and current relationships for each converter conduction state. Once these relationships are established, a magnetic structure that reproduces the flux additions or subtractions defined by the state equations is then constructed and appropriate transformer and/or inductive windings located to provide the required mmfs to produce the fluxes needed.

A more intuitive approach to synthesis is to first assume that the final magnetic structure will be three-legged, with an air-gapped center leg reserved for all inductive converter functions. All transformer windings are then placed on the outer portions of the structure, with primaries located on one outer side and secondaries on the opposite outer side. With a knowledge of the topology of the converter to be magnetically integrated, begin to interconnect the inductive and transformer-related windings until the desired magnetic relationships are satisfied. This step may require a number of iterations, but usually not many. As an aid in this interconnect procedure, assume that the inductive center leg is "isolated" from the outer legs, and that the outer legs are reserved only for transformer functions.

12.11. SMALL-SIGNAL MODELING CONSIDERATIONS

With the ability to easily develop an equivalent electrical model for any magnetic circuit regardless of its complexity, we can then apply the small-signal modeling methods of Chapter 10 to examine dynamic responses of importance for converter stability and control. The equivalent electrical model is simply substituted for the magnetic system within the converter being examined, and small-signal modeling and analysis methods applied to the resulting circuit.

For example, recall that we were able to develop equivalent circuit models for the integrated magnetic forward converter of Fig. 12.25. These models are

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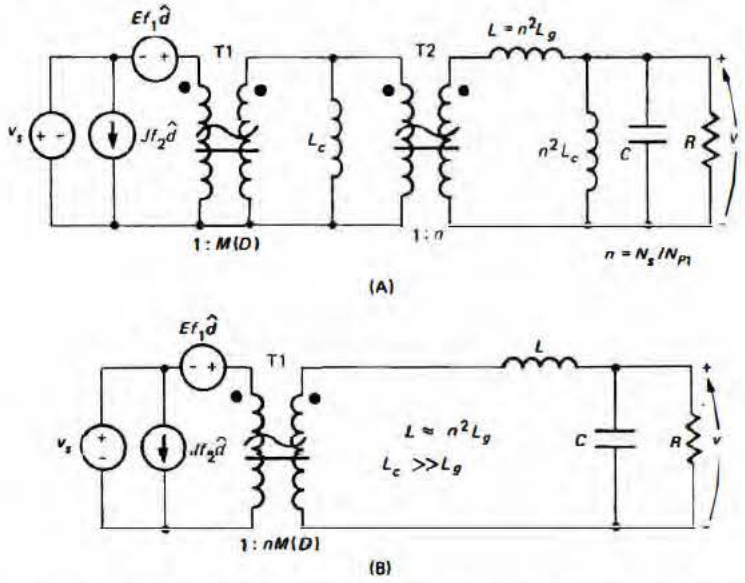


Fig. 12.47. Small-signal modeling of the integrated magnetic forward converter of Fig. 12.25.

illustrated in Figs. 12.30A and B. Since we were able to deduce that this particular converter was of the buck family, then the small-signal canonical model for a transformer-isolated buck SPC should apply, such as the one shown in Fig. 10.5 of Chapter 10.

Placing the various components of the electrical model of Fig. 12.30 into the proper canonical form results in the small-signal model of Fig. 12.47A. Note that we have retained all inductive elements in this instance. If we assume that the value of L_c is much greater than that of the air gap inductance, L_g, then a simplified canonical model can be constructed, as shown in Fig. 12.47B, which corresponds to the SPC of Fig. 12.30B.

Once again, the utility of the canonical model for SPCs becomes very evident. Addition to this model of various inductances and/or transformer elements that may be present in an integrated magnetic SPC is simple and straightforward, and their effects on small-signal responses readily found by inspection of their circuit position within the canonical model.

12.12. RIPPLE CURRENT CONTROL FOR BUCK AND BOOST CONVERTERS WITH INTEGRATED MAGNETICS

As was demonstrated in Section 12.4, auxiliary windings can be added to the inductors of basic buck and boost converters to facilitate control and reduction of

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input or output ripple currents. In a similar manner, windings can also be added to the center legs of the integrated magnetic versions of these converters to reduce input or output ripple current magnitudes.

For example, if a second winding is added to the gapped center leg of the magnetic used in the forward converter of Fig. 12.32, along with a DC isolation capacitor and a small external inductor for ripple trimming, then we can utilize the transformer equations of Section 12.3 to select the number of turns of this second winding so as to adjust the SPC's load current ripple to essentially zero!

The resulting integrated magnetic forward converter is shown in Fig. 12.48. The external inductor (L_{ext}) is defined to first order by the equation accompanying this figure, assuming that $N_{L1} = N_s$, and that the gap inductance (L_g) is much smaller than that of the ungapped outer legs of the magnetic structure. Both center leg windings are wound tightly together to maximize magnetic coupling between them and to minimize parasitic leakage inductances. The DC blocking capacitor, C2, is usually made large to minimize voltage ripple across it.

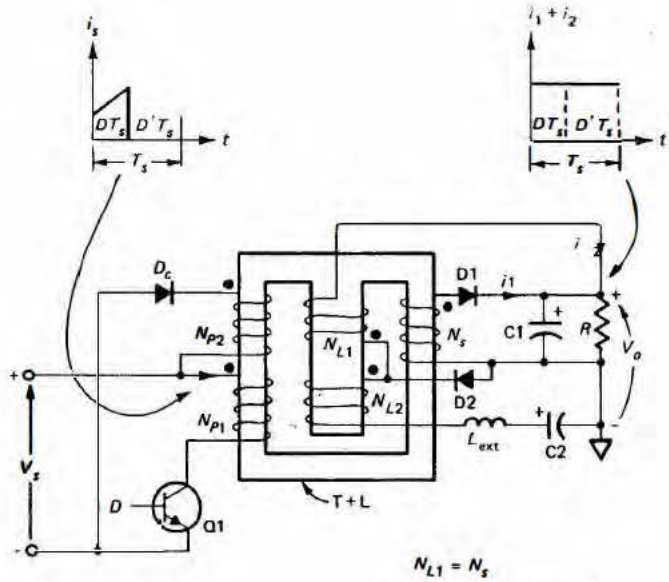


Fig. 12.48. Zero output ripple current version of an integrated magnetic forward converter.

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With it's position as shown in Fig. 12.48, this blocking capacitor will see an average DC voltage equal to that of the output potential, V_o.

The addition of this second winding does not compromise the buck input-to-output voltage gain of the forward converter, and it remains as defined earlier by Eq. (12.33). In practice, the ideal nature of the zero-slope output ripple current will not be achieved and will have some slight slope during intervals when the primary switch element (Q1 in Fig. 12.48) is ON. This slope will be proportional to the values of the inductances of the outer legs of the magnetic structure which are not controlled by the ripple-reduction center leg winding. If these induc-

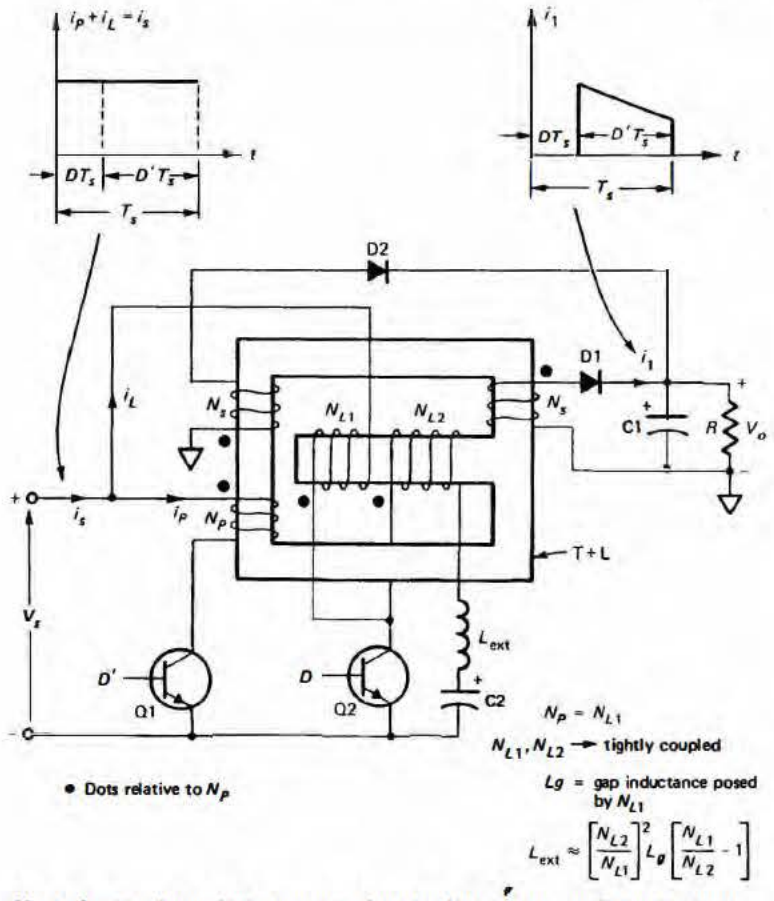


Fig. 12.49. Zero input ripple current version of an integrated magnetic boost converter.

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tances are much larger than that of the gapped center leg (say 10 times), then this current deviation due to magnetization energies will be very small and can be neglected for all intensive purposes.

Fig. 12.49 shows the integrated magnetic boost converter of Fig. 12.33 altered to include a control winding to adjust the input ripple current of this SPC to zero. Once again, we can use the transformer equations of Section 12.3 to select control winding turns and the value of the external trimming inductor, as evidenced by the equation accompanying this figure. The input-to-output boost voltage gain of this converter does not change from that defined by Eq. (12.34).

In a similar fashion, we can add ripple control windings to any of the more complex integrated magnetic converters of this chapter. This is to be expected, however, since they are descendants of families parented by either the basic buck or boost converter (see Chapter 11).

12.13. CAUTIONS IN DESIGNING INTEGRATED MAGNETIC CONVERTERS

Blending of inductors and transformers of SPCs into single magnetic systems can be very advantageous, often resulting in converter designs of lower cost, weight, and size than their discrete magnetic counterparts. Conversion performance can also be improved and component stresses reduced, provided the integration process is well thought out and executed properly.

For the most part, integrating magnetic elements of a converter will not add to the many other design aspects and difficulties that an engineer must contend with during development phases. It does place additional burden on the designer to properly specify the performance of the magnetic for production use, and on its manufacturer to insure a consistent magnetic product that may be much more complex than a simple transformer or inductor. Both of these burdens add up to additional recurring and nonrecurring costs associated with an SPC. Also, changing an integrated magnetic design once it is in production can be much more costly than a discrete version because of the intimate relationships that must exist between its various inductances and/or transformer elements.

It is obvious from our modeling work of this chapter that the integration process of SPC magnetics introduces additional inductive elements in their converter circuits. A good example is the magnetizing inductances of the outer legs of the magnetic assembly (e.g., L_c in Fig. 12.39). However, by making these inductances much larger than that of the gap, their contributions to overall SPC circuit performance will be small. Nevertheless, one should always remember that they are real and finite in value, and that the energies stored in them by SPC operations must be released and dissipated in a manner so as not to harm surrounding semiconductor switches and diodes.

There are some subtle electrical problems to watch out for when coupling

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inductors together on a common core. In the case of a multi-output buck-derived converter with coupled output inductors (Figs. 8.4, 12.15, 12.23), imbalances in the required turns ratio relationships between inductor and transformer windings can produce circulating currents in output filter networks, resulting in high output voltage ripple. Extreme imbalance can produce high power loss in output filter capacitors due to ESR voltage drops which, in turn, could result in possible damage and even destruction of the capacitors.

Always remember when designing a coupled-inductor magnetic for a converter that the DC mmf seen by its material will be the *sum* total of winding mmfs. Therefore, it is wise to always verify that the core material of the magnetic will not be operating near saturation under maximum DC bias conditions. As we mentioned earlier in Section 12.1, operation in a nonlinear portion of the material's *B-H* loop will also result in an inaccurate electrical model that might be derived for the magnetic circuit. Also, nonlinear operation does not necessarily imply that the user circuit of the magnetic will automatically malfunction. Frequently, however, higher-than-normal inductor currents produced by core operation near saturation can cause stress or permanent damage to other converter circuit components.

When coupling the input and output inductors of a Ćuk converter to reduce current ripple (Fig. 12.7), a highly undesirable output voltage *polarity reversal* can occur when input power is first applied (Ref. 13). This transient phenomenon is illustrated in Fig. 12.50A for a transformer-isolated version of this SPC. In converter applications where short term reversals of voltage polarity could produce damage (e.g., polarized filter capacitors and monolithic integrated circuits), this phenomenon must be circumvented or reduced to acceptable magnitudes.

As shown, inrush current through the primary winding of the inductor (L1) due to first turn-on of switch Q1 or by charging of the primary energy capacitance, C_P, when V_s is first applied, will produce a secondary transient current. The direction of this current is *opposite* to that of normal current flow when the converter is operating in a steady-state fashion, and results in a *reversal* of output voltage during the period of the current transient.

This transient condition will persist until the potential voltage levels of C1 and C2 reach values to counteract that impressed across L2 by transformer action from L1. Thus, the reversal time period will be determined by the time constants and magnitudes of power stage impedances and output load values.

Figs. 12.50B and C show two viable ways of protecting loads against this transient output reversal. In part B, a blocking diode (D_B) is placed in line with L2 to insure a proper unidirectional current path for steady-state output current, but prevents reversal current flow at converter turn-on. However, its presence does lower conversion efficiency because full load current must pass through it during normal operation. In part C, a clamp diode (D_c) is added across the out-

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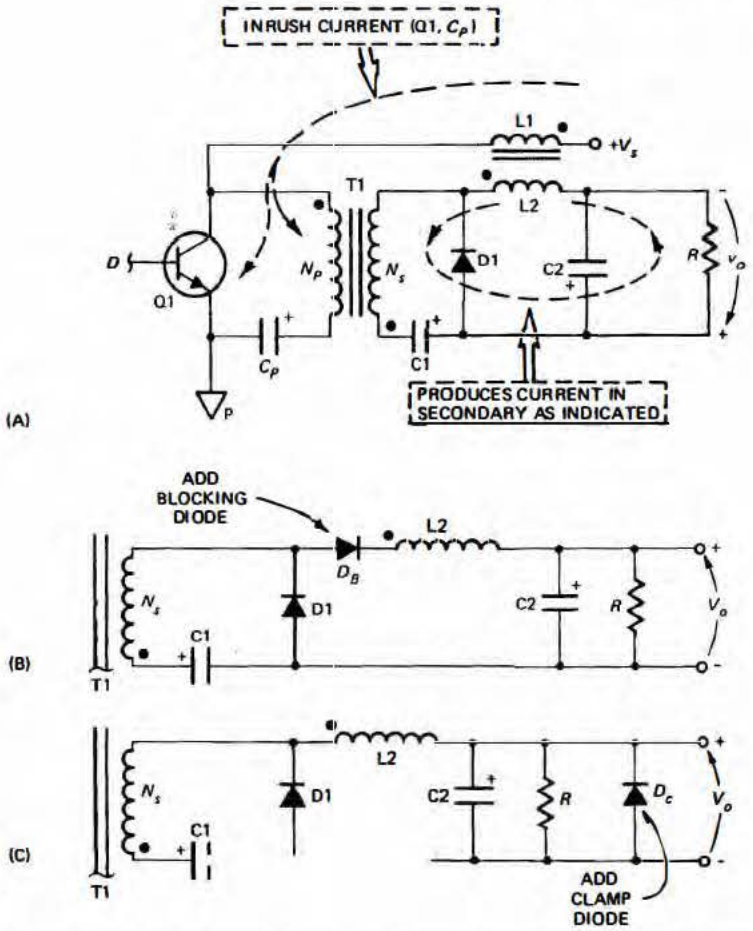


Fig. 12.50. Output voltage polarity reversal in a coupled-inductor Ćuk converter and possible methods for prevention and load protection.

put terminals of the SPC to limit the transient reversal voltage to less than a volt. During normal operation, this diode will be reverse-biased and therefore will dissipate no power. Use of a Schottky part is recommended for this diode to keep the reversal clamp voltage to an absolute minimum.

Coupling of inductors in various parts of a converter can complicate its small-signal model, often introducing additional poles or zeros in transfer functions that can produce reduced gain or even instability in a closed-loop SPC unless

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accounted for. However, as we saw in Chapter 10, the canonical model can be easily modified to include unregulated portions of a multi-output converter. The designer is therefore cautioned to always reflect any parts of a converter that is tied by magnetic means to a controlled loop when constructing a small-signal model for stability studies.

Finally, a few words about the design of the integrated magnetic buck and boost converters is in order before completing our exploration of integrated magnetics for SPCs. The amount of energy to be stored in the center legs of the designs that we have shown in this chapter will, of course, be dependent on the total output power needs of their converters. This center leg also will have significant DC bias because the unidirectional nature of its flux. Since the dimensions of a ferromagnetic material can be directly related to energy storage capability, one should attempt to estimate the size of the center leg of the magnetic from a knowledge of the energy needed and the rate at which it must be supplied. This estimate can then be used to select a magnetic material, core size/shape, turns and air gap lengths that will produce a design that meets or exceeds the energy storage requirement. For those interested in the details of magnetic field energy and its relation to core volume and material characteristics, Ref. 9 listed in the bibliography section of this book is again highly recommended for supplementary reading.

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Suggested Reading and Other Information Sources

Unfortunately, for the reader interested in the pursuit of previous work done in the field of switched-mode DC-to-DC power converter design, there is no single information source available today that can be considered comprehensive in its coverage of this subject. As witness the variety of publications given in the reference section of this text, most of the useful design information is scattered in books, magazines and in the proceedings of a host of conferences and other technical symposia, many of which are not directly related to the aspects of power converter design.

However, there are information sources available that are considered essential references for anyone beginning a career in the field of power electronics, as well as for those individuals engaged in serious research on related subjects. The purpose of this section is to provide a listing of these information sources, along with other data important for location and procurement.

1. CONFERENCE RECORDS

Perhaps the best-known technical meeting concerned with the subjects of power electronics is the annual Power Electronics Specialists Conference (PESC). Currently sponsored by the Aerospace and Electronic Systems Society of the Institute of Electrical and Electronic Engineers (IEEE), this conference brings together specialists in circuits, systems, electron devices, magnetics, control theory, instrumentation and power engineering for interspeciality discussions of new ideas, research and development, applications, and the latest advances in the field of power electronics. The conference was first held in 1970, and its technical programs consist of papers which describe original and unpublished work, both experimental and analytical. Records of all conferences may be obtained at a nominal cost from the IEEE Services Center, 445 Hoes Lane, Piscataway, New Jersey, USA, 08854. IEEE catalog numbers are given below for records from 1970 to 1984:

Year	IEEE Catalog Number
1970	70C31-AES
1971	71C15-AES
1972	72CHO-652-8 AES
1973	73CHO-787-2 AES

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Year	IEEE Catalog Number
1974	74CHO-863-1 AES
1975	75CHO-965-4 AES
1976	76CH-1084-3 AES
1977	77CH-1213-8 AES
1978	78CH-1337-5 AES
1979	79CH-1461-3 AES
1980	80CH-1529-7 AES
1981	81CH-1652-7 AES
1982	82CH-1762-4 AES
1983	83CH-1877-0 AES
1984	84CH-2000-8 AES

Another IEEE meeting of particular interest to individuals concerned with power semiconductor devices and their application is the International Semiconductor Power Converter Conference (ISPCC). This conference was first held in 1952 and has been repeated every five years since then. The ISPCC is sponsored by the Industry Applications Society (IAS) of the IEEE. As with the PESC records, the service office of the IEEE should be contacted on availability of past conference proceedings. At the time of publication of this text, the last ISPCC meeting was held in 1982 and its IEEE catalog record number is 82CH-1682-4 IAS.

Aside from the IEEE-sponsored PESC and ISPCC meetings, there are two other conferences related to power conversion that are frequented by power electronics engineers. Both are held annually and both are sponsored by United States-based corporations. The oldest of these two conferences is POWERCON, with its first forum held in 1974. While all POWERCON conferences have been held to date in various parts of the United States, the other corporation-sponsored conference is often conducted in cities of European countries as well as in the United States. This latter conference is called the Power Conversion International Conference (PCI). The first PCI conference was held in Munich, West Germany, in 1979.

POWERCON is sponsored by Power Concepts, Incorporated, and is a registered service mark of that corporation. Persons interested in purchasing copies of conference records should contact the POWERCON business office at Post Office Box 5226, Ventura, California USA, 93003 for information on cost and availability.

The PCI conference is sponsored by Interlec Communications, Incorporated. Questions on purchase and availability of conference records should be directed to their business office at 2909 Ocean Drive, Oxnard, California USA, 93030.

There are many other worldwide society-sponsored conferences that include power electronic subjects as a part of their forum. Examples are the International Telecommunications Energy Conference and the annual IEEE-sponsored Industry Applications Society (IAS) meeting. Most of these conferences are coordinated through the IEEE in the United States; therefore, it is recommended that the service office of IEEE be contacted to learn about such conferences and on how to obtain proceeding records. The address of the IEEE service office is given above in the discussion about the PESC proceedings.

2. TECHNICAL BOOKS

For most persons (authors of this text included) now actively engaged in the development of power converters, proper methods of design practice were learned by on-the-job industrial rather than engineering college experiences. It is widely recognized within the community of

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power electronics engineers today that the lack of formal college educational opportunities in power electronics has hampered progress and technical advancements in these fields. This educational dilemma is also reflected by the lack of fundamental textbooks containing subject matter related to power electronics circuit design, analysis, and synthesis.

However, over the past ten years, a limited number of technical books devoted to power electronics components, circuits and systems have appeared on the scene. The following is a list of those texts which the authors feel are useful reading materials for both the novice and the professional power electronics engineer. In addition to this list, the reader is also encouraged to obtain copies of the texts listed in the Bibliography.

1. Roddam, T., *Transistor Inverters and Converters*, D. Van Nostrand Company, Inc., Princeton, NJ, 1963.
2. Pressman, A. I., *Switching And Linear Power Supply, Power Converter Design*, Hayden Book Company, Inc., Rochelle Park, New Jersey, 1977.
3. Devan, S. B. and Straughen, A., *Power Electronics Circuits*, John Wiley & Sons, New York, 1975.
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5. Wood, P., *Switching Power Converters*, Van Nostrand Reinhold Company, New York, 1981.
6. Middlebrook, R. D. and Ćuk, S., *Advances in Switched-Mode Power Conversion*, TESLAco, Inc., Pasadena, California, 1981 (multi-volume series).
7. McLyman, Colonel Wm. T., *Transformer and Inductor Design Handbook*, Marcel Dekker, Inc., New York, 1978.
8. McLyman, Colonel Wm. T., *Magnetic Core Selection for Transformers and Inductors*. Marcel Dekker, Inc., New York, 1982.
9. Bedford, B. D. and Hoft, R. G., *Principles of Inverter Circuits*, John Wiley & Sons, New York, 1964.

The multi-volume series published by TESLAco (No. 6 above) is particularly useful, as it contains the majority of the papers published by the Power Electronics Group at the California Institute of Technology (CALTECH) since 1970. Included in these volumes are many of the CALTECH papers listed earlier as text references for this book. Information on price and availability of the volumes can be obtained by contacting the TESLAco business office at 490 South Rosemead Blvd., Suite #6, Pasadena, California 91107 USA.

3. MAGAZINES, JOURNALS, AND PERIODICALS

The current plight of the power electronics engineer in his search for regular and periodic information on subjects important to his field is perhaps exemplified by the lack of periodicals, journals or magazines devoted to such subject matter. At the time of the publication of this book, only one of the magazines listed below is considered by many subscribers to be one that is directed to power electronics designers. With respect to the others, they have, at irregular intervals, published technical articles of interest to power conversion design engineers. The authors of this text suggest that readers interested in obtaining copies of such articles contact the editors of each publication and request available index listings.

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Publication	Publisher/Editor Contact
1. *Powerconversion International Magazine*	Intertec Communications, Inc. 2909 Ocean Drive Oxnard, CA 93030 USA
2. *IEEE Transactions on Aerospace and Electronic Systems*	IEEE Service Office 445 Hoes Lane Piscataway, NJ 08854 USA
3. *IEEE Transactions on Magnetics*	Same contact as above.
4. *IEEE Transactions on Industry Applications*	Same contact as above.
5. *EDN Magazine*	Cahners Publishing Co. 221 Columbus Avenue Boston, MA 02116 USA
6. *Electronic Design Magazine*	Hayden Publishing Co. 50 Essex Street Rochelle Park, NJ 07662 USA
7. *Electronic Products Magazine*	Hearst Business Communications, Inc. UTP Division 645 Stewart Avenue Garden City, NY 11530 USA
8. *Wireless World*	IPC Electrical-Electronic Press Ltd., Quadrant House, The Quadrant, Sutton Surrey ENGLAND SM2 5AS
9. *Electronics Magazine*	McGraw-Hill Publishers 305 Madison Avenue New York, NY 10017 USA

4. PATENT FILES

Perhaps the most thought-provoking sources of information on power converter design are foreign and domestic patent records. At the time of the publication of this book, there were well over 4,300,000 patents on file in the United States Patent Office alone, with an average patent application submittal rate on the order of 100,000 per year.

Because of the enormous number of patents (on everything from the safety pin to Nikola Tesla's electromagnetic motor concept), patent records have special formats and codings to distinguish various invention categories. Many of these categories deal with power conversion circuit concepts and, therefore, it is not difficult (although somewhat time-consuming) for an interested researcher to locate them during a patent file search.

A complete file of all United States patents (including the first one issued in 1790 to Samuel Hopkins for an improvement in "The making of Pot ash and Pearl ash by a new Apparatus and Process") is maintained by the United States Patent and Trademark Office in Arlington, Virginia. The office is located at Crystal Plaza, 2021 Jefferson Davis Highway, in Arlington. Copies of patents can also be obtained from this office at a nominal cost. For those persons wishing to obtain a detailed guide to the standards for patent drawings, etc., the Patent and Trademark Office in Washington, D.C. 20231 can provide a copy, again at a small cost.

In addition to the central patent record office in Virginia, many major United States cities have public libraries that maintain copies and records of patents. Therefore, it is recom-

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mended that your local public library be contacted to see if they have patent files available for viewing and copying, before going directly to the U.S. Patent Office. Also, there are many patent information data banks that are accessible by computer telecommunication methods today. Many companies subscribe to such information services and your employer might be one of them.

Finally, for those readers who might enjoy a light-hearted look at the history of patents plus a guide to the preparation of a patent, *The Patent Book*, by James Gregory and Kevin Mulligan, is highly recommended. This book was first published in 1979 by A & W Publishers, Inc., 95 Madison Avenue, New York, New York 10016 USA, and its Library of Congress Catalog Card Number is 78-68388.

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