

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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DELTA ELECTRONICS, INC.

Petitioner

v.

VICOR CORPORATION

Patent Owner

IPR2024-00227  
Patent No. 9,516,761

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DECLARATION OF PROF. JUAN RIVAS-DAVILA

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1. I, Dr. Juan Rivas-Davila, hereby declare as follows:

**I. ENGAGEMENT AND COMPENSATION**

2. I have been retained by Vicor Corporation (“Patent Owner”) as an expert in the *inter partes* review proceeding described above. I have been asked to provide my technical review, analysis, insights, and opinions regarding the references that form the basis for the alleged grounds of unpatentability set forth in the Petition for *inter partes* review of US 9,516,761 (the ’761 Patent). For this service, my billing rate is an hourly consulting fee of \$525 / hour, and I am reimbursed for actual expenses. My compensation in no way depends on the outcome of this matter.

3. This declaration sets forth my analyses and opinions based on the materials I have considered thus far and the bases for my opinions. I understand that this declaration will be used in the above mentioned *inter partes* review. In forming my opinions, I have considered the following documents:

| <b>Exhibit No.</b> | <b>Description</b>                                 |
|--------------------|----------------------------------------------------|
| 1001               | United States Patent No. 9,516,761 (“’761 Patent”) |
| 1002               | Declaration of Dr. Steven B. Leeb                  |
| 1003               | <i>Curriculum Vitae</i> of Dr. Steven B. Leeb      |
| 1004               | File History of U.S. Patent No. 9,516,761          |
| 1005               | U.S. No. 8,966,747                                 |

|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1007 | Ericsson BMR 453 series DC/DC converters Technical Specification (July 2010), <i>available at</i> <a href="https://web.archive.org/web/20101108165728/http://archive.ericsson.net/service/internet/picov/get?DocNo=28701-EN/LZT146395&amp;Lang=EN&amp;HighestFree=Y">https://web.archive.org/web/20101108165728/http://archive.ericsson.net/service/internet/picov/get?DocNo=28701-EN/LZT146395&amp;Lang=EN&amp;HighestFree=Y</a> . (“Ericsson-BMR”) |
| 1008 | Robert W. Erickson and Dragan Maksimovic, <i>Fundamentals of Power Electronics</i> (2d ed. 2001). (“ <i>Fundamentals</i> ”)                                                                                                                                                                                                                                                                                                                          |
| 1009 | U.S. Patent 6,965,517 (“Wanes”)                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 1010 | U.S. Patent 6,970,367 (“Takeshima”)                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 1011 | G. Spiazzi, L. Rossetto, P. Mattavelli, P. Cova, and N. Delmonte, <i>Layout Considerations and Thermal Analysis of a 1.8 MHz Resonant VRM</i> , 2007 IEEE Industry Applications Annual Meeting, 1993 (2007). (“Spiazzi”)                                                                                                                                                                                                                             |
| 1012 | Laszlo Huber, Kevin Hsu, Milan M. Jovanovi, Dennis Solley, Gennady Gurov and Robert J. Porter, <i>1.8-MHz, 48-V Resonant VRM: Analysis, Design, and Performance Evaluation</i> , 21 IEEE Transactions on Power Electronics 79 (2006)                                                                                                                                                                                                                 |
| 1014 | Picture of Ericsson BMR 453 series DC/DC converter,<br><a href="https://web.archive.org/web/20120131104718/http://www.ericsson.com/solutions/news/powermodules/2009/hires_BMR453_jan09.jpg">https://web.archive.org/web/20120131104718/http://www.ericsson.com/solutions/news/powermodules/2009/hires_BMR453_jan09.jpg</a> .                                                                                                                         |
| 1018 | <u>Power Modules: Digital DC/DC converter family integrates PMBus connectivity</u> (2009), <i>available at</i> <a href="https://web.archive.org/web/20090902060840/http://www.ericsson.com:80/technology/docs/article_PowerModules_digital_dc-dc.pdf">https://web.archive.org/web/20090902060840/http://www.ericsson.com:80/technology/docs/article_PowerModules_digital_dc-dc.pdf</a>                                                               |
| 1019 | U.S. Patent 6,466,454                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 1020 | U.S. Patent 8,749,990                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 1023 | U.S. Patent Application No. 2011/0057713                                                                                                                                                                                                                                                                                                                                                                                                             |

|      |                                                                                                                                                                                                                                                                                                                                    |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1024 | U.S. Patent 6,724,631                                                                                                                                                                                                                                                                                                              |
| 1025 | Claim Chart for the Infringement of Independent Claim 1 and Dependent Claims 2, 3, 4, 5, 6, 7 of Complainant Vicor Corporation's United States Patent 9,516,761 by Delta U50SU4P162 High Power Density 48V / 12V Bi-Directional DC-DC Converter Power Module and Computing Systems Containing the Same ( <i>filed under seal</i> ) |
| 1026 | Ericsson BMR 453 series DC/DC converters Technical Specification (September 2008) ("BMR-2008")                                                                                                                                                                                                                                     |
| 2002 | Nadjahi, <i>et al.</i> , "A review of thermal management and innovative cooling strategies for data center", Sustainable Computing: Informatics and Systems 19 14–28 (2018).                                                                                                                                                       |
| 2003 | Kheirabadi, <i>et al.</i> , "Cooling of server electronics: A design review of existing technology", Applied Thermal Engineering 105, 622–638 (2016).                                                                                                                                                                              |
| 2004 | Almoli, "Air Flow Management Inside Data Centers", Doctoral Thesis, University of Leeds, (Feb. 2013), available at <a href="https://core.ac.uk/download/pdf/17187065.pdf">https://core.ac.uk/download/pdf/17187065.pdf</a>                                                                                                         |
| 2005 | Xu, <i>et al.</i> , "Extension of Air Cooling for High Power Processors", 2004 Inter Society Conference on Thermal Phenomena, pp. 183-192 (2004).                                                                                                                                                                                  |
| 2006 | U.S. Pat. No. 7,361,844.                                                                                                                                                                                                                                                                                                           |
| 2008 | Severns and Bloom, <i>Modern DC-To-DC Switch-Mode Power Converter Circuits</i> , Van Nostrand Reinhold Co., New York, 1985.                                                                                                                                                                                                        |
| 2009 | Declaration of Steven B. Leeb, Ph.D. in Support of SynQor's Motion for a Preliminary Injunction, from SynQor v. Ericsson, Inc., et al., Civil Action No. 2:11-cv-54-TJW-CE (E.D. Tex. Feb. 8, 2011).                                                                                                                               |
| 2010 | Intel, Power Supply Design Guide for Desktop Platform Form Vectors, Revision 1.31, April 2013, available at                                                                                                                                                                                                                        |

|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | <a href="https://www.smeps.us/Power_Supply_Design_Guide_Desktop_Platform_Rev_1_31.pdf">https://www.smeps.us/Power_Supply_Design_Guide_Desktop_Platform_Rev_1_31.pdf</a>                                                                                                                                                                                                                                                                                              |
| 2011 | Intel, Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.0 Design Guidelines, July 2005, available at <a href="https://www.intel.com/content/dam/www/public/us/en/documents/design-guides/voltage-regulator-module-enterprise-voltage-regulator-down-10-0-guidelines.pdf">https://www.intel.com/content/dam/www/public/us/en/documents/design-guides/voltage-regulator-module-enterprise-voltage-regulator-down-10-0-guidelines.pdf</a> |
| 2012 | U.S. Pat. No. 10,199,950.                                                                                                                                                                                                                                                                                                                                                                                                                                            |

## II. QUALIFICATIONS

4. I am currently an Associate Professor in the Department of Electrical Engineering at Stanford University and Fellow at the Precourt Institute For Energy. At Stanford, my research focuses on high-frequency power converters, such as the ones at issue in this matter. I was also responsible in 2023-2024 for teaching courses in the Electrical Engineering Department entitled “Power Electronics” and “Resonant Converters”. My laboratory at Stanford is the Stanford University Power Electronics Research Laboratory. I joined Stanford in 2014 as an Assistant Professor.

5. I hold a Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology (MIT), awarded in 2006. My Ph.D. thesis was entitled “Radio Frequency dc-dc Power Conversion”. I also hold a Master’s Degree in Electrical Engineering from MIT (2003), and a Bachelor of Arts degree from the Monterrey Institute of Technology (1998).

6. Prior to joining Stanford, I was an Assistant Professor in the Electrical Engineering Department at the University of Michigan (2011-2013).

7. During the timeframe 2007-2011, I worked as the Lead Power Electronics Engineer for General Electric's Global Research Center. My work there focused on the development of high-frequency power converters.

8. From 2018 to June 2021, I served as an Associate Editor for the IEEE Power Electronics Society Journal of Emerging and Selected Topics in Power Electronics. I am also a reviewer for the IEEE Power Electronics Society. From 2019 to 2021, I served as Vice Chair of the Technical Committee for Power & Control Core Technologies for the IEEE Power Electronics Society.

9. I am attaching a copy of my C.V. to this declaration. As shown in my C.V., I have authored dozens of papers in the field of Power Electronics and the design of power converters. I am a named inventor on nineteen issued patents relating to power electronics.

### **III. MY UNDERSTANDING OF THE RELEVANT LAW**

#### **A. Claim Construction**

10. I understand that a claim term in an *inter partes* review is to be interpreted according to standards applied by district courts. First, the language of the claims themselves is of primary importance in the effort to determine precisely what it is that is patented. The terms used in a claim are generally given the

ordinary and customary meaning that the terms would have to a person of ordinary skill in the art in question at the time of the alleged invention, unless the term is expressly defined in the patent. The person of ordinary skill in the art reads the claim in the context of the entire patent, including the specification. Next to the language of the claims, the specification of the patent is the single best source for interpreting the claim terms. The claims may also be interpreted using the record of correspondence between the patent applicant and the Patent Office, and also with reference to other sources of evidence that can help to define the meaning of terms to a person of ordinary skill in the relevant time frame. I define the relevant time frame in ¶76, below.

## **B. Anticipation**

11. I understand that a claim in an issued patent can be invalid if it is anticipated. In this case, “anticipation” means that there is a single prior art reference that discloses every element of the claim, arranged in the way required by the claim.

12. I understand that an anticipating prior art reference must disclose each of the claim elements expressly or inherently. I understand that “inherent” disclosure means that the claim element, although not expressly described by the prior art reference, must necessarily be present based on the disclosure. I

understand that a mere probability that the element is present is not sufficient to qualify as “inherent disclosure”.

### **C. Obviousness**

13. I understand that a claim in an issued patent can be invalid if it is obvious. Unlike anticipation, obviousness does not require that every element of the claim be in a single prior art reference. Instead, it is possible for claim elements to be described in different prior art references, so long as there is motivation or sufficient reasoning to combine the references, and a reasonable expectation of success.

14. I understand that a claim is invalid for obviousness if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the alleged invention was made to a person having ordinary skill in the art to which said subject matter pertains.

15. I understand, therefore, that when evaluating obviousness, one must consider obviousness of the claim “as a whole”. This consideration must be from the perspective of the person of ordinary skill in the relevant art, and that such perspective must be considered as of the “time the invention was made”.

16. The level of ordinary skill in the art is discussed in ¶77 below.

17. The relevant time frame for obviousness, the “time the invention was made”, is discussed in ¶76, below.

18. I understand that in considering the obviousness of a claim, one must consider four things. These include the scope and content of the prior art, the level of ordinary skill in the art at the relevant time, the differences between the prior art and the claim, and any “secondary considerations”. I understand that these four things were specified by the U.S. Supreme Court in a case called *Graham v. John Deere*, and are therefore called the “*Graham* factors”.

19. I understand that “secondary considerations” include real-world evidence that can tend to make a conclusion of obviousness either more probable or less probable. For example, the commercial success of a product embodying a claim of the patent could provide evidence tending to show that the claimed invention is not obvious. In order to understand the strength of the evidence, one would want to know whether the commercial success is traceable to a certain aspect of the claim not disclosed in a single prior art reference (i.e., whether there is a causal “nexus” to the claim language). One would also want to know how the market reacted to disclosure of the invention, and whether commercial success might be traceable to things other than innovation, for example the market power of the seller, an advertising campaign, or the existence of a complex system having many features beyond the claims that might be desirable to a consumer. One

would also want to know how the product compared to similar products not embodying the claim. I understand that commercial success evidence should be reasonably commensurate with the scope of the claim, but that it is not necessary for a commercial product to embody the full scope of the claim.

20. Other kinds of secondary considerations are possible. For example, evidence that the relevant field had a long-established, unsolved problem or need that was later provided by the claimed invention could be indicative of non-obviousness. Evidence that others had tried, but failed to make an aspect of the claim might indicate that the art lacked the requisite skill to do so. Evidence of copying of the patent owner's products before the patent was published might also indicate that its approach to solving a particular problem was not obvious. Evidence that the art recognized the value of products embodying a claim, for example, by praising the named inventors' work, might tend to show that the claim was non-obvious.

21. I further understand that prior art references can be combined where there is an express or implied rationale to do so. Such a rationale might include an expected advantage to be obtained, or might be implied under the circumstances. For example, a claim is likely obvious if design needs or market pressures existing in the prior art make it natural for one or more known components to be combined, where each component continues to function in the expected manner when

combined (i.e., when there are no unpredictable results). In these cases, the combination must be within the capabilities of a person of ordinary skill in the art.

22. I understand that when considering obviousness, one must not refer to teachings in the specification of the patent itself. One can, however, refer to portions of the specification admitted to be prior art.

#### **IV. TECHNICAL INTRODUCTION**

23. The following Technical Introduction is intended to describe concepts necessary to understand the '761 patent, and is not necessarily directed to any particular timeframe.

##### **A. Voltage, Current, and Resistance**

24. The '761 patent relates to power converters. Because the subject matter is complex, a brief introduction of the technology involved is appropriate.

25. Electricity concerns the flow of charged particles through a material. Materials that allow easy flow of electrons are called “conductors”, while materials that impede the flow of electrons are called “insulators”. The extent to which a material impedes the flow of electrons through it is called its “resistivity”. Some materials, like “semiconductors” can change their resistivities. An electrical component made from a material with resistivity, with a particular geometry, is said to have a “resistance”, which reflects its ability to impede the flow of electrons.

26. The flow of electrons (charged particles) per unit time is called “current”. Current is measured in Amperes and often represented by the letter “i” or “I”. The energy of electrons is called their “potential”, and is measured in Volts. A “voltage” is a difference between potential between locations, and often represented by the letter “v” or “V”. Current will tend to flow from higher to lower potential. When electrical current flows through a material that has a resistance (often represented by the letter “R”), it will lose some of its energy, creating a potential difference, or voltage, across the resistance. This is expressed as Ohm’s law:  $V=IR$ , or the voltage difference across the resistance (V) is equal to the current flowing through the resistance (I) times the resistance (R).

27. These basics of electricity can often be analogized to water in a pipe, where the electrical current is like the flow of water, the potential is like water pressure, and the resistance is the amount of resistance to flow (e.g. like sand packed in a pipe). Just as high water pressure can force a flow of water through a pipe clogged with sand, a high voltage can force current to flow through a material that has resistance.

### **B. Alternating Current (AC) and Direct Current (DC).**

28. Electrical current can be thought of as having two forms: Alternating Current (AC) and Direct Current (DC). Direct Current essentially means that the current flows in only one direction (imagine a steady stream of water leaving a

pipe). Alternating current means the current flows back and forth, alternating directions (imagine water first leaving a pipe, and then being drawn back in, in alternating cycles).

29. Voltage can also be described as AC or DC. A DC voltage is one that typically points in only one direction (meaning that voltage is pushing/pulling electrons in one direction), while an AC voltage is one points in alternating directions (the voltage is pushing/pulling electrons in alternating directions).

### **C. Power**

30. Electrical power is the amount of electrical energy that can be delivered in a unit time. Power is typically measured in Watts. When power is delivered to a device, the power can be expressed as the voltage across the device times the overall current through the device, or as  $V$  times  $I$ . Because power is equal to  $VI$ , the same power can be delivered by 1 Ampere of current at 10 Volts as 10 Amperes of current at 1 V.

31. Electrical power may often be used at different voltage levels. For example, a fan might be powered using DC at 12 V, whereas a modern microprocessor might require DC at less than 1 V. Furthermore, power can arise from sources at different voltage levels, and can be in AC or DC form.

#### **D. Power Converters**

32. The job of a power converter is to transform the characteristics of electrical power. This can mean changing voltage and current levels, changing between AC and DC, or both.

33. One simple power converting device that has been known for more than a century is called a “transformer”. A transformer has two separate wires that are usually electrically isolated from one another. Each wire is formed into a coil, having a series of loops (or “turns”). One coil of wire is called the “primary winding”, while another is called the “secondary winding”. The windings of each wire are placed in close proximity to one another, and are usually wound around the same “core” made of a magnetizable material. Then, when an alternating current passes through one of the windings (e.g. the primary winding), it will cause an alternating magnetic field that will induce an AC voltage in the respective other winding (e.g., the secondary winding). In an ideal transformer, the ratio of the voltage across the primary winding to the voltage induced in the secondary winding is equal to the ratio of the number of turns (loops) of wire in the primary winding to the number of turns in the secondary winding. I say “ideal transformer”, because when using a transformer, usually some loss of power occurs. However, in a well-designed transformer, most of the power will be preserved. Transformers thus provide a very easy way to transform power to

different voltage levels. However, transformers only work with AC power, not with DC power.

34. The utility power system in the United States works with AC power. This is to minimize the transmission losses in power lines. Transmission losses are approximately equal to the resistance of the power lines (which is low, but not zero) times the *square* of the current flowing through them ( $I^2R$ ). Because losses increase with the square of the current, it is desirable to keep current low in power lines. Current can be kept low, but still deliver the same amount of power, by increasing the voltage of the power ( $P=VI$ ). For this reason, utilities will use transformers to step up the voltage to a very high voltage for transmission along power lines, and then step the voltage back down, using another transformer near where the power is to be used. Because transformers only work with AC power, it is convenient to use AC power in utility power lines.

#### **E. DC to DC Power Converters**

35. Many power converters convert one DC voltage to another, for example, lowering or “downconverting” a high DC voltage to a low DC voltage.

36. Although transformers only work with AC power, transformers are often used when converting one DC voltage to another. To accomplish this, a DC voltage first needs to be changed to an AC voltage so that it will work with a transformer. Then, the transformer can be used to change the AC voltage level.

Then, the transformed AC voltage needs to be changed back to a DC voltage. The process flow is indicated conceptually here:

DC voltage → AC voltage → Transformer → Transformed AC voltage → DC Voltage

37. To transform a DC voltage to an AC voltage, a power converter may use switches, often implemented as power MOSFETs. A MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a transistor. A MOSFET has a channel with source and drain terminals (connections), and a separate gate terminal. By applying specific voltage levels to the gate terminal, the MOSFET will change the resistance of its channel, effectively turning the channel ON and OFF. A MOSFET that has its channel turned ON will have low channel resistance, and current will be able to easily flow through the channel. A MOSFET that has its channel turned OFF will have a high channel resistance, and current will not be able to flow through its channel.

38. A MOSFET is a “power” MOSFET when it is designed to handle higher amounts of power, in part by making the MOSFET large in order to lower the channel resistance (in the water analogy, by having a wider pipe for water to flow through).

39. MOSFETs usually have parallel body diodes. A diode is a semiconductor device that usually allows current flow in only one direction. A

diode will begin conducting current in that direction if the voltage across the diode exceeds a turn-on voltage, called the “forward voltage drop”.

40. MOSFET switches can be used to convert a DC voltage to an AC voltage using specific circuit topologies. By topology, I mean the way in which circuit elements are connected to one another. One example topology is called a “full bridge”, and is shown in a portion of Fig. 4 of Vicor’s U.S. Pat. No. 10,199,950 patent, which is reproduced here:

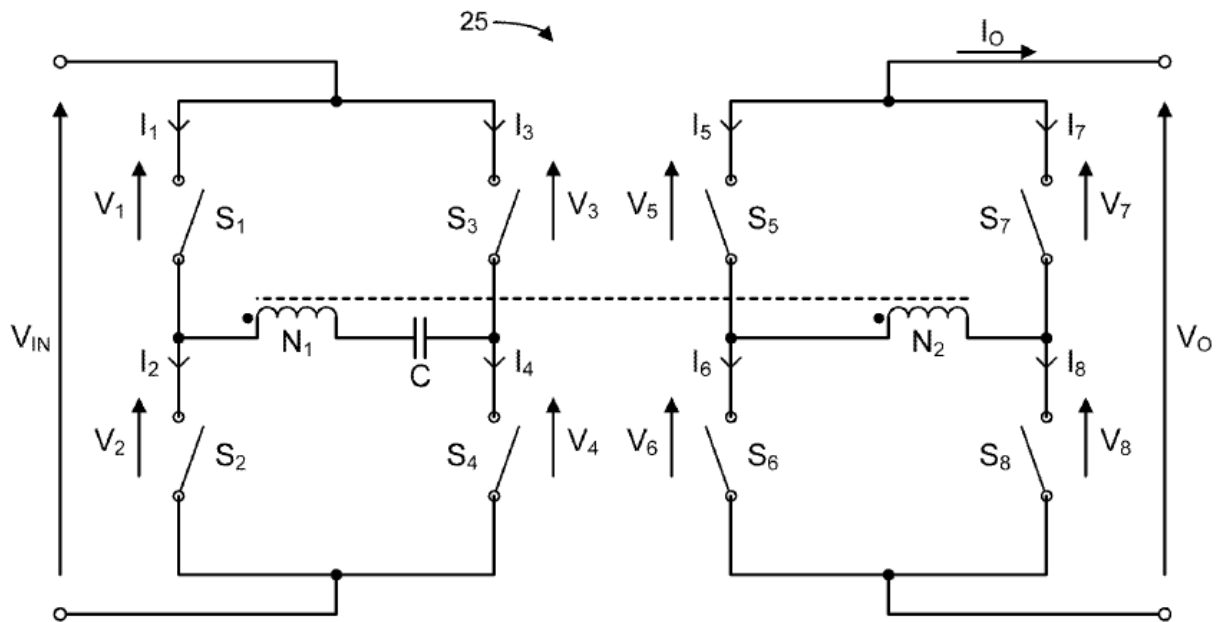


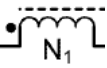
FIG. 4

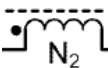
(Ex. 2012, Fig. 4, 5:25-36).

41. This circuit has an input DC voltage on the left side, called “ $V_{IN}$ ”, and an output DC voltage on the right side, called “ $V_O$ ”. The object of this circuit is to

transform the DC voltage  $V_{IN}$  to a different voltage level ( $V_O$ ) without significant loss of overall power.

42. The circuit of Fig. 4 operates with a transformer, which is shown by

the symbol  representing the primary winding near the left side, and the

symbol  representing the secondary winding near the right side. While

these two windings are separated by some distance in the circuit diagram of Fig. 4,

in practice they would both be wound around the same magnetizable core. In

general, the side of the transformer that includes the primary winding is called the

“primary side”, while the side of the transformer that includes the secondary

winding is called the “secondary side”. The symbol “ $N_1$ ” usually indicates that the

transformer has  $N_1$  turns in its primary winding, and “ $N_2$ ” indicates that the

transformer has  $N_2$  turns in its secondary winding, such that the ratio of voltage

across the primary winding to the voltage across the secondary winding should be

$N_1/N_2$ , not accounting for non-idealities and losses in the transformer.

43. The DC input voltage  $V_{IN}$  is converted to an AC voltage across the

transformer by the action of several switches, labeled  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$ . For

example, the converter might turn switches  $S_1$  and  $S_4$  ON at the same time,

allowing them to conduct, while  $S_2$  and  $S_3$  are OFF. This effectively allows current

to flow from left to right across the transformer winding  $N_1$  (neglecting, for the

moment, the action of the capacitor labeled “C”). A short time later, the converter may turn  $S_1$  and  $S_4$  OFF, while turning  $S_2$  and  $S_3$  ON. This reverses the flow of current across the transformer. By repeating this process at a frequency (called the “operating” or “switching” frequency), the DC input voltage can be changed to an AC voltage.

44. When an AC voltage is placed across the transformer primary winding, an AC voltage will appear across the transformer secondary winding ( $N_2$ ) as well. This AC voltage will have a different overall voltage level, depending on the ratio of the turns in each transformer winding, as explained above, and accounting for any non-idealities and losses in the transformer.

45. The AC voltage in the secondary winding then needs to be converted back to DC output voltage. To do this, another set of switches are used:  $S_5$ ,  $S_6$ ,  $S_7$  and  $S_8$ . These switches are turned ON and OFF in alternation ( $S_5$  and  $S_8$  will be ON while  $S_6$  and  $S_7$  are OFF, and *vice versa*), in order to force the alternating current in the secondary-side circuit to flow in one direction. Obviously, the switches need to be turned ON and OFF with precise timing, in order for this process to occur. The process of turning AC into DC is called “rectification”.

46. When switches that need to be turned ON and OFF with precise timing are used for rectification, the process is often called “synchronous rectification”, and each switch (usually a power MOSFET) can be called a

“synchronous rectifier”. There are other ways to perform rectification. For example, instead of switches, diodes can be used to perform rectification, because they only allow current to flow in one direction in most modes of operation. Diodes, however, experience a voltage drop when current flows through them, and so are less efficient than MOSFETs, which can be made to have very low channel resistance, and thus very low voltage drop, when they are ON.

47. The term “rectification” should not be confused with the similar-sounding term “regulation”, discussed below.

#### **F. Zero-Voltage and Zero-Current Switching**

48. The switches in a power converter (for example  $S_1$  through  $S_8$  discussed above) are usually implemented as power MOSFETs. As discussed above, power MOSFETs turn their channels ON and OFF depending on the voltage that is placed on their gate terminals. When the channel of a power MOSFET is ON, it has a very low channel resistance, and current can flow through it easily with very low resistive losses. When the channel of a power MOSFET is OFF, it has a very high channel resistance, and current essentially cannot flow through it. However, when undergoing the process of switching from ON to OFF or vice versa, power MOSFETs can have intermediate channel resistances. These intermediate channel resistances can allow significant current flow at relatively

high losses. Thus, power MOSFETs can cause relatively higher resistive losses during the act of switching than during normal operation in the ON and OFF states.

49. To avoid such losses, some devices attempt to cause switch transitions when there is zero voltage across the MOSFET channel, and/or zero current flowing through the MOSFET. With zero voltage across the switch and zero current flowing in the circuit branch containing the transistor channel, no current will flow through the MOSFET channel when it is in the act of switching.

### **G. Fixed-ratio converters and Regulating converters**

50. A converter like the one shown in Fig. 4 of the '950 patent above will provide an output voltage,  $V_o$ , that is a fixed ratio of the input voltage. Neglecting losses, this ratio ( $V_o/V_{in}$ ) is proportional to the ratio of transformer turns,  $N_2/N_1$ . When the input voltage  $V_{in}$  varies, the output voltage  $V_o$  will also vary, always maintaining the ratio  $V_o/V_{in}$  approximately equal to  $N_2/N_1$ .

51. These so-called “fixed ratio” converters have certain applications, but often the “load” (or the device attached to the output of the converter, which uses its output voltage) will require a precise voltage, like 1.00 V. This is especially true for microprocessors and other integrated circuits. In order to provide a precise and non-varying output voltage, many power converters will employ “regulation”. With regulation, the power converter in some way monitors the level of the output voltage. When the output voltage goes too high or too low, feedback into the

power converter circuitry will change some aspect of the converter's operation to counteract the deviation in output voltage. The change in operation can take a variety of forms, for example, the converter might change its operating frequency, in a technique called "frequency modulation". A converter could also change the amount of time in a switching cycle that the primary-side or secondary-side MOSFETs are ON and OFF within a switching cycle, a technique called "pulse-width modulation" or "PWM". There are several other ways to provide a regulated converter output.

52. Because regulating converters hold their output voltage constant while the input voltage varies, the voltage transformation ratio  $V_{\text{out}}/V_{\text{in}}$  is not fixed, but rather varies (because only  $V_{\text{out}}$  is fixed while  $V_{\text{in}}$  varies).

#### **H. Resonant circuits**

53. The discussion above related to Fig. 4 of the '950 patent did not take into account the action of the capacitor C. Fig. 4 is shown again here:

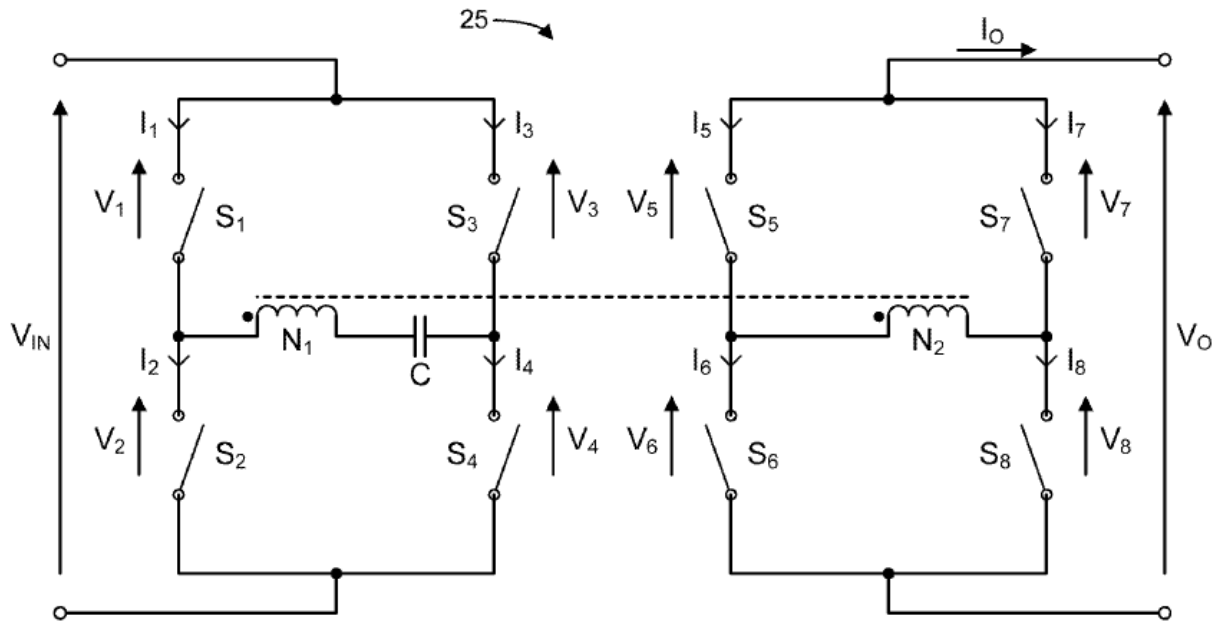


FIG. 4

(Ex. 2012, Fig. 4).

54. The capacitor  $C$  comprises two conducting surfaces that are separated by insulation. Because the two surfaces are isolated from one another, a capacitor will block continuous direct current. However, a capacitor has a special interaction with AC. With AC, current can initially flow into one side of the capacitor and deliver charge to one surface of the capacitor. That charge will attract opposite charges to the other surface of the capacitor, creating a voltage across the capacitor when charged. When the alternating current reverses direction, charge will begin to flow out of one side of the capacitor, allowing opposite charges to escape from the other side, lowering the voltage again. The net effect of this is that an AC current into and out of a capacitor will have a waveform that is proportional to the

time derivative of the voltage function across the capacitor. The proportionality constant relates to the ability of a capacitor to store charge, which is denoted as the capacitance (often called “C”). The capacitance is a fundamental characteristic of a capacitor.

55. A capacitor can be one part of a resonant circuit. A resonant circuit is created when a capacitor is placed in series or parallel with an inductor. An inductor is an element that is formed from a coil of wire. An inductor has no effect on direct current, which simply passes through the wire. However, with AC, the alternating current creates a changing magnetic field. The changing magnetic field, in turn, induces a voltage in the wire that forms the inductor. The induced voltage opposes changes in the alternating current. The net effect of this is that, with AC, the voltage across an inductor will have a waveform that is proportional to the time derivative of the current function in the inductor. The proportionality constant relates to the ability of an inductor to induce an opposing voltage, which is denoted as the inductance (often called “L”). The inductance is a fundamental characteristic of an inductor. Each winding of a transformer is an inductor.

56. To form a resonant circuit, an inductor and capacitor can be placed in series or in parallel. These elements will have a certain frequency, called the resonant frequency. The resonant frequency is defined by the equation

$$f = \frac{1}{(2\pi)\sqrt{LC}}$$

for both series and parallel resonant circuits, and is constant (subject

only to environmental changes in L and C). When there is an applied AC voltage at the resonant frequency in a series-resonant circuit, for example, the impedance in the circuit will be at a minimum. The applied AC voltage in a resonant circuit can have a frequency (called the “operating frequency” or “switching frequency” if switches are used) that is different from the resonant frequency.

## **I. Isolation**

57. Transformers in power converters can provide galvanic isolation. This is because a transformer does not have a galvanic (wired) connection between its primary and secondary windings. Instead, the two windings are only magnetically coupled. For that reason, if no other galvanic connection is provided between the primary and secondary winding circuits, a power converter using a transformer is said to be “isolated” or “isolating”. Isolation can provide safety and noise-suppression benefits, where noise means an irregular and unwanted variation in the voltage delivered.

## **V. TECHNOLOGY OF THE '761 PATENT**

### **1. The Petition’s argument**

58. I have reviewed the Petition for inter partes review. The Petition argues as follows:

“the purported innovation of the '761 Patent is the purely functional result that the power dissipated on the top and bottom sides of the power converter’s printed circuit board (PCB) are roughly the same

(specifically, within 150% of each other). This functional result was the natural outcome, however, of a conventional layout of power converter electrical components on a PCB, in particular a layout that was symmetrical on top and bottom.”

(Petition, p. 1). This argument seems to set the claims up as a simple, inherent result from a common package arrangement.

59. In my opinion, however, the Petition is incorrect, because the claims of the '761 patent are neither the natural result of a common structure, nor was the structure common. Rather, the approach of the '761 patent was counterintuitive and advantageous.

60. Claim 1 of the '761 patent requires a plurality of power semiconductor devices to be arranged into two sets, one on the top of a printed circuit board (“PCB”), and one set on the bottom. Here, “power semiconductor devices” are usually MOSFETs (Metal Oxide Semiconductor Field Effect Transistors). These MOSFETs act as switches in the power converter. They are “power” MOSFETs, as I discuss above in ¶38, because they are made much larger than logic-level transistors found in an integrated circuit, in order to increase their channel width and decrease their resistance. As current flows through a resistance the power dissipated is equal to the square of the current times the resistance ( $P = I^2 R$ ). Therefore, lower resistance translates into lower power dissipation in the

form of conduction losses. Power dissipation in a device is the measure of heat generated during its operation.

61. Having such power MOSFETs symmetrically arranged on the top and bottom of a circuit board is necessary, but not sufficient, to achieve balanced heat generation for MOSFETs on each side of the board, as required by claim limitation 1[e]. This is because heat generation depends on a number of variables, including the MOSFET's channel resistance and how the MOSFETs are used in the converter (how they are turned ON and OFF and how much current they carry).

62. To achieve balanced heat generation from MOSFETs on opposite sides of a converter's PCB, the *layout* and *operation* of the converter circuit need to be suitably engineered. At the outset, the converter's circuit has to be *designed* in a way that makes it *possible* to partition companion MOSFETs, carrying similar currents, between the top and bottom surfaces of a PCB. For example, using the principles of the '761 patent, one might choose to use pairs of MOSFETs configured topologically in parallel, with identical or complementary driving waveforms, in such a way that each member of the pair is guaranteed to experience the same voltage-current waveforms across its channel. This would allow each MOSFET in a given pair to be placed on the top and bottom surfaces, respectively, of a PCB, and approximately equalize power dissipation, i.e. heat generation, in operation.

## 2. Datacenter thermal management

63. Balanced heat generation at the top and bottom of a PCB was not considered a desirable thing in the relevant timeframe. Converters of the type described in the '761 patent are used as on-board power converters for servers. That is, the converters are mounted on the same board as a server CPU, and provide a portion of the power supply system to the CPU of the server. The servers are placed in racks in data centers, as shown in the following image:



Fig. 1. Data center in Nokia, Lannion.

(Ex. 2002, Fig. 1, p. 2). This image shows a series of vertically-shaped cabinets, each having a number of racks, like drawers.

64. In such data centers, thermal management is a significant issue. Data centers use approximately 2% of the U.S. electricity supply, and about 33% of that electricity is used by cooling systems external to the servers themselves. (Ex.

**Condenser** Heat expulsion to atmosphere

**CRAC or CRAH unit**

Cold air stream (blue arrow)  
Hot air stream (red arrow)

(Ex. 2003, Fig. 4, p. 5). As shown in the figure above, cold air enters the server rack

space in specific aisles, called “cold aisles”, enters the front of the servers, and passes through to other aisles, called “hot aisles”.

66. The typical flow of air through a server (from cold aisle to hot aisle) is shown here:

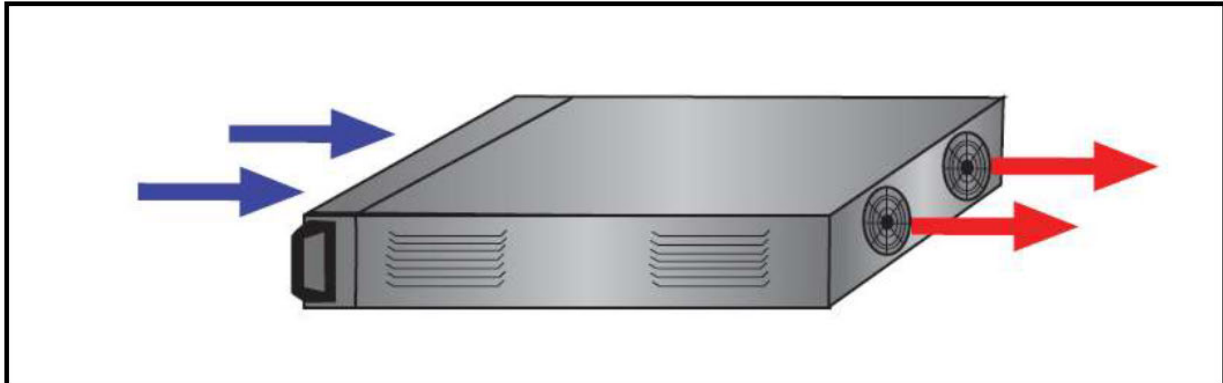


**Figure 4.5 Location of the fan on the traditional server [32].**

(Ex. 2004, Fig. 4.5, p. 98).

67. Air flowing through the server racks in this manner would flow over components on the main board, as illustrated here:

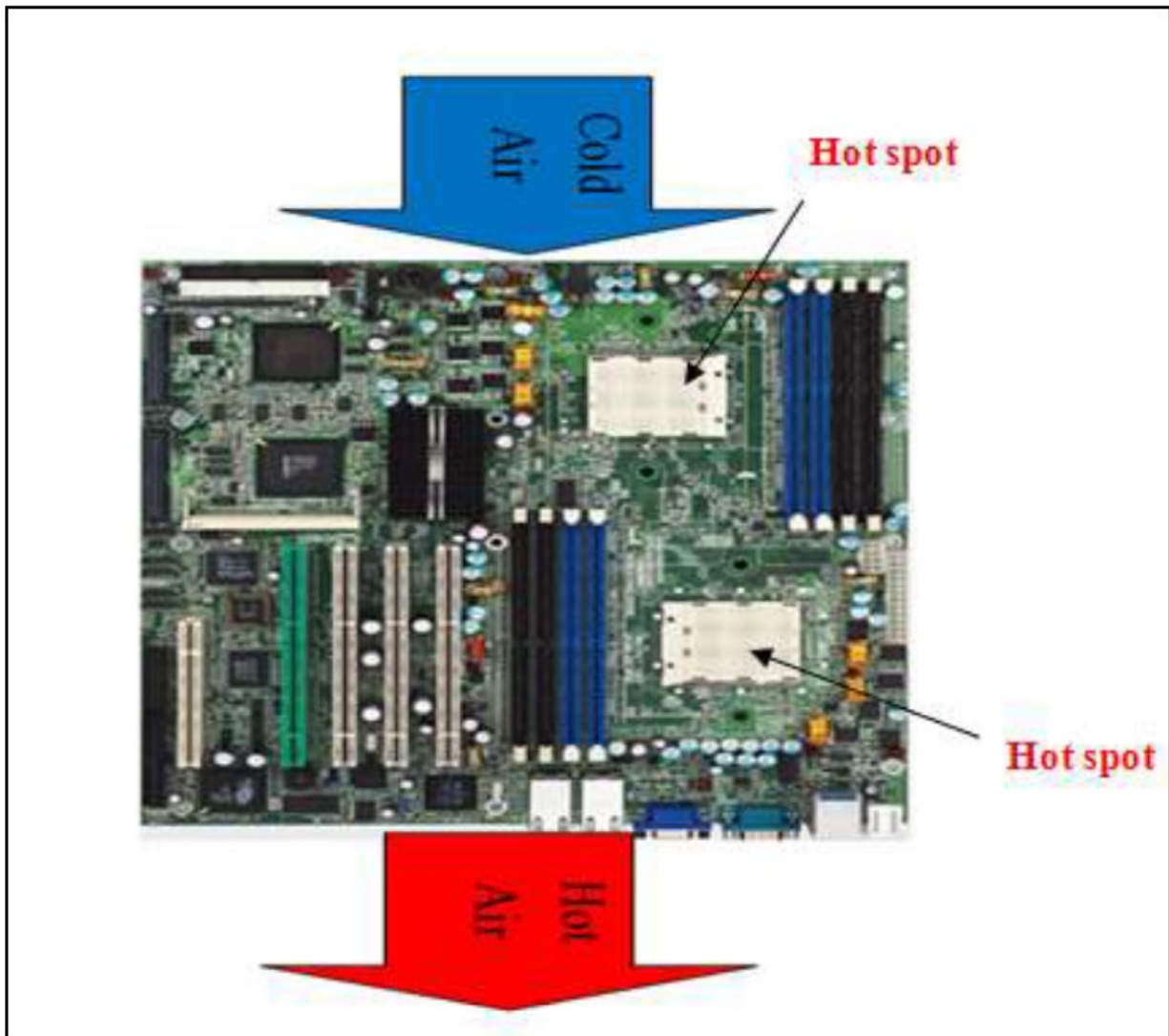


**Figure 4.9 Thunder K8S Pro S882 server mother board [78].**

(Ex. 2004, Fig. 4.9, p. 104). This internal arrangement of fan and airflow was typical for computer systems in the relevant timeframe.

68. Because of this arrangement, components on the server motherboard were typically outfitted with a heat sink exposed to the cool air flow. The heat sink

was intended to facilitate heat extraction from the components on the top surface of the PCB to the air flow:

“At the server level, all electronics are cooled through direct forced air convection with heat sink attachments required for high heat flux components [9]. Dedicated server fans drive cold aisle air through individual servers and release the heated exhaust air back into the facility through allocated hot aisles [11].”

(Ex. 2003, p. 4).

69. Heat sinks were typically attached to the top of power converters, because the converter’s bottom side was soldered to the server’s “motherboard”. This means that components on the bottom of the power converter’s PCB would have higher thermal resistance to the heat sink. (Ex. 2005, Fig. 2, Table I).

70. While limited heat extraction from components mounted to the bottom of the converter’s PCB is possible, thermal resistance between components mounted to the top side of the converter’s PCB and external cooling was typically far less than thermal resistance from components mounted on the bottom side of the converter’s PCB. Thus, it was considered advantageous to place components that generated considerable heat, such as MOSFETs, on the power converter’s top side closest to the heat sink. As Vicor’s prior power-converter U.S. patent 7,361,844 (incorporated by reference into the ’761 patent at 1:42-47), entitled, “Power Converter Package and Thermal Management” stated:

“In applications where heat is primarily removed by forced airflow or by an external heat sink coupled to the top surface 35, **cooling of power dissipating components, such as MOSFET power switches 448, is enhanced by placing the devices on the top surface of the circuit board 442**, in close proximity to the large top surface 35.”

(Ex. 2006, 11:17-23)(Emphasis added)(*see also* 5:4-11, 12:13-17). This was true even where measures were taken to increase thermal conductivity from the bottom side. (*e.g.* Ex. 2006, 11:44-48).

71. Thus, it was counterintuitive to place MOSFETs on the bottom surfaces of a power converter’s PCB, or to approximately balance the total heat generated by MOSFETs on opposite sides of the converter’s PCB. To the contrary, a PHOSITA would have sought to place MOSFETs on the top surface of the converter’s PCB.

### **3. The approach of the ’761 patent**

72. The ’761 patent seeks to distribute MOSFETS symmetrically, with approximately balanced heat generation, to improve efficiency and decrease waste heat. Unexpectedly, this compensated for the high thermal resistance in the heat path from the bottom of the package.

As the ’761 patent explains,

“One benefit of sharing footprints allows the pair of components to share a common set of conductive vias used to electrically connect the components on the PCB surfaces to internal conductive layers,

e.g. used to form the windings of the transformer. Because each via is used for both components in the pair, the total number of vias for making connections to the pair of components may be reduced (by as much as a factor of two) increasing the area of conductive layers useable for making connections and thus reducing resistance.”

(Ex. 1001, 24:25-34).

73. This benefit can be explained as follows: in power converters of the type used in the '761 patent, the top surface is packed with components. The inner layers of the power converters are primarily occupied by transformer windings, which need to be wide to handle high current levels. Switching MOSFETS need to be located near their respective winding terminals, and connected to those terminals by vias (electrical connections extending vertically through the PCB), in order to minimize the path through which current flows. By having MOSFETs placed in symmetrical positions on the top and bottom surfaces of the PCB, and having those MOSFETs share connections to transformer windings, companion MOSFET terminals can share vias, thus reducing the overall number of vias. The area otherwise taken up by vias can thus be devoted to conductive pathways, reducing overall resistance.

#### **4. The prior art**

74. In my view, the prior art cited in the Petition does not show the key elements of the '761 patent. There is no prior art that discloses the advantages of

the invention of the '761 patent or addresses the power dissipation/heat generation balance. References that place MOSFETs on a top and bottom surface do so in unusual contexts (*e.g.* Wanes, on the top and bottom of a lead frame over a board and Spiazzi, on the top and bottom of a copper base plate) or place a only a small subset of MOSFETs on the bottom side of a converter's PCB (Ericsson BMR and Takeshima) without balancing overall heat generation from power semiconductor devices mounted to the top and bottom surfaces of the converter's PCB. These references are also silent about the potential benefits of doing so.

75. One can compare this to Delta's product [REDACTED], [REDACTED]

[REDACTED]

[REDACTED] [REDACTED]

[REDACTED] [REDACTED]

[REDACTED]

[REDACTED] [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] (Ex. 1025).

## **VI. RELEVANT TIMEFRAME FOR DETERMINING OBVIOUSNESS**

76. I understand that obviousness must be evaluated at the time the alleged invention was made. From the front page of the '761 patent (left column, field “(62)” under “Related U.S. Application Data”), I understand that the first patent application was filed on May 11, 2011. I will assume for the purpose of this report that May 11, 2011, is the date the purported invention was made, with the understanding that my testimony will also be applicable to some time prior to May 11, 2011, approximately in the early-to-mid 2011. I may refer to this time period as the “relevant time frame”, and my testimony concerning obviousness is directed to this timeframe, even if I occasionally do not explicitly use a past tense.

## **VII. LEVEL OF ORDINARY SKILL IN THE ART**

77. I understand that the legal question of obviousness must be assessed from the perspective of a Person Having Ordinary Skill In The Art (“PHOSITA”) at the time of the invention. I understand that the Petitioner has stated that a person having ordinary skill in the art in the relevant timeframe “would have at least a Master’s degree in electrical engineering and two or more years of work experience relating to power electronics and the design of switching power converters, with more experience potentially substituting for education or vice versa.” I will apply this definition at this stage of the proceeding.

## VIII. CLAIM CONSTRUCTION

**A. Claim limitation 1[d]—“a power converter including...1[d] a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top surface....a second set of the power semiconductor devices being mounted on the bottom surface”**

78. Limitation 1[d] of claim 1 recites:

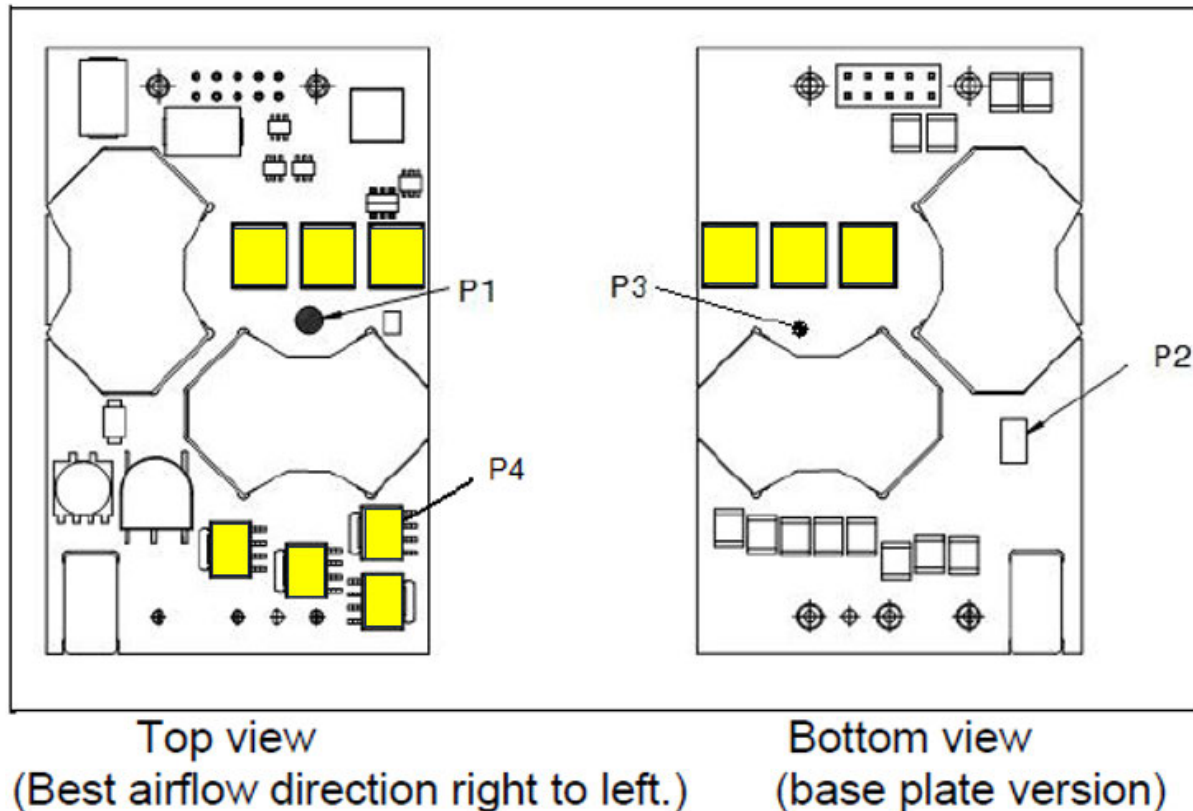
“a power converter including...1[d] a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top surface and electrically connected to dissipate power at a level,  $P_t$ , during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom surface and electrically connected to dissipate power at a level.  $P_b$ , during operation of the converter;”

79. In my opinion, claim limitation 1[d] should be construed such that “the first and second sets of the power semiconductor devices comprise all power semiconductor devices in the power converter.”

### 1. Relevance of the issue

80. I understand this issue to be relevant to the Petition’s assertion of obviousness over certain of the prior art references, like the “Ericsson BMR” data sheet. The device depicted in this data sheet has ten power semiconductor devices: seven on the top surface of the device, and three on the bottom surface. The ten power semiconductor devices are shown in the following figure from page 24 of

Ericsson BMR, which shows the top side (left) and bottom side (right), and where each power semiconductor device has been highlighted in yellow:



(Ex 1007, p. 24). As the figures illustrate, there are seven power semiconductor devices on the top surface, and three on the bottom surface.

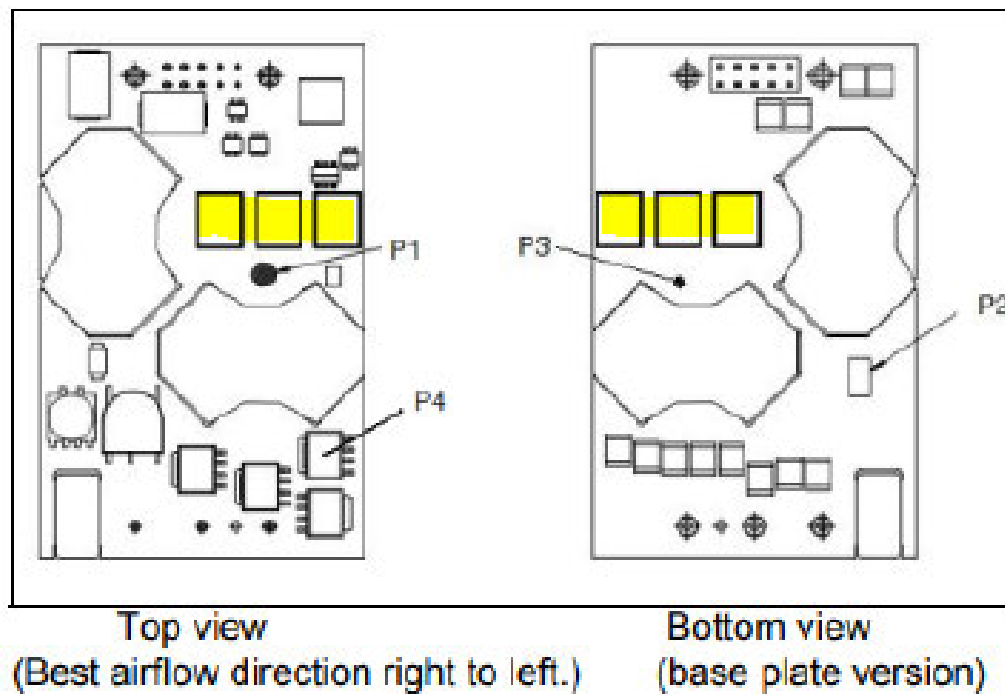
81. The presence of more than twice as many power semiconductor devices on the top surface of the PCB as on its bottom surface teaches away from claim limitation 1[e], which reads:

“the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level  $P_t$ ,  $P_b$  is less than 150% of the other

level Pb, Pt.”

More specifically, the three MOSFETs at the bottom of the PCB do not generate nearly as much heat as the seven MOSFETs at the top of the PCB.

82. The Petition disregards this issue by selectively including three of the seven MOSFETs in the “first set”, and ignoring the other four MOSFETs at the top. (Petition, p. 10). The Petition’s selection of devices is shown here:



(Petition, p. 22).

83. I understand that the Petition only counts three power MOSFETs on each side of the Ericsson BMR device, while effectively ignoring the other four power MOSFETs on the top of the device.

84. In my view, this is an incorrect reading of claim 1 of the '761 patent.

85. The specification of the '761 patent focuses on balancing the overall heat generation from all power MOSFETS (referred to in the following passage as “power FETs” or “power Field-Effect Transistors”) on the top and bottom surfaces of the PCB:

“In some examples, the FETs are arranged such that during operation, **the power FETs on the top surface dissipate power at a level that is comparable to the level of power dissipated by the power FETs on the bottom surface.** Also, the level of power dissipated by the power FETs in the upper input cell is comparable to the level of power dissipated by the power FETs in the lower input cell. For example, the level of power dissipated by the power FETs on one surface is less than 150% of the level of power dissipated by the power FETs on the other surface. The level of power dissipated by the power FETs in the upper cell is less than 150% of the level of power dissipated by the power FETs in the lower cell, and vice versa.”

(Ex. 1001, 25:11-24)(Emphasis added).

86. In my opinion, the '761 patent is clearly describing all of the power FETs on the top side of the PCB as one set, all of the power FETs on its bottom side as a second set, and comparing the heat generation of those two sets in their respective aggregates.

87. I did not see any embodiment in the '761 patent that describes balancing the power dissipation/heat generation of *subsets* of power semiconductor

devices on the top and bottom of the PCB. In my view, this is because, if one can balance the heat generation from the power MOSFETs on both sides of the PCB merely by choosing arbitrary *subsets* of devices on each surface, then claim limitation 1[e] is meaningless. Any time there are power MOSFETs on the top and bottom of the PCB—even if they were to be grossly unbalanced—one can attempt to assert the presence of limitation 1[e] by simply choosing and testing different subsets of the FETs until one is found on the top that coincidentally matches the operating heat generation of an equally arbitrary subset from the bottom of the PCB. This empties claim limitation 1[e] of meaning, and is contrary to the specification.

88. As I discuss above in ¶75, I have reviewed the infringement contentions for the Delta product [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]. [REDACTED]

## **IX. THE PRIOR ART DOES NOT RENDER THE CLAIMS OBVIOUS**

89. In my opinion, the Grounds in the Petition would not have rendered the claims of the '761 patent obvious.

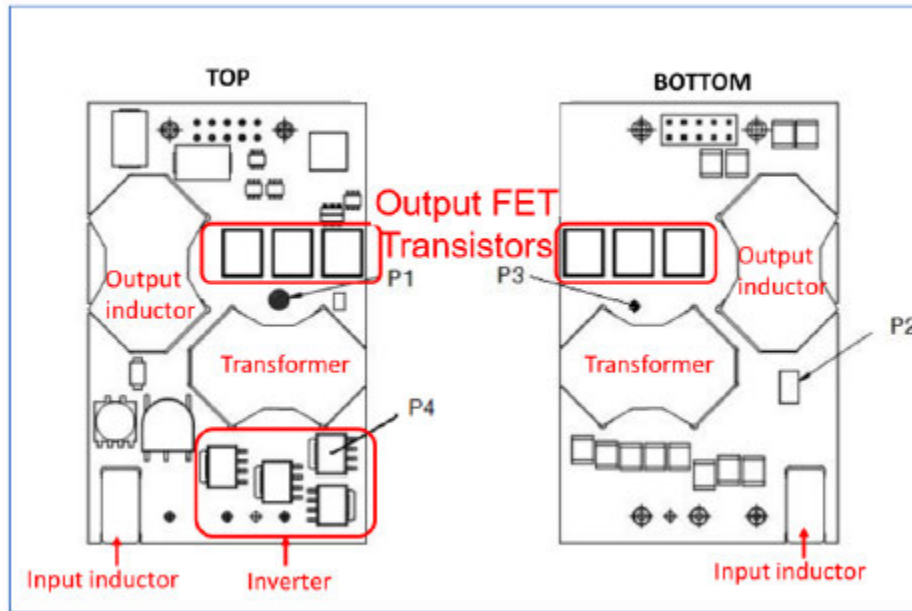
### **A. Ground I – (Ericsson BMR or BMR 2008) does not render the claims obvious**

90. First, in my opinion, Ground I (obviousness over Ericsson-BMR or BMR 2008) does not render the claims obvious.

#### **1. Ericsson BMR does not meet claim element 1[e]**

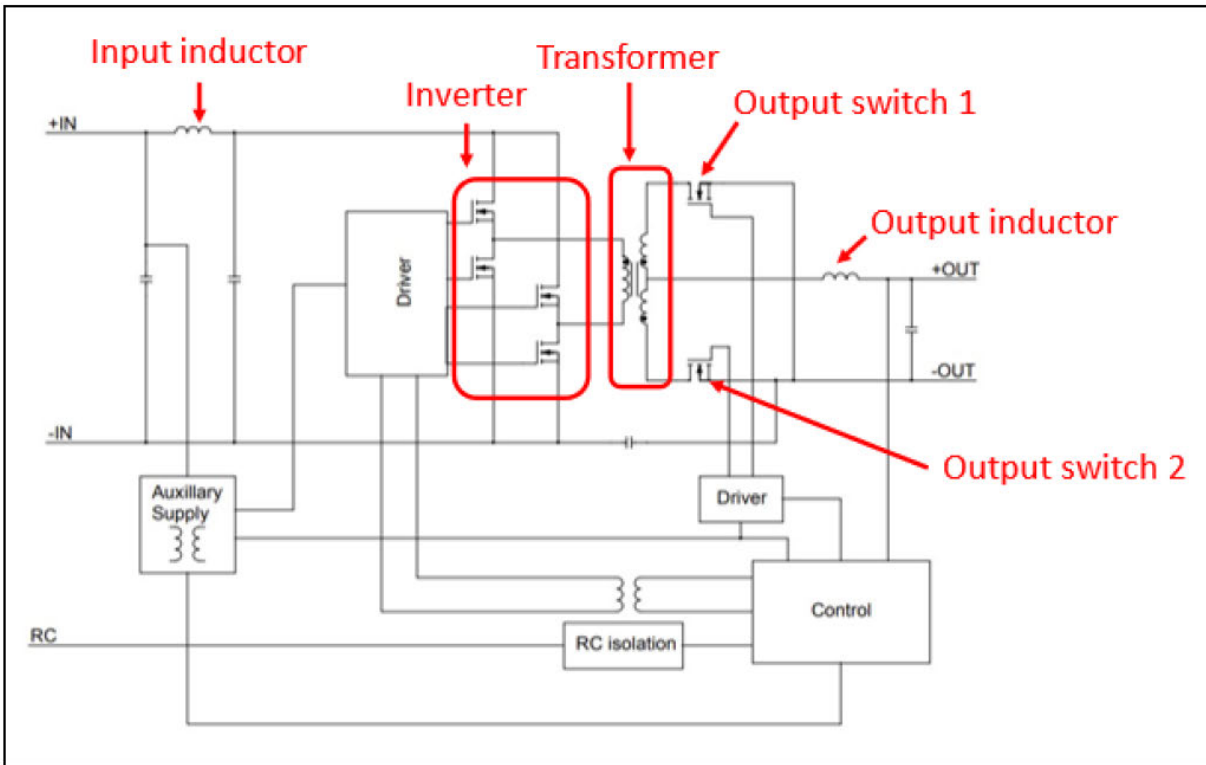
91. As I discuss above, Limitation 1[d] should be construed such that the first set and second set include all power semiconductor devices in the power converter.

92. With a proper construction of claim limitation 1[d], the Ground does not render obvious claim limitation 1[e], and in my view, teaches away from the limitation. Specifically, the Petition focuses only on a *subset* of power semiconductor devices, namely the output (secondary-side) MOSFETs, while ignoring *input* MOSFETs of the inverter, shown in the box labeled “Inverter” in the lower left of the annotated diagram from page 24 of the Petition (the labeling was present in the Petition).



(Petition, p. 24)(annotations in Petition).

93. This inverter, as shown, has four “primary” or input power MOSFETs. These MOSFETs can be seen in the circuit diagram from page 23 of the Petition, with red labeling added already in the Petition:



(Petition, p. 24)(Annotations in Petition). The four input MOSFETs of the inverter

are shown with MOSFET symbols, e.g. . (Ex. 1007, p. 24)(lower left, Table referring to “primary MOSFET” P4). The four input MOSFETs can be seen on the top surface of the device in the Figure on page 1 of Ex. 1007, reproduced here with added red arrows and a label:



(Ex. 1007, p. 1). These MOSFETs are power semiconductor devices.

94. By excluding the input (primary) MOSFETs, the Petition's argument fails to show that Ericsson BMR meets limitation 1[e]. The top of the PCB actually has seven MOSFETs (the three secondary MOSFETs and the four arbitrarily-excluded primary MOSFETs), while the bottom has only three. A PHOSITA would not expect the seven MOSFETs on the top surface to generate approximately the same heat as the three on the bottom surface.

95. Although an analysis of heat generation requires knowledge of how the MOSFETs are driven—and Delta does not provide this information—we do know that primary switches process all of the converter's power, as do secondary switches. That is, if the amount of power processed by the converter is "P", primary switches process power P, and secondary switches process power P.

Assuming, as Delta appears to assert, that the three secondary MOSFETs on the top side of the device process the same power as the three secondary MOSFETs on the bottom side of the device (each processing  $P/2$ ), then the MOSFETs on the top side of the device process  $P+P/2$  (or  $1.5 P$ ) and the MOSFETs on the bottom side of the device process  $0.5 P$ , or three times less power. As the heat generation of power semiconductor devices relates to power processed, top-side MOSFETs process three times as much power, giving rise to a commensurately greater amount of heat.

96. Thus, in my view, the Petition has not demonstrated that Ericsson BMR renders claim 1 obvious. The Petition argues that Ericsson 2008 has the same information as Ericsson BMR, so it would not render the claims obvious for the same reasons.

97. Thus, I am of the opinion that Ground I thus does not render the claims obvious.

**B. Ground II (Ericsson BMR or BMR 2008 and Spiazzi) does not render the claims obvious**

98. I am likewise of the opinion that Ground II does not render the claims obvious.

**1. Spiazzi does not change anything about Ericsson BMR or BMR-2008**

99. As I understand this Ground, the Petition is not proposing that it would have been obvious to change Ericsson BMR or BMR-2008 using Spiazzi, and so Ground II fails for the same reasons as Ground I.

**2. Spiazzi would not help a PHOSITA understand Ericsson BMR or BMR-2008**

100. The Petition argues that Spiazzi would help a PHOSITA recognize that the way Spiazzi operates is the way Ericsson BMR would operate. (Petition, pp. 36-39). In particular, the Petition appears to argue that a PHOSITA would recognize that Ericsson BMR would achieve test results similar to those of Spiazzi. (Petition, pp. 38-39).

101. The Petition's reasoning is incorrect. Spiazzi and Ericsson BMR are very different circuits, with different principles of operation. Spiazzi provides an academic model of converter heat, not a commercial converter like Ericsson's BMR. (Ex. 1011, p. 1, left column)(Petition, p. 87). Spiazzi is a high-frequency (1.8 MHz) resonant converter (Ex. 1011, p. 1, left column and title) while Ericsson BMR operates at a much lower (180 kHz) frequency (Ex. 1007, p. 7). This alone negates the Petition's argument that temperature test results would be the same for Spiazzi and Ericsson BMR. Resonant operation implies that the primary-side MOSFETs would be driven differently than in Ericsson BMR, and high-frequency

operation can impact dissipation of power semiconductor devices. (Ex. 1011, p. 2).

102. Moreover, Spiazzi uses phase-shift regulation, while Petitioner does not define how Ericsson BMR provides regulation. (Ex. 1012, p. 1, Abstract)(*cited by* Ex. 1011, p. 1, left column). The method of regulation is relevant, because a different regulation method can cause primary- or secondary-side switches to switch differently, or with different duty cycles, thus increasing or decreasing the heat generation of certain MOSFETs.

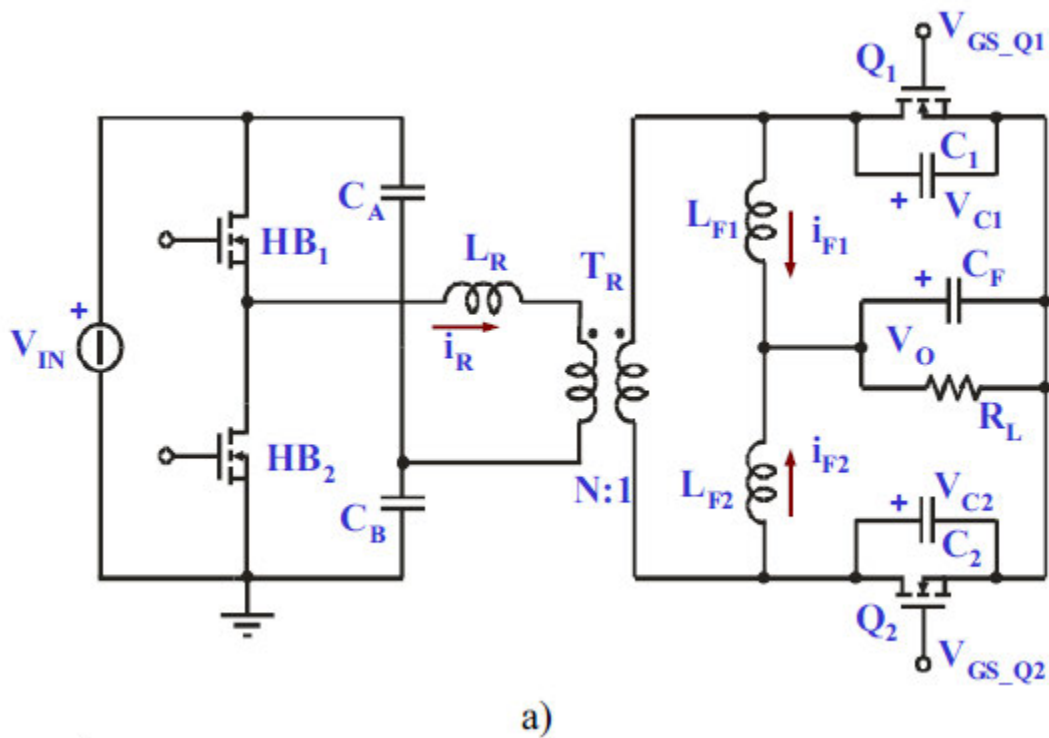
103. Spiazzi also states that its circuit is difficult to characterize thermally, because of the layout-dependent nature of the losses, stating:

“In this section we want to discuss the converter power losses distribution that will be used for the thermal simulation of the PCBs. **Due to the strong dependence on the layout, losses calculation is just an exercise**, without any correlation with the reality. **The only way is to measure them on the prototype**, which is usually not an easy task.”

(Ex. 1011, p. 3, right column, bottom)(Emphasis added).

104. The Petition argues that “Spiazzi teaches a half-bridge converter, which, like Ericsson-BMR’s full-bridge converter, would have at least obviously applied balanced power cycles in order to avoid saturating the transformer.” (Petition, p. 38). No further explanation is provided.

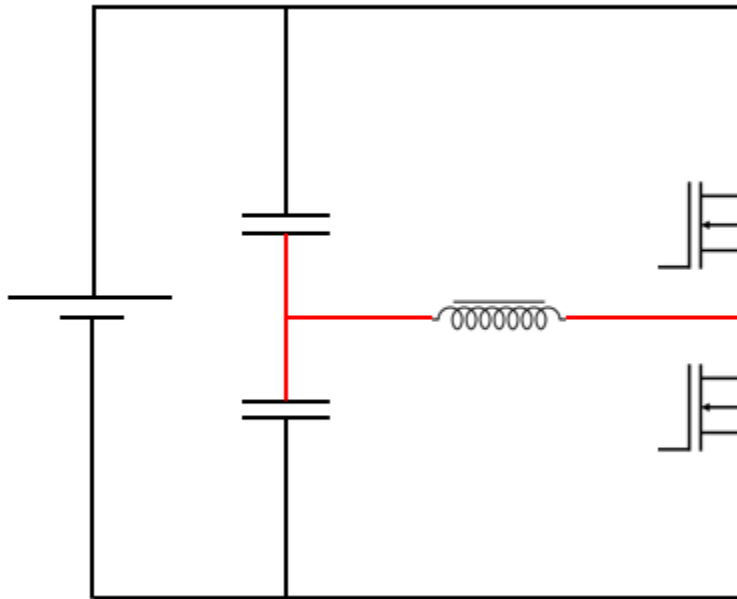
105. In my opinion, the Petition's argument is incorrect. As discussed in the textbooks submitted by Petition as Ex. 1008 at pp. 148-150, a transformer can saturate when its magnetizing current is not balanced in both directions, *i.e.*, when there is a DC component to the winding's magnetizing current. Spiazzi's half-bridge converter, however, connects two voltage-dividing input capacitors ( $C_A$  and  $C_B$ ) in series with its transformer primary winding, as shown here:



(Ex. 1011, p. 2, Fig. 1a). This is a common arrangement in a half-bridge converter, where the primary transformer winding is connected between two MOSFET switches ( $HB_1$  and  $HB_2$ ) and two voltage-dividing capacitors. The primary side of this converter is equivalent to show this in a simplified form below, where the portion that connects the transformer winding (symbol:  $\overline{\text{oooooo}}$ ) and inductor

$L_R$  (same symbol) between two capacitors (symbol:  $\equiv$ ) and the MOSFETs

(symbol:  $\text{MOSFET}$ ), where I color the connection over the transformer and inductor  $L_R$  in red:

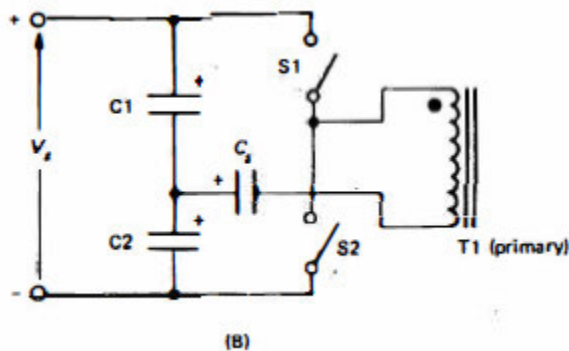


106. The voltage-dividing capacitors  $C_A$  and  $C_B$  of Spiazzi prevent saturation of the transformer independently of the duty cycle of the power semiconductor switches. For example, as the well-known textbook *Severns and Bloom* explained:

“For those DC transformation circuits which use a bridge or half-bridge primary switch connection, **a particularly simple means is available for eliminating transformer core saturation** due to primary volt-second imbalance. In these two converter circuits, the

primary winding of their transformers can be DC-isolated by the insertion of a series capacitor ( $C_s$ ) as shown in Fig. 4.20. **Notice that for the half-bridge version (Fig. 4.20B), the series DC-blocking capacitor function is accomplished inherently by the presence of the voltage-division capacitors,  $C_1$  and  $C_2$ .**”

(Ex. 2008, p. 116, Fig. 4.20B). Fig. 4.20B of *Severns and Bloom*, referenced in the quote above, is shown here:



(Ex. 2008, p. 117, Fig. 4.20B). This circuit has voltage-divider capacitors  $C_1$  and  $C_2$ , just like the voltage-divider capacitors  $C_A$  and  $C_B$  of Spiazzi. Both sets of voltage-dividing capacitors block DC components of the current, and prevent saturation of the transformer core due to imbalance independently of the duty cycle of its power semiconductor switches. Thus, I disagree with Dr. Leeb’s assertion (Ex. 1003, ¶112) that Spiazzi “would have at least obviously applied balanced power cycles in order to avoid saturating the transformer”.

107. I note that Dr. Leeb testified in a prior case that a similar circuit would not saturate the transformer because it was a half-bridge converter. The circuit about which Dr. Leeb testified is shown here:

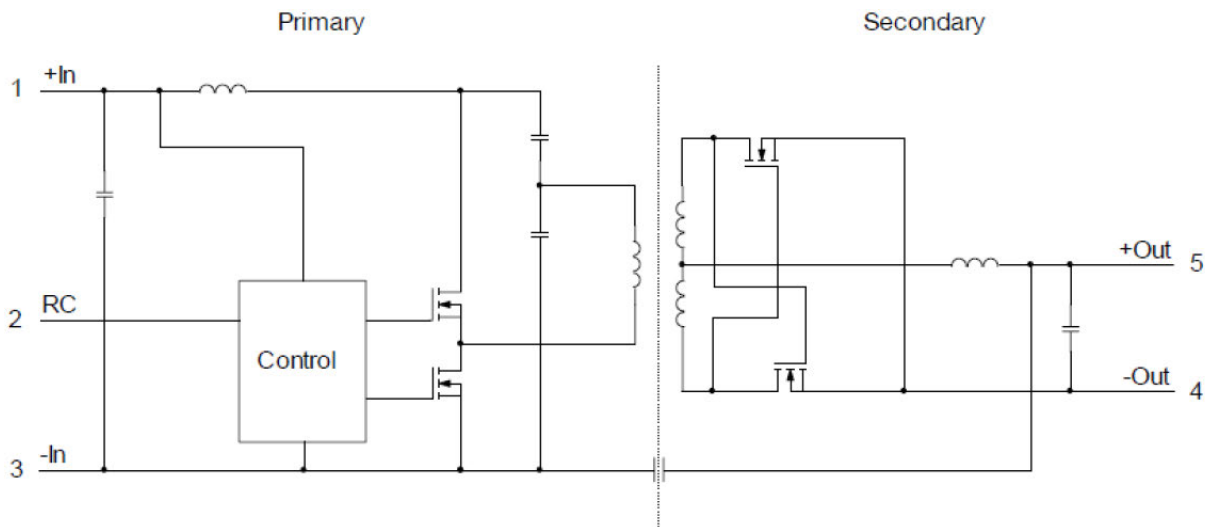


Exhibit I, PKM4303NF Datasheet at 4.

(Ex. 2009, ¶28, p. 14). This circuit, like the circuits of Spiazzi and *Severns and Bloom*, also uses a half-bridge topology with a transformer primary winding connected between two MOSFET switches and two voltage-dividing capacitors, where the voltage-dividing capacitors would prevent transformer saturation.

108. Thus, I disagree with Dr. Leeb's reasoning in the present case, that a PHOSITA would find it obvious to drive a half-bridge converter in a balanced way to avoid transformer saturation. Half-bridge circuits with series capacitors are driven with unbalanced duty cycles for good reason (for example, to regulate the output voltage) without risk of transformer saturation.

109. Because of the different nature of the Spiazzi and Ericsson BMR circuits, the fact that Spiazzi teaches that losses from its circuit are highly layout-dependent, and the fact that the Petition's only argument to connect the two circuits is factually wrong, I am of the opinion that the Petition has not shown that a PHOSITA would have believed that testing on Spiazzi's converter would apply to Ericsson BMR.

### **3. Spiazzi does not teach limitation 1[e]**

110. In my opinion, Spiazzi also does not teach claim limitation 1[e]. First, Spiazzi, like Ericsson-BMR, places its input MOSFETs (HB1 and HB2) only on the top side of the device. (Ex. 1011, Fig. 5a). This unbalances heat generation of the power semiconductor devices on the top and bottom sides of the Board. As Spiazzi's Table II (below) indicates, the primary-side (input) MOSFETs on the top side dissipated about twice the power (1.02 W) of the secondary-side MOSFETs (0.44 W) on the top side. (Ex. 1011, p. 4, Table II). Table II is reproduced here, with highlighting added:

TABLE II. DISSIPATED POWER FOR THE MAIN HEATING COMPONENTS ESTIMATED FROM MEASUREMENTS

| Component          | Ref. name | I <sub>out</sub> =30A<br>Power<br>[W] | I <sub>out</sub> =40A<br>Power<br>[W] | I <sub>out</sub> =50A<br>Power<br>[W] |
|--------------------|-----------|---------------------------------------|---------------------------------------|---------------------------------------|
| Primary MOSFET 1   | IRF7855   | 0.32                                  | 0.51                                  | 0.72                                  |
| Primary MOSFET 2   | IRF7855   | 0.32                                  | 0.51                                  | 0.72                                  |
| Primary driver     | LM5101A   | 1.0                                   | 1.0                                   | 1.0                                   |
| Primary inductor   | -         | 0.43                                  | 0.68                                  | 0.95                                  |
| Transformer        | -         | 0.9                                   | 1.5                                   | 2.1                                   |
| Secondary inductor | -         | 0.18                                  | 0.32                                  | 0.5                                   |
| Secondary traces   | -         | 0.15                                  | 0.22                                  | 0.27                                  |
| Secondary MOSFET 1 | IRF7836   | 0.087                                 | 0.11                                  | 0.21                                  |
| Secondary MOSFET 2 | IRF7836   | 0.087                                 | 0.11                                  | 0.21                                  |
| Secondary MOSFET 3 | IRF7836   | 0.087                                 | 0.11                                  | 0.21                                  |
| Secondary MOSFET 4 | IRF7836   | 0.087                                 | 0.11                                  | 0.21                                  |
| Secondary driver   | IRF7319   | 1.0                                   | 1.0                                   | 1.0                                   |

(Ex. 1011, p. 4, Table II)(highlighting added).

111. If one assumes for the moment (as Delta argues) that four bottom-side secondary MOSFETs would dissipate the same power as top-side secondary MOSFETs, this would mean that top-side MOSFETs, including primary MOSFETs, would in the aggregate generate heat at a rate of 1.46 W (0.51 + 0.51 + 0.11 + 0.11 + 0.11 + 0.11), whereas the bottom-side MOSFETs would dissipate power at only 0.44 W (0.11 + 0.11 + 0.11 + 0.11), or more than three times less. (1.46 / 0.44 = 3.31).

112. Delta argues that “Spiazzi further confirms that Ericsson-BMR’s full-bridge circuit would produce substantially similar results of power dissipation on both sides of the Ericsson-BMR module”, referring in particular to Spiazzi’s statement that “[s]imilar results were obtained for the downward surfaces.” See EX1011 at 1999.” (Petition, p. 38)(emphasis in original).

113. However, Spiazzi’s statements about its temperature measurements do not indicate that Spiazzi meets claim limitation 1[e]. Spiazzi measured temperature on only one side of the board. (Ex. 1011, p. 7). Spiazzi’s statement that “[s]imilar results were obtained for the downward surfaces” cannot be referring to the *entire set* of Table III, because numerous components in Table III (such as primary MOSFETs 1 and 2, Primary driver, Primary inductor wound, Primary inductor core, and Transformer) are not found on the downward surface. Instead, Spiazzi is simply commenting that the results were similar, which is relevant to the primary purpose of his paper, showing general agreement between Spiazzi’s numerical model and measured values—regardless of what those values were. (Ex. 1011, p. 7, right column, p. 1, Abstract).

#### **4. Spiazzi teaches away from the claims**

114. I am further of the opinion that Spiazzi teaches away from the claims of the ’761 patent. Specifically, Spiazzi teaches that, if MOSFETs are placed on the bottom of a PCB, it is necessary to add a heat-conducting layer between PCB

fiberglass layers in order to remove heat. (Ex. 1011, p. 3, bridging left and right columns)(“Having power components on both sides of the PCB, the only way to remove the heat was to have a dissipating layer in between the two component layers, that was also used as ground connection at secondary side.”).

115. This is consistent with the conventional wisdom I discuss above in ¶¶72-73 to place MOSFETs on the top side of the PCB, and teaches away from the claims by counseling a PHOSITA to (1) place MOSFETs on the top of the PCB or otherwise (2) use a thick copper baseplate (rather than a multi-layer PCB) where (1) is not possible. Placing MOSFETs on the top of the device teaches away from limitations 1[d] and 1[e], whereas using a thick copper baseplate teaches away from limitations 1[b] and 1[c], because a copper baseplate would interfere with a transformer structure using PCB windings (and indeed, Spiazzi uses a transformer with windings above the PCB). (Petition, p. 86)(“Spiazzi’s windings are not formed by traces in one or more of the conductive layers in the PCB.”)(Ex. 1011, p. 2).

116. I am thus of the opinion that Ground II thus does not render the claims obvious.

**C. Ground III (Ericsson BMR and Wanes) does not render the claims obvious**

117. I am further of the opinion that Ground III (Ericsson BMR and Wanes) does not render the claims obvious.

**1. Wanes teaches away from Ericsson BMR and BMR 2008**

118. First, I am of the opinion that Wanes teaches away from the combination with Ericsson BMR or Ericsson 2008. Wanes is an unusual converter design, the construction of which requires some background.

119. The Petition focuses on the embodiment of Fig. 9A and 9B, shown here:

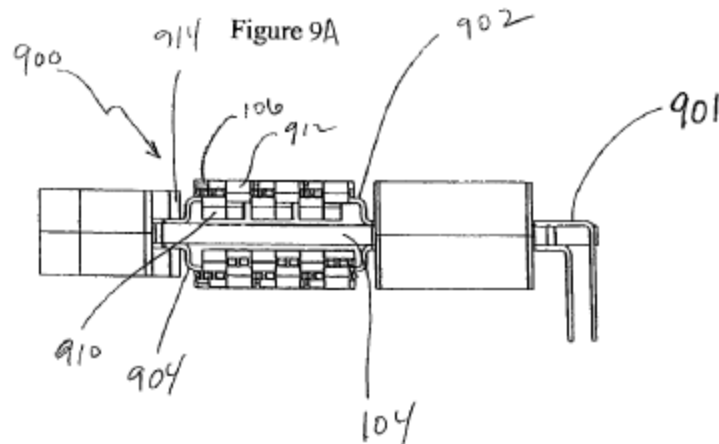
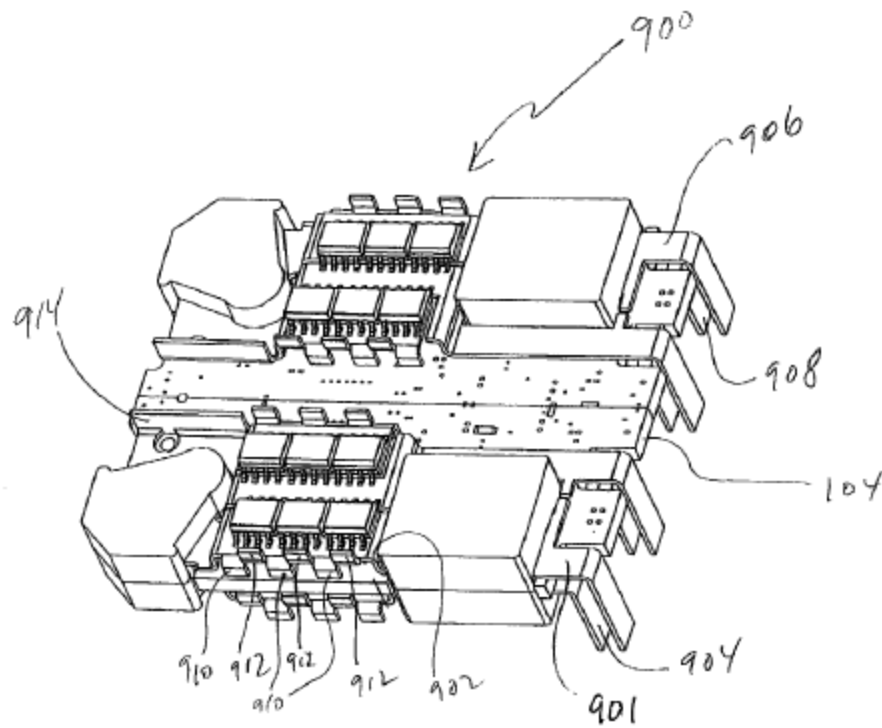


FIGURE 9B

(Ex. 1009, Fig. 9A, 9B). In Fig. 9A of Wanes, there is a circuit board 104. (Ex. 1009, 3:65). Mounted to that board are copper structures 902, as shown below, with added green coloring to show the PCB, and added copper coloring to show the copper structures 902:

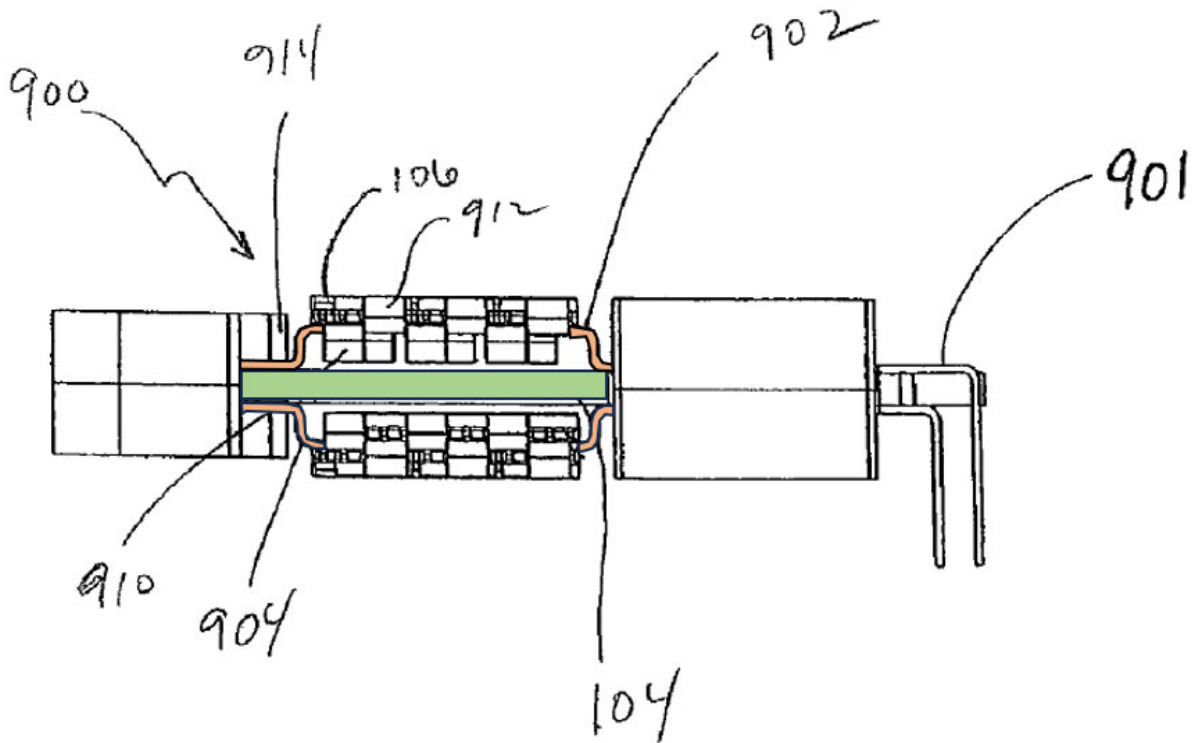


FIGURE 9B

(Ex. 1009, Fig. 9B, 11:4-36, 5:39-47).

120. The raised copper structures 902 serve to mount MOSFETs separate and apart from the circuit board. (Ex. 1009, 11:20-23, 7:37-40). The copper structures 902 also serve as a conductor that forms the secondary winding of the transformer. (Ex. 1009, 4:33-37, 5:39-60).

121. Wanes teaches that the copper structure 902 should not be within the PCB structure, for thermal management reasons:

“burying the thick copper layer within the PCB does not allow

effective dissipation of heat carried in the encapsulated copper layer, and will tend to reduce the number of substrate layers available for other design purposes.”

(Ex. 1009, 6:3-7).

122. Secondary windings in a converter providing N:1 voltage step-down carry N times more current than primary windings. Higher current in secondary windings leads to higher resistive losses, which are proportional to the *square* of the current. A PHOSITA would thus likely have understood Wanes to be teaching the use of a thick, *external* copper structure, or lead-frame, for the secondary winding because the secondary winding would give rise to high resistive losses.

123. Ericsson BMR and BMR 2008, however, are structurally different. Nor does the Petition provide any argument that Ericsson BMR and BMR 2008 should be modified to include a raised copper structure, or lead-frame, that could serve to support a mounting surface for MOSFETs and provide a secondary transformer winding. Instead, according to the Petition, the windings of Ericsson BMR (and BMR 2008) are found within the PCB—exactly what Wanes teaches *not* to do. (Ex. 1009, 6:3-7).

124. I am thus of the opinion that Ground III thus does not render the claims obvious.

**D. Ground IV (Obviousness over Takeshima) does not render the claims obvious**

125. I am further of the opinion that Ground IV (Obviousness over Takeshima) does not render the claims obvious.

**1. There is no motivation to modify Takeshima to reach limitation 1[d]**

126. First, I am of the view that there would have been no motivation to modify Takeshima to reach limitation 1[d]. This limitation reads:

“1[d] a plurality of power semiconductor devices, a first set of the power semiconductor devices being mounted on the top surface and electrically connected to dissipate power at a level, Pt, during operation of the converter, a second set of the power semiconductor devices being mounted on the bottom surface and electrically connected to dissipate power at a level. Pb, during operation of the converter;...”

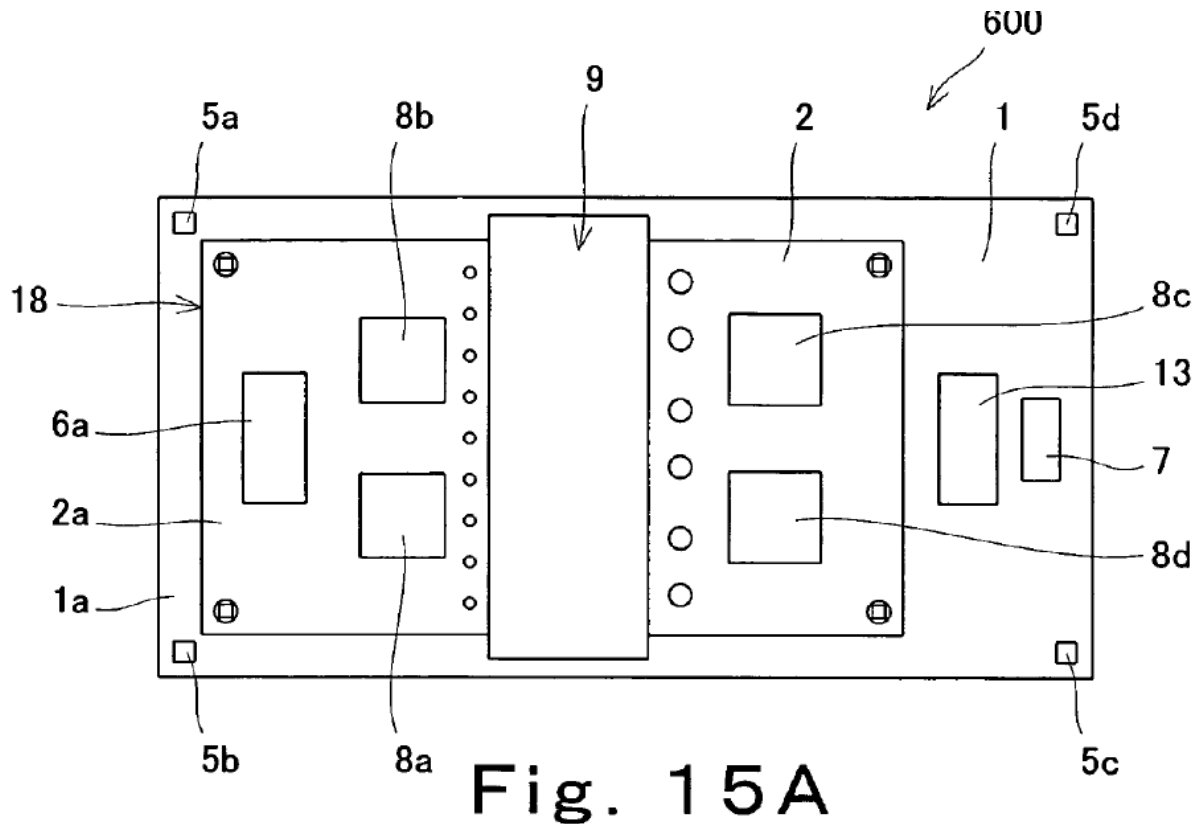
127. To meet limitation 1[d], the Petition argues that a PHOSITA would have combined the Fig. 2 embodiment of Takeshima with the Fig. 14 embodiment, resulting in a Fig. 14 embodiment that has MOSFETs on the secondary side on the top and bottom of the PCB. (Petition, p. 56-58). With respect to motivation for this alteration of Takeshima’s embodiments, the Petition argues:

“Takeshima teaches that ‘MOS field-effect transistors (hereafter abbreviated as ‘MOSFETs’) 8a and 8b’ are placed on the top and bottom of the PCB, as shown here in this annotated Figure 2: [Figure

omitted] Takeshima teaches that this layout could ‘advantage[ously]’ employ a ‘half-bridge’ converter circuit such as that shown in Figure 7, and further that ‘other converter circuits may be used.’ *See* EX1010 at 7:47-50, 14:44-59.”

(Petition, pp. 56-57).

128. In my opinion, there are several problems with this motivation. The first problem is that reference to a half-bridge or other converter topology says nothing about *where* its power semiconductor components should be located, and in particular, whether they should be placed on the top and/or bottom of a PCB. This is important because the circuit of Fig. 14 *already has a layout*, and it has *no MOSFETs on the bottom of the device*. Specifically, Fig. 14 belongs to the “third preferred embodiment” of Takeshima (Ex. 1010, 8:8-11), and the third preferred embodiment layout is shown in Fig. 15 (Ex. 10101, 8:12-18), with MOSFETs 8a-8d located on the *top* of the PCB:



(Ex. 1010, Fig. 15A).

129. Thus, the Petition only provides a purported motivation (using a half-bridge primary-side topology) that does not address the main modification needed to combine the Fig. 2 and Fig. 14 embodiments: namely, splitting the MOSFETs shown on the top of the device in Fig. 15A into two sets, and placing these MOSFETs into overlapping positions on the top and bottom of the PCB. .

130. Moreover, Takeshima explains with respect to another embodiment, that of Fig. 5, that Takeshima intentionally places topologically parallel MOSFETs together. (Ex. 1010, 12:53-64). This can have a variety of advantages such as reducing wiring lengths and optimizing a layer of thick wiring for the high-current-

carrying devices. (Ex. 1010, 12:53-64). It is also consistent with the known methodology of placing high-power-dissipating devices on the top surface of the PCB (see ¶¶68-71, above).

131. The Petition does not address the fact that Takeshima expressly places the MOSFETs of the third embodiment (including Fig. 14) on the same side of the board, nor the likely reasons for it, and thus fails to make a reasonable case for obviousness.

**2. Takeshima does not disclose or render obvious limitation 1[e]**

132. I am also of the opinion that Takeshima fails to disclose or render obvious limitation 1[e]. This limitation reads:

“1[e] wherein the power semiconductor devices are distributed between the first and second sets to distribute heat generation during operation of the converter such that each level Pt, Pb is less than 150% of the other level Pb, Pt.”

133. The Petition argues that “[a] POSITA would have known to operate Takeshima’s half-bridge converter with balanced power cycles on the top and bottom sides in order to avoid saturating the transformer” (Petition, p. 59), and that, with balanced power cycles on the primary side, “a POSITA would have expected” the MOSFETs to generate approximately equal heat. (Petition, p. 59).

134. I am of the opinion that this argument is incorrect. Takeshima’s half-bridge power converter (as shown in Fig. 14) has capacitors 6a and 6b in series

with transformer primary winding 9a that preclude transformer saturation and enable it to operate with a variable, unbalanced duty cycle. Fig. 14 is reproduced here, with the voltage-dividing series capacitors outlined with added red-dashed boxes:

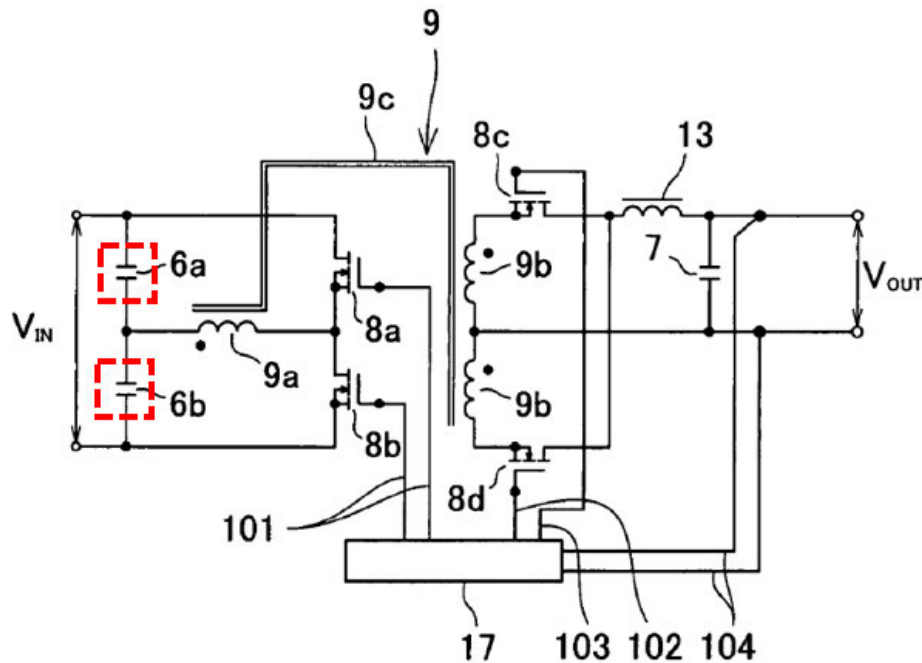


**Fig. 14**

(Ex. 1010, Fig. 14).

135. The topology of Takeshima's half-bridge embodiment connects the primary-side transformer winding 9a between the primary-side switches and the voltage-dividing capacitors 6a and 6b, in the same way I discuss above in ¶¶105-

109. This arrangement prevents transformer saturation, because the voltage-dividing capacitors block DC components of the transformer current. (Ex. 2008, p. 100, Fig. 4.20B). The half-bridge topology of Takeshima also prevents transformer saturation in the same way as the circuit about which Dr. Leeb testified in a prior case as I discuss above in ¶107. (Ex. 2009, ¶¶28, 31, pp. 14, 18).

136. Thus, I am of the opinion that the Petition is incorrect that a PHOSITA would know to operate Takeshima with balanced power cycles to avoid saturating the transformer. .

137. In fact, a PHOSITA would probably expect that Takeshima's MOSFETs, even if rearranged in the manner discussed in the Petition, would have unbalanced power dissipation. This is because Takeshima's third embodiment (on which the Petition relies) is a regulating converter that uses PWM to operate both primary and secondary MOSFETs with a variable duty cycle to regulate the output voltage. (20:10-23). As Takeshima explains:

“The output voltage from both ends of the output smoothing capacitor 7 is constantly monitored by the control circuit 17, and the control circuit 17 controls the on-off ratio of the switching operation of the MOSFETs 8a and 8b by varying the turn-on signal in order to stabilize the output voltage. The turn-on signal is also applied to the gate terminals of the MOSFETs 8c and 8d with the same phase. Consequently, the MOSFETs 8c and 8d will perform a rectified operation in response to the turn-on signal (commonly called

‘synchronous rectification’). Since the control circuit 17 operates in the above-described manner, the direct current voltage that is output from the switching power supply device 100 is stabilized.”

(Ex. 1010, 20:10-23). The Petition does not address this PWM regulation. With such regulation, output MOSFETs operate with a variable duty cycle, in unbalanced fashion, in order to compensate for the variation in input voltage. In systems in which Takeshima’s device could be expected to be used (powering personal computers, 1:9-29, 2:7-11), input voltages vary. (Ex. 2010, p. 14, Table 5)(Ex. 2011, p. 12, Fig. 3). That, in fact, is the reason that output regulation is needed in Takeshima’s embodiment 3 device. Specifically, in personal computers, there is a power supply unit (the black box attached to the power cord in most personal computers that provides (usually) a 12 V DC output. This voltage, in the relevant timeframe, could vary over a range of, e.g., 10% (+/-5%). (Ex. 2010, p. 14, Table 5). When supplied to a processor, however, the voltage needed to be regulated more tightly, for example to +/- 20 mV at a 1.1 V input. (Ex. 2011, p. 12, Fig. 3). This typically required a Voltage Regulator Module on the board to supply the voltage to the processor. Takeshima represents such a voltage regulator. (Ex. 1010, 1:9-29, 18:45-47). That, in fact, is the reason that output regulation is needed in Takeshima’s embodiment 3 device.

138. For these reasons, I am of the opinion that the Petition has not met its burden to demonstrate that a hypothetically-modified Takeshima would meet limitation 1[e], and Ground IV does not render the claims obvious.

**E. Ground V (Takeshima and Spiazzi) does not render the claims obvious**

139. I am further of the opinion that Ground V (obviousness over Takeshima in view of Spiazzi) similarly does not render the claims obvious.

**1. Spiazzi's method of operation is not relevant to Takeshima**

140. Ground V is not clear. However, to the extent the Petition is arguing that a PHOSITA would use statements in Spiazzi to recognize that Takeshima would meet limitation 1[e], it is my opinion that the Petition is incorrect.

Takeshima does not teach limitation 1[e], as I discuss above in ¶¶132-138, and Spiazzi does not provide balanced operation, as I discuss above in ¶¶110-113.

141. Moreover, Spiazzi and Takeshima are very different circuits, such that a PHOSITA would not think that test results from Spiazzi apply to Takeshima. In particular, Spiazzi is a phase-shift modulated circuit (Ex. 1012, p. 1, Abstract)(cited by Ex. 1011, p. 1, left column), while Takeshima is a pulse-width modulated circuit (Ex. 1010, 20:10-23). Spiazzi is regulating the output by shifting the phase between primary and secondary side MOSFETs, while Takeshima is regulating the output by changing the ON and OFF times of the primary and

secondary side MOSFETs. There is thus no reason to think that Spiazzi's circuit would behave similarly to Takeshima's.

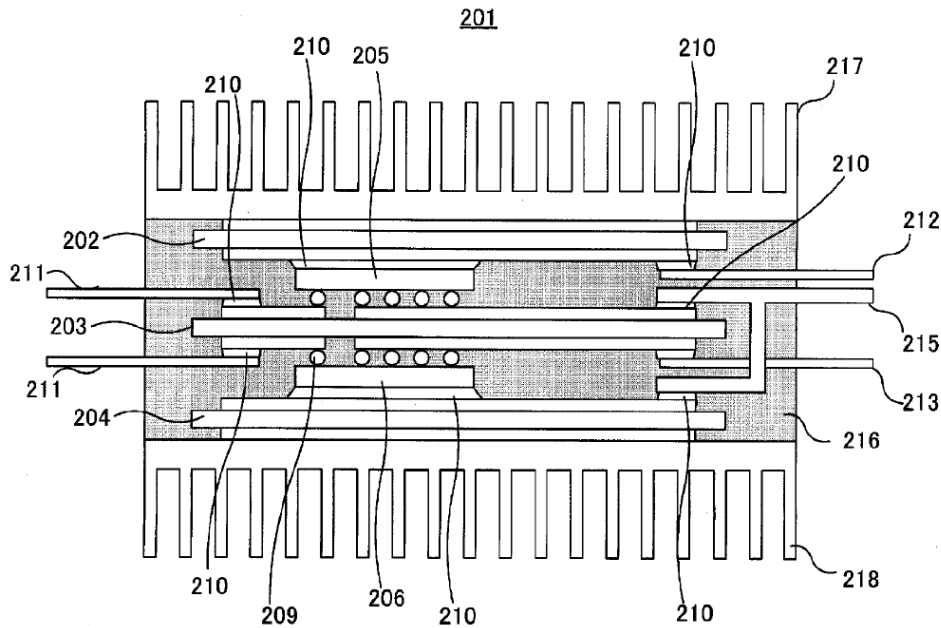
## **2. Spiazzi and Takeshima teach away from one another**

142. I am also of the opinion that Takeshima and Spiazzi teach away from one another. First, Takeshima teaches separating MOSFETs from control circuitry, in order to achieve a host of advantages. (Ex. 1010, 13:49-14:31). Spiazzi, however, places control circuitry on the same board surface as the MOSFETs (Figs. 5). Spiazzi teaches that with components on both sides of the board, thermal management is difficult, and that it is best to use a thick copper baseplate between two layers of PCB, as in PCB 2. (Ex. 1011, p. 3, bridging left and right columns). This thick copper baseplate interferes with the formation of transformer windings within the PCB, and thus runs contrary to the allegation of the Petition (Petition, p. 56) that Takeshima contains transformer windings within the PCB conductive layers. It would thus not be obvious to combine the two references.

## **3. The Kawanami reference**

143. Finally, I note that the Petition cites that Kawanami reference (Ex. 1023). In my view, the Kawanami reference is very different from Takeshima and Spiazzi. Kawanami is a power converter designed for electric motor control applications. (Ex. 1023, ¶0002). Its structure is markedly different from that of

both Spiazzi and Takeshima, having a semiconductor package with multiple substrates, where each of several chips are mounted to their own substrates, and these substrates are stacked. This is shown in Fig. 1 of Kawanami, reproduced here:



(Ex. 1023, Fig. 1). In Fig. 1, elements 202 and 204 are insulated substrates (possibly a fiberglass reinforced epoxy laminate of a PCB), while elements 205 and 206 are semiconductor chips. (Ex. 1023, ¶¶0038-0039). The chips are further separated by an insulating element 203. (Ex. 1023, ¶0038). Kawanami also has heat sinks with radiating fins (217 and 218) on both sides of the device. (Ex. 1023, ¶¶0040, 0084-0085).

144. Given the differences in structure and area of application between Kawanami on the one hand and Spiazzi and Takeshima<sup>1</sup> on the other hand, a PHOSITA would not take recommendations from Kawanami and believe them to be relevant to Spiazzi or Takeshima. In particular, while Kawanami is able, in its particular application field, to place heat sinks on both sides of the device, Spiazzi teaches that by having MOSFETs on both sides of a PCB, a copper baseplate within the PCB layers is required to manage heat. (Ex. 1011, p. 3, bridging left and right columns).

145. I am thus of the opinion that Ground V thus does not render the claims obvious.

**F. Ground VI (Takeshima and Wanes) does not render the claims obvious**

146. I am further of the opinion that Ground VI (obviousness over Takeshima in view of Wanes) does not render the claims obvious.

147. First, Ground VI is not clear. The Petition provides no overview or explanation of what, if anything, is being modified in Takeshima. In the mapping for claim 1, the Petition merely refers back to Ground IV, except under limitation 1[e]. There, the Petition states only that “[i]n the asserted embodiment,

---

<sup>1</sup> Both Spiazzi and Takeshima are directed to voltage regulators (VRs) to power CPUs. (Ex. 1011, p. 1, left column)(Ex. 1010, 1:9-25).

Takeshima's module is in the environment of Wanes, thus confirming equal or at least approximately equal power dissipation and thus satisfying this element."

(Petition, pp. 77-78). The Petition, however, provides no evidence from Wanes to prove this, and no explanation of what the "asserted embodiment" is. It is also unclear what is meant by "the environment of Wanes". I do not see that the Petition cites to Wanes (Ex. 1009) under its analysis for claim 1 at all. Other than citations to Dr. Leeb's declaration and cross-references to Ground IV, the Petition only quotes Spiazzi (Ex. 1011) under limitation 1[e].

148. This leaves the manner in which Wanes is applied in Ground VI entirely a matter of speculation. Furthermore, because there is no apparent modification to Takeshima based on Wanes, the Ground adds nothing to the already-deficient Ground IV (or, if Spiazzi is being applied, Ground VI).

149. I am thus of the opinion that Ground VI thus does not render the claims obvious.

**G. Ground VII (Ericsson BMR or Ericsson 2008 and Takeshima) does not render the claims obvious**

150. I am further of the opinion that Ground VII (obviousness over Ericsson BMR or Ericsson 2008 in view of Takeshima) does not render the claims obvious.

151. The assertion against claim 1 in Ground VII is based on Ground I, because the claim mapping under each claim element refers back to the

corresponding element of claim 1 under Ground I. Ground VII purports to alter the argumentation under Ground I as to claim 1 in only two ways, namely:

- under limitation 1[c], by arguing that a PHOSITA would have been motivated to form Ericsson-BMR's transformer windings within a PCB based on Takeshima (Petition, p. 80); and
- under limitation 1[d], by arguing that "Takeshima further confirms that Ericsson's output FETS<sup>9</sup> could have been those that are placed symmetrically and that it would have been an obvious design choice for the output FETs used as output switches by Ericsson-BMR". (Petition, p. 81).

152. Ground VII thus does not address the deficiencies in Ground I that I discuss above.

153. Thus, I am of the opinion that Ground VII thus does not render the claims obvious.

#### **H. Ground VIII (Spiazzi and Wanes) does not render the claims obvious**

154. Finally, I am of the opinion that Ground VIII (obviousness over Spiazzi in view of Wanes) does not render the claims obvious.

##### **1. The combination does not render obvious limitation 1[c]**

155. First, in my view, the combination of Spiazzi and Wanes would not render obvious limitation 1[c], which requires "1[c] a magnetic core structure

magnetically coupled to a winding formed by traces in one or more of the conductive layers in the PCB”.

156. The Petition proposes to modify Spiazzi with Wanes, arguing:

“Spiazzi’s windings are not formed by traces in one or more of the conductive layers in the PCB. However, Wanes does teach the layout approach of using the converter PCB to form windings....A POSITA would have been motivated to form Spiazzi’s windings in the manner described in Wanes for a number of reasons.”

(Petition, p. 86). The Petition then argues that forming transformer windings as PCB layers was well-known and space-efficient, and that Spiazzi would have moved toward that technique upon transition from a research product to a commercial device. (Petition, p. 87).

157. The principal issue with this reasoning is that Spiazzi does not provide a multilayer circuit board that *could be* used for windings. Spiazzi has two variants, PCB1 and PCB2. (Ex. 1011, p. 3). Both of these structures have two PCB layers that sandwich a middle copper plate that acts as a ground plane (in PCB1 the middle copper layer is 0.14 mm thick and in PCB2 it is 0.7 mm thick, p. 3). Spiazzi ultimately recommends PCB2. (Ex. 1011, p. 7). According to Spiazzi, the middle heat-conducting layer is *necessary* to remove heat when components are placed on the back side of the structure. Spiazzi explains:

“Having power components on both sides of the PCB, the only way

to remove the heat was to have a dissipating layer in between the two component layers....”

(Ex. 1011, p. 3, bridging left and right columns).

158. A PHOSITA would not have expected to be able to construct transformer windings in Spiazzi’s structure, because windings would conflict with Spiazzi’s copper plate, which Spiazzi says is “the only way” to sufficiently remove heat. (Ex. 1011, p. 3, bridging left and right columns). Notably, the Petition does not assert that there would have been a reasonable expectation of success in modifying Spiazzi’s structure to accommodate a multi-layer PCB, without a thermally-conductive baseplate, that could use PCB conductive layers to form transformer windings.

## **2. The combination does not teach limitations 1[d] and 1[e]**

159. I am also of the opinion that the combination relies only on Spiazzi to meet limitations 1[d] and 1[e]. As I discuss above in ¶¶110-111, however, Spiazzi’s input MOSFETs are entirely located on the top side of the device, and Spiazzi’s own measurements indicate that the MOSFETs on the top side would dissipate 3.31 times the power of the MOSFETs on the bottom side. (Ex. 1011, p. 4, Table II). Furthermore, contrary to the Petition’s assertion, Spiazzi’s statement that “[s]imilar results were obtained for the downward surfaces” is not sufficiently clear to demonstrate that claim limitation 1[e] was met.

160. The Petition's argument based on a statement in Huber (Ex. 1012) is incorrect. In the section in which the statement occurs, Huber, *et al.* are attempting to provide a simple mathematical characterization of the converter while at steady state. The statement that "the behavior of the circuit *is the same* as during the positive half cycle" means that, in general, the mathematical relationships in the simplified model do not need to be re-derived for the negative half cycle. At that stage in the article, however, Huber, *et al.* had not considered output regulation over changes in input voltage and output current. Output regulation in Huber's converter depends on a phase-shift between primary and secondary MOSFETs. The Petition fails to consider the effect of output regulation under operating conditions.

161. Moreover, there is substantial guesswork involved in the obviousness argument, because the Petition seeks to rearrange, in an unspecified fashion, Spiazzi to incorporate PCB transformer windings. Transformer windings tend to occupy large portions of a PCB, and Wanes further teaches to use an exposed, raised copper portion to form secondary windings. (Ex. 1009, 6:3-7). It is unclear how these teachings could be combined. The Petition's contemplated design is not specified. Spiazzi itself emphasizes that for its converter, stating "component placement and routing have a strong impact not only on parasitic components, but also on the overall converter efficiency, thus affecting the thermal management"

(Ex. 1011, p. 1) and that “[d]ue to the strong dependence on the layout, losses calculation is just an exercise, without any correlation with the reality. The only way is to measure them on the prototype, which is usually not an easy task.” (Ex. 1011, p. 3).

162. Once a PHOSITA changes the Spiazzi layout, a PHOSITA would expect, based on Spiazzi’s own statements, to achieve fundamentally different heat generation results, which the Petition completely fails to address.

163. I am thus of the opinion that the Grounds in the Petition thus fail to carry the Petitioner’s burden.

**X. OATH**

164. This declaration and my opinions herein are made to the best of my knowledge and understanding, and based on the material available to me, at the time of signing this declaration. I declare under penalty of perjury under the laws of the United States of America that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon.

February 28, 2024  
Date



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Dr. Juan Rivas-Davila



# Juan Manuel Rivas Davila

ASSOCIATE PROFESSOR

Electrical Engineering Department, Stanford University

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*My lab is the Stanford University Power Electronics Research Laboratory (SUPER-Lab), and we work in high frequency power electronics. My research interests are broadly in circuits, power electronics, resonant converters, gate drives, high-frequency passive components, Wide Bandgap devices, and finding new applications for converters.*

## Academic History

### Massachusetts Institute of Technology

DOCTOR OF SCIENCE

- Advisor: Prof. David J. Perreault

Cambridge, MA

September 2003–May 2006

### Massachusetts Institute of Technology

MASTER OF SCIENCE

- Advisor: Prof. David J. Perreault

Cambridge, MA

September 2001–May 2003

### Monterrey Institute of Technology

BACHELOR OF ARTS

- Graduated with honors

Mexico City, Mexico

September 1994–May 1998

## Employment History

### Stanford University

ASSOCIATE PROFESSOR

- Electrical Engineering Department

Stanford, CA

September 2020–Present

### Stanford University

ASSISTANT PROFESSOR

- Electrical Engineering Department

Stanford, CA

January 2014–August 2020

### University of Michigan

ASSISTANT PROFESSOR

- Electrical Engineering and Computer Science Department

Ann Arbor, MI

September 2011–December 2013

### General Electric, Global Research Center

LEAD POWER ELECTRONICS ENGINEER

Niskayuna, NY

September 2007–June 2011

### Thompson Consulting Inc.

ENGINEERING CONSULTANT

October 2006–August 2007

### Massachusetts Institute of Technology

POSTDOCTORAL ASSOCIATE

Cambridge, MA

May 2006–August 2007

### Comunicacion en Radio y Luz de Emergencia

CHIEF DESIGN ENGINEER

Mexico City, Mexico

January 1999–August 2000

## Professional Activities

### IEEE Power Electronics Society

ASSOCIATE EDITOR

- Transactions on Power Electronics

January 2015 → June 2021

## IEEE Power Electronics Society

ASSOCIATE EDITOR

2018 → June 2021

- Journal of Emerging and Selected Topics in Power Electronics

## IEEE Power Electronics Society

REVIEWER

→ present

- Applied Power Electronics Conference and exhibit
- Energy Conversion Congress and Exhibit
- Control and modeling in power Electronics

## IEEE Power Electronics Society

VICE CHAIR OF THE TECHNICAL COMMITTEE 1

2019 → 2021

- Power & Control Core Technologies

## IEEE Power Electronics Society

VICE CHAIR OF THE TECHNICAL PROGRAM COMMITTEE

→ 2020

- 12th Annual Energy Conversion Congress and Exposition (ECCE)

## IEEE Power Electronics Society

GENERAL CHAIR

→ 2017

- IEEE Control and Modeling of Power Electronics Workshop

# Awards and Honors

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## IEEE Applied Power Electronics Conference and Exposition (APEC).

Orlando, Fla

OUTSTANDING POSTER AWARD

2023

- “A Low-Ripple High-Frequency High-Voltage Power Supply for Ion Pumps” by Z. Ye; K. Surakitbovorn; S. Park; J. Rivas-Davila

## IEEE Transactions on Power Electronics

POWER ELECTRONICS PRIZE LETTER AWARD

2021

- “6.78-MHz Wireless Power Transfer With Self-Resonant Coils at 95% DC–DC Efficiency,” by L. Gu; G. Zulauf; A. Stein; P. A. Kyaw; T. Chen and J. M. R. Davila

## Workshop on Control and Modeling for Power Electronics

Cartagena, Colombia

BEST PAPER AWARD

2021

- “A High Frequency Resonant Gate Driver for SiC MOSFETs,” by Z. Ye; Z. Tong; L. Gu and J. Rivas-Davila

## Workshop on Control and Modeling for Power Electronics

Aalborg Denmark

BEST PAPER AWARD

2020

- “1 kW, Multi-MHz Wireless Charging for Electric Transportation,” by T. Phan; G. Zulauf; J. A. Fan and J. M. Rivas-Davila,

## NXP Homebrew RF design Challenge

THIRD PLACE AWARD

2019

- “A High Efficiency Switchmode RF Amplifier using a MRF101AN LDMOS Device for a CubeSat Plasma Thruster” by W. Braun, D. Tsifakis, C. Charles, R. Boswell, J. Rivas-Davila

## IEEE Applied Power Electronics Conference and Exposition (APEC).

Anaheim, CA

BEST PRESENTATION AWARD

2019

- “Empirical Circuit Model for Output Capacitance Losses in Silicon Carbide Power Devices” by Z. Tong, S. Park and J. Rivas-Davila

## International Power Electronics Conference

Niigata, Japan

BEST PAPER AWARD

2018

- “Design of a GaN-Based Wireless Power Transfer System at 13.56 MHz to Replace Conventional Wired Connection in a Vehicle” K. Surakitbovorn and J. Rivas-Davilla.

## Workshop on Control and Modeling for Power Electronics

Padova, Italy

BEST PAPER AWARD

2018

- “High-Frequency Bidirectional Resonant Converter for High Conversion Ratio and Variable Load Operation” by Lei Gu, Kawin Surakitbovorn, Grayson Zulauf, Sombuddha Chakraborty and Juan Rivas-Davila.

## IEEE Industry Applications Society

Tampa, FL

SECOND PRIZE WILL PORTNOY

2017

- “Inductance Cancellation in RF resonant power converters”

## Workshop on Control and Modeling for Power Electronics

Vancouver, Ca

BEST PAPER AWARD

2015

- “13.56 MHz high voltage multi-level resonant DC-DC converter,” by L. Raymond, W. Liang, L. Gu and J. R. Davila.

## CAREER Award

SF FACULTY EARLY CAREER DEVELOPMENT (CAREER) PROGRAM

2013

- Project: “Power Converters with embedded passive components” by Rivas J.

## IEEE Transactions on Power Electronics

SECOND PRIZE PAPER AWARD

2012

- High- Frequency Resonant SEPIC Converter With Wide Input and Output Voltage Ranges” by Hu, J.; Sagneri, A.D.; Rivas, J. M.; Han, Y.; Davis, S. M.; Monticelli, D. J. Perreault; IEEE Transactions on Power Electronics, vol.27, no.1, pp.189-200, Jan. 2012

## Power Electronics Specialists Conference

Rhodes, Greece

CONFERENCE PAPER AWARD

2008

- “A Very High Frequency dc-dc Converter Based on a Class  $\Phi 2$  Resonant Inverter” by Juan M. Rivas, Olivia Leitermann, Yehui Han and David J. Perreault.

## IEEE Transactions on Power Electronics

BEST PAPER AWARD

2007

- “Resistance Compression Networks for Radio- Frequency Power conversion” by Han Y, Leitermann O, Jackson D, Rivas J, Perreault D. IEEE Transactions on Power Electronics , Page(s): 41-53, Jan 2007.

# Publications

## REFEREED JOURNAL PUBLICATIONS

### Near spurious-free thickness shear mode lithium niobate resonator for piezoelectric power conversion

K NGUYEN, V CHULUKHADZE, E STOLT, W BRAUN, J SEGOVIA-FERNANDEZ, ...

, 2023

- IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control

### A Spurious-Free Piezoelectric Resonator Based 3.2 kW DC-DC Converter for EV On-Board Chargers

E STOLT, W BRAUN, K NGUYEN, V CHULUKHADZE, R LU, J RIVAS-DAVILA

, 2023

- IEEE Transactions on Power Electronics

### 1 kW MHz wideband class E power amplifier

J Xu, Z Tong, J RIVAS-DAVILA

3, 84-92, 2022

- IEEE Open Journal of Power Electronics

### A novel high-efficiency three-phase multilevel pv inverter with reduced dc-link capacitance

T CHEN, L GU, WJ DALLY, J RIVAS-DAVILA, J FOX

70 (5), 4751-4761, 2022

- IEEE Transactions on Industrial Electronics

### Frequency-Selective MHz Power Amplifier for Dielectric Barrier Discharge Plasma Generation

J Xu, K SURAKITBOVORN, B WANG, MA CAPPELLI, J RIVAS-DAVILA

3, 846-855, 2022

- IEEE Open Journal of Power Electronics

### Optimized resonators for piezoelectric power conversion

WD BRAUN, EA STOLT, L GU, J SEGOVIA-FERNANDEZ, S CHAKRABORTY, R LU, ...

2, 212-224, 2021

- IEEE Open Journal of Power Electronics

### Small-and large-signal dynamic output capacitance and energy loss in GaN-on-Si power HEMTs

J ZHUANG, G ZULAUF, J ROIG-GUITART, J PLUMMER, J RIVAS

68 (4), 1819-1826, 2021

- IEEE Transactions on Electron Devices

### Fixed-frequency control of piezoelectric resonator dc-dc converters for spurious mode avoidance

E STOLT, WD BRAUN, L GU, J SEGOVIA-FERNANDEZ, S CHAKRABORTY, R LU, ...

2, 582-590, 2021

- IEEE Open Journal of Power Electronics

## Wideband PPT Class Inverter Using Phase-Switched Impedance Modulation and Reactance Compensation

Z TONG, L GU, J RIVAS-DAVILA

69 (6), 5724-5734, 2021

- IEEE Transactions on Industrial Electronics

## Real-time Selective Harmonic Minimization Using a Hybrid Analog/Digital Computing Method

J POON, M SINHA, SV DHOPLE, J RIVAS-DAVILA

37 (5), 5078-5088, 2021

- IEEE Transactions on Power Electronics

## 6.78-MHz wireless power transfer with self-resonant coils at 95% DC-DC efficiency

L GU, G ZULAUF, A STEIN, PA KYAW, T CHEN, JMR DAVILA

36 (3), 2456-2460, 2020

- IEEE Transactions on Power Electronics

## Optimized design of multi-MHz frequency isolated auxiliary power supply for gate drivers in medium-voltage converters

OC SPRO, P LEFRANC, S PARK, JM RIVAS-DAVILA, D PEFTITSIS, OM MIDTGÅRD, ...

35 (9), 9494-9509, 2020

- IEEE Transactions on Power Electronics

## Push-Pull Class RF Power Amplifier

L GU, G ZULAUF, Z ZHANG, S CHAKRABORTY, J RIVAS-DAVILA

35 (10), 10515-10531, 2020

- IEEE Transactions on Power Electronics

## The impact of multi-MHz switching frequencies on dynamic on-resistance in GaN-on-Si HEMTs

G ZULAUF, M GUACCI, JM RIVAS-DAVILA, JW KOLAR

1, 210-215, 2020

- IEEE Open Journal of Power Electronics

## Lightweight high voltage generator for untethered electroadhesive perching of micro air vehicles

S PARK, DS DREW, S FOLLMER, J RIVAS-DAVILA

5 (3), 4485-4492, 2020

- IEEE Robotics and Automation Letters

## Origins of Soft-Switching Coss Losses in SiC Power MOSFETs and Diodes for Resonant Converter Applications

Z TONG, J ROIG-GUITART, T NEYER, JD PLUMMER, JM RIVAS-DAVILA

9 (4 ...), 2020

- IEEE Journal of Emerging and Selected Topics in Power Electronics

## Design and fabrication of three-dimensional printed air-core transformers for high-frequency power applications

Z TONG, WD BRAUN, JM RIVAS-DAVILA

35 (8), 8472-8489, 2020

- IEEE Transactions on Power Electronics

## Decentralized carrier phase shifting for optimal harmonic minimization in asymmetric parallel-connected inverters

J POON, B JOHNSON, SV DHOPLE, J RIVAS-DAVILA

36 (5), 5915-5925, 2020

- IEEE Transactions on Power Electronics

## Modular ON/OFF and phase-shifting for high-speed radio frequency power modulation

K SURAKITBOVORN, JM RIVAS-DAVILA

1, 393-406, 2020

- IEEE Open Journal of Power Electronics

## A simple method to combine the output power from multiple class-E power amplifiers

K SURAKITBOVORN, JM RIVAS-DAVILA

10 (2 ...), 2020

- IEEE Journal of Emerging and Selected Topics in Power Electronics

## A hybrid Cockcroft-Walton/Dickson multiplier for high voltage generation

S PARK, J YANG, J RIVAS-DAVILA

35 (3), 2714-2723, 2019

- IEEE Transactions on Power Electronics

## **Cascode GaN/SiC: A wide-bandgap heterogenous power device for high-frequency applications**

J XU, L GU, Z YE, S KARGARRAZI, JM RIVAS-DAVILA

35 (6), 6340-6349, 2019

- IEEE Transactions on Power Electronics

## **Single-turn air-core coils for high-frequency inductive wireless power transfer**

G ZULAUF, JM RIVAS-DAVILA

35 (3), 2917-2932, 2019

- IEEE Transactions on Power Electronics

## **On the techniques to utilize SiC power devices in high-and very high-frequency power converters**

Z TONG, L GU, Z YE, K SURAKITBOVORN, J RIVAS-DAVILA

34 (12), 12181-12192, 2019

- IEEE Transactions on Power Electronics

## **Output capacitance loss characterization of silicon carbide Schottky diodes**

Z TONG, G ZULAUF, JL XU, JD PLUMMER, J RIVAS-DAVILA

7 (2), 865-878, 2019

- IEEE Journal of Emerging and Selected Topics in Power Electronics

## **A multiresonant gate driver for high-frequency resonant converters**

L GU, Z TONG, W LIANG, J RIVAS-DAVILA

67 (2), 1405-1414, 2019

- IEEE Transactions on Industrial Electronics

## **Effect of class 2 ceramic capacitor variations on switched-capacitor and resonant switched-capacitor converters**

J XU, L GU, J RIVAS-DAVILA

8 (3 ...), 2019

- IEEE Journal of Emerging and Selected Topics in Power Electronics

## **On the optimization of a class-E power amplifier with GaN HEMTs at megahertz operation**

KN SURAKITBOVORN, JM RIVAS-DAVILA

35 (4), 4009-4023, 2019

- IEEE Transactions on Power Electronics

## **High-frequency bidirectional resonant converter for high conversion ratio and variable load operation**

L GU, K SURAKITBOVORN, G ZULAUF, S CHAKRABORTY, J RIVAS-DAVILA

8 (3 ...), 2019

- IEEE Journal of Emerging and Selected Topics in Power Electronics

## **A method to eliminate discrete inductors in a class-E inverter used in wireless power transfer applications**

K SURAKITBOVORN, JM RIVAS-DAVILA

8 (3 ...), 2019

- IEEE Journal of Emerging and Selected Topics in Power Electronics

## **COSS Losses in 600 V GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters**

G ZULAUF, S PARK, W LIANG, KN SURAKITBOVORN, J RIVAS-DAVILA

33 (12), 10748-10763, 2018

- IEEE Transactions on Power Electronics

## **Active power device selection in high-and very-high-frequency power converters**

G ZULAUF, Z TONG, JD PLUMMER, JM RIVAS-DAVILA

34 (7), 6818-6833, 2018

- IEEE Transactions on Power Electronics

## **Measurements for Superjunction MOSFETs: Limitations and Opportunities**

GD ZULAUF, J ROIG-GUITART, JD PLUMMER, JM RIVAS-DAVILA

66 (1), 578-584, 2018

- IEEE Transactions on Electron Devices

## **A wide-input-range high-efficiency step-down power factor correction converter using a variable frequency multiplier technique**

L GU, W LIANG, M PRAGLIN, S CHAKRABORTY, J RIVAS-DAVILA

33 (11), 9399-9411, 2018

- IEEE Transactions on power electronics

## **Implementing an impedance compression network to compensate for misalignments in a wireless power transfer system**

J CHOI, J XU, R MAKHOUL, JMR DAVILA

34 (5), 4173-4184, 2018

- IEEE Transactions on Power Electronics

## Duty cycle and frequency modulations in class-e dc-dc converters for a wide range of input and output voltages

S PARK, J RIVAS-DAVILA

33 (12), 10524-10538, 2018

- IEEE Transactions on Power Electronics

## An integrated RF power delivery and plasma micro-thruster system for nano-satellites

W LIANG, C CHARLES, L RAYMOND, A STUCHBERY, K SURAKITBOVORN, L GU, ...

6, 115, 2018

- Frontiers in Physics

## High-frequency, high-power resonant inverter with eGaN FET for wireless power transfer

J CHOI, D TSUKIYAMA, Y TSURUDA, JMR DAVILA

33 (3), 1890-1896, 2017

- IEEE Transactions on Power Electronics

## Vacuum Testing of a Miniaturized Switch Mode Amplifier Powering an Electrothermal Plasma Micro-Thruster

C CHARLES, W LIANG, L RAYMOND, J RIVAS-DAVILA, RW BOSWELL

5, 2017

- Frontiers in Physics

## Design of a class-DE rectifier with shunt inductance and nonlinear capacitance for high-voltage conversion

S PARK, JM RIVAS

33 (3), 2282-2294, 2017

- IEEE Transactions on Power Electronics

## Low-mass RF power inverter for cubesat applications using 3-D printed inductors

W LIANG, L RAYMOND, M PRAGLIN, D BIGGS, F RIGHETTI, M CAPPELLI, ...

5 (2), 880-890, 2016

- IEEE Journal of Emerging and Selected Topics in Power Electronics

## 3-D-printed air-core inductors for high-frequency power converters

W LIANG, L RAYMOND, J RIVAS

31 (1), 52-64, 2015

- IEEE Transactions on Power Electronics

## 13.56 MHz high density DC-DC converter with PCB inductors

W LIANG, J GLASER, J RIVAS

30 (8), 4291-4301, 2014

- IEEE Transactions on Power Electronics

## A Very High Frequency DC-DC Converter Based on a Class $\Phi_{-2}$ Resonant Inverter

JM RIVAS, O LEITERMANN, Y HAN, DJ PERREAULT

26 (10), 2980-2992, 2011

- IEEE Transactions on Power Electronics

## High-frequency resonant SEPIC converter with wide input and output voltage ranges

J HU, AD SAGNERI, JM RIVAS, Y HAN, SM DAVIS, DJ PERREAULT

27 (1), 189-200, 2011

- IEEE Transactions on Power Electronics

## Very-high-frequency resonant boost converters

RCN PILAWA-PODGURSKI, AD SAGNERI, JM RIVAS, DI ANDERSON, DJ PERREAULT

24 (6), 1654-1665, 2009

- IEEE Transactions on Power Electronics

## Resistance compression networks for radio-frequency power conversion

Y HAN, O LEITERMANN, DA JACKSON, JM RIVAS, DJ PERREAULT

22 (1), 41-53, 2007

- IEEE Transactions on Power Electronics

## New architectures for radio-frequency DC-DC power conversion

JM RIVAS, RS WAHBY, JS SHAFRAN, DJ PERREAULT

21 (2), 380-393, 2006

- IEEE Transactions on Power Electronics

## Performance improvement of alternators with switched-mode rectifiers

J RIVAS, D PERREAULT, T KEIM

19 (3), 561-568, 2004

- IEEE Transactions on Energy Conversion

## REFEREED CONFERENCE/SYMPOSIA PROCEEDINGS

## **Spurious-Free Lithium Niobate Bulk Acoustic Resonator for Piezoelectric Power Conversion**

K NGUYEN, E STOLT, W BRAUN, V CHULUKHADZE, J SEGOVIA-FERNANDEZ, ...

- 2023 Joint Conference of the European Frequency and Time Forum and IEEE ...

## **Wideband Push-Pull Class E Amplifier for RF Power Delivery**

Z TONG, JM RIVAS-DAVILA

- 2023 IEEE 24th Workshop on Control and Modeling for Power Electronics ...

## **A Low-Ripple High-Frequency High-Voltage Power Supply for Ion Pumps**

Z YE, K SURAKITBOVORN, S PARK, J RIVAS-DAVILA

- 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), 2074-2079

## **Forward-zero cycle closed-loop control of piezoelectric resonator dc-dc converters**

EA STOLT, WD BRAUN, JM RIVAS-DAVILA

- 2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics ...

## **Analytical Circuit Model for COSS Losses in SiC Junction Termination Extensions**

J ZHUANG, Z TONG, J VICTORY, A BOLOTNIKOV, J ROIG, K JIA, J RIVAS-DAVILA

- 2022; International Exhibition and Conference for Power ...

## **1.7 kW 6.78 MHz wireless power transfer with air-core coils at 95.7% DC-DC efficiency**

L GU, J RIVAS-DAVILA

- 2021 IEEE Wireless Power Transfer Conference (WPTC), 1-4

## **Piezoelectric Resonator Second Harmonic Cancellation in Class $\Phi 2$ Inverters**

EA STOLT, WD BRAUN, CY DANIEL, JM RIVAS-DAVILA

- 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics ...

## **Class E power amplifier with piezoelectric resonator output branch**

C DANIEL, E STOLT, J RIVAS-DAVILA

- 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics ...

## **A High Frequency Resonant Gate Driver for SiC MOSFETs**

Z YE, Z TONG, L GU, J RIVAS-DAVILA

- 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics ...

## **Real-time selective harmonic minimization using hybrid analog/digital computing**

J POON, M SINHA, SV DHOPLE, J RIVAS-DAVILA

- 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), 1041-1046

## **Reverse Recovery Testing of Small-Signal Schottky Diodes**

WD BRAUN, EA STOLT, L GU, JM RIVAS-DAVILA

- 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 5611-5615

## **Inductorless soft switching dc-dc converter with an optimized piezoelectric resonator**

WD BRAUN, Z TONG, J RIVAS-DAVILA

- 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2272-2278

## **Design and Optimization of 6.78 MHz Wireless Power Transfer with Self-Resonant Coils**

L GU, G ZULAUF, A STEIN, PA KYAW, T CHEN, JM RIVAS-DAVILA

- 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics ...

## **A physical investigation of large-signal dynamic output capacitance and energy loss in GaN-on-Si power HEMTs at high-frequency applications**

J ZHUANG, G ZULAUF, J ROIG, JD PLUMMER, J RIVAS-DAVILA

- 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 189-194

## **Demonstration of GaN impact ionization avalanche transit-time (IMPATT) diode**

D JI, B ERCAN, J ZHUANG, L GU, J RIVAS-DAVILA, S CHOWDHURY

- 2020 Device Research Conference (DRC), 1-2

## **1 kW, Multi-MHz Wireless Charging for Electric Transportation**

T PHAN, G ZULAUF, JA FAN, JM RIVAS-DAVILA

- 2020 IEEE 21st Workshop on Control and Modeling for Power Electronics ...

## **Low-Ripple High-Voltage DC Generation Using a Serially Segmented Multiphase Voltage Multiplier**

S PARK, J RIVAS-DAVILA

- 2020 IEEE Energy Conversion Congress and Exposition (ECCE), 962-968

## **An Investigation into the Causes of COSS Losses in GaN-on-Si HEMTs**

J ZHUANG, G ZULAUF, J ROIG, JD PLUMMER, J RIVAS-DAVILA

- 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 1-7

## **Cascode GaN/SiC power device for MHz switching**

J XU, L GU, Z YE, S KARGARRAZI, J RIVAS-DAVILA

- 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2780-2785

## **Miniature high-voltage dc-dc power converters for space and micro-robotic applications**

S PARK, A GOLDIN, J RIVAS-DAVILA

- 2019 IEEE Energy Conversion Congress and Exposition (ECCE), 2007-2014

## **A compact 45 V-to-54 kV modular dc-dc converter**

S PARK, L GU, J RIVAS-DAVILA

- 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 1-7

## **3-D printed air-core toroidal transformer for high-frequency power conversion**

Z TONG, WD BRAUN, JM RIVAS-DAVILA

- 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 1-7

## **Multiphase GaN Class-D Resonant Amplifier for High-Intensity Focused Ultrasound**

L GU, Q STEDMAN, M RASMUSSEN, CN PAI, K BRENNER, B MA, AS ERGUN, ...

- 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 1-6

## **MRI compatible dc modulator for an envelope tracking transmitter**

WD BRAUN, L GU, G SCOTT, J RIVAS-DAVILA

- 2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL), 1-4

## **Empirical circuit model for output capacitance losses in silicon carbide power devices**

Z TONG, S PARK, J RIVAS-DAVILA

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## Presentations

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### DEPARTMENT SEMINARS

#### Universidad Autonoma de San Luis Potosi

“HIGH-FREQUENCY POWER CONVERSION WITH WIDE BANDGAP SEMICONDUCTORS”

Remote seminar

November 13 2020

#### University of Pennsylvania

“HIGH-FREQUENCY POWER CONVERSION WITH WIDE BANDGAP SEMICONDUCTORS”

Remote seminar

October 27 2020

## Chinese University of Hong Kong

“VERY HIGH FREQUENCY RESEARCH DIRECTIONS AND WIRELESS POWER TRANSFER”

Shenzhen, PRC

September 12, 2018

## ETH, Zurich, Switzerland

“VERY HIGH FREQUENCY POWER ELECTRONICS: RESEARCH DIRECTIONS AND NEW APPLICATIONS”

Zurich, Switzerland

October 23, 2017

## International Workshop on Power Electronics

“HIGH-FREQUENCY POWER CONVERTERS”

Kyoto, Japan

October 27, 2016

## Massachusetts Institute of Technology

“POWER ELECTRONICS AT THE SUPER-LAB”

Cambridge, MA

June 16, 2016

## UCLA

“POWER ELECTRONICS AT THE SUPER-LAB”

Los Angeles, CA

March 28, 2016

## PELS chapter at UC Berkeley

“POWER ELECTRONICS AT THE SUPER-LAB”

Berkeley, CA

November 4, 2015

## Stanford University’s Energy and Environment Affiliates Program

“REVOLUTIONIZING POWER ELECTRONICS WITH VERY HIGH FREQUENCY POWER CONVERSION”

Stanford, CA

January 14, 2014

## Center for Integrated Circuits and Systems at MIT

“CIRCUIT DESIGN FOR VHF POWER CONVERSION”

Cambridge, MA

November 9, 2006

## INVITED PLENARY TALKS AND DISTINGUISHED LECTURES

### China Power Supply Society Conference

“DESIGN CONSIDERATIONS OF RADIO FREQUENCY POWER CONVERTERS”

Shenzhen, China

November 1, 2019

### International Conference on Silicon Carbide and Related Materials

“DRIVING METHODS FOR SIC DEVICES AT HIGH-FREQUENCIES”

Kyoto, Japan

September 29, 2019

### High VOLT Interactive by Texas Instruments

“HIGH-VOLTAGE LOW-CURRENT PORTABLE DC-DC CONVERTERS”

San Jose, CA

October 10, 2018

### Panasonic Corporation

“HIGH-FREQUENCY POWER CONVERTERS”

Kyoto, Japan

October 28, 2016

### SFBAC PELS Chapter

“THE TRIALS & TRIBULATIONS OF EVALUATING GAN AND SIC SWITCHING DEVICES”

Santa Clara, CA

September 29, 2016

### Energy Efficient TV Technologies organized by Ozyegin University

“POWER ELECTRONICS FOR ENERGY EFFICIENT TV’S”

Antalya, Turkey

August 25, 2014

### IEEE I-THERM

“REVOLUTIONIZING POWER ELECTRONICS WITH VERY HIGH FREQUENCY POWER CONVERSION”

Orlando, FL

May 28, 2014