$$\Delta V_{GS} = V_{step,peak} \cdot \frac{C_{gd2}}{C_{gs1} + C_{gs2} + C_{gd2}} \tag{20.31}$$

and the change in output current is given by

$$\Delta I_o = \frac{\beta_2}{2}(\Delta V_{GS} + V_{GS} - V_{THN})^2 - \frac{\beta_2}{2}(V_{GS} - V_{THN})^2 = \frac{\beta_2}{2}\Delta V_{GS}^2 + g_{m2}\Delta V_{GS} \tag{20.32}$$

The rate at which V_{GS} decays back to its DC value is determined by the time constant, τ. However, the effective resistance needed to charge or discharge the node that defines V_{GS} is dependent on the direction of the pulse generator. If a negative-going pulse is applied to the current mirror, then the effective resistance is simply R. However, if a positive-going pulse is applied to the mirror, then the effective resistance that discharges the change in gate-source voltage is now $1/g_{m1}$ such that

$$\tau = \frac{1}{g_{m1}} \cdot (C_{gs1} + C_{gs2} + C_{gd2}) \tag{20.33}$$

The rate at which the output current decays back to its DC value is approximated by

$$\tau_o \approx 2\tau \tag{20.34}$$

Example 20.7

Determine the peak current deviation and the time it takes the output current to return to its steady-state value for the simple current mirror given in Ex. 20.1 using the test circuit given in Fig. 20.11. Assume the step transitions from 0 to 2.5 V. Compare the hand calculations with PSPICE.

We know that $I_{D1} = I_{D2} = I_o = 10$ μA, $L_1 = L_2 = 5$ μm, and $W_1 = W_2 = 15$ μm. Therefore,

$$C_{gs1} = \tfrac{2}{3}C'_{ox}W_1L_1 = 40 \text{ fF}$$

$$C_{gs2} = \tfrac{2}{3}C'_{ox}W_2L_2 = 40 \text{ fF}$$

$$C_{gd2} = CGDO \cdot W_2 = 5.7 \text{ fF}$$

$$\beta_1 = \frac{KP \cdot W_1}{L_1} = 150 \frac{\mu A}{V^2}$$

$$\beta_2 = 150 \frac{\mu A}{V^2}$$

$$g_{m1} = \sqrt{2\beta_1 I_{D1}} = 55 \frac{\mu A}{V}$$

$$g_{m2} = 55 \frac{\mu A}{V}$$

The change in gate-source voltage is given by

$$\Delta V_{GS} = 2.5 \cdot \frac{5.7}{40 + 40 + 5.7} \approx 0.18 \text{ V}$$

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and the change in the output current, using Eq. (20.32), is given by

$$\Delta I_o = 75 \times 10^{-6}(0.18)^2 + 55 \times 10^{-6}(0.18) = 12\ \mu\text{A}\ !$$

The time constant for V_{GS} decay using Eqs. (20.33) and (20.34), is given by

$$\tau = \frac{1}{55 \times 10^{-6}} \cdot (40 + 40 + 5.7) \times 10^{-15} \approx 1.5\ \text{ns}$$

and the output current time constant is

$$\tau_o = 3\ \text{ns}$$

The PSPICE simulations are shown in Fig. 20.12. The hand calculations are very close to the simulation results. Note the simulation problems encountered with the output current. Putting a series resistor between the pulse source and the current source helps to "slow" things down enough to eliminate these problems. Of course, the results are affected because the resistor acts to increase the pulse risetime applied to the current source. ■

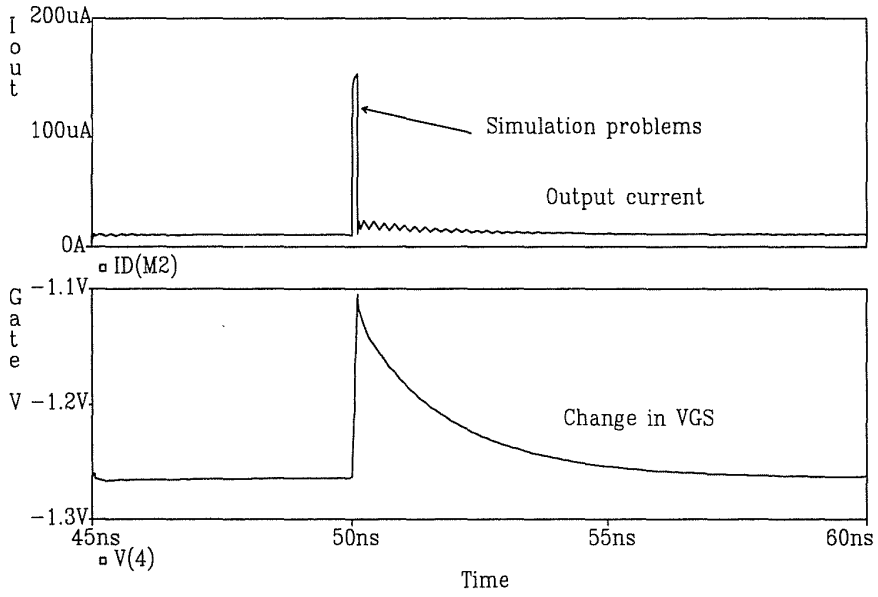


Figure 20.12 Simulated pulse response of the current mirror in Ex. 20.1.

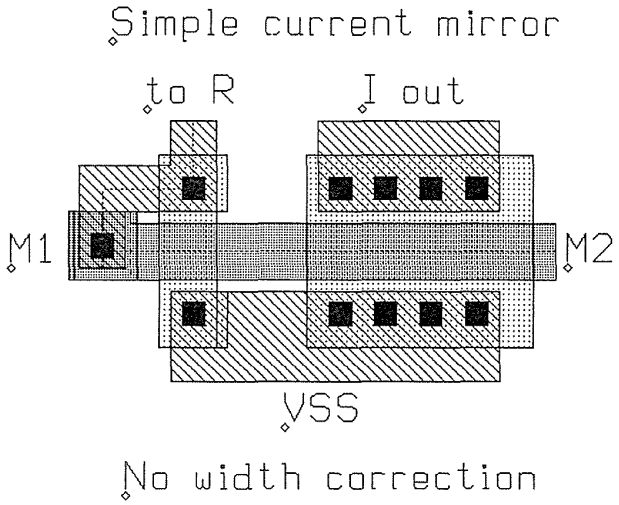
Poor transient response of a current mirror can severely limit the performance of a circuit. In some cases, such as the current sources discussed later in the chapter that use negative feedback, the current source can actually become unstable and oscillate.

20.1.5 Layout of the Simple Current Mirror

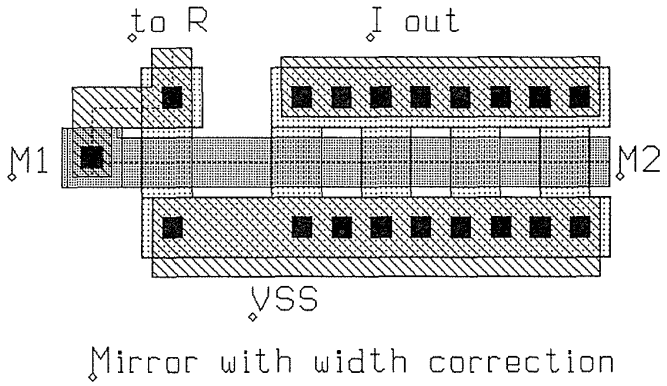
When laying out the current mirror, the lateral diffusion and the oxide encroachment on the length and width of the MOSFET must be taken into consideration. The lateral

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diffusion, *DL,* given in the BSIM model, and the oxide encroachment, *DW,* in the BSIM model will cause errors in the ratio $\frac{W_2L_1}{W_1L_2}$. If the requirement that $L_{1drawn} = L_{2drawn}$ is imposed, then the ratio $\frac{L_1}{L_2} = \frac{L_{1drawn}-DL}{L_{2drawn}-DL}$ is unity. Since the widths of the devices determine the relative currents in the mirror, the widths cannot be equal. Figure 20.13a shows a current mirror layout without width compensation. The width ratio, $\frac{W_2}{W_1}$, can be written



(a)



(b)

Figure 20.13 Layout of a MOSFET mirror to eliminate oxide encroachment effects.

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as $\frac{W_{2drawn}-DW}{W_{1drawn}-DW}$, which is clearly not an integer if the drawn widths are not equal. Figure 20.13b shows how to layout a current mirror to avoid these problems. The layout of M2 is basically four MOSFETs in parallel. This can be specified in SPICE by adding M = X after the MOSFET statement in the netlist, where X is the number of MOSFETs. The lines in the netlist may look similar to

```
M1    1 1 0 0      CMOSNB     L=5u W=5u
M2    2 1 0 0      CMOSNB     L=5u W=5u M=4
```

20.1.6 Matching in MOSFET Mirrors

Many analog applications are quite susceptible to errors due to layout. In circuits in which devices need to be matched, layout becomes a very critical factor. For example, in the basic current mirror shown in Fig. 20.1, first-order process errors can cause the mirrored current to be significantly different from the reference current. Process parameters such as gate-oxide thickness, lateral diffusion, oxide encroachment and, oxide charge density can drastically affect the performance of a device. Layout methods can be used to minimize the first-order effects of these parameter variations.

Threshold Voltage and Transconductance Parameter

In a given current mirror application, the values for the threshold voltages are critical in determining the overall accuracy of the mirror. Again examine the basic current mirror shown in Fig. 20.1. Since both devices have the same value for V_{GS} and assuming that β for both devices are equal, examine the effect of a mismatch in threshold voltages between the two devices [3]. If it is assumed that the threshold mismatched is distributed across both devices such that

$$V_{THN1} = V_{THN} - 0.5\Delta V_{THN} \tag{20.35}$$

$$V_{THN2} = V_{THN} + 0.5\Delta V_{THN} \tag{20.36}$$

where V_{THN} is the average value of V_{THN1} and V_{THN2} and ΔV_{THN} is the mismatch, then,

$$\frac{I_O}{I_{D1}} = \frac{\beta(V_{GS} - V_{THN} - 0.5\Delta V_{THN})^2}{\beta(V_{GS} - V_{THN} + 0.5\Delta V_{THN})^2} = \frac{\left[1 - \frac{\Delta V_{THN}}{2(V_{GS}-V_{THN})}\right]^2}{\left[1 + \frac{\Delta V_{THN}}{2(V_{GS}-V_{THN})}\right]^2} \tag{20.37}$$

If both expressions are squared and the higher order terms are ignored, then the first-order expression for the ratio of currents becomes

$$\frac{I_O}{I_{D1}} \approx 1 - \frac{2\Delta V_{THN}}{(V_{GS} - V_{THN})} \tag{20.38}$$

Equation (20.38) is quite revealing because it shows that as V_{GS} decreases, the difference in the mirrored currents increases due to threshold voltage mismatch. This is particularly critical for devices that are separated by relatively long distances, since the threshold voltage is quite susceptible to process gradients.

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The same analysis can be performed on the transconductance parameter, KP_n. If $KP_{n1} = KP_n - 0.5\Delta KP_n$ and $KP_{n2} = KP_n + 0.5\Delta KP_n$, where KP_n is the average of KP_{n1} and KP_{n2}, then assuming perfect matching on all other parameters, the difference in the currents becomes

$$\frac{I_O}{I_{D1}} \approx 1 + \frac{\Delta KP_n}{KP_n} \tag{20.39}$$

Drain to Source Voltage and Lambda

One aspect of current mirrors that is critical in generating accurate currents is the product of the drain to source voltage and lambda. In the basic current mirror, the ratio of the output current to the reference current is affected by both factors. For example, in Fig. 20.14, assume that the two devices are perfectly matched, except for their values of $\lambda = \lambda_c + \lambda_m$ and V_{DS}. If $V_{DS1} = 2$ V, $V_{DS2} = 4$ V, and $\lambda_1 = 0.05$, $\lambda_2 = 0.04$, then

$$\frac{I_o}{I_{D1}} = \frac{1 + (\lambda_c + \lambda_m)V_{DS2}}{1 + (\lambda_c + \lambda_m)V_{DS1}} = \frac{1 + (0.05)4}{1 + (0.04)2} = 1.11 \tag{20.40}$$

resulting in over 11 percent error. In some applications, it may be difficult to ensure that the drain to source voltages are the same for both devices. If possible, effort should be made to design the circuit so that the values of V_{DS} are equal.

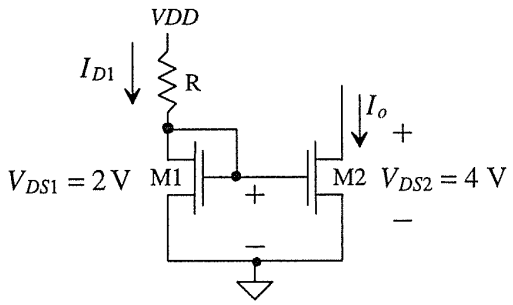


Figure 20.14 Basic current mirror with differing values of drain to source voltages.

Layout Techniques to Improve Matching

Most analog applications require that the length of the gate in an analog design be several times larger than the minimum drawn gate length, since the channel length modulation, λ_c , has less effect on larger devices than smaller ones. As a result, minimum-sized devices are rarely used in analog applications as is found in many digital circuits. However, the larger devices can result in larger parasitics if some layout issues are not considered. Figure 20.15a illustrates a basic MOSFET device with a large *W/L*. Since the width of the device is quite large, the diffusion resistance of the source and drain can be modeled as shown in Fig. 20.15b. The diffusion resistance can easily be reduced by simply adding as many contacts as possible along the width of both source and drain as seen in Fig. 20.15c. As was discussed in previous chapters, the

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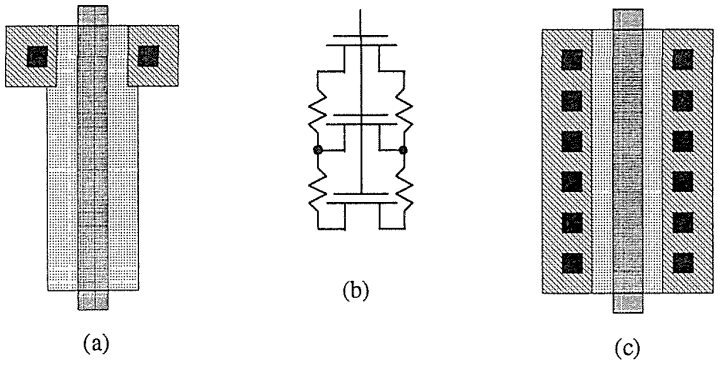


Figure 20.15 (a) Large device with a single contact and (b) its equivalent circuit. (c) Adding more contacts to reduce parasitic resistance.

increase in number of contacts results in lower resistance, more current capability, and a more distributed current load throughout the device. However, as the device size increases, another technique is used which distributes the parasitics (both resistive and capacitive) into smaller contributions.

Examine Fig. 20.16. Here, a single device with a large *W/L* is split into several parallel devices, each with one-fourth of the original *W*. One result of splitting the device into several parts is smaller overall parasitic capacitance associated with the reversed-biased diffusion substrate diode (the drain or source depletion capacitance to substrate). Since values of C_{db} and C_{sb} are proportional to *W*, the split device reduces these parasitics by a factor of $(n + 1)/2n$ where n is the number of parallel devices and is odd. If n is even, then the C_{sb} is reduced by one-half and C_{db} is reduced by $(n + 2)/2n$ [5].

Notice also, that Fig. 20.16 has dummy poly strips on both sides of the device. These strips are used to help minimize the effects of undercutting the poly on the outer

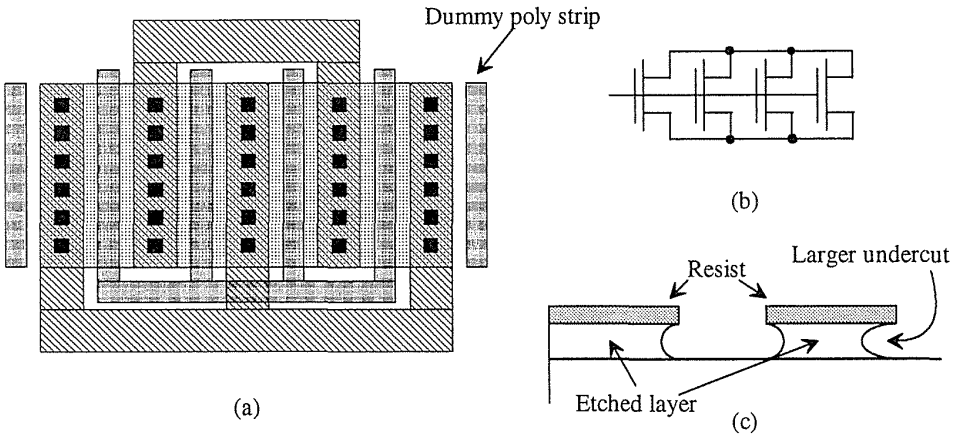


Figure 20.16 (a) A parallel device with dummy strips, (b) the equivalent circuit and (c) undercutting.

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edges after patterning. If the dummy strips had not been used, the poly would have been etched out more under the outermost gates, resulting in a mismatch between the four parallel devices.

When matching two devices, it is imperative that the two devices be as symmetrical as possible. Always orient the two devices in the same direction, unlike that illustrated in Fig. 20.17. Splitting the devices into parallel devices and interdigitizing them can distribute process gradients across both devices, thus improving matching. An example of this can be seen in Fig. 20.18. Note the use of dummy poly strips on this layout. A good exercise at this point is to lay out the mirror of Fig. 20.18 in a common-centroid arrangement (see Figs. 7.7 and 7.9).

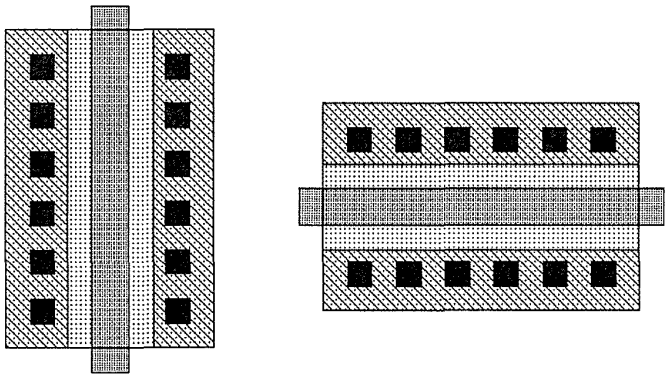
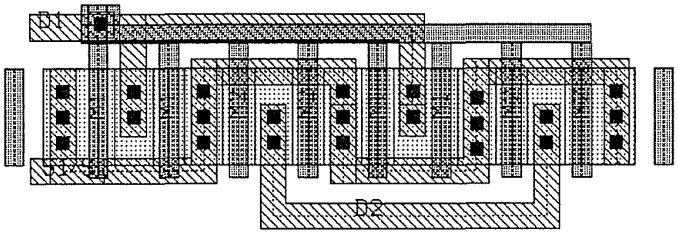
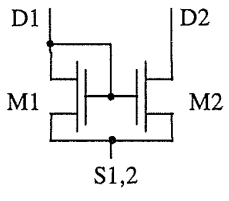


Figure 20.17 Devices with differing orientation.



(a)



(b)

Figure 20.18 (a) Layout of a simple current mirror using interdigitation and (b) equivalent circuit.

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20.2 Other Current Sources/Sinks

The basic current mirror can be improved significantly with negative feedback. There are two widely used current mirrors of this type, known as a Wilson current mirror and the regulated cascode. Both offer stable current values for wide voltage swings and enhanced output impedance.

The Wilson mirror [1, 3] can be seen in Fig. 20.19. Series sampling is used at the output to increase the output impedance and stabilize the drain current I_{D4}. The feedback mechanism is as follows. Suppose that I_{D1} is a constant and stable reference current and the voltage, V_o, increases, which causes I_{D4} to increase. I_{D2} increases by the same amount while I_{D1} stays constant. As a result, the voltage at node A decreases, thus decreasing V_{GS4} and stabilizing the current through M4.

The output impedance can be found by analyzing the circuit shown in Fig. 20.20. Note that since the gate of M1 is a DC voltage, $v_{gs1} = 0$ and the only contribution to the small-signal circuit from M1 is the resistance, r_o. Source absorption also converts the controlled current source of $g_{m3}v_{gs3}$ into its equivalent resistance of $1/g_{m3}$. From this circuit, we can generate the following equations,

$$v_{sb4} = v_{gs2} \tag{20.41}$$

$$v_{gs2} = i_t(r_{o3} \| \frac{1}{g_{m3}}) \tag{20.42}$$

$$v_{gs4} = -v_{gs2}[1 + g_{m2}(r_{o1} \| r_{o2})] = -i_t(r_{o3} \| \frac{1}{g_{m3}})[1 + g_{m2}(r_{o1} \| r_{o2})] \tag{20.43}$$

$$i_t = g_{m4}v_{gs4} - g_{mb4}v_{sb4} + \frac{v_t - v_{gs2}}{r_{o4}} \tag{20.44}$$

Plugging Eqs. (20.41 - 20.43) into Eq. (20.44), yields,

$$R_{out} = \frac{v_t}{i_t} = r_{o4}\left[1 + g_{m4}(r_{o3} \| \frac{1}{g_{m3}})(1 + g_{m2}(r_{o1} \| r_{o2}))\right] + g_{mb4}\left[(r_{o3} \| \frac{1}{g_{m3}}) + \frac{1}{r_{o4}}(r_{o3} \| \frac{1}{g_{m3}})\right] \tag{20.45}$$

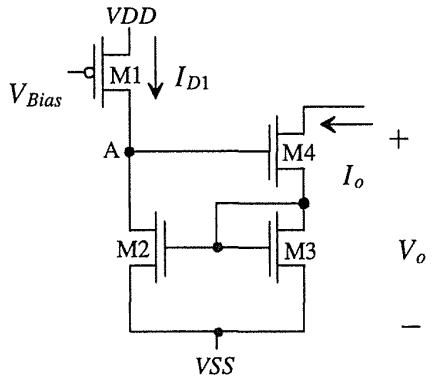


Figure 20.19 Wilson current mirror.

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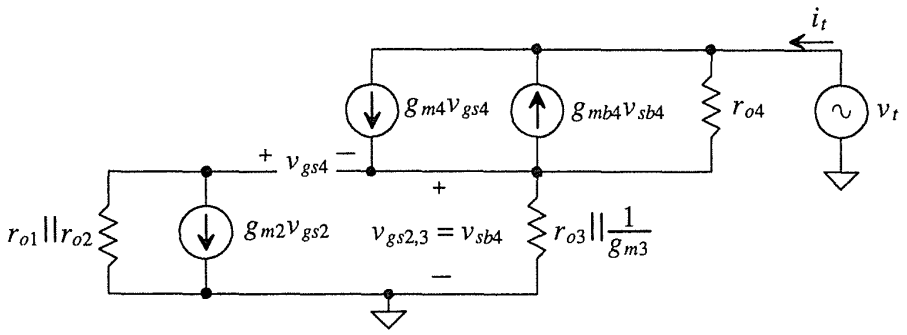


Figure 20.20 Small signal model of the Wilson current mirror used to determine output resistance.

which can be approximated as

$$R_{out} \approx r_{o4}\left[1 + g_{m2}(r_{o1}||r_{o2}) + g_{mb4}(\frac{1}{g_{m3}}) + \frac{1}{r_{o4}g_{m3}}\right] \tag{20.46}$$

If it is assumed that $r_{o3}||\frac{1}{g_{m3}} \approx \frac{1}{g_{m3}}$ and that $g_{m3} \approx g_{m4}$ then Eq. (20.46) can be further reduced. If the last two terms in the equation are assumed to be negligible and if $r_o = r_{o1} \approx r_{o2} \approx r_{o4}$ then R_{out} becomes,

$$R_{out} \approx r_o + g_{m2}\frac{r_o^2}{2} \tag{20.47}$$

It now becomes apparent that with the r_o^2 term in Eq. (20.47), the Wilson current mirror has an output impedance similar in size to the cascode current mirror.

One problem associated with this mirror is the minimum voltage required to keep I_o constant. As seen in Fig. 20.19, the minimum output voltage, V_o, necessary to keep both M3 and M4 in saturation is

$$V_o(\text{min}) = V_{GS3} + V_{DS4,sat} = V_{GS3} + V_{GS4} - V_{THN4} \tag{20.48}$$

which can be written in terms of the drain current, I_o, as

$$V_o(\text{min}) = \sqrt{\frac{2I_o}{\beta_3}} + V_{THN3} + \sqrt{\frac{2I_o}{\beta_4}} = 2\sqrt{\frac{2I_o}{\beta_{3,4}}} + V_{THN3} \tag{20.49}$$

if $\beta_3 = \beta_4$. As I_o increases, V_o(min) becomes larger by two times the square root of I_o.

Regulated Cascode Current Source/Sink

Another popular type of current mirror is the regulated cascode current mirror [6]. This current mirror also uses negative feedback to stabilize the output current and increase the output impedance to a higher degree than the Wilson mirror. Figure 20.21 illustrates a regulated cascode current mirror. The transistors M2 and M4 make up the negative feedback loop, which stabilizes I_o. If I_o were to increase, then, since a constant

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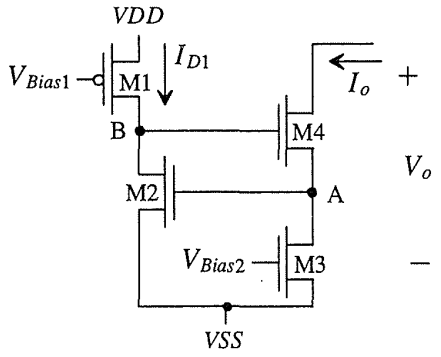


Figure 20.21 Regulated cascode current sink.

current flows through M3, the voltage on node A would rise, which in turn would increase the current through M2. Since the current through M1 is also a constant amount, the voltage at node B would decrease, thereby offsetting the increase in I_o by decreasing V_{GS3}.

This current mirror offers some significant advantages over any of the previously discussed current mirrors. First, the output impedance of this current mirror is significantly higher. The small-signal equivalent circuit is shown in Fig. 20.22. Since M1 and M3 are used in conjunction with DC bias sources, only their resistances, r_{o1} and r_{o3}, respectively, will appear in the small-signal model. However, both M2 and M4 contribute to the model. Notice that there is only a subtle difference in the small-signal model shown for Fig. 20.7 (cascode) and Fig. 20.20 (Wilson). The main difference is the fact that the device, M3, is no longer gate-drain connected, and so the controlled source, $g_{m3}v_{gs}$ is no longer source absorbed. The analysis for calculating the output resistance R_{out} is identical to that performed for the Wilson current mirror, except that the resistor that was represented as, $r_{o3}\|1/g_{m3}$ is now just r_{o3}. The resistance, R_{out} now becomes,

$$R_{out} = \frac{v_t}{i_t} = r_{o4}\left[1 + g_{m4}r_{o3}(1 + g_{m2}(r_{o1}\|r_{o2})) + g_{mb4}r_{o3} + \frac{r_{o3}}{r_{o4}})\right] \qquad (20.50)$$

which is dominated by the effective r_o^3 term composed of r_{o3}, r_{o4} and the parallel combination of r_{o1} and r_{o2}. R_{out} can be further reduced to

$$R_{out} = \frac{v_t}{i_t} \approx g_{m2}g_{m4}(r_{o1}\|r_{o2})r_{o3}r_{o4} \approx \frac{g_m^2 r_o^3}{2} \qquad (20.51)$$

if all the devices are matched. Assuming typical values of g_m = 20 μA/V and r_o=10MΩ, we see that the output of the regulated cascode is approximately 400 GΩ!

Another positive attribute of the regulated cascode is that its minimum value of V_o is lower than most of the other configurations. Since the negative feedback stabilizes

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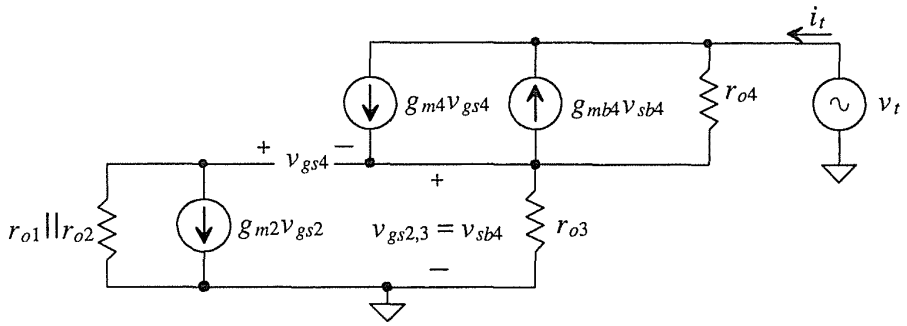


Figure 20.22 Small-signal model of the regulated cascode current mirror used to determine output resistance.

the voltages at nodes A and B, the output resistance is so large that M4 can become nonsaturated and still maintain a fairly constant current. The minimum output voltage is then determined by the fact that I_{D2} starts to change as node A starts to drop and M3 goes into nonsaturation. Therefore, the minimum output voltage is approximately a single V_{DS3}(sat).

One might question how the current sink shown in Fig. 20.21 can be used as a current mirror. With some modification, a true current mirror can be formed. Examine Fig. 20.23. With the addition of transistors M1, M5, M6, and M7, the input current, I_{D1} can be mirrored quite accurately through M3. If the current through M2 is identical to I_o, and $\beta_2 = \beta_3$, note that $V_{GS2} = V_{GS3} = V_{DS3}$ and that M3 is effectively always saturated since $V_{DS3} \geq V_{GS3} - V_{THN3}$. This condition fails, however, if V_{GS2} changes.

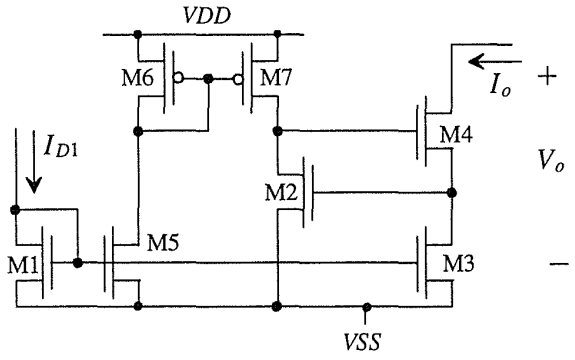


Figure 20.23 Regulated cascode current mirror.

Example 20.8

Estimate and determine, through SPICE simulation, the output resistance of the current sink shown in Fig. Ex20.8.

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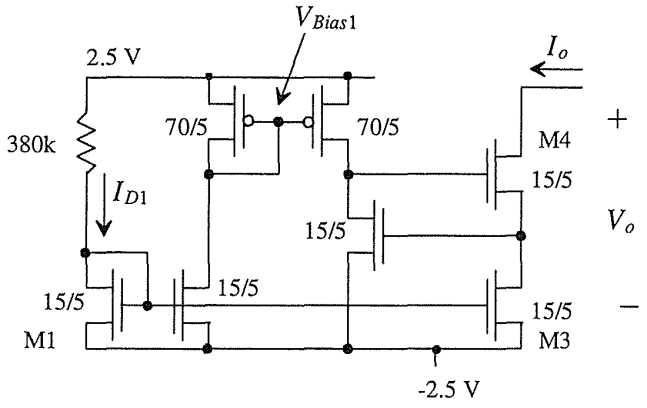


Figure Ex20.8

From Ex. 20.1 the current that flows in all MOSFETs in Fig. Ex20.8 is 10 μA and the output resistance is 1.67 MEG. The transconductance, g_m, from Ex. 20.4 is 55 μA/V. The output resistance can be estimated, using Eq. (20.51), as 6.9 GΩ, or approximately 50 times larger than the basic cascode of Ex. 20.4. Simulation results are shown in Fig. 20.24. The minimum voltage across the current source is approximately 1.3 V (0.3 V) with both M3 and M4 saturated (only M3 saturated). This corresponds to –1.2 V (–2.2 V) on the drain of M4. The current through the 380k resistor is slightly different from the output current when all MOSFETs are in the saturation region. This is the result of differing drain-source voltages between M1 and M3. The folded cascode current

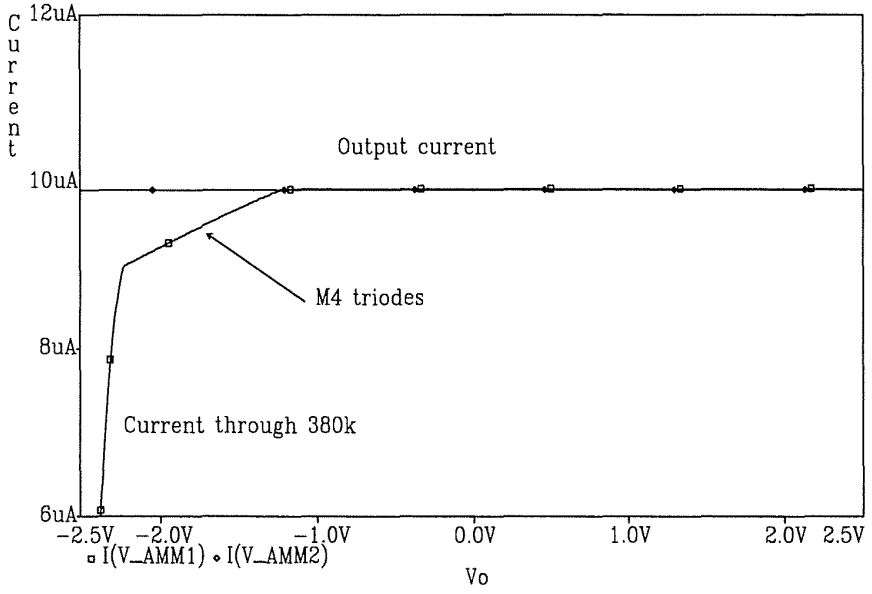


Figure 20.24 Simulation results for Ex. 20.8.

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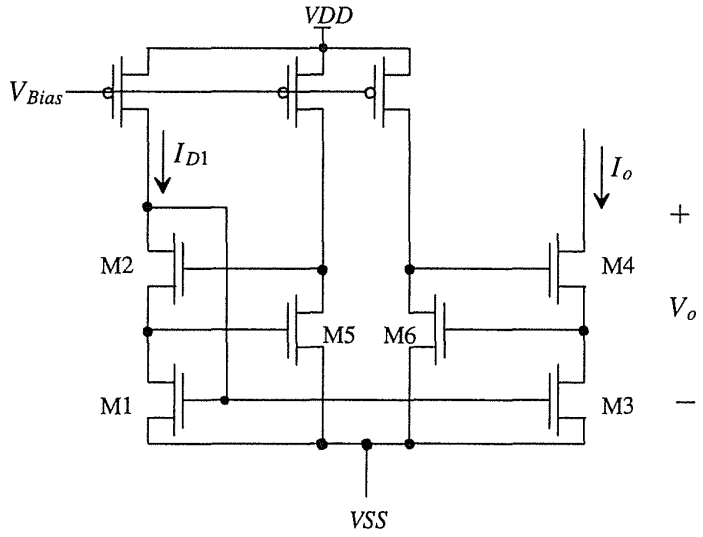


Figure 20.25 Improved regulated cascode current mirror.

mirror of Fig. 20.25 overcomes this mismatch by forcing the drain-source voltage of these two transistors equal. This configuration is preferred when matching is important, that is, matching between I_{D1} and I_o. ■

Wide-Swing, Low-Voltage Current Mirror

A wide-swing current mirror is shown in Fig. 20.26 [7, 8]. Wide swing here means that the minimum voltage across the current sink is $2\Delta V$ ($\Delta V = 0.37$ V when $V_{THN} = 0.83$ and

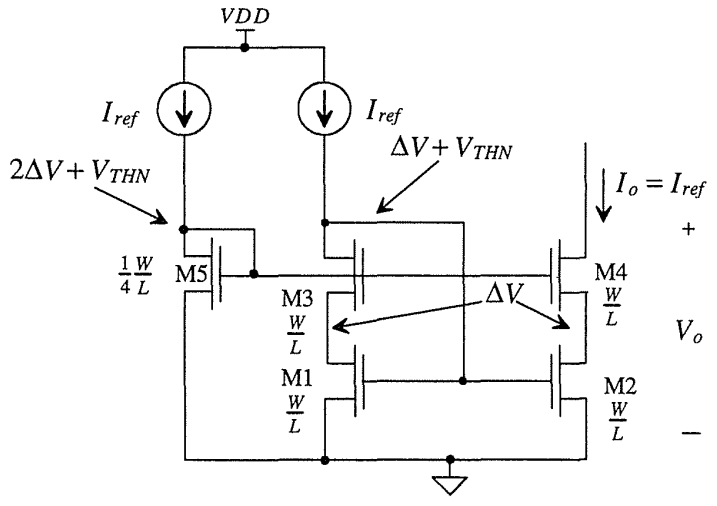


Figure 20.26 A high-swing cascode current mirror.

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V_{GS} = 1.2 V). This design is based on the wide-swing current mirror of Fig. 20.6 and is very useful in practical circuit design. MOSFETs M1 through M4 form a current mirror and therefore can be used in any of the applications discussed so far. We will see that current mirrors can be used as active loads for differential pairs and in voltage references. The minimum voltage across the wide-swing current source is one threshold voltage drop less than the regular cascode of Fig. 20.5, while the output resistance is the same, that is, $g_m \cdot r_o^2$. An example of a 10 μA current source based on the example values given in this chapter is shown in Fig. 20.27. MOSFETs M6 through M11 are added to supply current to M5. M5 is used to generate the bias voltage on the gates of M3 and M4 for wide-swing operation. Figure 20.28 shows the simulation results for the circuit of Fig. 20.27 when the output of the current source is swept from –2.5 to 2.5 V. This figure should be compared to Fig. Ex20.4.

Note that the body effect has been neglected in this analysis. This will cause V_{GS3} and V_{GS4} to be larger than predicted by $\Delta V + V_{THN}$. The current sink functions properly because $V_{DS,sat}$ (of M1 and M2) is smaller than predicted by $V_{GS} - V_{THN}$ (see Ch. 5). In several practical situations, for example, using this mirror in a folded-cascode op-amp, the size of M5 must be made smaller (perhaps (1/5)·*W*/*L*).

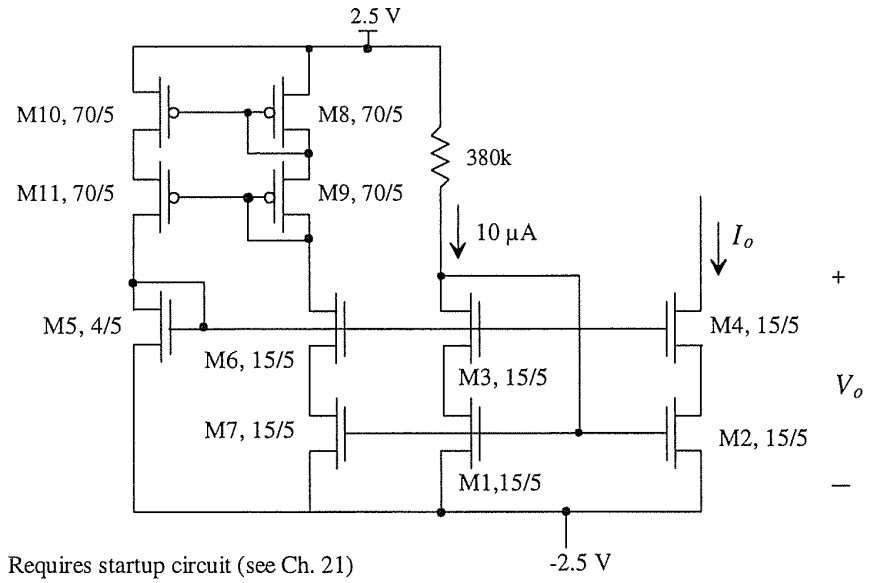


Figure 20.27 A 10 μA wide-swing current sink.

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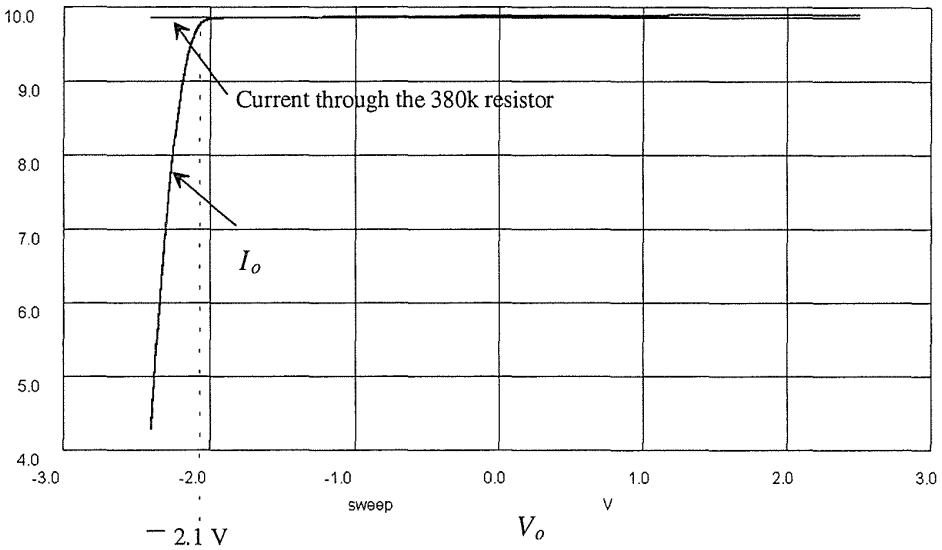


Figure 20.28 Simulation results for the current mirror of Fig. 20.27.

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PROBLEMS

Unless otherwise stated, use CN20 parameters, $VDD = 5$ V and $VSS = 0$ V.

20.1 Repeat Ex. 1 using a current of 1 μA and a V_{GS} of 1 V.

20.2 Design a circuit to bias the MOSFET in Fig. P20.2 so that its drain current is 5-μA. Estimate the minimum voltage across M1 if it is to remain in saturation.

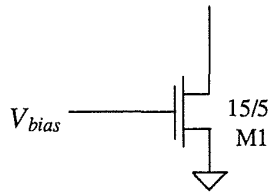


Figure P20.2

20.3 Determine the current that flows in M3 (Fig. P20.3). Neglect oxide encroachment and the finite output resistance of the M3.

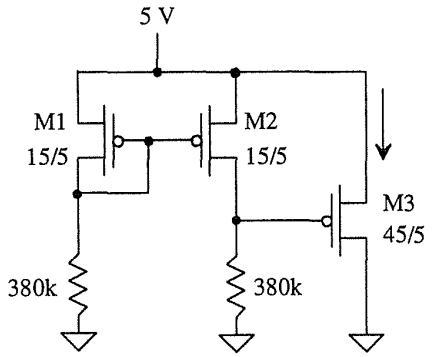


Figure P20.3

20.4 Determine the currents that flow in Fig. Ex20.3 if the size of M2 is increased to 30/5. Again, neglect oxide encroachment. Does V_{GS2} of V_{SG3} change? Why?

20.5 Determine the AC current that flows in v_t in Fig. P20.5. Assume $\lambda = 0.06$.

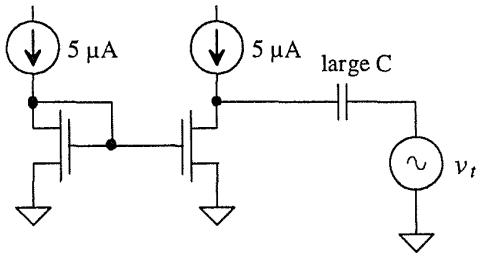


Figure P20.5

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20.6 Design a bias circuit so that the current that flows in M1 and M2 of Fig. P20.6 is 1 μA. What are the small-signal resistances looking into the drains of M2 and M1? What is the minimum voltage across M1 and M2 for operation in the saturation region?

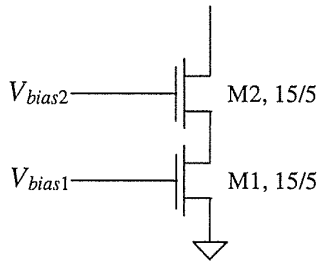


Figure P20.6

20.7 Using a small-signal analysis, verify that Eq. (20.11) is correct.

20.8 Using the circuit topology shown in Fig. P20.8 design current sources with output currents of 10 and 15 μA. Estimate, using hand calculations, the minimum voltage across the current sources and the output resistance. Verify the operation of your design with SPICE. What is the V_{SG} of the 100/5 MOSFETs that source 10 μA of current?

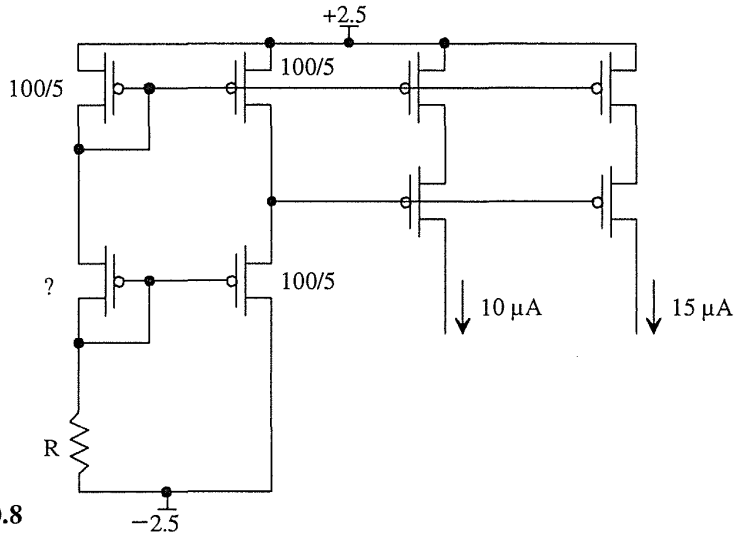


Figure P20.8

20.9 Repeat Ex. 20.5 for *VSS* changing from –2.4 to –2.6 V.

20.10 Verify that the temperature coefficient of the basic current mirror is given by Eq. (20.19).

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20.11 Verify that the temperature coefficient of the transconductance parameter is given by

$$\frac{1}{KP(T)} \cdot \frac{\partial KP(T)}{\partial T} = \frac{-1.5}{T}$$

20.12 In order to reduce the power dissipation in current mirrors one might be tempted to design a circuit with a small diode, connected MOSFET as shown in Fig. P20.12. The problem with this design is that changes on the drain of M2 can have a large effect on the gate voltage of M1/M2, ultimately being limited by the gate-source capacitance of M2. Using SPICE simulations, show how the output current is affected by an abrupt change across M2 of 1 V and –1 V.

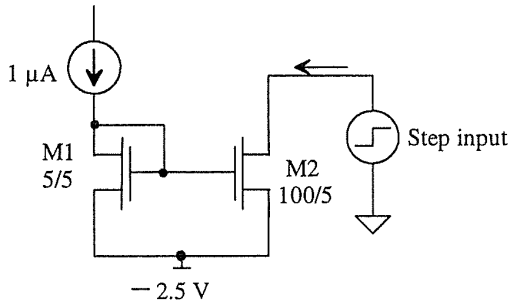


Figure P20.12

20.13 Lay out the current mirror shown in Fig. P20.13, avoiding oxide encroachment.

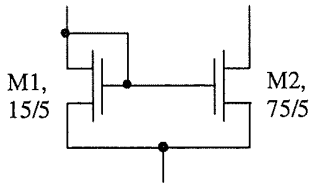


Figure P20.13

20.14 Suppose that a threshold voltage difference of 10 mV exists between the two MOSFETs used in a current mirror made using equal-size MOSFETs. How would you expect the difference in the drain currents to change with the MOSFET V_{GS}? Is matching between the currents better or worse with large V_{GS}? What happens to the minimum voltage across the current mirror if V_{GS} is increased?

20.15 Using the Wilson current mirror shown in Fig. P20.15, and the CN20 process, design a mirror in which $I_o = 150$ μA with $I_{REF} = 50$ μA for $VDD = 5$ *V*, $VSS = 0$ *V*. Verify your design with SPICE.

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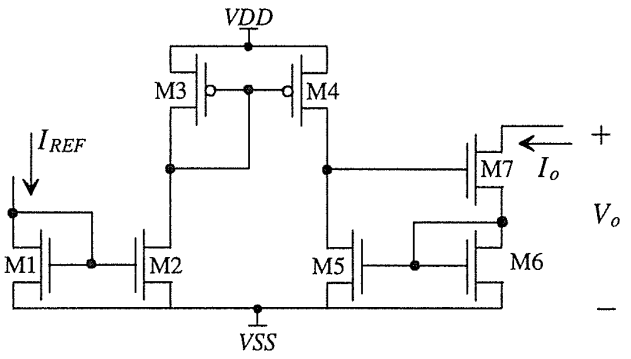


Figure P20.15

20.16 A Wilson current mirror (Fig. P20.15) is designed with $VDD = 5V$, $VSS = 0V$, $I_{REF} = 10\ \mu A$ and all devices sized 10 μ/10μ.

a. Calculate the value of the small-signal output resistance of the Wilson current mirror.

b. Verify part (a) with SPICE.

c. Calculate the minimum output voltage, V_o(min).

d. Construct a plot showing I_o versus V_o(min) for I_o varying from 5 μA to 50 μA in 5 μA increments.

e. Use SPICE to generate I_o versus V_o curves. How does this compare to the plot generated in part (d)?

f. Lay out the devices M4 through M7, assuming that each device is 40/5 using an interditigated layout technique to match devices M5 and M6. Use parallel devices for M4 and M7.

20.17 Repeat Problem 20.16, parts (a-e), for a cascode current mirror made using 15/5 devices.

20.18 Design a regulated cascode current sink of 1 μA. Estimate the output resistance of the current sink. Using SPICE similar to Fig. 20.24, show the output current change with voltage across the current sink.

20.19 The basic idea used in the regulated cascode current sink is shown in Fig. P20.19. What is the output resistance of this configuration? Show that if the gain A is $g_m(r_o/2)$, then the output resistance of the configuration reduces to that given by Eq. (20.51).

20.20 With respect to the wide-swing current mirror shown in Fig. 20.26, show that, neglecting the body effect, the drains of M1 and M2 are ΔV (the excess gate voltage) when M5 is one-fourth the size of the other MOSFETs.

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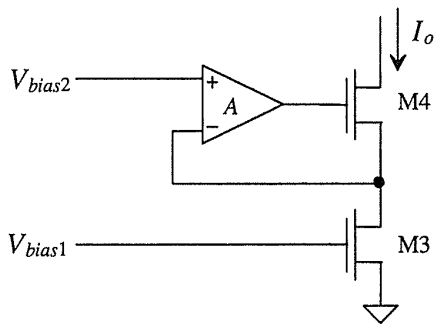


Figure P20.19

20.21 The basic current mirror finds extensive use as a load in differential amplifiers. Consider the schematic of the modified current mirror shown in Fig. P20.21. This configuration is termed a wide-band configuration since the addition of the source follower helps improve the ability of M1 to drive the large-input capacitance of M2. Estimate the small-signal resistance to ground at both nodes A and B. If a resistor is used to connect node A to *VDD*, write an equation relating the drain currents of M1 and M2 to the resistor value.

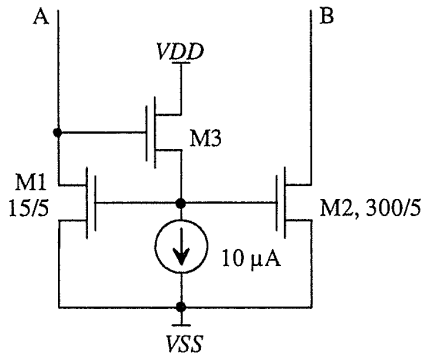


Figure P20.21

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Chapter

21

References

This chapter discusses voltage and current references, and in general how we can use voltage references to bias the current sources and sinks discussed in the last chapter. A good reference is insensitive to temperature, process, and supply voltage variations.

21.1 Voltage Dividers

In CMOS integrated circuit design, we can derive reference voltages from the power supplies using the resistor and the MOSFET. Figure 21.1 shows the basic idea. The voltage divider formed with two resistors has the advantage of simplicity, temperature insensitivity (as was shown in Ch. 7), and process insensitivity, that is, changes in the sheet resistance have no effect on the voltage division. The main problem with this circuit is that in order to reduce the power dissipation (i.e., the current through the resistors), the resistors must be made large. Since large resistors require a large area on the die, this voltage divider may not be practical in many cases. The voltage divider formed between the resistor and the MOSFET can be recognized as the same circuit we used for a bias in the current mirror. The final circuit, a voltage divider between an n- and p-MOSFET, has the advantage that the layout can be small. In the following two subsections, we analyze the behavior of these last two voltage dividers.

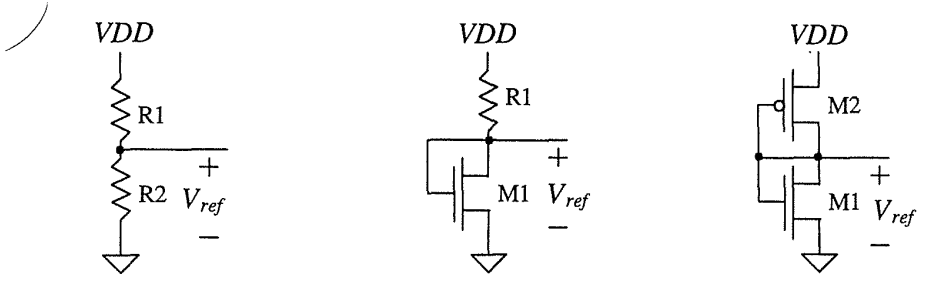


Figure 21.1 Implementation of voltage dividers in CMOS.

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21.1.1 The Resistor-MOSFET Divider

The reference voltage used in the resistor-MOSFET divider is equal to the V_{GS} of the MOSFET. We know for this circuit that

$$I_D = \frac{VDD - V_{ref}}{R} = \frac{\beta_1}{2}(V_{ref} - V_{THN})^2 \tag{21.1}$$

or

$$V_{ref} = V_{THN} + \sqrt{\frac{2I_D}{\beta_1}} = V_{THN} + \sqrt{\frac{2(VDD - V_{ref})}{R \cdot \beta_1}} \tag{21.2}$$

The sensitivity of the reference voltage to VDD when $VDD >> V_{ref}$ is

$$S_{VDD}^{V_{ref}} = \frac{VDD}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial VDD} \approx \frac{1}{V_{THN} \cdot \sqrt{\frac{2R\beta_1}{VDD}} + 2} \tag{21.3}$$

The temperature coefficient of the resistor-MOSFET voltage divider is given by

$$TC(V_{ref}) = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T} \tag{21.4}$$

or with the help of Eq. (20.25) with $VSS = 0$

$$TC(V_{ref}) = \frac{1}{V_{ref}}\left[V_{THN} \cdot TCV_{TH} - \frac{1}{2}\sqrt{\frac{2L_1}{W_1} \cdot \frac{VDD}{R \cdot KP(T)}} \cdot \left[\frac{1}{R}\frac{\partial R}{\partial T} - \frac{1.5}{T}\right]\right] \tag{21.5}$$

A modification of the basic MOSFET divider is shown in Fig. 21.2. The reference voltage in this circuit is given by

$$V_{ref} = V_{GS}\left(\frac{R_1}{R_2} + 1\right) \tag{21.6}$$

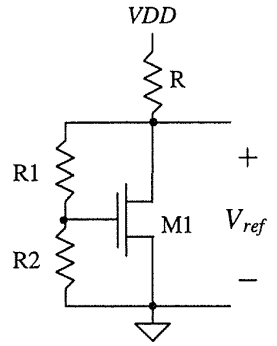


Figure 21.2 Modification of the resistor-MOSFET voltage divider.

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21.1.2 The MOSFET-Only Voltage Divider

The MOSFET-only voltage divider shown in Fig. 21.3 generates a reference voltage equal to the voltage on the gates of the MOSFETs with respect to ground. Since $I_{D1} = I_{D2}$ we can write

$$\frac{\beta_1}{2}(V_{ref} - VSS - V_{THN})^2 = \frac{\beta_2}{2}(VDD - V_{ref} - V_{THP})^2 \tag{21.7}$$

or the reference voltage is given by

$$V_{ref} = \frac{VDD - V_{THP} + \sqrt{\frac{\beta_1}{\beta_2}}(VSS + V_{THN})}{\sqrt{\frac{\beta_1}{\beta_2}} + 1} \tag{21.8}$$

or knowing the reference voltage and the power supply voltages gives

$$\frac{\beta_1}{\beta_2} = \left[\frac{VDD - V_{ref} - V_{THP}}{V_{ref} - VSS - V_{THN}}\right]^2 \tag{21.9}$$

The sensitivity of V_{ref} with respect to VDD is given by

$$S_{VDD}^{V_{ref}} = \frac{VDD}{VDD - V_{THP} + \sqrt{\frac{\beta_1}{\beta_2}}(VSS + V_{THN})} \tag{21.10}$$

The temperature dependence of the MOSFET-only voltage divider, using Eq. (21.8), and assuming the temperature dependence of the ratio of the transconductance parameters, $\frac{\beta_1}{\beta_2}$, is negligible, is given by

$$TC(V_{ref}) = \frac{1}{V_{ref}} \cdot \frac{\partial V_{ref}}{\partial T} = \frac{1}{V_{ref}} \cdot \frac{1}{\sqrt{\frac{\beta_1}{\beta_2}} + 1} \cdot \left[\frac{\partial(-V_{THP})}{\partial T} + \sqrt{\frac{\beta_1}{\beta_2}}\frac{\partial V_{THN}}{\partial T}\right] \tag{21.11}$$

From Ch. 9 we know that

$$\frac{\partial V_{THN}}{\partial T} = TCV_{THN} \cdot V_{THN} = (-.003°C^{-1})(0.8\ V) = -2.4\ \frac{\text{mV}}{°\text{C}} \tag{21.12}$$

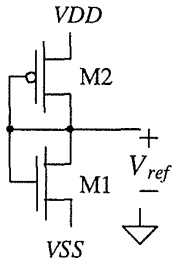


Figure 21.3 MOSFET-only voltage divider used between VDD and VSS.

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and

$$-\frac{\partial V_{THP}}{\partial T} = -TCV_{TH} \cdot V_{THP} = -(-0.003°C^{-1})(0.9V) = 2.7\frac{mV}{°C} \qquad (21.13)$$

To achieve $TC(V_{ref}) = 0$ requires

$$-\frac{\partial V_{THP}}{\partial T} = -\sqrt{\frac{\beta_1}{\beta_2}} \cdot \frac{\partial V_{THN}}{\partial T} \Rightarrow 2.7\frac{mV}{°C} = \sqrt{\frac{\beta_1}{\beta_2}} \cdot 2.4\frac{mV}{°C} \qquad (21.14)$$

or

$$\sqrt{\frac{\beta_1}{\beta_2}} = 1.125 \qquad (21.15)$$

Zero temperature coefficient, to a first order, can be met by satisfying this equation. However, this ratio is most often set by the desired V_{ref}.

Example 21.1

Design a 3 V reference using the MOSFET-only voltage divider assuming *VDD* = +5 V and *VSS* = 0 V. Determine the temperature coefficient of the reference. Verify your hand calculations with SPICE. Compare the power dissipation when $L_1 = L_2 = 5$ μm with $L_1 = L_2 = 50$ μm.

Since we know that $V_{THN} = 0.8$ V and $V_{THP} = 0.9$ V, we can determine the ratio of β_1 to β_2 using Eq. (21.9):

$$\frac{\beta_1}{\beta_2} = \left[\frac{5-3-0.9}{3-0-0.8}\right]^2 = 0.25$$

Setting $L_1 = L_2 = W_1 = 5$ μm gives

$$\frac{KP_n W_1 L_2}{KP_P W_2 L_1} = \frac{\left(50\times10^{-6}\frac{A}{V^2}\right)5\mu 5\mu}{\left(17\times10^{-6}\frac{A}{V^2}\right)W_2 5\mu} = 0.25$$

or solving gives $W_2 = 60$ μm. The temperature coefficient is given by

$$TC(V_{ref}) = \frac{1}{3} \cdot \frac{1}{\sqrt{\frac{50\cdot5}{17\cdot60}}+1} \cdot \left[.0027 + \sqrt{\frac{50\cdot5}{17\cdot60}}(-0.0024)\right] = 337 \text{ ppm/°C}$$

The PSPICE simulation results are shown in Fig. 21.4. The temperature coefficient of this reference calculated from the figure is approximately 400 ppm/°C. The small difference between PSPICE and our hand calculations can be attributed to the temperature coefficients of the threshold voltages. The drain current when $L = 5$ μm is 125 μA, and the power dissipated by the circuit is 600 μW. When $L = 50$ μm, the drain current drops to 12.5 μA and the power dissipation becomes 60 μW. Reducing the power dissipation requires that we

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use larger devices. Using the threshold voltage drop of an additional device in series with the two of Fig. 21.3 will help with this problem. ■

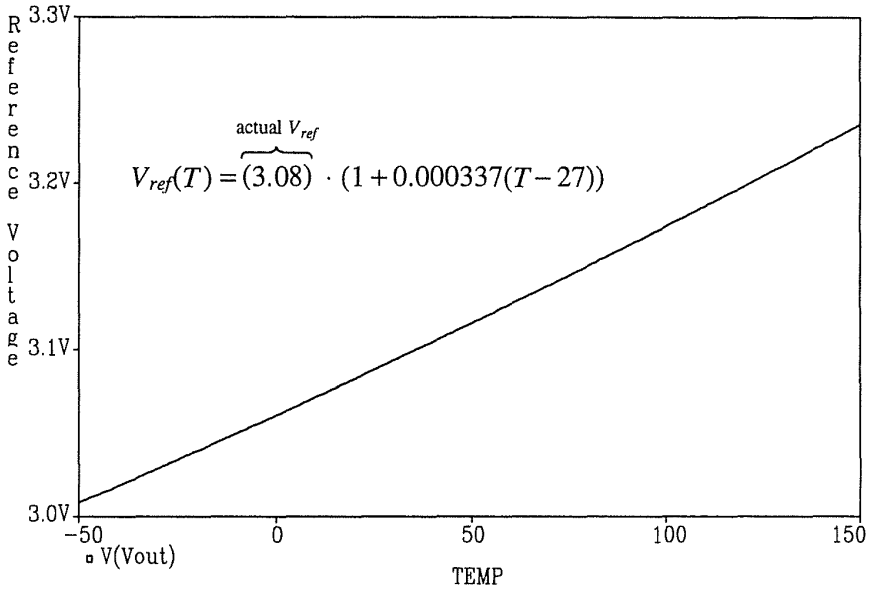


Figure 21.4 Temperature characteristics of the voltage divider designed in Ex. 21.1.

A three-MOSFET voltage divider is shown in Fig. 21.5. Two reference voltages are available in this configuration. The two p-channel MOSFETs are laid out in their own wells to avoid body effect. Designing voltage dividers in modern processes requires the designer to look at the maximum gate-source voltage. Generally, the maximum potential across the gate oxide should be below 7 MV/cm, or 0.7 V/10 Å. Circuits designed with a process that has an oxide thickness of 100 Å should limit the

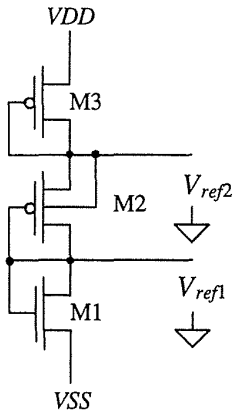


Figure 21.5 Three-MOSFET voltage divider.

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oxide-source or oxide-substrate potential to 7 V or less. Reliability in many cases can be related to the maximum voltage or stress across the gate oxide.

The design of this type of divider consists of determining the reference voltages needed, selecting a drain current through the MOSFETs, and solving for the size of the devices.

Example 21.2

Design a 2 V and a 3.5 V voltage reference using the three-MOSFET voltage divider of Fig. 21.5. Assume that VDD = +5 V, VSS = 0 V, the drain current of the MOSFETs is 10 μA, and that $L_1 = L_2 = L_3$ = 20 μm. Compare the area required for layout of this design with the area used in Ex. 21.1 if L = 50 μm.

Since V_{GS1} = 2 V, we can solve for W_1 knowing

$$10\ \mu\text{A} = \frac{KP_n}{2} \cdot \frac{W_1}{20\mu\text{m}}(2-0.8)^2 \text{ which gives } W_1 \approx 5\ \mu\text{m}$$

The width of M2 is determined in a similar manner, since V_{SG2} = 1.5 V, using

$$10\ \mu\text{A} = \frac{KP_p}{2} \cdot \frac{W_2}{20\mu\text{m}}(1.5-0.9)^2 \Rightarrow W_2 = 65\ \mu\text{m}$$

The width of M3, with V_{SG3} = 1.5 V, is also 65 μm.

The area of the reference designed in Ex. 21.1 (using the case when L = 50 μm and drain current is 12.5 μA) can be estimated by

$$A_{Ex21.1} = L_1W_1 + L_2W_2 = 3250\ \mu\text{m}^2$$

while the area needed in this example is 2700 μm². In addition, the power dissipation is slightly lower, 50 μW, when we use a second MOSFET. ■

A useful application of the dual-reference voltage divider is shown in Fig. 21.6a. Here the reference is used to bias the cascode current source. The current through the reference, that is, the current through M1, M2, and M3, is selected as equal to or a multiple of the desired current through M4 and M5. Following the discussion of the last chapter, if it is desirable to design a 10 μA current source, we may set the current through M1 to 10 μA and the voltage across M1, V_{GS1} (= V_{GS4}), to 1.2 V. The current in M1 is mirrored in M4. The size of M2 can be set equal to the size of M1, while the size of M3 is selected to drop VDD – 2.4 V at the bias current. Sometimes the bias voltages generated by M1 and M2 are simply labeled "Bias" as shown in Fig. 21.6b. A complicated schematic can be simplified by not showing the bias MOSFETs.

The main drawback of using the references described in this section is that all, that is, the resistor-resistor, resistor-MOSFET, and MOSFET-only dividers are very sensitive to the power supply voltages and temperature. The remainder of this chapter discusses the means of designing voltage references and biasing current sources to reduce the sensitivity to temperature and the power supplies.

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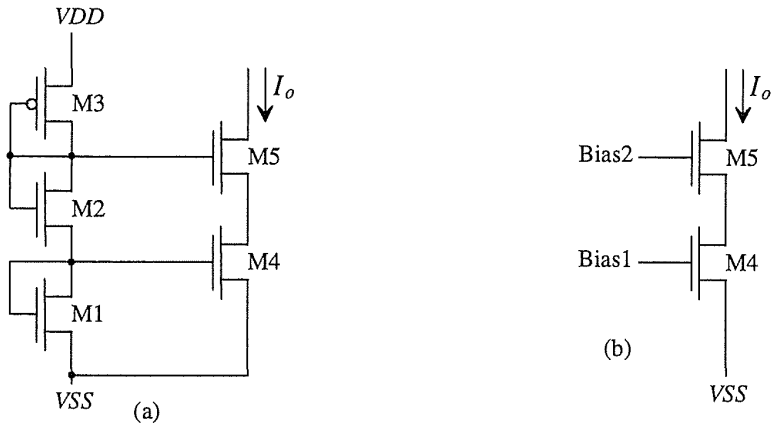


Figure 21.6 Use of the three-MOSFET voltage divider to bias the cascode current source: (a) full schematic and (b) simplified schematic.

21.2 Current Source Self-Biasing

The biasing methods presented so far for current sources have been dependent on the power supply voltages and temperature. Changes in *VDD* or *VSS* directly affect the currents in the circuit. In this section, we discuss three methods of biasing which reduce the effects of power supply variations and possibly temperature on currents present in a current source [1, 2].

21.2.1 Threshold Voltage Referenced Self-Biasing

Consider the biasing circuit shown in Fig. 21.7. MOSFETs M3 and M4 force the same current to flow through M1 and M2. The product of this current and the resistor R is equal to the gate-source voltage of M1 or, neglecting the output resistance of the MOSFETs and the body effect,

$$IR = V_{GS1} = V_{THN} + \sqrt{\frac{2I}{\beta_1}} \tag{21.16}$$

If β_1 is large, the current, I, is given by

$$I \approx \frac{V_{THN}}{R} \tag{21.17}$$

In practice, the second term in Eq. (21.16) is not negligible, and the current is given by

$$I = \frac{V_{GS1}}{R} \tag{21.18}$$

where practical values of V_{GS1} are 1.0 to 1.2 V. These equations predict that the current is independent of the power supply voltages. Indeed, if the output resistance of the MOSFET were infinite, this would be the case. However, the current is dependent, albeit much less than the previous methods discussed, on the supply voltages. Cascoding M3 and M4 helps to make the bias circuit behave more ideal. The accuracy

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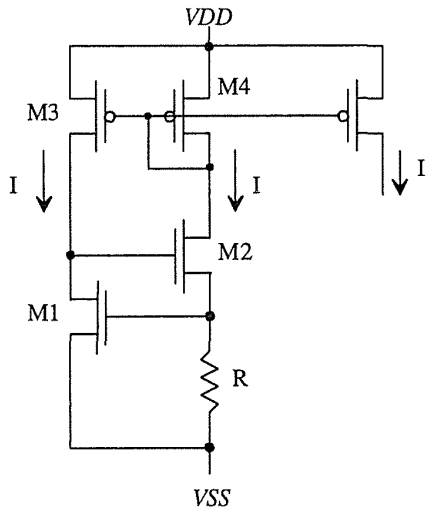


Figure 21.7 Threshold reference self-biasing circuit.

of the current, I, is limited by the threshold voltage accuracy, which may vary by 20 percent, and the n+ resistivity, value which can vary by 20 percent as well.

The temperature performance of the threshold bias circuit can be determined by considering Eq. (21.17). The temperature coefficient of the threshold voltage is (from Ch. 9) approximately –3,000 ppm/°C, while the temperature coefficient of an n+ resistor is (from Ch. 7) 2,000 ppm/°C. The threshold voltage decreases with increasing temperature, while the resistance, R, increases with increasing temperature. The result is a reference current with a large negative temperature coefficient.

The possibility that the current, I, may be zero exists in all self-biased circuits. (Consider what happens when the gates of M3 and M4 are at *VDD* and the gate of M2 is at *VSS*.) Figure 21.8a illustrates this graphically. Point A in this figure is the desired operating point, while point B corresponds to $I = 0$. Figure 21.8b shows the reference with a startup circuit used to avoid operation at point B. If the gate of M2 is at or near *VSS*, M5 turns on and pulls this node upward toward point B. Since the circuit is stable at either point A or B, the gate potential continues increasing until it reaches $2V_{GS}$. This causes M5 to turn off. Once the self-biasing circuit is operating at point B, the startup circuit does not affect the reference operation.

21.2.2 Diode Referenced Self-Biasing

Many biasing circuits use the parasitic pnp transistor formed by the p+ implant (the emitter), the n-well (the base), and the p-type substrate (collector) available in an n-well process in conjunction with the CMOS transistors to generate reference currents or voltages. The layout of the parasitic pnp transistor is shown in Fig. 21.9a with a cross-sectional view shown in Fig. 21.9b. The base of this parasitic transistor is tied to the substrate, which in turn is tied to *VSS*. The transistor is connected as a diode. This

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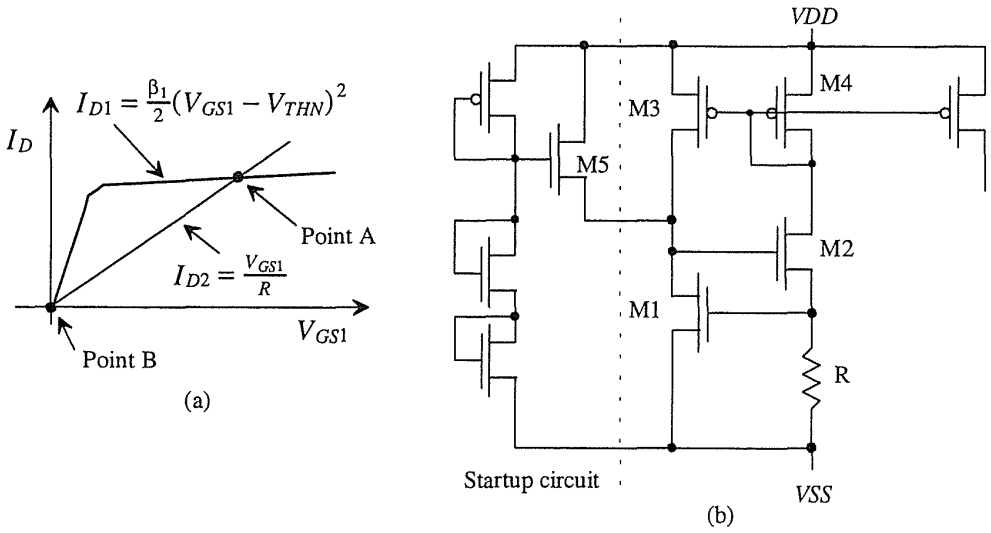


Figure 21.8 (a) Two possible operating points of self-biased circuit. (b) A startup circuit.

configuration reduces the effective resistance in series with the diode and the leakage to substrate.

The emitter size of the pnp is of importance in our applications. The minimum size allowable in the CN20 process is 6 μm square, or an area of 36 μm² (36×10^{-12} m²). Notice how the transistor in Fig. 21.9c is specified by the number "1" indicating minimum size. If we were to specify 8 for the size of the pnp transistor, this would correspond to an emitter area of 8·36 μm² or 288 μm².

It is important to simulate these parasitic transistors using SPICE. Since the base will be tied to the emitter, we can use a diode model statement to model the device. The current through a forward-biased diode is given by

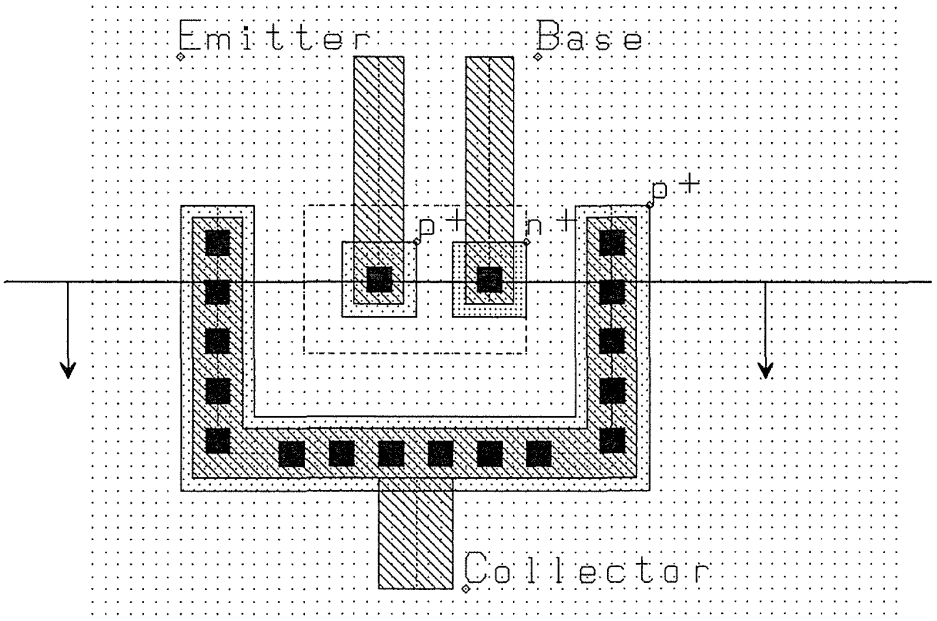
$$I_d = I_s \cdot e^{V_d/n \cdot V_T} \tag{21.19}$$

where V_d is the voltage across the diode and V_T is the thermal voltage KT/q or 26 mV at room temperature (see Ch. 2).

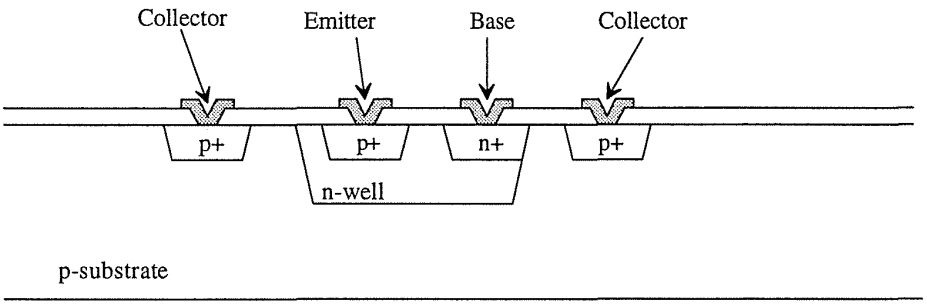
The first parameter of interest in Eq. (21.19) is the scale current, I_s. This current can be determined by the BSIM p-channel model parameter, *JS*, which characterizes the leakage from the p+ source or drain implant to well. For the minimum-size pnp with emitter size A_E the scale current is given by

$$I_s = JS \cdot AE = 10^{-8}\frac{\text{A}}{\text{m}^2} \cdot 36\ \mu\text{m}^2 = 360 \times 10^{-21}\ \text{A} \tag{21.20}$$

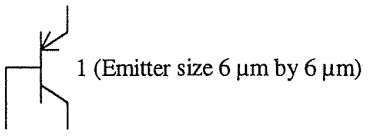
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(a)



(b)



(c)

Figure 21.9 Layout (a) and cross-sectional view (b) of the parasitic pnp transistor available in an n-well CMOS process and (c) schematic representation of a minimum-size parasitic pnp, that is, emitter area of 6 μm by 6μm.

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which is unrealistically low. The default value of the current density, *JS*, was used in the models (this was discussed in greater detail back in Ch. 14), meaning that the current density was not measured. A more realistic value for the saturation current may be

$$I_s = 10^{-15} \text{ A} \tag{21.21}$$

Without measuring the diode characteristics, we cannot determine I_s or n (the emission coefficient). If we assume that $n = 1$, we can use the following diode model for the pnp parasitic transistor and get reasonable agreement with experimental results

```
.MODEL          PNPDIOD     D( is=1E-15 n=1)
```

The specifications for the diode connected pnp transistors shown in Fig. 21.10 is

```
D1    1     5     PNPDIOD
D2    2     5     PNPDIOD     8
```

where the area factor, A (= 8), scales *IS* (i.e., the scale current for D2 is *A·IS*).

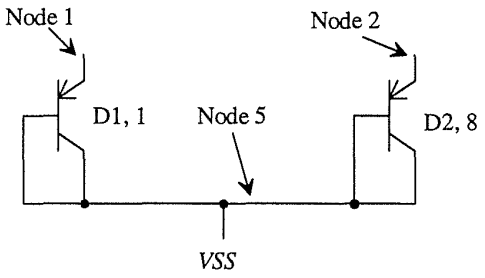


Figure 21.10 Diagram of two parasitic pnp transistors and their implementation in SPICE.

A diode-referenced self-biasing circuit is shown in Fig. 21.11. In this figure the cascode mirrors made with M1 through M8 force the same current, I, to flow through D1 and R. If the voltage across the diode is V_d, then the current I (= I_d) is given by

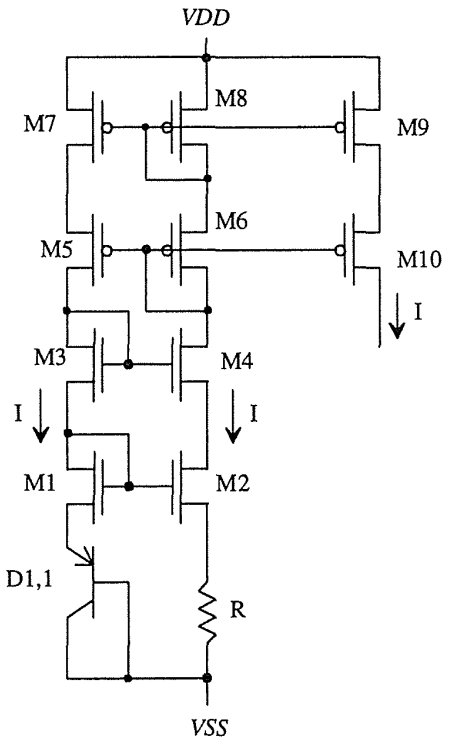
$$I = \frac{V_d}{R} = I_s e^{V_d/n \cdot V_T} \tag{21.22}$$

or solving for the resistor value given a current level I results in

$$R = \frac{n \cdot V_T}{I} \ln \frac{I}{I_s} \tag{21.23}$$

The main benefit of this circuit over the threshold referenced self-biasing circuit of the previous section is the better matching, from wafer to wafer and on the same die, of the diode voltage over the threshold voltage. The main problem with this biasing circuit, as with the threshold reference biasing scheme, is the temperature dependence. The temperature coefficient of the diode is approximately – 2 mV/°C or – 3,300 ppm/°C for a diode with 0.6 V forward bias. This, coupled with the positive temperature coefficient

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Requires startup circuit

Figure 21.11 Diode referenced self-biasing circuit.

of the n+ resistor of around 2,000 ppm/°C, causes the biasing circuit to have a negative temperature coefficient.

21.2.3 Thermal Voltage Referenced Self-Biasing

A thermal voltage, V_T, referenced self-biasing circuit is shown in Fig. 21.12. Again, the cascode connection of M1 through M8 forces the same current through D1 and D2. D2 has an emitter area K times larger than D1. In this configuration, the voltage across D1 must be equal to the voltage across D2 and R, or

$$V_{d1} = IR + V_{d2} \tag{21.24}$$

We know that

$$I_{d1} = I_s e^{V_{d1}/nV_T} \rightarrow V_{d1} = nV_T \cdot \ln \frac{I}{I_s} \tag{21.25}$$

and

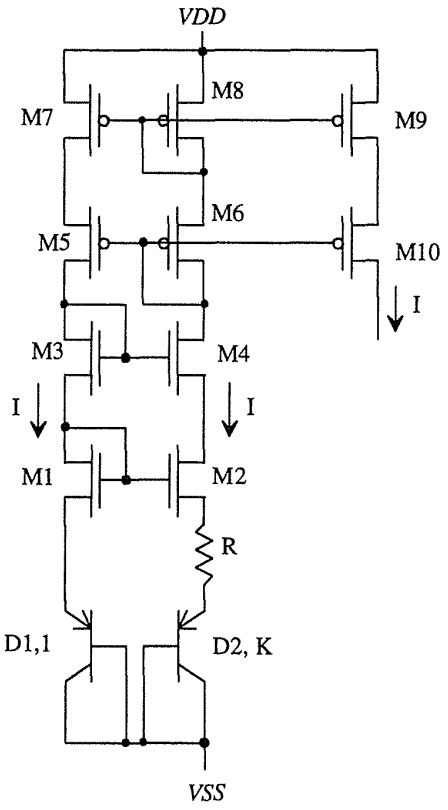
$$I_{d2} = K \cdot I_s e^{V_{d2}/nV_T} \rightarrow V_{d2} = nV_T \cdot \ln \frac{I}{K \cdot I_s} \tag{21.26}$$

Solving for R in terms of the reference current I results in

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$$R = \frac{nV_T \cdot \ln K}{I} \text{ or } I = \frac{nk \cdot \ln K}{qR} \cdot T \tag{21.27}$$

Notice that the current is proportional to the absolute temperature (PTAT). For $K = 8$ and $n = 1$, the voltage drop across R is only 50 mV. Mismatches in the gate-source voltages of M1 and M2 can result in large variations in I when using this scheme. Generally, M1 and M2 are made large for better matching of the IV characteristics. We should also keep in mind that the resistance value R may change up to 20 percent from wafer to wafer. If a precise current is needed, some sort of on-die tuning is required. More often, however, we care more about the relative current levels and temperature changes on a given die than about the die-to-die relative current levels.



Requires startup circuit

Figure 21.12 Thermal voltage referenced self-biasing circuit.

The main advantage of this current reference is in its temperature characteristics. The temperature dependence of the current I is given by

$$TC_I = \frac{1}{I}\frac{dI}{dT} = \frac{1}{V_T}\frac{\partial V_T}{\partial T} - \frac{1}{R} \cdot \frac{\partial R}{\partial T} \tag{21.28}$$

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The second term in this equation is simply the *TC* of the resistor, or approximately 2,000 ppm/°C. The first term in this equation is the *TC* of the thermal voltage, given by

$$TC_{V_T} = \frac{1}{V_T}\frac{\partial V_T}{\partial T} = \frac{q}{kT}\cdot\frac{k}{q} = +3,300 \text{ ppm/°C or ppm/°K} \tag{21.29}$$

(T in kelvin) where the change in the thermal voltage with temperature is given by

$$\frac{\partial V_T}{\partial T} = \frac{k}{q} = 0.085 \text{ mV/°C} \tag{21.30}$$

The temperature coefficient of this reference is on the order of +1,000 ppm/°C. The fact that both the temperature coefficient of the thermal voltage and the resistor are positive helps give better temperature characteristics than the diode or threshold voltage references. Practically, the problem with this reference is the matching of the MOSFETs and the susceptibility to externally coupled noise across *R*.

Note how the temperature coefficient is dependent on a given temperature; that is, we get different temperature coefficients at $T = 300$ °K and $T = 350$ °K. This is true with any temperature coefficient (i.e., *TC* is a function of temperature).

Example 21.3

Design a 10 μA current source using the thermal voltage self-biased reference. Simulate the temperature characteristics of the design.

Referring to Fig. 21.12, if we require that the current *I* is 10 μA and that the gate-source voltages are 1.2 V, then the size of the n-channel MOSFETs is 15/5 and the size of the p-channel MOSFETs is 70/5 (see Ex. 20.3). If the emitter area of the diode D2 is eight times larger than D1, then the resistor value is given by

$$R = \frac{26 \text{ mV}\cdot \ln 8}{10 \text{ μA}} = 5.4 \text{ kΩ}$$

The PSPICE simulation results are shown in Fig. 21.13. The output current is taken as the current through M9 and M10, each sized 70/5, in Fig. 21.12. The netlist is shown below. To aid in convergence of the DC sweep, we used the .NODESET command to set the high-impedance nodes, nodes 2 and 12, and the voltage at the top of the resistor to zero volts. The .NODESET line doesn't force the nodes to zero volts; it just starts the simulation with these initial guesses. Also, the .OPTIONS statement was used to loosen the tolerances and increase the DC and bias point iteration limit, ITL1, and the DC/bias point educated guess iteration limit, ITL2. Notice that the TC of the resistor is specified in the netlist as 2,000 ppm/°C. ■

```
*** Top Level Netlist ***
D1      7 3             pnpdiod
D2      8 3             pnpdiod         8
M1      4 4 7 3         CMOSNB          L=5u W=15u
M2      2 4 11 3        CMOSNB          L=5u W=15u
```

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```
M3      1 1 4 3          CMOSNB      L=5u W=15u
M4      9 1 2 3          CMOSNB      L=5u W=15u
M5      1 9 12 6         CMOSPB      L=5u W=70u
M6      9 9 10 6         CMOSPB      L=5u W=70u
M7      12 10 6 6        CMOSPB      L=5u W=70u
M8      10 10 6 6        CMOSPB      L=5u W=70u
M9      13 10 6 6        CMOSPB      L=5u W=70u
M10     14 9 13 6        CMOSPB      L=5u W=70u
R1      8 11    5.4k     TC1=0.002
VDD     6 0     DC 2.5
Vout    14 0    DC 0
VSS     3 0     DC -2.5
.NODESET V(8)=0 V(2)=0 V(12)=0
***** Spice models and macro models *****
.MODEL CMOSNB NMOS LEVEL=4
+...BSIM
.MODEL PNPDIOD D
+IS=1E-15 n=1
.MODEL CMOSPB PMOS LEVEL=4
+ ...BSIM
.OPTION RELTOL=0.01 ABSTOL=1n VNTOL=1m ITL1=100 ITL2=100
.probe
.DC Vout -1 1 .01    temp -25 75 25
.end
```

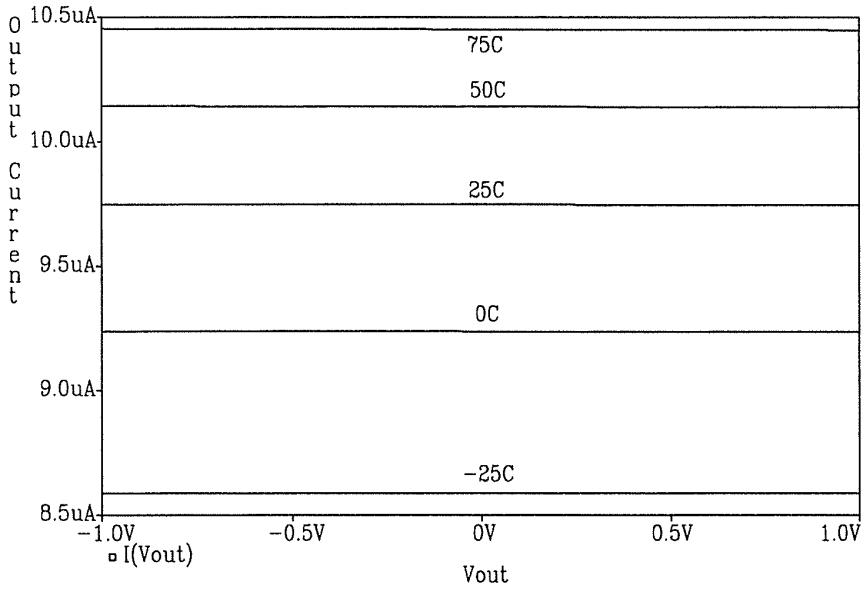


Figure 21.13 Temperature characteristics of the thermal referenced self-biasing circuit of

21.3 Bandgap Voltage References

Bandgap voltage references combine the positive *TC* of the thermal voltage with the negative *TC* of the diode forward voltage (the bandgap energy, E_g, of silicon decreases

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with increasing temperature; refer to Ch. 9) in a circuit to achieve a voltage reference with a zero *TC*. Once we have a temperature-independent voltage reference, it is a simple matter, with the use of an op-amp, to generate multiples of the reference.

21.3.1 Bandgap Referenced Biasing

The circuit shown in Fig. 21.14 is an example of a bandgap reference. The diode D3 is the same size as D2, while the resistor in series with D3 is L times larger than the resistor in series with D2. The current I in the figure is given by Eq. (21.27), or

$$I = \frac{nV_T \cdot \ln K}{R} \tag{21.31}$$

The reference output voltage with respect to *VSS* is given by

$$V_{ref} = I \cdot L \cdot R + V_{d3} \tag{21.32}$$

or

$$V_{ref} = (L \cdot n \cdot \ln K)V_T + V_{d3} \tag{21.33}$$

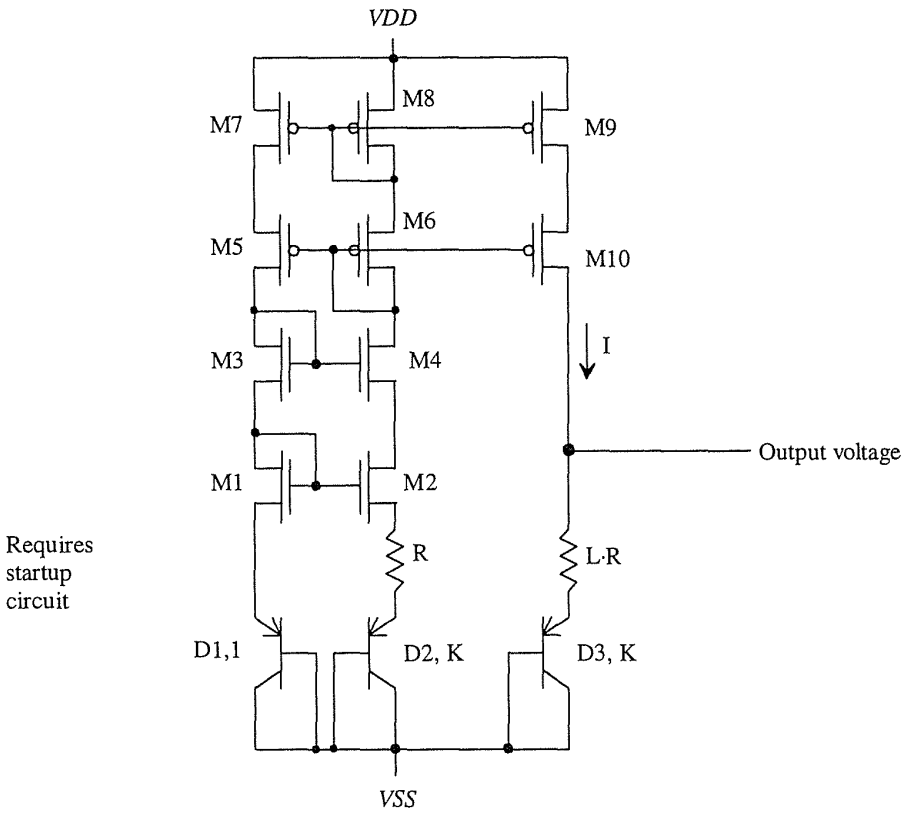


Figure 21.14 A bandgap voltage reference.

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The *TC* of the bandgap reference is zero when

$$\frac{\partial V_{ref}}{\partial T} = L \cdot n \cdot \ln K \cdot \overbrace{\frac{\partial V_T}{\partial T}}^{0.085\ mV/°C} + \overbrace{\frac{\partial V_{d3}}{\partial T}}^{-2\ mV/°C} = 0 \tag{21.34}$$

This is true when

$$L \cdot n \cdot \ln K = \frac{2}{0.085} = 23.5 \tag{21.35}$$

For $n = 1$ and $K = 8$ the factor L is 11.3 for a zero *TC*. We will round L up to 12 for the design here. The reference voltage, with respect to *VSS*, may also be written as

$$V_{ref} = (Ln \ln K) \cdot V_T + nV_T \cdot \ln \frac{I}{K \cdot I_s} \tag{21.36}$$

The reference voltage at 300 °K for $I = 10\ \mu A$, $I_s = 10^{-15}$A, $n = 1$, $K = 8$, and $L = 12$ is 1.25V (i.e., $V_{ref} = 1.25$ if *VSS* = 0 and *VDD* = 5 V). A PSPICE simulation of this bandgap is shown in Fig. 21.15. The current source designed in Ex. 21.3 was used to bias a resistor of value 65 kΩ and a diode with an area of eight times the minimum size. Note: To accurately predict the reference voltage, thorough characterization of the parasitic pnp is required over process and temperature variations.

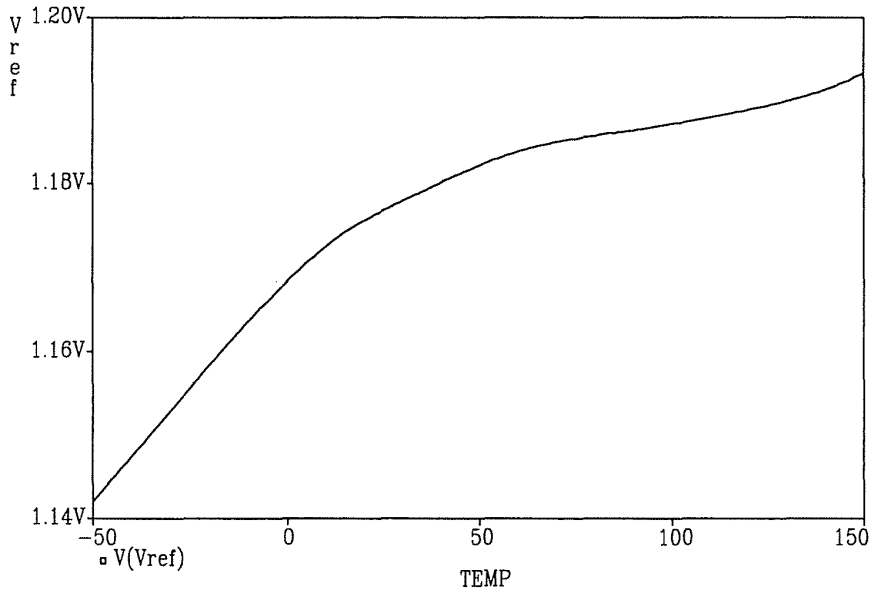


Figure 21.15 PSPICE simulation results of a bandgap voltage reference.

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21.4 Beta Multiplier Referenced Self-Biasing

A biasing scheme that deserves special mention is the β multiplier reference of Fig. 21.16 [3]. The width of M2 is made K times larger than the width of M1, so that

$$\beta_2 = K \cdot \beta_1, \text{ assuming } L_1 = L_2 \text{ and } W_2 = K \cdot W_1 \tag{21.37}$$

and therefore

$$V_{GS1} = V_{GS2} + IR \tag{21.38}$$

We can write V_{GS} of MOSFETs M1 and M2 in terms of the current I as

$$V_{GS1} = \sqrt{\frac{2I}{\beta_1}} + V_{THN} \tag{21.39}$$

and neglecting the body effect

$$V_{GS2} = \sqrt{\frac{2I}{K \cdot \beta_1}} + V_{THN} \tag{21.40}$$

Solving for I using the previous three equations yields

$$I = \frac{2}{R^2 \beta_1} \cdot \left(1 - \sqrt{\frac{1}{K}}\right)^2 \tag{21.41}$$

This is the basic design equation for this reference. The size parameter K must always be greater than 1. The temperature coefficient of the current reference is given by

$$TC_I = \frac{1}{I}\frac{\partial I}{\partial T} = -2 \cdot \frac{1}{R}\frac{\partial R}{\partial T} - \frac{1}{KP(T)}\frac{\partial KP(T)}{\partial T} = -4{,}000 \text{ ppm/°C} + \frac{1.5}{T} \tag{21.42}$$

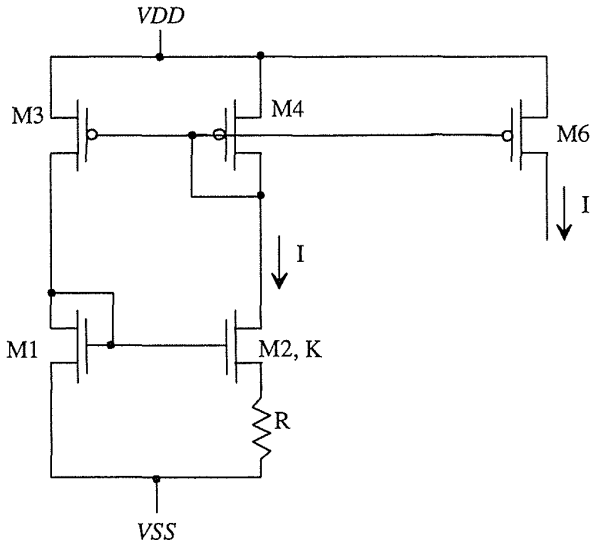


Figure 21.16 β multiplier referenced self-biasing ($\beta_2 = K \cdot \beta_1$).

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Example 21.4

Using the β multiplier current reference, design a 10 μA current source. Estimate the *TC* of the reference and assume *VDD* = –*VSS* = 2.5 V.

If we set $L_1 = L_2 = W_1 = 5$ μm and $K = 4$, then using Eq. (21.41) and solving for *R* results in

$$R^2 = \frac{2}{10\ \mu A \cdot 50\frac{\mu A}{V^2}} \cdot \frac{1}{4} \rightarrow R = 31.6\ k\Omega$$

The *TC* at 300 °K from Eq. (21.42) is 1,000 ppm/°C. A schematic of the design is shown in Fig. 21.17. Cascode MOSFETs were used to reduce the effects of the finite r_o of the MOSFETs. ■

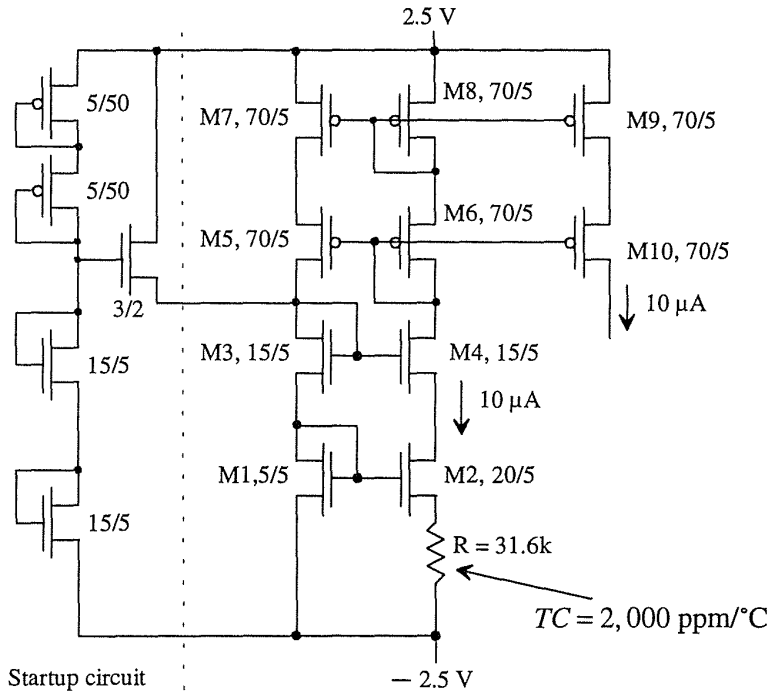


Figure 21.17 A 10 μA reference using a transconductance multiplier self-biased reference.

21.4.1 A Voltage Reference

It is of interest to determine the temperature dependence of V_{GS1} in Fig. 21.16. If the reference is designed correctly, we can make the *TC* of V_{GS1} equal to zero. We define our reference voltage as

$$V_{ref} = V_{GS1} \tag{21.43}$$

Substituting Eq. (21.41) into Eq. (21.38) results in

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$$V_{ref} = V_{GS1} = \frac{2}{R\beta_1}\left(1 - \frac{1}{\sqrt{K}}\right) + V_{THN} \tag{21.44}$$

The change in V_{ref} with temperature is

$$\frac{dV_{ref}}{dT} = \frac{dV_{THN}}{dT} - \frac{2}{R\beta_1}\left(1 - \frac{1}{\sqrt{K}}\right)\left[\frac{1}{R}\frac{\partial R}{\partial T} + \frac{1}{KP(T)}\frac{\partial KP(T)}{\partial T}\right] \tag{21.45}$$

or

$$\frac{dV_{ref}}{dT} = -2.4 \text{ mV/°C} + \frac{2}{R\beta_1}\left[1 - \frac{1}{\sqrt{K}}\right]\left[-2{,}000 \text{ ppm/°C} + \frac{1.5}{T}\right] \tag{21.46}$$

At 300 °K Eq. (21.46) is equal to zero when

$$\frac{2}{R\beta_1}\left[1 - \frac{1}{\sqrt{K}}\right] = \frac{2{,}400}{3{,}000} = 0.8 \tag{21.47}$$

Furthermore, if $K = 4$ we require that

$$R = \frac{1}{0.8 \cdot \beta_1} \tag{21.48}$$

and

$$V_{ref} = 0.8 + V_{THN} = 1.63 \text{ V} \tag{21.49}$$

There will be an error in the reference voltage associated with the change in the threshold voltage due to process variations and body effect as well as changes in R, β, and T. Using p-channel MOSFETs in their own well eliminates errors due to the body effect. The threshold voltage can vary by as much as 20 percent (this is part of the reason why the body effect is neglected so often in our hand calculations). Thus, precision voltages are more difficult to achieve than the bandgap reference of the last section. Often, voltage references are adjusted on die by laser trimming via metal options a resistor value. The following example illustrates the design and temperature performance of a zero *TC* voltage reference using the β multiplier self-biased reference.

Example 21.5

Design a zero *TC* voltage β multiplier reference at 300 °K with *VSS* = 0 V and *VDD* = 5 V. Simulate the design for changing *VDD* and temperature.

We will use the general cascode schematic of Fig. 21.17 (with the same sizes) with *VDD* swept in the simulations and *VSS* = 0. The resistor for this design is

$$R = \frac{1}{0.8 \cdot 50 \frac{\mu A}{V^2}} = 25 \text{ k}\Omega$$

The simulation results are shown in Fig. 21.18. ■

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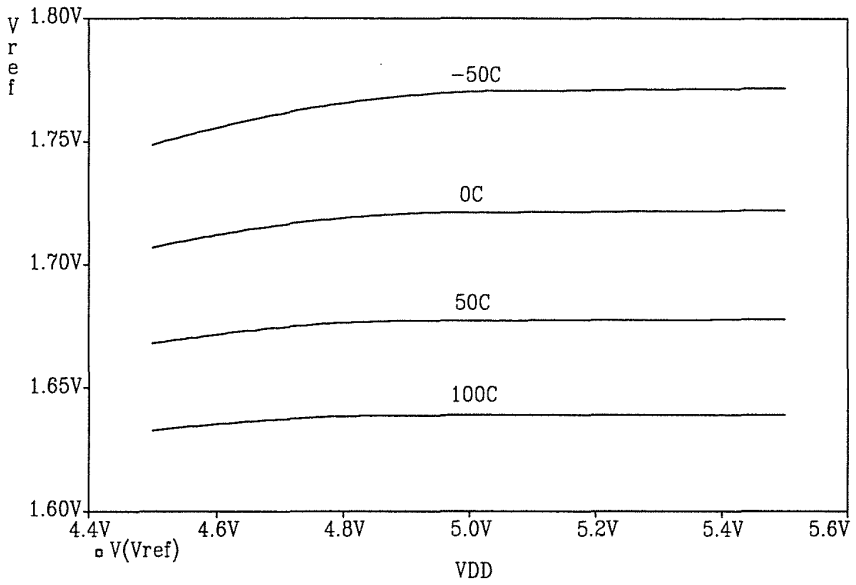


Figure 21.18 Temperature characteristics of the beta multiplier voltage reference.

21.4.2 Operation in the Subthreshold Region

For low-power operation, it may be desirable to operate a current source/sink in the weak inversion, or subthreshold region. Currents in these circuits can be 100 nA or less. Consider the value of the resistor needed for $I_{D1} = 100$ nA in Eq. (20.4). If $VDD - VSS >> V_{GS}$, then the value of R for the simple current mirror is given by

$$R \approx \frac{VDD - VSS}{I_{D1}} \tag{21.50}$$

If $VDD - VSS = 5$ V, then $R = 50$ MEG! Clearly, the basic current mirror with resistor bias will not be useful in circuits operating in the subthreshold region.

Consider designing the basic β multiplier of Fig. 21.16 so that it operates in the subthreshold region where the current is given, from Ch. 6, by

$$I \approx I_{\text{exp}} = I_{DO}\frac{W}{L} \cdot (e^{(V_{GS}-V_{THN})/(n \cdot V_T)}) \tag{21.51}$$

Following the same procedure as in the case of strong inversion

$$V_{GS1} = nV_T \cdot \ln\left[\frac{I \cdot L}{I_{DO} \cdot W}\right] + V_{THN} \tag{21.52}$$

and

$$V_{GS2} = nV_T \cdot \ln\left[\frac{I \cdot L}{I_{DO} \cdot K \cdot W}\right] + V_{THN} \tag{21.53}$$

Solving for the subthreshold current I using Eq. (21.38) and Eqs. (21.52) and (21.53), we get

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$$I_D = \frac{n \cdot V_T}{R} \cdot \ln K \tag{21.54}$$

Note the similarity to the thermal voltage referenced self-biasing circuit. Note also that this current reference can be used to generate a bandgap voltage reference as was discussed in Sec. 21.3.1. The following example illustrates the design of a subthreshold current source.

Example 21.6

Design and simulate a 75 nA current source with *VDD* = 5 V and *VSS* = 0.

Using Eq. (21.54) with K = 8, n = 1, V_T = 26 mV @ room temperature (approximately 27 °C) yields

$$R = \frac{26\text{mV}}{75\text{nA}} \cdot \ln 8 = 720\ \text{k}\Omega$$

We will use the general schematic of Fig. 21.17 with W_2, which is now 40 μm.

The resulting SPICE simulation of the output current versus voltage at the drain of M10 is shown in Fig. 21.19. Notice that V_{out} can get very close to V_{DD}, within 100 mV, before M10 begins to shut off. Also notice that the current is almost twice what we designed for. This is due to the body effect of M2. Small variations across R have a large effect on the current. Using the p-channel MOSFETs version of Fig. 21.16 with each p-channel in its own well eliminates the body-effect problem. ■

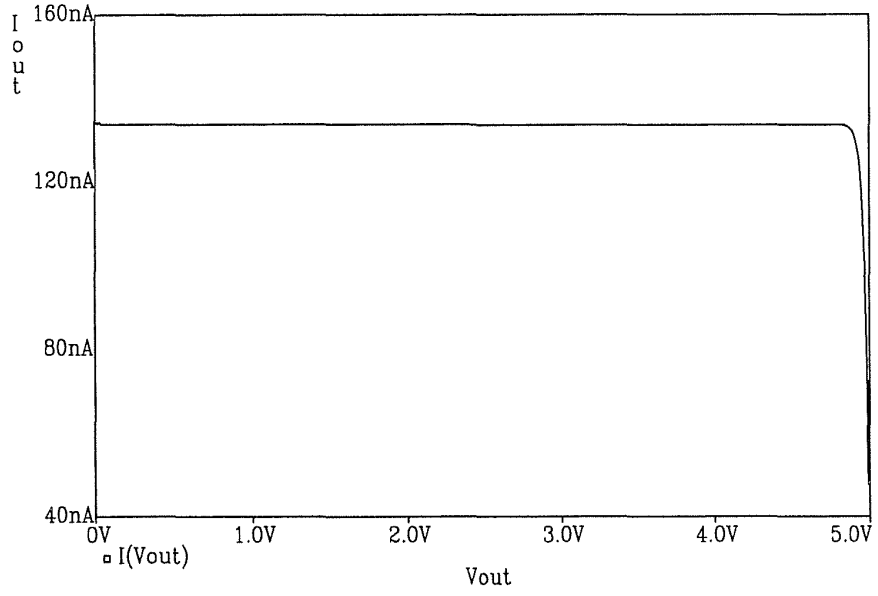


Figure 21.19 Simulation results of Ex. 21.6, the design of a subthreshold current source.

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[1] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits,* 3rd ed., John Wiley and Sons, 1993. ISBN 0-471-57495-3.

[2] R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI-Design Techniques for Analog and Digital Circuits,* McGraw-Hill Publishing Co., 1990. ISBN 0-07-023253-9.

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PROBLEMS

21.1 Design a resistor-MOSFET voltage divider, Fig. P21.1, so that the reference voltage, V_{ref}, is 2 V and the current through the resistor is 10 μA. Verify the operation of the circuit using SPICE.

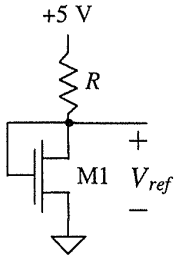


Figure P21.1

21.2 Determine the output voltage and temperature coefficient of the voltage reference in Fig. P21.1 if W/L = 20/5 and R = 400k. Assume that the TC of the resistor is 10,000 ppm/°C. Compare the hand-calculated TC of the reference to SPICE simulations.

21.3 Design a MOSFET-MOSFET voltage divider, Fig. P21.3, so that the reference voltage, V_{ref}, is 2 V and the current through each MOSFET is 10 μA. Verify the operation of the circuit using SPICE.

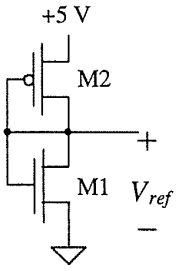


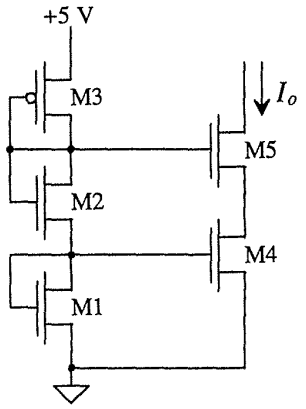
Figure P21.3

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21.4 Determine the output voltage and temperature coefficient of the voltage reference in Fig. P21.3 if the *W/L* of both MOSFETs is 20/20. Compare the hand-calculated *TC* of the reference to SPICE simulations.

21.5 Calculate and simulate the sensitivity of the reference described in Problem 4 to *VDD*.

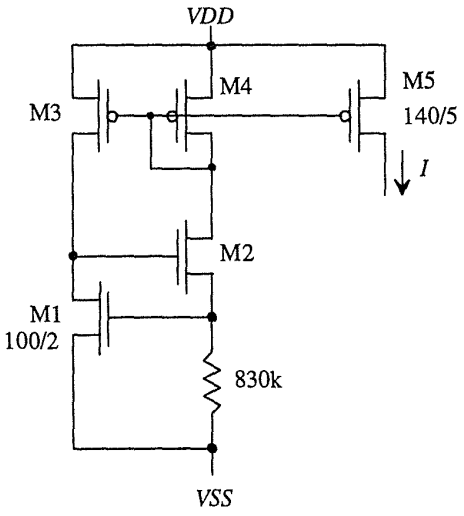
21.6 Select the size of M3 in Fig. P21.6 so that 10 μA flows in all MOSFETs in the circuit. Assume that M5 and M4 are operating in the saturation region.



All n-channels are 15/5.

Figure P21.6

21.7 Determine the current *I* in Fig. P21.7. Neglect oxide encroachment and assume that M5 is operating in the saturation region.



All unlabeled n-channels are 15/5.
All unlabeled p-channels are 70/5.

Figure P21.7

21.8 Sketch a startup circuit for the threshold-voltage referenced current source of Fig. P21.7. Assume the maximum current in the startup circuit is 1 μA.

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21.9 Lay out a parasitic PNP transistor with an emitter size of 2 (emitter size of 12 μm by 6 μm). What value of IS will be used in the diode model if the area specified for the diode is 1 (which is the same as not specifying an area for the diode)?

21.10 Design a 5 μA current source using the diode referenced self-biasing circuit of Fig. 21.11. Verify the operation of your design using SPICE. (Either include a startup circuit or use the .NODESET statement to keep the circuit from operating at point B in Fig. 21.8.)

21.11 Repeat Ex. 21.3 for a 5 μA current source.

21.12 Verify that Eq. (21.36) is correct. How is the resulting reference voltage affected by using an $L = 12$ instead of 11.3 (Does the reference voltage increase or decrease? Why?)

21.13 The main reason for using the cascode MOSFETs, M1 through M10, shown in Fig. 21.14 is to force the same current through D2 and D3. The main problem with this configuration is the dependence of the reference voltage on changes in the power supply. Using an op-amp to force the same currents through D2 and D3 can improve the sensitivity of the reference voltage to power supply variations (Fig. P21.13). Knowing the reference voltage is given by

$$V_{ref} = V_{d2} + I \cdot L \cdot R$$

show that the current that flows in D1 and D2 is

$$I = \frac{nV_T \cdot \ln K}{R}$$

and therefore

$$V_{ref} = (L \cdot n \cdot \ln K) \cdot V_T + \overbrace{nV_T \cdot \ln \frac{I}{I_S}}^{V_{d2}}$$

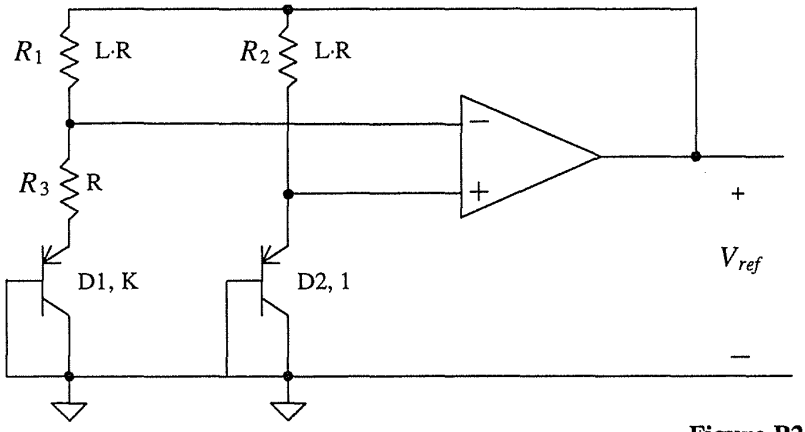
Determine the conditions under which the *TC* of the reference is zero (review Eq. [21.34]).

21.14 Estimate the power dissipated by the startup circuit shown in Fig. 21.17.

21.15 Using the β multiplier voltage reference, design a voltage reference with a *TC* of +1,000 ppm/°C. Simulate the operation of the reference. Often, in digital systems, it is desirable to increase the supply voltage used to power the digital logic with increasing temperature to compensate for the increase in the MOSFETs' effective resistance and thus the increase in the gate-delay times.

21.16 The β multiplier reference is an example of a circuit that uses positive feedback (the loop gain is less than one). Discuss methods of ensuring a stable operating point for the circuit.

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A bandgap reference

Figure P21.13

21.17 An important consideration in the design of a voltage or current reference is the design of the startup circuit. Consider the portion of the bandgap reference of Fig. P21.13 shown in Fig. P21.17a. Using SPICE, plot V_{ref} against V_{plus} (the noninverting input of the op-amp) and V_{minus} (the inverting input of the op-amp). The result should look similar to Fig. P21.17b. Design a startup circuit for the bandgap of Fig. P21.13.

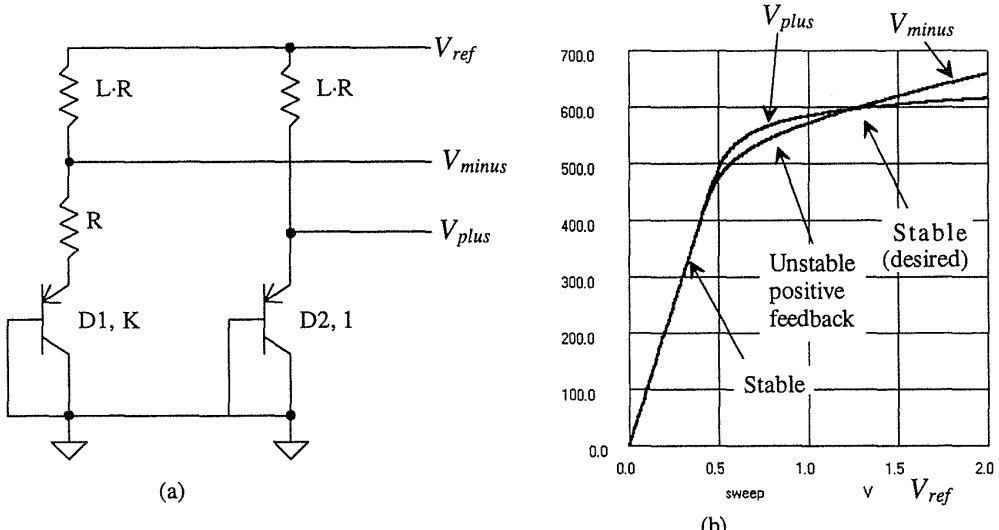


Figure P21.17

21.18 Show that if $K = 1$ and $R_1 \neq R_2$, in Fig. P21.13, the output of the bandgap reference can be written as $V_{ref} = V_{d2} + \frac{R_1}{R_3} nV_T \cdot \ln \frac{R_1}{R_2}$.

21.19 Repeat Ex. 21.6 for a 0.1 μA current source.

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Chapter

22

Amplifiers

Single-stage amplifiers are used in virtually every op-amp design. By replacing a passive load resistor with a MOSFET transistor (called an active load), significant amounts of chip area can be saved. An active load can also produce higher values of resistance when compared with a passive resistor, resulting in higher gains.

Several types of active loads are studied in this chapter. The gate-drain connected load consists of a MOSFET with the gate and drain shorted and provides large bandwidths at the cost of reduced gain and low-output impedance. The current source load amplifier has a higher gain and higher output impedance, but usually at the expense of producing a lower bandwidth. Current source load amplifiers are preferred when external feedback is applied to the amplifier to set the gain. The chapter will explore basic single-stage amplifiers with active loads, as well as the corresponding tradeoffs associated with each. The cascode amplifier will also be examined in detail along with several configurations of output stages, including the push-pull amplifier.

22.1 Gate-Drain Connected Loads

The four types of gate-drain connected load amplifiers are shown in Fig. 22.1. All four of these configurations are basic common source voltage amplifiers. In each configuration, M1 and M2 are assumed to be biased in the saturation region.

22.1.1 Common Source Amplifiers

Examine the AC small-signal circuit shown in Fig. 22.1a. Since many MOSFET amplifiers will be analyzed here using small-signal analysis, an intuitive approach will be presented which allows the designer to analyze the circuit very quickly. Begin by replacing M2 with a resistor of value $\frac{1}{g_{m2}}$ and replacing M1 with a current source of value $g_{m1} \cdot v_{in}$, provided $\frac{1}{g_{m2}} << r_{o1}$. The equivalent circuit is shown in Fig. 22.2. Note that there is no body effect in either MOSFET and that only the low-frequency model is

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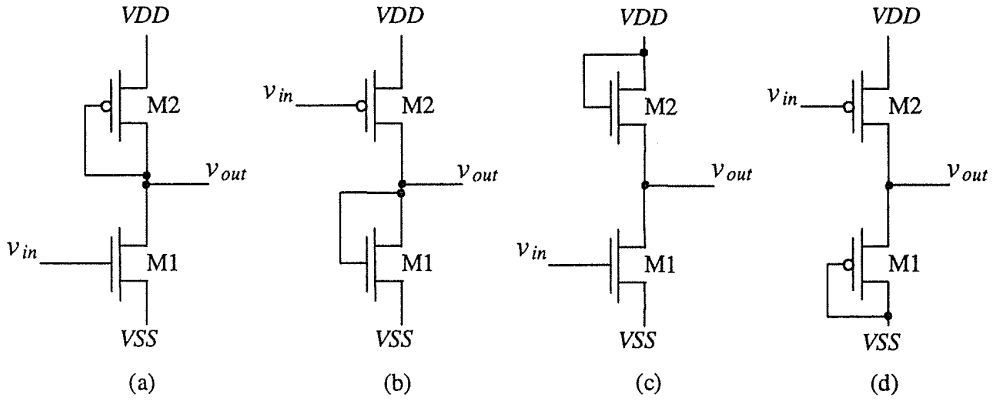


Figure 22.1 The four active load configurations available in CMOS.

shown. Again, as was seen in Ch. 9, a gate-drain connected MOSFET has a small-signal resistance of value $\frac{1}{g_m}$. The small-signal gain of this circuit is given by

$$\frac{v_{out}}{v_{in}} = \frac{-i_d \cdot \frac{1}{g_{m2}}}{i_d \cdot \frac{1}{g_{m1}}} = -\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}}} = -\frac{\text{resistance in the drain}}{\text{resistance in the source}} = -\frac{g_{m1}}{g_{m2}} \qquad (22.1)$$

This result is very important in the intuitive analysis. It states that the small-signal gain of a common source amplifier is simply the resistance in the drain of M1 divided by the resistance in the source (the resistance looking into the source of M1 added to any resistance from the source of M1 to ground).

The intuitive approach results in an approximation for the gain. The actual value of the resistance in the drain, as will be soon discovered, is $\frac{1}{g_{m2}} || r_{o1} || r_{o2}$. In most cases, however, r_o will be much greater than $\frac{1}{g_m}$, and the approximation is an accurate one.

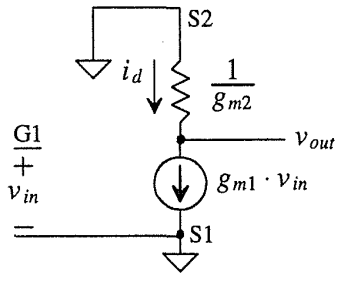


Figure 22.2 Simplified circuit of Fig. 22.1a.

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Example 22.1

Determine the small-signal AC gain of the circuit shown in Fig. 22.3 using the intuitive method presented in Eq. (22.1).

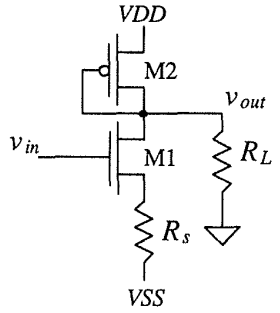


Figure 22.3 Amplifier analyzed in Ex. 22.1.

The small-signal gain of this circuit is given by

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{\text{resistance in the drain}}{\text{resistance in source}}$$

The resistance in the drain is the parallel combination of all resistances connected to the drain of M1 given by

$$\text{Resistance in the drain} = \frac{1}{g_{m2}} || R_L \text{ for } r_{o1} >> \frac{1}{g_{m2}}$$

The resistance in the source is the sum of the resistance looking into the source of M1 and the resistance connected from the source of M1 to ground. For the present problem, this resistance is given by

$$R_{\text{in the source}} = \frac{1}{g_{m1}} + R_s$$

The voltage gain is then given by

$$A_v = -\frac{\frac{1}{g_{m2}} || R_L}{\frac{1}{g_{m1}} + R_s} \text{ which for } R_L \to \infty \text{ and } R_s \to 0 \text{ reduces to } -\frac{g_{m1}}{g_{m2}} \blacksquare$$

We can determine the exact gain of the amplifier of Fig. 22.1a using the full small-signal model shown in Fig. 22.4. Using KCL at the output of the amplifier gives

$$g_{m1} v_{in} + \frac{v_{out}}{r_{o2} || r_{o1}} = -g_{m2} v_{out} \tag{22.2}$$

or

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2} + \frac{1}{r_{o1}+r_{o2}}} = -\frac{\frac{1}{g_{m2}} || r_{o1} || r_{o2}}{\frac{1}{g_{m1}}} = -\frac{\text{resistance in the drain}}{\text{resistance in the source}} \tag{22.3}$$

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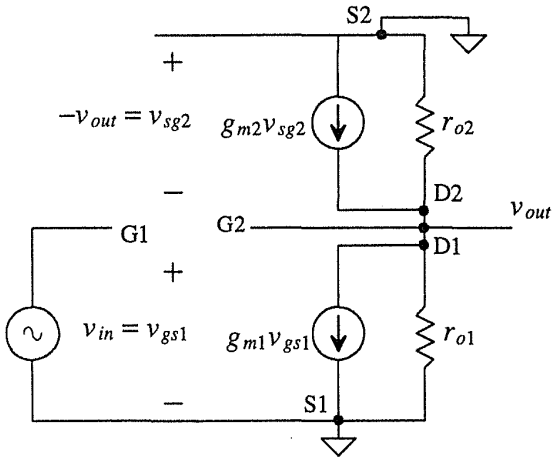


Figure 22.4 Small-signal model of the amplifier shown in Fig. 22.1(a).

For the case when $\frac{1}{g_{m2}} << r_{o1} || r_{o2}$, this reduces to

$$A_v = -\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}}} = -\frac{g_{m1}}{g_{m2}} \tag{22.4}$$

which is the same form as Eq. (22.2).

Now consider the frequency response of the common source amplifier of Fig. 22.1a. The high-frequency equivalent circuit is shown in Fig. 22.5, with the MOSFET capacitances drawn explicitly. A source resistance is added to the circuit to model the effects of the driving source impedance. Miller's Theorem is used to break C_{gd1} into two parts; a capacitance at the gate of M1 to ground and a capacitance from the drain of M1 to ground. Two *RC* time constants exist in this circuit, one on the input of the circuit and one on the output of the circuit. The input time constant, neglecting C_{gb}, is given by

$$\tau_{in} = R_s(C_{MI} + C_{gs1}) \tag{22.5}$$

where the Miller capacitance at the input, C_{MI} is

$$C_{MI} = C_{gd1}(1 + \frac{g_{m1}}{g_{m2}}) \tag{22.6}$$

When using Miller's Theorem, it should be noted that the capacitance, C_{gd1}, is multiplied by the factor (1 – *K*), where *K* is the gain, $-\frac{g_{m1}}{g_{m2}}$.

The output time constant is found in a similar way and is given by

$$\tau_{out} = \frac{1}{g_{m2}} \cdot (C_{gs2} + C_{MO} + C_{db1} + C_{db2}) \tag{22.7}$$

The Miller capacitance which appears at the output, C_{MO}, now becomes

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$$C_{MO} = C_{gd1}(1 - \frac{1}{K}) = C_{gd1}(1 + \frac{g_{m2}}{g_{m1}}) \tag{22.8}$$

The frequency response of this amplifier is given by

$$A_v(f) = \frac{-\frac{g_{m1}}{g_{m2}}}{\left(1 + j\frac{f}{f_{in}}\right)\left(1 + j\frac{f}{f_{out}}\right)} \tag{22.9}$$

where

$$f_{in} = \frac{1}{2\pi\tau_{in}} \tag{22.10}$$

and

$$f_{out} = \frac{1}{2\pi\tau_{out}} \tag{22.11}$$

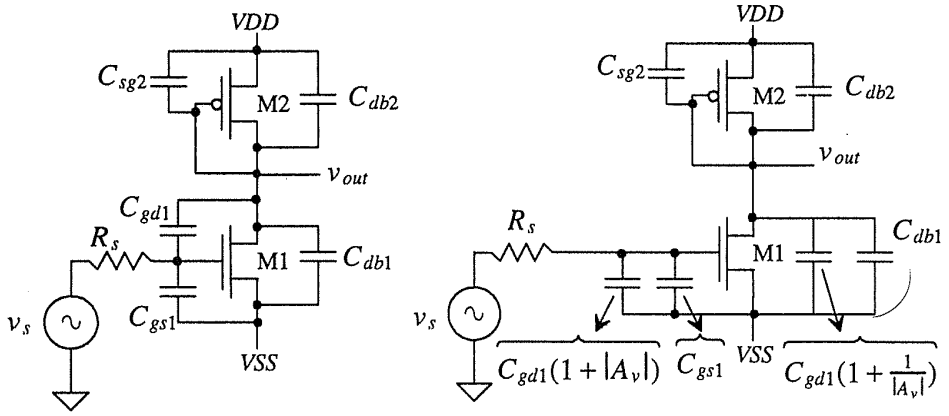


Figure 22.5 Frequency response of the simple common source amplifier with active load.

It should be noted that when using Miller's Theorem, a zero is neglected. For example, in Fig. 22.6, if the input is assumed to be driven from a voltage source so that the input parasitics can be ignored, the transfer function becomes,

$$\frac{v_o}{v_{in}} = -g_{m1}R_{Leq}\frac{(1 - s/\omega_{z1})}{(1 + s/\omega_{p1})} \tag{22.12}$$

where ω_{z1} is a right-hand plane zero of value

$$\omega_{z1} = \frac{g_{m1}}{C_{gd1}} \tag{22.13}$$

and ω_{p1} is the pole at the output of the amplifier of value

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$$\omega_{p1} = \frac{1}{R_{Leq}(C_{Leq} + C_{gd1})} \tag{22.14}$$

where $C_{Leq} = C_{sg2} + C_{db1} + C_{db2}$ and $R_{Leq} = r_{o1} \| r_{o2} \| 1/g_{m2}$. The magnitude response of the right-hand plane zero is usually ignored since its value typically places it well beyond the pole frequency. However, the phase response can cause problems since a right-hand plane zero has the same phase as a left-hand plane pole, which could seriously affect stability when the single-stage amplifier is used within an op-amp. These stability issues along with the compensation techniques are presented in Ch. 25.

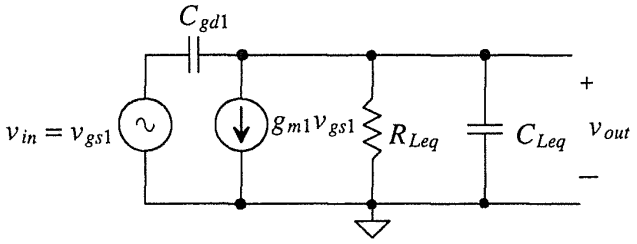


Figure 22.6 Small-signal model used to calculate the RHP zero for amplifiers in Fig. 22.1a-d.

Example 22.2

Determine the gain and bandwidth of the amplifier shown in Fig. 22.7.
Determine the output voltage when the input voltage is $10^{-3}\sin 2\pi \cdot 1000t$ volts.

The drain current that flows in M1, and thus M2, is given by

$$I_D = \frac{\beta_1}{2}(V_{GS1} - V_{THN})^2 = \frac{50\mu}{2} \cdot \frac{5\mu}{5\mu}(2.5 - 0.8)^2 = 72\ \mu\text{A}$$

while V_{SG2} is determined by

$$I_D = 72\ \mu\text{A} = \frac{\beta_2}{2}(V_{SG2} - V_{THP})^2 = \frac{17\mu}{2} \cdot \frac{15\mu}{5\mu}(V_{SG2} - 0.9)^2 \Rightarrow V_{SG2} \approx 2.5\ \text{V}$$

The DC portion of the output voltage is approximately 0 V. The AC gain is given by

$$A_v = -\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}}} = -\frac{g_{m1}}{g_{m2}} = -\frac{\sqrt{2\beta_1 I_D}}{\sqrt{2\beta_2 I_D}} = -1$$

Voltage gains in the neighborhood of 1 are common when using gate-drain connected loads. At this point it may appear that this amplifier is almost worthless; however, we will see that when this amplifier is used with additional circuitry (e.g., a current source load for a differential pair) it can be very useful. The output voltage when the input is a 1 mV sine wave at 1 kHz is given by

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$$v_{OUT} = \overbrace{0\ V}^{DC} + \overbrace{10^{-3}\sin(2\pi \cdot 1000t + \pi)}^{AC\ component}$$

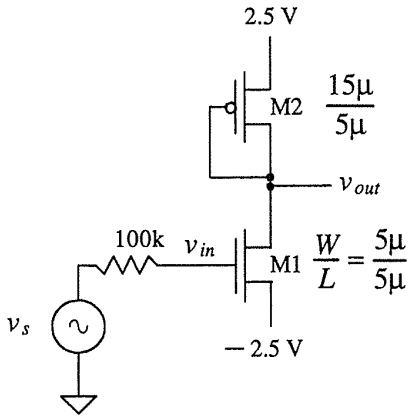


Figure 22.7 Amplifier used in Ex. 22.2.

The bandwidth of the amplifier is calculated by first estimating the capacitances of the MOSFETs. Assuming the drain diffusion to substrate/well is 2.5 V and the n-channel drain area measures 6 μm by 6 μm, while the p-channel drain area measures 15 μm by 6 μm, we find that the capacitances are given by

$$C_{db1} = \frac{CJ \cdot AD}{\left(1 - \frac{V_{db1}}{PB}\right)^{MJ}} + \frac{CJSW \cdot PD}{\left(1 - \frac{V_{db1}}{PBSW}\right)^{MJSW}} = \frac{1.04 \times 10^{-4}\frac{\text{F}}{\text{m}^2} \cdot 36 \times 10^{-12}\text{m}^2}{\left(1 + \frac{2.5}{0.8}\right)^{0.66}} +$$

$$\frac{2.2 \times 10^{-10}\frac{\text{F}}{\text{m}} \cdot 24 \times 10^{-6}\text{m}}{\left(1 + \frac{2.5}{0.8}\right)^{0.18}} = 5.5\ \text{fF}$$

and for the p-channel $C_{db2} = 15.4$ fF. The other capacitances are calculated from

$$C_{gd1} = CGDO \cdot W = 3.8 \times 10^{-10}\frac{\text{F}}{\text{m}} \cdot 5\mu\text{m} = 1.9\ \text{fF}$$

$$C_{gs1} = \frac{2}{3}WLC'_{ox} = \frac{2}{3} \cdot 5\mu\text{m} \cdot 5\mu\text{m} \cdot 800\frac{\text{aF}}{\mu\text{m}^2} = 13.3\ \text{fF}$$

$$C_{sg2} = \frac{2}{3}WLC'_{ox} = \frac{2}{3} \cdot 15\mu\text{m} \cdot 5\mu\text{m} \cdot 800\frac{\text{aF}}{\mu\text{m}^2} = 48\ \text{fF}$$

The input time constant is given by

$$\tau_{in} = 100\text{k} \cdot [1.9\text{fF}(1+1) + 13.3\text{fF}] = 1.7\ \text{ns}$$

and the output time constant is given by

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$$\tau_{out} = \frac{1}{\sqrt{2 \cdot 17\frac{\mu A}{V} \cdot \frac{15\mu}{5\mu} \cdot 72\ \mu A}} \cdot (48\ \text{fF} + 1.9\ \text{fF}(1+1) + 5.5\ \text{fF} + 15.4\ \text{fF}) = 840\ \text{ps}$$

The input time constant dominates. Therefore, the bandwidth of this amplifier can be estimated by

$$f_{3dB} = f_{in} = \frac{1}{2\pi \cdot 1.7\text{ns}} = 93.6\ \text{MHz}$$

Large bandwidth is the main advantage of the active gate/drain-connected load amplifier while low gain is the main drawback. ■

The previous discussion was centered around common source voltage amplifiers. Consider the circuit shown in Fig. 22.8. This amplifier can be thought of as a transimpedance amplifier, that is, voltage out and current in. The input impedance of this amplifier is given by

$$R_{in} = \frac{1}{g_{m3}} \tag{22.15}$$

The input current, i_{in}, is determined by

$$i_{in} = g_{m3} v_{in} = g_{m3} v_{gs3} = g_{m3} v_{gs1} \tag{22.16}$$

The current through M1, and thus M2, is given by

$$i_d = g_{m1} v_{in} = \frac{g_{m1}}{g_{m3}} \cdot i_{in} \tag{22.17}$$

This equation can be rewritten as

$$\frac{i_d}{i_{in}} = \frac{\beta_1}{\beta_3} = \frac{W_1 L_3}{W_3 L_1} \tag{22.18}$$

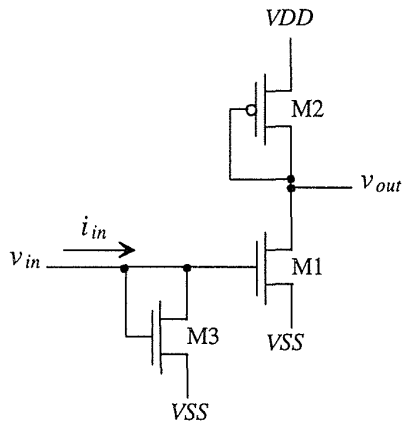


Figure 22.8 An implementation of the transimpedance amplifier.

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That is, we can get a current gain simply by adjusting the size of M1 and M3. The transresistance gain of this configuration is given by

$$A_R = \frac{v_{out}}{i_{in}} = -\frac{i_d \frac{1}{g_{m2}}}{i_d \cdot \frac{W_3 L_1}{W_1 L_3}} = -\frac{W_1 L_3}{g_{m2} W_3 L_1} \tag{22.19}$$

Adding M3 and thus the resistor of value $\frac{1}{g_{m3}}$ to ground lowers the input time constant and thus increases the bandwidth of the amplifier.

Before we proceed any further, let's review, or again verify, how to determine the small-signal, low-frequency resistances looking into the drain and source of a MOSFET. Using this information will greatly aid in our intuitive analysis of CMOS circuits. Consider the test circuit shown in Fig. 22.9. Here the DC voltages ensure that the MOSFET is operating in the saturation region. We are concerned with the AC current that flows through v_t. This test voltage divided by i_d gives us the small-signal AC resistance looking into the drain of the MOSFET. In other words, this is the resistance connected to ground at the drain node.

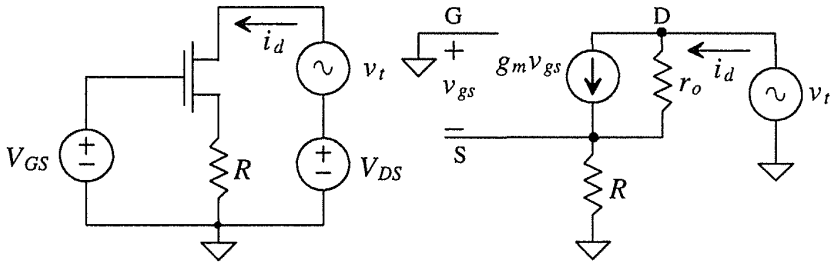


Figure 22.9 Circuit used to determine the resistance looking into the drain of a MOSFET.

Neglecting the body effect, we may write, the test voltage as

$$v_t = (i_d - g_m v_{gs}) r_o + i_d R \tag{22.20}$$

where

$$v_{gs} = -i_d R \tag{22.21}$$

The resistance looking into the drain of the MOSFET is then given by

$$R_o = r_d = \frac{v_t}{i_d} = (1 + g_m R) r_o + R \approx (1 + g_m R) r_o \tag{22.22}$$

keeping in mind that $r_o \approx \frac{1}{\lambda I_D}$.

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Example 22.3

Repeat Ex. 22.1 without neglecting the loading effects of the output resistances of M1 and M2. Use the circuit shown in Fig. 22.3.

The resistance looking into the drain of M2 is $\frac{1}{g_{m2}}||r_{o2}$, while the resistance looking into the drain of M1 is $r_{o1}(1+g_{m1}R_s)$. The exact gain of the circuit is simply

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{\frac{1}{g_{m2}}||r_{o2}||[r_{o1}(1+g_{m1}R_s)]||R_L}{R_s+\frac{1}{g_{m1}}}$$

or when $r_{01}||r_{o2} >> \frac{1}{g_{m2}}$ this reduces to

$$A_V = \frac{\frac{1}{g_{m2}}||R_L}{R_s+\frac{1}{g_{m1}}} \blacksquare$$

The resistance looking into the source of the MOSFET can be found using the circuit shown in Fig. 22.10. Neglecting the body effect and output resistance of the MOSFET gives

$$v_{in} = v_{gs} + i_d R \tag{22.23}$$

Since $g_m v_{gs} = i_d$, this equation can be written as

$$v_{in} = \frac{i_d}{g_m} + i_d R = i_d\left[\frac{1}{g_m} + R\right] \tag{22.24}$$

We can look at this in a simplified manner; that is, $\frac{1}{g_m}$ is the resistance looking into the source of a MOSFET, while R is the resistance connected from the source of the MOSFET to ground. Note that R can be the parallel combination of several resistances.

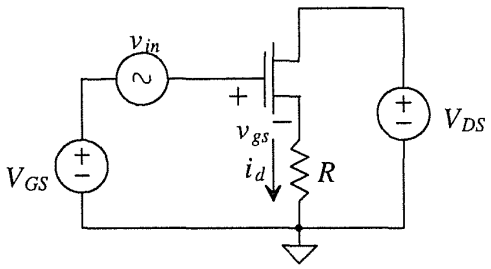


Figure 22.10 Circuit used to determine the resistance looking into the source of a MOSFET.

22.1.2 The Source Follower

Source-follower configurations using active loads are shown in Fig. 22.11. The MOSFET M2 sources current, while M1 sinks current. A source follower implemented in CMOS has an asymmetric drive capability; that is, the ability of the follower to source current is not equal to the ability to sink current for a given bias condition and

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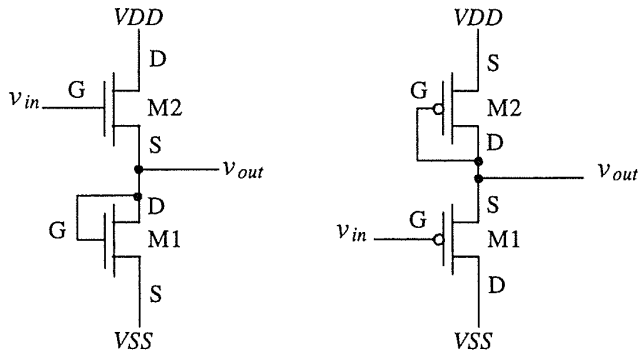


Figure 22.11 Source followers using active loads.

AC input signal. Also, in both configurations, the common drain amplifier exhibits the body effect. Before we analyze the small-signal behavior of this amplifier, let's determine how the body effect comes into play. From Ch. 9

$$g_{mb} = g_m \cdot \eta \tag{22.25}$$

where, using the BSIM SPICE parameters,

$$\eta = \frac{K1}{2\sqrt{PHI + V_{SB}}} - K2 \tag{22.26}$$

From this equation we can see that the larger the source-substrate potential of the MOSFET, the smaller g_{mb}.

Example 22.4

Determine η for the NMOS source follower shown above when the source of M1 is at 0 V potential and $VSS = -2.5$ V using CN20 parameters.

If we use Eq. (22.26) we get

$$\eta = \frac{K1}{2\sqrt{PHI + V_{SB}}} - K2 = \frac{1.49}{2\sqrt{0.75 + 2.5}} - 0.315 = 0.098$$

Therefore, the body transconductance, g_{mb}, is approximately 10 percent of the forward transconductance, g_m. The assumption that the transconductance from the body effect, g_{mb}, is negligible is valid for large V_{SB}. ■

The small-signal gain of the NMOS source follower shown in Fig. 22.11 is simply determined by a voltage divider between the resistance looking into the source of M2 with the resistance of the gate-drain connected load, M1. The output voltage is given by

$$v_{out} = v_{in} \cdot \frac{\frac{1}{g_{m1}}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} \tag{22.27}$$

or the gain of the source follower with an active load, remembering $g_m = \sqrt{2\beta_1 I_D}$, is

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$$A_v = \frac{v_{out}}{v_{in}} = \frac{\frac{1}{g_{m1}}}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} = \frac{1}{1 + \frac{g_{m1}}{g_{m2}}} = \frac{1}{1 + \sqrt{\frac{W_1 L_2}{W_2 L_1}}} \tag{22.28}$$

The output resistance of the source follower shown in this figure is

$$R_{out} = \frac{1}{g_{m1}} || \frac{1}{g_{m2}} \tag{22.29}$$

Again, it should be noted that M2 can only source current, while M1 can only sink current and the gain is always less than one.

22.1.3 Common Gate Amplifiers

The common gate amplifier with active load is shown in Fig. 22.12. The input resistance of this amplifier is simply the resistance looking into the source of M1, or

$$R_{in} = \frac{1}{g_{m1}} \tag{22.30}$$

The gain of this amplifier, again neglecting the body effect, is

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-i_d \cdot \frac{1}{g_{m2}}}{-v_{gs1}} = \frac{-i_d \cdot \frac{1}{g_{m2}}}{-i_d \cdot \frac{1}{g_{m1}}} = \frac{\text{resistance in the drain}}{\text{resistance in the source}} = \frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}}} \tag{22.31}$$

or

$$A_v = \frac{g_{m1}}{g_{m2}} = \sqrt{\frac{KP_n}{KP_p} \cdot \frac{W_1 L_2}{W_2 L_1}} \tag{22.32}$$

which is the same form as the gain for the common source amplifier with active load.

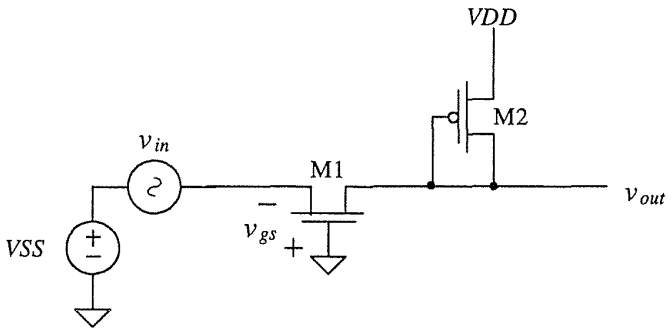


Figure 22.12 The common gate amplifier.

22.2 Current Source Loads

The current source load provides an amplifier with the largest possible load resistance available in a CMOS process. This section examines single-stage amplifier configurations utilizing current sources (or sinks) as loads.

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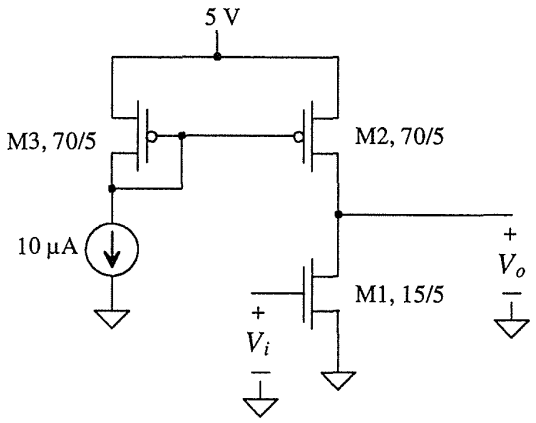


Figure 22.13 Common source amplifier with current source load.

Consider the common source amplifier with current source load shown in Fig. 22.13. The MOSFET M1 is the common source component of the amplifier, while the MOSFET M2 is the current source load. The DC transfer characteristics are shown in Fig. 22.14 for this amplifier. The slope of the line when both transistors are saturated corresponds to the small-signal gain of the amplifier. If we bias M1 and M2 so that they are both saturated, we see that the DC output voltage of the amplifier is very dependent on the DC biasing at the input of the amplifier. This is a common problem in CMOS analog integrated circuit design, that is, determining the exact voltage on the drains of two-series connected p- and n-channel MOSFETs. Feedback is normally employed to set the output voltage of the amplifier at some known value. This results in

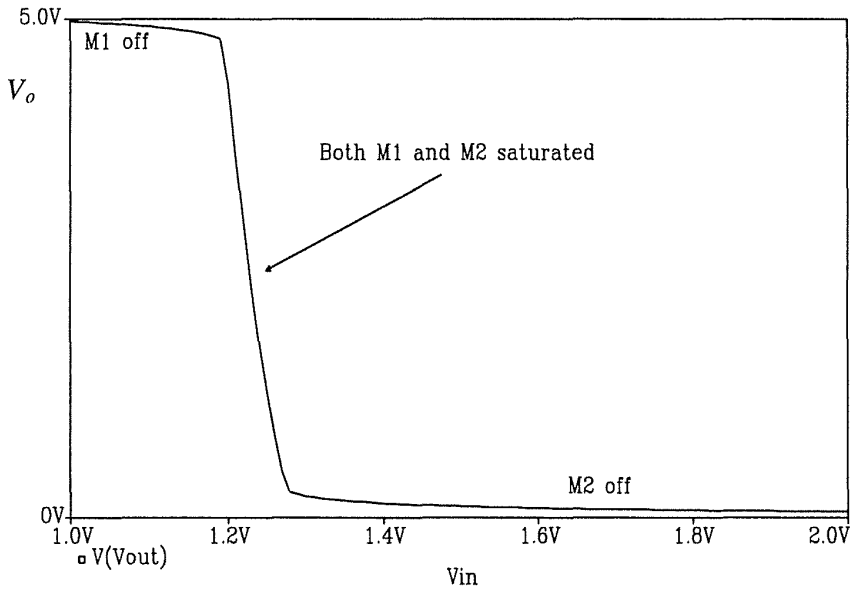


Figure 22.14 DC transfer characteristics for the amplifier shown in Fig. 22.11.

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a DC voltage on the input of the amplifier. A common feedback scheme used to bias the single-stage amplifier is to AC couple the input signal to the gate of M1 and to take the output signal from the drain of M2/M1. A large resistor is then placed between the output and the input. When the basic amplifier is designed properly, this forces M1 and M2 into the saturation region.

The resistance looking into the drain of M2 is simply the output resistance given by $r_{o2} \approx 1/\lambda I_D = 1/(0.6 \cdot 10\ \mu A) = 1.667\ M\Omega$. This is in parallel with the resistance looking into the drain of M1, which is also 1.667 MΩ, assuming both λs are 0.06 V^{-1}. If we follow the intuitive method discussed in the last section, the voltage gain of a common source amplifier is the total parallel resistance at the drain of M1 divided by the resistance in the source of M1, or

$$A_v = \frac{v_o}{v_i} = -\frac{r_{o1} \| r_{o2}}{\frac{1}{g_{m1}}} = -\frac{g_{m1}}{g_{o1} + g_{o2}} \tag{22.33}$$

It is of interest to determine how the DC bias current affects the small-signal gain. Making the appropriate substitutions into Eq. 22.33 we get

$$A_v = \frac{-\sqrt{2\beta_1 I_D}}{I_D(\lambda_1 + \lambda_2)} = \frac{-\sqrt{2\beta_1}}{(\lambda_1 + \lambda_2) \cdot \sqrt{I_D}} \tag{22.34}$$

This equation shows that the lower the bias drain current, the larger the gain. Figure 22.15 shows the voltage gain of this configuration (Fig. 22.13) plotted against the drain bias current. The gain levels off below about 0.1 μA because the MOSFETs enter the subthreshold region where both the transconductance and output resistance of the MOSFET are linearly dependent on the drain current (see Chs. 6 and 9).

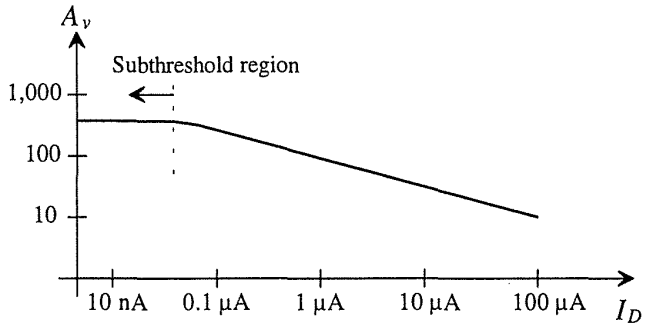


Figure 22.15 Voltage gain of common source amplifier with current source load plotted against biasing current.

The gain of the amplifier can be increased by using a cascode current load in place of M2. The resistance looking into the drain of the cascode current source/load is much larger than the output resistance of M1. This situation is sometimes referred to as the open circuit gain of a common source amplifier. The open circuit gain of M1 can be written as

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$$A_v = -\frac{r_{o1}}{\frac{1}{g_{m1}}} = -g_{m1} r_{o1} = -\frac{\sqrt{2\beta_1 I_D}}{I_D \lambda_1} \tag{22.35}$$

which increases the gain by a factor of two over the circuit of Fig. 22.13.

The frequency performance of the current source load amplifier is poorer than the gate-drain connected load amplifiers of the last section. Referring to Fig. 21.13, the drain of M1 and M2 is termed a high-impedance node, that is, a node with only drain connections. The effective resistance at this node to ground is $r_{o1} \| r_{o2}$. A node connected to the source of a MOSFET or a MOSFET with its drain and gate connected is termed a low-impedance node. The small-signal resistance looking into the source of a MOSFET and the small-signal resistance of the diode connected MOSFET are both $1/g_m$.

Example 22.5

Estimate the bandwidth of the amplifier shown in Fig. 22.13.

We begin by redrawing this schematic with the relevant capacitances included as shown in Fig. 22.16. We assume that the gate of M2 is connected to AC ground because of the low small-signal resistance of M3.

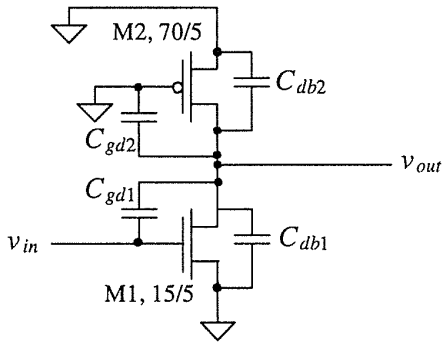


Figure 22.16 Fig. 22.13 with capacitances included.

The gain of the amplifier is

$$A_v = -g_{m1}(r_{o1} \| r_{o2}) = -\left[\sqrt{2 \cdot 50\frac{\mu A}{V^2} \cdot \frac{15}{5} \cdot 10\ \mu A}\right] \cdot (833k) = -46\ V/V$$

The MOSFET capacitances are now calculated. The gate-drain capacitance of the p-channel MOSFET M2 is given by

$$C_{gd2} = CGDO \cdot W_2 = 5 \times 10^{-10}\frac{F}{m} \cdot 70\ \mu m = 35\ fF$$

while the gate-drain capacitance of M1 is

$$C_{gd1} = CGDO \cdot W_1 = 3.8 \times 10^{-10}\frac{F}{m} \cdot 15\ \mu m = 5.7\ fF$$

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To calculate the worst-case depletion capacitances of the drain implants, we can assume zero potential across the junction and areas of 6 μm by the width of the MOSFET. The depletion capacitances are then given by

$$C_{db1} = CJ \cdot \overbrace{6\ \mu\text{m} \cdot W_1}^{\text{Area of drain}} = 1.0 \times 10^{-4} \frac{\text{F}}{\text{m}^2} \cdot 6\ \mu\text{m} \cdot 15\ \mu\text{m} = 9\ \text{fF}$$

and

$$C_{db2} = 3.25 \times 10^{-4} \cdot 6\ \mu\text{m} \cdot 70\ \mu\text{m} = 137\ \text{fF}$$

Note that because the gain is much higher than the gate-drain connected amplifier, the Miller capacitance that appears at the output, C_{MO}, is,

$$C_{MO} = C_{gd1}\left(1 + \frac{1}{46}\right) \approx C_{gd1}$$

and the output time constant becomes

$$\tau_{out} = (r_{o1} \| r_{o2}) \cdot (C_{gd2} + C_{gd1} + C_{db1} + C_{db2}) = 833\text{k} \cdot 187\ \text{fF} = 155.8\ \text{ns}$$

and the 3 dB frequency of this amplifier is given by

$$f_{out} = \frac{1}{2\pi \cdot \tau_{out}} = 1\ \text{MHz}$$

a significantly lower bandwidth than the amplifier of Ex. 22.2 with a correspondingly higher gain.

If this amplifier was driven from an identical stage with output resistance, $R_{out} = r_{o1} \| r_{o2}$, and capacitance, C_{out}, which is

$$C_{out} = (C_{gd2} + C_{gd1} + C_{db1} + C_{db2}) = 187\ \text{fF}$$

then the input time constant is given by

$$\tau_{in} = R_{out} \cdot [C_{gs1} + (1 + |A_v|)C_{gd1} + C_{out}]$$

where

$$C_{gs1} = \frac{2}{3} \cdot C'_{ox} \cdot W_1 \cdot L_1 = 40\ \text{fF}$$

and

$$\tau_{in} = 866k \cdot \left(40\ \text{fF} + \overbrace{(1+46)5.7\ \text{fF}}^{\text{Miller capacitance}} + 187\text{fF} \right) = 429\ \text{ns}$$

The input time constant is increased by the Miller effect across the gate-drain capacitance of M1 and the output capacitance of the driving circuit. The methods available to minimize the effect of the Miller capacitance will be explained in the section discussing the cascode connection. ■

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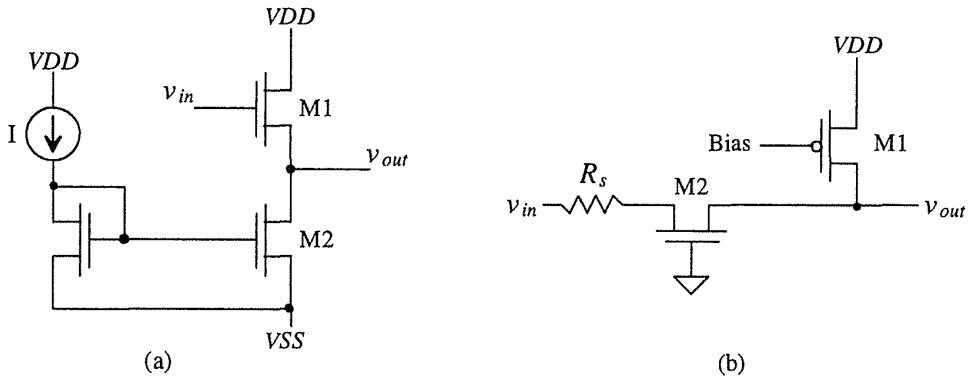


Figure 22.17 (a) Source follower and (b) common gate amplifier.

The source-follower configuration using a current source load is shown in Fig. 22.17a. Neglecting the body effect, we see that the voltage gain of the configuration is given by a voltage divider between the resistance looking into the source of M2 and the resistance looking into the drain of M1, or

$$A_v = \frac{v_o}{v_i} = \frac{r_{o2}}{r_{o2} + \frac{1}{g_{m1}}} = \frac{g_{m1} r_{o2}}{1 + g_{m1} r_{o2}} \approx 1 \qquad (22.36)$$

The output resistance is the parallel combination of the resistance looking into the source of M2 and the resistance looking into the drain of M1, or

$$R_o = \frac{1}{g_{m2}} || r_{o2} \qquad (22.37)$$

The common gate configuration using a current source load is shown in Fig. 22.17b. The resistance looking into the drain of M1 is r_{o1} while the resistance looking into the drain of M2 is $r_{o2}(1 + g_{m2} R_s)$. The resistance in the source of M2 is $R_s + \frac{1}{g_{m2}}$. Therefore, the gain of the common gate configuration using a current source load is

$$A_v = \frac{[r_{o1} || (r_{o2}(1 + g_{m2} R_s))]}{R_s + \frac{1}{g_{m2}}} \qquad (22.38)$$

It is important to realize that there are current sourcing/sinking limitations with current source loads. For example, the maximum current the source follower above can sink is the constant current supplied by M2. When the source follower is sourcing current to a load, it must also supply current to M2.

The amplifiers we have discussed so far in this chapter are class A amplifiers; that is, they conduct current over the entire range or cycle of a sinusoidal input signal. Class B amplifiers conduct over half of the cycle, while class AB amplifiers conduct over a range slightly greater than half a cycle. Most often in analog CMOS circuit design we are concerned with class A or AB amplifiers. Class B amplifiers are most

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often used for the generation of pulses. Usually we make no distinction between the "class" of an amplifier unless we are concerned with power dissipation. Output stages, the stages in a circuit used to drive an external load, are usually where the designer is interested in power dissipation and distortion (a term used to describe how well an amplifier reproduces a scaled version of the input signal). The source-follower circuit of Fig. 22.17(a) is an example of a class A output stage utilized in an op-amp design.

The power conversion efficiency of an amplifier is defined by

$$\% \text{ efficiency} = \frac{\text{Load power, } P_l}{\text{Supply power, } P_s} \times 100\ \% \tag{22.39}$$

If the source-follower above is driving a resistor, R_L, with an rms voltage v_{out}, then

$$P_l = \frac{(v_{out})^2}{R_L} \tag{22.40}$$

The power supplied to the amplifier can be specified by

$$P_s = I(VDD - VSS) \tag{22.41}$$

If $VDD = -VSS$ and the output voltage can swing up to VDD and down to VSS, then the maximum efficiency of the class amplifier occurs when

$$v_{out} = \frac{VDD}{\sqrt{2}} = IR_L \tag{22.42}$$

The maximum conversion efficiency of the class A amplifier is 25 percent.

22.2.1 The Cascode Connection

The basic cascode amplifier is shown in Fig. 22.18a. This amplifier has two advantages over the basic common source amplifier with current source load discussed previously; the gain is greater due to the large output resistance, and the absence of the Miller capacitance keeps the input time constant from becoming long. Biasing of the cascode amplifier will be discussed in Ch. 24 in conjunction with diff-amp design.

The small-signal model for the basic amplifier is seen in Fig. 22.18b. The gain from v_{in} to the drain of M1, v_{d1}, can be found by

$$A_{v1} = \frac{v_{d1}}{v_{in}} = \frac{-i_d \cdot (r_{ins2} || r_{o1})}{i_d \cdot \frac{1}{g_{m1}}} \tag{22.43}$$

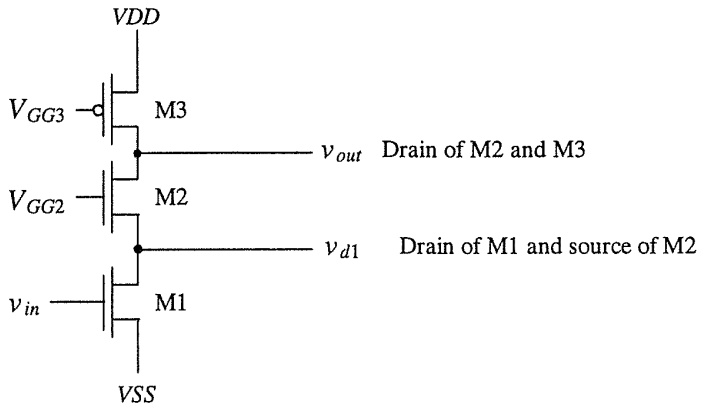
where r_{ins2} is the small-signal resistance seen looking into the source of M2. Since the drain of M2 is not on AC ground, it cannot be assumed that $r_{ins2} = 1/g_{m2}$. If a test source is applied as seen in Fig. 22.19, the following equations may be written:

$$i_t = -(g_{m2}v_{gs2} - g_{mb2}v_{sb2} + \frac{v_o - v_t}{r_{o2}}) = g_{m2}v_t - g_{mb2}v_t + \frac{v_t - v_o}{r_{o2}} \tag{22.44}$$

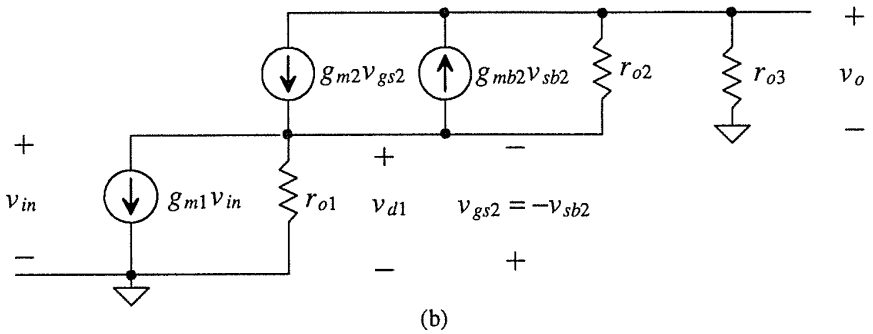
$$v_o = i_t r_{o3} \tag{22.45}$$

Therefore, r_{ins2} is

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(a)



(b)

Figure 22.18 (a) Cascode amplifier and (b) small-signal model.

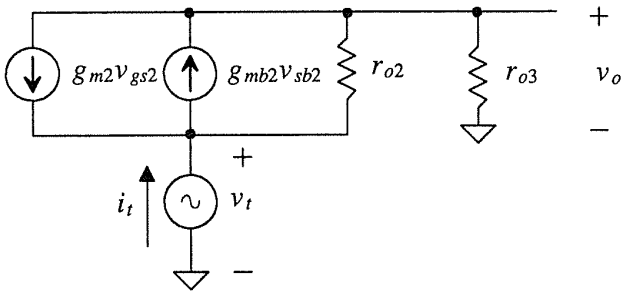


Figure 22.19 Small-signal model used for finding the impedance looking into the source of M2.

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$$r_{ins2} = \frac{v_t}{i_t} = \frac{1 + \frac{r_{o3}}{r_{o2}}}{g_{m2} + g_{mb2} + \frac{1}{r_{o2}}} \approx \frac{1}{g_{m2}}(1 + \frac{r_{o3}}{r_{o2}}) \tag{22.46}$$

and the gain, A_{v1}, becomes,

$$A_{v1} = \frac{v_{d1}}{v_{in}} \approx -g_{m1}\left[\frac{1}{g_{m2}}\left(1 + \frac{r_{o3}}{r_{o2}}\right) || r_{o1}\right] \approx -\frac{g_{m1}}{g_{m2}}\left(1 + \frac{r_{o3}}{r_{o2}}\right) \tag{22.47}$$

The gain of the common gate stage, M2, with current source load M1 is

$$A_{v2} = \frac{v_{out}}{v_{d1}} = \frac{\overbrace{-i_d \cdot r_{o2}(1 + g_{m2}r_{o1})}^{\text{R into drain of M2}} || r_{03}}{-i_d \cdot \frac{1}{g_{m2}}(1 + \frac{r_{o3}}{r_{o2}})} = g_{m2} \cdot \frac{[(r_{o2}(1 + g_{m2}r_{o1})) || r_{o3}]}{(1 + \frac{r_{o3}}{r_{o2}})} \tag{22.48}$$

The overall gain is the product of A_{v1} and A_{v2} given by

$$A_v = A_{v1} \cdot A_{v2} = -g_{m1} \cdot [(r_{o2}(1 + g_{m2}r_{o1})) || r_{o3}] \approx -g_{m1}r_{o3} \tag{22.49}$$

which is not much of a gain improvement over the basic current source amplifier. The output resistance of M3 limits the gain. Figure 22.20 shows a configuration for increasing the resistance looking into the drain of M3. The MOSFETs M3 and M4 form a cascode current source load. The output resistance is the parallel combination of the resistance looking into the drain of M3 with the resistance looking into the drain of M2. This parallel combination can be written as

$$R_o = [r_{o2}(1 + g_{m2}r_{o1})] || [r_{o3}(1 + g_{m3}r_{o4})] \tag{22.50}$$

and the gain is

$$A_v = -g_{m1} \cdot R_o \tag{22.51}$$

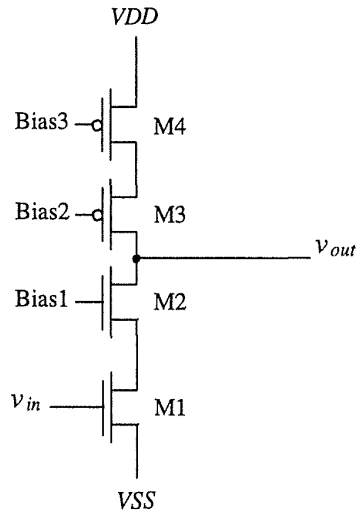


Figure 22.20 Dual cascode amplifier.

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The frequency response of the cascode illustrates another advantage of the configuration. Assume that the cascode amplifier is being driven by a circuit with an output resistance and capacitance, R_{L1} and C_{L1}, respectively. Applying Miller's Theorem to the circuit shown in Fig. 22.18a, the high-frequency small-signal model for the cascode can be seen in Fig. 22.21. Note that the capacitance C_2 and C_3 represent the lumped capacitance to ground at those nodes whose values are

$$C_2 = C_{bd1} + C_{bs2} + C_{gs2} + C_{gd1}\left(1 + \frac{1}{|A_{v1}|}\right) \tag{22.52}$$

$$C_3 = C_{gd2} + C_{bd2} + C_{bd3} + C_{gd3} + C_L \tag{22.53}$$

where C_L is the capacitance of any load attached to the output. The input capacitance, C_1, becomes

$$C_1 = C_{gs1} + C_{L1} + C_{gd1}(1 + |A_{v1}|) = C_{gs1} + C_{L1} + C_{gd1}\left[1 + \frac{g_{m1}}{g_{m2}}\left(1 + \frac{r_{o3}}{r_{o2}}\right)\right] \tag{22.54}$$

Notice that the Miller capacitance that appears at the input is much smaller compared to the simple common source amplifier with a current source load case. This is simply because the gain, v_{d1}/v_{in} is very small. Therefore, the Miller capacitance no longer dominates the time constant associated with the input. The time constants become

$$\tau_{in} = R_{L1} \cdot (C_{L1} + C_1) \tag{22.55}$$

$$\tau_{out} = r_{o3} \cdot C_3 \tag{22.56}$$

and the time constant associated with node A is

$$\tau_A = \left[\frac{1}{g_{m2}}\left(1 + \frac{r_{o3}}{r_{o2}}\right) || r_{o1}\right] \cdot C_2 \tag{22.57}$$

Note that the input time constant, τ_{in}, and the output time constant, τ_{out}, are roughly the same order of magnitude assuming that the cascode is driving another stage with an input capacitance of the same order of magnitude. The time constant associated with

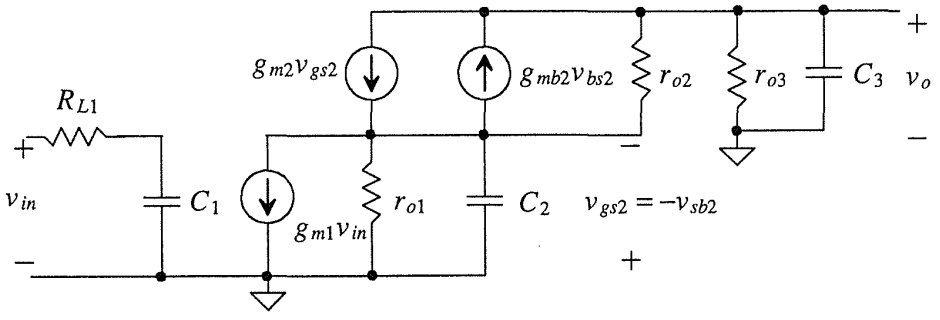


Figure 22.21 High-frequency equivalent circuit for the cascode amplifier.

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node A, τ_A, will be somewhat negligible since it has such a low impedance to ground and contributes little to the overall frequency response.

One drawback to using the cascode connection is the reduction in output voltage swing. Since there are more transistors in the circuit, more of the supply voltages will be required to keep the devices in saturation. Again, referring to Fig. 22.18a, the maximum output voltage that will keep all the devices in saturation will be limited by the point at which M2 becomes nonsaturated. This occurs when

$$V_{GS2} - V_{THN2} = V_{DS2} \tag{22.58}$$

or when

$$V_{o(\min)} = V_{GG2} - V_{THN2} \tag{22.59}$$

One might wonder why M2 will become nonsaturated before M1. Since the impedance at the output node is much greater than the impedance of node v_{d1}, the voltage at the output will be decreasing at a much faster rate than the voltage at node v_{d1}. This is equivalent to saying that since the gain from the input to the output is much greater than the gain from the input to node v_{d1}, as the input voltage rises, the voltage, v_o, will decrease faster than the voltage at v_{d1}.

The maximum positive voltage that can appear at the output of the cascode while maintaining all transistors in saturation will be limited by the point at which M3 becomes nonsaturated. Applying the same reasoning as before, we find that the maximum positive output voltage occurs when

$$v_{SG} - V_{THP3} = v_{SD} \tag{22.60}$$

or

$$v_o(\max) = V_{GG3} + V_{TH3} \tag{22.61}$$

So the values of the bias voltages become very critical when considering output swing.

22.2.2 The Push-Pull Amplifier

The push-pull amplifier shown in Fig. 22.22 is the inverter discussed in Ch. 11 operating with both M1 and M2 in the saturation region. This configuration, when designed properly, can sink and source equal amounts of current. Both M1 and M2 act as common source amplifiers. The effective resistance at the drains of these transistors to AC ground is the parallel combination of each MOSFET's output resistance. The resistance in the sources of M1 and M2 is the parallel combination of the resistance seen looking into the source of M1 and M2. The gain of this configuration is then

$$A_v = \frac{-i_d \cdot (r_{o1} || r_{o2})}{i_d \cdot \left(\frac{1}{g_{m1}} || \frac{1}{g_{m2}}\right)} = -(g_{m1} + g_{m2}) \cdot (r_{o1} || r_{o2}) \tag{22.62}$$

The push-pull amplifier is popular as an output amplifier because of equal source and sink capability and the ability to pull the output to *VDD* or *VSS*. Figure

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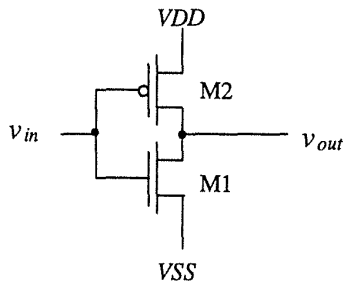


Figure 22.22 The push-pull amplifier.

22.23 shows a configuration that sets the gain of the amplifier to unity. The push-pull configuration is used as a buffer in this schematic; that is, it provides current drive capability. Error amplifiers are used to sense and compare the output voltage and then adjust the gate drive of M1 and M2. Another benefit of this arrangement is that the output resistance of the amplifier is reduced. This is desirable when the amplifier is used as a buffer in op-amp applications. In practice, this configuration has several practical problems, for example, design of the error amplifiers for maximum power conversion efficiency, stability, and crossover distortion when operated class B.

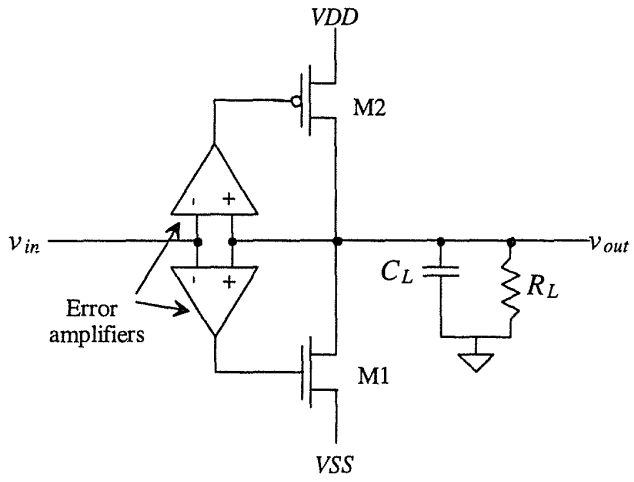


Figure 22.23 Using the push-pull amplifier as a unity gain buffer.

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22.3 Noise and Distortion in Amplifiers

Noise

Let's consider the noise performance of the common source amplifier with the current source load shown in Fig. 22.13 and in simplified form in Fig. 22.24a. In our noise analysis, we will neglect the noise contributions of the devices connected to the gate of M2. Figure 22.24b shows the circuit with the noise sources added. Following the procedure of Ch. 7 with the noise models of Ch. 9, the sum of each mean squared contribution is equal to the mean squared output noise given by

$$\overline{v_T^2} = (r_{o1} \| r_{o2} \| \frac{1}{j\omega C_t})^2 \cdot (\overline{i_{1/f,1}^2} + \overline{i_{1/f,2}^2} + \overline{i_{therm,1}^2} + \overline{i_{therm,2}^2}) \tag{22.63}$$

where C_t is the sum of the capacitances in parallel with r_{o1} and r_{o2}. The RMS output noise over a given bandwidth is

$$\sqrt{\overline{v_{on}^2}} = \left[\int_{f_L}^{f_H} \overline{v_T^2} \cdot df \right]^{1/2} \tag{22.64}$$

For low frequencies the gain of this amplifier is $-g_{m1} \cdot (r_{o1} \| r_{o2})$, so the squared magnitude of the transfer function is

$$|H(j\omega)|^2 = \frac{(g_{m1}(r_{o1} \| r_{o2}))^2}{\left[1 + \left(\frac{f}{f_{in}}\right)^2\right]\left[1 + \left(\frac{f}{f_{out}}\right)^2\right]} \tag{22.65}$$

while the RMS input noise is

$$\sqrt{\overline{v_{ino}^2}} = \left[\int_{f_L}^{f_H} \frac{\overline{v_T^2}}{|H(j\omega)|^2} \cdot df \right]^{1/2} \tag{22.66}$$

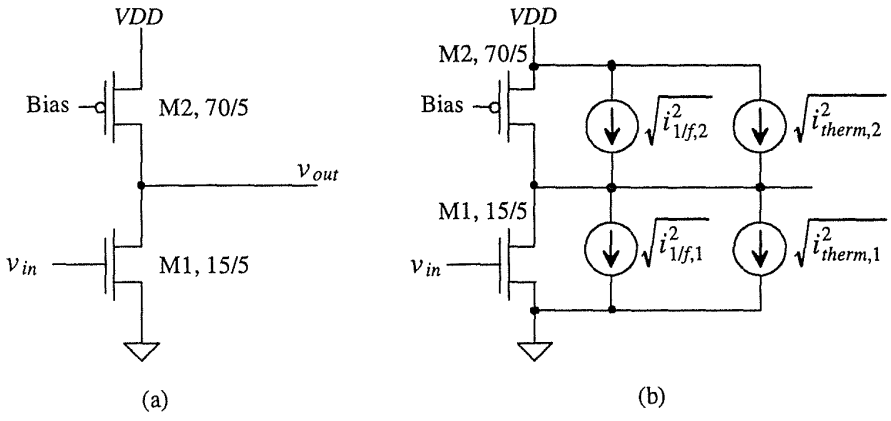


Figure 22.24 (a) Common source amplifier with current source load and (b) with noise sources included.

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Distortion

Consider how well this amplifier, Fig. 22.24a, produces a scaled version of the input on its output. Ideally, the output of the amplifier is related to the input by a constant A_v, the voltage gain. The gain for this amplifier is given by

$$|A_v| = g_m(r_{o1} \| r_{o2}) \Rightarrow \sqrt{2\beta_1(I_D + i_d)} \cdot \frac{1}{2\lambda(I_D + i_d)} = \frac{\sqrt{2\beta_1}}{2\lambda\sqrt{I_D + i_d}} \quad (22.67)$$

Normally, the AC component of the drain current, i_d, is assumed to be much less than the DC component of the drain current, I_D, and the amplifier gain is essentially constant (small-signal aproximation). If the AC component is comparable to the DC component, noticeable distortion results. The voltage gain for large inputs is dependent on the input signal amplitude.

Characterizing an amplifier begins by applying a pure single-tone sinusoid of the form

$$V_{in}(t) = V_p \sin \omega t \quad (22.68)$$

to the input of the amplifier. The output of the amplifier is a series of tones at an integer multiple of the input tone given by

$$V_{out}(t) = a_1 V_p \sin(\omega t) + a_2 V_p \sin(2\omega t) + \cdots + a_n V_p \sin(n\omega t) \quad (22.69)$$

The magnitude of the fundamental or wanted signal is $a_1 V_p$. Ideally, a_2 through a_n are zero, and the amplifier is free of distortion. The nth term harmonic distortion is given by

$$HD_n = \frac{a_n}{a_1}, \text{ for } n > 1 \quad (22.70)$$

The total harmonic distortion (THD) is given by

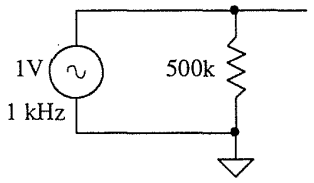
$$\text{THD} = \sqrt{\frac{a_2^2 + a_3^2 + a_4^2 + \cdots + a_n^2}{a_1^2}} \quad (22.71)$$

Output buffers, amplifiers used to drive a large load capacitance or low resistance, are examples of amplifiers where low THD is important. If the output amplifier is biased so that the DC component of the drain current is large compared to the transient or time-varying current, the buffer dissipates too much power for most applications. Therefore, in almost all situations, the biasing current in an output buffer is comparable, or even smaller for class B operation than the time-varying current. We reduce the distortion by employing feedback around the amplifier (see Ch. 23). If the open-loop gain of an op-amp varies from 1,000 to 10,000 depending on the amplitude of the input signal, then the feedback around the amplifier reduces the gain sensitivity. In fact, it is nearly impossible to design a linear output amplifier with low distortion without the use of feedback.

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Modeling Distortion with SPICE

SPICE can be used to simulate distortion using a transient analysis and the .FOUR (Fourier) statement [5]. The general form of this statement is .FOUR FREQ OVl <OV2 OVI . . . where FREQ is the frequency of the fundamental and OV1 . . . are the outputs of the circuit (the voltage or current outputs for which SPICE will calculate distortion). As a simple example, consider the circuit and netlist shown in Fig. 22.25. The input sine wave must have at least one full period for the .FOUR statement to calculate distortion. If more than one period is used, SPICE will use the output over the last full period. Also, the maximum transient step size should be less than the period of the input divide by 100. For the example of Fig. 22.25 with a 1 kHz input (a period of 1 ms), the maximum print size should be 10 μs.




```
*** Top Level Netlist ***
.four 1k V(1)
R1 1 0 500k
V1 1 0 DC 0 AC 0 0 SIN(0 1 1khz 0 0)
.tran 10u 2m 0 10u
.end
```

Figure 22.25 Simple circuit to demonstrate the use of the .FOUR statement.

The resulting simulation output is as follows.

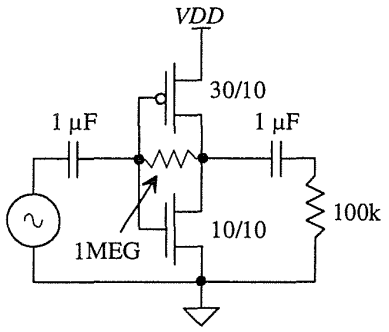
```
Fourier analysis for v(1):
  No. Harmonics: 10, THD: 3.17012e-006 %, Gridsize: 200, Interpolation Degree: 1
```

Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
0	0	-5.602e-009	0	0	0
1	1000	0.999632	-9e-6	1	0
2	2000	1.12039e-008	-86.4	1.12e-8	-86.4
3	3000	1.12039e-008	-84.6	1.12e-8	-84.6
4	4000	1.12039e-008	-82.8	1.12e-8	-82.8
5	5000	1.12039e-008	-81	1.12e-8	-81
6	6000	1.12039e-008	-79.2	1.12e-8	-79.2
7	7000	1.12039e-008	-77.4	1.12e-8	-77.4
8	8000	1.12039e-008	-75.6	1.12e-8	-75.6
9	9000	1.12039e-008	-73.8	1.12e-8	-73.8

Notice that, as we would expect, this circuit's output doesn't show any harmonic distortion. SPICE calculates the magnitude and phase of the first nine harmonics and DC. Also note that SPICE automatically calculates the THD for a circuit.

As a more practical example, consider the push-pull amplifier shown in Fig. 26.26. This circuit is biased so that the DC voltage on the gates of the MOSFETs is the same as the DC voltage on the drains (both MOSFETs are in saturation). The 100kΩ resistor simulates the effects of a load (and keeps the output coupling capacitor from floating).

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```
*** Top Level Netlist ***
.four 1MEG V(4)
C1 5 3 1u
C2 4 1 1u
M1 1 5 0 0 CMOSNB  L=10u W=10u
M2 1 5 6 6 CMOSPB  L=10u W=30u
R1 1 5 1MEG
R2 0 4 1MEG
V1 3 0 DC 0 AC 0 0 SIN(0 10m 1MEG 0 0)
VDD 6 0 DC 5 AC 0 0
(SPICE MOSFET models not shown)
.tran 10n 1u 0 10n
.end
```

Figure 22.26 Determining distortion in a push-pull amplifier.

The calculated THD will be a strong function of the input signal amplitude. Let's begin by simulating the circuit with a 10 mV input signal. The resulting SPICE output gives a THD of 0.18 percent. If the input amplitude is increased to 100 mV, the THD becomes 1.6 percent.

22.3.1 Modeling Amplifier Noise

Figure 22.27 shows how the input and output RMS noise sources are added to a noiseless amplifier. The signal to noise ratio (*SNR*) of an amplifier is defined by

$$SNR_{in} = 10\log\frac{v_{in}^2}{\overline{v_{ino}^2}} \tag{22.72}$$

where v_{in}^2 is the square of the RMS input signal and

$$SNR_{out} = 10\log\frac{v_{out}^2}{\overline{v_{on}^2}} \tag{22.73}$$

for the *SNR* on the output of the amplifier. The *SNR* is used to compare signal levels to amplifier noise levels. A *SNR* of 0 dB means that the squared RMS input (or output) signal is equal to the mean squared noise present on the input (or output) of an amplifier.

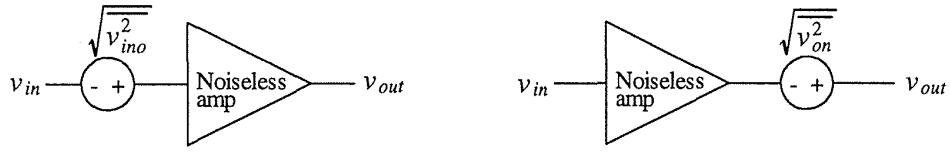


Figure 22.27 Addition of RMS noise voltages to the input or output of an amplifier.

Now consider the practical situation shown in Fig. 22.28 of the amplifier being driven by a voltage source with a source resistance R_s. The source resistance generates

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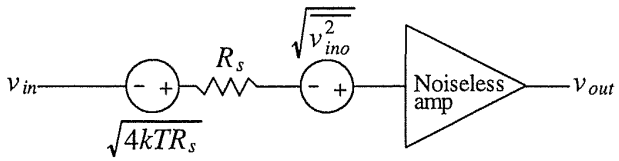


Figure 22.28 Determination of the noise figure of an amplifier.

thermal noise with a mean squared amplitude of $4kTR_s$. We can define the noise figure (*NF*) of an amplifier as the ratio of the output of a noisy amplifier with the source resistor connected over the output of a noise-free amplifier with the noisy source resistor connected. This can be written as

$$NF = 10\log\left[\frac{|H(j\omega)|^2 \cdot \left(4kTR_s + \overline{v_{ino}^2}\right)}{|H(j\omega)|^2 \cdot (4kTR_s)}\right] \tag{22.74}$$

or

$$NF = 10\log\left[\frac{4kTR_s + \overline{v_{ino}^2}}{4kTR_s}\right] \tag{22.75}$$

The *NF* is a useful figure to compare the relative noise performance of amplifiers. *NF* varies with source resistance and bandwidth and is usually specified using contours of constant *NF* versus frequency or source resistance. We have assumed in this derivation that the source impedance is much smaller than the input resistance of the amplifier, so that the RMS input signal to the amplifier is v_{in}. A voltage divider between source resistance and amplifier input resistance is used when this is not the case. The input SNR can be calculated, at a given source resistance, by

$$SNR_{in} = 10\log\frac{v_{in}^2}{\overline{v_{ino}^2} + 4kTR_s} = 10\log\frac{v_{in}^2}{4kTR_s} - NF \tag{22.76}$$

Sometimes the noise of an amplifier is specified using the noise temperature, T_n, instead of the NF. Consider the amplifier shown in Fig. 22.29a with the source resistance at T = 0 °K. The amplifier input RMS noise voltage is $\sqrt{\overline{v_{ino}^2}}$. Now consider the circuit shown in Fig. 22.29b where the amplifier is noiseless, $\sqrt{\overline{v_{ino}^2}} = 0$. We increase the temperature of the resistor until the thermal noise from the resistor is equal to $\sqrt{\overline{v_{ino}^2}}$. The temperature of the resistor at this point is labeled T_n for the noise temperature. We can relate the noise temperature to NF by first rewriting Eq. (22.75) as

$$NF = 10\log\left[1 + \frac{\overline{v_{ino}^2}}{4kTR_s}\right] \tag{22.77}$$

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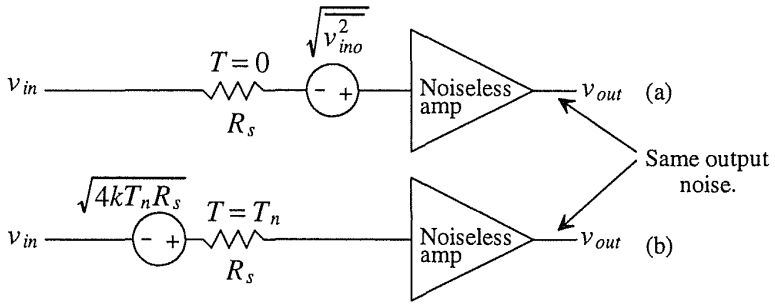


Figure 22.29 Determination of the noise temperature of an amplifier.

The mean squared input noise in Fig. 22.29b is given by

$$\overline{v_{ino}^2} = 4kT_nR_s = 4kTR_s[10^{NF/10} - 1] \tag{22.78}$$

or the noise temperature in terms of the NF is given by

$$T_n = T(10^{NF/10} - 1) \tag{22.79}$$

where the noise figure, NF, is in dB and T is the temperature in kelvin at which the NF was measured. The NF can also be written in terms of the noise temperature as

$$NF = 10\log\left(\frac{T_n}{T} + 1\right) \tag{22.80}$$

22.4 A Class AB Amplifier

Consider the class A common source amplifier shown in Fig. 22.30. We know that the maximum efficiency of this amplifier is 25 percent. In this section, we are interested in the large-signal performance of the amplifier. We know that M1 can only sink current from the load capacitance and the current source I sources current to the load capacitance. The maximum rate at which the load capacitance can be charged is called the slew rate (SR) and is given by

$$SR = \frac{I}{C_L} = \frac{dV}{dt} \tag{22.81}$$

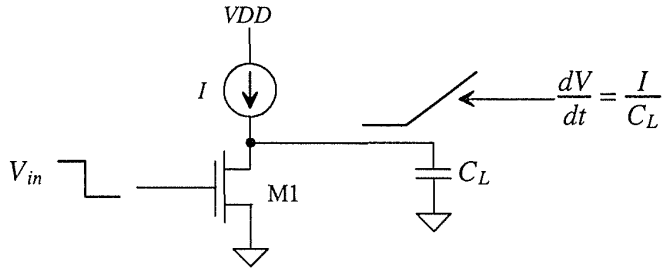


Figure 22.30 Common source amplifier with current source load.

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If I is 10 μA and C_L is 1 pF, then the slew rate of the amplifier is 10 V/μs. In many analog or digital applications, this rate of change may be too slow. Usually the capacitance is not a variable available to the design engineer, and increasing the current I results in greater power dissipation. Designing an amplifier that eliminates the current source limitations in charging or discharging the load capacitance is desirable.

Consider the amplifier configuration shown in Fig. 22.31. The value of the batteries determines the class (A, B, or AB) of the amplifier. When the input goes positive, V_{GS2} will increase while V_{SG1} will decrease. This causes the current in M2 to increase and the current in M1 to decrease. The magnitude of the input voltage when M1 turns off is determined by VGG1. This configuration does not exhibit output slew-rate limitations due to the absence of a current source in series with the charging or discharging path. The output voltage swing is limited to a threshold voltage below *VDD* and above *VSS*.

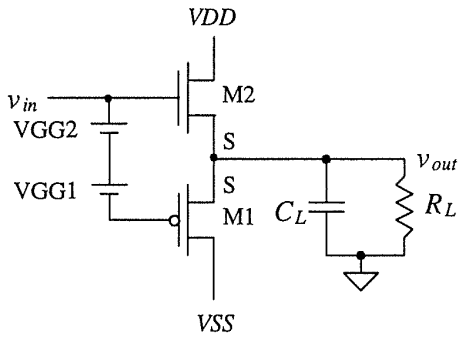


Figure 22.31 Implementation of a class AB (or class B) amplifier.

The floating batteries in Fig. 22.31 can be implemented with the circuit shown in Fig. 22.32. The gate of M6 is biased with a DC voltage so that its DC drain current is equal to the DC current through M3. MOSFET M3 is simply a current source. The gate-source voltages of M4 and M5 are constant (because of the constant current provided by M3) and used as the biasing voltage needed to bias M1 and M2 on. This configuration is useful as an output buffer in an op-amp when the gate of M6 is connected to an active load used in a differential pair and the gate of M3 is connected to the same bias voltage as used in the diff-amp current source.

A class AB amplifier based on a floating current source is shown in Fig. 22.33 [6]. The current source in this figure is used to set the DC current flowing in the MOSFETs. Keeping in mind that the input current, i_{in}, can be negative or positive (i.e., flow into or out of the circuit), an increase in i_{in} causes V_{SG4} to decrease (causing M6 to source less current) and V_{GS1} to increase (causing M1 to sink more current). The output voltage of this circuit can swing from *VDD* to *VSS*; thus, this configuration finds extensive use in low-voltage design.

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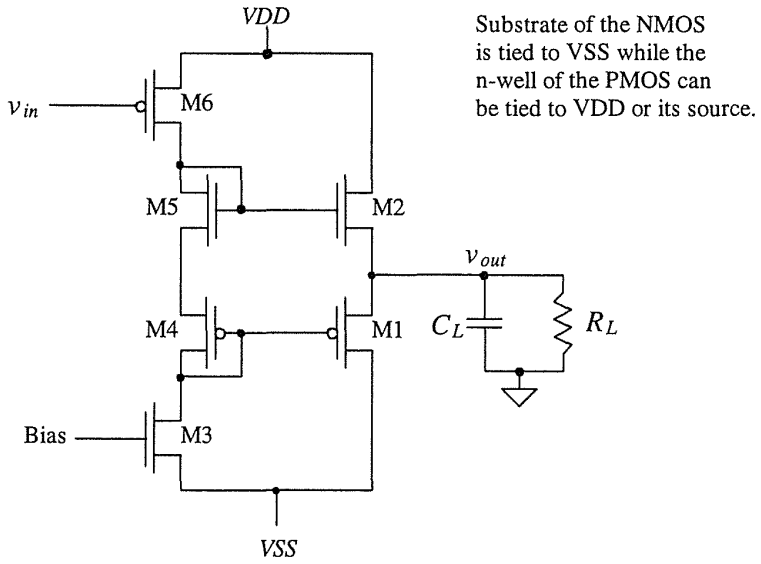


Figure 22.32 Practical implementation of a class AB amplifier in a complementary source-follower configuration.

The circuit shown in Fig. 22.34 is another implementation of a class AB amplifier useful in driving capacitive loads (a load resistor kills the gain of this amplifier). The schematic block symbol, an op-amp with the noninverting terminal grounded, is also shown in this figure. Let's begin the analysis of this amplifier by determining the DC operating point with input, v_{in}, grounded. Let's also assume that all n- and p-channel MOSFETs in this figure are the same size, say, 15/5 for the NMOS and 70/5 for the PMOS. If this is true, then the bias voltages generated by M13 through

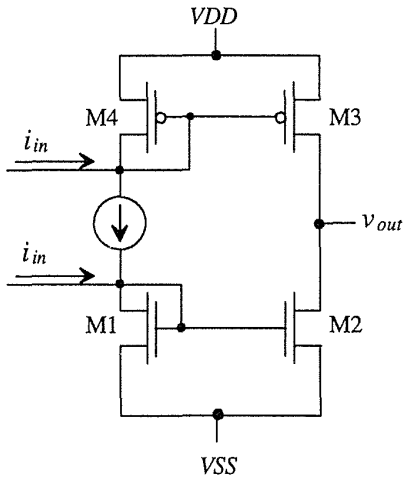


Figure 22.33 Class AB amplifier using floating current sources.

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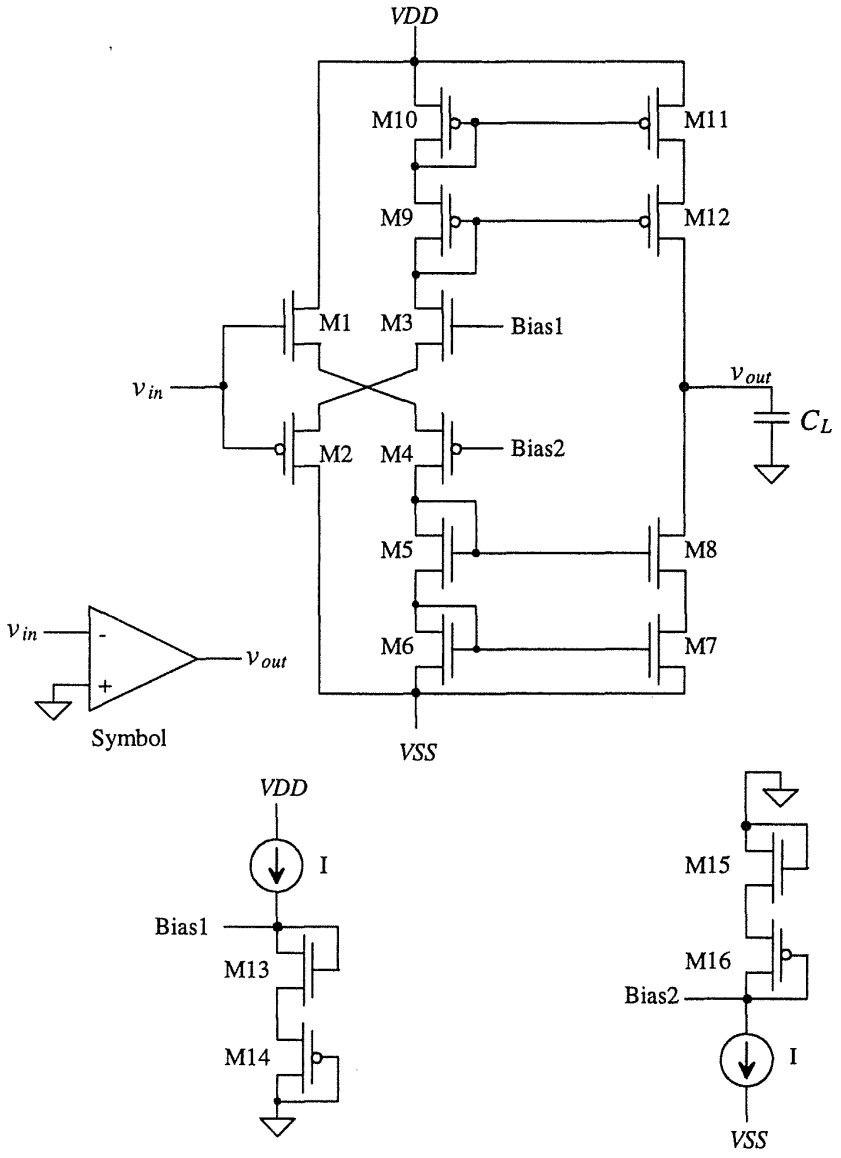


Figure 22.34 Implementation of a class AB amplifier.

M16 force a current I to flow in all remaining MOSFETs. If output driver MOSFETs M7, M8, M11, and M12 are K times larger than M5, M6, M9, and M10, then a current $K \cdot I$ flows in these output MOSFETs. Sizing the output transistors is useful if larger-current drive capability is needed. The open-loop gain of this amplifier is given by

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$$A_v = -\frac{g_{m12}r_{o12}r_{o11} \| g_{m7}r_{o7}r_{o8}}{\frac{1}{g_{m1}} + \frac{1}{g_{m4}}} \tag{22.82}$$

This type of amplifier is sometimes called an operational transconductance amplifier (OTA) and finds use in sampled data circuits where analog data are stored on a capacitor.

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[3] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits,* 3rd ed., John Wiley and Sons, 1993. ISBN 0-471-57495-3.

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[5] P. W. Tuinenga, *SPICE - A Guide to Circuit Simulation and Analysis Using PSPICE,* 3rd ed., Prentice Hall, 1995. ISBN 0-13-436049-4.

[6] R. Hogervorst, K. J. de Langen, and J. H. Huijsing, *1.1.2 Low-Power Low-Voltage VLSI Operational Amplifier Cells,* 1996 ISCAS Tutorials.

PROBLEMS

22.1 Show that the gate-drain connected MOSFET shown in Fig. P22.1 behaves like a small-signal resistor of value $1/g_m$.

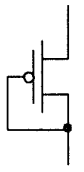


Figure P22.1

22.2 Using small-signal models, verify that the gain given in Ex. 22.1 is correct.

22.3 Verify Miller's Theorem using the amplifier configuration shown in Fig. P22.3a.

22.4 Consider the schematic of a two-MOSFET amplifier shown in Fig. P22.4. Determine the following:

a. The DC voltages and currents.

b. The small-signal low-frequency gain.

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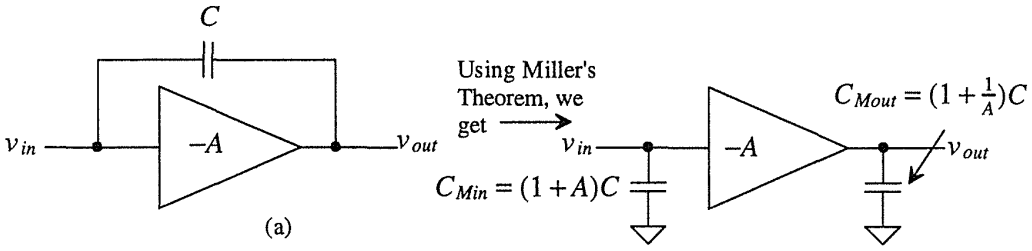


Figure P22.3

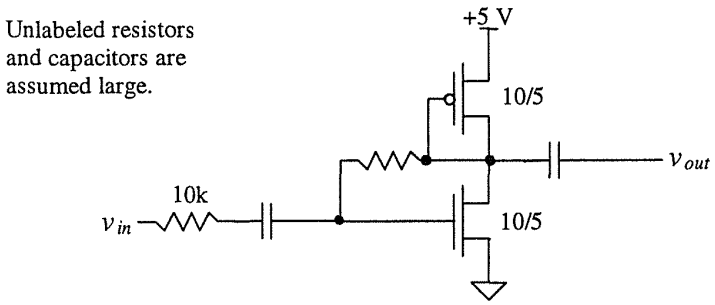


Figure P22.4

c. C_{sg2}, C_{db2}, C_{gd1}, C_{gs1}, and C_{db1}. Assume that the areas of the drains and sources of the MOSFETs measure 6 μm by 10 μm.

d. The frequency response.

e. The location of the zero in the amplifier frequency response.

22.5 This problem investigates how the body effect influences the gain of the source-follower amplifier. Consider the source follower shown in Fig. P22.5. Show that the gain of this configuration, assuming an ideal current sink, is given by

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{g_m + g_{mb}} = \frac{1}{1+\eta}$$

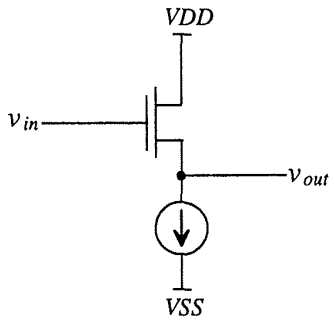


Figure P22.5

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22.6 Show that if we include the body effect in the derivation of the resistance looking into the drain of the MOSFET with source resistance shown in Fig. 22.9, the resistance becomes

$$R_o \approx [1+(1+\eta)g_m R]\cdot r_o$$

22.7 For the amplifiers shown in Fig. P22.7 derive the small-signal voltage gains using small-signal models. Assume that the MOSFETs used in these amplifiers are biased in the saturation region.

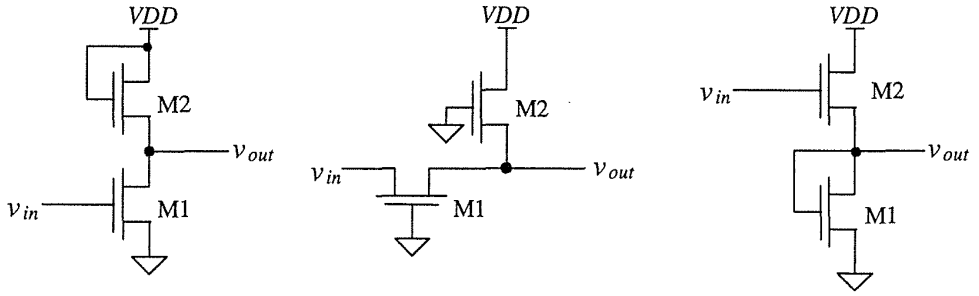


Figure P22.7

22.8 Estimate the small-signal voltage gain of the amplifier shown in Fig. 22.13 assuming that both M1 and M2 are biased in the saturation region.

22.9 Repeat Problem 4 for the amplifier shown in Fig. P22.9.

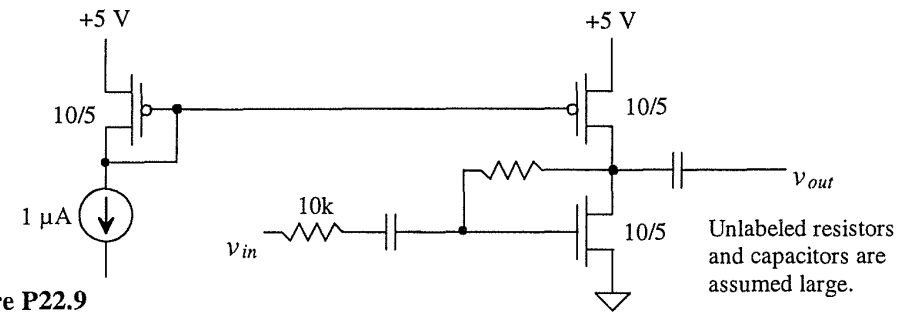


Figure P22.9

22.10 With respect to Fig. 22.17a, what is the small-signal resistance looking into the source of M1? the drain of M2? What is the small-signal resistance from the gate of M2 to ground?

22.11 Verify that Eq. (22.51) is correct. With respect to Fig. 22.20, what is the small-signal resistance looking into the drain of M4 (in terms of g_{mn}, g_{mp}, and r_{on} and r_{op})? the source of M3? the drain of M3? the source of M2? the drain of M1? the drain of M2? the total small-signal resistance at the output (the drains of M2 and M3)?

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22.12 Repeat Problem 11 (calculating the actual numbers) if 5 μA of current flows in the MOSFETs of Fig. 22.20. Assume all MOSFETs measure 50/5.

22.13 Using the small-signal models, verify that Eq. (22.62) is correct.

22.14 For the amplifier section shown in Fig. P22.14, estimate the minimum and maximum voltages allowable on the output in order to keep all MOSFETs in the saturation region.

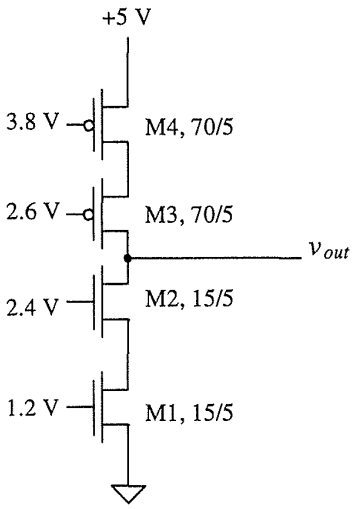


Figure P22.14

22.15 Assume that the amplifier of Fig. P22.9 is driving a 10 pF load capacitor. What is the maximum rate the load capacitance can be charged (what is the slew rate)? Is there a slew-rate limitation for discharging the capacitor?

22.16 For the circuit shown in Fig. P22.16, use SPICE to plot the output voltage against the input voltage. What limits the minimum and maximum output voltage swing? Also plot the current through M1 and M2 against the input voltage.

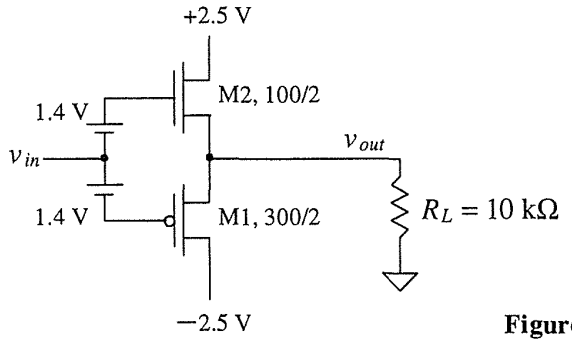


Figure P22.16

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Chapter

23

Feedback Amplifiers

Feedback is a very powerful concept and has numerous applications. Examples of feedback systems abound in everyday life. For example, the thermostat on an air conditioner unit uses feedback to maintain a comfortable temperature within a room. Similiarly, our bodies use feedback to increase antibodies to fight off an infection. By definition, feedback is the process of combining the output of a system with its input. In the air conditioner example, the temperature of the room is considered to be the output of the system, and the temperature set on the thermostat, the system input. The thermostat subtracts the value of the room temperature from the input value. If the temperature in the room is higher than the temperature set on the thermostat, the air conditioner turns on until the temperature in the room is less than or equal to the desired set value.

Thus, it can be said that feedback stabilizes a system. However, not all types of feedback have this property. There are two types of feedback: positive and negative. Negative feedback stabilizes, while positive feedback has the opposite effect. A good example of positive feedback is when a microphone is held too closely to the speaker of a public address (PA) system. More than likely, most people have heard the loud ringing that occurs. The positive feedback causes the system to become unstable, and the undesired effect is clearly recognizable.

Positive feedback occurs when the system output is added to the system input, whereas negative feedback occurs when the system output is subtracted from its input. For our purposes in this chapter, only negative feedback will be considered. While positive feedback can be useful if controlled, its applications will be discussed in a later chapter. However, methods for minimizing positive feedback effects will be discussed here.

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23.1 The Feedback Equation

Consider the feedback system shown in Fig. 23.1. The variables used in this diagram are labeled as an x value because they may be either a voltage or a current. The input signal, x_s, and the output signal x_o, may be either a voltage or a current. However, the feedback signal, x_f, must be the same type of signal as the input signal. If the input signal is a voltage, then the feedback signal must also be a voltage.

The block A_{OL} represents an amplifier's open-loop gain and is frequency dependent. The input to the amplifier, x_i, is the difference in the input source signal and the feedback signal, or

$$x_i = x_s - x_f \tag{23.1}$$

and the output is given by

$$x_o = A_{OL}(j\omega) \cdot (x_s - x_f) \tag{23.2}$$

In the following discussion, we will assume that all components of the system are ideal, meaning that the feedback network, β, will not load the amplifier. The specifications for the system can then be defined as follows:

$$A_{OL} = \frac{x_o}{x_i} \tag{23.3}$$

The *feedback factor*, β, is defined as

$$\beta = \frac{x_f}{x_o} \tag{23.4}$$

and the closed-loop gain, A_{CL}, is

$$A_{CL} = \frac{x_o}{x_s} \tag{23.5}$$

Realizing that

$$x_f = \beta \cdot x_o \tag{23.6}$$

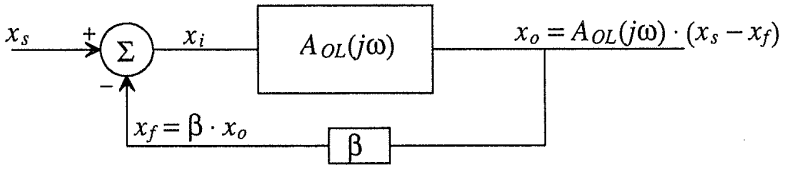


Figure 23.1 Basic block diagram to illustrate the feedback concept.

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and plugging in Eq. (23.6) into (23.2) and solving for the closed-loop gain, we find that A_{CL} becomes

$$A_{CL} = \frac{x_o}{x_s} = \frac{A_{OL}}{1 + A_{OL}\beta} \tag{23.7}$$

where the frequency dependence of A_{OL} has not been shown.

Note the dependence of the A_{CL} on the value of A_{OL}. If the value of A_{OL} becomes large (A_{OL} approaches infinity), then the value of A_{CL} approaches $\frac{1}{\beta}$. This illustrates the need for having a high-gain amplifier. If A_{OL} is very large, then the closed-loop gain becomes highly dependent on the feedback components.

The term $A_{OL}\beta$ is often referred to as the loop gain and will be used in later sections to determine overall amplifier stability.

23.2 Properties of Negative Feedback on Amplifier Design

When used in the design of amplifiers, feedback can provide a number of advantages. These advantages include desensitizing the gain to process parameter variation, reducing nonlinear distortion, reducing the effects of noise, extending the useful bandwidth of the amplifier, and controlling the input and output impedance levels.

23.2.1 Gain Desensitivity

Since the value of the open-loop gain, A_{OL}, is large, its value may change significantly with temperature, mismatch of devices, and other parameter variations. However, negative feedback desensitizes the closed-loop gain from changes in the open-loop gain. The following derivation illustrates this property.

Differentiating both sides of Eq. (23.7) yields

$$\frac{dA_{CL}}{dA_{OL}} = \frac{1}{(1 + A_{OL}\beta)^2} \text{ or } dA_{CL} = \frac{dA_{OL}}{(1 + A_{OL}\beta)^2} \tag{23.8}$$

Dividing each side of Eq. (23.8) by the corresponding factors in Eq. (23.7),

$$\frac{dA_{CL}}{A_{CL}} = \frac{1}{(1 + A_{OL}\beta)} \cdot \frac{dA_{OL}}{A_{OL}} \tag{23.9}$$

where $\frac{dA_{CL}}{A_{CL}}$ represents the fractional change in A_{CL} for a given fractional change in $\frac{dA_{OL}}{A_{OL}}$.

Using Eq. (23.9), if A_{OL} = 10,000 V/V (assuming a voltage amplifier) and β = 1/10 V/V, it can be seen that if $\frac{dA_{OL}}{A_{OL}}$ = 10%, then the change in the closed-loop gain, $\frac{dA_{CL}}{A_{CL}}$ = 0.01 %! This can easily be verified by using Eq. (23.7) for A_{OL}=10,000 and 9,000, keeping β = 1/10 V/V and solving for A_{CL} for each case. The resulting difference proves the immunity of the closed-loop gain to changes in A_{OL}.

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23.2.2 Bandwidth Extension

Negative feedback also increases the usable bandwidth of an amplifier. Assume that an amplifier has the frequency response given by

$$A_{OLH}(s) = \frac{A_{OL}\omega_H}{s+\omega_H} = A_{OL}\frac{1}{\frac{s}{\omega_H}+1} \tag{23.10}$$

$A_{OLH}(s)$ is simply the high-frequency dependent version of A_{OL} and is approximated using a first-order pole at ω_H. Plugging Eq. (23.10) into Eq. (23.7) yields the high-frequency dependent closed-loop version of Eq. (23.7)

$$A_{CLH}(s) = \frac{A_{OLH}(s)}{1+A_{OLH}(s)\beta} = \frac{A_{OL}\omega_H}{s+\omega_H(1+A_{OL}\beta)} \tag{23.11}$$

which can be rewritten as

$$A_{CLH}(s) = \frac{A_{OL}}{(1+A_{OL}\beta)} \cdot \frac{1}{\frac{s}{\omega_H(1+A_{OL}\beta)}+1} = \frac{A_{OL}}{(1+A_{OL}\beta)} \cdot \frac{1}{\frac{s}{\omega_{HF}}+1} \tag{23.12}$$

Note that the resulting equation is composed of two parts. The first factor should be recognized as Eq. (23.7) and is simply the expression for the closed-loop gain at midband. The second factor is the frequency dependent term. It is interesting to observe that the original –3 dB frequency ω_H in Eq. (23.10) is now multiplied by $(1+A_{OL}\beta)$. Figure 23.2 illustrates the bandwidth extension from using negative feedback. The original open-loop frequency response is drawn in the solid line, while the closed-loop frequency response is illustrated in the dashed line. The closed-loop response shows a decrease in the gain and at the same time an increase in bandwidth.

If one were to decrease the value of β, from Eq. (23.11), it can be seen that two interesting effects occur. First, the closed-loop value of the gain will increase, since the

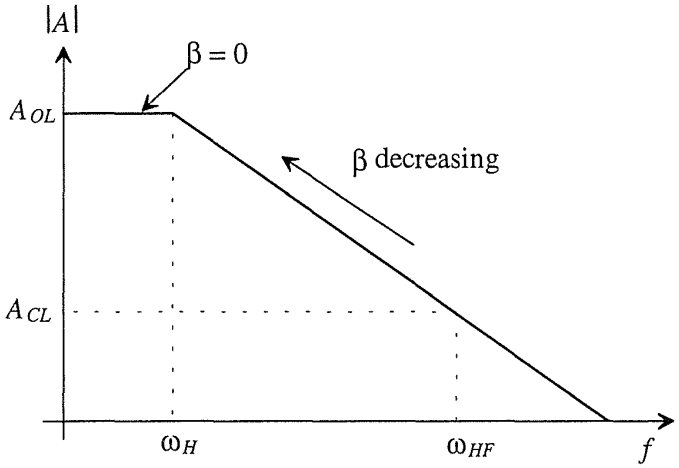


Figure 23.2 Extension of the high-frequency pole by using feedback.

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first factor in Fig. 23.12 increases with a decrease in β. Second, the frequency response decreases since ω_H is multiplied by $(1 + A_{OL}\beta)$ and β is decreasing. The resulting frequency response curve is seen in Fig. 23.2. As β decreases, the overall curve follows the original open-loop curve. Naturally, if β decreases to 0, the amplifier no longer contains any feedback and the amplifier is operating in the open-loop configuration. It should be seen that when using feedback, one trades gain for bandwidth.

The same analysis can be applied to the low-frequency response of an amplifier. Equation (23.13) approximates the low-frequency response of an amplifier with a single first-order low-frequency pole.

$$A_{OLL}(s) = A_{OL}\frac{s}{s+\omega_L} \tag{23.13}$$

If we plug Eq. (23.13) into Eq. (23.7), the closed-loop low-frequency response becomes

$$A_{CLL}(s) = \frac{A_{OLL}(s)}{1+A_{OLL}(s)\beta} = \frac{A_{OL}\frac{s}{s+\omega_L}}{1+A_{OL}\frac{s}{s+\omega_L}\beta} = \frac{A_{OL}}{1+A_{OL}\beta}\frac{s}{s+\frac{\omega_L}{1+A_{OL}\beta}} \tag{23.14}$$

The result in Eq. (23.14) is comprised of the standard closed-loop gain at midband and the frequency dependent term. Note however, that with feedback, the original low-frequency pole, ω_L, in Eq. (23.13) is now divided by $1+A_{OL}\beta$ in Eq. (23.14). Figure 23.3 illustrates the effect of the feedback on the low-frequency response of an amplifier.

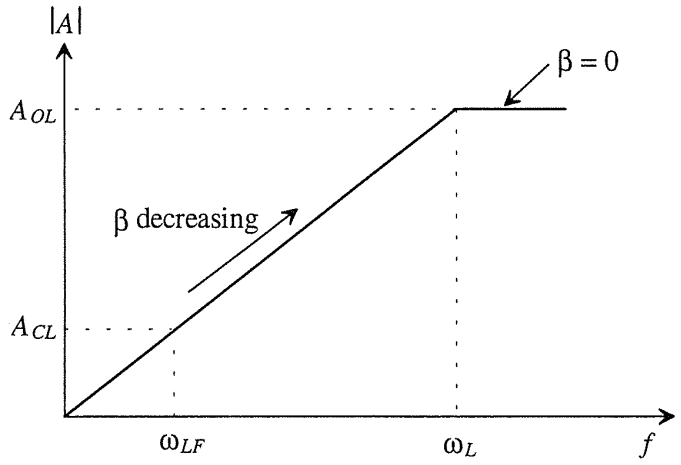


Figure 23.3 Extension of the low-frequency bandwidth by using feedback.

23.2.3 Reduction in Nonlinear Distortion

Negative feedback can also improve the nonlinear behavior of an amplifier. Examine the transfer curve of the voltage amplifier shown in Fig. 23.4 without feedback. Ideally, the amplifier should have a straight line from $-2\text{ V} < V_{in} < 2\text{ V}$. However, nonlinear behavior in the amplifier causes a different slope to occur when $V_{in} > 1\text{V}$ and $V_{in} < -1\text{ V}$.

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The reasons for nonlinearity will be discussed in a future chapter. Note that the output voltage is limited by the value of the power supply (+ 15 V).

Since the gain of the amplifier can be defined as the slope of the transfer curve, we can deduce that

$$A_{OL} = \frac{\Delta V_O}{\Delta V_{IN}} = 10\,\text{V/V} \quad -10\,\text{V} \le V_O \le 10\,\text{V} \tag{23.15}$$

and

$$A_{OL} = \frac{\Delta V_O}{\Delta V_{IN}} = 5\,\text{V/V} \quad V_O > 10 \text{ and } V_O < -10\,\text{V} \tag{23.16}$$

Now suppose that feedback is applied around the amplifier with $\beta = 0.1$ V/V and the transfer curve is redrawn. The gain of the amplifier with feedback becomes

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta} = \frac{10}{1 + 10(0.1)} = 5\,\text{V/V} \quad -10\,\text{V} < V_O < 10\,\text{V} \tag{23.17}$$

and

$$A_{CL} = \frac{5}{1 + 5(0.1)} = \frac{10}{3} \quad V_O > 10\,\text{V and } V_O < -10\,\text{V} \tag{23.18}$$

The resulting transfer curve is illustrated in Fig. 23.4. Note that with feedback, the overall transfer curve is much more linear, resulting in an amplifier that has less nonlinear distortion than the amplifier shown in Fig. 23.4.

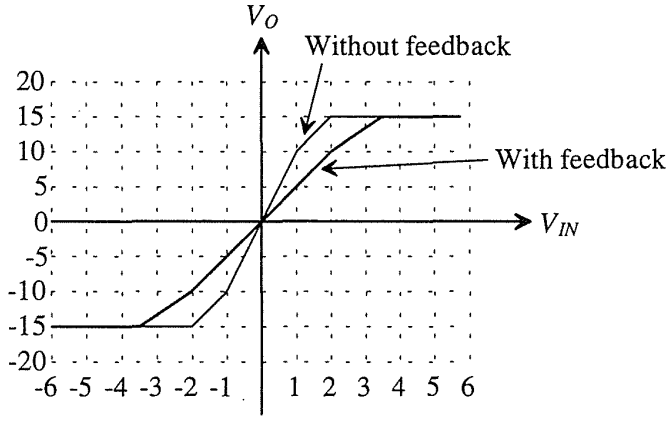


Figure 23.4 Using feedback to improve amplifier linearity.

23.2.4 Input and Output Impedance Control

Input and output impedances of an amplifier can be controlled using negative feedback. As seen in Fig. 23.5, R_i is the small-signal input impedance looking into an amplifier without feedback, and R_{inf} is the input impedance with feedback applied. Similiarly, R_{of}

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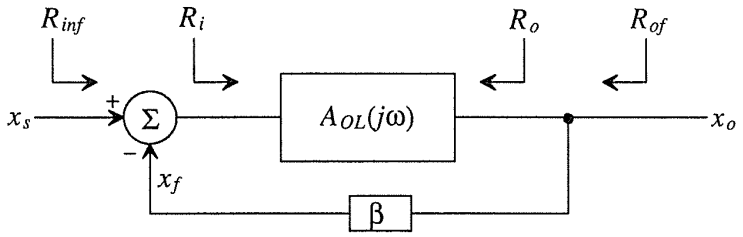


Figure 23.5 Determining the input and output impedances with and without feedback.

and R_o are the output impedances with and without feedback, respectively. Feedback allows us either to increase or decrease both R_{inf} and R_{of} by a factor of $(1 + A_{OL}\beta)$. Although an example of this property is difficult to derive in a general way, proofs of this property will be illustrated with actual circuit examples in a later section. For the time being, it will be sufficient to summarize the impedance control properties of feedback with Table 23.1. Note that the closed-loop impedances are completely dependent on the type of variable that is used (voltage or current) at the input and the output.

If the input variable, x_s, is a voltage, the closed-loop input resistance, R_{inf}, is equal to the open-loop value of the input resistance, R_{in}, multiplied by the value of $1 + A_{OL}\beta$. If the input variable is a current, R_{inf} is divided by the same factor. Alternatively, if the output variable, x_o, is a voltage, then the closed-loop output impedance is the open-loop output impedance divided by $(1 + A_{OL}\beta)$. And if the output variable is a current, the open-loop output impedance is multiplied by the same factor.

Obviously, this concept is a powerful one. We can adjust both input and output impedances in a larger or smaller direction simply by choosing the type of feedback used in the circuit.

Input Variable, x_s	Output Variable, x_o	R_{inf}	R_{of}
V	V	$R_i \cdot (1 + A_{OL}\beta)$	$R_o/(1 + A_{OL}\beta)$
V	I	$R_i \cdot (1 + A_{OL}\beta)$	$R_o \cdot (1 + A_{OL}\beta)$
I	V	$R_i/(1 + A_{OL}\beta)$	$R_o/(1 + A_{OL}\beta)$
I	I	$R_i/(1 + A_{OL}\beta)$	$R_o \cdot (1 + A_{OL}\beta)$

Table 23.1 Summary of impedances with feedback.

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23.3 Recognizing Feedback Topologies

Examine the general single-loop feedback circuit in Fig. 23.6. Remember that x_s, x_i, and x_f must all either be currents or all be voltages, and that the output variable, x_o may be either a voltage or a current. As a result of these restrictions, a total of four types of feedback are possible (Table 23.2).

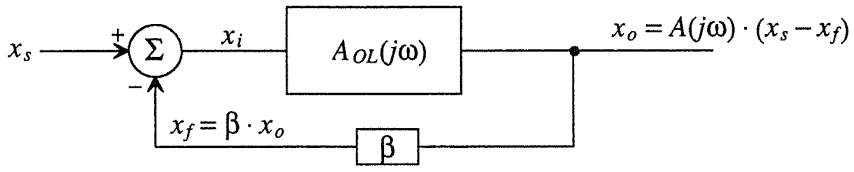


Figure 23.6 Basic block diagram to illustrate the feedback concept.

x_s, x_i, x_f	x_o	Feedback Type (mixing-sampling)
Voltage	Voltage	Series-shunt
Voltage	Current	Series-series
Current	Current	Shunt-series
Current	Voltage	Shunt-shunt

Table 23.2 Feedback type as a function of system variables.

The input summation is often referred to as input mixing. If the input variables, x_s, x_i, and x_f can be written as voltages, the mixing is referred to as series or voltage mixing. If the input variables can be written as currents, it is referred to as shunt or current mixing. The type of variable used at the output determines the second term, known as sampling. If the output variable is a voltage, the sampling is referred to as shunt or voltage sampling. If the output variable is a current, the sampling is known as series or current sampling.

In the analysis of feedback amplifiers, the following terminology will apply. The term *basic amplifier* will correspond to the gain circuit, A_{OL}, in the block level feedback diagrams. When determining the value of A_{OL}, it is very important to determine the loading due to the β network and any source and load resistance. The β network is also known as the feedback network. The overall circuit that includes both A_{OL} and β will be referred to as the *feedback amplifier*.

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23.3.1 Input Mixing

Figures 23.7a and b illustrate the inputs to two generic feedback amplifiers. The basic amplifier in 23.7a is used in a series mixing configuration since the equation, $x_i = x_s - x_f$ can be written in terms of the voltages. Note also that the basic amplifier and the β network are in series with each other. In Fig. 23.7b, however, the basic amplifier is used in a shunt mixing configuration. Here, the summation at the input can only be written in terms of currents such that $i_i = i_s - i_f$. The feedback circuit and the basic amplifier circuit are both in parallel, or it can be said that the feedback shunts the basic amplifier.

23.3.2 Output Sampling

Determining the type of variable used at the output is not an obvious endeavor. However, a general model followed by several examples will help clarify the proper procedure. Figures 23.7c and d show the outputs of two generic feedback amplifiers. Shunt sampling is shown in Fig. 23.7c. Note that the feedback circuit is shunting, or in parallel with the basic amplifier circuit. The output variable is considered a voltage because the feedback circuit "senses" or samples the voltage across R_L. Series sampling is seen in Fig. 23.7d. Here, the feedback network is in series with the basic amplifier circuit. The output variable is a current since the feedback circuit now senses the

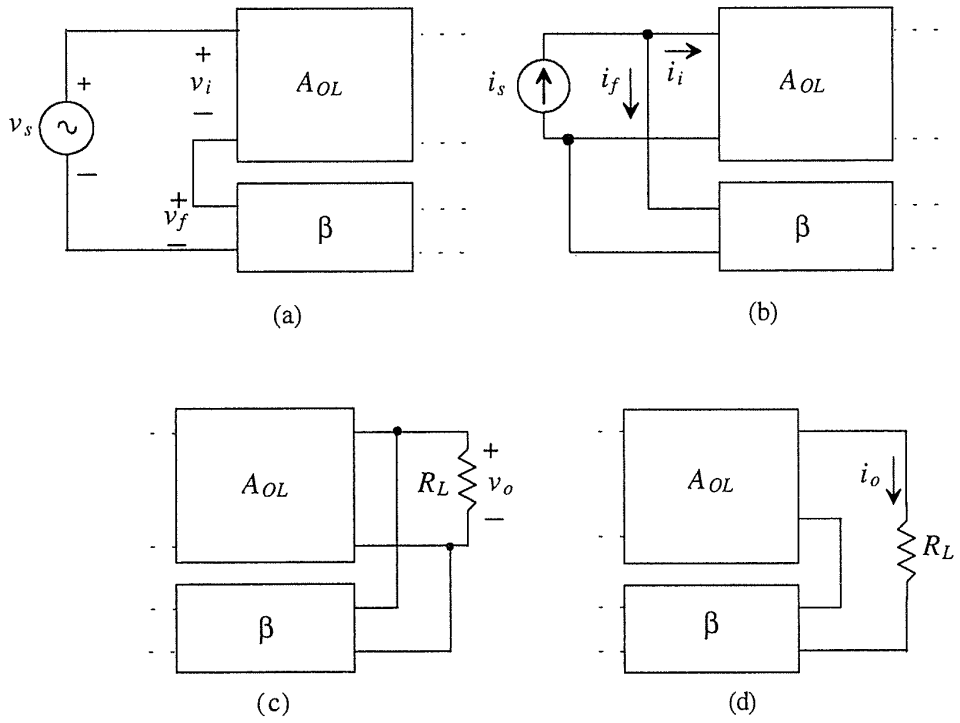


Figure 23.7 Generic block diagrams for input circuits (a) series mixing and (b) shunt mixing and output circuits, (c) shunt sampling, and (d) series sampling.

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current through the load resistor. Two rules that help distinguish between the two types of output sampling are:

Rule 1: If one terminal of the output active device (drain or source) is driving the load and the other terminal is attached to the feedback network, the output sampling is series.

Rule 2: If the load and the beta network are connected to the same node, the output sampling is shunt.

23.3.3 The Feedback Network

When analyzing feedback circuits, it would be wise first to recognize the basic amplifier circuit, A_{OL}, and the β network by tracing the small-signal path from the input to the output and back through the feedback. The path from the input through the A_{OL} circuit to the output will be denoted as the forward path and the path from the output back through the β network, as the feedback path. Determining which path the signal takes is not obvious when there are several devices from which to choose. Some rules that will aid in the analysis are as follows:

- The *forward path* through the basic amplifier circuit will always take the path that has the highest gain.
- The AC small-signal will always enter either a gate or a source and will always exit either a drain or a source. The gain from drain to source is very small (at least for linear applications) and is considered to be negligible for most of our applications. A small-signal will never exit through the gate.
- The feedback signal must subtract from the input signal. To ensure that this is the case, one must count the number of inversions around the loop. Every time a signal crosses a gate-to-drain junction (common source amplification), an inversion occurs. Examples of this will be discussed next.

Examine Fig. 23.8a. Note that the signal path in the forward direction progresses through the path with the highest gain—from the gate of M1 to the drain of M1, into the gate of M2 and out the drain of M2. The feedback path consists of the resistors R_1 and R_2. The feedback variable consists of the voltage that appears across R_1.

An Important Assumption

One might attempt to draw the forward path from the gate of M1 to the source of M1, through the feedback resistor, R_2, and to the output. In actuality, this would be a legitimate forward path because in some cases the feedback network is actually bidirectional. However, the signal will have very little gain since the gain from gate to source of any MOS device is a maximum of one (common drain amplification) and the gain from v_f to v_2 in the forward direction will be less than one because of the voltage divider relationship between R_5 and R_2. *Thus, for all of the analysis performed in this*

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chapter, the forward path through the amplifier circuit dominates the expression for the total forward gain from input to output, while the forward path through the feedback is assumed to be negligible. This important assumption greatly simplifies the analysis and is a good one, since the amplifier will have very poor performance if there is not a good deal of gain through the basic amplifier. (Ideally, the value of A_{OL} is infinite.) If an active device is used in the feedback network, the forward gain through the β network is minimized.

Figure 23.8b has the same basic transistor topology, except it uses current as its input. The forward path consists of the source of M1, out the drain of M1 into the gate of M2 and out the source of M2. The feedback path consists of R_5 and R_2, and the feedback variable is the current, i_f. Note that the forward path has the highest possible gain path, since M1 acts as a common gate amplifier. The forward path could progress from the input through R_2 and into the drain of M2. However, since the small-signal gain from the drain to the source of M2 is extremely small, it will be neglected.

Counting Inversions Around the Loop

It is also necessary to check the circuit to ensure that the feedback is indeed negative. Counting the number of inversions around the loop in Fig. 23.8a may initially give the wrong impression, because the number of gate-to-drain junctions encountered by the signal around the loop is two. This implies positive feedback since the feedback variable must be inverted with respect to the input signal. However, the final mixing between v_1 and v_f will provide the additional negative behavior needed to ensure the proper feedback. Notice the relationship that exists between v_1 and v_f. Since $v_i = v_1 - v_f$ the voltage v_f has a subtractive effect on v_i. Thus, a positive change in the signal entering the gate of M1 will result in a positive change in the source of M1 and a smaller, stable voltage v_i. If v_f had been negative with respect to v_1, then v_i would be, $v_i = v_s + v_f$ and positive feedback would occur.

Now examine Fig. 23.8b. Again, if we count the number of inversions around the loop from input back to the mixing variable, i_f, the number of inversions is odd, which is exactly what is needed, since KCL tells us that $i_i = i_1 - i_f$. The direction of the feedback current from the output is opposite the direction of i_f; however, the signal is inverted, making it equivalent to i_f, as illustrated from Fig. 23.9.

Examples of Recognizing Feedback Topologies

Now that the method for recognizing feedback has been discussed, examples will be presented to solidify the concepts. Again examine Fig. 23.8. Here, two types of feedback are illustrated. Transferring the block diagram concepts to transistor-level circuits can be a difficult task. However, several other rules can be applied which will reveal the type of sampling used in the circuit. The term *input active device* is used to denote the transistor that is being driven by the input source. The term *output active device* is used to denote the transistor used to drive the load.

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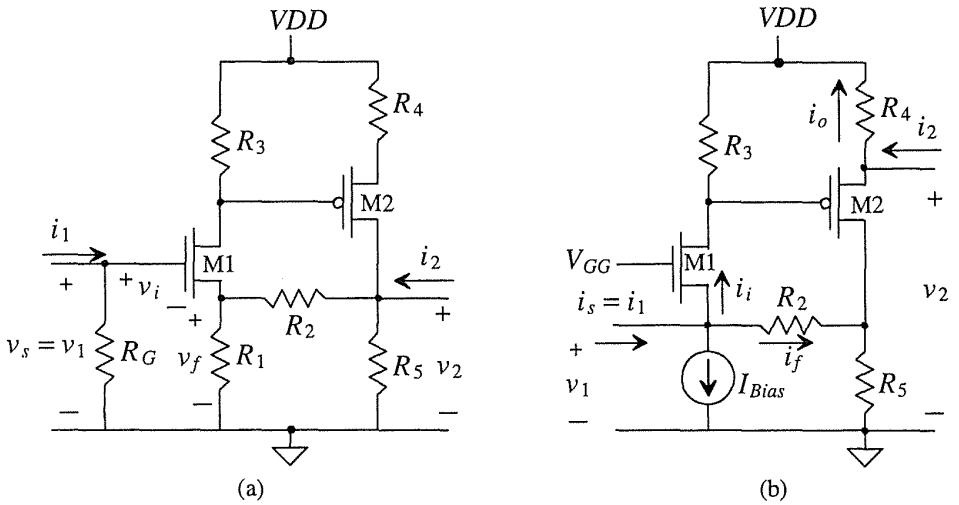


Figure 23.8 Feedback topologies (a) series-shunt and (b) shunt-series.

In Fig. 23.8a, the input variables can only be written in terms of voltages such that $v_i = v_s - v_f$. We could attempt to sum currents at the node on the gate. However, the current flowing into the resistor, R_G, will not be the result of any feedback, thus making current mixing impossible. The output sampling is of the shunt type since the β network and the basic amplifier are in parallel (the β network is connected to the same node as the output) and v_o is the voltage being sampled. This amplifier employs series mixing and shunt sampling, and is referred to as a series-shunt feedback amplifier configuration.

Figure 23.8b illustrates shunt-series feedback. The DC current source is viewed as an AC open circuit, and the DC voltage source, V_{GG}, is considered as an AC short circuit. Note how the input variables can only be written in terms of currents forming the expression, $i_i = i_s - i_f$. Series sampling is used at the output since the feedback network is in series with the basic amplifier. This amplifier configuration also follows rule 2, mentioned previously; thus, the proper small-signal output variable is the current, i_o. Note that the direction of the small-signal output current, i_o, is consistent with the direction of the small-signal model, since *VDD* is considered a small-signal ground.

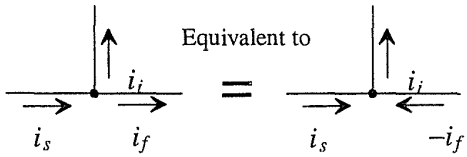


Figure 23.9 Shunt mixing illustrated with an odd number of inversions.

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The variables v_1, i_1, v_2, and i_2 may or may not correspond to the defined input and output variables of the feedback circuit. For example, in Fig. 23.3b, the correct output variable is defined as i_o. However, the gain of the feedback amplifier can be ascertained in terms of v_1, i_1, v_2, and i_2, since $v_2 = i_o \cdot R_4$. Also note that v_1/i_1 and v_2/i_2 correspond to the input and output impedances, respectively, of the feedback amplifier.

Series-series feedback is illustrated in Fig. 23.10a. Although the input variables are written in terms of voltages, the output variable is considered to be a current since the feedback network is in series with the amplifier output. Note that the only difference between Figs. 23.10a and 23.8a is in placement of the output terminal. The same holds true for Figs. 23.10b and 23.8b. Lastly, Fig. 23.10b illustrates shunt-shunt feedback. Current summation occurs at the input which typifies shunt or current mixing, and the β network made up of R_5 and R_2 shunts the output.

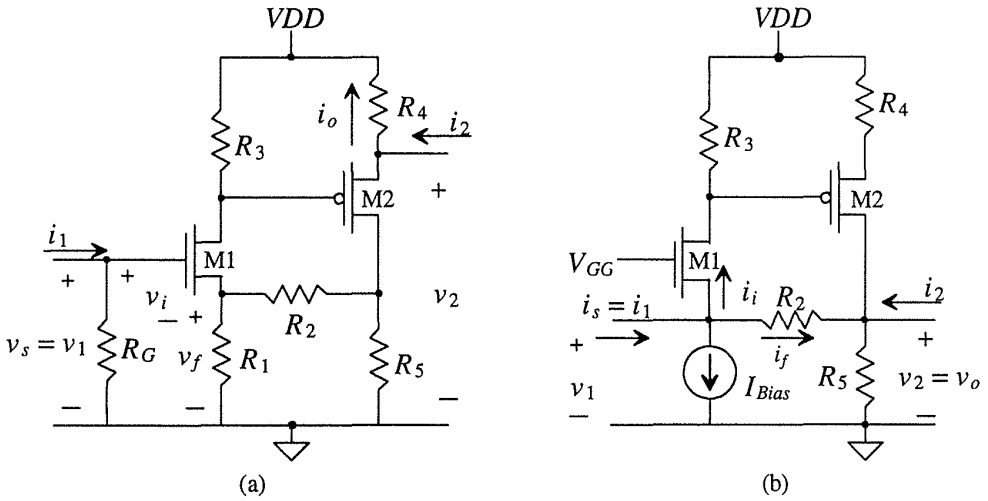


Figure 23.10 Feedback topologies: (a) series-series and (b) shunt-shunt.

23.3.4 Calculating Open-Loop Parameters

Once the feedback topology can be recognized, the analysis of the circuit can begin. We will perform two types of analysis: open-loop and closed-loop. Openloop analysis entails approximately 80 percent of the circuit analysis required to solve a feedback problem. Open-loop values are then used to calculate the closed-loop values, so extreme care must be taken when analyzing the open-loop circuit. We will then "close the loop" and calculate the feedback characteristics of the overall feedback amplifier

The method of analysis for feedback amplifiers can be confusing if we do not distinguish between open- and closed-loop notation. We will denote the open-loop voltage and current variables by use of the * notation. The open-loop parameters include A_{OL}, R_i, R_o, and β and are defined as follows.

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$$A_{OL} = \frac{x_o^*}{x_s^*} \text{ and is the open-loop gain of the basic amplifier} \quad (23.19)$$

$$R_i = \frac{v_1^*}{i_1^*} \text{ and is the open-loop input impedance} \quad (23.20)$$

$$R_o = \frac{v_2^*}{i_2^*} \text{ and is the open-loop output impedance} \quad (23.21)$$

$$\beta = \frac{x_f^*}{x_o^*} \text{ and is the gain through the feedback network} \quad (23.22)$$

In our discussion of general feedback principles in Sec. 23.1, it was assumed that the β network was ideal, meaning that the impedance of the β network did not load the amplifier circuit. However, in real-life applications, the β network can cause loading effects on both the input source and the output of the amplifier circuit. The type of feedback used will determine how the β network loading is calculated. As we progress in the discussion of each feedback topology, the method of determining the β network loading will be presented.

All variables in the following analysis are considered to be small-signal AC voltages or currents. We will perform the open-loop analysis using the following steps:

1. Replace input source with Norton or Thevenin equivalent circuit and calculate open-loop gain. The amplifier circuit will produce a different type of gain for each type of feedback. For example, the open-loop gain for an amplifier used in a series-shunt configuration will have units of V/V. This is a standard voltage amplifier since the output variable is a voltage and the input mixing sums voltages. An amplifier using series-series feedback will have a gain with units of I/V, since the output variable is now a current and the input mixing uses voltages. This type of amplifier is also known as a transconductance amplifier since the units of the gain, I/V, are equivalent to a conductance. Similiarly, an amplifier used in the shunt-series configuration has a gain with units of I/I (a current amplifier), and an amplifier used in a shunt-shunt configuration will have a gain with units of V/I and is known as a transimpedance amplifier.

2. When calculating the open-loop gain of the circuit, consider the β network loading. An equivalent resistance, $R_{\beta i}$ and $R_{\beta o}$, as seen in Fig. 23.11 will represent the total input and output resistance of the β network. The method for calculating $R_{\beta i}$ involves the following steps.

   - If the output sampling is shunt (voltage), short the output node to ground.
   - If the output sampling is series (current), remove the device driving the output load as if it were taken "out-of-socket."
   - Calculate $R_{\beta i}$ as the impedance looking from the input into the β network.

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The method for calculating $R_{\beta o}$ involves similar methodology:

- If the input mixing is shunt (current), short the output node to ground.
- If the input mixing is series (voltage), remove the input active device as if it were taken "out-of-socket."
- Calculate $R_{\beta o}$ as the impedance looking from the output into the β network.

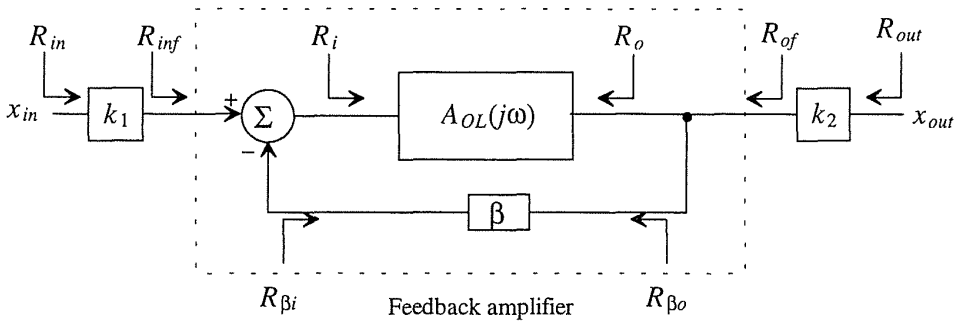


Figure 23.11 Block diagram of a generic feedback amplifier that distinguishes between open- and closed-loop impedances.

The method for determining the loading of the β network is rooted in basic two-port theory where each type of feedback configuration corresponds to one of the four basic two-port topologies. For further information regarding two-port theory, the reader is advised to consult [1]. One method used to easily remember the above rules is to remember that if mixing or sampling is shunt, then "short" the input or output, respectively. If the mixing or sampling is series, then "sever" the input or output device, respectively, by taking it "out-of-socket."

3. Calculate feedback factor, β, for the amplifier. The open-loop circuit is analyzed to determine the gain from the output back to the point where the feedback variable mixes with the input.
4. Determine the open-loop input and output impedances, R_i and R_o. These impedances can be calculated using standard circuit analysis techniques.

23.3.5 Calculating Closed-Loop Parameters

Once all the open-loop parameters are obtained, the closed-loop values are easily calculated. The closed-loop gain is

$$A_{CL} = \frac{x_o}{x_s} = \frac{A_{OL}}{1 + A_{OL} \cdot \beta} \tag{23.23}$$

for all four topologies. The closed-loop input impedances represent only the input and output impedances of the feedback amplifier. The input impedance from the input

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source, R_{in}, may correspond to R_{inf} if there is no gain from the source to the source, x_{in}, to the input of the feedback amplifier, x_s. Similiarly, the value of the output resistance, R_{out}, may or may not correspond to R_{of}, depending on the type of sampling used. Figure 23.11 illustrates this distinction. Calculating the input and output impedances of the feedback amplifier is dependent on the type of mixing and sampling circuits used, respectively.

$$\text{For series input mixing, } R_{inf} = R_i(1 + A_{OL}\beta) \tag{23.24}$$

$$\text{For shunt input mixing, } R_{inf} = \frac{R_i}{(1 + A_{OL}\beta)} \tag{23.25}$$

The value of the closed-loop output impedances will be as follows:

$$\text{For series output sampling, } R_{of} = R_o(1 + A_{OL}\beta) \tag{23.26}$$

$$\text{For shunt output sampling, } R_{of} = \frac{R_o}{(1 + A_{OL}\beta)} \tag{23.27}$$

Equations (23.24)-(23.27) will be derived with each specific topology. However, it is important to note the effectiveness of using feedback to control input and output impedances. Note that if series mixing or series sampling is used, the open-loop value of the input or output impedance is multiplied by $(1 + A_{OL}\beta)$; and if shunt mixing or shunt sampling is used, the open-loop values of impedances are divided by the same factor. Now that the general methodology has been described, a detailed examination of the four feedback topologies will be presented. The analysis of the four basic feedback topologies begins at the discrete level and progresses into more complex integrated circuits throughout the section.

23.4 The Voltage Amp (Series-Shunt Feedback)

Consider the ideal voltage feedback amplifier shown in Fig. 23.12, with open-loop values, A_{OL}, β, R_i, and R_o already given. The basic amplifier is a voltage amplifier with gain given V/V. Since this is an ideal feedback amplifier, the β network does not load the basic amplifier, meaning that $R_{\beta o} = \infty$ and $R_{\beta i} = 0$.

To determine what type of feedback is present in the circuit, examine the input variables. Since input variables, x_s, x_i, and x_f, correspond to the voltages, v_s, v_i, and v_f, such that the equation, $v_i = v_s - v_f$, can be written, the input mixing is series. The output mixing can be determined using the previous rules. Since the output of the amplifier, A_{OL}, and the β network are attached in parallel (both being connected to the load, R_L), the output mixing is considered to be shunt.

From Sec. 23.1, we already know that the closed-loop gain of the amplifier is

$$A_{CL} = \frac{v_o}{v_s} = \frac{A_{OL}}{1 + A_{OL} \cdot \beta} \tag{23.28}$$

Notice that as A_{OL} approaches infinity, Eq. (23.28) approximates to

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$$A_{CL} \approx \frac{1}{\beta} \tag{23.29}$$

Equation (23.29) is important because it illustrates another power feedback concept. The entire gain of the feedback amplifier can be approximated as the inverse of β as the basic amplifier gain increases to higher and higher values.

We can calculate how the feedback affects the input impedance of the amplifier by applying a test voltage directly to the input of the feedback amp shown in Fig. 23.12, so that $v_s = v_{test}$ and $i_i = i_{test}$. Writing a voltage loop at the input and assuming that the feedback network does not load the amplifier gives

$$v_{test} = i_{test} \cdot R_i + \beta \cdot v_o = i_{test} \cdot R_i + \beta \cdot \frac{A_{OL}}{1 + A_{OL}\beta} \cdot v_{test} \tag{23.30}$$

Equation 23.30 simplifies to

$$R_{inf} = \frac{v_{test}}{i_{test}} = R_i \cdot (1 + A_{OL}\beta) \tag{23.31}$$

The gain of the open-loop amplifier was decreased by $1 + A_{OL}\beta$, while the input impedance, the impedance the source sees, was increased by $1 + A_{OL}\beta$.

Calculation of the output impedance proceeds in the same way as the calculation of the input resistance except that the test voltage is applied to the output of the amplifier with the input shorted to ground with $v_o = v_{test}$ and $i_o = i_{test}$. Writing a loop equation at the output gives

$$v_{test} = i_{test} \cdot R_o + A_{OL} \cdot v_i = i_{test} \cdot R_o + A_{OL} \cdot (-\beta \cdot v_o) \tag{23.32}$$

since the input is shorted to ground and $v_i = -v_f = -\beta \cdot v_o$. The output impedance is given by

$$R_{of} = \frac{v_{test}}{i_{test}} = \frac{R_o}{1 + A_{OL}\beta} \tag{23.33}$$

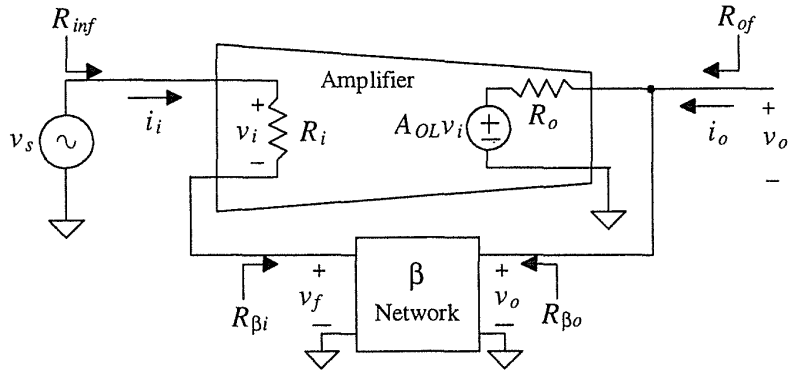


Figure 23.12 An ideal voltage amplifier (series-shunt).

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or the output resistance is reduced by $1 + A_{OL}\beta$. Ideally, a voltage amplifier has infinite input resistance and zero output resistance. Adding feedback to a voltage amplifier with finite input resistance and nonzero output resistance help make the amplifier closer to the ideal.

Now that the ideal series-shunt amplifier has been examined from a block level point of view, a discussion of the nonideal series-shunt feedback amplifier at the transistor level with loading effects will be considered. The amplifier seen in Fig. 23.13 was analyzed previously and was determined to use series-shunt feedback.

The small-signal circuit of the feedback circuit is seen in Fig. 23.14. Note that the forward path consists of the following nodes: 1, 2, 3. The feedback path consists of nodes 3 and 4, with the feedback variable, v_f, appearing across R_1. In the previous discussion, it was assumed that the β network did not load the amplifier circuit. However, to accurately calculate the open-loop gain, A_{OL}, the loading of R_1 and R_2 on both the input and the output of the amplifier circuit needs to be considered. Note that the resistor R_S is initially ignored, since it is essentially outside the feedback amplifier.

Since we are analyzing a series-shunt amplifier, we may determine the loading caused by the β network on the input, $R_{\beta i}$ and the output $R_{\beta o}$ in the following way (refer to Fig. 23.15). Looking into the β network from the input, we observe the resistance seen with the output terminal shorted to ground. The equivalent resistance to ground seen is the loading of the β network seen by the input of the amplifier. In this example, R_2 is seen. Therefore, in the open-loop model used to determine A_{OL}, we will include R_2 in parallel with R_1. The loading at the output is found similarly. Since the input mixing is series, we will remove M1 "out-of-socket" and look into the β network from the output. The equivalent resistance seen is then attached to the output of the open-loop model. In this example, the equivalent resistance is $R_2 + R_1$ and is attached to the output of the open-loop model. The resulting open-loop model is seen in Fig. 23.16.

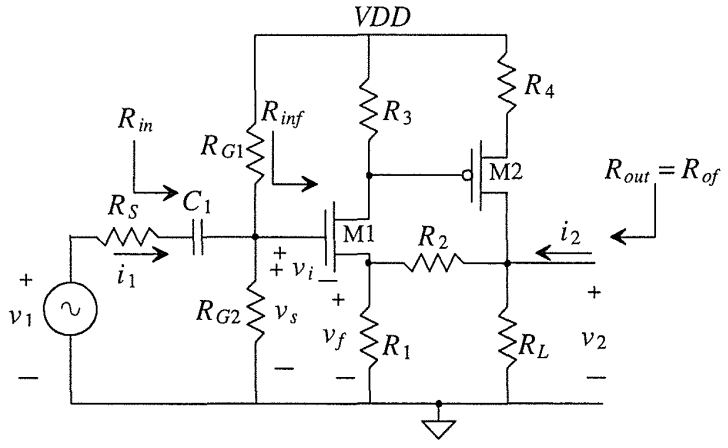


Figure 23.13 Transistor-level series-shunt feedback amplifier.

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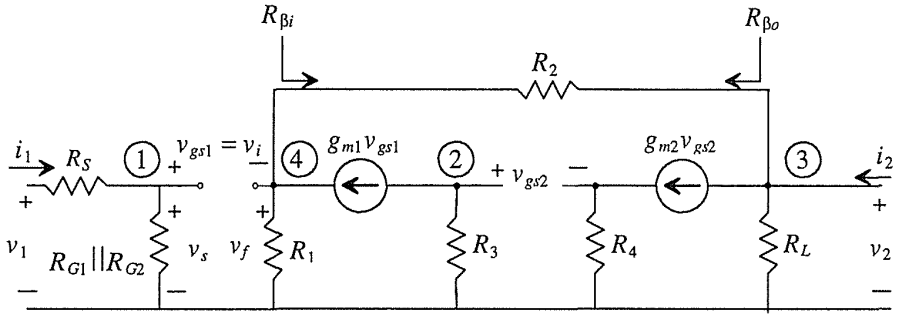


Figure 23.14 Closed-loop small-signal model of Fig. 23.8.

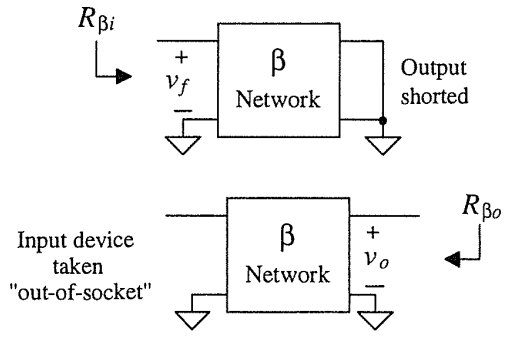


Figure 23.15 Determining the loading due to the feedback network for a series-shunt amplifier.

We will initially assume that r_o for the MOSFETS is much larger than the discrete resistors and that the bulk and source are tied together (v_{sb} = 0). As we progress through the chapter, more difficult circuits will include drain-to-source resistances to our small-signal analysis.

The open-loop model is now ready to be analyzed in order to calculate A_{OL}. Since we are using a series (voltage)-shunt (voltage) feedback amplifier, the units of A_{OL} will be V/V and

$$A_{OL} = \frac{v_2^*}{v_s^*} \tag{23.34}$$

Solving for A_{OL} yields

$$A_{OL} = \frac{v_2^*}{v_s^*} = \left(\frac{v_2^*}{v_{gs2}^*}\right)\left(\frac{v_{gs2}^*}{v_{gs1}^*}\right)\left(\frac{v_{gs1}^*}{v_s^*}\right) = [-g_{m2}R_L||(R_2+R_1)]\left[-\frac{g_{m1}R_3}{1+g_{m2}R_4}\right]\left[\frac{1}{1+g_{m1}(R_1||R_2)}\right] \tag{23.35}$$

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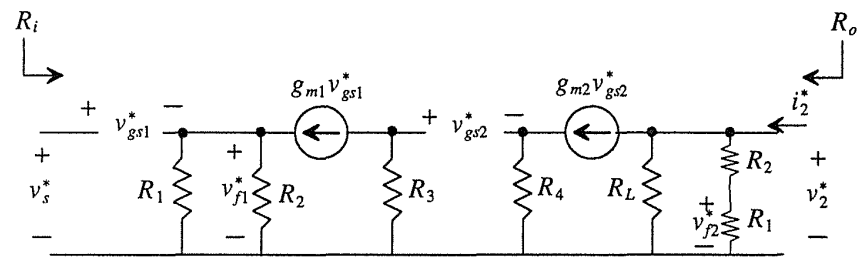


Figure 23.16 Open-loop small-signal model of Fig. 23.8.

Next, the value of β can also be calculated from the open-loop model. Remembering that β is defined as the gain from the output back to the input mixing variable, v_f, we can write

$$\beta = \frac{v_f^*}{v_2^*} = \frac{R_1}{R_1 + R_2} \tag{23.36}$$

since the β network is simply a voltage divider relationship. Notice that the open-loop circuit now contains two values of R_2 and v_f^*. In this example, since r_o was assumed to be infinite, the gain from v_2^* to v_{f1}^* will be zero. If r_o had not been neglected, the gain from v_2^* to v_{f1}^* would have been small but finite. Therefore, it can be said that a reverse path exists through the basic amplifier as well as through the feedback network. However, the gain from v_2^* to v_{f2}^*, though less than one, will be significantly larger than from v_2^* to v_{f1}^*. *Therefore, just as the forward path through the feedback network was neglected, the reverse path through the basic amplifier is assumed to be much smaller than the reverse path through the feedback path. Therefore, the value of* β *is calculated using the resistor, R_2, closest to the output.*

Next, the value for R_i and R_o will be calculated. These values are determined using the open-loop model generated in Fig. 23.16. Since we are using MOS devices, it should be obvious that the input resistance to the open-loop circuit is ∞. The output resistance, however, can be calculated shorting the gate of M1 to ground and applying a test voltage to the output. Since the input is grounded, $v_{g2} = 0$, and R_o is simply the parallel combination of resistances at the output (assuming that r_{o2} is very large).

$$R_o = \frac{v_o^*}{i_2^*} = R_L || (R_1 + R_2) \tag{23.37}$$

Once the open-loop values are calculated, the closed-loop values are easily attained. The closed-loop values are

$$A_{CL} = \frac{v_2}{v_s} = \frac{A_{OL}}{1 + A_{OL}\beta} \tag{23.38}$$

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$$R_{inf} = \frac{v_s}{i_s} = R_i(1 + A_{OL}\beta) \tag{23.39}$$

$$R_{out} = R_{of} = \frac{v_2}{i_2} = \frac{R_o}{1 + A_{OL}\beta} \tag{23.40}$$

Analysis of this problem has not yet been completed. Notice that we initially neglected the source resistance and the biasing resistors, R_{G1} and R_{G2}, since they played no part in the feedback analysis of the amplifier. However, they will have an effect in the overall gain and need to be considered. The total gain of the entire circuit is

$$\frac{v_2}{v_1} = \frac{v_s}{v_1} \cdot \frac{v_2}{v_s} = \frac{R_{G1} || R_{G2}}{R_{G1} || R_{G2} + R_S} \cdot A_{CL} \tag{23.41}$$

and the value of R_{in} as seen by the signal source is

$$R_{in} = \frac{v_1}{i_1} = R_{G1} || R_{G2} \tag{23.42}$$

and the analysis is now complete. Notice that the value of R_{in} is not the same as R_{inf}.

Example 23.1

For the series-shunt circuit shown in Fig. 23.17a, draw the closed-loop small-signal model and identify the forward and feedback paths, draw the open-loop model, calculate A_{OL}, β, R_i, and R_o, and calculate the closed-loop parameters v_2/v_1, v_1/i_1, and v_2/i_2. You may assume that $r_o = \infty$ for both devices and that DC analysis has already been performed with $g_{m1} = g_{m2} = 1$ mA/V.

The closed-loop small-signal model can be seen in Fig. 23.17b with the forward and feedback paths drawn. The open-loop model with loading effects is seen in Fig. 23.17c. Since the output uses shunt sampling, the value of $R_{\beta i}$ is found by shorting the output node and looking at the load resistance resulting from the feedback network. In this case, $R_{\beta i}$ is equal to R_2. Since the input mixing is series, the input device, M1, is "severed," so that only $R_1 + R_2$ is seen looking into the feedback loop from the output. Thus, $R_{\beta o} = R_1 + R_2$.

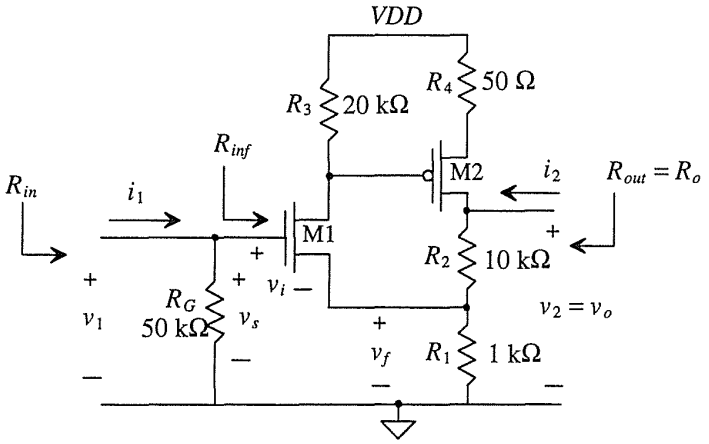
The values of r_o are considered to be infinite, so the values of R_i and R_o can be found by inspection, $R_i = \infty$, and $R_o = R_1 + R_2 = 11$ kΩ. Notice that when solving the open-loop circuit (Fig. 23.17c) v_1 and R_G are not included since we are only interested in solving the feedback portion of the circuit.

The open-loop gain, A_{OL}, can be found simply as the gain of two common source amplifiers with source resistance,

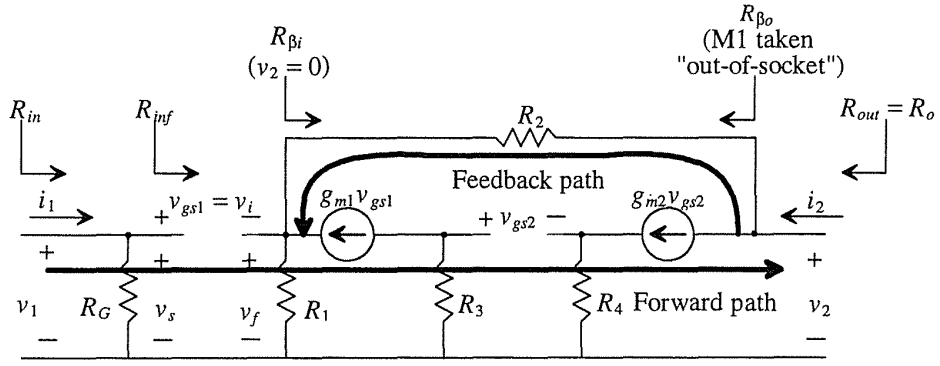
$$A_{OL} = \frac{v_2^*}{v_s^*} = \frac{v_2^*}{v_{g2}^*} \cdot \frac{v_{g2}^*}{v_s^*} = \left[\frac{-g_{m2}(R_2 + R_1)}{1 + g_{m2}R_4}\right]\left[\frac{-g_{m1}R_3}{1 + g_{m1}(R_1 || R_2)}\right] = 109.8 \text{ V/V}$$

The value of β is always the gain from the output to the feedback variable. In this case, a simple voltage divider relationship exists such that

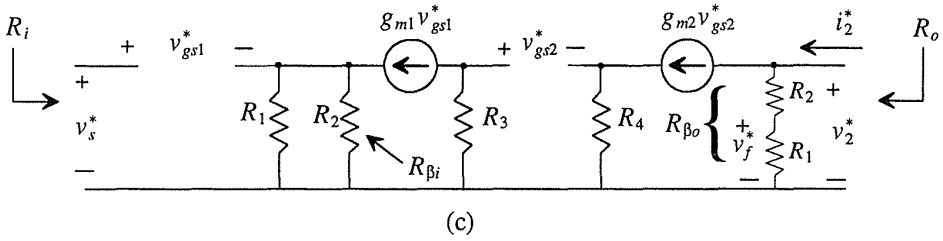
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(a)



(b)



(c)

Figure 23.17 (a) Series-shunt circuit used in Ex. 23.1; (b) its closed-loop small-signal model; and (c) the resulting open-loop model.

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$$\beta = \frac{v_f^*}{v_2^*} = \frac{R_1}{R_1 + R_2} = 0.0909 \text{ V/V}$$

Again, notice that the product of $A_{OL}\beta$ is positive and unitless. Now that the open-loop values are calculated, the closed-loop values can be found by using Eqs. (23.38) - (23.40).

$$A_{CL} = \frac{v_2}{v_s} = \frac{A_{OL}}{1 + A_{OL}\beta} = \frac{109.8}{1 + (109.8 \cdot 0.0909)} = 10 \text{ V/V}$$

A simple check will verify that the solution is correct if $A_{CL} \approx \frac{1}{\beta}$, which is the case.

Notice in Fig. 23.17a and Fig. 23.17b that closed-loop output impedance, R_{of} is equal to the value of R_{out}. However, the value of the closed-loop input impedance, R_{inf}, is not equal to R_{in}, since the feedback amplifier itself excludes the input source and the gate resistor, R_G. The closed-loop values, R_{inf}, and R_{of}, are also easily attained, that is,

$$R_{inf} = \infty \text{ (since } R_i = \infty)$$

and

$$R_{of} = R_{out} = \frac{v_2}{i_2} = \frac{R_o}{(1 + A_{OL}\beta)} = \frac{11 \text{ k}\Omega}{10.98} = 1.002 \ \Omega$$

The last step involves finding R_{in} and v_2/v_1. The value of R_{in} can be found by examining Fig. 23.17a as,

$$R_{in} = \frac{v_1}{i_1} = R_G || R_{inf} = 50 \text{ k}\Omega$$

The overall gain, v_2/v_1, will be equal to the value of A_{CL} since the input voltage, v_1 is equal to v_s. If we had included a value for a source resistance, then an additional voltage divider relationship would have been needed to formulate v_2/v_1 as seen in Eq. (23.41)

$$\frac{v_2}{v_1} = A_{CL} = 10 \text{ V/V} \ \blacksquare$$

23.5 The Transimpedance Amp (Shunt-Shunt Feedback)

Shunt-shunt feedback mixes current at its input and samples voltage at the output. Consider the ideal shunt-shunt feedback amplifier shown with open-loop values, A_{OL}, β, R_i, and R_o, in Fig. 23.18. In the ideal case, $R_{\beta i}$ is infinite and $R_{\beta o}$ is zero. Notice that the basic amplifier and the β network are in parallel at both the input and the output. The β network shunts the basic amplifier; therefore, the input variable is a current. Looking into the output of the amplifier, we see that the feedback path is in parallel with or shunts the output signal. Therefore, the output signal is a voltage. Also note that since the input variable is a current and the output variable is a voltage, the basic amplifier

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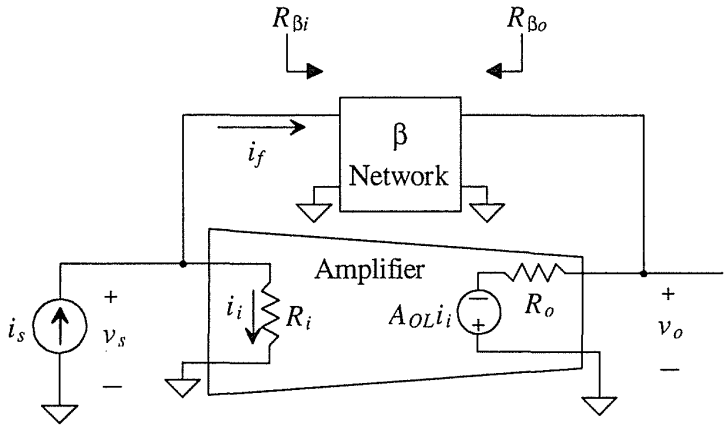


Figure 23.18 An ideal transimpedance (shunt-shunt) amplifier.

has units of V/I, also known as a transimpedance amplifier. Since $A_{OL}\beta$ should always be unitless and positive, β will have units of I/V (mhos).

The closed-loop gain is

$$A_{CL} = \frac{v_o}{i_s} = \frac{A_{OL}}{1 + A_{OL}\beta} \tag{23.43}$$

Notice that the basic amplifier circuit is inverting, corresponding to an ideal op-amp circuit. Since A_{OL} is negative, then β must also be negative to ensure that negative feedback exists.

To calculate the input impedance of the transimpedance amplifier we apply a test current source to the input of the amplifier, such that $i_s = i_{test}$ and $v_s = v_{test}$. The test current and the input impedance are determined by

$$i_{test} = \frac{v_{test}}{R_i} + i_f = \frac{v_{test}}{R_i} + \beta v_o = \frac{v_{test}}{R_i} + \beta A_{OL} i_i = \frac{(1 + A_{OL}\beta) \cdot v_{test}}{R_i} \tag{23.44}$$

Assuming that the β network does not load the basic amplifier, we note that the closed-loop input impedance becomes

$$R_{inf} = \frac{v_{test}}{i_{test}} = \frac{R_i}{1 + A_{OL}\beta} \tag{23.45}$$

A similar analysis of the output impedance of the transimpedance amplifier shows that

$$R_{of} = \frac{R_o}{(1 + A_{OL}\beta)} \tag{23.46}$$

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The ideal transimpedance amplifier has zero input resistance and zero output resistance. We can see from Eqs. (23.45) and (23.46) that the addition of the feedback helps to make the basic amplifier appear closer to the ideal.

Now examine the transistor level shunt-shunt feedback circuit shown in Fig. 23.19. The closed-loop and open-loop small-signal models are seen in Fig. 23.20 and Fig. 23.21, respectively. The gate is attached to AC ground since it is attached to a DC source and the DC current source I_{SS} is an AC open circuit. Interestingly, since the values of r_{o1} and r_{o2} have been included, there is a feedback path through the basic amplifier. However, this gain is very small compared to the feedback path through the β network and is typically assumed to be negligible.

The open-loop analysis begins by evaluating the effects of the β network on the basic amplifier using the rules stated earlier. The resistance, $R_{\beta t}$, will be the equivalent resistance seen looking into the β network from the input with the output node shorted to ground. The equivalent resistance looking into the β network from the output, $R_{\beta o}$, will be calculated with the input shorted to ground.

Since we are using shunt-shunt feedback, A_{OL} will be defined as

$$A_{OL} = \frac{v_2^*}{i_s^*} = \frac{v_2^*}{v_{g2}^*} \cdot \frac{v_{g2}^*}{v_1^*} \cdot \frac{v_1^*}{i_s^*} \tag{23.47}$$

Solving the first term in Eq. (23.47), can be quite extensive if using standard circuit analysis. A circuit technique based on two-port theory will greatly simplify the analysis.

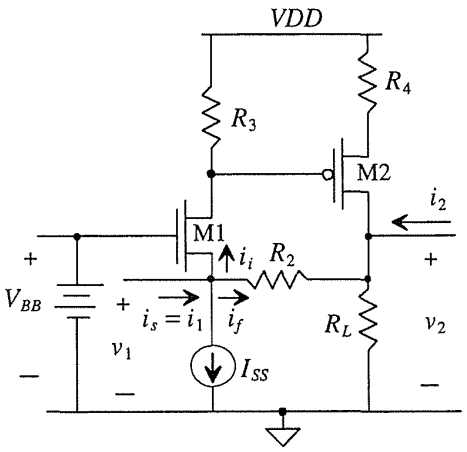


Figure 23.19 Shunt-shunt feedback amplifier.

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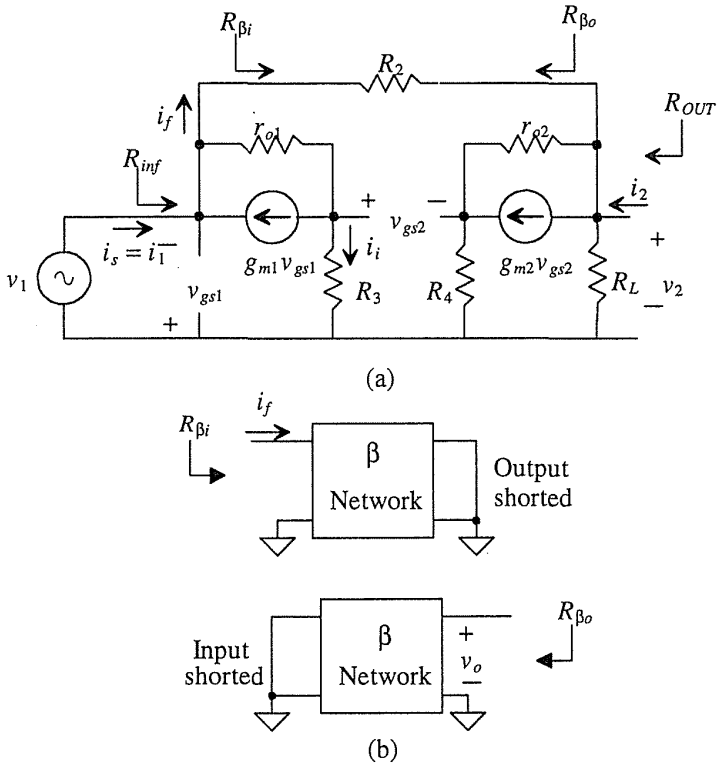


Figure 23.20 (a) Closed-loop small-signal model of Fig. 23.19 and (b) method for determining the feedback network loading.

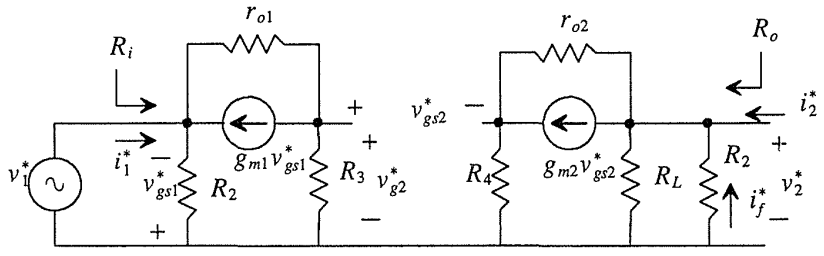


Figure 23.21 Open-loop small-signal model of Fig. 23.19.

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For example, the equivalent circuit for the gain, $\frac{v_2^*}{v_{g2}^*}$, can be seen in Fig. 23.22a. However, the circuit seen in Fig. 23.22b shows the equivalent circuit using an equivalent transconductance, G_M , and output resistance, R_{Leq}. The gain of the equivalent circuit, and hence the actual circuit, is

$$\frac{v_2^*}{v_{g2}^*} = G_M R_{Leq} \tag{23.48}$$

The value of R_{Leq} can easily be found as

$$R_{Leq} = R_L || R_2 || R_{inD2} \tag{23.49}$$

where R_{inD2} is the resistance seen looking into the drain of M2. From Ch. 20, we know that this resistance is

$$R_{inD2} = [(1 + g_{m2}R_4)r_{o2} + R_4] \tag{23.50}$$

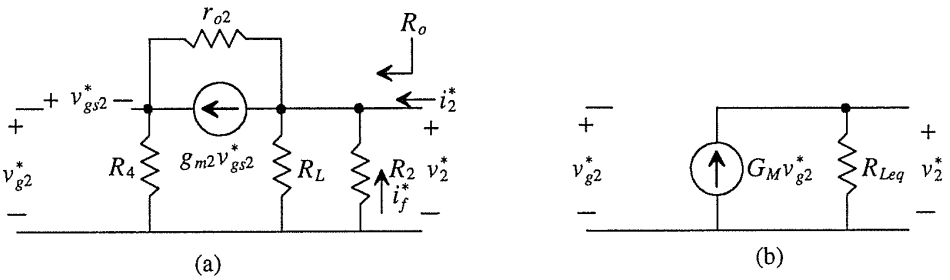


Figure 23.22 (a) Solving a portion of Fig. 23.21, including the drain-to-source resistance, and (b) the equivalent transconductance model.

The value of G_M is the short-circuit transconductance [2] and is defined as

$$G_M = \frac{i_o^*}{v_{g2}^*} \ (R_{Leq} = 0) \tag{23.51}$$

which means that the effective transconductance can be found by shorting the equivalent load resistance, in this case $R_L || R_2$, and finding the gain from the short-circuit current to the input voltage. As seen in Fig. 23.23, the equations used to find G_M are

$$i_o^* = -g_{m2}v_{gs2} + \frac{v_{s2}}{r_{o2}} \tag{23.52}$$

$$v_{s2}^* = -i_o R_4 \tag{23.53}$$

$$v_{s2}^* + v_{gs2}^* = v_{g2}^* \tag{23.54}$$

and solving Eqs. (23.52) - (23.54) yields

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$$G_M = \frac{i_o^*}{v_{g2}^*} = \frac{-g_{m2}}{1 + g_{m2}R_4 + \frac{R_4}{r_{o2}}} \tag{23.55}$$

the gain, $\frac{v_2^*}{v_{g2}^*}$, becomes

$$\frac{v_2^*}{v_{g2}^*} = \frac{-g_{m2}(R_L||R_2||[(1 + g_{m2}R_4)r_{o2} + R_4)]}{1 + g_{m2}R_4 + \frac{R_4}{r_{o2}}} \tag{23.56}$$

Referring back to Eq. (23.47), the second factor, $\frac{v_{g2}^*}{v_1^*}$, can be found by analyzing Fig. 23.21 as

$$\frac{v_{g2}^*}{v_1^*} = \frac{g_{m1}R_3 + \frac{R_3}{r_{o1}}}{1 + \frac{R_3}{r_{o1}}} \tag{23.57}$$

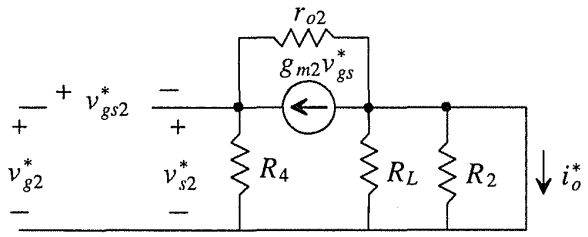


Figure 23.23 Circuit used to determine the equivalent transconductance.

The last term in Eq. (23.47) is simply the input resistance, R_i, of the open-loop circuit shown. Using a test source, we can determine this value to be

$$R_i = \frac{v_1^*}{i_s^*} = \frac{v_t}{i_t}||R_2 = \left(\frac{1 + \frac{R_3}{r_{o1}}}{g_{m1} + \frac{1}{r_{o1}}}\right)||R_2 \tag{23.58}$$

Therefore, the entire expression for the open-loop gain, A_{OL}, becomes

$$A_{OL} = \frac{v_2^*}{i_s^*} = \frac{-g_{m2}(R_L||R_2||((1 + g_{m2}R_4)r_{o2} + R_4))}{1 + g_{m2}R_4 + \frac{R_4}{r_{o2}}} \cdot \frac{g_{m1}R_3 + \frac{R_3}{r_{o1}}}{1 + \frac{R_3}{r_{o1}}} \cdot \left(\frac{1 + \frac{R_3}{r_{o1}}}{g_{m1} + \frac{1}{r_{o1}}}\right)||R_2\ \Omega \tag{23.59}$$

At first glance, this equation may appear quite daunting. However, notice that if r_{o2} is much greater than R_2, R_4, and R_L and if r_{o1} is much greater than R_3, the open-loop gain simplifies to

A_{OL} = [common source amp with source resistance][common gate amp][R_i]

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$$\approx \frac{-g_{m2}(R_L||R_2)}{1+g_{m2}R_4} \cdot g_{m1}R_3 \cdot \frac{1}{g_{m1}}||R_2\ \Omega \qquad (23.60)$$

Equation (23.60) is typically used for discrete designs in which higher values of currents are used, therefore requiring lower resistor values. However, active loads can easily be used, as seen in Fig. 23.24. Here, the resistor, r_{o3} now replaces R_3. Since R_4 is a source degeneration resistor, its value will be small. The active load that replaces R_4 is a gate-drain connected device and equal to $\frac{1}{g_{m4}}||r_{o4}$. And the resistor, R_L, is now replaced by r_{o5}. Therefore, the open-loop gain of Fig. 23.24 can be written by using Eq. (23.29) and making the proper substitutions:

$$A_{OL} = \frac{-g_{m2}(r_{o5}||R_2||(1+g_{m2}(\frac{1}{gm4}||r_{o4}))r_{o2}+\frac{1}{gm4}||r_{o4}))}{1+g_{m2}\left(\frac{1}{gm4}||r_{o4}\right)+\frac{\frac{1}{gm4}||r_{o4}}{r_{o2}}} \cdot \frac{g_{m1}r_{o3}+\frac{r_{o3}}{r_{o1}}}{1+\frac{r_{o3}}{r_{o1}}}\left[\frac{1+\frac{r_{o3}}{r_{o1}}}{g_{m1}+\frac{1}{r_{o1}}}||R_2\right] \qquad (23.61)$$

which can be approximated as

$$A_{OL} = \frac{v_2^*}{i_s^*} \approx \frac{-g_{m2}(R_2)}{1+g_{m2}\left(\frac{1}{gm4}\right)} \cdot \frac{1+g_{m1}r_{o3}}{2} \cdot \left(\frac{1}{g_{m1}}||R_2\right)\Omega \qquad (23.62)$$

if it is assumed that $r_{o1} \approx r_{o3}$ and that the discrete resistor, R_2, is relatively small compared to the impedances of the active loads. An active device could have been used to substitute even the resistor, R_2. This will be discussed further later in the chapter.

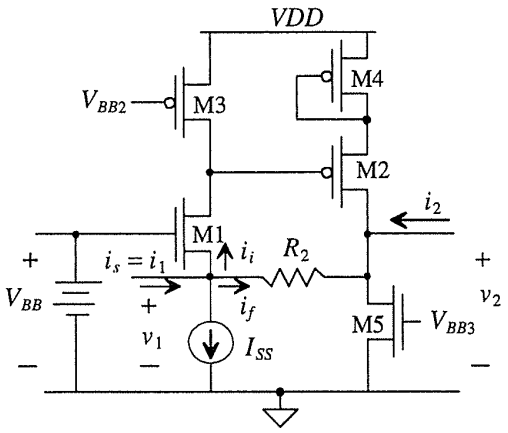


Figure 23.24 Shunt-shunt feedback amplifier using active loads.

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Next, the value of β is calculated as

$$\beta = \frac{i_f^*}{v_2^*} = -\frac{1}{R_2} \text{ mhos} \tag{23.63}$$

Again, note that $A_{OL}\beta$ is unitless and overall positive.

Now that all of the open-loop parameters, A_{OL}, β, R_i, and R_o, have been found, the closed-loop values are easily calculated. The value for the closed-loop gain is

$$A_{CL} = \frac{v_2}{i_s} = \frac{A_{OL}}{1 + A_{OL}\beta} \tag{23.64}$$

The closed-loop input impedance is

$$R_{inf} = \frac{R_i}{1 + A_{OL}\beta} \tag{23.65}$$

and the value for the closed-loop output impedance is

$$R_{of} = R_{out} = \frac{R_o}{1 + A_{OL}\beta} \tag{23.66}$$

We should be able to see a trend in the feedback effects. Shunt mixing and shunt sampling cause the input and output impedances to decrease by the factor $(1 + A_{OL}\beta)$. Similarly, series input mixing and series sampling cause the input and output impedances to increase by the factor $(1 + A_{OL}\beta)$.

In many cases, the overall gain is expressed in terms of a voltage gain, $\frac{v_2}{v_1}$. Since we have calculated the transfer function in terms of the current, i_s, we can easily express this in terms of v_1 by

$$\frac{v_2}{v_1} = \frac{v_2}{i_s(R_{inf})} = A_{CL}\left(\frac{1}{R_{inf}}\right) \tag{23.67}$$

23.5.1 Simple Feedback Using a Gate-Drain Resistor

One of the most popular and simplest examples of shunt-shunt feedback is seen in Fig. 23.25 and consists of a simple inverting amplifier with a resistor connecting the gate and the drain. The feedback resistor, R_2, is usually a large value and serves several important functions. When analyzing the DC characteristics of this circuit, the voltage at the drain will be equal to the voltage on the gate, since there is no DC current flowing through R_2 (when the input is AC coupled). This ensures that the device is always in saturation and provides biasing with no other components needed. We will examine the effects of R_2 on the AC response of the amplifier and soon discover that it has little effect on the gain of the amplifier as well.

Figure 23.26a and b shows the small-signal models for the closed and open-loop circuits, respectively. Since the feedback resistor sums current at the gate of M1, the mixing circuit is shunt. And since the feedback is taken off of the same node as the

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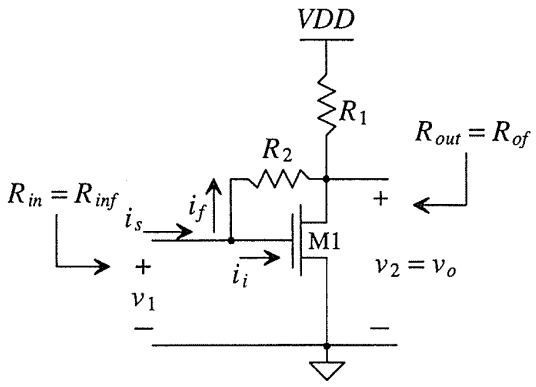


Figure 23.25 Shunt-shunt feedback using a simple gate-drain connected device.

output, the sampling circuit is shunt. Therefore, the value of $R_{\beta i}$ for the open-loop model is found by shorting the output and looking into the feedback loop from the input, and the value of $R_{\beta o}$ is found by shorting the input and looking into the feedback loop from the output.

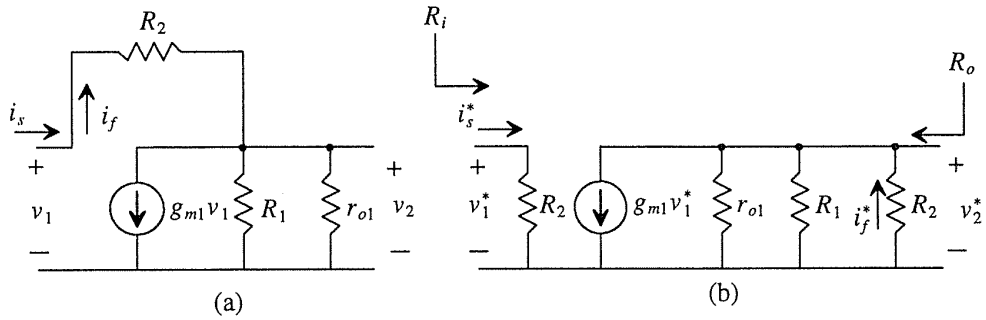


Figure 23.26 Small-signal model of Fig. 23.25: (a) the closed-loop model and (b) the open-loop model.

The open-loop values can be calculated as

$$A_{OL} = \frac{v_2^*}{i_s^*} = \frac{v_2^*}{v_1^*} \cdot \frac{v_1^*}{i_s^*} = [-g_{m1}(R_1||R_2||r_{o1})][R2] \text{ V/A} \tag{23.68}$$

$$R_i = R_2 \tag{23.69}$$

$$R_o = R_1||R_2||r_{o1} \tag{23.70}$$

and

$$\beta = \frac{i_f^*}{v_2^*} = -\frac{1}{R_2} \tag{23.71}$$

Using Eqs. (23.43) - (23.46), we find that the closed-loop values become

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$$A_{CL} = \frac{v_2}{i_s} = \frac{A_{OL}}{1 + A_{OL}\beta} = \frac{-g_{m1}R_oR_2}{1 + g_{m1}R_oR_2\frac{1}{R_2}} \tag{23.72}$$

$$R_{inf} = \frac{v_1}{i_s} = \frac{R_2}{1 + g_{m1}R_oR_2\frac{1}{R_2}} \text{ and } R_{of} = \frac{R_o}{1 + g_{m1}R_oR_2\frac{1}{R_2}} \tag{23.73}$$

The value of R_{inf} is also equal to the value of R_{in} since no source resistance is associated with v_1. Notice that the value of the closed-loop gain is dependent on R_2. However, most applications of this amplifier use voltage as the input variable. Therefore, the value of the overall voltage gain becomes

$$\frac{v_2}{v_1} = \frac{v_2}{i_s} \cdot \frac{i_s}{v_1} = A_{CL} \cdot \frac{1}{R_{inf}} = -g_{m1}R_o = -g_{m1}(R_1 || R_2 || r_{o1}) \tag{23.74}$$

and if the value of R_2 is chosen to be much larger than R_1 then its effect on the AC midband gain is minimized.

Example 23.2

Calculate the gain, $\frac{v_o}{v_s}$, of the shunt-shunt amplifier in Fig. 23.27 assuming that A = 500,000 V/A, R_i = 10 Ω, and R_o = 10 Ω. Notice that the circuit is similar to a simple inverting op-amp.

First, we will source transform the voltage source to a current source, since the input mixing is shunt. The model of the amplifier is in terms of A, not A_{OL}, since we must now include the loading of the feedback resistor, and R_L and R_S in the calculation of A_{OL}. The basic amplifier circuit, a transimpedance amplifier with units of V/I, has an ideal input and output impedance of 0 Ω. Next, we will determine the loading of the β network consisting of R_F on the basic amplifier as seen in Fig. 23.28. A_{OL} can be determined as

$$A_{OL} = \frac{v_o^*}{i_s^*} = -A \cdot \left(\frac{R_F || R_L}{R_F || R_L + R_o}\right) \cdot \left(\frac{R_s || R_F}{R_s || R_F + R_i}\right) \Omega$$

$$= -500{,}000 \cdot 0.989 \cdot 0.989 = -489{,}060 \text{ V/A}$$

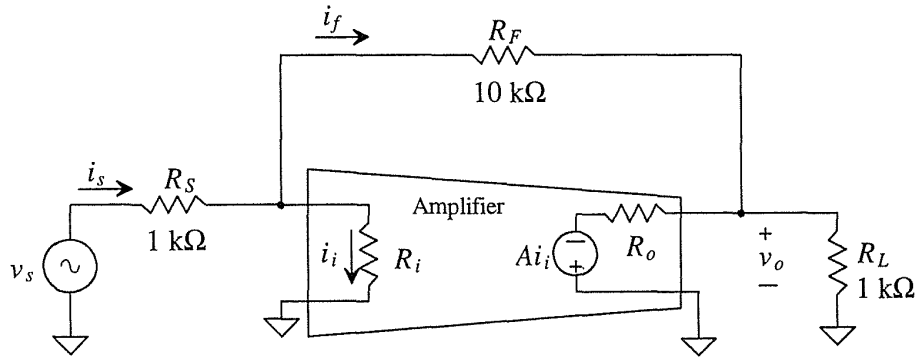


Figure 23.27 A transimpedance amplifier example.

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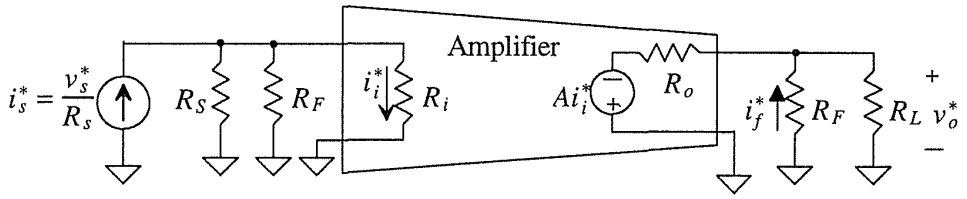


Figure 23.28 Open-loop transimpedance amplifier used in Example 23.2.

The value of β is easily calculated as

$$\beta = \frac{i_f^*}{v_o^*} = -\frac{1}{R_f} = -0.0001 \text{ A/V}$$

And A_{CL} becomes

$$A_{CL} = \frac{v_o}{i_s} = \frac{-489,060}{1 + -489,060 \cdot -0.0001} = -9.8\,\text{k}\Omega \approx R_F$$

Since $v_s = i_s \cdot R_s$, the overall voltage gain is given by

$$\frac{v_o}{v_s} = \frac{v_o}{i_s} \cdot \frac{1}{R_s} = A_{CL} \cdot \frac{1}{R_s} = -\frac{9.8\text{k}}{1\text{k}} = -9.8 \text{ V/V} \approx -\frac{R_F}{R_s}$$

Notice that this is the gain of the standard inverting op-amp configuration. ■

23.6 The Transconductance Amp (Series-Series Feedback)

A series-series feedback amp with open-loop values is shown in Fig. 23.29. Ideally, the values of $R_{\beta i}$ and $R_{\beta o}$ are zero. The feedback resistor R_F is in series with the input and the output of the amplifier. Therefore, the input of the amplifier is a voltage, and the output is a current. The units of A_{OL} will be I/V (a transconductance), and the units of β will be V/I (ohms). Transconductance amplifiers also have high-input and high-output impedance.

The closed-loop gain of the transconductance amplifier is

$$A_{CL} = \frac{i_o}{v_s} = \frac{A_{OL}}{1 + A_{OL}\beta} \text{ A/V} \qquad (23.75)$$

The input impedance is again given by applying a test voltage to the input of the feedback amp and calculating the current that flows into the input of the amplifier. Also, the assumption that the feedback network does not load the amplifier will be used. Setting $v_{test} = v_s$, $i_{test} = i_s$ and writing a loop at the input of the amplifier give

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$$v_{test} = i_{test} \cdot R_i + v_f = i_{test} \cdot R_i + \beta \cdot A_{OL} \cdot i_{test} \cdot R_i \tag{23.76}$$

and so the input resistance with feedback is now

$$R_{inf} = \frac{v_{test}}{i_{test}} = R_i \cdot (1 + A_{OL}\beta) \text{ for } R_o \to \infty \tag{23.77}$$

keeping in mind that $i_{test} \cdot R_i = v_i$ and $A_{OL} \cdot v_i = i_o$. The output resistance is determined by applying a test current at the output with the input source shorted, and is given by

$$v_{test} = (i_{test} - A_{OL}v_i) \cdot R_o = [i_{test} - A_{OL} \cdot (-\beta i_{test})] \cdot R_o \tag{23.78}$$

since $i_{test} = i_{out}$, $v_i = -v_f$, and $R_{\beta o} = 0$. The output resistance is given by

$$R_{of} = \frac{v_{test}}{i_{test}} = R_o \cdot (1 + A_{OL}\beta) \tag{23.79}$$

The ideal transconductance amplifier has infinite output and input resistance. Again, feedback helps to make the amplifier appear closer to the ideal.

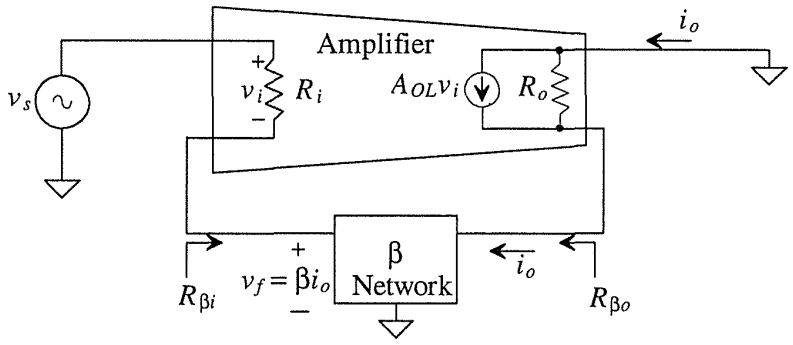


Figure 23.29 An ideal transconductance amplifier.

Now examine the transistor level circuit in Fig. 23.30. Notice the similarity to Fig. 23.13, the circuit used in the series-shunt example; the only difference is the location of the output connection. The feedback loops in both circuits are identical, so the feedback in Fig. 23.30 is known to be negative.

Since the output and the feedback are connected to two separate terminals of the output device, the output variable is a current, sampling i_o. The small-signal model for this circuit is shown in Fig. 23.31 with the open-loop, small-signal model shown in Fig. 23.32. Since the output sampling is a current, loading of the β network will be slightly different from that of the series-shunt example. The input utilizes series mixing; therefore the loading of the β network on the output will be identical to the series-shunt example discussed previously ($R_{\beta o} = R_1 + R_2$). However, since the output sampling is

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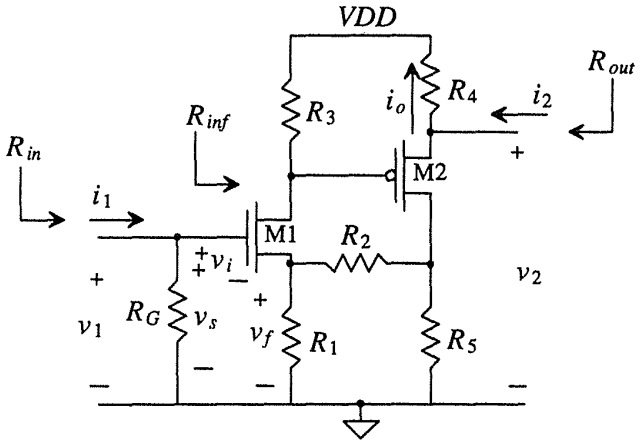


Figure 23.30 Transistor-level series-series feedback amplifier.

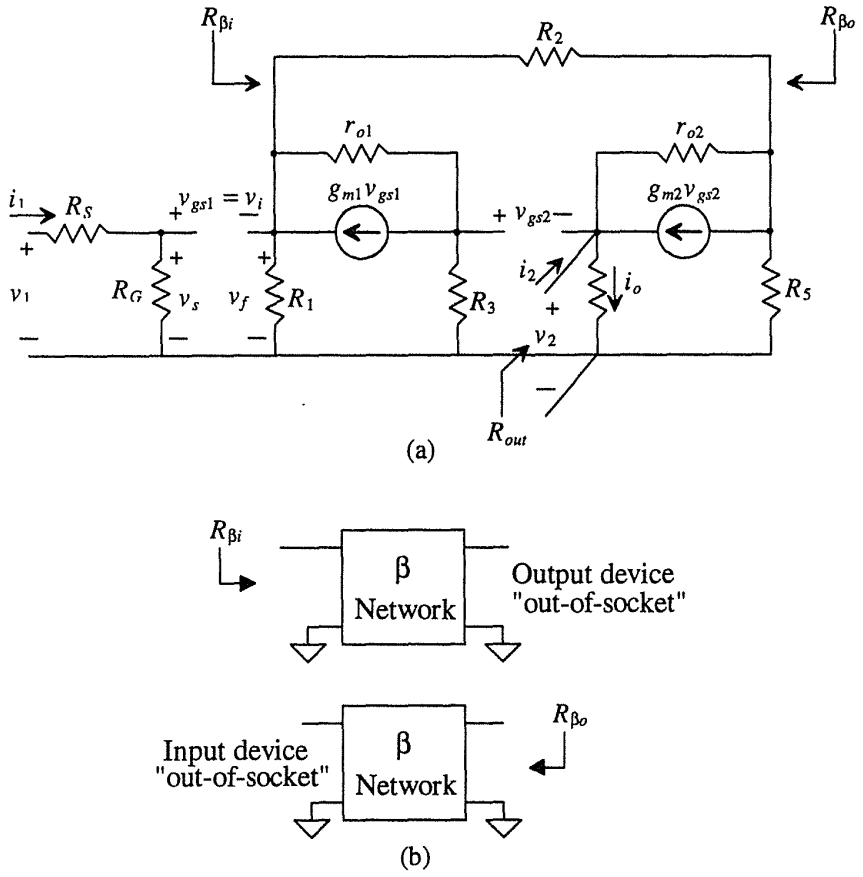


Figure 23.31 (a) Closed-loop small-signal model of Fig. 23.30 and (b) method for determining feedback loading.

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series, the equivalent resistance, $R_{\beta i}$, will be the resistance seen looking into the β network from the input, with the output device taken "out-of-socket" and $R_{\beta i} = R_2 + R_5$.

Once the open-loop model has been constructed, A_{OL} can be calculated as

$$A_{OL} = \frac{i_o^*}{v_s^*} = \frac{i_o^*}{v_{g2}^*}\frac{v_{g2}^*}{v_s^*} \tag{23.80}$$

where the term, $\frac{i_o^*}{v_{g2}^*}$, can be determined by using straightforward circuit analysis to solve $\frac{v_2^*}{v_{g2}^*}$ and then dividing the result by R_4,

$$\frac{i_o^*}{v_{g2}^*} = \frac{g_{m2}}{1 + g_{m2}R_4 + \frac{R_4 + R_5 \| (R_2 + R_1)}{r_{o2}}} \tag{23.81}$$

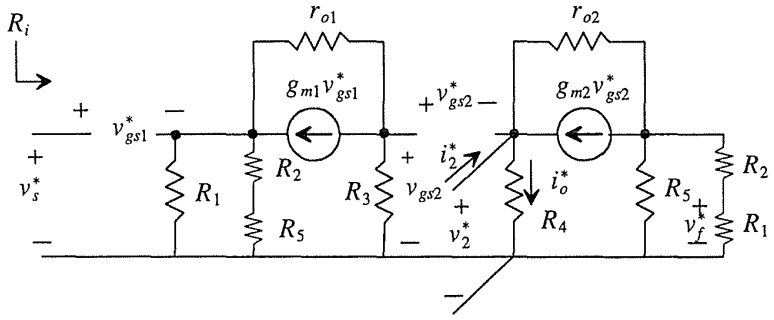


Figure 23.32 Open-loop small-signal model of Fig. 23.30.

The term, $\frac{v_{g2}^*}{v_s^*}$, is found by using the G_M method presented in the previous section on shunt-shunt feedback and is

$$\frac{v_{g2}}{v_s^*} = \frac{-g_{m1}(R_3 \| [(1 + g_{m1}R_A)r_{o1} + R_A)]}{1 + g_{m1}R_A + \frac{R_A}{r_{o1}}} \text{ mhos} \tag{23.82}$$

where $R_A = R_1 \| (R_2 + R_5)$. The feedback factor, β, is

$$\beta = \frac{v_f^*}{i_o^*} \approx \frac{-R_5 R_1}{R_5 + R_1 + R_2} \ \Omega \tag{23.83}$$

And the closed-loop gain is simply

$$A_{CL} = \frac{i_o}{v_s} = \frac{A_{OL}}{1 + A_{OL}\beta} \text{ mhos} \tag{23.84}$$

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The value of R_i is obviously infinite, resulting in an identical value of R_{inf}. Therefore, $R_{in}=R_{inf}||R_G=R_G$.

Calculating R_o for a series output requires some explanation. Examine Fig. 23.33. The value of R_o is the value seen looking in series with the load resistor. In this case, the value of R_o becomes

$$R_o = R_4 + \frac{\frac{R_B}{r_{o2}}+1}{\frac{1}{r_{o2}}+g_{m2}} \approx R_4 + \frac{1}{g_{m2}} \tag{23.85}$$

where $R_B = R_5||(R_1+R_2)$and the closed-loop value becomes

$$R_{of} = R_o(1+A_{OL}\beta) \tag{23.86}$$

Notice, however, that R_{of} is not the same as R_{out}, in this case. Typically, R_{out} is designated as the resistance in parallel with the load. Taking the resistance in series with the load is not a practical specification. Therefore, the resistance R_{out} can be described as seen in Fig. 23.34. In part (a), it can be seen that $R_{of} = R_o(1+A_{OL}\beta)$ and that $R'_{of} = R_{of} - R_4$. If we want to find a value for R_{out}, using Fig. 23.34b, R_{out} is simply

$$R_{out} = R_4||R'_{of} = R_4||(R_{of}-R_4) \tag{23.87}$$

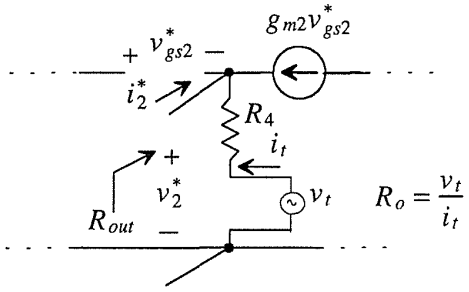


Figure 23.33 Calculation of the output impedance for the circuit in Fig. 23.30.

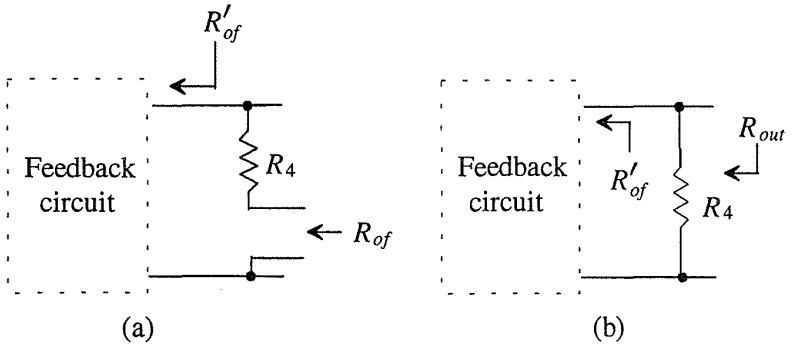


Figure 23.34 Determining the output resistance of a series sampling circuit.

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23.7 The Current Amplifier (Shunt-Series Feedback)

The last feedback topology to be discussed is the shunt-series feedback amplifier, also known as a current amplifier. As can be expected, both A_{OL} and β have units of I/I, and we can expect the input impedance to be very low and the output impedance very high. Figure 23.35 illustrates the ideal shunt-series amplifier with open-loop values included. Based on past derivations, we can expect that

$$R_{inf} = \frac{R_i}{(1 + A_{OL}\beta)} \tag{23.88}$$

and R_{of} to be

$$R_{of} = R_o(1 + A_{OL}\beta) \tag{23.89}$$

The derivations of this topology will be left to the reader in the Problems section.

The transistor-level circuit shown in Fig. 23.36 is similar to the shunt-shunt topology, except for the placement of the output signal. The reader will also be asked to analyze the shunt-series circuit in the Problems section.

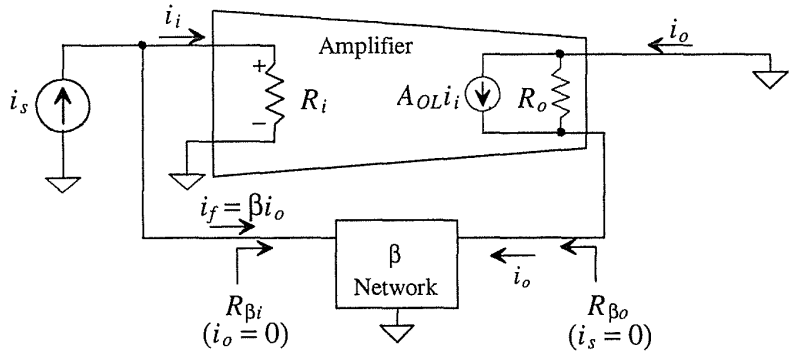


Figure 23.35 An ideal current feedback amplifier.

Example 23.3

Examine the current amplifier seen in Fig. 23.37a. Using feedback analysis, draw open-loop small-signal models and derive values for A_{OL}, β, R_i, R_o, R_{out}, and the overall voltage gain, $\frac{v_2}{v_1}$.

Notice that although this circuit is similiar to the cascode current sink, we can also use it, though unconventionally, as a voltage op-amp. The analysis begins by identifying the feedback circuit. The current summation that occurs at the gate of M4 indicates that shunt mixing is utilized. Since the output and the feedback are taken off separate terminals of the output device, the output sampling is series. The open-loop model is seen in Fig. 23.37b. The only loading on the input due to the feedback network is r_{o2}, since M4 can be taken

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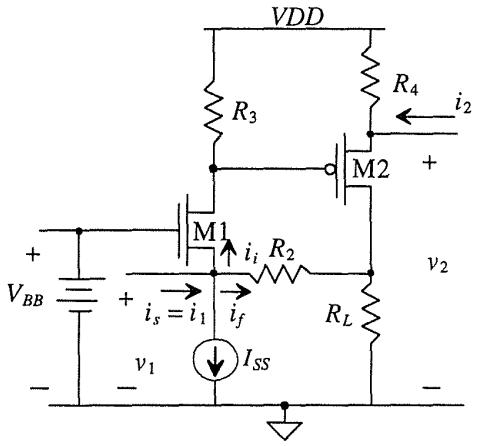


Figure 23.36 A shunt-series feedback amplifier.

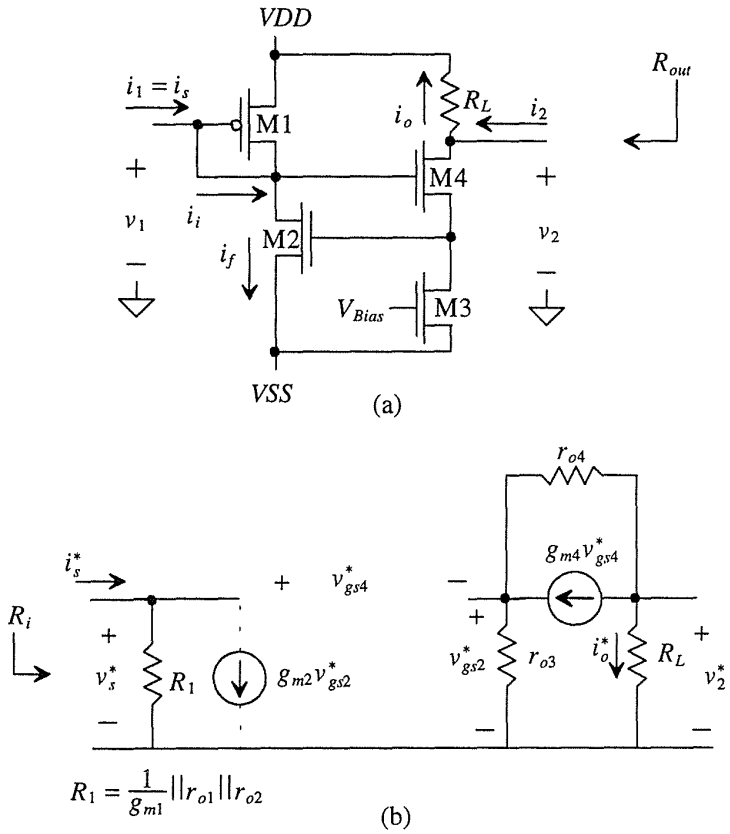


Figure 23.37 (a) Circuit used in Ex. 23.3 and (b) the open-loop model.

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"out-of-socket" ($v_{gs2} = 0$). The feedback does not load the output at all. However, we must remember to include the controlled source for determining i_f. The dependent source, $g_{m2}v_{gs}$, will not be included in calculating A_{OL} but will be needed for calculating β. Solving this open-loop circuit for A_{OL} yields (see Problem 23.28):

$$A_{OL} = \frac{i_o^*}{i_s^*} = \frac{v_2^*}{v_s^*} \cdot \frac{R_1}{R_L} = \frac{-g_{m4}(R_L || ((1+g_{m4}r_{o3})r_{o4} + r_{o3}))}{1 + g_{m4}r_{o3} + \frac{r_{o3}}{r_{o4}}} \cdot \frac{R_1}{R_L} \approx \frac{-g_{m4}R_1}{1 + g_{m4}r_{o3} + \frac{r_{o3}}{r_{o4}}} \text{ A/A}$$

The output, R_o, is found by the same manner presented in the discussion of series-series amplifiers and is

$$R_o = R_L + (1 + g_{m4}r_{o3})r_{o4} + r_{o3}$$

Similiarly, the value of R_{out} becomes

$$R_{out} = (R_o(1 + A_{OL}\beta) - R_L) || R_L$$

and R_i is simply R_1, with

$$R_{if} = \frac{R_1}{1 + A_{OL}\beta}$$

The feedback variable is $i_f^* \approx g_{m2}v_{gs2}^* = -g_{m2}i_o^*r_{o3}$, and the value of β can be calculated as

$$\beta = \frac{i_f^*}{i_o^*} = -g_{m2}r_{o3} \text{ A/A}$$

The overall voltage gain is

$$\frac{v_2}{v_1} = \frac{i_o \cdot R_L}{i_s \cdot R_{if}} = \frac{A_{OL}}{1 + A_{OL}\beta} \cdot \frac{R_L}{R_{if}} \text{ V/V} \quad \blacksquare$$

23.8 Stability

The previous sections illustrated the benefits of feedback and the corresponding tradeoff in gain. However, a critical concern must be examined when applying negative feedback. Some circuits will cause a phase shift in the input signal large enough that the feedback becomes positive (the output adds to the original input), resulting in an unstable system. The occurrence of instability can be minimized with some careful analysis of both the open-loop amplifier, A_{OL}, and the feedback network, β.

The loop gain is defined as

$$T = A_{OL}\beta \tag{23.90}$$

Remember that the product of $A_{OL}\beta$ must itself always be positive. By examining the frequency response of the loop gain, T, the overall stability of the system can be

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determined. The stability of the system can be summarized with the following rules and is illustrated in Fig. 23.38.

Case 1: If the change in the phase of $A_{OL}\beta$ is equal to 180° and the magnitude is below 0 dB, the system will be stable.

Case 2: If the change in the phase of $A_{OL}\beta$ is equal to 180° and the magnitude equals 0 dB, the system may or may not be stable.

Case 3: If the change in the phase of $A_{OL}\beta$ is equal to 180° and the magnitude is above 0 dB, the system will be unstable.

One might wonder why the 180° phase shift and the magnitude of 0 dB (gain of 1) are such critical factors. The answer may be better understood with a qualitative rather than a quantitative explanation. In order for positive feedback to occur, the output must be added back to its original input signal. The PA system example illustrates this concept. If the loudspeaker, which represents the output of the system, is added back to the input (the microphone), the system becomes unstable because the amplifier is attempting to amplify its own output. The result is a loud, high-pitched, ringing sound, which most people have unfortunately experienced.

In negative feedback applications, the addition of the feedback signal to the original input occurs because of the additional phase shift introduced by the frequency dependent components within A_{OL} and β. Because the feedback signal is already

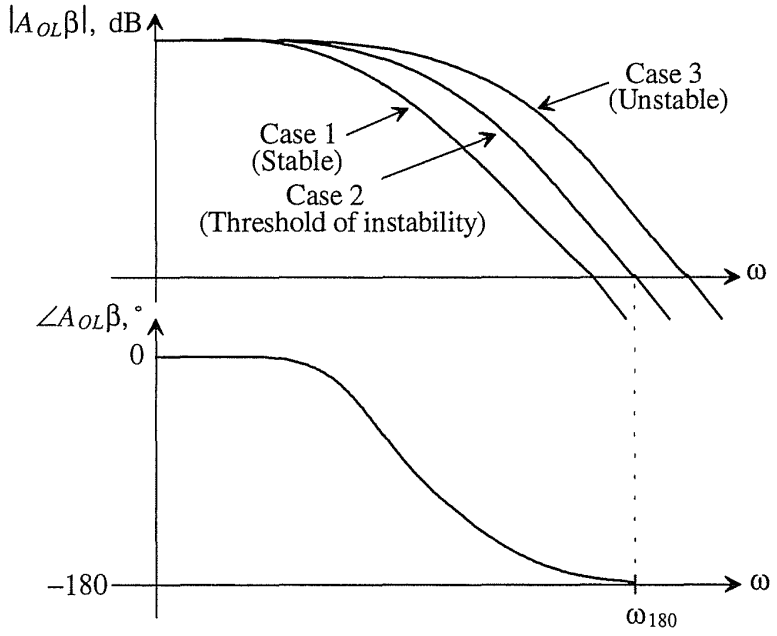


Figure 23.38 Stability analysis using the frequency response of the loop gain.

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inverted with respect to the input, an additional 180° of phase shift will cause the feedback signal to be positive with respect to the input. It is this second 180° degrees of phase shift that becomes the important concern. Thus, the frequency response of the loop gain must be examined. The magnitude of 0 dB is also important. If the gain around the loop is less than 1, the output settles to a stable value. However, if the gain around the loop is greater than 1, the amplifier output grows and becomes unstable quickly.

Assume that A_{OL} can be described with the following frequency response:

$$A_{OL}(s) = -\frac{10}{\left(1+\frac{s}{10}\right)^2} \tag{23.91}$$

Two poles exist at $\omega = 10$ rad/s with a gain at DC equal to –10 V/V. Also assume that β is frequency dependent and has a single pole at $\omega = 10$ rad/s:

$$\beta = \frac{-1}{(\frac{s}{10}+1)} \tag{23.92}$$

The loop gain then, is

$$A_{OL}\beta = \frac{10}{\left(1+\frac{s}{10}\right)^2} \cdot \frac{1}{\left(\frac{s}{10}+1\right)} \tag{23.93}$$

The Bode plot of the loop gain can be seen in Fig. 23.39. It can be seen that since the phase plot crosses 180° slightly before the magnitude plot crosses 0 dB, the system is unstable.

A more precise method of performing the same analysis will now be described. We can use the exact formulas to solve for the exact frequency which the phase plot crosses 180°. The phase of the loop gain, by definition, is

$$\begin{aligned} Arg[A_{OL}(j\omega)\beta(j\omega)] = {} & \tan^{-1}\left(\frac{\omega}{z_1}\right) + \tan^{-1}\left(\frac{\omega}{z_2}\right) + ... + \tan^{-1}\left(\frac{\omega}{z_n}\right) \\ & - \tan^{-1}\left(\frac{\omega}{p_1}\right) - \tan^{-1}\left(\frac{\omega}{p_2}\right) - .... - \tan^{-1}\left(\frac{\omega}{p_n}\right) \end{aligned} \tag{23.94}$$

where $z_1, z_2 \ldots z_n$ are the zeros in the system and $p_1, p_2 \ldots p_n$ are the poles. Since our example has three poles at the same frequency and no zeros, the phase response of the loop gain can be expressed as

$$Arg[A_{OL}(j\omega)\beta(j\omega)] = -3\tan^{-1}\left(\frac{\omega_{180}}{10}\right) = -180 \tag{23.95}$$

where ω_{180} is the frequency at which the phase response is equal to –180°. Solving for ω_{180} yields

$$\omega_{180} = 17.32 \text{ rad/s} \tag{23.96}$$

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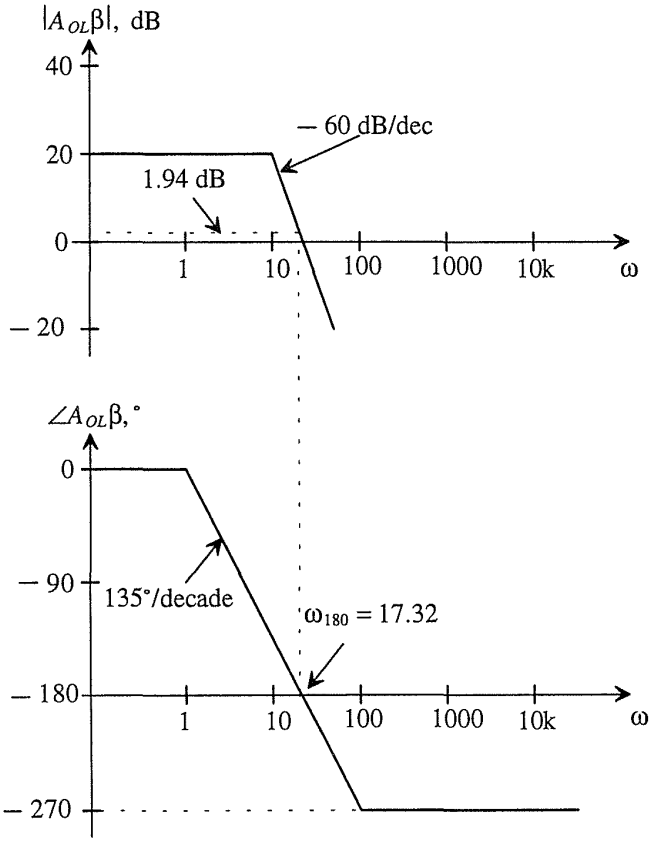


Figure 23.39 Stability analysis using the frequency response of the loop gain.

The magnitude of the loop gain is defined as,

$$20\text{Log}|A_{OL}(j\omega)\beta(j\omega)| = 20\text{Log}(A_o) + 20\text{Log}\sqrt{\left(\frac{\omega}{z_1}\right)^2 + 1} + 20\text{Log}\sqrt{\left(\frac{\omega}{z_2}\right)^2 + 1} + ..$$

$$+ 20\text{Log}\sqrt{\left(\frac{\omega}{z_n}\right)^2 + 1} - 20\text{Log}\sqrt{\left(\frac{\omega}{p_1}\right)^2 + 1} - .. - 20\text{Log}\sqrt{\left(\frac{\omega}{p_n}\right)^2 + 1} \qquad (23.97)$$

where, z_1, z_2 . . . z_n are the zeros of the system, p_1, p_2, . . . p_n are the poles, and A_o is the midband gain. Plugging in the value for ω_{180} into Eq. (23.97), we can solve for the magnitude of the loop gain at the point at which its phase is –180°:

$$20\text{Log}|A_{OL}(j\omega)\beta(j\omega)| = 20\text{Log}(10) - 3\left(20\text{Log}\sqrt{\left(\frac{17.32}{10}\right)^2 + 1}\right) \qquad (23.98)$$

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$$|A_{OL}(j\omega_{180})\beta(j\omega_{180})| = 1.94 \text{ dB} \quad (23.99)$$

which, using rule 3, verifies that the system is unstable.

Stability is typically measured using two specifications: gain margin and phase margin. Gain margin is defined as the difference between the magnitude of $A_{OL}\beta$ at ω_{180} and unity, whereas phase margin is defined as the difference between the value of the phase at the frequency in which the magnitude of $A_{OL}\beta$ is equal to unity and ω_{180}. Figure 23.40 illustrates both definitions. It should be noted that phase margin is the typical specification used for stability. Amplifiers should be designed to have a phase margin of at least 45°, though 60° phase margin is more acceptable.

In our previous discussion, only the frequency domain analysis was considered. The effect of phase margin in the time domain is related to settling time. As the phase margin increases, less time is required for the signal to settle. As the phase margin approaches 0°, the signal will oscillate indefinitely.

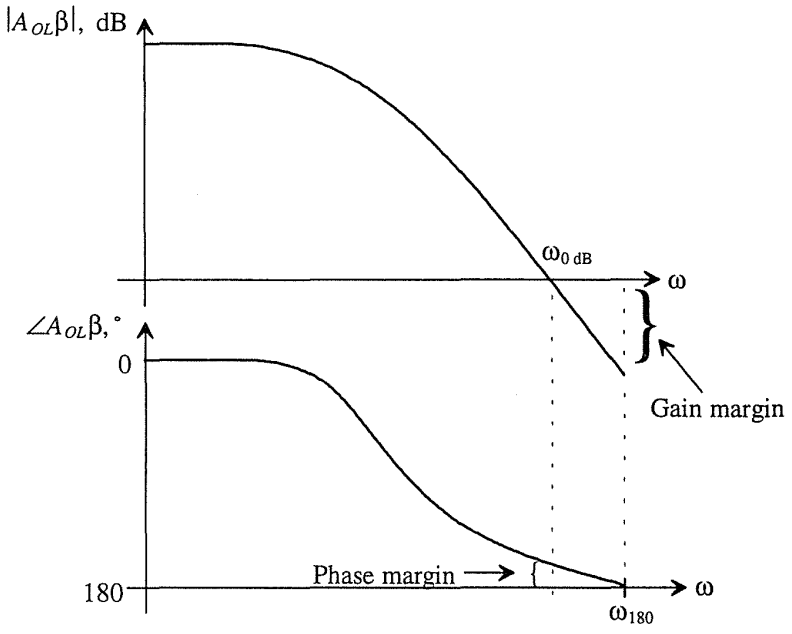


Figure 23.40 Gain margin and phase margin definitions.

23.8.1 The Return Ratio

In some cases, it may be more practical to determine the loop gain from a system point of view. One method used to determine a good approximation of the loop-gain frequency response is to break the loop, input a test signal, and determine the returned value back to the point that the loop was broken. This method is called the return ratio

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(*RR*) method. Consider the block diagram of the single-loop structure in Fig. 23.41 with the loop "open." The gain around the loop is,

$$RR = \frac{x_f}{x_i} = -T = -A_{OL}\beta \tag{23.100}$$

This gain represents the path from the input back around through the feedback network. It should be noted that the *RR* method may vary quite extensively from the two-port method in finding the value of $A_{OL}\beta$, but for purposes of plotting the loop gain frequency response, the *RR* should be sufficient [3].

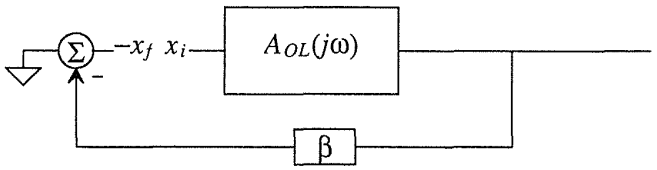


Figure 23.41 Determining the loop gain by opening the feedback loop.

The *RR* is found by first replacing all independent sources with their ideal impedances. Next, a dependent source is chosen, and the feedback loop is broken between the chosen source and the rest of the circuit. An independent test source is inserted at the node where the dependent source resided and a test signal is injected into the loop. The *RR* is then the ratio of the returned signal (which now appears across the dependent source) and the test signal, such that

$$RR = -\frac{v_r}{v_t} \tag{23.101}$$

An example will illustrate this method further.

Example 23.4

Determine the *RR* for the series-shunt op-amp circuit shown in Fig. 23.42a and compare that value to the value $A_{OL}\beta$ using the two-port method. Assume that the op-amp can be modeled as shown in Fig. 23.42b.

Since there is only one dependent source in the circuit, deciding where to break the loop is a simple endeavor. Next, the dependent source is separated from the rest of the circuit, and an independent source, v_t, is put in its original position as seen in Fig. 23.43a. The returned signal is now across the dependent source. By inspection, the value of the *RR* can be found to be

$$RR = -\frac{v_r}{v_t} = A \cdot \left(\frac{R_I \| R_1}{R_I \| R_1 + R_2}\right) \cdot \left(\frac{R_2 + R_I \| R_1}{R_2 + R_I \| R_1 + R_o}\right) = 49,726$$

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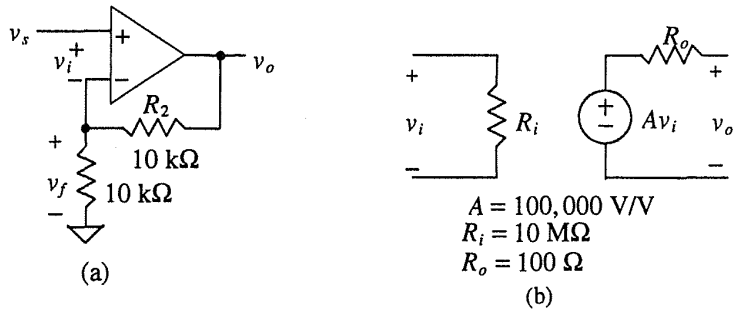


Figure 23.42 (a) A series-shunt amplifier used in Ex. 23.4 and (b) the model used for the op-amp.

Next, the open-loop model for the original circuit is found using the two-port analysis presented in Sec. 23.2. The circuit, taking the β network loading effects into account, can be seen in Fig. 23.43b. The value of A_{OL} is easily calculated as

$$A_{OL} = \frac{v_o^*}{v_s^*} = A \cdot \left(\frac{R_1 + R_2}{R_o + R_1 + R_2}\right) \cdot \left(\frac{R_I}{R_1 || R_2 + R_I}\right) = 99,497$$

The value of β by inspection is

$$\beta = \frac{v_f^*}{v_o^*} = \frac{R_1}{R_1 + R_2} = 0.5$$

and the value of $A_{OL}\beta$ is

$$A_{OL}\beta = (99{,}497)(0.5) = 49{,}748$$

The two methods yielded very similiar answers. ■

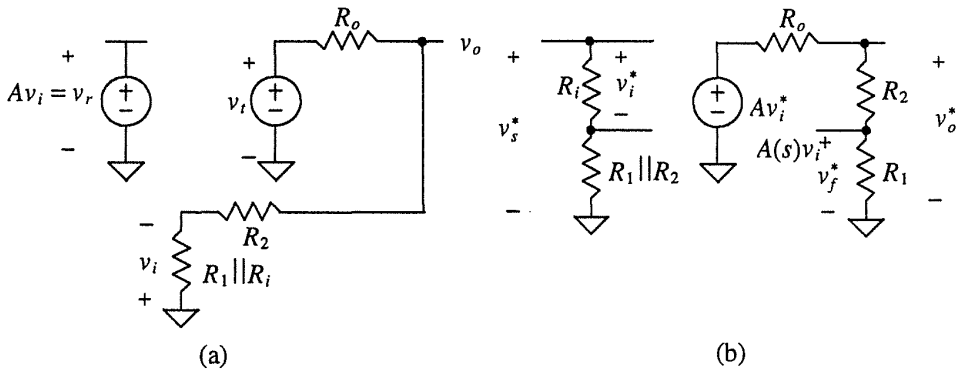


Figure 23.43 (a) The model used to calculate return ratio and (b) the model used for the two-port analysis of loop gain for Fig. 23.42.

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If $A_{OL}\beta$ is frequency dependent, then the phase and gain margin of the circuit can be plotted so as to determine the phase and gain margin. Now suppose that the circuit used in Ex. 23.4 was frequency dependent as seen in Fig. 23.44. Using the same strategy presented in Ex. 23.4 and using the *RR* method, the value of the loop gain becomes

$$RR = -\frac{v_r}{v_t} = \frac{49,726}{(s/200+1)^3} \tag{23.102}$$

The gain and phase margin can then be analyzed to determine if the system is stable (see Problem 23.34).

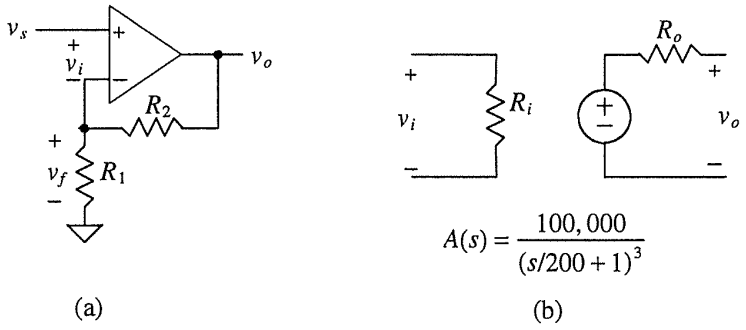


Figure 23.44 (a) A series-shunt amplifier used in Ex. 23.4 and (b) the model used for the op-amp.

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[1] A. S. Sedra and K. C. Smith, *Microelectronic Circuits,* Saunders College Publishing, 1991. ISBN 0-03-051648-X.

[2] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design,* Holt, Rinehart and Winston, 1987. ISBN 0-03-006587-9.

[3] P. J. Hurst, "Exact Simulation of Feedback Circuit Parameters," *IEEE Transactions on Circuits and Systems*, Vol. 38, No. 11, pp. 1382-1389, November 1991.

PROBLEMS

23.1 An op-amp is designed so that the open-loop gain is guaranteed to be 150,000 ± 10 percent V/V. If the amplifier is to be used in a closed-loop configuration with β = 0.1 V/V, determine the tolerance of the closed-loop gain.

23.2 What is the maximum possible value of β using resistors in the feedback loop of a noninverting op-amp circuit? Sketch this op-amp circuit when β = 1/2.

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23.3 Examine the feedback loop in Fig. P23.3. A noise source, v_n, is injected in the system between two amplifier stages. (a) Determine an expression for v_o which includes both the noise and the input signal, v_s. (b) Repeat (a) for the case where there is no feedback ($\beta = 0$). (c) If $A_1 = A_2 = 200$, and feedback is again applied around the circuit, what value of β will be required to reduce the noise by one-half as compared to the case stated in (b)?

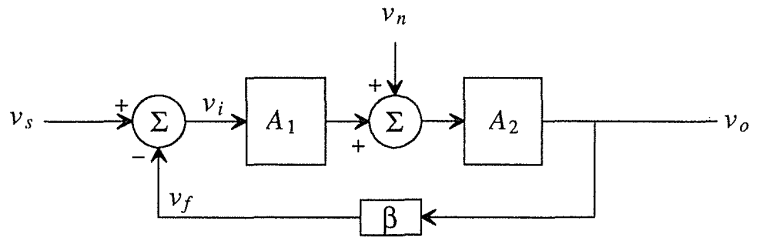


Figure P23.3

23.4 An amplifier can be characterized as follows:

$$A(s) = 10,000 \cdot \frac{100}{s+100} \text{ V/V}$$

A series of these amplifiers are connected in cascade, and feedback is used around each amplifier. Determine the number of stages needed to produce an overall gain of 1,000 with a high-frequency rolloff (at -20 dB/decade) occurring at 100,000 rad/sec. Assume that the first stage produces the desired high-frequency pole and that the remaining stages are designed so that their high-frequency poles are at least a factor of four greater.

23.5 An amplifier can be characterized as follows:

$$A(s) = 1,000 \cdot \frac{s}{s+100} \text{ V/V}$$

and is connected in a feedback loop with a variable β. Determine the value of β for which the low-frequency rolloff is 50 rad/sec. What is the value of the closed-loop gain at that point?

23.6 Make a table summarizing the four feedback topologies according to the following categories: input variable, output variable, units of A_{OL}, units of β, method to calculate $R_{\beta i}$ and $R_{\beta o}$, and expressions for A_{CL}, R_{if}, and R_{of}.

23.7 Using the two n-channel common source amplifiers shown in Fig. P23.7 and the addition of a single resistor, draw (a) a series-shunt feedback amplifier, (b) a series-series feedback amplifier, (c) a shunt-shunt feedback amplifier, and (d) a shunt-series amplifier. For each case, identify the forward and feedback paths, ensure that the feedback is negative by counting the inversions around the loop,

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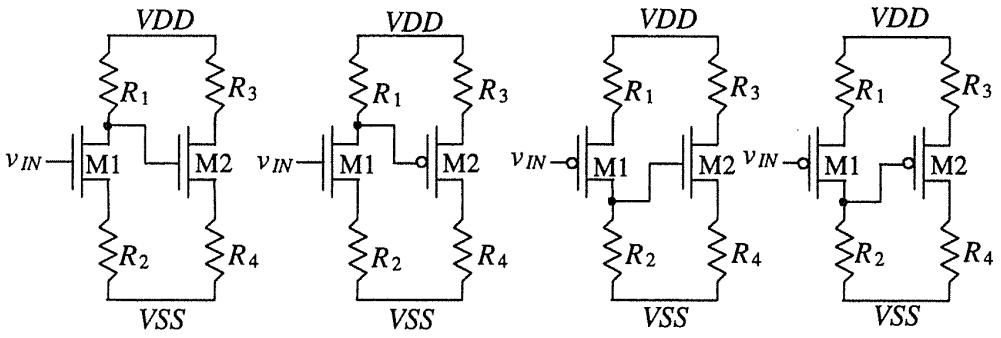


Figure P23.7 Figure P23.8 Figure P23.9 Figure P23.10

and label the input variable, the feedback variable, and the output variable. Assume that the input voltage, v_{IN}, has a DC component that biases M1.

23.8 Repeat Problem 23.7 using the two-transistor circuit shown in Fig. P23.8.

23.9 Repeat Problem 23.7 using Fig. P23.9.

23.10 Repeat Problem 23.7 using Fig. P23.10.

For each of the following feedback analysis problems, assume that the circuit has been properly DC biased and that MOSFETs have been characterized. The n-channel devices have $g_m = 0.06$ A/V and $r_o = 70$ kΩ. The p-channel devices have $g_m = 0.04$ A/V and $r_o = 50$ kΩ.

23.11 Using the series-shunt amplifier shown in Fig. P23.11, (a) identify the feedback topology by labeling the mixing variables and output variable, (b) verify that negative feedback is employed, (c) draw the closed-loop small-signal model, and (d) find the expression for the resistors $R_{\beta i}$ and $R_{\beta o}$.

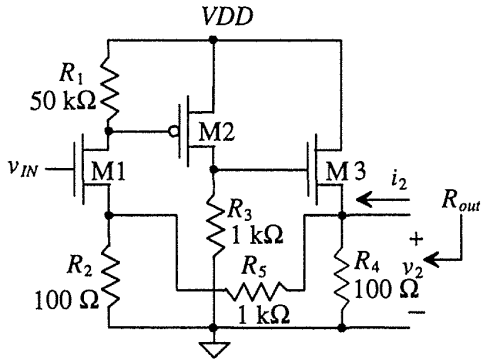


Figure P23.11

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23.12 Using Fig. P23.11 and the results from Problem 23.11, (a) draw the small-signal open-loop model for the circuit and (b) find the expressions for the open-loop parameters, A_{OL}, β, R_i, and R_o and (c) the closed-loop parameters, A_{CL} and R_{out}. Note that finding R_{in} is a trivial matter since the signal is input into the gate of M1.

23.13 Using the series-shunt amplifier shown in Fig. P23.13, (a) verify the feedback topology by labeling the mixing variables and the output variable closed-loop small-signal model and (b) find the values of $R_{\beta i}$ and $R_{\beta o}$.

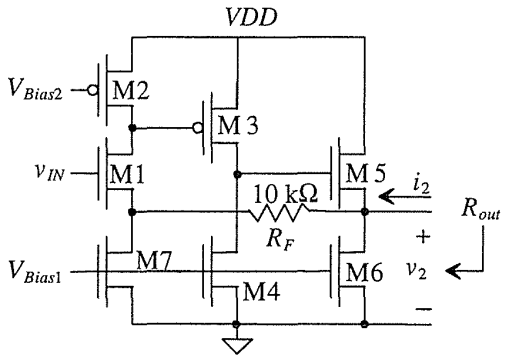


Figure P23.13

23.14 Using the series-shunt amplifier shown in Fig. P23.13 and the results from Problem 23.13, (a) draw the small-signal open-loop model for the circuit and (b) calculate the open-loop parameters, A_{OL}, β, R_i, and R_o and (c) the closed-loop parameters, A_{CL}, and R_{out}. Note that Fig. P23.13 is identical to Fig. P23.11 except the resistors have been replaced with active loads.

23.15 Using the principles of feedback analysis, find the value of the voltage gain, $\frac{v_2}{v_{in}}$ and $\frac{v_2}{i_2}$ for the series-shunt circuit shown in Fig. P23.15.

23.16 A shunt-shunt feedback amplifier is shown in Fig. P23.16. (a) Identify the feedback topology by labeling the input mixing variables and the output variables, (b) verify that negative feedback is employed, (c) draw the closed-loop small-signal model, and (d) find the values of $R_{\beta i}$ and $R_{\beta o}$.

23.17 Using the shunt-shunt amplifier shown in Fig. P23.16 and the results from Problem 23.16, (a) draw the small-signal open-loop model for the circuit and (b) calculate expressions for the open-loop parameters, A_{OL}, β, R_i, and R_o and (c) the closed-loop parameters, A_{CL}, R_{in}, and R_{out}.

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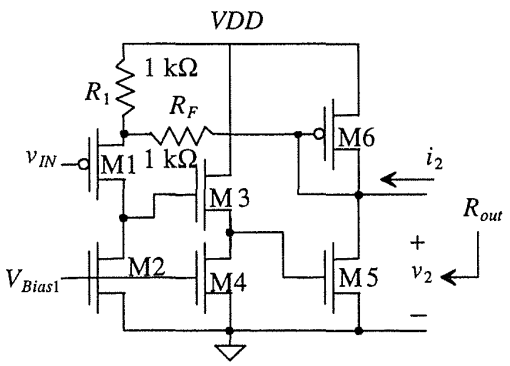


Figure P23.15

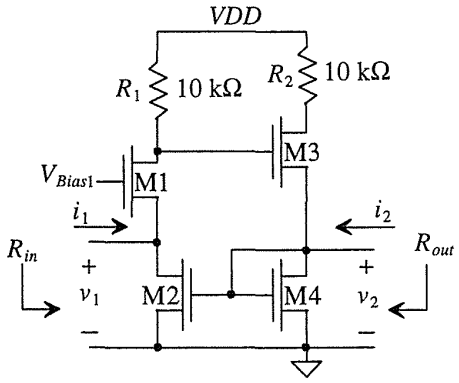


Figure P23.16

23.18 Using the principles of feedback analysis, find the value of the voltage gain, $\frac{v_2}{v_1}$, $\frac{v_1}{i_1}$, and $\frac{v_2}{i_2}$ for the shunt-shunt circuit shown in Fig. P23.18.

23.19 Using the series-series feedback amplifier shown in Fig. P23.19, (a) identify the feedback topology, (b) verify that negative feedback is employed, (c) draw the closed-loop small-signal model, and (d) find the values of $R_{\beta i}$ and $R_{\beta o}$.

23.20 Using the series-series amplifier shown in Fig. P23.19 and the results from

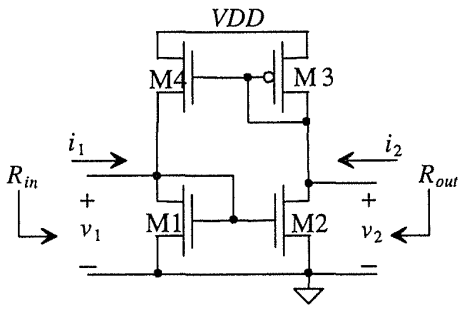


Figure P23.18

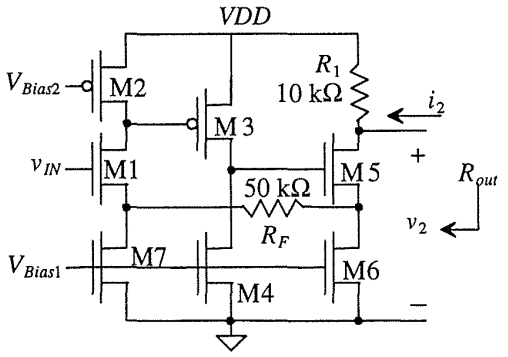


Figure P23.19

problem 23.19, (a) draw the small-signal open-loop model for the circuit and (b) calculate the open-loop parameters, A_{OL}, β, R_i, and R_o and (c) the closed-loop parameters, A_{CL}, R_{in}, and R_{out}.

23.21 Using the shunt-series amplifier in Fig. 23.35, derive the expressions for A_{OL}, R_i, and R_o.

23.22 Convert the shunt-shunt amplifier shown in Fig. P23.16 into a shunt-series feedback amplifier without adding any components. (a) Identify the feedback

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topology, (b) verify that negative feedback is employed, (c) draw the closed-loop small-signal model, and (d) find the values of $R_{\beta i}$ and $R_{\beta o}$.

23.23 Using the shunt-series amplifier from Problem 23.22, (a) draw the small-signal open-loop model for the circuit and (b) calculate the open-loop parameters, A_{OL}, β, R_i, and R_o and (c) the closed-loop parameters, A_{CL}, R_{in}, and R_{out}.

23.24 A feedback amplifier is shown in Fig. P23.24. Identify the feedback topology and determine the value of the voltage gain, $\frac{v_2}{v_1}$, R_{in}, and R_{out}.

23.25 Notice that the amplifier shown in Fig. P23.25 is a simple common source amplifier with source resistance. Explain how this is actually a very simple feedback amplifier and determine the type of feedback used. Determine A_{OL} and β.

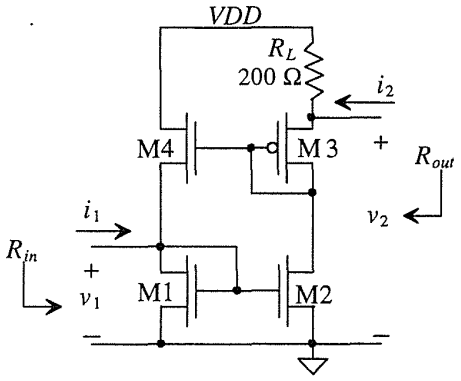


Figure P23.24

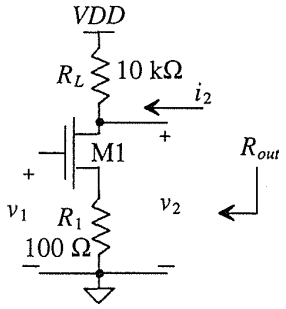


Figure P23.25

23.26 A feedback amplifier is shown in Fig. P23.26. Identify the feedback topology and determine the value of the voltage gain, $\frac{v_2}{v_1}$, R_{in}, and R_{out}.

23.27 A feedback amplifier is shown in Fig. P23.27. Identify the feedback topology and determine the value of the voltage gain, $\frac{v_2}{v_1}$ and R_{out}.

23.28 Prove that the expression for the open-loop gain of Ex. 23.3 is correct.

23.29 Determine if the amplifier seen in Fig. 23.45 is stable.

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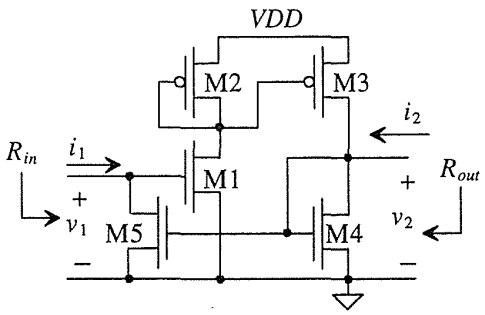


Figure P23.26

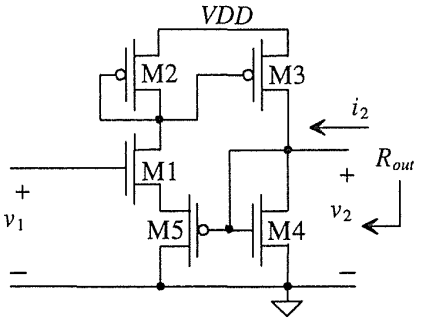


Figure P23.27

23.30 The op-amp shown in Fig. P23.30a can be modeled with the circuit of Fig. P23.30b. With a feedback factor, $\beta = 1$, determine if the op-amp is stable (and the corresponding phase and gain margins) for the following transfer function and $\omega_2 = 10^5$, 10^6, 10^7, and 5×10^6 rad/sec.

$$A_{OL}(j\omega) = \frac{10,000}{\left(1 + j\frac{\omega}{100}\right)\left(1 + j\frac{\omega}{\omega_2}\right)}$$

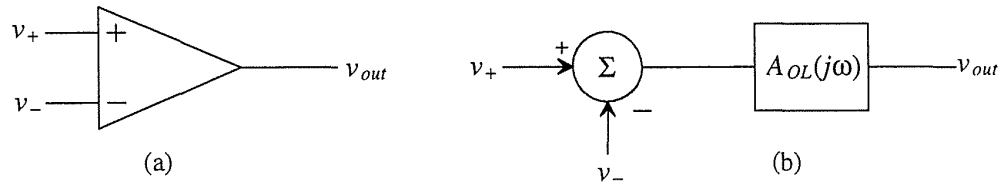


Figure P23.30

23.31 The phase plot of an amplifier is shown in Fig. P23.31. The amplifier has a midband gain of –1,000 and 3 zeros at $\omega = \infty$ and three other unspecified poles. If the amplifier is configured in a feedback configuration and β is frequency independent, what is the exact value of β that would be necessary to cause the amplifier to oscillate?

23.32 You have just measured the gain of the op-amp circuit shown in Fig. P23.32. You know from basic op-amp theory that the gain of the circuit should be $-R_2/R_1$ V/V. However, your measurements with R_2 = 10 kΩ and R_1 = 1 kΩ revealed that the gain was only –5 V/V. What is the open-loop gain of the op-amp?

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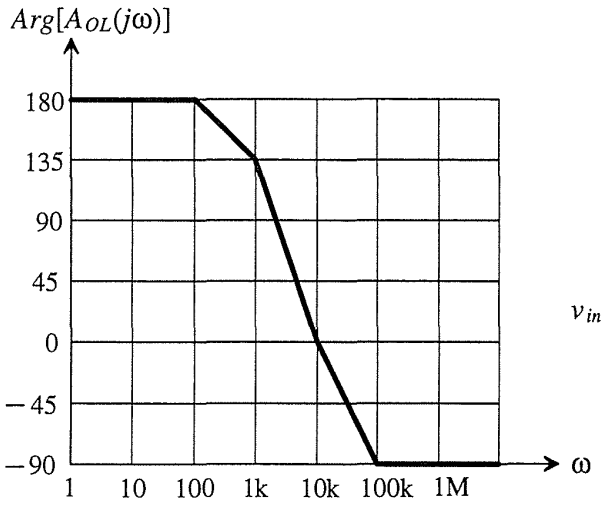


Figure P23.31

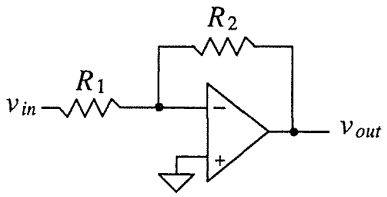


Figure P23.32

23.33 Using the circuit shown in Fig. P23.33 and the *RR* method, find a value of R_1 and A_o which will cause the phase margin to equal 45° at ω = 8,000 rad/sec. The amplifier can be modeled as having an infinite input impedance and zero output resistance and has a frequency response of

$$A(s) = \frac{-A_o}{(s/200+1)(s/10,000+1)}$$

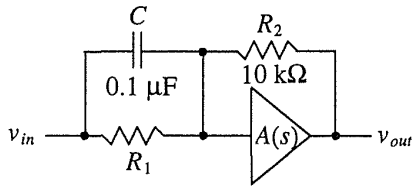


Figure P23.33

23.34 Determine if the system with a return ratio as described by Eq. (23.102) is stable.

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Chapter

24

Differential Amplifiers

This chapter is concerned with the differential amplifier, an amplifier that amplifies the difference between two signals. The diff-amp is a fundamental building block in CMOS analog integrated circuit design, and an understanding of its operation and design is extremely important. In this chapter, we discuss three basic types of differential amplifiers: the source coupled pair, the source cross-coupled pair, and the current differential amplifier.

24.1 The Source Coupled Pair

The source coupled pair comprised of M1 and M2 is shown in Fig. 24.1 [1]. The MOSFET current mirror made using M5 and M6 is used to provide a source current for the pair of I_{SS}. Throughout this book unless otherwise stated, we will assume that M1 and M2 of the source coupled pair are of equal size, so that $\beta_1 = \beta_2 = \beta$. Summing the AC and DC components of the current at the sources of M1 and M2 yields

$$I_{SS} = i_{D1} + i_{D2} \tag{24.1}$$

If we label the input voltages at the gates of M1 and M2 as v_{I1} and v_{I2} we can write the difference as

$$v_{DI} = v_{I1} - v_{I2} = v_{GS1} - v_{GS2} \tag{24.2}$$

or because of the symmetry of the circuit

$$v_{GS1} = -v_{GS2} = \frac{v_{DI}}{2} \tag{24.3}$$

When the gates of M1 and M2 are grounded

$$I_{D1} = I_{D2} = \frac{I_{SS}}{2} \tag{24.4}$$

Since we know that a saturated MOSFET follows the relation

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$$i_D = \frac{\beta}{2}(v_{GS} - V_{THN})^2 \tag{24.5}$$

the difference in the input voltages may be written as

$$v_{DI} = \sqrt{\frac{2}{\beta}}\left(\sqrt{i_{D1}} - \sqrt{i_{D2}}\right) \tag{24.6}$$

Using Eqs. (24.6) and (24.1), we can write expressions for the drain currents of the MOSFETs in saturation in terms of the difference voltage as

$$i_{D1} = \frac{I_{SS}}{2}\left|1 + \sqrt{\left(\frac{\beta v_{DI}^2}{I_{SS}} - \frac{\beta^2 v_{DI}^4}{4I_{SS}^2}\right)}\right| \tag{24.7}$$

and

$$i_{D2} = \frac{I_{SS}}{2}\left|1 - \sqrt{\left(\frac{\beta v_{DI}^2}{I_{SS}} - \frac{\beta^2 v_{DI}^4}{4I_{SS}^2}\right)}\right| \tag{24.8}$$

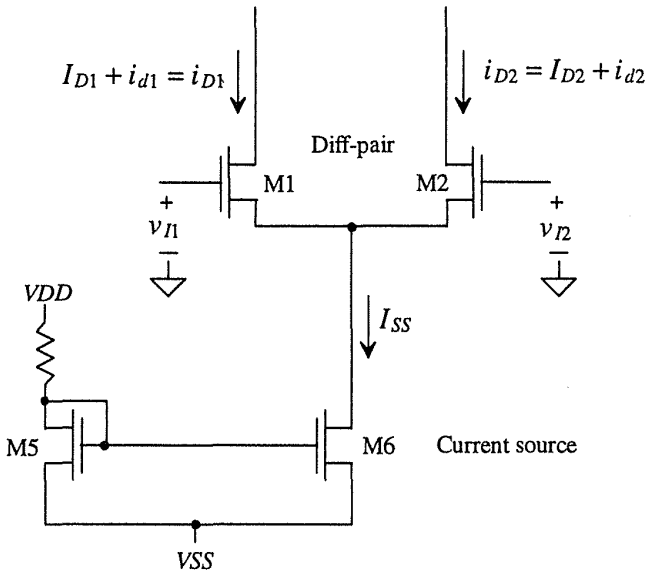


Figure 24.1 Differential amplifier.

In order to understand the operation of this amplifier, let's assume that $v_{I2} = 0$, that is, the gate of M2 is connected to ground, so that $v_{I1} = v_{DI}$. If v_{I1} is held at *VDD*; then M2 is off and M1 conducts the current I_{SS} (i.e., $i_{D1} = I_{D1} = I_{SS}$). If, for linear operation, M1 and M2 are required to remain in the saturation region, then the point at which the input voltage turns M2 off is the same point at which all of I_{SS} begins to flow in M1. If we label the input voltage at this point v_{DIMAX}, then setting Eq. (24.4) equal to

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I_{SS} and realizing at this point that the source potential of the diff-pair is $-V_{THN}$ (due to M2 starting to turn off), we arrive at

$$v_{DIMAX} = \sqrt{\frac{2I_{SS}}{\beta}} \tag{24.9}$$

This result also holds for the case when v_{D2} is not zero or in general:

$$v_{DIMAX} = v_{I1} - v_{I2} = \sqrt{\frac{2I_{SS}}{\beta}} \tag{24.10}$$

Example 24.1

Referring to the diff-amp of Fig. 24.1, if I_{SS} = 10 μA and $W_2 = W_1$ = 15 μm and $L_2 = L_1$ = 5 μm, determine and compare to simulations v_{DIMAX}.

From Eq. (24.9) we have

$$v_{DIMAX} = \sqrt{\frac{2 \cdot 10\,\mu}{50\frac{\mu A}{V^2} \cdot \frac{15}{5}}} = 364 \text{ mV}$$

The simulation results are shown in Fig. 24.2. ■

The minimum difference voltage, when all the current flows in M2, can be determined in a similar manner as

$$v_{DIMIN} = -\sqrt{\frac{2I_{SS}}{\beta}} \tag{24.11}$$

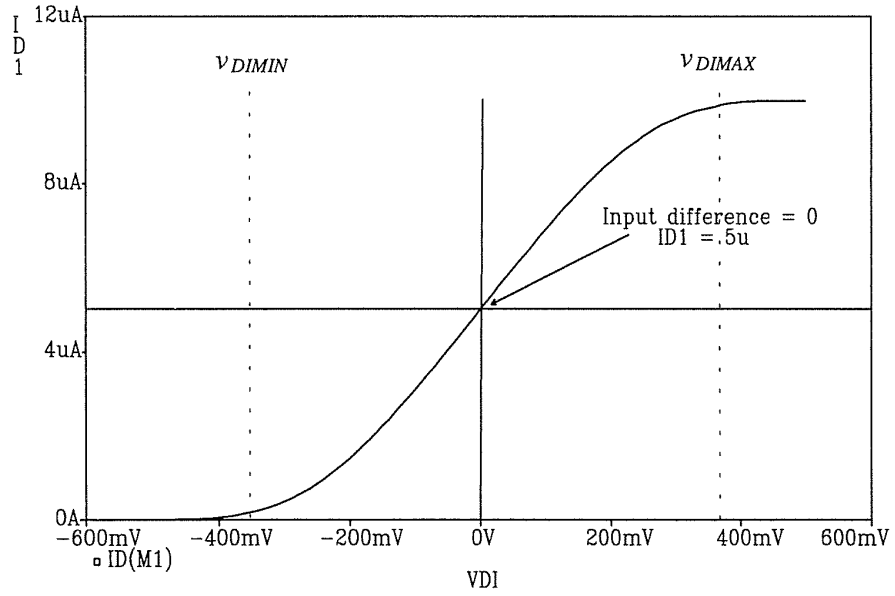


Figure 24.2 Transfer characteristics of the source coupled differential amplifier of Ex. 24.1.

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The transconductance gain of the differential amplifier is given by the slope of the transfer characteristics in Fig. 24.2 between v_{DIMIN} and v_{DMAX} (when M1 and M2 are in the saturation region). This large-signal transconductance is given by

$$G_m = \frac{di_{D1}}{dv_{DI}} = \frac{I_{SS}}{2\sqrt{2I_{SS}/\beta}} = \frac{\sqrt{2\beta I_{SS}}}{4} = \frac{g_m}{4} \tag{24.12}$$

which is of the same form as the small-signal transconductance of a MOSFET. Note that the transconductance can be increased by increasing I_{SS} or making the MOSFETs M1 and M2 larger (wider).

24.1.1 Current Source Load

The CMOS differential amplifier is most often used with a current source load as shown in Fig. 24.3. Consider the case when the gates of M1 and M2 are grounded. Under these circumstances, a current $I_{SS}/2$ flows in M1-M4. The drain voltage of M4 is at the same potential as the gate of M3/M4 (and the drain of M3). Therefore, the potential difference between the drain of M1 and M2 is zero. The fact that the drain of M4 is at the same potential as the gate of M3 is used to bias the next stage at a particular current level. We can select the sizes of the devices similar to the method used in determining the sizes of the current sources and sinks. We begin by selecting a minimum length based on channel length modulation considerations. For the CN20 process, we will use 5 μm for the lengths. The widths are determined by the gate-source voltage of the MOSFETs. In many designs, the *W/L* ratios of the diff-amp with current source load are made very large. The voltage above V_{THN} may be only 0.1 V in these designs. In general, we will set V_{GS} to 1.2 V in our designs. Note that the body effect when using

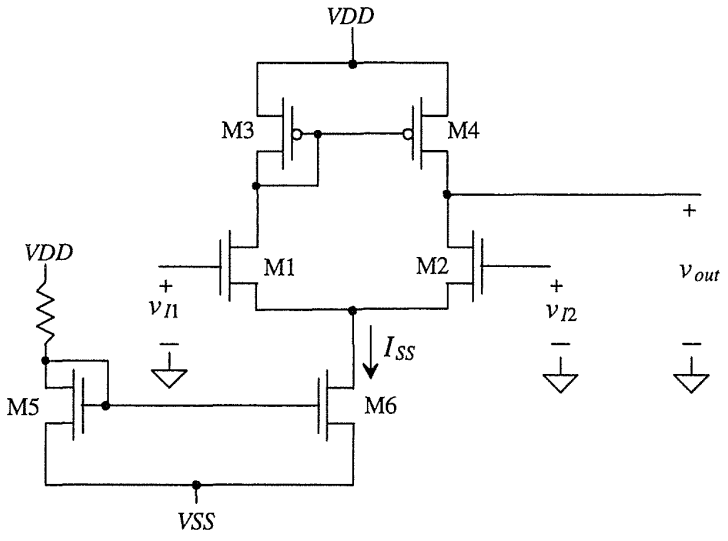


Figure 24.3 Differential amplifier with current source load M3 and M4.

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the n-channel MOSFET diff-amp may increase the threshold voltage of M1 and M2 to approximately 1.2 V. This simply means that the circuit we design will have a V_{GS} of 1.5 V or 0.3 volts above V_{THN}. The benefits of using an n-channel diff-pair in an n-well process are better threshold voltage matching because of the body effect and lower capacitance at the sources of the MOSFETs to AC ground. In a practical case one might use a p-channel MOSFET diff-pair (see Fig. 24.4) on the input of the amplifier in order to eliminate the body effect.

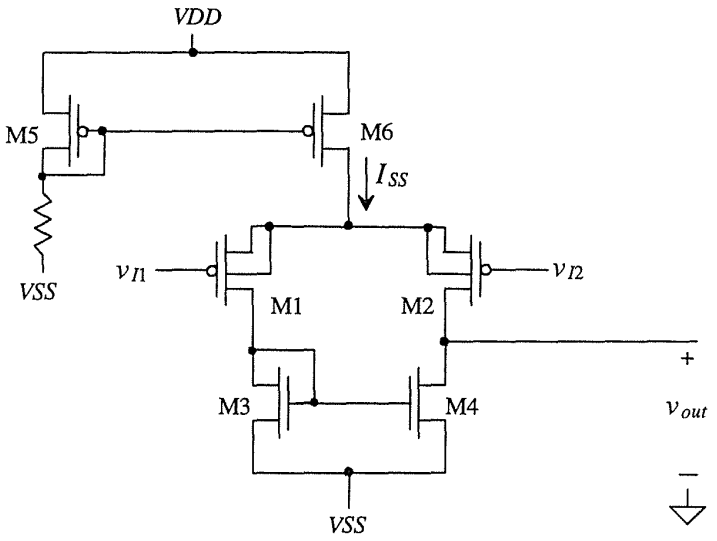


Figure 24.4 P-channel differential amplifier.

Example 24.2

For the differential pair with current source load of Fig. 24.3, plot the transfer characteristics using SPICE when I_{SS} = 20 μA and $W_1 = W_2$ = 15 μm, $W_3 = W_4$ = 70 μm, while the length of the devices is 5 μm. Assume $VDD = -VSS$ = 2.5 V.

In this simulation, we will ground the gate of M2 and perform a DC sweep of v_{I1}. The results are shown in Fig. 24.5. Note that when both inputs are at ground potential the output voltage is 3.8 V. MOSFETs M1 through M4 have 10 μA drain current, and the gate-source voltages are 1.2 V. The slope of this curve around the v_{I1} = 0 is the voltage gain of the amplifier, which we will determine quantitatively later in the section. ■

Up to this point, we have only considered the difference between v_{I1} and v_{I2}, with the common voltage between the two being ground or 0 V. However, another important issue that needs to be discussed is the range of common input voltages the amplifier will continue to operate properly. In other words, if a common signal is input on the gates of M1 and M2, a maximum and minimum voltage exists in which the transistors fail to

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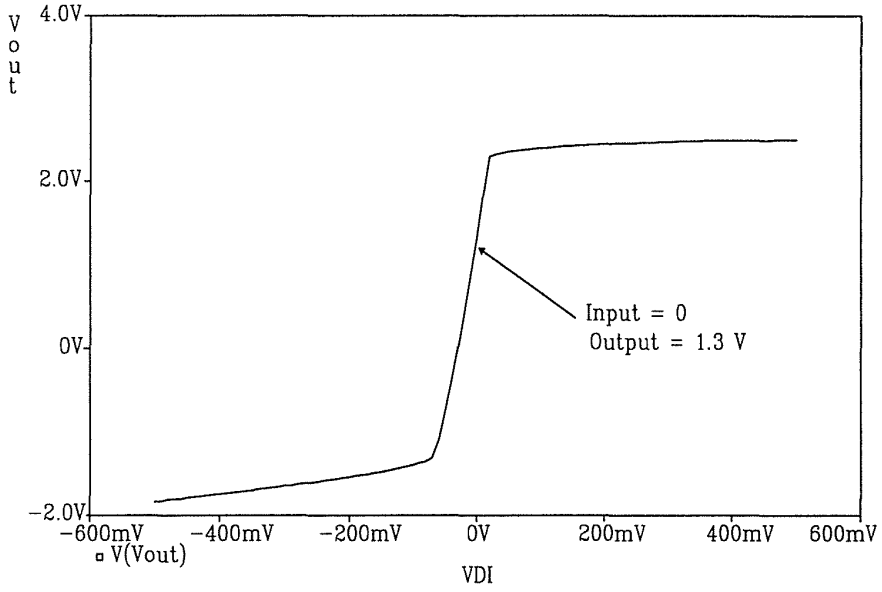


Figure 24.5 DC sweep of the differential amplifier of Ex. 24.2.

stay in the saturation region. This range of common input signals is also known as the *common-mode range* (CMR).

Consider the schematic shown in Fig. 24.6 of a differential amplifier with the gates of M1 and M2 tied together. If v_I starts at zero and is taken toward *VSS*, we will reach a point where M6 will go into the triode region. The v_I at this point is the minimum input voltage allowed on the input of the diff-amp for linear operation. We will label this input potential as

$$v_{IMIN} = \text{minimum allowable input voltage} \tag{24.13}$$

This minimum voltage is given by summing the voltages from the input of the diff-amp to *VSS* when the input is at v_{IMIN} and M6 is on the verge of going into the triode region or

$$v_{IMIN} = \overbrace{\sqrt{\frac{I_{SS}}{\beta_1}} + V_{THN}}^{V_{GS} \text{ of M1 or M2}} + \overbrace{\sqrt{\frac{2I_{SS}}{\beta_6}}}^{V_{DS6} = V_{GS6} - V_{THN}} + VSS \tag{24.14}$$

The maximum allowable input voltage occurs when v_{IMAX} is taken toward *VDD* and M1 and M2 go into the triode region. This occurs when

$$V_{DS1} = V_{GS1} - V_{THN} \rightarrow V_{D1} = V_{G1} - V_{THN} \tag{24.15}$$

Since $V_{G1} = v_{IMAX}$, we get

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$$v_{IMAX} = VDD - \overbrace{\left[\sqrt{\frac{I_{SS}}{\beta_3}} + V_{THP}\right]}^{V_{SG3}} + V_{THN} \tag{24.16}$$

Since V_{THP} is approximately equal to V_{THN}, this reduces to

$$v_{IMAX} \approx VDD - \sqrt{\frac{I_{SS}}{\beta_3}} \tag{24.17}$$

The input common-mode range over which all the MOSFETs in the differential amplifier behave linearly is then,

$$\text{Positive CMR (or limit)} = v_{IMAX} \tag{24.18}$$

and

$$\text{Negative CMR (or limit)} = v_{IMIN} \tag{24.19}$$

We have not included the body effect on the threshold voltages in this derivation. This omission can be justified by considering how we defined a MOSFET in saturation, that is, $V_{DS} \geq V_{GS} - V_{THN}$, back in Ch. 5. We found that the MOSFET entered the saturation region earlier than predicted by this equation because of the uneven charge distribution in the channel. Including the body effect in this derivation would not help us predict the common-mode range with any additional accuracy. Consider the following example.

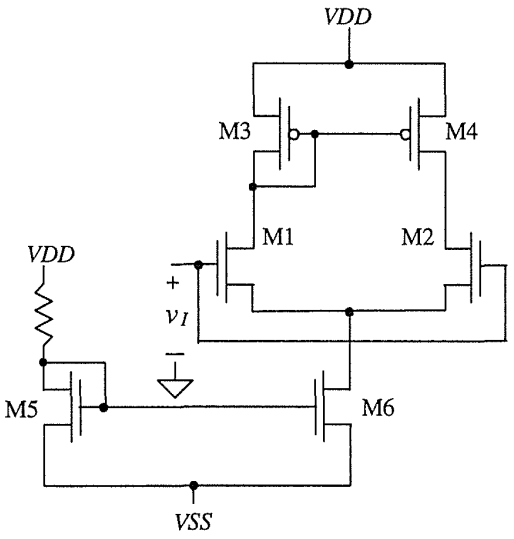


Figure 24.6 Differential amplifier configuration used to determine input common-mode range.

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Example 24.3

Estimate and compare with simulations both the positive and negative CMR for the differential amplifier of Ex. 24.2. Assume the MOSFET M6 used in the current mirror has $W_6 = 30$ μm and $L_6 = 5$ μm for an I_{SS} of 20 μA.

We begin by calculating the positive CMR

$$v_{IMAX} = 2.5 - \sqrt{\frac{20\ \mu A}{17\frac{\mu A}{V^2}\cdot\frac{70}{5}}} = 2.1\ V$$

and the negative CMR is

$$v_{IMIN} = \sqrt{\frac{20\ \mu A}{50\frac{\mu A}{V^2}\cdot\frac{15}{5}}} + 0.83 + \sqrt{\frac{2\cdot 20\mu A}{50\frac{\mu A}{V^2}\cdot\frac{30}{5}}} - 2.5 = -0.94\ V$$

Figure 24.7 shows the current through M1 ($I_{SS}/2$ = 10 μA) and the drain-source voltage of M1 plotted against a voltage applied to the gates of M1 (or M2 since they are tied together). The negative CMR is shown in the figure as the point where the drain current of M1 starts to go to zero. The positive CMR is set by the point where M1 goes into the triode region ($V_{DS1} < V_{GS1} - V_{THN}$). Note that the sum of the currents, $I_{D1} + I_{D2}$, are not constant because of the finite output resistance of M6, that is, the current I_{SS} increases as V_{DS6} increases. These results will be used extensively in the design of op-amp circuits in the next chapter. ■

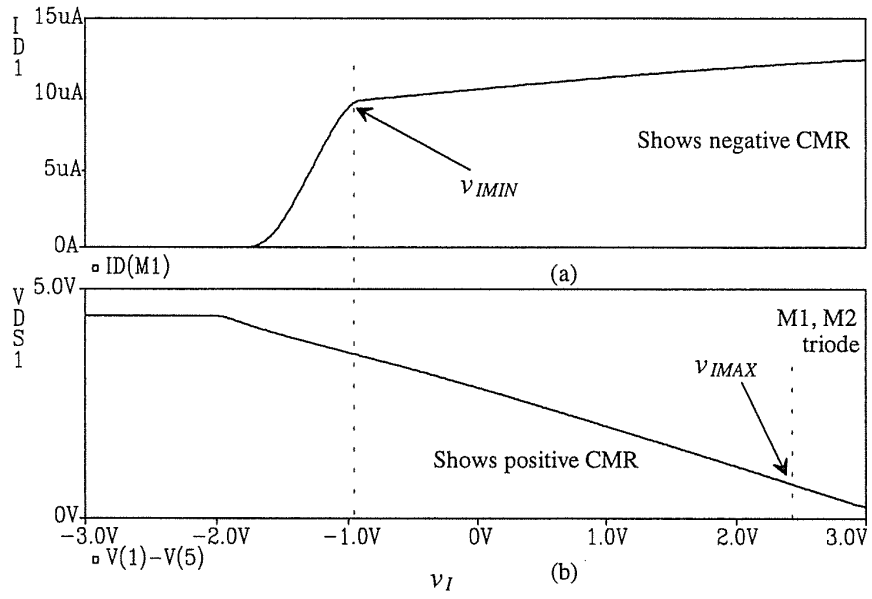


Figure 24.7 (a) Drain current of M1 plotted against input voltage (gates of M1 and M2 tied together) and (b) the drain-source voltage of M1 going into triode.

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Now let's determine the small-signal gain of the differential amplifier of Fig. 24.3. Let's begin by assuming that the gate of M2 is at AC ground. The input voltage is given by

$$v_{i1} = v_{gs1} - v_{gs2} = i_{d1} \cdot \frac{1}{g_{m1}} - i_{d2} \cdot \frac{1}{g_{m2}} \tag{24.20}$$

Ideally, zero AC current flows into the drain of M6 so that

$$i_{d1} = -i_{d2} = i_d \text{ and } g_{m1} = g_{m2} = g_m \tag{24.21}$$

and

$$v_{i1} = i_d\left(\frac{2}{g_m}\right) \tag{24.22}$$

The idea that the drain current of M2 flows out of M2's drain rather than into the drain is simply understood by thinking about how the overall AC + DC current changes. Increasing v_{I1} causes i_{D1} to increase and i_{D2} to decrease. A decrease in the overall drain current of M2 is taken to mean that the AC current is flowing out of the drain. This is explained better with the use of Fig. 24.8. The current entering the output node is composed of a current from the current mirror and a current from M2. The MOSFET's M3 drain current is mirrored by M4, and the increase in drain current through M1 is equal to the decrease in drain current through M2. The total current, $2i_d$ is driven into the resistance at the output node. The resistance looking into the drain of M4 is given by

$$r_{o4} = \frac{1}{\lambda I_D} \tag{24.23}$$

while the resistance looking into the drain of M2 is

$$R_{intoD2} = r_{o2}\left(1 + g_{m2} \cdot \frac{1}{g_{m1}}\right) \approx r_{o2} \tag{24.24}$$

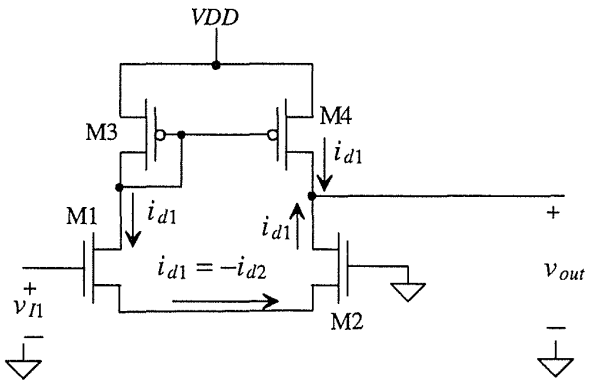


Figure 24.8 Differential amplifier with AC currents shown.

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The voltage gain of the differential amplifier is given by

$$A_v = \frac{v_{out}}{v_{i1}} = \frac{v_{out}}{v_{i1} - v_{i2}} = \frac{2i_d(r_{02} || r_{o4})}{i_d \cdot \frac{2}{g_m}} = g_m(r_{o2} || r_{o4}) \qquad (24.25)$$

This gain can also be written

$$A_v = \frac{2\sqrt{\beta}}{(\lambda_2 + \lambda_4)\sqrt{I_{SS}}} \qquad (24.26)$$

In other words, lowering the diff-pair bias current increases the gain at the price of bandwidth and slew rate.

Consider the differential amplifier driving a load capacitance C_L shown in Fig. 24.9. If an input step is applied to the diff-amp that goes from 0 to *VSS*, then M1, M3, and M4 shut off. MOSFET M2 goes into the triode region, and the current I_{SS} is applied directly to the load capacitance. Under these conditions, the capacitor is discharged at its maximum rate, called the slew rate. This rate of discharge is given, assuming that the load capacitance is large compared to the output capacitance of the differential amplifier, by

$$\frac{dV}{dt} = \frac{I_{SS}}{C_L} \text{ (V/μs)} \qquad (24.27)$$

It can be seen that if we applied a positive step pulse M2 would turn off and the current through M1, M3, and M4 would be I_{SS}. Therefore, the maximum rate at which the load capacitance can be charged is given by this equation as well. When the capacitor is fully charged, M4 cuts off and the current in M1 and M3 remains I_{SS}. In the derivation of the slew-rate, we have neglected the MOSFET capacitances present in the output

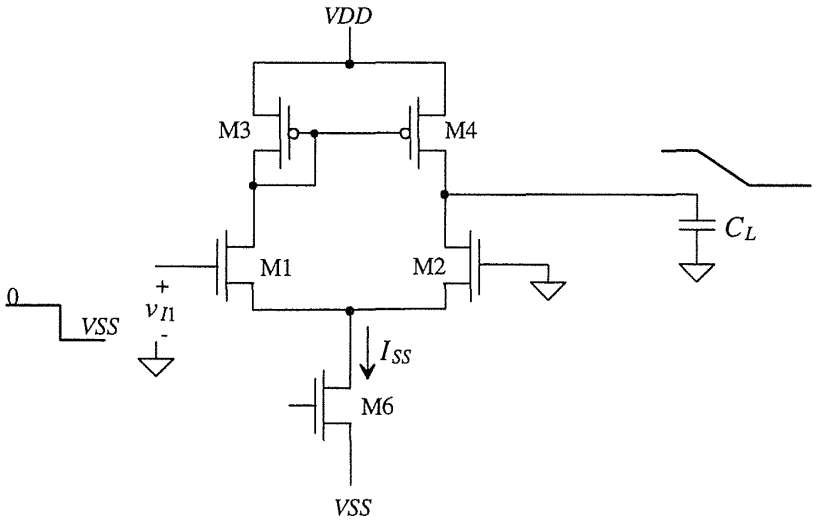


Figure 24.9 Slew-rate limitations of the differential amplifier.

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node. In the derivation of the amplifier's small-signal frequency response, we will not neglect these capacitances.

Consider the schematic of the output node shown in Fig. 24.10. We know from the derivation of the small-signal gain that the effective resistance to ground at this node is approximately $r_{o2}||r_{o4}$. The total capacitance at the output node to ground is given by

$$C_{tot} = C_L + C_{db4} + C_{gd4} + C_{db2} + C_{gd2} \tag{24.28}$$

The time constant at the output node is given by

$$\tau_{out} = (r_{o2}||r_{04}) \cdot C_{tot} \tag{24.29}$$

The upper 3 dB frequency is given by

$$f_{out} = \frac{1}{2\pi\tau_{out}} \tag{24.30}$$

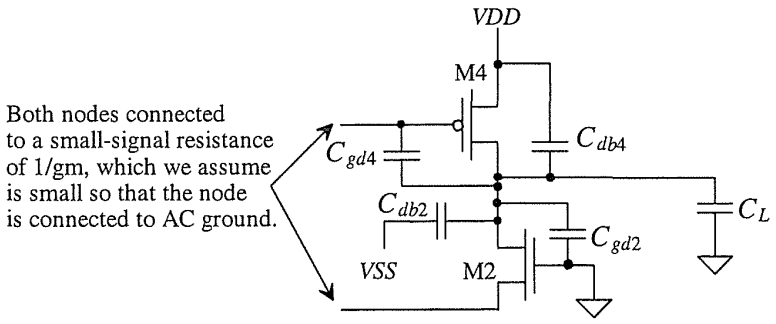


Figure 24.10 Capacitances at the output node used to calculate the frequency response of the differential amplifier.

Example 24.4

For the differential amplifier shown in Fig. 24.11, calculate the slew rate and the small-signal upper 3 dB frequency. Compare your hand calculations with SPICE. Assume that the length of the drain implant regions is 6 μm and that the width of the implant is equal to the width of the MOSFET.

We begin this problem by calculating the MOSFET capacitances. We will approximate the drain depletion capacitances using the bottom zero bias capacitance, or

$$C_{db2} = cj \cdot 6\ \mu\text{m} \cdot W_2 = 1.04 \times 10^{-4} \cdot 6\mu \cdot 15\mu = 9.4\ \text{fF}$$

and

$$C_{db4} = cj \cdot 6\mu \cdot 70\mu = 137\ \text{fF}$$

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The drain-gate capacitances of the MOSFETs are given by

$$C_{gd2} = CGDO \cdot W_2 = 3.8 \times 10^{-10} \cdot 15\ \mu\text{m} = 5.7\ \text{fF}$$

and

$$C_{gd4} = CGDO \cdot W_4 = 5 \times 10^{-10} \cdot 70\ \mu\text{m} = 35\ \text{fF}$$

The total capacitance is given by

$$C_{tot} = 2\ \text{pF} + 137\ \text{fF} + 35\ \text{fF} + 9.4\ \text{fF} + 5.7\ \text{fF} = 2.19\ \text{pF}$$

The slew rate is given by

$$SR = \frac{dV}{dt} = \frac{20\ \mu\text{A}}{2.19\ \text{pF}} = 9.1 \frac{\text{V}}{\mu\text{s}}$$

The output time constant is given by

$$\tau = (r_{02} || r_{o4}) \cdot C_{tot} = \frac{1}{2\lambda \frac{I_{SS}}{2}} \cdot C_{tot} = \frac{1}{0.06 \cdot 20\ \mu\text{A}} \cdot 2.19\ \text{pF} = 1.8\ \mu\text{s}$$

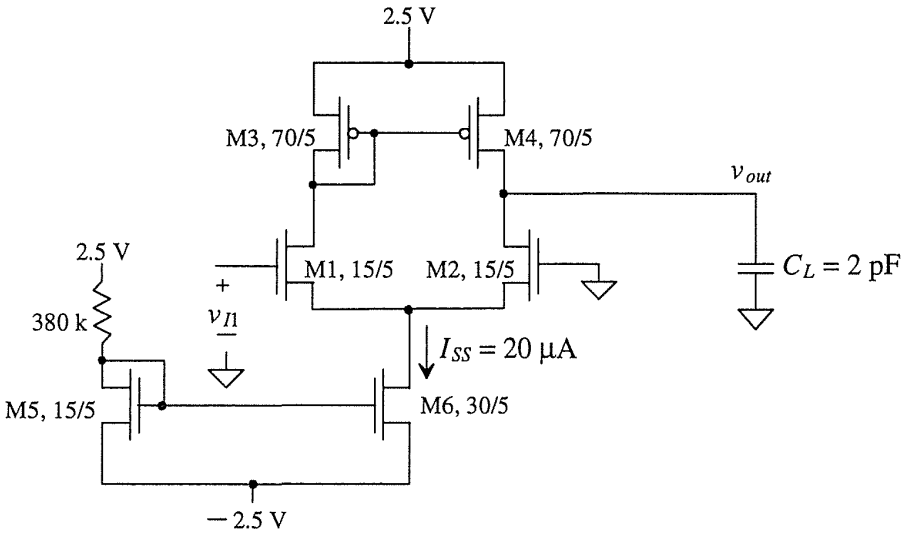


Figure 24.11 Differential amplifier used in Ex. 24.4.

The upper 3 dB frequency is, from Eq. (24.30), 87 kHz. SPICE simulation results are shown in Fig. 24.12. The SR is determined by pulsing the gate of M1 from 0 to – 2.5 V, while the gate of M2 is held at ground potential. The hand calculations were very close to the simulation results. ■

This example presents an important, but not obvious, problem encountered in SPICE simulation. Consider what would happen if, during the SPICE simulation of the slew rate, we pulsed the gate of M1 negative at the beginning or close to the beginning

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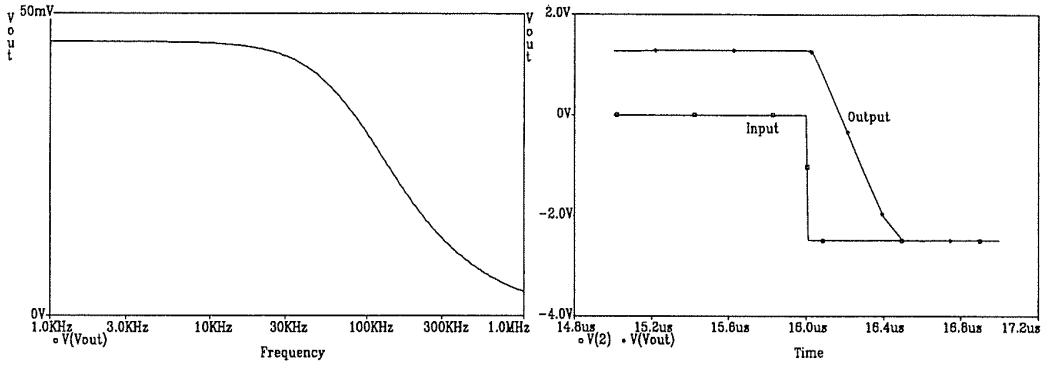


Figure 24.12 SPICE simulation results for Ex. 24.4.

of the simulation. Steady-state conditions would not have been reached in the circuit, and the simulation would likely not converge. However, if we apply the input signal after the circuit has reached steady-state conditions, say approximately 15 μs for the present simulation, the simulation converges (and the frustration level is low). This results in a general rule for simulating analog circuits in SPICE, that is:

When performing a transient simulation allow a considerable amount of time for the circuit to reach steady-state conditions before applying the inputs.

24.1.2 Common-Mode Rejection Ratio

An important aspect of the differential amplifier is its ability to reject a common signal applied to both inputs. Often, in analog systems, signals are transmitted differentially, and the ability of an amplifier to reject coupled noise into each line is very desirable. Consider the amplifier shown in Fig. 24.13. Since the input is no longer a differential signal, the common source node can no longer be considered an AC ground. The current source at the source of M1 and M2 has been replaced with its small-signal output resistance. If we apply an AC signal to the gates of M1/M2, equivalent to saying that a common signal is applied to the input of the differential amplifier, we can calculate the common-mode gain. We begin by writing the AC small-signal common-mode input voltage, v_c, as

$$v_c = v_{gs1,2} + 2i_d r_{o6} \tag{24.31}$$

The MOSFETs M1 and M2 each source a current, i_d, through the output resistance of the current source, r_{o6}. This equation may be rewritten as

$$v_c = i_d\left(\frac{1}{g_m} + 2r_{o6}\right) \approx i_d \cdot 2r_{o6} \tag{24.32}$$

The output voltage, because of the symmetry of the circuit, is given by

$$v_{out} = -i_d \cdot \frac{1}{g_{m3}} = -i_d \cdot \frac{1}{g_{m4}} \tag{24.33}$$

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The common-mode gain is

$$A_c = \frac{v_{out}}{v_c} = -\frac{1/g_{m4}}{2r_{o6}} = -\frac{1}{2g_{m4}r_{o6}} \tag{24.34}$$

assuming $g_{m3} = g_{m4}$. The common-mode gain can be decreased (ideally it is zero) by increasing the output resistance of the current source connected to the source coupled pair. The difference-mode gain was given by Eq. (24.25) as $|A_v| = g_{m1}(r_{o2}||r_{o4})$. The common-mode rejection ratio (CMRR), in dB, of the differential amplifier with current source load is given by

$$\text{CMRR} = 20\log\left|\frac{A_v}{A_c}\right| = 20\log\left|g_{m1}(r_{o2}||r_{o4})\cdot 2g_{m4}r_{o6}\right| \tag{24.35}$$

or in generic terms where the output resistance of the current source is R_{out},

$$\text{CMRR} = 20\log\left|2g_{m1}g_{m4}(r_{o2}||r_{o4})R_{out}\right| \tag{24.36}$$

Using a cascode current source can greatly increase the CMRR at the price of increased negative common-mode range (CMR). Also, in this analysis we have only discussed low-frequency CMRR. At high frequencies the capacitance at the sources of M1 and M2 to ground (this capacitance is in parallel with the r_{o6} in Fig. 24.13) dominates the output impedance of the current source. The effect causes the CMRR to decrease with increasing frequency.

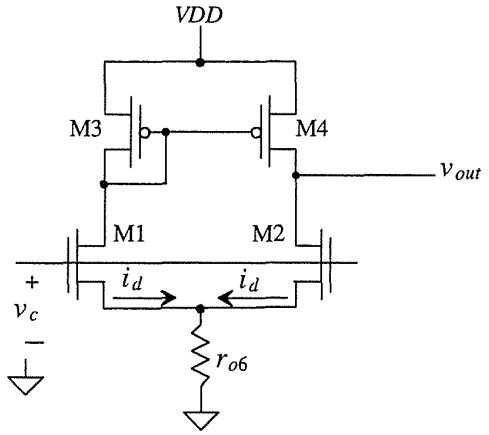


Figure 24.13 Differential amplifier configuration used to determine input CMRR.

24.1.3 Noise

Consider the diff-amp shown in Fig. 24.14, with the noise sources of each MOSFET drawn in the schematic. From Ch. 9 we can write the mean squared noise current generated between each MOSFET's drain and source as

$$\overline{i_n^2} = \overline{i_{therm}^2} + \overline{i_{1/f}^2} = 6kT\sqrt{2\beta I_D} + \frac{KF\cdot I_D^{AF}}{f\cdot C_{ox}'\cdot L^2},\ \left(\frac{\text{A}^2}{\text{Hz}}\right) \tag{24.37}$$

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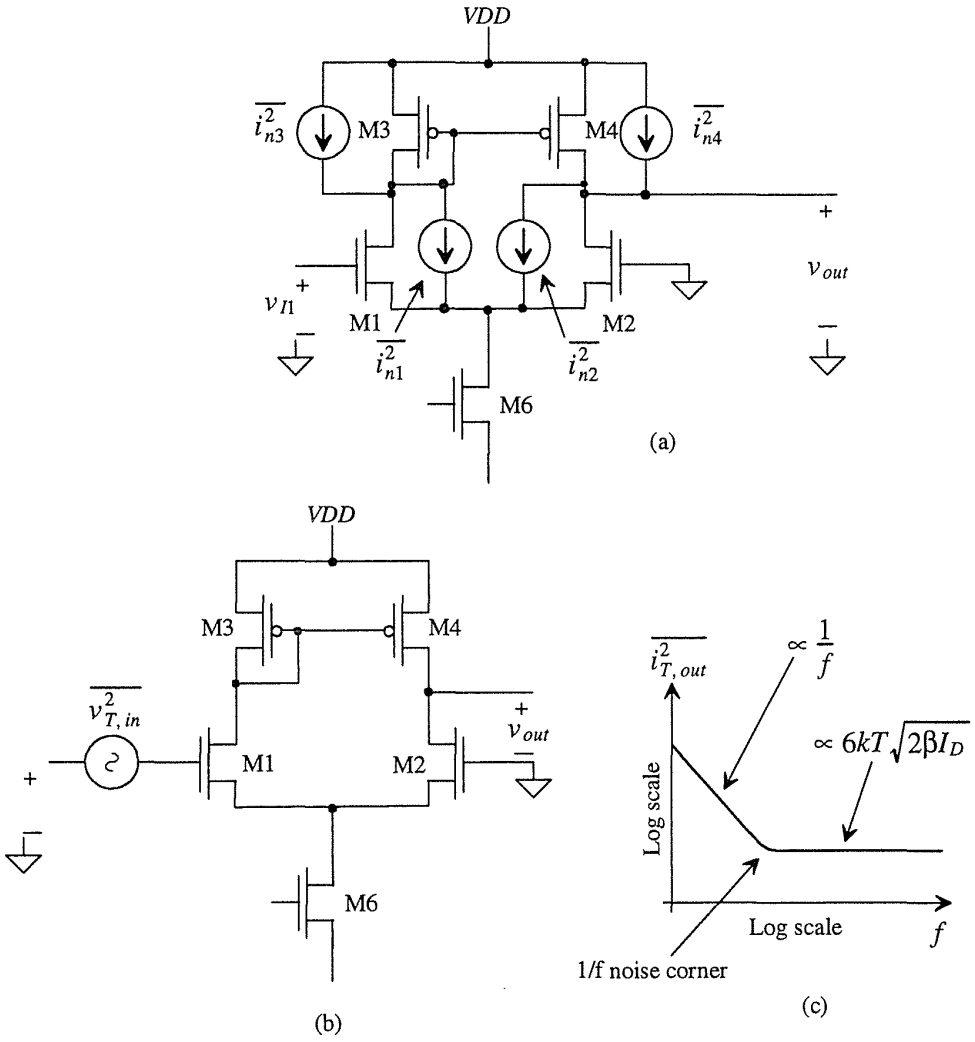


Figure 24.14 (a) Noise sources added into the basic differential amplifier and (b) modeling the amplifier noise on the input and (c) total output noise over a 1-Hz bandwidth.

The noise current generated in M1 (or M3) is mirrored in M4, so that the total mean squared noise current at the output node is

$$\overline{i_{T,out}^2} = \overline{i_{n1}^2} + \overline{i_{n2}^2} + \overline{i_{n3}^2} + \overline{i_{n4}^2} \tag{24.38}$$

This is assuming that M6 doesn't generate any noise current and we are interested in a frequency range where the capacitances in the circuit do not come into play. The total mean squared output noise is

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$$\overline{v_{T,out}^2} = \left(\overline{i_{n1}^2} + \overline{i_{n2}^2} + \overline{i_{n3}^2} + \overline{i_{n4}^2}\right)(r_{o2}||r_{o4})^2, \quad \left(\frac{V^2}{Hz}\right) \tag{24.39}$$

while the total mean squared input-referred noise is

$$\overline{v_{T,in}^2} = \frac{\overline{v_{T,out}^2}}{A_v^2} = \frac{1}{g_{m1}^2}\left(\overline{i_{n1}^2} + \overline{i_{n2}^2} + \overline{i_{n3}^2} + \overline{i_{n4}^2}\right) \tag{24.40}$$

Both the thermal and 1/f input noise contributions can be reduced by reducing the source coupled pair bias current, I_{SS}. Increasing the length of the load MOSFETs M3 and M4, relative to the length of M1 and M2, has the effect of making the input or output 1/f noise contributions determined mainly by M1 and M2.

24.1.4 Matching Considerations

One important aspect of differential amplifiers is the dependence of the performance on the matching of devices. Layout techniques can be used to minimize the first-order effects of mismatch due to oxide gradients and other process variations. Interdigitation was introduced in Ch. 20 when discussing current mirrors. However, a more effective layout technique should be used when matching is critical, as is the case for the

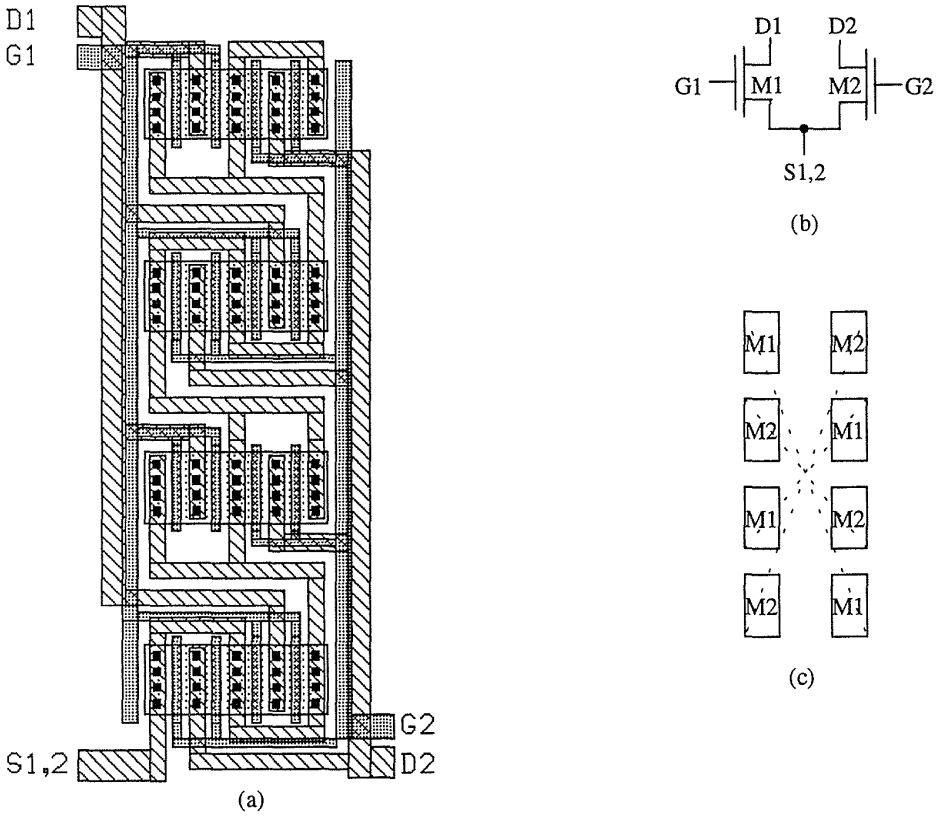


Figure 24.15 (a) Common-centroid layout for the differential pair of (b) with parasitic matching (c) layout of MOSFETs and common center.

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differential amplifier. Common-centroid layout, as the name implies, constructs two devices symmetrically about a common center in the layout. This allows the two devices to cancel process gradients in both the x and y directions and exposes both devices to heat sources in an identical manner.

As seen in Fig. 24.15, the source coupled pair is interdigitated in three separate rows and alternately connected in the vertical direction. The common source node (S1,2) intertwines the entire structure. Note how the layout is completely symmetrical about the centroid (center). Although this layout technique is labor intensive, the benefits would warrant the extra time required to minimize the nonideal effects.

The input offset voltage of a diff-pair, resulting from mismatches in threshold voltage, geometrys and load resistances, can be determined with the help of Fig. 24.16 [2]. The value of the offset-voltage is given by

$$V_{OS} = V_{GS1} - V_{GS2} = V_{THN1} + \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{THN2} - \sqrt{\frac{2I_{D2}}{\beta_2}} \qquad (24.41)$$

We can define the differences and averages of the threshold voltage, load resistance, and geometry as ΔV_{THN} ($V_{THN1} - V_{THN2}$), V_{THN} (average of V_{THN1} and V_{THN2}), ΔR_L ($R_{L1} - R_{L2}$), R_L (average of R_{L1} and R_{L2}), $\Delta(W/L)$ [$(W_1/L_1) - (W_2/L_2)$] and $\Delta(W/L)$ [average of (W_1/L_1) and (W_2/L_2)]. Thus, we can make the appropriate substitutions into Eq. (24.41), requiring $I_{D1}R_{L1} = I_{D2}R_{L2}$, with the result:

$$V_{OS} = \Delta V_{THN} + \frac{V_{GS} - V_{THN}}{2} \cdot \left[\frac{-\Delta R_L}{R_L} - \frac{\Delta(W/L)}{(W/L)} \right] \qquad (24.42)$$

The threshold voltage mismatch must be reduced using layout techniques. Mismatches resulting from unequal geometry and differences in the load resistance can be reduced by designing with a small V_{GS} (V_{GS} close to V_{THN}). This should be compared with Eq. (20.38), which showed that using small V_{GS} in a current mirror resulted in a large mirrored current difference.

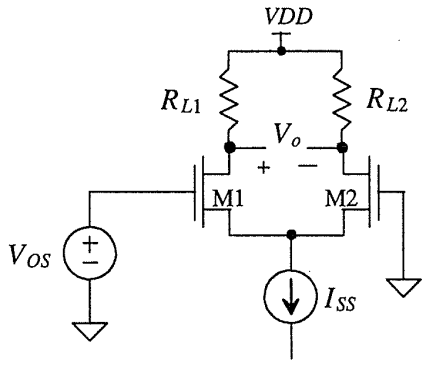


Figure 24.16 Determination of diff-amp input offset voltage.

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24.2 The Source Cross-Coupled Pair

The source cross-coupled pair is shown in Fig. 24.17 [3, 4]. This configuration is very useful in practical circuit design. Assuming that both inputs are connected to ground and that all n-channels and all p-channels are the same size, a current I_{SS} flows in all the MOSFETs in the circuit. Normally, we could design the circuit so that I_{SS} = 10 μA and the gate-source voltage is 1.2 V. This results in our already familiar sizes of 15/5 for the n-channels and 70/5 for the p-channels.

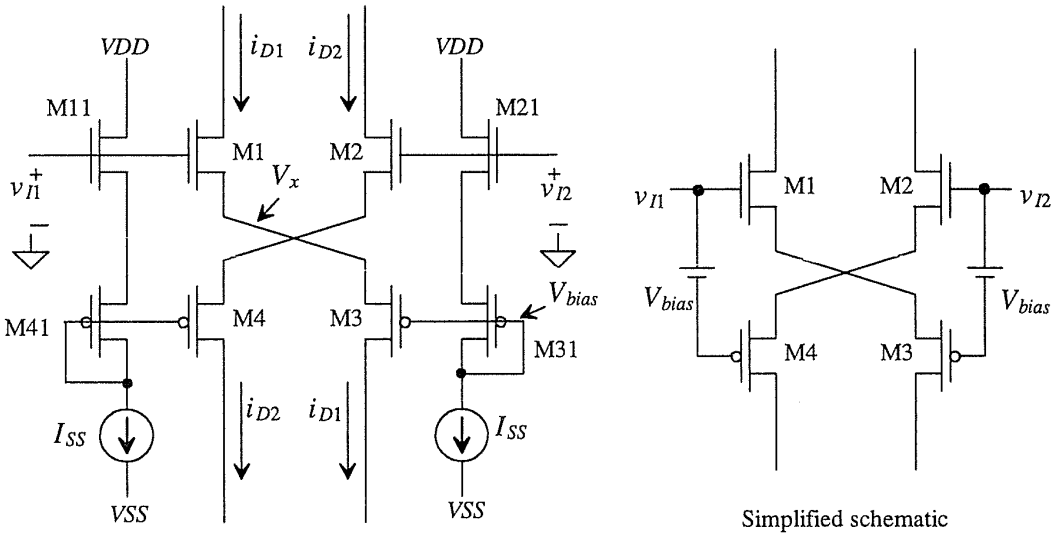


Figure 24.17 Source cross-coupled differential amplifier, n-channel input devices.

With the gate of M2 grounded, the gate of M4 is at a constant potential that we will label V_{bias} (or approximately –2.4 V with the above sizes). We will label the potential at the source of M1 and M4 as V_x. The input voltage can be written, assuming that M1 and M4 remain in the saturation region, as

$$v_{I1} = \sqrt{\frac{2i_{D1}}{\beta_1}} + V_x + V_{THN} \tag{24.43}$$

and for M3

$$i_{D1} = \frac{\beta_3}{2}(V_x + V_{bias} - V_{THP})^2 \tag{24.44}$$

Solving Eq. (24.44) for V_x yields

$$V_x = \sqrt{\frac{2i_{D1}}{\beta_3}} - V_{bias} + V_{THP} \tag{24.45}$$

Substituting this equation into Eq. (24.43) results in

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$$v_{I1} = \sqrt{2i_{D1}}\left[\frac{1}{\sqrt{\beta_1}} + \frac{1}{\sqrt{\beta_3}}\right] - V_{bias} + V_{THP} + V_{THN} \tag{24.46}$$

When $v_{I1} = 0$ the $i_{D1} = I_{SS}$. This equation can be rewritten as

$$i_{D1} = \frac{1}{2} \cdot (v_{I1} + V_{bias} - V_{THP} - V_{THN})^2 \frac{\beta_1\beta_3}{\left(\sqrt{\beta_1} + \sqrt{\beta_3}\right)^2} \tag{24.47}$$

while a similar analysis for i_{D2}, with v_{I1} grounded, yields

$$i_{D2} = \frac{1}{2} \cdot (v_{I2} + V_{bias} - V_{THP} - V_{THN})^2 \frac{\beta_2\beta_4}{\left(\sqrt{\beta_2} + \sqrt{\beta_4}\right)^2} \tag{24.48}$$

Normally, $\beta_1 = \beta_2$ and $\beta_3 = \beta_4$. Note that the diff-amp output currents, i_{D1} and i_{D2}, are available at both the top and bottom of the amplifier.

Earlier in the chapter we defined the difference in the input voltages as

$$v_{DI} = v_{I1} - v_{I2} \tag{24.49}$$

Equations (24.47) and (24.48) can be written in the more general case by substituting v_{DI} for v_{I1} in Eq. (24.47) and $-v_{DI}$ for v_{I2} in Eq. (24.48).

An important characteristic of the source cross-coupled differential amplifier is that as v_{DI} is increased i_{D1} continues to increase and i_{D2} shuts off while the opposite is true for when v_{DI} decreases. In other words, the amplifier is operating class AB where neither of the output currents is zero as long as their magnitudes remain less than I_{SS}. The maximum difference in potential between the two inputs so that neither output current is zero is given by

$$|v_{DMIN}| = -V_{bias} + V_{THP} + V_{THN} \tag{24.50}$$

Example 24.5

Referring to the diff-amp of Fig. 24.17, if $I_{SS} = 10$ μA and all NMOS have a 15/5 size while all PMOS have a 70/5 size, estimate and compare to simulations v_{DMIN}.

We know that with these sizes and biasing current, the gate-source potential of all MOSFETs is approximately 1.2 V. Knowing this, we get

$$|v_{DMIN}| = -2.4 + 0.91 + 0.83 = -660 \text{ mV}$$

The simulation results are shown in Fig. 24.18 where $v_{I2} = 0$. This figure should be compared with Fig. 24.2 where the drain current flattens out at I_{SS}. It should be obvious from Fig. 24.18 that source cross-coupled diff-amp does not exhibit slew-rate limitations. The lack of slew-rate limitations results from the absence of a current source in series with M1 or M2. ■

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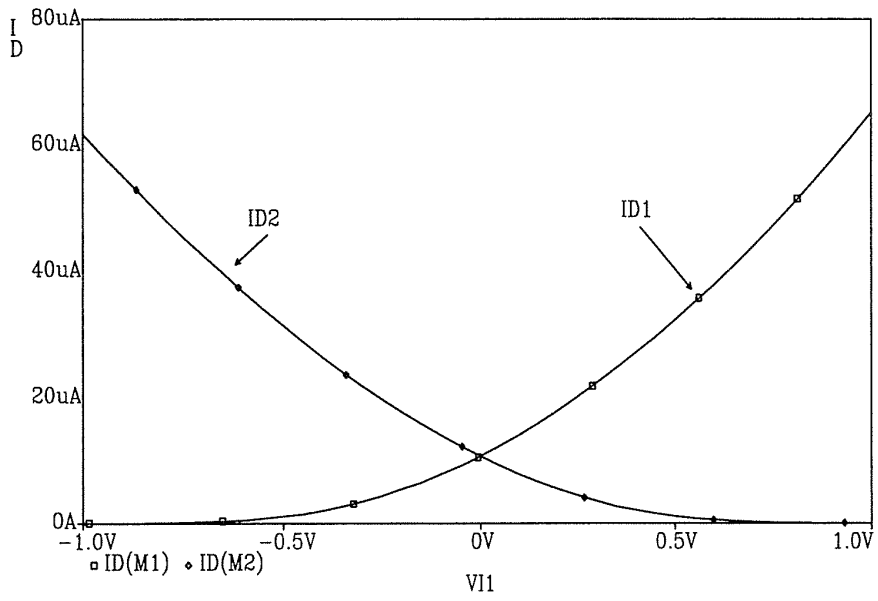


Figure 24.18 Transfer characteristics of the diff-amp of Ex. 24.5.

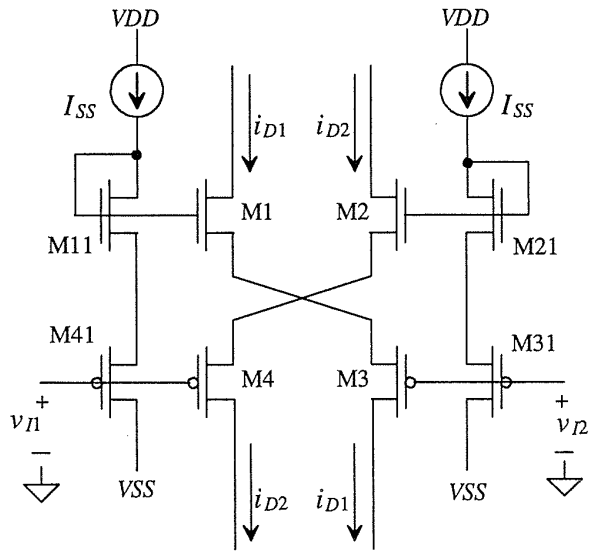


Figure 24.19 Source cross-coupled differential amplifier, p-channel input devices.

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The p-channel version of the source cross-coupled differential amplifier is shown in Fig. 24.19. Normally, the type, p-channel or n-channel, version of this differential amplifier used is dependent on the common-mode range (CMR). The n-channel version has the best positive CMR, while the p-channel version has the best negative CMR. Calculation of the CMR is presented in the next section.

24.2.1 Current Source Load

The source cross-coupled differential amplifier with active loads is shown in Fig. 24.20. Note that we could have easily added a pair of active loads in series with the drain of M1 and M4 to obtain a differential output amplifier. The small-signal gain of this amplifier can be analyzed intuitively. Superposition will be used to find the gain from the output back to each input. First, determine the small-signal gain, $\frac{v_o}{v_{I1}}$, with v_{I2} grounded. Neglecting the bulk effect, we can see that the voltage gain from the gate of M1 to the source of M1 is simply a common drain amplifier of the form

$$\frac{v_{s1}}{v_{I1}} = \frac{g_{m1}R_{Leq}}{1+g_{m1}R_{Leq}} \text{ V/V} \tag{24.51}$$

where R_{Leq} is simply the load seen by the source of M1. This can be found by using a test source (as seen in Fig. 24.21) to determine the effective impedance seen looking into the source of M3. This results in

$$R_{Leq} = \frac{v_t}{i_t} = \frac{1+\frac{1}{g_{m3}r_{o3}}}{g_{m3}+\frac{1}{r_{o3}}} \approx \frac{1}{g_{m3}} \tag{24.52}$$

Therefore, the voltage gain from v_{I1} to the source of M1 becomes

$$\frac{v_{s1}}{v_{I1}} = \frac{g_{m1}\frac{1}{g_{m3}}}{1+g_{m1}\frac{1}{g_{m3}}} \tag{24.53}$$

The voltage gain from v_{s1} to v_{g9} is the same form as a common gate amplifier. This gain is

$$\frac{v_{g9}}{v_{s1}} = g_{m3}\frac{1}{g_{m5}} \tag{24.54}$$

And finally, the gain from the gate of M9 to the output is simply $-g_{m9}r_{o8}||r_{o9}$, and

$$\frac{v_o}{v_{I1}} = -\frac{g_{m1}\frac{1}{g_{m5}}}{1+g_{m1}\frac{1}{gm3}}g_{m9}(r_{o9}||r_{o8}) \tag{24.55}$$

Using the same type of analysis, we find that the expression from v_{I2} to the output is

$$\frac{v_o}{v_{I2}} = \frac{g_{m2}\frac{1}{g_{m6}}}{1+g_{m2}\frac{1}{gm4}}g_{m8}(r_{o8}||r_{o9}) = \text{[common source w/source resistance][common source]} \tag{24.56}$$

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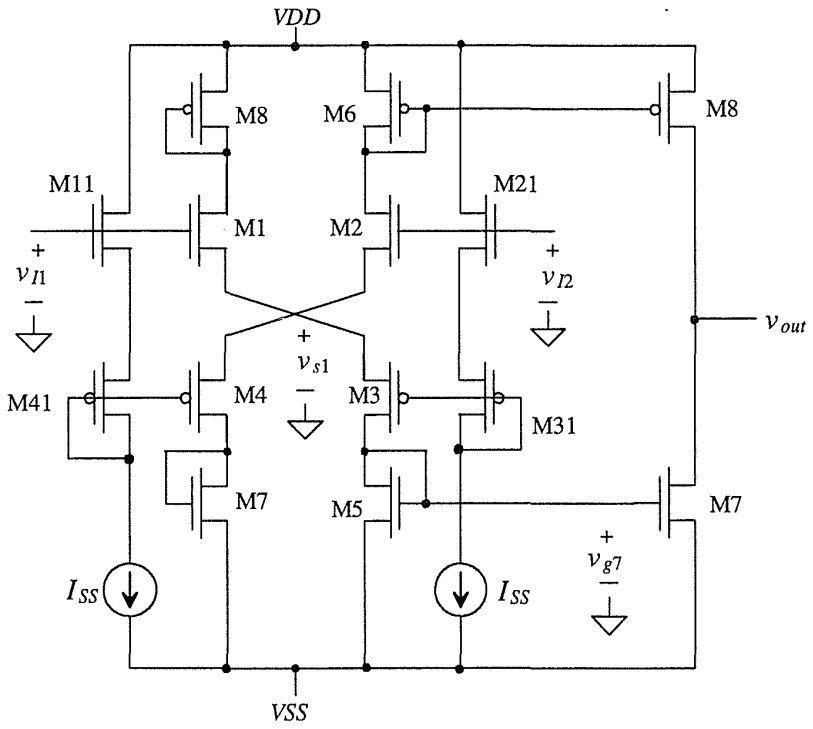


Figure 24.20 Source cross-coupled differential amplifier, with current source loads.

Superposition can now be used to determine the total effect of each input on the output. Therefore, if M1 and M2 are matched, as are M3 and M4, and if M5 and M6 are designed so that their g_m's are equal as are M7 and M8, then the differential gain can be expressed as

$$v_o = (v_{I2} - v_{I1}) \frac{g_{m1,2}\frac{1}{g_{m5,6}}}{1 + g_{m1,2}\frac{1}{gm3,4}} g_{m8,9}(r_{o8} || r_{o9}) \Rightarrow \frac{v_o}{v_d} = \frac{g_{m1,2}\frac{1}{g_{m5,6}}}{1 + g_{m1,2}\frac{1}{gm3,4}} g_{m8,9}(r_{o8} || r_{o9}) \tag{24.57}$$

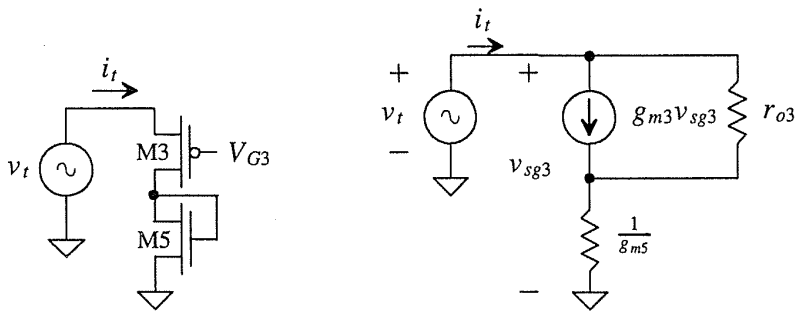


Figure 24.21 (a) Simplified schematic and (b) small-signal model..

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The positive common-mode voltage range is determined in exactly the same manner as with the source coupled diff-amp. The positive CMR is given by

$$v_{IMAX} \approx VDD - \sqrt{\frac{2I_{SS}}{\beta_6}} \tag{24.58}$$

while the negative CMR is given by

$$v_{IMIN} = \overbrace{\sqrt{\frac{2I_{SS}}{\beta_1}} + V_{THN}}^{V_{GS1}} + \overbrace{\sqrt{\frac{2I_{SS}}{\beta_3}}}^{V_{DS3}} + \overbrace{\sqrt{\frac{2I_{SS}}{\beta_5}} + V_{THN}}^{V_{GS3}} + VSS \tag{24.59}$$

The positive CMR is similar to the basic source coupled differential amplifier. However, the negative CMR is considerably worse. Figure 24.22 shows a biasing scheme that is useful for significantly decreasing the negative CMR of the amplifier at the price of a small decrease in the positive CMR. Capacitors between the gates of M1-M4, Fig. 24.20, eliminate the slew-rate limitations caused by the biasing current sources charging the input capacitances.

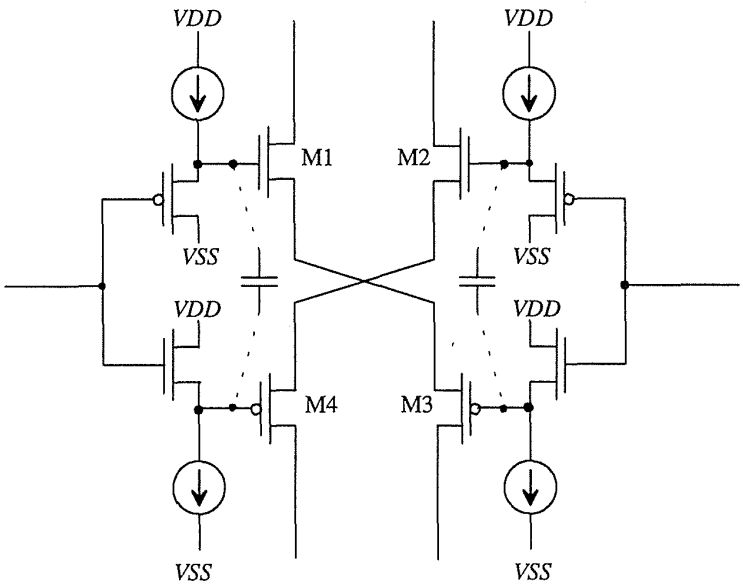


Figure 24.22 Biasing scheme used to increase common-mode range.

An alternative current source load configuration is shown in Fig. 24.23. For class AB operation of this differential amplifier, we cannot place both a current mirror in series with the drains of M1/M2 and a current mirror in series with the drains of M4/M3. The gain of this configuration is given by

$$A_v = \frac{v_{out}}{v_{i1} - v_{i2}} = \frac{r_{o2} \| r_{o6}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}}} \tag{24.60}$$

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assuming $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$.

This differential amplifier is useful as a direct replacement of the source coupled pair, especially when slew-rate limitations are a concern. The bandwidth and CMRR are approximately the same as the source coupled diff-amp, while the circuit complexity and power dissipation are higher.

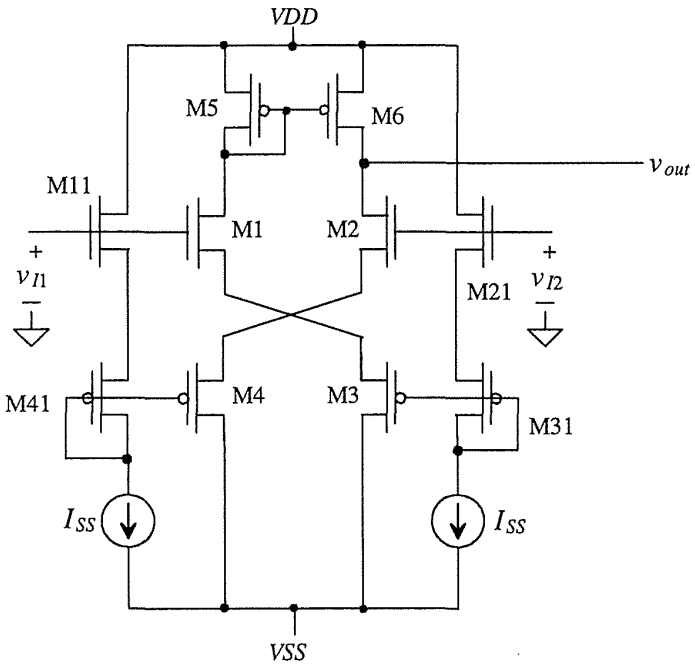


Figure 24.23 Alternative current source load configuration.

24.3 Cascode Loads

The differential amplifier with current source load of Fig. 24.3 gave a voltage gain of $g_m(r_{o2}||r_{o4})$. For many applications this gain may be too low. Using a cascode current source load in place of M3/M4 results in a gain of approximately $g_m r_{o2}$ (review Sec. 22.2.1). This modest improvement in gain can be increased by cascoding M1 and M2 as well. Figure 24.24 shows the resulting circuit configuration. The MOSFET MC6 is selected so that its V_{GS} keeps M1/M2 and MC1/MC2 in the saturation region. The gain of this configuration is given by

$$A_v = g_{m1}(R_{into\ DC2}||R_{into\ DC4}) \tag{24.61}$$

The resistance looking into the drain of MC2, assuming M2 and MC2 are the same size, is given by

$$R_{into\ DC2} \approx g_{m2} \cdot r_{o2}^2 \tag{24.62}$$

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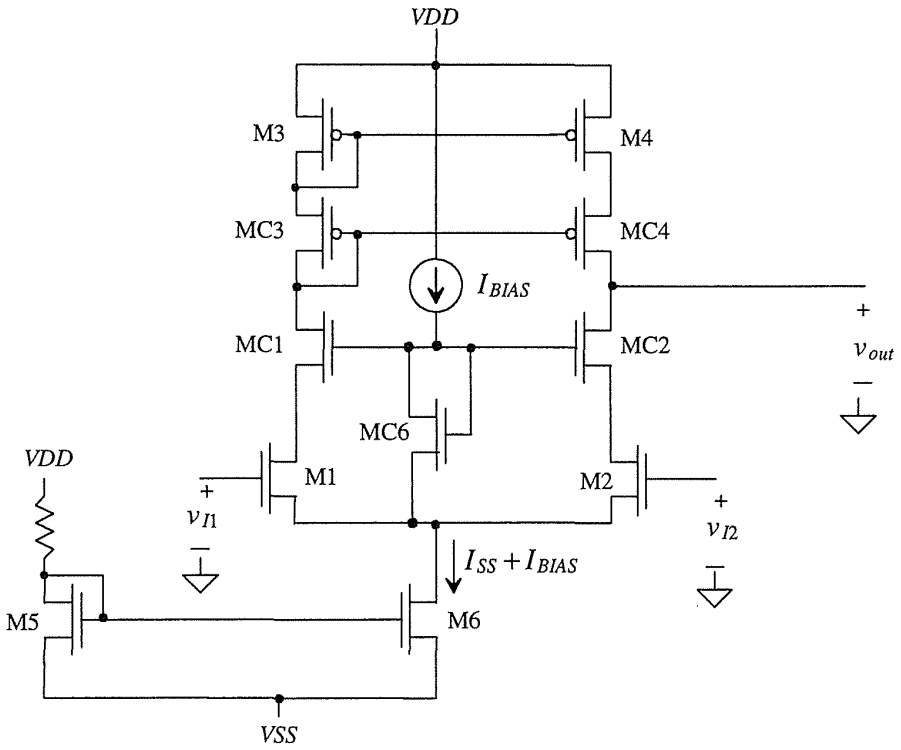


Figure 24.24 Cascode differential amplifier.

and the resistance looking into the drain of MC4, again assuming MC4 and M4 are the same size, is given by

$$R_{into\,DC4} \approx g_{m4} \cdot r_{o4}^2 \tag{24.63}$$

The gain of the cascode differential amplifier may be written as

$$A_v = g_{m1}\left(g_{m2}r_{o2}^2 \| g_{m4}r_{o4}^2\right) \tag{24.64}$$

The main drawback of using the cascode differential amplifier is the major reduction in positive common-mode range. In the negative direction, v_{IMIN} is identical to the source coupled diff-amp discussed in Sec. 24.1. The minimum common-mode voltage is limited by M6 becoming nonsaturated. Hence,

$$v_{IMIN} = \sqrt{\frac{2(I_{SS}+I_{BIAS})}{\beta_6}} + \sqrt{\frac{I_{SS}}{\beta_{1,2}}} + V_{THN1,2} + V_{SS} \tag{24.65}$$

The positive common-mode signal is limited by the additional circuitry required by the cascode loads. Notice that v_{IMAX} in this case will be limited by the amount of voltage necessary to keep M1, MC1, MC3, and M3 in their respective saturation regions. However, an interesting fact concerning this circuit is the DC feedback caused by MC6. Since the current through MC6 is constant, v_{SGC6} will be constant. Therefore,

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as the common-mode voltage on the gates of M1 and M2 begins to increase, the drains of M1 and M2 will normally decrease. However, since the current through M1 and M2 is also constant, the common source node, marked as node B, also begins to increase. Thus, node B (the gates of MC1 and MC2) also increases. The currents through MC1 and MC2 are also constant; thus, the value of $v_{GSC1,2}$ will attempt to stay constant, pulling the drains of M1 and M2 up. This feedback action attempts to keep M1 and M2 from going into nonsaturation. Therefore, the maximum common-mode voltage, v_{IMAX}, will be limited by MC1 and MC2 going into nonsaturation. This occurs when

$$v_{DSC1} = v_{GSC1} - v_{THC1} \tag{24.66}$$

where the voltage on drain of MC1 (and MC2) is

$$v_{DC1} = v_{DD} - v_{SG3} - v_{SGC3} \tag{24.67}$$

and the voltage on the gate of MC1 (MC2) is

$$v_{GC1} = v_{INMAX} - v_{GS1} + v_{GSC6} \tag{24.68}$$

Plugging into Eq. (24.66) and substituting for the values of V_{SG},

$$v_{INMAX} = V_{DD} - \sqrt{\frac{I_{SS}}{\beta_1}} - \sqrt{\frac{I_{SS}}{\beta_{C3}}} - \sqrt{\frac{I_{SS}}{\beta_3}} + \sqrt{\frac{2I_{BIAS}}{\beta_{C6}}} - 2V_{THP} + V_{THN} \tag{24.69}$$

This assumes that the threshold voltages for all the n- and p-type devices are approximately the same. Example 24.6 will illustrate the degraded CMR for the cascode loaded diff-amp.

Example 24.6

Determine the size of M6, MC6, and MB1-MB3 in Fig. 24.25 so that M1 and M2 remain in saturation. Assume I_{SS} is 20 μA, and estimate the gain of the configuration and the common-mode range.

The gate-source voltage of M1/M2 or MC1/MC2 is determined by solving

$$\frac{I_{SS}}{2} = \frac{\beta_{C1}}{2}(V_{GS} - V_{THN})^2 \rightarrow V_{GS} = 1.2 \text{ V}$$

Therefore, the minimum voltage from the gate of MC1 to the source of M1 (in other words V_{GSC6}) is the sum of V_{GSC6} + $V_{DS,sat}$, or approximately 1.5 V. If we design for I_{BIAS} = 10 μA, we can solve for the size of MC6 with

$$10\ \mu A = \frac{50\frac{\mu A}{V^2}}{2}\frac{W_{C6}}{5\ \mu m}(1.5 - 0.83)^2 \rightarrow W_{C6} \approx 5\ \mu m$$

Since a current of 10 μA flows in M5, we set MB3 to the same size, that is, 15/5, so that its drain current is 10 μA as well. MOSFETs MB2 and MB1 form a current mirror. The drain current of MB3 is mirrored in MB1. We can set the sizes of MB2 and MB3 to 70/5. The only remaining MOSFET needing size specifications is M6. The total current that flows in M6 is I_{SS} + I_{BIAS} = 30 μA, so

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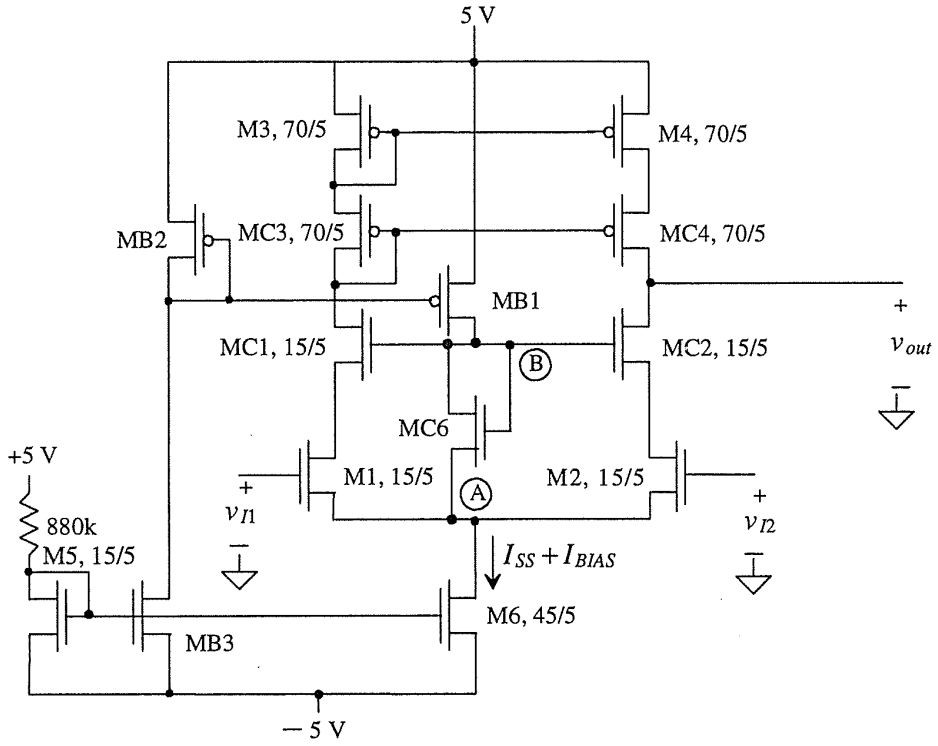


Figure 24.25 Cascode differential amplifier used in Ex. 24.6.

its size is set to 45/5. The gain of the cascode differential amplifier is given, with the help of Eq. (24.64), by

$$A_v = 55\frac{\mu A}{V^2}\left[55\frac{\mu A}{V^2}(833k)^2 \| 70\frac{\mu A}{V^2}(833k)^2\right] = 1,175 \text{ V/V}$$

A noncascode configuration has a gain in the neighborhood of 50 V/V.

The common-mode range will be calculated from Eq. (24.65) and Eq. (24.69). Here the value of v_{IMIN} becomes

$$v_{IMIN} = .365 + .365 + .83 - 5 = -3.44 \text{ V}$$

and the value for v_{IMAX} becomes

$$v_{IMAX} = 5 - .365 - .289 - .289 + .632 - 2(.91) + .83 = 3.77 \text{ V} \quad \blacksquare$$

24.4 Wide-Swing Differential Amplifiers

An increasingly important concern with the advent of low-voltage design is the need for improved common-mode range. A technique used to extend the allowable input swing of a diff-amp is to use two complementary diff-amp stages in parallel [5, 6] as shown in

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Fig. 24.26. To understand the operation of this circuit, consider the case when the DC component of the input signal, v_{in}, is such that both diff-amps are on (and the AC component is small compared to the DC). The current through the diff-pairs M1/M2 and M9/M10 is I, while the current through the summing MOSFETs M4 and M12 is $2I$. If M5 is the same size as M4 and if M7 is the same size as M12, then a current $2I$ flows in the output transistors. The small-signal voltage gain, assuming $g_{m1} = g_{m2}$ and $g_{m9} = g_{m10}$, is given by

$$A_v = (g_{m1} + g_{m9})[r_{o7}(2I) \| r_{o5}(2I)] = \frac{(g_{m1} + g_{m9})}{\lambda_7 2I + \lambda_5 2I} = \frac{\sqrt{2\beta_1 I} + \sqrt{2\beta_9 I}}{2I(\lambda_7 + \lambda_5)} \qquad (24.70)$$

If the input is such that the p-channel diff-amp is on and the n-channel diff-amp is off, then a current I flows in the summing MOSFETs M4 and M12 and zero current flows in M1, M2, M3, and M6. The current that flows in M5 and M7 is now I. The small-signal voltage gain is

$$A_v = g_{m9}[r_{o7}(I) \| r_{o5}(I)] = \frac{\sqrt{2\beta_9 I}}{I(\lambda_7 + \lambda_5)} \qquad (24.71)$$

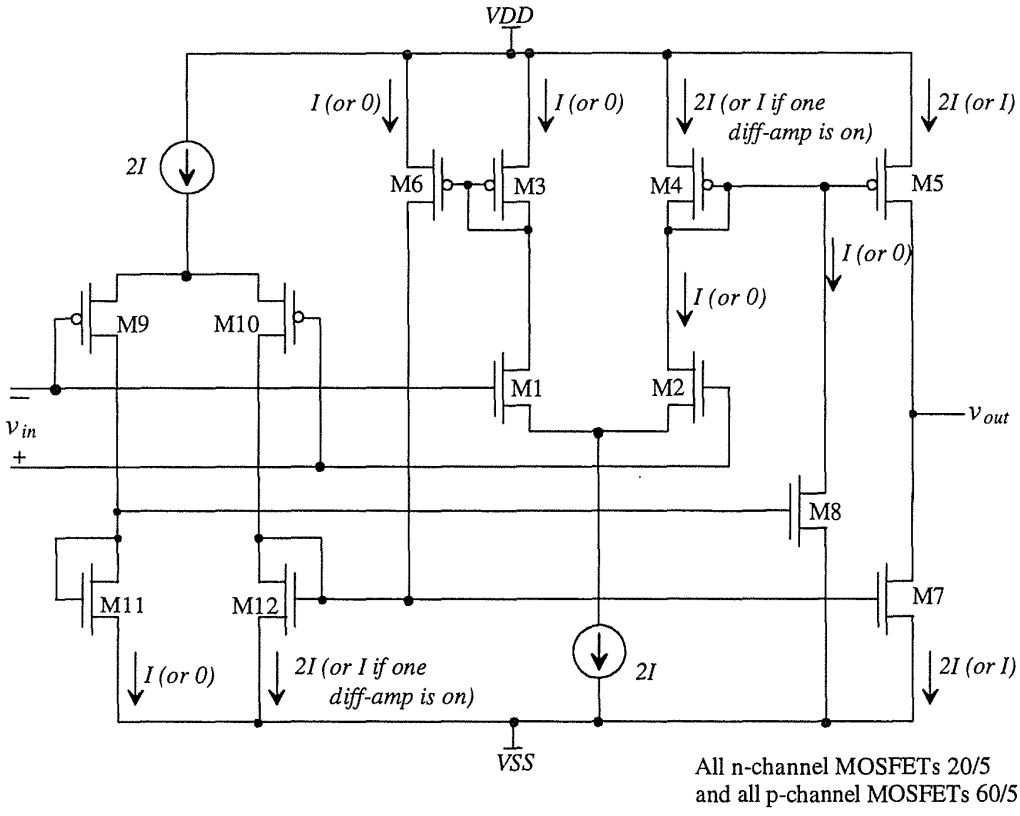


Figure 24.26 Two parallel differential amplifiers used to increase input swing.

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The small-signal gain when the p-channel diff-amp is off and the n-channel diff-amp on is given by

$$A_v = g_{m1}[r_{o7}(I) \| r_{o5}(I)] = \frac{\sqrt{2\beta_1 I}}{I(\lambda_7 + \lambda_5)} \tag{24.72}$$

It is desirable to have a smooth transition from having a single diff-amp on to having both diff-amps on. If we require

$$\beta_1 = \beta_9 = \beta \Rightarrow G_m = \sqrt{2\beta I} \tag{24.73}$$

then Eqs. (24.70) through (24.72) can be rewritten as

$$A_v = G_m \cdot [r_{o7}(I) \| r_{o5}(I)] \tag{24.74}$$

For low distortion a constant gain is important. Also, for a stable amplifier it is important that the amplifier can be compensated (more on this in Ch. 25) to ensure stability. An amplifier with a gain dependent on the input signal amplitude is difficult to compensate.

The amplifier of Fig. 24.26 is called an operational transconductance amplifier (OTA). OTAs are very useful in CMOS analog circuit design. If we set the size of the n-channel MOSFETs in Fig. 24.26 to 20/5 and the p-channel MOSFETs to 60/5 (to satisfy Eq. [24.73] with $KP_n = 50\ \mu A/V^2$ and $KP_p = 17\ \mu A/V^2$) and the current $I = 1\ \mu A$, then the small-signal gain of the circuit, using Eq. (24.72) with $\lambda = 0.06$, is 166 V/V (= A_v). SPICE simulations (using the BSIM model) with $VDD = |VSS| = 2.5$ V resulted in a gain of 240 with common-mode input voltages of 2, 0, and – 2 V. Cascoding M5 and M7 can increase the gain of the OTA.

24.4.1 Current Differential Amplifier

Another wide-swing differential amplifier is the current differencing amplifier. The current diff-amp is shown schematically in Fig. 24.27. In the following discussion, let's assume that M1 through M4 are the same size. If both i_1 and i_2 are zero, then a current I_{SS} flows in all MOSFETs in the circuit. Now assume that i_1 is increased above zero, but less than I_{SS}. This causes the current in both M1 and M2 to increase. As a result, the drain current in M3 decreases in order to keep $i_{D2} + i_{D3} = 2I_{SS}$. The decrease in M3 drain current is mirrored in M4, forcing the current i_1 out of the diff-amp. A similar argument can be made for increasing i_2; that is, it causes the output of the differential amplifier to sink a current equal to i_2. Ratioing the sizes of M1-M4 can be used to give the diff-amp a gain or to scale the input currents.

The input impedance of the current differential amplifier is simply the small-signal resistance of a diode connected MOSFET, or

$$R_{in} = \frac{1}{g_m} \tag{24.75}$$

This configuration finds applications in both low-power and high-speed circuit design.

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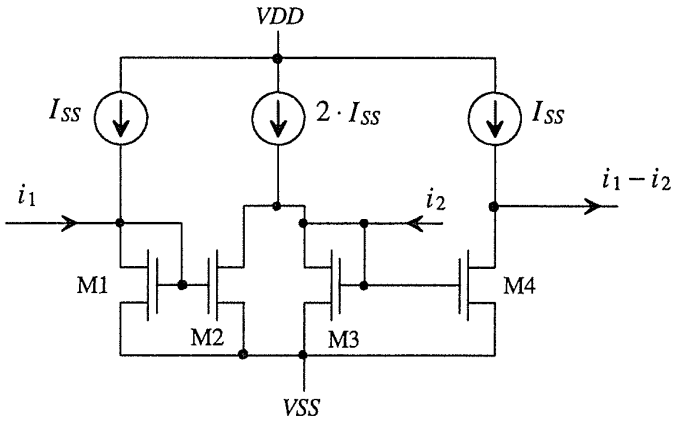


Figure 24.27 Current differential amplifier.

24.4.2 Constant Transconductance Diff-Amp

A rail-to-rail differential amplifier made using n- and p-channel diff-amps is shown in Fig. 24.28 [7,8]. It is desirable, for distortion and compensation reasons, that the overall transconductance of the diff-amp remain constant independent of the region of operation, that is, operation with both n- and p-channel diff-amps on or only a single diff-amp on. A constant g_m is guaranteed over the input range if

$$g_m = g_{mn} + g_{mp} = \sqrt{2\beta_n I_n} + \sqrt{2\beta_p I_p} = \text{constant} \tag{24.76}$$

where g_{mn} and g_{mp} are the transconductances of the n- and p-channel diff-amps and g_m is the overall transconductance of the input stage. Since β_n and β_p are constant and can be made equal, Eq. (24.76) can be rewritten as (assuming both diff-amps are operating),

$$\sqrt{I_n} + \sqrt{I_p} = \text{constant} \tag{24.77}$$

This equation always holds if both differential amplifiers are on. The problem with nonconstant transconductance occurs if only one diff-amp is on. If, for example, the common-mode input (common input voltage on the + and – inputs of the differential amplifier) is large enough to shut the p-channel diff-amp off, then $I_p = 0$ and the transconductance of the overall input diff-amp changes.

The solution to this problem begins by making

$$I_n = I_p = I_o \tag{24.78}$$

When both diff-amps are on (keeping in mind we have already set the requirement that $\beta_n = \beta_p$), Eq. (24.77) reduces to

$$2\sqrt{I_o} = \text{constant} \tag{24.79}$$

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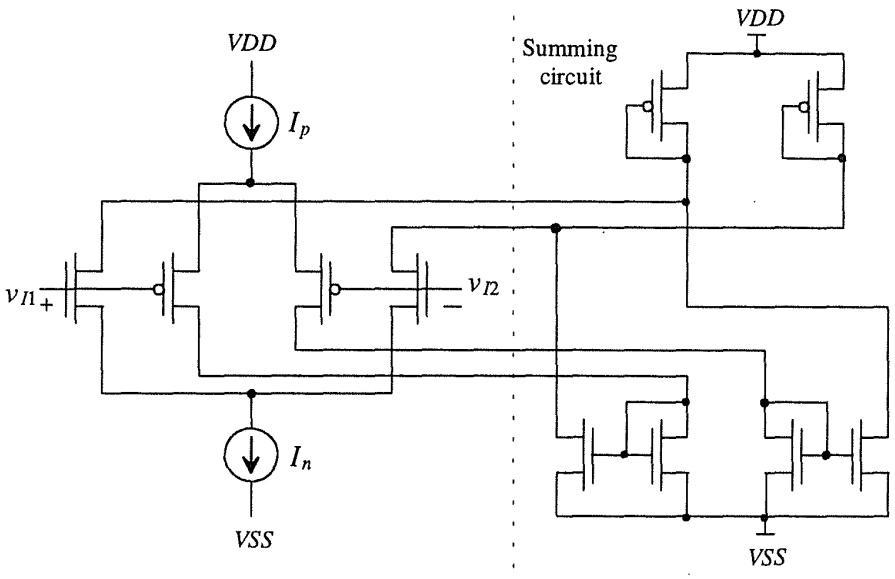


Figure 24.28 Rail-to-rail differential amplifier.

If we add a current of $3I_o$ to I_n (or to I_p) when the p-channel diff-pair (n-channel diff-pair) is off, the transconductance of the pair is constant, or

$$\overbrace{2\sqrt{I_o}}^{\text{both on}} = \overbrace{\sqrt{3I_o + I_n}}^{\text{n diff-amp on}} = \overbrace{\sqrt{3I_o + I_p}}^{\text{p diff-amp on}} \text{ if } I_o = I_p = I_n \qquad (24.80)$$

An example of a constant-g_m rail-to-rail input stage is shown in Fig. 24.29. The summing circuit of Fig. 24.28 is not shown in this figure. MOSFETs M1-M4 make up the p- and n-channel diff-pairs, while MP1 and MN1 source the constant current I_o when both diff-pairs are on. (MP1 and MN1 represent the constant current sources shown in Fig. 24.28.) When both diff-pairs are on, the current out of each current diff-amp is approximately 0. (The drain current of M6 and M7 is approximately 0.) If the common-mode input voltage becomes large enough to shut the p-channel diff-pair off, then MOSFETs MS1 and MS2 are off as well. This causes the current in M5 to become I_o. The current in M6 mirrors the current in M5. Since M6 is three times larger than M5, the current in M6 becomes $3I_o$.

Discussion

In general, the constant-g_m diff-amp is used in an op-amp to keep from overcompensating the op-amp and to avoid distortion when the op-amp is used with large signals where the diff-amps, on the input of the op-amp, are turning on and off with variations in the input signal. Several practical problems exist with these uses of the constant-g_m diff-amp. Since the value of g_m may vary with process variations by 20

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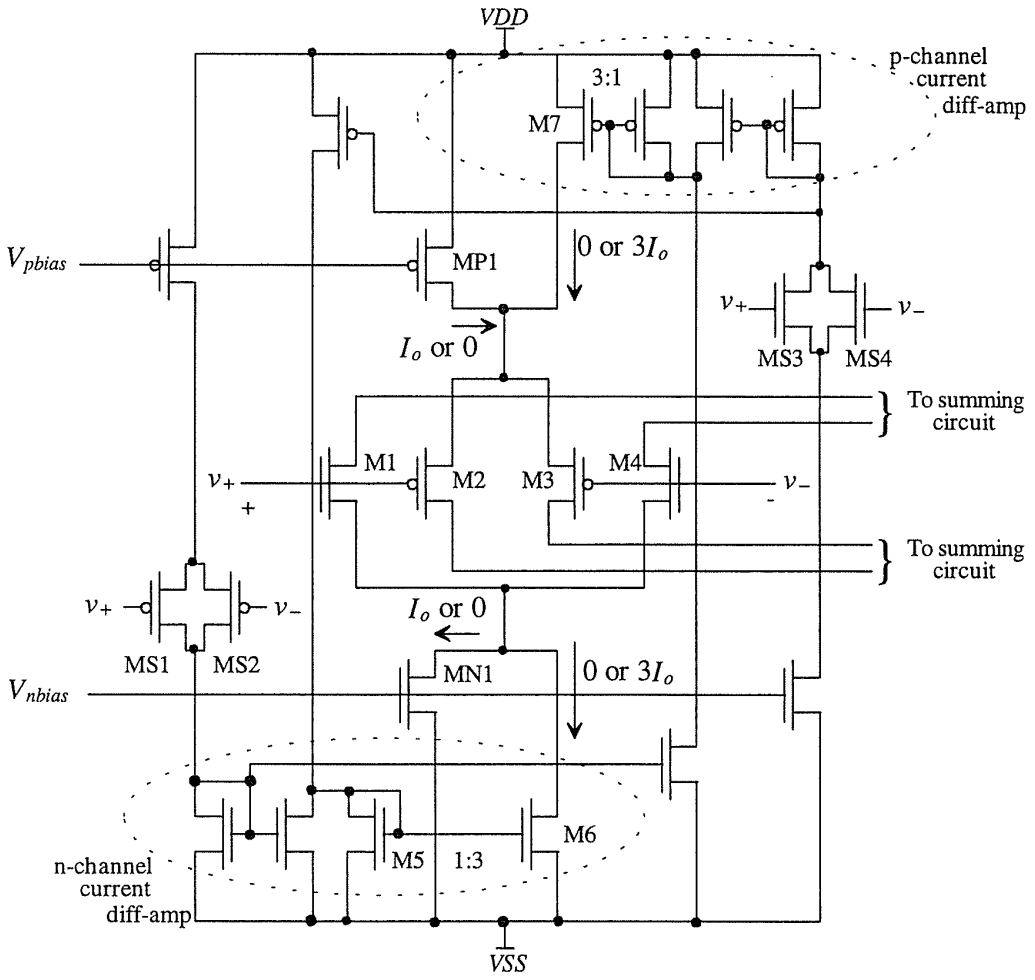


Figure 24.29 A wide-swing diff-amp with constant gm.

percent we may still overcompensate an op-amp design. Using the constant-g_m stage to avoid overcompensation is useful, but since we may over- (or under-) compensate the op-amp with process variations, the added complexity and power draw may not yield improvements justifying the additional circuitry. Using the constant-g_m stage to avoid distortion is based on keeping the unity gain frequency of an op-amp, f_u, a constant independent of the common-mode input voltage. In practice, mismatches (threshold voltage and geometry) in the input diff-pair and changes in DC biasing conditions, resulting from the diff-amps turning off and on, can cause distortion. In some cases, this distortion can be worse than the distortion resulting from the nonconstant f_u (which we get with the nonconstant g_m diff-amp). The distortion resulting from mismatches can be modeled as an offset-voltage that is dependent on the input common-mode

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voltage. Since the DC currents sourced or sinked from a constant-g_m diff-amp are not constant, the DC operating point of the circuit summing the currents changes with the input signals' amplitude. The result is a change in the low-frequency gain and added distortion.

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PROBLEMS

24.1 For the diff-amp shown in Fig. P24.1 determine the drain current of M1 as a function of the input voltage, $v_{I1} - v_{I2}$. Show your work and neglect body effect.

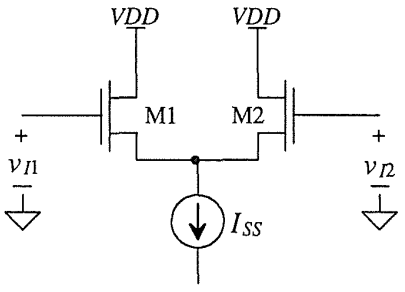


Figure P24.1

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24.2 Repeat Ex. 24.1 if the widths of M1 and M2 are increased to 100 μm. Determine the transconductance of the diff-amp. Write i_{d2} as a product of g_m (= $g_{m1} = g_{m2}$) and v_{I1} (with v_{I2} = AC ground), v_{I2} (with v_{I1} = AC ground), and $v_{I1} - v_{I2}$.

24.3 Using the diff-amp topology shown in Fig. P24.3, design a circuit that will change a 1-V square wave into a 0 to 5 V square wave at 1 kHz. Note that many of the MOSFETs in this circuit are operating in the cutoff, saturation, or triode regions.

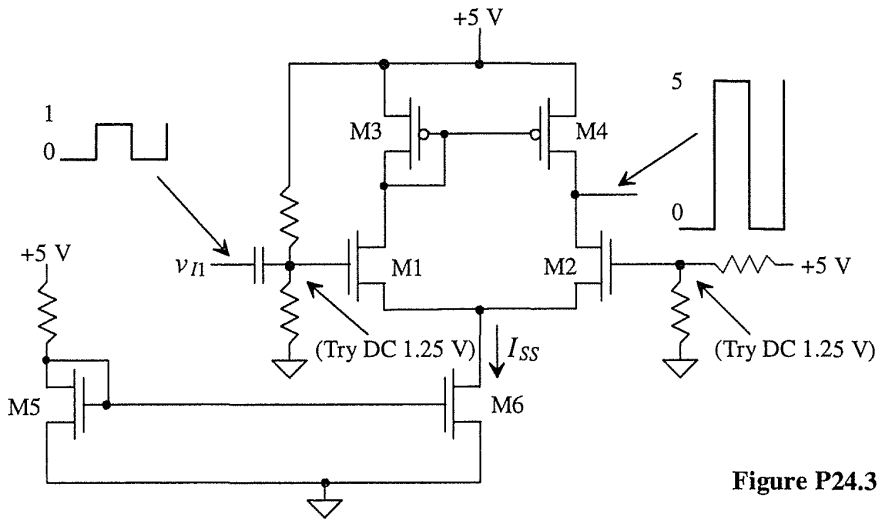


Figure P24.3

24.4 Simulate the operation of the circuit designed in Problem 24.3.

24.5 Determine the small-signal gain and the input common-mode-range (CMR) for the diff-amps shown in Fig. P24.5. All n-channels are 15/5, all p-channels are 70/5, and the resistors are 3.8 MEG.

24.6 Verify the results of Problem 24.5 using SPICE.

24.7 Estimate the slew-rate limitations in charging and discharging a 1 pF capacitor tied to the outputs of the diff-amps shown in Fig. P24.5.

24.8 For the n-channel diff-pair shown in Fig. P24.8, show that if the body effect is included in the analysis of the transconductance, the following relationships are valid.

$$i_{d1} = \frac{g_m}{2}[v_{i1} - v_{i2}] - \frac{g_{mb}}{2}[v_{i1} + v_{i2}]$$

$$i_{d2} = -\frac{g_m}{2}[v_{i1} - v_{i2}] - \frac{g_{mb}}{2}[v_{i1} + v_{i2}]$$

Remember that when the body of the n-channel MOSFET is not drawn, it is connected to *VSS*.

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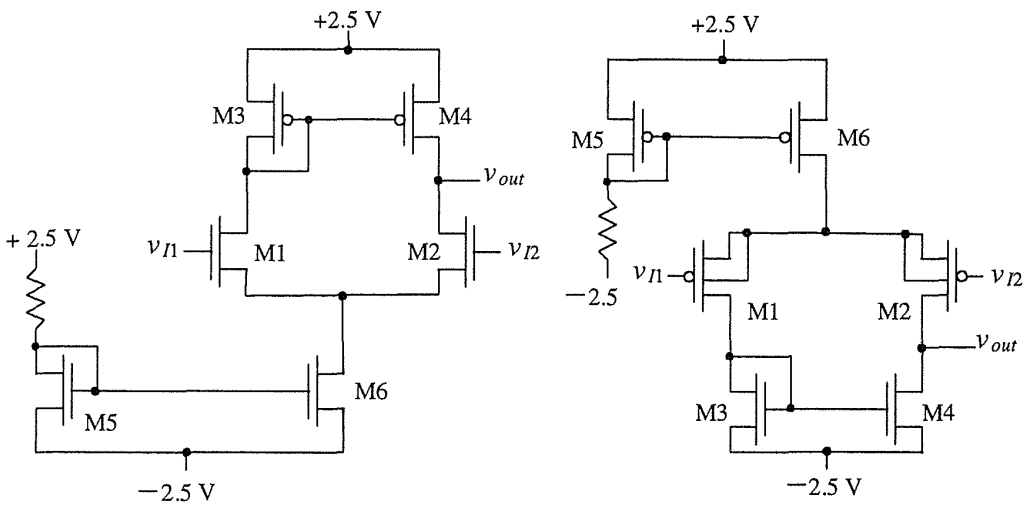


Figure P24.5

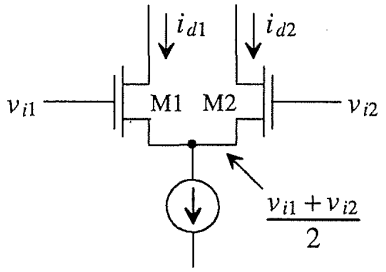


Figure P24.8

24.9 The diff-amp configuration shown in Fig. P24.9 is useful in situations where a truly differential output signal is needed. Determine the following:

(a) The transconductance of the diff-amp.

(b) The drain currents of all MOSFETs in terms of the input voltages and g_{mn} (the transconductance of an n-channel MOSFET).

(c) The small-signal voltage gain, $(v_{O1} - v_{O2})/(v_{I1} - v_{I2})$.

24.10 Determine the CMRR of the diff-amp shown in Fig. 24.13 if a cascode current source is used for the tail current, that is, I_{SS}.

24.11 Develop an expression for the CMRR of the diff-amp of Fig. 24.13 as a function of frequency, assuming the current source output impedance can be modeled by a simple capacitor. Assume that the parasitic capacitance on the drain of M4 is negligible.

24.12 Determine the RMS input noise voltage for the diff-amp of Ex. 24.2 over a bandwidth of 1 to 1 kHz. Assume $KF = 10^{-25}$ V^{2}F and $AF = 1.3$.

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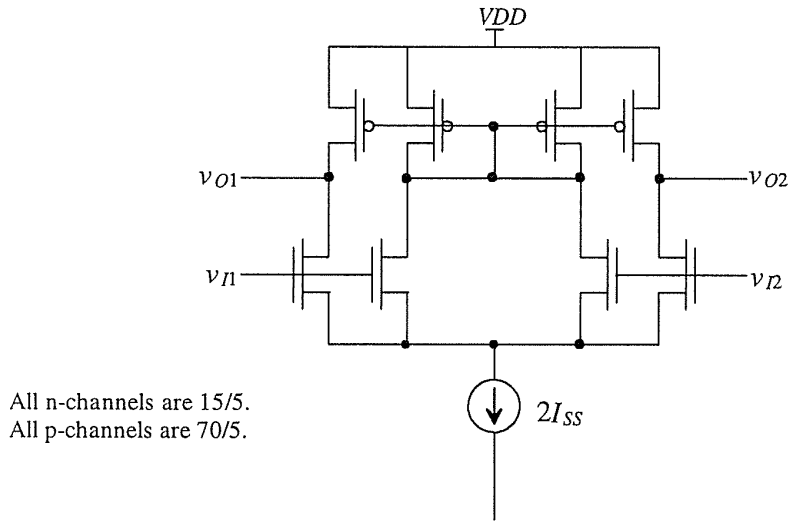


Figure P24.9

24.13 Verify the calculated noise voltage determined in Problem 24.12 with SPICE simulation results.

24.14 Repeat Ex. 24.5 if the MOSFETs (both n- and p-channels) used in the diff-amp are 100/5.

24.15 Determine the small-signal gain of the amplifier shown in Fig. P24.15. Also determine the input CMR of the amplifier if the minimum voltage across a current source/sink is 0.3 V.

24.16 Repeat Problem 24.15 if the active current source loads M6/M8 and M5/M7 are replaced with wide-swing current mirrors, Fig. P24.16. Note that the CMR of the amplifier remains unchanged if V_{bias} is selected correctly; see the discussion in Sec. 20.2.

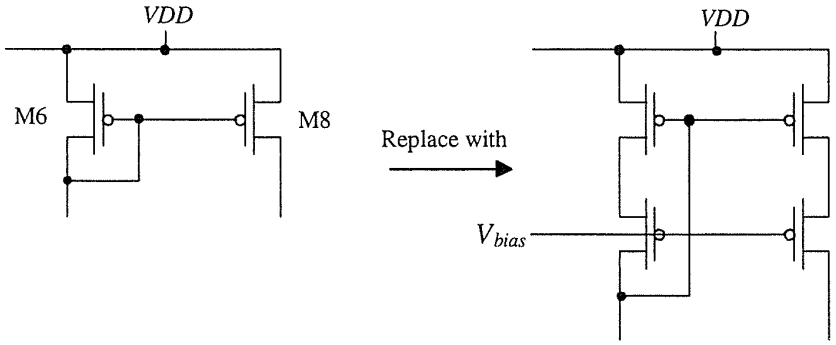
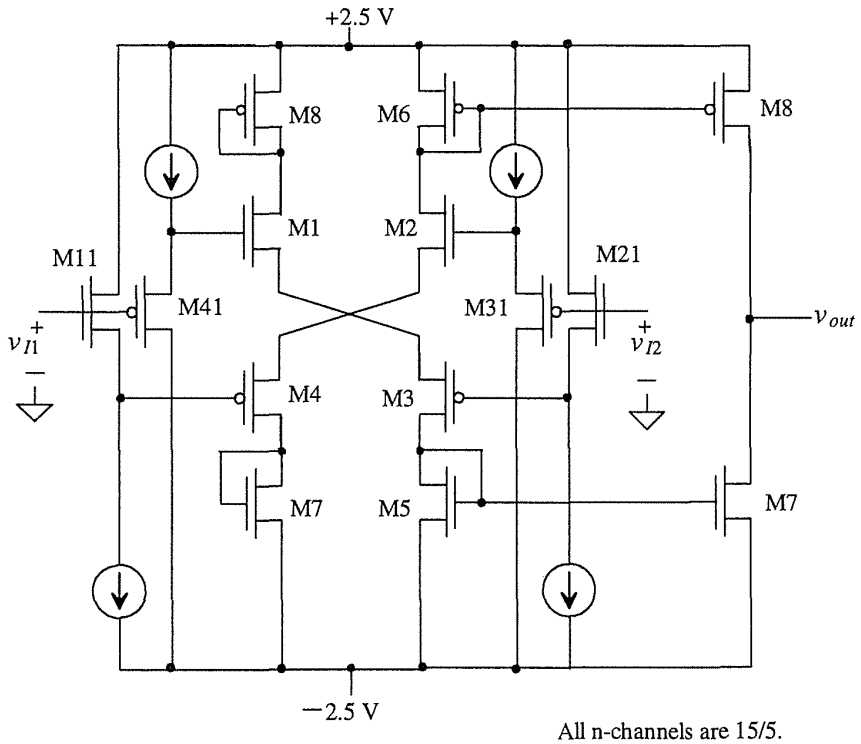


Figure P24.16

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All n-channels are 15/5.
All p-channels are 70/5.
The current sources/sinks are 10 μA.

Figure P24.15

All unlabeled n-channels 15/5.
All unlabeled p-channels 70/5.

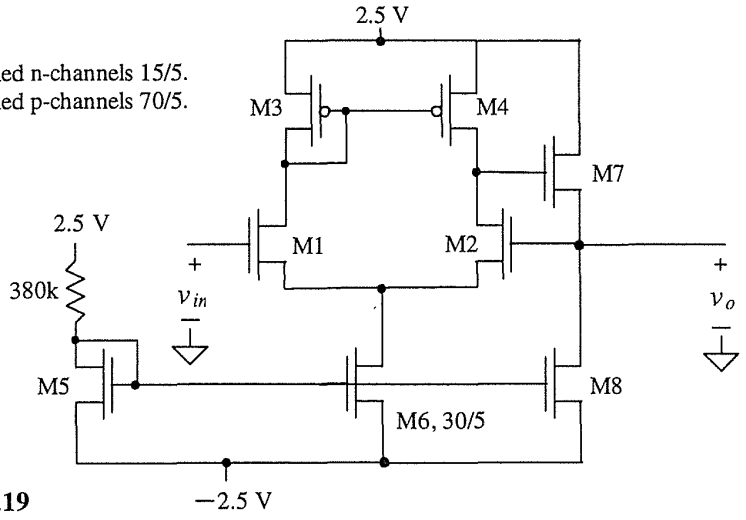


Figure P24.19

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24.17 Repeat Ex. 24.6 if I_{SS} is 2 μA.

24.18 If $VDD = -VSS = 2.5$ V, $I_{SS} = 10$ μA, and an n-channel MOSFET size of 15/5, estimate the input CMR (in current) for the current diff-amp of Fig. 24.25.

24.19 Determine v_o/v_{in} for the circuit of Fig. P24.19. This circuit is a voltage follower.

24.20 What is the purpose of MS1/MS2 and MS3/MS4 in the diff-amp of Fig. 24.29?

24.21 Show that the output current of the circuit shown in Fig. P24.21 is related to the square of the difference of the input voltages, v_{I1} and v_{I2}.

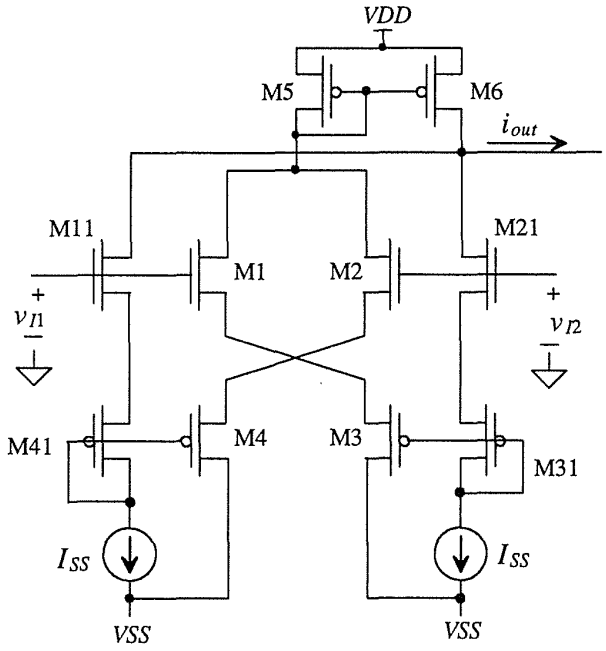


Figure P24.21

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Chapter

25

Operational Amplifiers

The operational amplifier (op-amp) is a fundamental building block in analog integrated circuit design [1-3]. A block diagram of the two-stage op-amp with output buffer is shown in Fig. 25.1. The first stage of an op-amp is a differential amplifier. This is followed by another gain stage, such as a common source stage, and finally an output buffer. If the op-amp is intended to drive a purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. If the op-amp is used to drive a resistive load or a large capacitive load (or a combination of both), the output buffer is used.

Since it is difficult to characterize a packaged op-amp that cannot drive a resistive load, we will begin the chapter with a discussion of the two-stage op-amp with output buffer. Design of the op-amp consists of determining the specifications, selecting device sizes and biasing conditions, compensating the op-amp for stability, simulating and characterizing the op-amp A_{OL} (open-loop gain), CMR (common-mode range on the input), CMRR (common-mode rejection ratio), PSRR (power supply rejection ratio), output voltage range, current sourcing/sinking capability, and power dissipation.

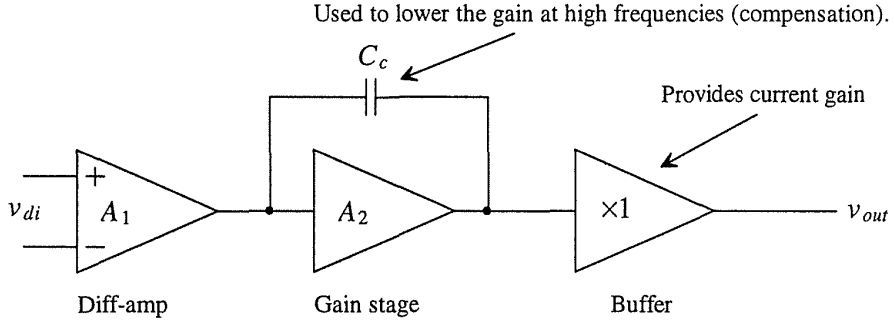


Figure 25.1 Block diagram of two-stage op-amp with output buffer.

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25.1 Basic CMOS Op-Amp Design

One possible op-amp design is shown in Fig. 25.2. We will use this configuration to illustrate the design of a CMOS op-amp.

Selection of the Differential Amplifier Bias Current, I_{SS}

Selection of the current I_{SS} is determined by gain, CMR, CMRR, power dissipation, noise, matching considerations and slew rate. (If slew rate is a concern, the source cross-coupled diff-amp should be considered for the first stage of the op-amp.) The small-signal gain of the differential amplifier is given in Eq. (24.25), or

$$A_1 = g_{m1}(r_{02} \| r_{o4}) = \frac{2\sqrt{\beta}}{(\lambda_2 + \lambda_4)\sqrt{I_{SS}}} = \frac{2}{(\lambda_2 + \lambda_4)(V_{GS} - V_{THN})} \tag{25.1}$$

In addition to selecting I_{SS}, we must determine a V_{GS} of the MOSFETs. Often, selection of the bias current is an iterative process: that is, we select a bias current and verify that the above characteristics of most importance are met. In general, the larger (increasing W while holding L constant) we make the MOSFETs in the differential pair at a given bias current, the lower V_{GS}, CMR is increased, noise is lowered, matching is better, and gain is increased (from the increase in β). The main drawbacks are increased layout area and parasitic capacitances (and thus lower speed).

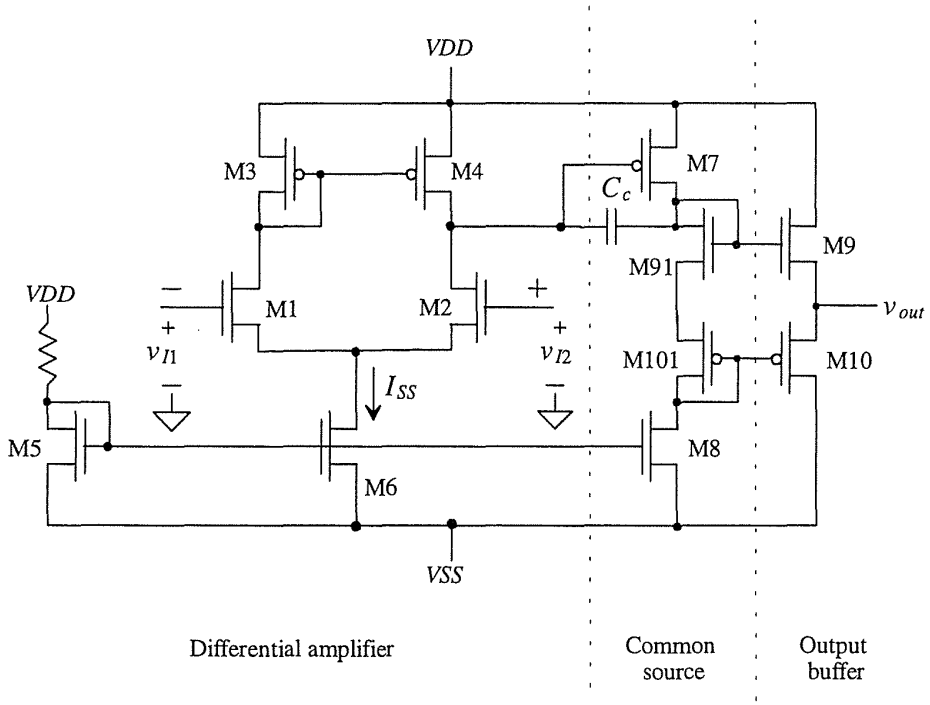


Figure 25.2 Operational amplifier with output buffer.

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We may start by selecting I_{SS} = 20 μA and V_{GS} = 1.2 V, which results in the differential amplifier of Exs. 24.2, 24.3, and 24.4 and Fig. 24.11. When designing an op-amp for off-chip use, the MOSFETs used in the differential input stage normally have widths in the several hundred μm range. For the same I_{SS} this increases the open-loop gain of the op-amp while decreasing V_{GS} (a desirable effect to improve op-amp common-mode range).

Selection of Device Sizes

The next step in the design of the op-amp is selection of the second-stage biasing current. The same considerations that applied to selection of the differential amplifier biasing current apply to the selection of the second-stage biasing current. It would be helpful at this point to review Fig. 20.3. With both inputs to the op-amp, (i.e., the gates of M1 and M2), at the same potential, the same current flows in M3 and M4. The result is that the drain of M4 is at the same potential as its gate. If we want to set the current that flows in M7 at 10 μA, we simply size it the same size as M4. If we want 5 μA to flow, we size M7 so that its *W/L* is half of M4s, that is, 35/5. We then size M8 so that its drain current, 10 μA in the present case, is equal to the current in M7. The gain of the second stage is given, assuming that $1/g_{m91} + 1/g_{m101}$ is small compared to $r_{o7}||r_{o8}$, by

$$A_2 = -g_{m7} \cdot (r_{o7}||r_{o8}) = \frac{-\sqrt{2\beta_7 I_{D7}}}{(\lambda_7 + \lambda_8) I_{D7}} = \frac{-2}{(\lambda_7 + \lambda_8)(V_{SG} - V_{THP})} \qquad (25.2)$$

The open-loop gain of the op-amp is given by

$$A_{OL} = A_1 \cdot A_2 = g_{m1}(r_{02}||r_{o4}) \cdot [-g_{m7}(r_{o7}||r_{o8})] \qquad (25.3)$$

If we use the sizes of Fig. 25.3, the open-loop gain of the op-amp is

$$|A_{OL}| = \overbrace{\sqrt{2 \cdot 50\frac{\mu A}{V^2} \cdot \frac{15}{5} \cdot 10\mu A}}^{g_{m1}} \cdot \overbrace{\left[\frac{1}{(0.06+0.06)10\mu A}\right]^2}^{(r_{o2}||r_{o4})\cdot(r_{o7}||r_{o8})} \cdot \overbrace{\sqrt{2 \cdot 17\frac{\mu A}{V^2} \cdot \frac{70}{5} \cdot 10\mu A}}^{g_{m7}}$$

$$= 2,600 \frac{V}{V}$$

Decreasing the bias currents to 1 μA will increase the open-loop gain by a factor of 10.

The output stage is a class AB type discussed in Ch. 22. The MOSFETs M91 and M101 are used to bias the source-follower buffers M9 and M10. The gate of M9 can swing up to *VDD*. If we want no more than 1.2 V across the gate-source potentials of M9 or M10, then the maximum current we can source, neglecting the body effect, is given by

$$I_{OUTMAX} = \frac{\beta_9}{2}(V_{GS9} - V_{THN})^2 = 50\frac{\mu A}{V^2} \cdot \frac{150}{2}(1.2 - 0.83)^2 = 500\ \mu A \qquad (25.4)$$

while the minimum current is given by

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$$I_{OUTMIN} = \frac{\beta_{10}}{2}(V_{SG10} - V_{THN})^2 = 17\,\frac{\mu A}{V^2} \cdot \frac{700}{2}(1.2 - 0.91)^2 = -500\ \mu A \quad (25.5)$$

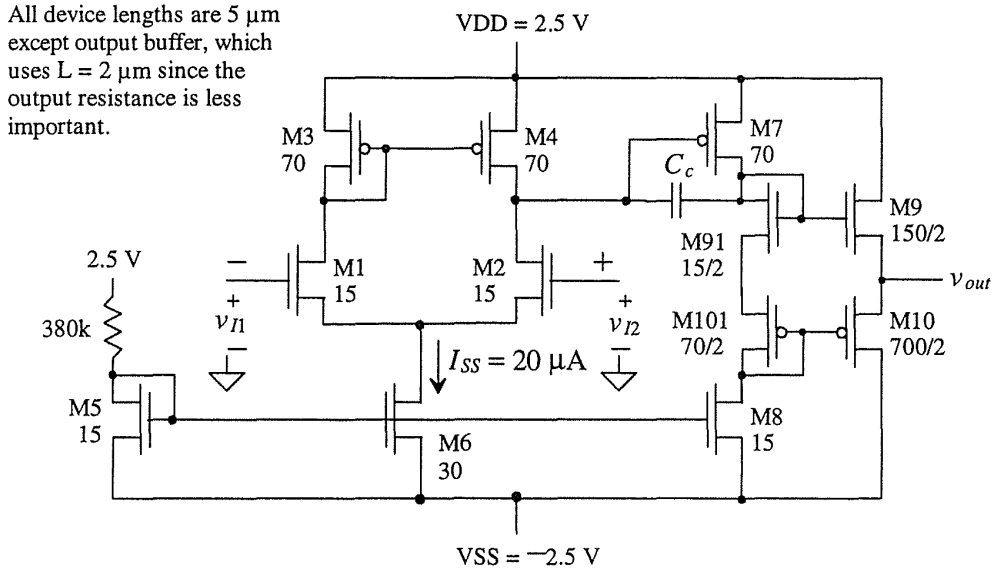


Figure 25.3 Operational amplifier with sizes.

Under these circumstances (load currents), the maximum output swing is given by

$$V_{OUTMAX} = VDD - 1.2 \quad (25.6)$$

and

$$V_{OUTMIN} = VSS + 1.2 \quad (25.7)$$

The maximum output current is highly dependent on the output voltage of the amplifier. For example, if $V_{out} = 0$ V, the op-amp, with 2.5 V supplies, can source a current of

$$I_{OUTMAX} = 50\frac{\mu A}{V^2} \cdot \frac{150}{2}(2.5 - 0.83)^2 = 10\ mA \quad (25.8)$$

The power dissipated by M9 is 2.5·0.010 = 25 mW! After reviewing the temperature characteristics of MOSFETs from Ch. 9, we can see that V_{GS9} will increase (until M9 shuts off) keeping the device from thermal runaway. Although the device and op-amp should not be harmed by this excessive power draw, it still may be important to avoid this situation. Implementation of a maximum current detect or short-circuit protection circuit on the output of the op-amp is needed. Consider the short-circuit protection circuit of Fig. 25.4. When the output current exceeds a value set by

$$I_{OUTMAX} = \frac{V_{THN}}{R} \quad (25.9)$$

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for an op-amp sourcing current or

$$I_{OUTMIN} = \frac{V_{THP}}{R} \tag{25.10}$$

for an op-amp sinking current, the gate drive is removed from M9 or M10. This keeps the MOSFETs from sourcing or sinking too much current. Typical values of the resistor for the present circuit are 1 kΩ.

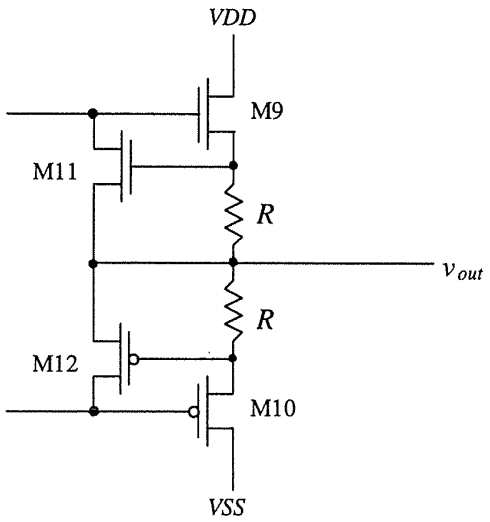


Figure 25.4 Addition of M11, M12, and the resistors to output stage for short-circuit protection.

Compensating the Op-amp

The last step in our first cut of the op-amp design is to select the compensation network. The closed-loop gain of an op-amp can be written in terms of the feedback equation by

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta} \tag{25.11}$$

We know from our discussion in Ch. 23 that the feedback amplifier becomes unstable when the loop gain $A_{OL}\beta = -1$. This is equivalent to the requirement that

$$|A_{OL}\beta| = 1 \text{ and } \angle A_{OL}\beta = \pm 180° \tag{25.12}$$

We know that β represents the amount of the output signal that is fed back and subtracted from the input of the amplifier. Therefore, the largest value of β possible without an amplifier in the feedback loop occurs when all of the output is fed back to the input, or in other words β = 1. The voltage follower configuration shown in Fig. 25.5 is an example of a closed-loop amplifier with β = 1. Under these circumstances, we can rewrite Eq. (25.12) as

$$|A_{OL}| = 1 \text{ and } \angle A_{OL} = \pm 180° \tag{25.13}$$

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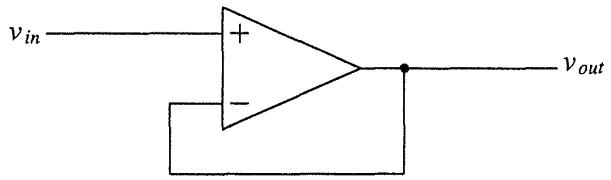


Figure 25.5 Voltage follower configuration, an example of a closed-loop amplifier with unity feedback factor.

We will use this result (i.e., we will consider the open-loop gain of an amplifier) in the following discussion on compensating the operational amplifier.

The small-signal model of the two-stage op-amp, considering the high-impedance nodes that give rise to the dominant poles, is shown in Fig. 25.6. The resistance to ground at the output of the differential amplifier is given by

$$R_1 = r_{o2} || r_{o4} \tag{25.14}$$

while the capacitance, see Eq. (24.28), at this node is given by

$$C_1 = C_{gs7} + C_{gd7}(1 + |A_2|) + C_{db4} + C_{gd4} + C_{db2} + C_{gd2} \tag{25.15}$$

For the present amplifier

$$R_1 = 833 \text{ k}\Omega$$

With the help of Ex. 24.4 and knowing

$$C_{gs7} = \frac{2}{3} \cdot C'_{ox} \cdot W_7 L_7 = 187 \text{ fF}$$

and

$$C_{gd7} = W \cdot CGDO = 70 \text{ µm} \cdot 5 \times 10^{-10} \frac{\text{F}}{\text{m}} = 35 \text{ fF}$$

The gain of stage two, A_2, from Eq. (25.2) is – 58 V/V. The capacitance C_1 is given, with the results of Ex. 24.4, by

$$C_1 = 187 + 35(1 + 58) + 190 = 2.44 \text{ pF}$$

The pole resulting from this time constant for the circuit shown in Fig. 25.3 is given by

$$f_1 = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \cdot 833 \text{ k} \cdot 2.44 \text{ pF}} = 78 \text{ kHz}$$

The pole resulting from the high-impedance node at the drain of M7 is characterized by R_2 and C_2, or

$$R_2 = r_{o7} || r_{o8} \tag{25.16}$$

and

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$$C_2 = C_{gd7}\left[1 + \frac{1}{|A_2|}\right] + C_{db7} + C_{db8} + C_{gd8} + C_{gd9} + C_{gd10} \qquad (25.17)$$

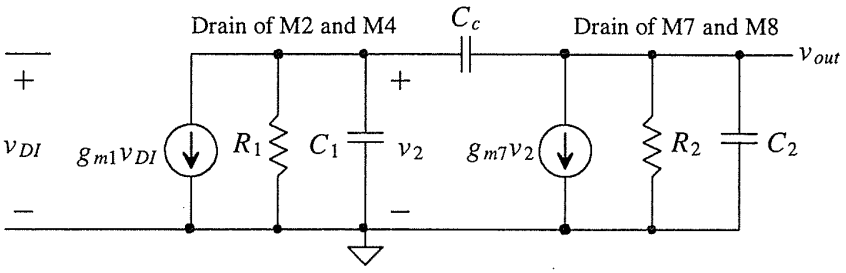


Figure 25.6 Small-signal model of two-stage op-amp.

The value of R_2 is the same as R_1 because the bias currents of the first and second stages are identical. The value of C_2 is the sum of C_{gd7} = 35 fF, C_{db7} = 137 fF, C_{db8} = 9.4 fF, C_{gd8} = 5.7 fF, and

$$C_{gd9} = 150\ \mu\text{m} \cdot 3.8 \times 10^{-10} = 57\ \text{fF}$$

and

$$C_{gd10} = 700\ \mu\text{m} \cdot 5 \times 10^{-10} = 350\ \text{fF}$$

or C_2 = 600 fF. The pole resulting from the high-impedance node at the drains of M9 and M10 is located at a frequency given by

$$f_2 = \frac{1}{2\pi R_2 C_2} = 318\ \text{kHz}$$

So far we have not considered the effect of adding a compensation capacitor C_c. Before we try to compensate the amplifier to ensure that it remains stable, let's discuss simulation of the open-loop gain of the amplifier. The simulation of the open-loop gain will be another indication of the dominant pole locations and can be compared to the hand calculations given above. A circuit useful in simulating the open-loop gain of an

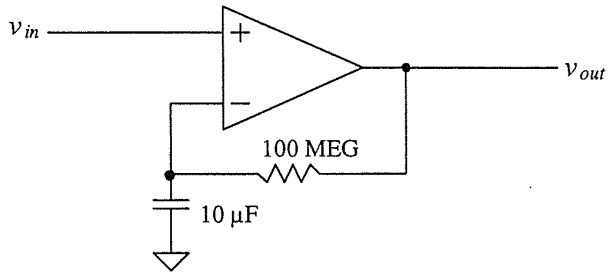


Figure 25.7 Circuit configuration used to measure open-loop gain and frequency response.

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op-amp with or without compensation is shown in Fig. 25.7. The resistive feedback ensures a stable DC operating condition, while the capacitor/resistor combination eliminates output AC signals fed back from the output of the op-amp. The SPICE simulation results of the amplifier described above without compensation and given schematically in Fig. 25.3 are shown in Fig. 25.8. The point at which the open-loop gain is unity (0 dB) corresponds to a phase shift of 160°, or a – 20 ° phase margin. In other words, highly unstable. Normally, we desire no less than a + 45 ° phase margin when compensating an op-amp.

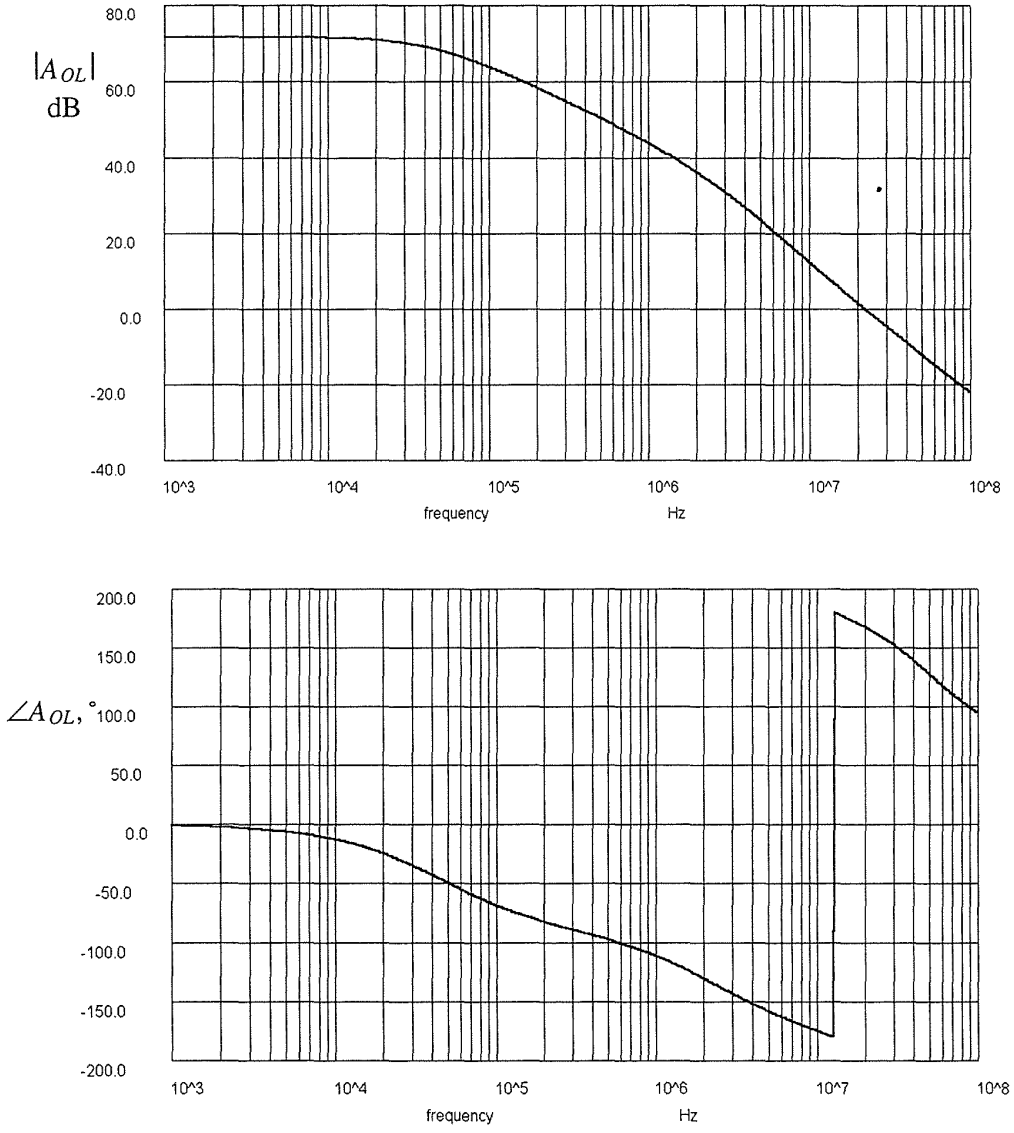


Figure 25.8 Open-loop uncompensated frequency response of the amplifier of Fig. 25.3.

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The compensation capacitor causes the gain to roll off long before the second pole takes effect. If C_c is much larger than C_1 ($v_2 \approx 0$ and all of $g_{m1}v_{DI}$ flows through C_c), then we can write the output voltage in terms of the input voltage as

$$v_{out} = \overbrace{g_{m1}v_{DI}}^{\text{I out of 1st stage}} \cdot \frac{1}{j\omega C_c} \tag{25.18}$$

$$A_{OL} = \frac{v_{out}}{v_{DI}} = \frac{g_{m1}}{j\omega C_c} \tag{25.19}$$

If we label the frequency when the magnitude of the open-loop gain is unity as f_u, then we can select the compensation capacitor based on

$$|A_{OL}| = \frac{g_{m1}}{2\pi f C_c} \tag{25.20}$$

or when $|A_{OL}|$ is unity

$$C_c = \frac{g_{m1}}{2\pi f_u} \tag{25.21}$$

This equation is useful for general-purpose op-amp design especially where bandwidth of the amplifier is not critical.

Compensation of the op-amp of Fig. 25.3 begins by inspecting the open-loop gain magnitude and phase plots of Fig. 25.8. Our hand calculations showed f_1 = 78 kHz and f_2 = 318 kHz, while SPICE simulation results give f_1 = 50 kHz and f_2 = 1.5 MHz. If we set the unity gain frequency at the location of the second pole, the phase of A_{OL} is approximately 135°, corresponding to a phase margin of 45°. To give a little more margin, we will set f_u to 1 MHz. The compensation capacitor is then

$$C_c = \frac{55\frac{\mu A}{V^2}}{2\pi 10^6} = 8.75 \text{ pF}$$

The compensated op-amp phase and magnitude plots are shown in Fig. 25.9. The phase margin is approximately 45°. Practically speaking, it may be wise to increase the compensation capacitor to 10 pF for a little extra head room.

At this point we may ask the question, "Why do we need a phase margin anyway?" The answer to this question involves the realization that a large load capacitance can increase the phase shift through the op-amp and the feedback network normally does not have zero propagation delay. Consider using an n-well resistor in the feedback loop. The delay through the n-well resistor translates into a phase shift at a given frequency given by

$$\theta = t_{delay} \cdot f \cdot 360° \tag{25.22}$$

Another important characteristic of adding a compensation capacitor is that the compensation capacitor combined with the diff-pair bias current sets the slew rate out of

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the op-amp. The maximum rate the output of an op-amp can change is approximated by I_{SS} charging C_c or

$$SR = \frac{dV_{out}}{dt} = \frac{I_{SS}}{C_c} \tag{25.23}$$

This is an important design factor in some situations. Replacing the source coupled pair with the source cross-coupled pair can eliminate slew-rate limitations in the basic two-stage op-amp at the price of a more complicated circuit and high-power dissipation.

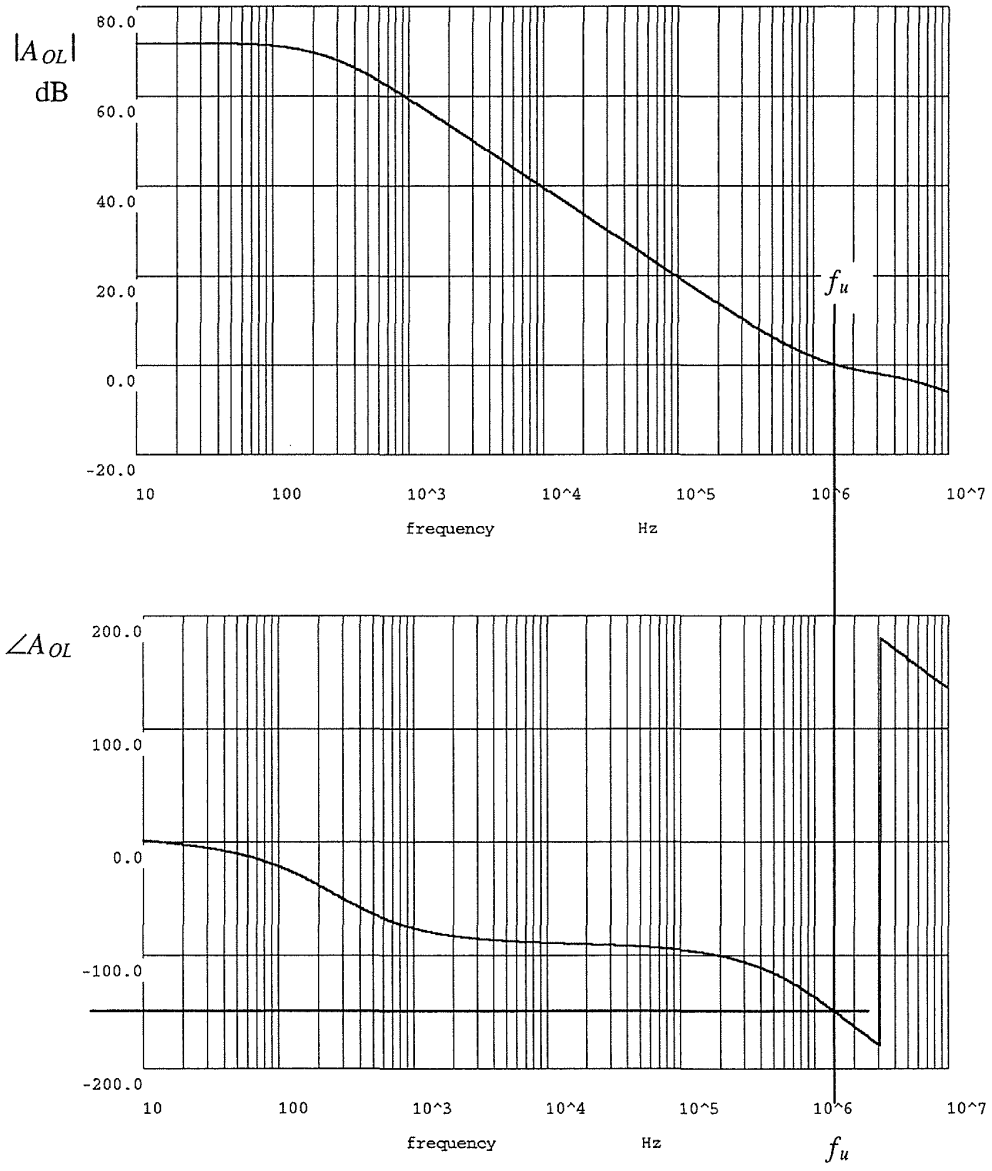


Figure 25.9 Open-loop compensated op-amp of Fig. 25.3.

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In the derivation of this compensation scheme, we assumed that C_c was much greater than C_1. This approximation has several practical problems. Reviewing Fig. 25.9, we see that A_{OL} has a zero at approximately f_u. The effect of the zero is to cause f_u to be less well defined. A more exact analysis of the two-stage op-amp *with* compensation capacitor of Fig. 25.6 gives a transfer function of

$$\frac{v_{out}}{v_{DI}} = \frac{g_{m1}g_{m7}R_1R_2\left(1-\frac{sC_c}{g_{m7}}\right)}{s^2R_1R_2[C_1C_2+C_c(C_1+C_2)]+s[R_1(C_1+C_c)+R_2(C_2+C_c)+g_{m7}R_1R_2C_c]+1} \tag{25.24}$$

The poles of this equation can be approximated by

$$p_1 \approx \frac{-1}{(1+g_{m7}R_2)C_cR_1} \tag{25.25}$$

and

$$p_2 \approx \frac{-g_{m7}C_c}{C_2C_1+C_2C_c+C_cC_1} \tag{25.26}$$

A right-hand plane zero is also present and is given by

$$z = \frac{g_{m7}}{C_c} \tag{25.27}$$

Comparing this result with Eq. (25.20), we see that if the transconductance of the first and second stages is comparable, the unity gain frequency of the op-amp and the location of the zero occur close together. Since the zero is in the right-half plane, the phase margin is further degraded. Intuitively, this effect can be understood by realizing that the output of the first stage is fed directly to the output of the second-stage, without inversion, through the compensation capacitor effectively degrading the phase margin.

To circumvent this feedthrough problem, we can insert a resistor in series with the compensation capacitor as shown in Fig. 25.10. Addition of the resistor R_z shifts the zero to a location given by

$$z = \frac{1}{C_c\left(\frac{1}{g_{m7}}-R_z\right)} \tag{25.28}$$

If we select R_z so that it is equal to $1/g_{m7}$ the zero disappears. Making R_z larger than $1/g_{m7}$ causes the zero to add to the open-loop phase response, increasing the phase margin. For this reason, this type of compensation is sometimes referred to as lead compensation.

For the op-amp of Fig. 25.3 with $g_{m7} = 70\ \mu A/V^2$, the value of the zero canceling resistor can be determined by

$$R_z = \frac{1}{g_{m7}} = 14.5\ k\Omega \tag{25.29}$$

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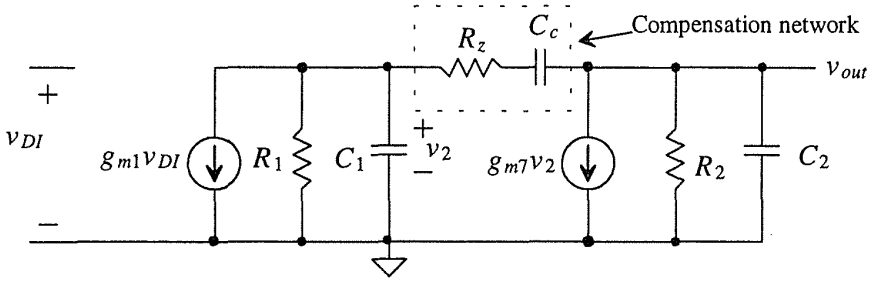


Figure 25.10 Practical compensation of a two-stage op-amp.

The selection of the compensation capacitor C_c is unchanged from our previous discussion since R_z has no effect on the low-frequency pole. A complete schematic[1] of the op-amp is shown in Fig. 25.11 with the compensation network in place. The open-loop gain magnitude and phase with this compensation network are shown in Fig. 25.12. The phase margin of the op-amp with the R_z / C_c combination is greatly improved over the C_c alone. *Any practical two-stage op-amp design should use the zero nulling resistor in the compensation network.*

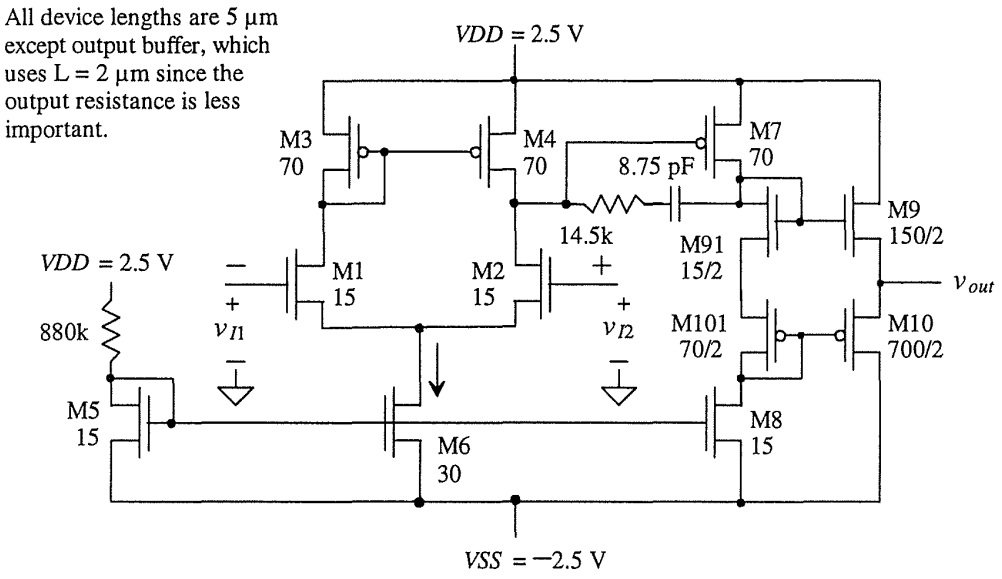


Figure 25.11 Op-amp schematic with compensation.

[1] We could bias the op-amp with a current source instead of the 880k resistor shown in Fig. 25.3. We chose to use the resistor to keep the schematic simple. In practice, any of the current references of Ch. 21 can provide the current through M15 and thus bias the op-amp.

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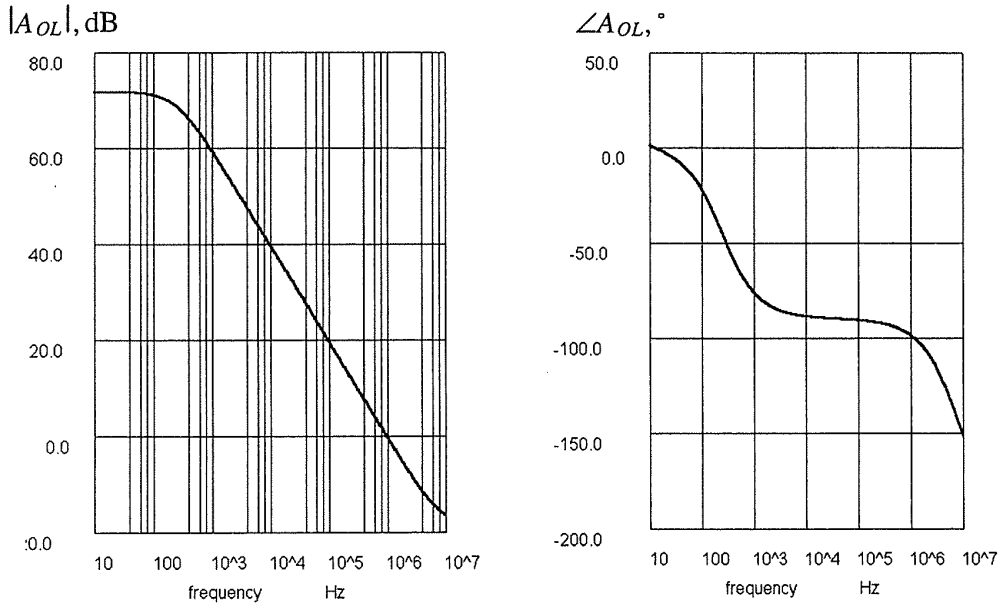


Figure 25.12 Open-loop gain and phase response of the amplifier of Fig. 25.11 with zero nulling resistor. Phase margin is approximately 80°.

The resistor, R_z, can also be implemented using a MOSFET (M13 in Fig. 25.13). This implementation is more desirable in general because the effective channel resistance of M13 can be selected to track the inverse of g_{m7} over temperature and process variations. A bias circuit consisting of M14, M15, and M16 generates a gate voltage for M13 (the MOSFET used as R_z). The channel resistance of a p-channel MOSFET in the triode region, from Ch. 9, is given by

$$R_{ch} = \frac{1}{\beta(V_{SG} - V_{THP})} = R_z \tag{25.30}$$

or setting this in terms of g_{m7} we arrive at

$$g_{m7} = \beta_7(V_{SG7} - V_{THP}) \text{ and } R_{ch}^{-1} = \beta_{13}(V_{SG13} - V_{THP}) \tag{25.31}$$

Using these two equations to determine the product of g_{m7} and R_{ch}, assuming $\beta_7 = \beta_{14} = \beta_{15}$ and $\beta_8 = \beta_{16}$, gives

$$g_{m7}R_{ch} = \frac{\beta_7}{\beta_{13}} = g_{m7}R_z \tag{25.32}$$

To make the zero vanish, from Eq. (25.28), we set the product equal to unity. For our op-amp of Fig. 25.11, we simply size M13 of Fig. 25.13 to 70/5, which is the same size as M7. For lead compensation (i.e., to increase the phase margin further), we set the product to a number greater than zero. The price we pay for reducing the op-amp sensitivity to process variations is a more complicated circuit and higher power dissipation.

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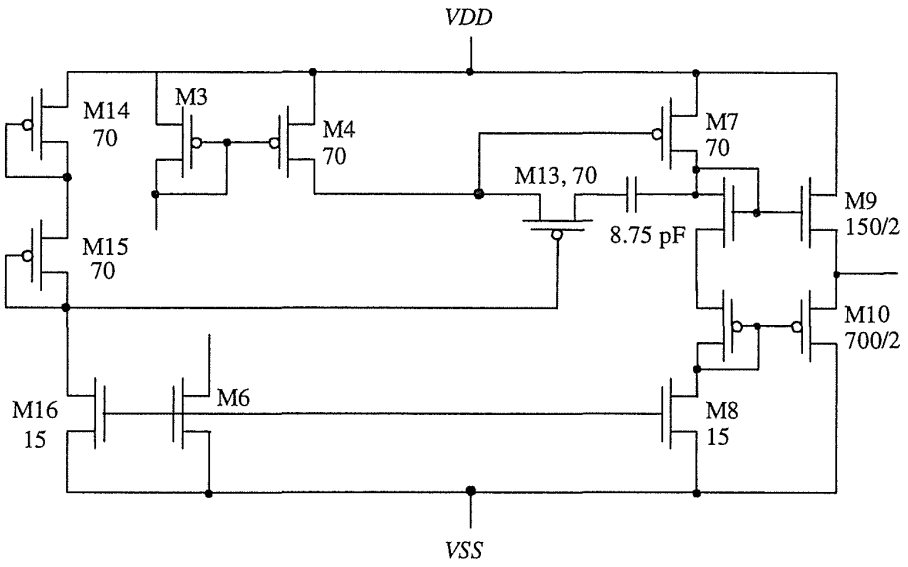


Figure 25.13 Partial schematic of an op-amp showing the use of M13 as a process-insensitive resistor used for compensation.

25.1.1 Characterizing the Op-Amp

Now that we have a rough op-amp design, we need to characterize the op-amp to determine its characteristics.

Input Offset Voltage

An op-amp parameter of great importance is the input offset voltage. Ideally, if we ground both inputs to the op-amp, the output voltage is zero. Realistically, the output voltage is nonzero because of mismatches in the input stage, called *random offsets*, and because the potential on the output of the second stage (for the example op-amp of this chapter, on the drains of M7 and M8) is not well defined, leading to a *systematic offset*. The random offsets in current mirrors and differential amplifiers due to differences in geometry and threshold voltages have already been discussed. The systematic offset results in a worst-case offset voltage of

$$V_{os,sys} = \frac{VDD}{A_{OL}} \text{ or } \frac{VSS}{A_{OL}} \tag{25.33}$$

The offset voltage of an op-amp is modeled as a DC voltage source in series with the noninverting input of an offset free op-amp. This is shown in Fig. 25.14a. The systematic offset is simulated by grounding the inverting input of the op-amp and sweeping the noninverting input. Simulation results for the op-amp of Fig. 25.11 are shown in Fig. 25.14b. The offset voltage is equal to the distance between the curve and the origin along the x-axis and in this case is approximately 0.1 mV. The slope of the transfer characteristics corresponds to the open-loop gain of the op-amp.

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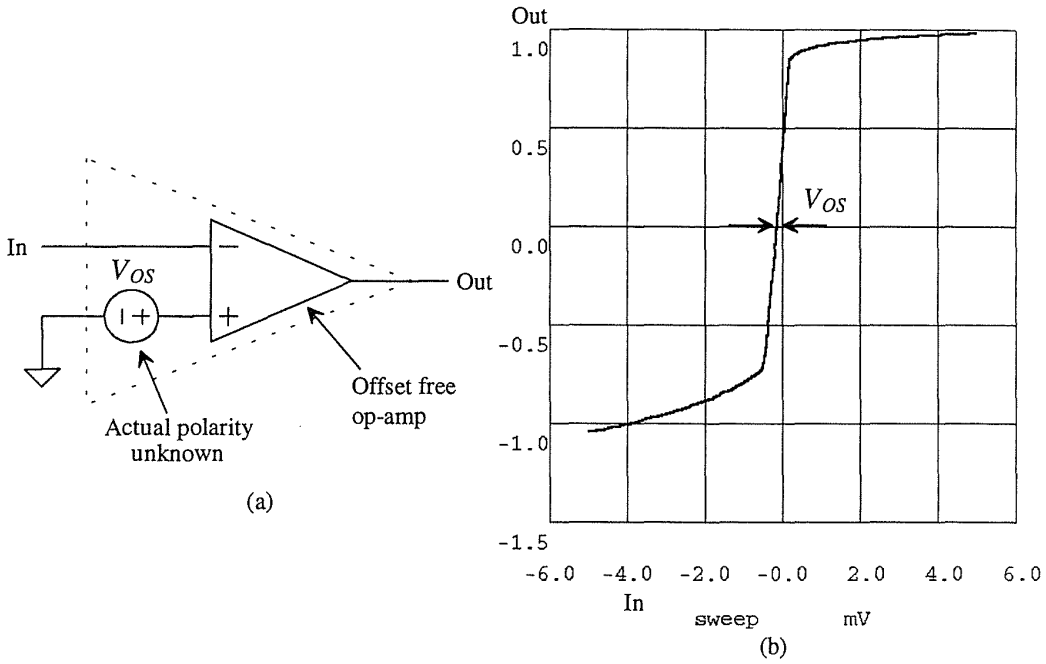


Figure 25.14 Simulation results of op-amp shown in Fig. 25.11 showing systematic offset.

Characterizing the Output Voltage Swing

The output voltage swing can be determined using Eqs. (25.4) through (25.7) for the class AB output stage of the op-amp shown in Fig. 25.11. The simulation results of 25.14b show that the output swing is approximately +/– 0.8 V. We are interested here in the range of outputs that are linearly related to the inputs. From this figure we see that input voltages of approximately +/– 0.5 mV on the input (neglecting the offset) result in an output voltage of $A_{OL}\cdot(v_{I2} - v_{I1})$.

Common Mode Rejection Ratio

The CMRR of an op-amp is calculated by multiplying the common-mode gain, A_c, of the input differential amplifier with the gain of the second stage and dividing the result into the open-loop gain A_{OL}. The CMRR of an op-amp in dB is given by

$$\text{CMRR} = 20\log\left(\frac{A_{OL}}{A_c A_2}\right) = 20\log\left(\frac{A_1}{A_c}\right) \qquad (25.34)$$

which shows that the op-amp CMRR is determined by the differential stage. Simulation of the CMRR can be performed with the circuits shown in Fig. 25.15. The CMRR is determined using Eq. (25.34) with the circuit outputs A_{OL} and $A_c\cdot A_2$. For the op-amp of Fig. 25.11, the CMRR is approximately 75 dB [from Eq. (24.35)] and the A_{OL}, from Fig. 25.12, is 72 dB. Knowing the CMRR and A_{OL}, we give the common-mode gain by

$$A_{cm} = (A_2 A_c)(\text{dB}) = A_{OL}(\text{dB}) - \text{CMRR(dB)} = 72 - 75 = -3 \text{ dB} = 0.707 \text{ V/V} \qquad (25.35)$$

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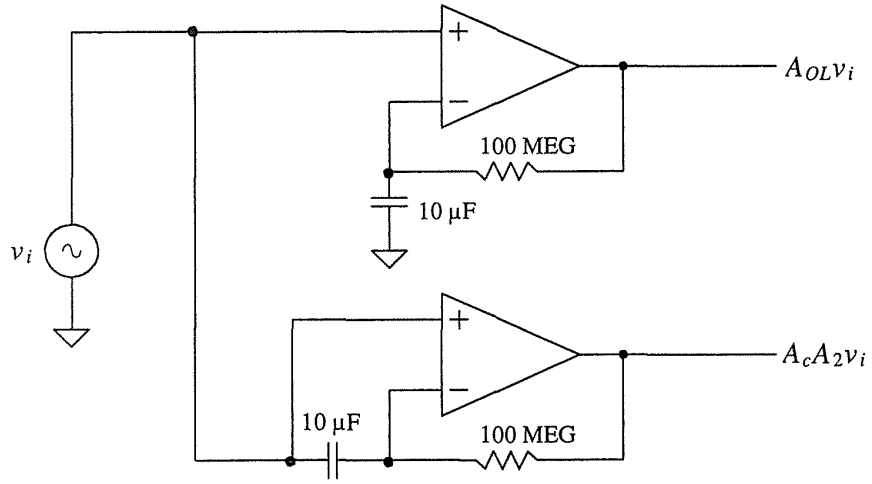


Figure 25.15 Circuit configuration used to simulate CMRR.

We can think of A_{cm} as the open-loop gain of the op-amp for common-mode signals. If the applied differential voltage is zero and we change the common-mode voltage by ΔV_c, then the output voltage will change by $\Delta V_o = A_{cm} \cdot \Delta V_c$. To compensate for the change in the output voltage, a nonzero input differential voltage develops on the input of the op-amp (an offset voltage that is a function of the common-mode voltage). This offset voltage can be estimated by

$$\Delta V_{OS} = \frac{\Delta V_o}{A_{OL}} = \frac{A_{cm}}{A_{OL}} \cdot \Delta V_c = \frac{\Delta V_c}{\text{CMRR}} \tag{25.36}$$

If we apply a 1 V common-mode signal to both inputs of the op-amp of Fig. 25.11, the offset voltage will change by 175 μV.

Power Dissipation

The power dissipated by an op-amp, P, is simply the product of the sum of the currents flowing in the current sources or sinks with the power supply voltages. For the op-amp of Fig. 25.11, $P = (VDD - VSS) \cdot (I_{D5} + I_{D6} + I_{D8} + I_{D10}) = 700\ \mu\text{W}$.

Power Supply Rejection Ratio

The power supply rejection ratio (PSRR) is a term used to describe how well an amplifier rejects noise or changes on the *VDD* and *VSS* power buses. This parameter can be extremely important in precision analog design. Consider the test setup shown in Fig. 25.16. The positive PSRR is defined by

$$\text{PSRR}^+ = \frac{A_{OL}}{v_{out}/v^+} \tag{25.37}$$

while the negative PSRR is defined by

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$$\text{PSRR}^- = \frac{A_{OL}}{v_{out}/v^-} \tag{25.38}$$

Let's begin by considering how the output voltage of the op-amp of Fig. 25.11 changes with changes on *VDD* (i.e., v^+). At relatively low frequencies, the compensation capacitor starts to effectively short the gate of M7 to its drain. At this point, we can think of M7 as a small-signal resistance of value $1/g_{m7}$. Since the resistance looking down into the drain of M91 is dominated by r_{o8} and $r_{o8} >> 1/g_{m7}$ almost all of v^+ is coupled to the output buffer and thus to the output of the op-amp. The gain from v^+ to v_{out} is plotted in Fig. 25.16c. For the negative PSRR, the effect of the coupling capacitor shorting the gate of M7 to its drain is to effectively short the drain of M8 to *VDD*. This causes the negative PSRR to increase with increasing frequency (see Fig. 25.16d). Because of the compensation scheme used, the PSRR of two-stage op-amps is poor. Discussed later in the chapter are a group of op-amps referred to as operational transconductance amplifiers (OTAs). These op-amps are one stage and are compensated by a load capacitance. In general, OTAs show much better PSRR than the two-stage variety discussed so far.

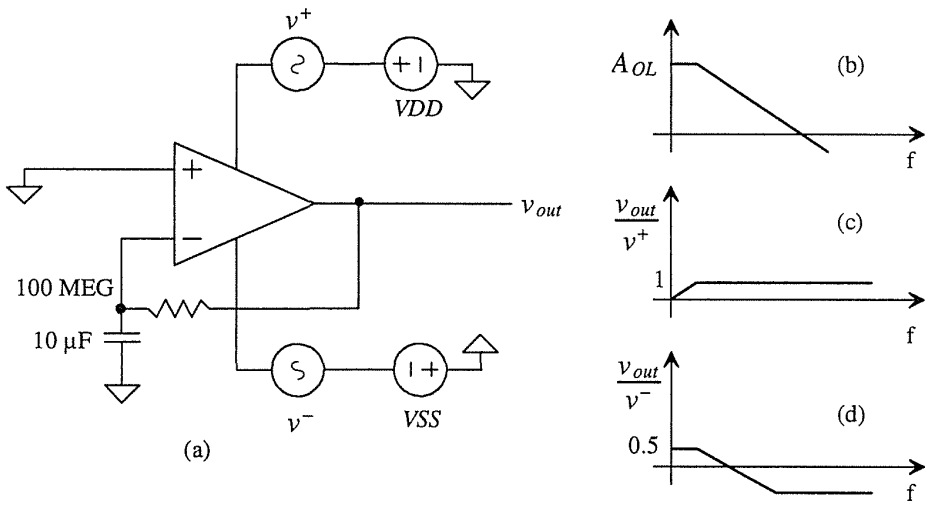


Figure 25.16 (a) Test setup to determine PSRR, (b) open-loop gain, (c) gain from AC signal on VDD to output, and (d) gain from AC signal on VSS to output.

Slew Rate

The slew-rate limitations of an op-amp built with the source coupled diff-amp is given by Eq. (25.23). The configuration shown in Fig. 25.17 is useful in measuring or simulating the slew-rate of an op-amp. For the op-amp of Fig. 25.11, the SR is 20 μA/8.75 pF or 2.25 V/μs. Normally, the slew-rate, overshoot, and settling time are specified for different loads. We will assume in the simulation of Fig. 25.11 that the op-amp is driving a 10 pF load (equivalent to a standard scope probe capacitance). The simulation results are shown in Fig. 25.18 for a 0 to 1 V step input into the follower. The simulation results and hand calculations are close.

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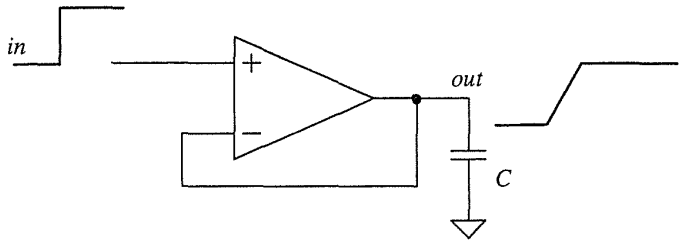


Figure 25.17 Circuit used to measure the slew rate of an op-amp.

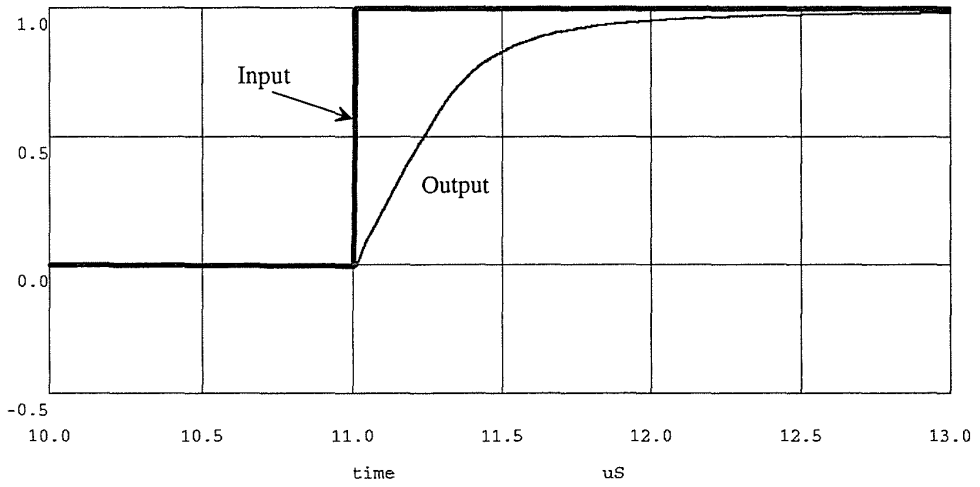


Figure 25.18 Slew-rate simulation results of the op-amp of Fig. 25.11 driving a 10 pF load.

If the SR is important in a particular application, the source cross-coupled configuration should be considered. An op-amp based on the sizes of Fig. 25.11 using the source cross-coupled pair is shown in Fig. 25.19. Again, as we discussed with the source coupled pair, the widths of M1/M2 and M3/M4 should be increased beyond 15 μm in practice. Increasing the widths has the effect of increasing the transconductance of the differential amplifier and thus increasing the gain of the op-amp.

25.1.2 Compensating the Op-Amp Without Buffer

The two-stage CMOS op-amp without output buffer is shown in Fig. 25.20. This configuration is useful as a comparator (without the compensation network included) or when the load is purely capacitive, a situation that occurs frequently when the op-amp is used on-chip in sampled data circuits. When compensating the two-stage op-amp, the load capacitance should be included with the calculation of C_2. Since the load capacitance affects the location of the second pole, it is possible that the compensated amplifier/load capacitance combination is unstable.

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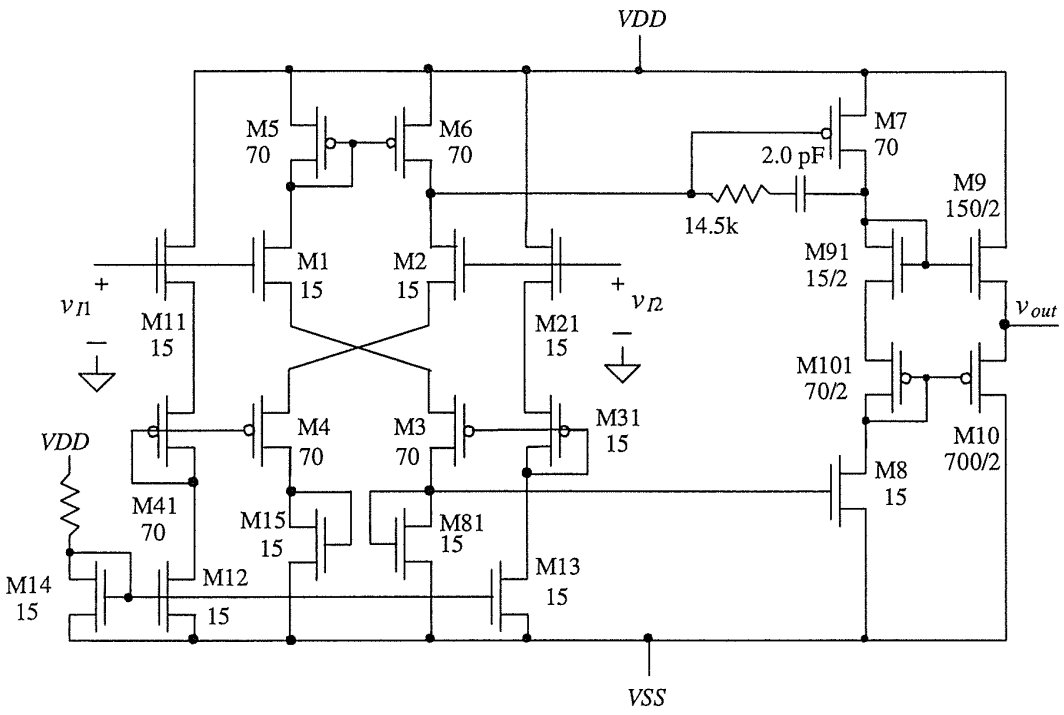


Figure 25.19 Op-amp without slew-rate limitations.

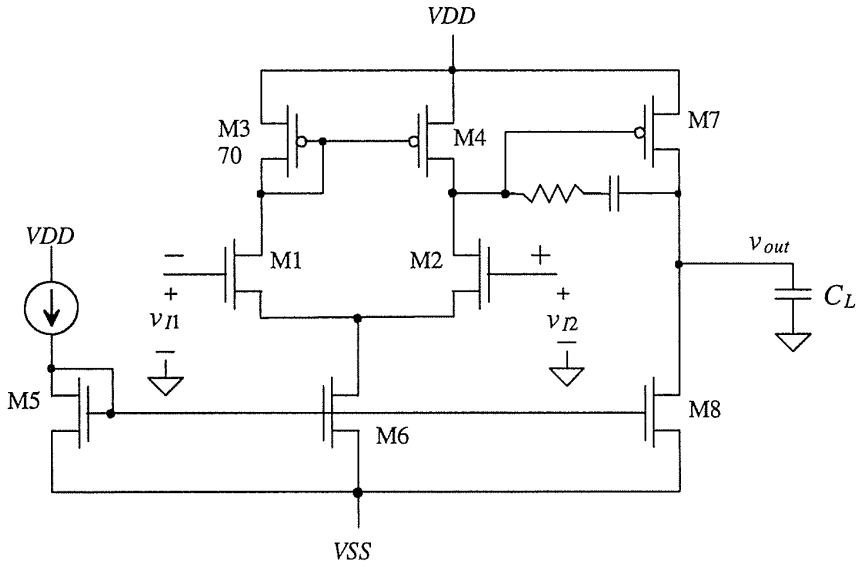


Figure 25.20 Two-stage op-amp without buffer.

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25.1.3 The Cascode Input Op-Amp

An unbuffered op-amp based on the cascode differential input stage is shown in Fig. 25.21. The cascode input stage is used to increase the overall open-loop gain of the op-amp. A source-follower stage consisting of M13 and M12 is used to provide a DC level shift between the output of the diff-amp and the output of the op-amp. This allows the output to swing up to *VDD* and down to *VSS*. The location of the first pole in this configuration is shifted lower in frequency due to the higher output resistance of the cascode configuration. Although the op-amp can have significantly higher gain than the basic current mirror configuration, the input common-mode range and CMRR are poorer. Because of the large gain of the first stage, this op-amp can be used without an output buffer. We must keep in mind that the output can source a current via M14 but is limited to sinking a current set by the size and biasing conditions of M15. One application of this amplifier is in a voltage regulator circuit where the op-amp is continuously sourcing a current to the load (keeping in mind the PSRR limitations).

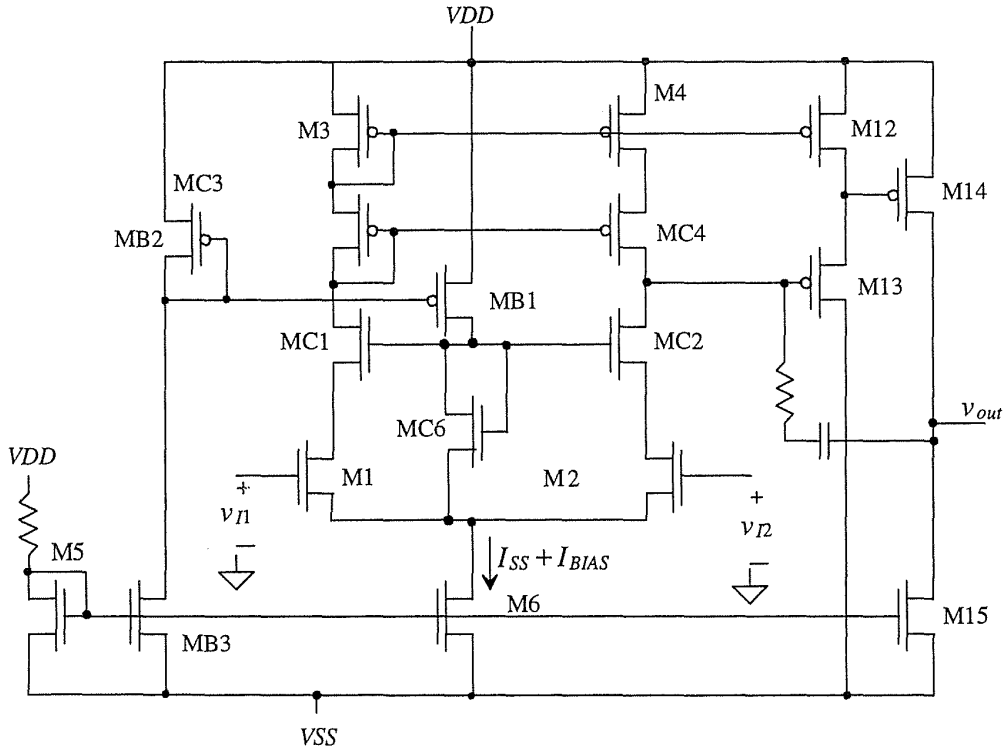


Figure 25.21 Unbuffered op-amp using a cascode differential amplifier.

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25.2 Operational Transconductance Amplifiers

The operational transconductance amplifier (OTA) is basically an op-amp without an output buffer. *An OTA without buffer can only drive capacitive loads.* An OTA can be defined as an amplifier where all nodes are low impedance except the input and output nodes. An example OTA is shown in Fig. 25.22. Note that the basic op-amp of Fig. 25.20 is not considered an OTA because the drain of M4 is a high-impedance node and not the input or output of the amplifier. Assuming that $\beta_1 = \beta_2$, $\beta_{31} = \beta_{41}$, we observe that the current i_{d31} or i_{d41} is given [see Eq. (24.12)] by

$$-i_{d31} = i_{d41} = \frac{g_{m1}}{2}(v_{I2} - v_{I1}) = i_d \tag{25.39}$$

Furthermore, if $\beta_4 = K{\cdot}\beta_{41} = K{\cdot}\beta_{31}$ and $\beta_{51} = \beta_5$, then $i_{d4} = -i_{d5} = K{\cdot}i_{d41} = -K{\cdot}i_{d31}$. If the impedance of the capacitor is large compared to $r_{o4}||r_{o5}$, then the output voltage of the OTA is given by

$$v_{out} = 2Ki_d(r_{o4}||r_{o5}) \tag{25.40}$$

and the voltage gain is

$$A_v = \frac{v_{out}}{v_{I2} - v_{I1}} = Kg_m(r_{o4}||r_{o5}) \tag{25.41}$$

where we have assigned the noninverting input of the OTA as the gate of M2. However, as the name states, we are interested in the transconductance (current out, voltage in) of the amplifier. If the impedance of the load capacitor or the resistance of

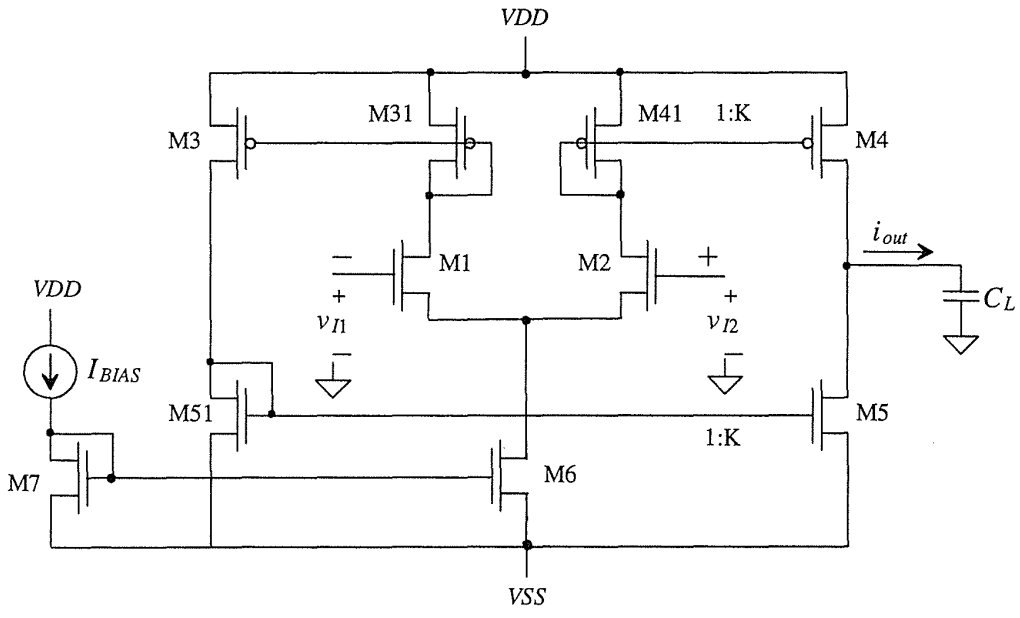


Figure 25.22 Basic configuration of an OTA.

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an external load is small compared to the output resistance, $r_{o4}||r_{o5}$, then the output current flows mainly in the external load. Under these circumstances, we can write the output current as

$$i_{out} = i_{d4} - i_{d5} = 2Ki_d \tag{25.42}$$

The transconductance of the OTA is given by

$$G_m = \frac{i_{out}}{v_{I2} - v_{I1}} = g_m K \tag{25.43}$$

In the following discussion, we will assume $K = 1$ so that $G_m = g_m$. In other words, the transconductance of the OTA is set by the transconductance of the input differential amplifier. A useful feature of the OTA is that its transconductance can be adjusted by the bias current. Filters made using the OTA can be tuned by changing the bias current labeled I_{BIAS} in Fig. 25.22. The symbol for the OTA is shown in Fig. 25.23.

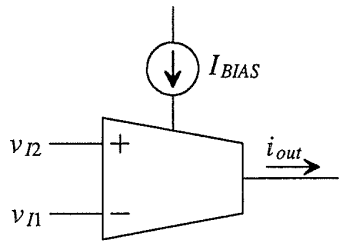


Figure 25.23 Schematic symbol of an OTA.

Example 25.1

Consider the OTA shown in Fig. 25.24. Determine I_{BIAS} and the transconductance of the OTA, g_m, as a function of $V_{control}$.

The bias current can be determined by realizing that the drain current of M10 and the drain current (and thus I_{BIAS}) of M8 are equal. The bias current can be written in terms of $V_{control}$ as

$$I_{BIAS} = \frac{V_{control} - V_{GS10}}{100\ \text{k}\Omega}$$

Since the W/L ratio of M10 is so large, we can assume $V_{GS10} \approx V_{THN} \approx 1\ V$. Using this result, I_{BIAS} varies from 0 to 15 μA for $V_{control}$, changing from 1 to 2.5 V, respectively. If $V_{control}$ is set to 2 V, then I_{BIAS} is 10 μA.

The transconductance of the OTA is given, keeping in mind I_{SS} (the drain current of M6) of the differential amplifier is $2I_{BIAS}$, by

$$g_m = \sqrt{2\beta I_{BIAS}} \tag{25.44}$$

or in terms of $V_{control}$

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$$g_m = \left[\frac{2\beta_1(V_{control}-1)}{100\ \text{k}\Omega}\right]^{1/2} = \left[\frac{2\cdot 50\frac{\mu\text{A}}{\text{V}^2}\cdot 15(V_{control}-1)}{100\ \text{k}\Omega\cdot 5}\right]^{1/2} \quad (25.45).$$

For $V_{control} = 2$ V, we get an OTA gain of $G_m = g_m = 55\ \mu\text{A/V}^2$. ■

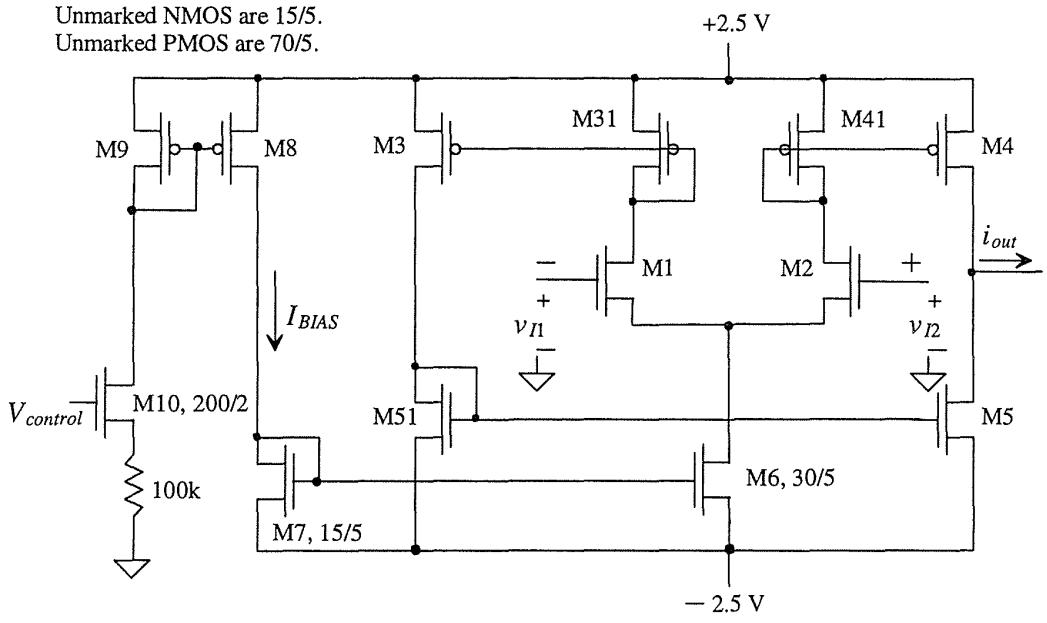


Figure 25.24 OTA of Ex. 25.1.

Example 25.2

Using the OTA of Fig. 25.24 with $V_{control}$ equal to 2 V ($I_{BIAS} = 10\ \mu$A), determine the transfer function, v_{out}/v_{in}, of the circuit shown in Fig. 25.25. Compare the hand calculations to a SPICE simulation.

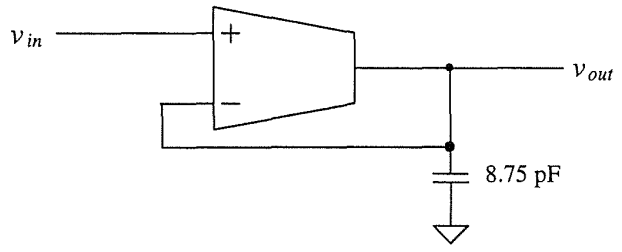


Figure 25.25 OTA circuit for Ex. 25.2.

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The current out of the OTA, i_{out}, is $g_m(v_{in} - v_{out})$. The output voltage is given by

$$v_{out} = i_{out} \cdot \frac{1}{j\omega C} = \frac{g_m}{j\omega C_L} \cdot (v_{in} - v_{out})$$

where C_L is the load capacitance, 8.75 pF in this case. The transfer function of the circuit is given by

$$\frac{v_{out}}{v_{in}} = \frac{1}{1 + j\omega\left(C_L \cdot \frac{1}{g_m}\right)} \tag{25.46}$$

The circuit of Fig. 25.25 performs the same function as a simple low-pass single-time constant filter with a capacitor value of C_L and a resistor value of $1/g_m$. The major advantage of this circuit is that the source, v_{in}, sees the input impedance of the OTA, which is practically infinite. The present circuit has a pole at a frequency of

$$f = \frac{1}{2\pi \cdot 8.75\text{p} \cdot \frac{1}{55\mu}} = 1 \text{ MHz}$$

The simulation results are shown in Fig. 25.26. An *important observation* we should make at this point is that increasing the load capacitance increases the phase margin of the OTA circuit (the dominant pole moves downward). ■

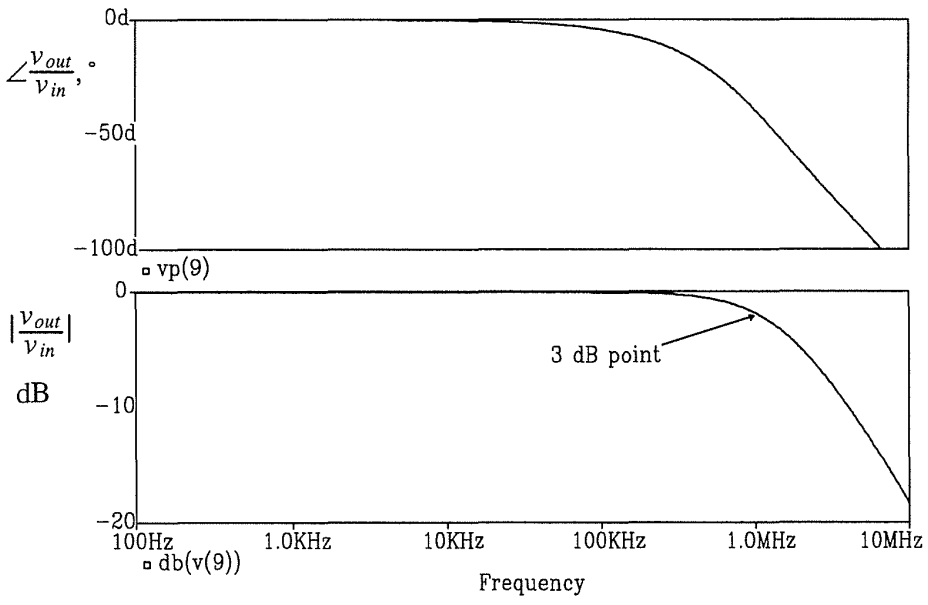


Figure 25.26 Phase/magnitude response of the OTA circuit of Fig. 25.25.

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A high-pass OTA circuit [4] is shown in Fig. 25.27. The transfer function of the circuit is given by

$$\frac{v_{out}}{v_{in}} = \frac{j\omega\left(C \cdot \frac{1}{g_m}\right)}{1 + j\omega\left(C \cdot \frac{1}{g_m}\right)} \tag{25.47}$$

Another name for the OTA-capacitor filter circuits of Figs. 25.25 and 25.27 is transconductor-C filters.

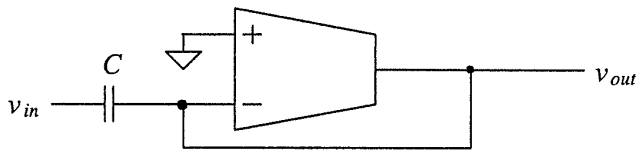


Figure 25.27 OTA circuit implementing a high-pass filter.

Two practical concerns when designing an OTA for filter applications are the input signal amplitude and the parasitic input/output capacitances. Large signals cause the OTA gain to become nonlinear. (An AC SPICE analysis does not reveal large-signal distortion.) The external capacitance should be large compared to the input/output parasitics of the OTA. This limits the maximum frequency of a filter built with an OTA and causes amplitude or phase errors. The errors can usually be tuned out with proper selection of I_{BIAS}.

Figure 25.28 shows a biquadratic (biquad for short) useful as a low-pass, high-pass, band-pass, or band-reject filter [4]. The input conditions and filter type are given in Table 25.1. If we assume that the transconductances of each stage are equal, then the natural frequency of the filter is given by

$$\omega_o = \frac{g_m}{\sqrt{C_1 C_2}} \tag{25.48}$$

while the Q of the filter is

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{25.49}$$

An ideal transconductance amplifier has infinite input and output resistances. The OTA of Fig. 25.23 has a modest output resistance. The output resistance of the OTA causes an error in the transfer function in filter applications. Increasing the output resistance is accomplished with the cascode OTA of Fig. 25.29. The transconductance of the amplifier is unchanged from the noncascode case. Adding the cascode MOSFETs has the effect of increasing the output resistance of the OTA while

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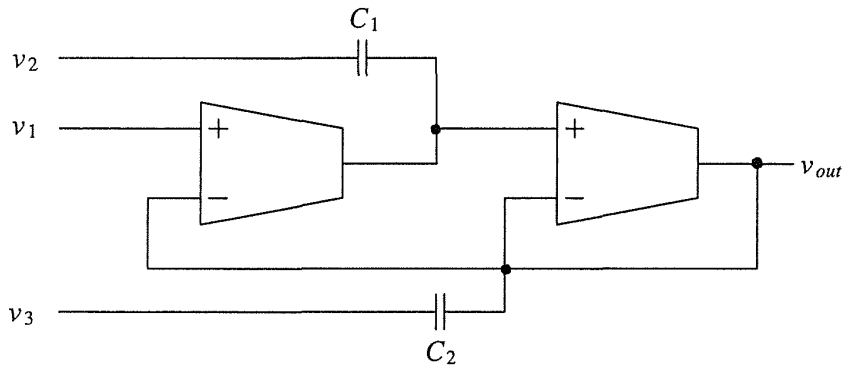


Figure 25.28 Biquad filter implementation using OTAs.

reducing the output swing. The MOSFET M9 is used to keep the drain of M3 at the same potential as the drain of M4 and thus eliminating errors due to channel length modulation. The bias voltages can be selected so that M4 and M5 are kept in the saturation region.

Filter Type		Input Conditions	Transfer Function
Low-pass		$v_{in} = v_1$, with v_2 and v_3 grounded	$\frac{g_m^2}{s^2C_1C_2 + sC_1g_m + g_m^2}$
High-pass		$v_{in} = v_3$, with v_1 and v_2 grounded	$\frac{s^2C_1C_2}{s^2C_1C_2 + sC_1g_m + g_m^2}$
Band-pass		$v_{in} = v_2$, with v_1 and v_3 grounded	$\frac{sC_1g_m}{s^2C_1C_2 + sC_1g_m + g_m^2}$
Band-reject		$v_{in} = v_1 = v_3$ with v_2 grounded	$\frac{s^2C_1C_2 + g_m^2}{s^2C_1C_2 + sC_1g_m + g_m^2}$

Table 25.1 Design equations for the Biquad filter.

25.2.1 Wide-Swing OTA

A wide-swing OTA first introduced in Ch. 24 is shown in Fig. 25.30 [5]. Wide swing here means that the input CMR is close to the supply voltages. Simulation results using the OTA are shown in Fig. 25.31 for an input voltage swing from zero up to +5 V. The output voltage swing of the OTA is limited by the supply voltages. The transconductance of the OTA (from Sec. 24.4) is $g_m = \sqrt{2\beta I} = \sqrt{2 \cdot \frac{20}{5} \cdot 50\frac{\mu A}{V^2} \cdot 1\ \mu A}$ $= 20\ \frac{\mu A}{V}$ for one diff-amp conducting and $40\ \frac{\mu A}{V}$ when both diff-amps are conducting. The unloaded low-frequency voltage gain of the OTA, again from Sec. 24.4, is 166 V/V independent of the number of diff-amps conducting current.

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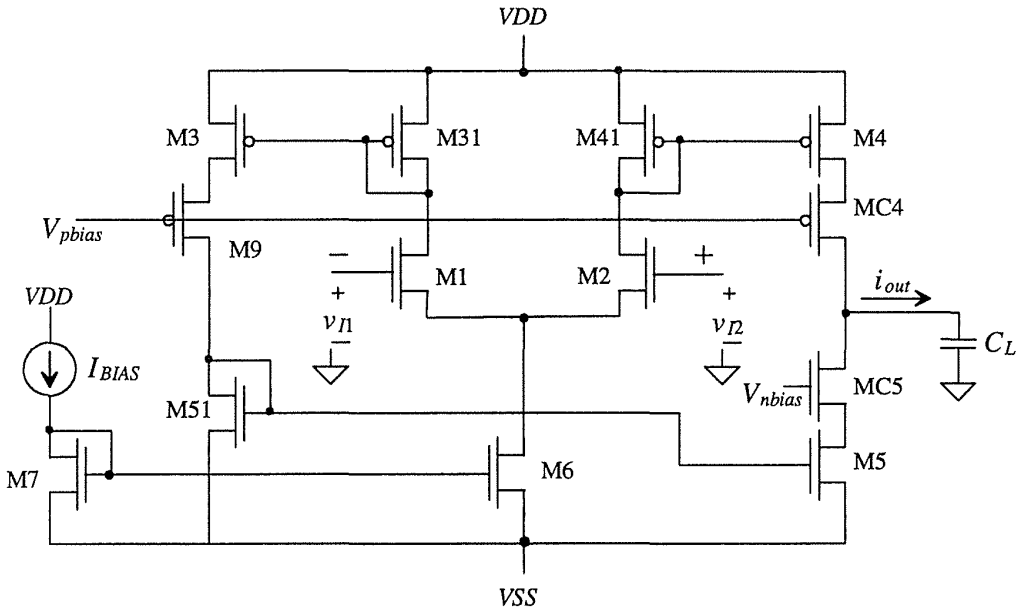


Figure 25.29 A cascode OTA.

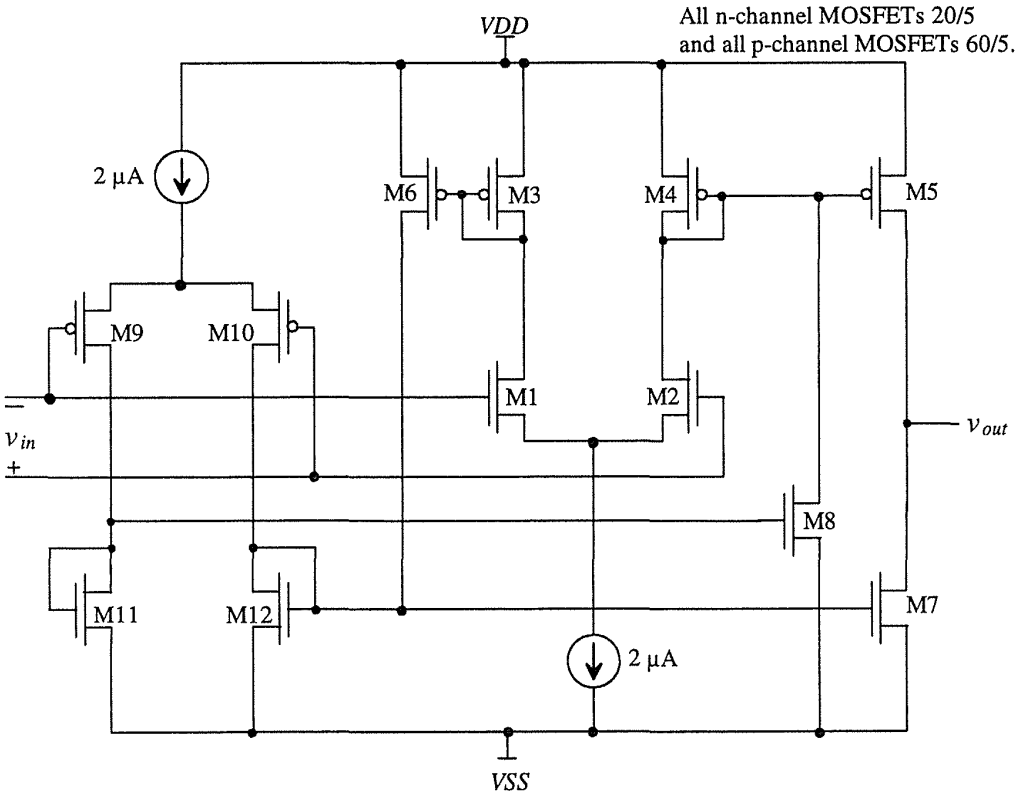


Figure 25.30 Wide-swing OTA first introduced in Ch. 24.

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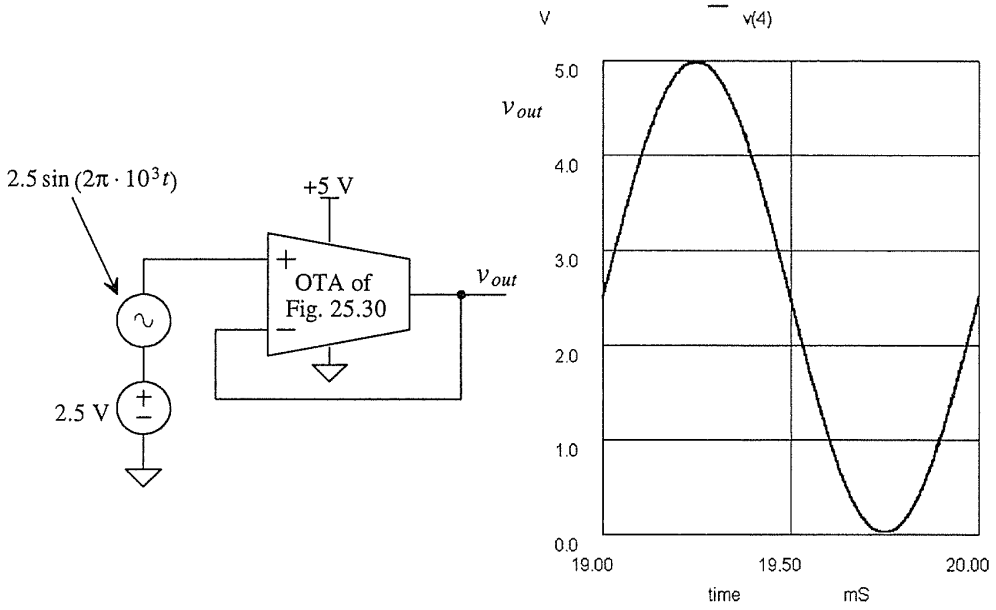


Figure 25.31 Simulation results (using BSIM model) of the OTA of Fig. 25.30 with VDD = +5 V and VSS = 0.

A circuit that operates in triode, saturation, or cutoff, such as the OTA of Fig. 25.30, is very difficult to simulate using SPICE. Using the level 2 model helps with convergence at the price of accuracy. For example, simulating the OTA of Fig. 25.30 using the level 2 model resulted in an open-loop gain of approximately 18, while using the BSIM model resulted in a voltage gain of 240. This result makes it clear that the level 2 model is useful only in functional testing, verifying that the circuit is connected correctly in the simulation. In order to achieve convergence using the BSIM model, the simulation included the .OPTIONS statement with RELTOL = 0.1, ABSTOL = 0.1u, and VNTOL = 50 mV. Simulating the circuit using AC analysis and achieving convergence are considerably easier than a DC sweep or transient analysis. An AC analysis begins by calculating the operating point. (This is the difficult part of the AC simulation.) This is followed by replacing the active devices with small-signal models.

Before we discuss the AC analysis of the OTA circuit of Fig. 25.30 to determine stability, we should discuss compensating OTAs. The closed-loop gain of an OTA circuit is given by

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL} \cdot \beta} \tag{25.50}$$

The maximum value of the feedback factor, β, without an amplifier in the feedback loop is unity, that is, all of the output voltage is fed back and subtracted from the input. Setting the feedback factor to unity follows the same procedure used in Sec. 25.1 [see Eqs. (25.12) and (25.13)] to determine the gain and phase margins of the op-amp. An

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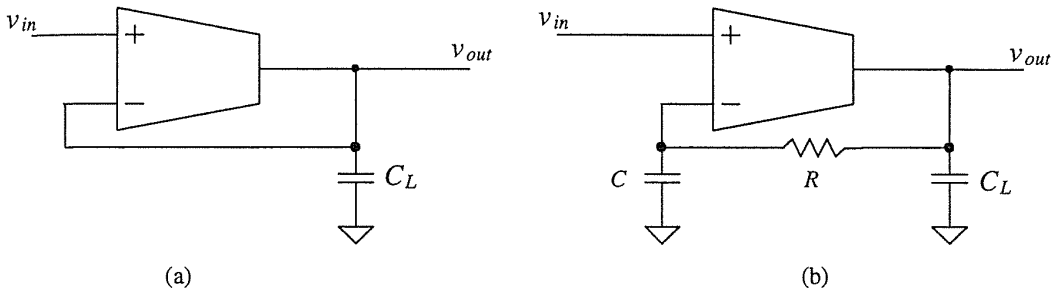


Figure 25.32 OTA circuit with (a) unity feedback factor and (b) DC stability.

OTA with a unity feedback factor is shown in Fig. 25.32a while Fig. 25.32b shows the configuration used to determine the open-loop gain of the OTA. The resistor/capacitor combination helps stabilize the DC output voltage of the OTA, ensuring that the MOSFETs used in the OTA operate in the saturation region. The feedback resistor should be much larger than the output resistance of the OTA, and the *RC* product should be much longer than the reciprocal of the lowest frequency of interest. This is equivalent to stating that *R* and *C* of Fig. 25.32b should have no effect on the AC performance of the circuit. If we assume that the impedance of the load capacitor is small compared to the output impedance of the OTA, then we can write

$$v_{out} = i_{out} \cdot \frac{1}{j\omega C_L} = g_m v_{in} \cdot \frac{1}{j\omega C_L} \tag{25.51}$$

or

$$\frac{v_{out}}{v_{in}} = \frac{g_m}{j\omega C_L} \Rightarrow \left|\frac{v_{out}}{v_{in}}\right| = \frac{g_m}{2\pi f C_L} \tag{25.52}$$

When determining the phase margin, we are interested in the frequency at which the magnitude of v_{out}/v_{in} is unity. Using Eq. (25.52) and labeling the frequency at which the magnitude of v_{out}/v_{in} is unity, f_u, we get

$$f_u = \frac{g_m}{2\pi C_L} \tag{25.53}$$

It would appear that the OTA (for feedback factors of unity or less) is always stable. Indeed, this is the case, provided the impedance of C_L is small compared to the output impedance of the OTA and the parasitic poles are at a much higher frequency than f_u.

The open-loop gain and phase responses of the OTA of Fig. 25.30 can be simulated using the test circuit shown in Fig. 25.33 (with $C_L = 0$). Figure 25.34 shows the simulation results with $V_{CM} = 2.5$ V. The unity gain frequency, f_u, is 60 MHz, while the phase at f_u is 150°, a 30° phase margin. An interesting observation can be made if V_{CM} is set to 0.5 V and then 4.5 V. These values of V_{CM} correspond to situations where the n- and p-channel diff-amps are not conducting. Under these conditions, the small-signal transconductance of the OTA is half of the value when both diff-amps are

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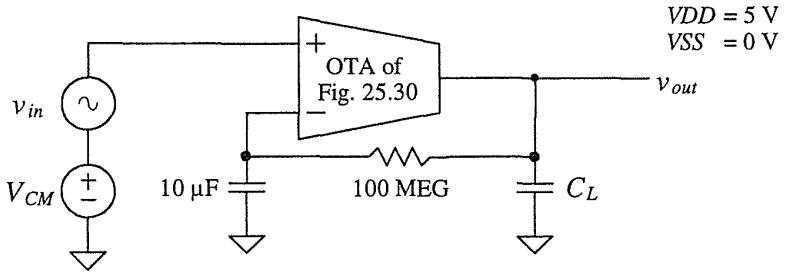


Figure 25.33 OTA circuit used to determine open-loop characteristics of OTA of Fig. 25.30.

on. The result is a shift in the unity gain frequency of the OTA, while the low-frequency gain of the OTA is unchanged, as discussed in Ch. 24. The unity gain frequency, f_u, with V_{CM} set at 0.5 or 4.5, is approximately 30 MHz; see Fig. 25.35 for the case $V_{CM} = 0.5$ V.

Compensating the OTA is simply a matter of selecting a minimum load capacitance. Increasing the load capacitance actually increases the phase margin of the OTA. Looking at the phase characteristics of the OTA in Fig. 25.34 (without a load), we see that adding and increasing the load capacitance shifts the point where the phase is –45° to a lower frequency. (Increasing the load capacitance lowers the first pole in the transfer function.) The point where the phase is –100° remains essentially

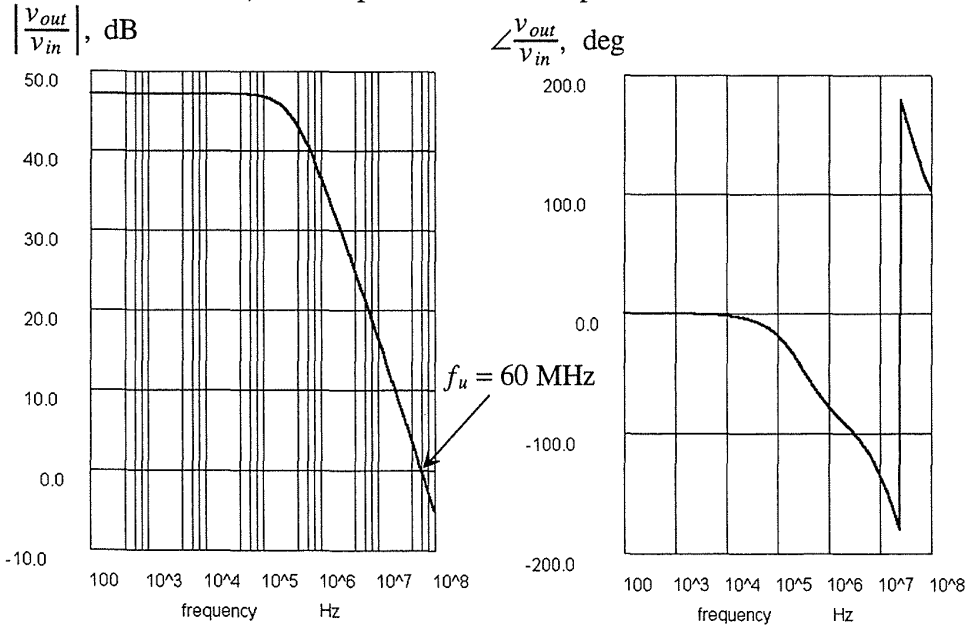


Figure 25.34 Open-loop simulation results of the OTA in Fig. 25.30 using the setup of Fig. 25.33 with $C_L = 0$ and $V_{CM} = 2.5$ V (both diff-amps on).

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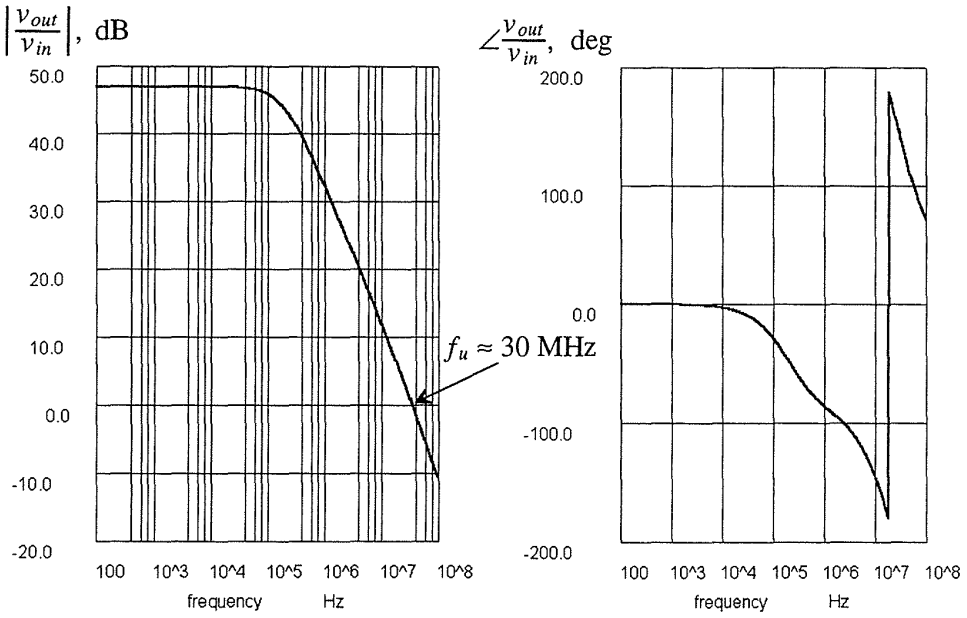


Figure 25.35 Open-loop simulation results of the OTA in Fig. 25.30 using the setup of Fig. 25.33 with $C_L = 0$ and $V_{CM} = 0.5$ V (p-channel diff-amp on).

unchanged since the other parasitic poles are not affected by the load capacitance. The frequency at a phase of −100° is approximately 3 MHz. If we set f_u = 3 MHz, then the phase margin is 80° (assuming no interaction from the other parasitic poles present in the circuit). From the beginning of the section, the transconductance of the OTA is 40 μA/V². Using Eq. (25.53) results in a minimum-load capacitance of 2.1 pF. Simulation results using C_L = 2.1 pF are shown in Fig. 25.36. The simulation results show f_u = 2.4 MHz and a phase margin of 70°. The difference between the hand calculations and the simulation results can be attributed to the parasitic poles present in the OTA. The parasitic poles present in any CMOS analog amplifier ultimately limit the complexity of the circuit. In practice, a minimum-load capacitance greater than 2.1 pF would be used. A possible practical load capacitance minimum of 5 pF would be appropriate in this design.

The OTA with Buffer

An op-amp can be made using an OTA with buffer circuit. The buffer is used to isolate the OTA from the load. The load can be resistive, capacitive, or a combination of the two. Compensating the OTA/buffer is somewhat different from compensating the OTA alone. Consider the OTA/buffer shown in Fig. 25.37. The buffer used in this figure is a source follower. To begin, let's try to compensate the op-amp by putting a load capacitance on the output of the source follower. This is similar to what we did for the OTA alone. Now, however, the output of the amplifier is a low impedance, that is, the output impedance of the source follower. Therefore, the load capacitance should have little effect on the phase margin of the amplifier. For the cases of very large load

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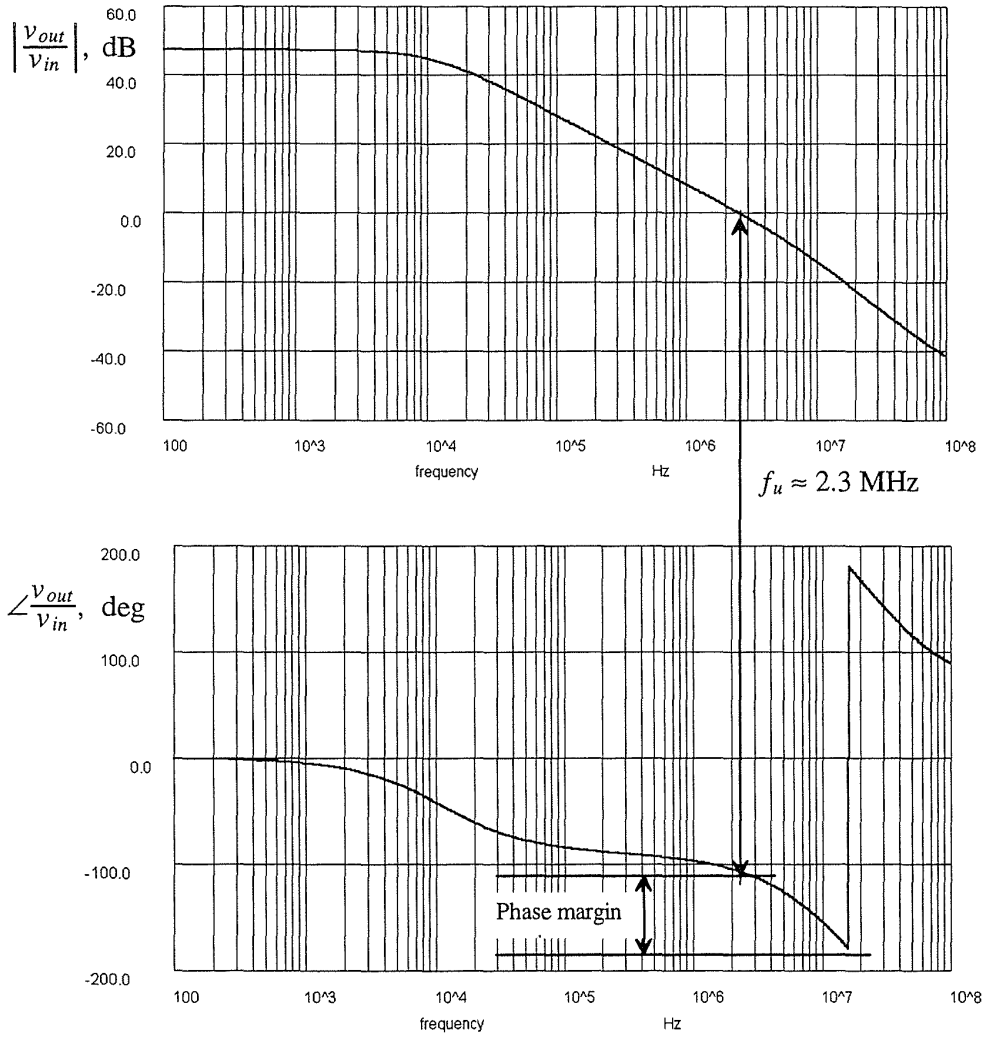


Figure 25.36 Compensating the OTA of Fig. 25.30 with a 2.1 pF cap.

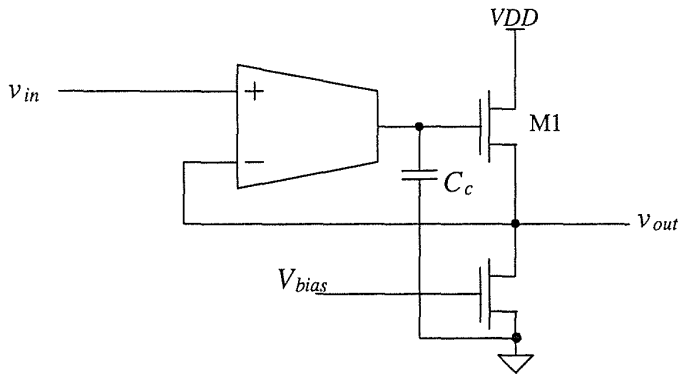


Figure 25.37 OTA with source-follower buffer (an op-amp).

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capacitances or a very small source follower, the load capacitance may indeed affect the phase margin of the amplifier. Normally, however, the buffer is designed so that it can easily source and sink (by making the value of the current source load used in the source follower large) the current needed to drive the load capacitance.

Next, we could try to compensate the amplifier using the input capacitance of the source follower. One might try to use the gate-source capacitance of M1 as the compensation capacitance on the output of the OTA. Ideally, however, the output voltage of the OTA and the output voltage of the source follower are the same, that is, the source follower has a voltage gain of +1. This means that the voltage on each side of the gate-source capacitance changes at the same rate. In other words, the AC voltage between the gate and source of M1, v_{gs1}, is zero (ideally). This means that zero displacement current flows through C_{gs1}, and therefore it cannot be used for compensation. The gate-drain capacitance of M1 can be used for compensation since it is connected directly to AC ground (*VDD*). Using C_{gd1} would require, for a practical value of compensation capacitance, M1 to be too large for most situations.

This discussion shows that the op-amp of Fig. 25.37 should be compensated with a capacitance from the output of the OTA to ground. The value of the compensation capacitor C_c is selected following the procedures of the last section. Notice that even though there is an amplifier in the feedback loop, the maximum value of the feedback factor, β, is still 1. This is because the amplifier has a voltage gain of unity.

Next consider the OTA/buffer shown in Fig. 25.38. This configuration is useful in voltage regulator design since the output can swing all the way up to *VDD*. With the use of feedback resistors, the gain of the circuit can be set to a multiple of the input voltage. Also, in this configuration β can be larger than one since there is an amplifier, M1, in the feedback loop. Since the amplifier is inverting (M1), the signal fed back is connected to the "+" input of the OTA.

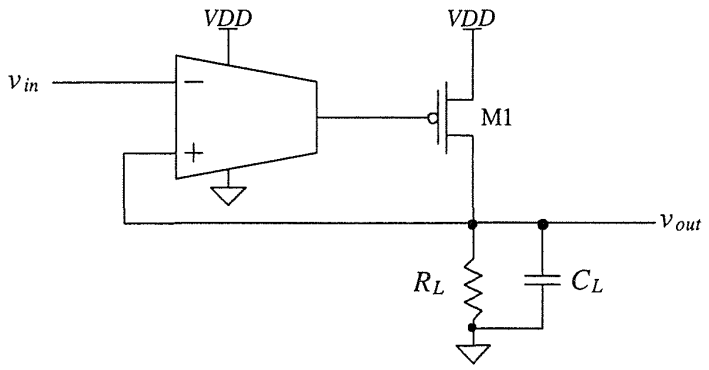


Figure 25.38 Op-amp made using the OTA/common-source amplifier.

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This circuit is basically a two-stage op-amp and can be compensated in the same way as the op-amp of Fig. 25.11. A problem exists, however, if the load capacitance is too large. Consider the following example.

Example 25.3

The circuit shown in Fig. 25.39 is used as a voltage regulator that generates an output voltage of 2.5 V with a maximum output current of 10 mA (into R_L) over *VDD* changes of 4 to 6 V. Design the circuit (select R_z, R_{min}, and C_c) so that the phase margin is approximately 90° when $C_L = 0$. Estimate the maximum C_L allowed so that the phase margin of the circuit remains greater than 45°.

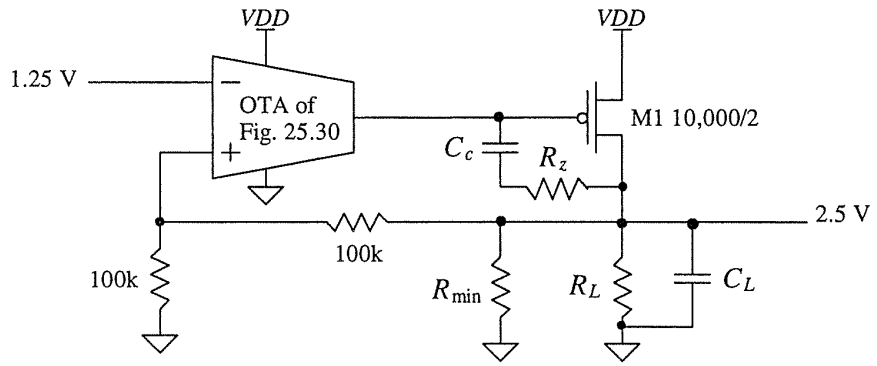


Figure 25.39 Voltage regulator of Ex. 25.3. Note to simulate a circuit with a large MOSFET set NRD and NRS to zero.

The solution to this example begins by following the compensation procedure given in Sec. 25.1. The value of R_1 (which is the output resistance of the OTA) is given by

$$R_1 = r_{o5} || r_{o7} = 4.2 \text{ MEG for } \lambda = 0.06 \text{ V}^{-1} \text{ and } I = 2 \text{ μA}$$

The value of C_1, since M1 is large compared to output capacitance of the OTA, is given by

$$C_1 = C_{gs1} + C_{gd1}(1 + |A_{v2}|) =$$

$$\frac{2}{3} \cdot (10,000)(2)(800 \text{ aF}) + (10,000 \text{ μm})\left(5 \times 10^{-10} \frac{\text{F}}{\text{m}}\right)(1 + |A_{v2}|) =$$

$$C_1 = 10.67 \text{ pF} + 5 \text{ pF} \cdot (1 + |A_{v2}|)$$

The location of the pole on the output of the OTA, before adding the compensation capacitor, is given by

$$f_1 = \frac{1}{2\pi \cdot R_1 C_1} = \frac{1}{2\pi \cdot 4.2 \text{ MEG} \cdot [10.67 + 5(1 + |A_{v2}|)]\text{pF}}$$

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The location of the pole on the output of M1, prior to adding the compensation network, is given by

$$f_2 = \frac{1}{2\pi \cdot R_2 C_2} = \frac{1}{2\pi \cdot (r_{o1} || R_L || R_{\min})\left[C_L + 5\text{ pF}(1 + \frac{1}{|A_{v2}|}) \right]}$$

The reason for adding R_{min} to the circuit will now be explained. If the regulator output current starts to decrease toward zero (i.e., R_L and r_{o1} move toward ∞), then M1 will start to turn off. This in turn pushes f_2 down in frequency toward f_1 (f_1 decreases also up to a point since A_{v2} increases with decreasing output current, see Fig. 22.15). At very low output currents, f_2 can be less than f_1. The result is an unstable feedback loop. Adding R_{min} to the regulator ensures that M1 is always sourcing at least some minimum current. For the present design, with an output voltage of 2.5 V, R_{min} will be set to 10 kΩ.[2] This forces M1 to source a minimum of 250 μA at any given time. If the regulator output current, I_{D1}, increases, then f_2 increases for a constant C_L, increasing the phase margin of the circuit. For this reason, in the remainder of the discussion, we will assume I_{D1} = 250 μA (the worst-case situation) so that

$$r_{o1} = \frac{1}{0.8 \cdot 250\ \mu\text{A}} = 5\ \text{k}\Omega \text{ and } R_L = \infty$$

where λ = 0.8 for M1 with a channel length of 2 μm. The second stage gain is then

$$|A_{v2}| = g_{m2} \cdot (r_{o1} || 10\ \text{k}\Omega) = \sqrt{2 \cdot 17\frac{\mu\text{A}}{\text{V}^2} \cdot \frac{10{,}000}{2} \cdot 250\mu\text{A}} \cdot (5\ \text{k} || 10\text{k})$$

$$= 21.7\ \text{V/V}$$

where g_{m2} is the transconductance of the second-stage (M1's transconductance). The location of f_1, using this gain, is 300 Hz, while f_2 is given by

$$f_2 = \frac{1}{2\pi \cdot (5\ \text{k} || 10\ \text{k})\left[C_L + 5\text{ pF}(1 + \frac{1}{|21.7|}) \right]} = \frac{1}{2\pi \cdot (3.3\ \text{k}\Omega)(C_L + 5\text{ pF})}$$

Adding the Compensation Capacitor

We cannot use Eq. (25.18) to determine the unity gain frequency of the loop since C_c will not be much larger than C_1. We can, however, write the open-loop gain (with the compensation capacitor) of the circuit (where g_{m1} is the transconductance of the OTA) as

$$\frac{v_{out}}{v_{in}} = \frac{\overbrace{g_{m1} \cdot R_1}^{\text{OTA gain}} \cdot \overbrace{21.7}^{\text{M1's gain}}}{\left(1 + j\frac{f}{f_{1C}}\right)\left(1 + j\frac{f}{f_{2C}}\right)}$$

[2] This value of resistor may be too small for most practical situations.

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where f_{1C} and f_{2C} are the frequencies of the two poles with the compensation capacitor added. Since f_{1C} (the dominant pole) is much less than f_{2C}, we can rewrite this equation for frequencies less than f_{2C} as

$$\left|\frac{v_{out}}{v_{in}}\right| \approx \frac{g_{m1}R_1 \cdot 21.7}{\sqrt{1+\left(\frac{f}{f_{1C}}\right)^2}} = \frac{3,650}{\sqrt{1+\left(\frac{f}{f_{1C}}\right)^2}}$$

By definition, when $f = f_u$, $|v_{out}/v_{in}| = 1$. Since f_u is much larger than f_{1C}, this equation can be rewritten as

$$f_u = f_{1C} \cdot 3,650 = f_{1C} \cdot A_{v1} \cdot A_{v2}$$

The location of the poles with compensation capacitor are given by

$$f_{1C} = \frac{1}{2\pi \cdot 4.2MEG \cdot [10.7 + (5 + C_c)(1 + 21.7)]} = \frac{1}{2\pi \cdot 4.2MEG \cdot [125\ \text{pF} + C_c(1 + 21.7)]}$$

and

$$f_{2C} = \frac{1}{2\pi \cdot 3.3\ \text{k}\Omega \cdot (C_L + C_c + 5\ \text{pF})} \qquad (25.54)$$

From the design requirements given earlier, the phase margin should be approximately 90° when $C_L = 0$. This can be met if f_{2C} (with $C_L = 0$) is ten times f_u, that is, $f_{2C} > 10 \cdot f_u$. If we set $f_u = 100$ kHz then $C_c = 55$ pF and $f_{2C} = 800$ kHz. The value of f_{2C} is only eight times larger than f_u. However, this value is very dependent on the value of λ when I_{D1} is small. Since our selection of λ, for M1 (0.8), may not be exact, we will simulate the circuit and verify that the design meets the given criteria.

The value of R_z can be picked based on the maximum g_m (g_{m2}) of M1. This occurs when $I_{D1} = 10$ mA or $g_{m2} = 41.23$ mA/V. If we set $R_z = 1/g_{m2}$ then $R_z = 25\ \Omega$. In order to increase the phase margin of the regulator, we will set $R_z = 100\ \Omega$ in this design. Note that R_z has little effect on the phase margin when the regulator is sourcing small amounts of current. Open-loop simulation results with $C_c = 55$ pF, $R_{min} = 10$ kΩ, $R_L = \infty$, and $C_L = 0$ are shown in Fig. 25.40. The common mode input voltage was set to 2.5 V in this open-loop simulation, and DC stability circuitry was used (see Fig. 25.33).

The unity gain frequency shown in this simulation matches the hand calculations. However, the second pole is about five times larger than the 800 kHz we calculated (this is good). Also, the right-hand plane zero appears to be located very close to the second pole. This causes the phase to decrease twice as fast. The phase margin under these circumstances meets the design criteria (i.e. 90°), when $C_L = 0$. A phase margin of 45° occurs when $f_{1C} = f_u$. Using Eq. (25.54) with $f_{1C} = 100$ kHz results in $C_L = 420$ pF. Simulation results showed that a capacitor five times this value, or 2100 pF, caused the phase margin to become 45° (with $I_{D1} = 250\ \mu$A). Increasing I_{D1} increases the phase margin. ■

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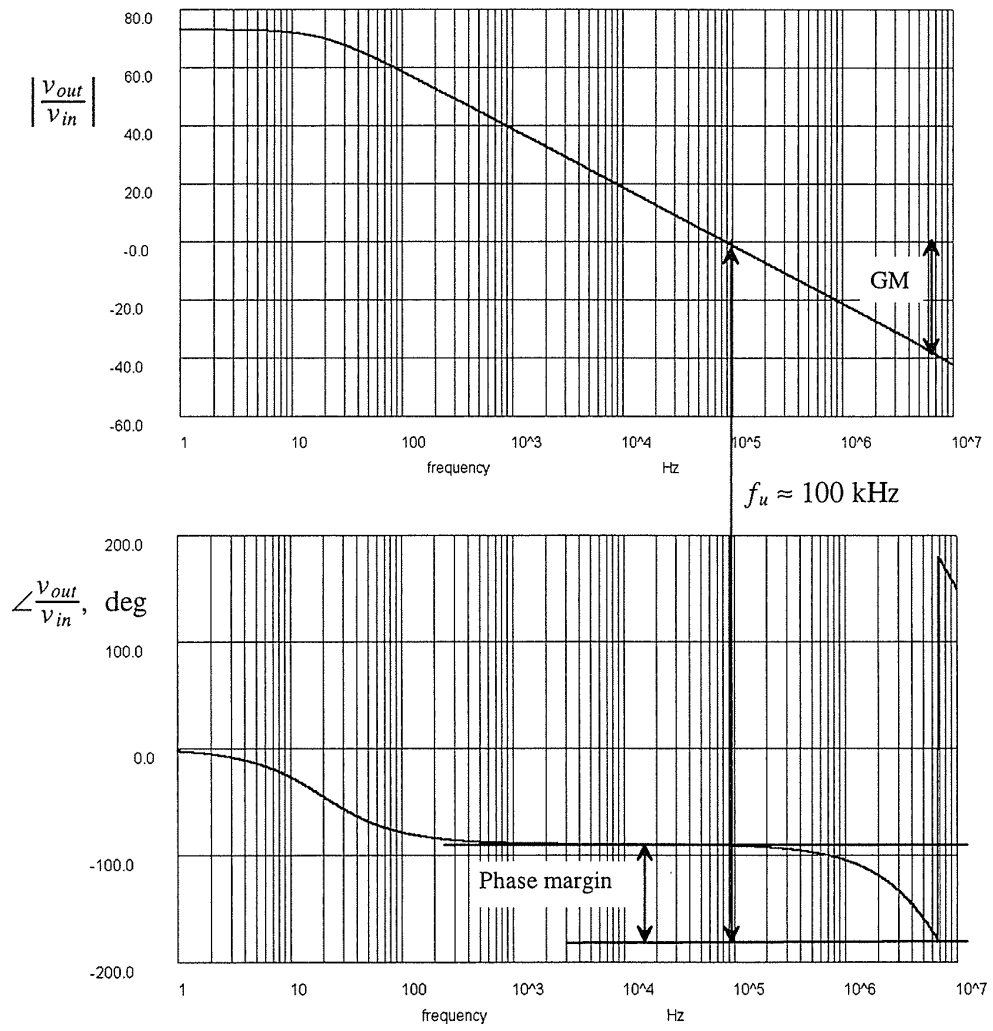


Figure 25.40 Open-loop frequency response for Ex. 25.3 (see text).

A final example of a wide-swing OTA with buffer is shown in Fig. 25.41. This is the OTA of Fig. 25.30, with four MOSFETs added to form an output stage. MOSFETs M13 and M14 can be thought of as "zero canceling resistors" used to shift the right-hand plane zero into the left-hand plane. M13 and M14 also help to reduce the current flowing in M15 and M16. We know that the current through M13 and M14 is well defined. The current through M15 and M16 is less well defined. Increasing the lengths of M13 and M14 helps to reduce the quiescent current in M15 and M16 and push the zero further into the left-half plane.

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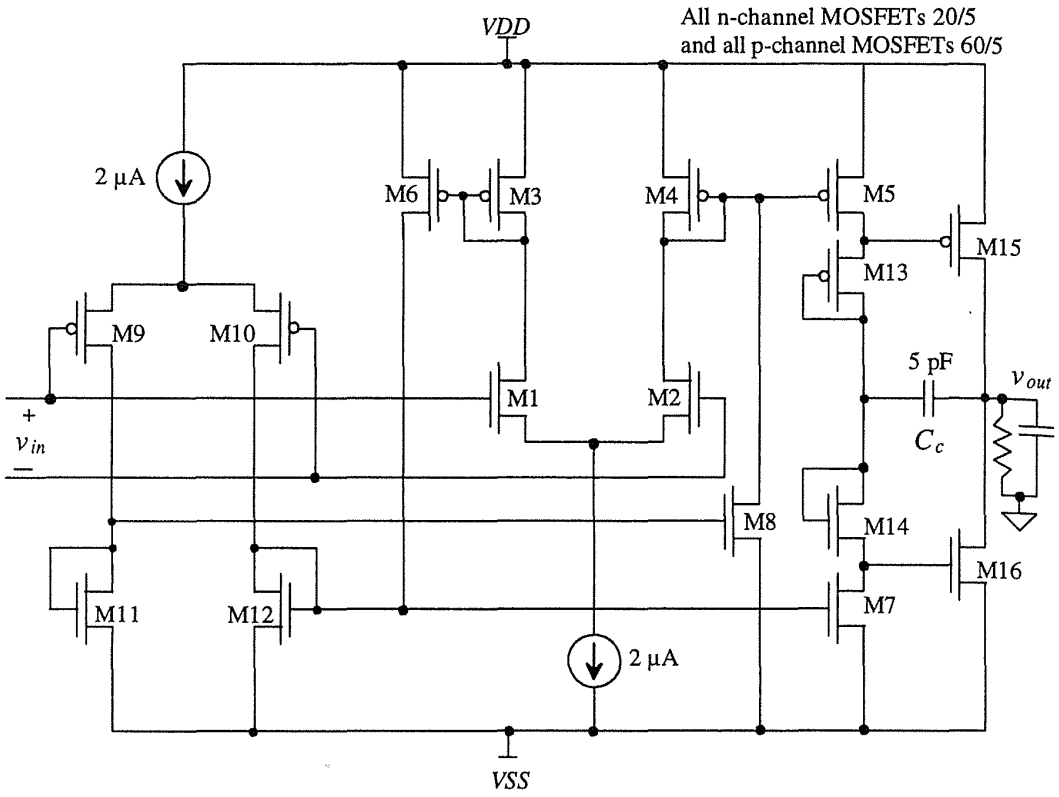


Figure 25.41 Wide-swing OTA with common-source output buffer.

The unity gain frequency of an OTA, f_u, is a strong function of the load capacitance. For the op-amp of Fig. 25.41, the unity gain frequency and the DC gain of the op-amp are a strong function of the load resistance and capacitance. This is due to the fact that the output stage has a gain greater than one. The resistor on the output of the op-amp affects the second-stage gain. The compensation capacitor is selected in the same manner as the OTA without output buffer, assuming the second stage has a gain of one. If the second-stage has a gain greater than one, then the Miller effect multiplies C_c by the second stage gain. This effectively increases the capacitance seen by the first stage, keeping the op-amp compensated. Again, the op-amp can become unstable, as we saw in Ex. 25.3, when the load capacitance becomes too large. Note that because the output buffer is inverting, the "+" and "–" inputs of the op-amp are switched.

25.2.2 The Folded-Cascode OTA

The folded-cascode OTA is shown in Fig. 25.42 [6-8]. The name "folded-cascode" comes from folding down p-channel cascode active loads of a diff-pair and changing the MOSFETs to n-channels. This OTA, like all OTAs, has good PSRR compared to the two-stage op-amp since the OTA is compensated with the load capacitance.

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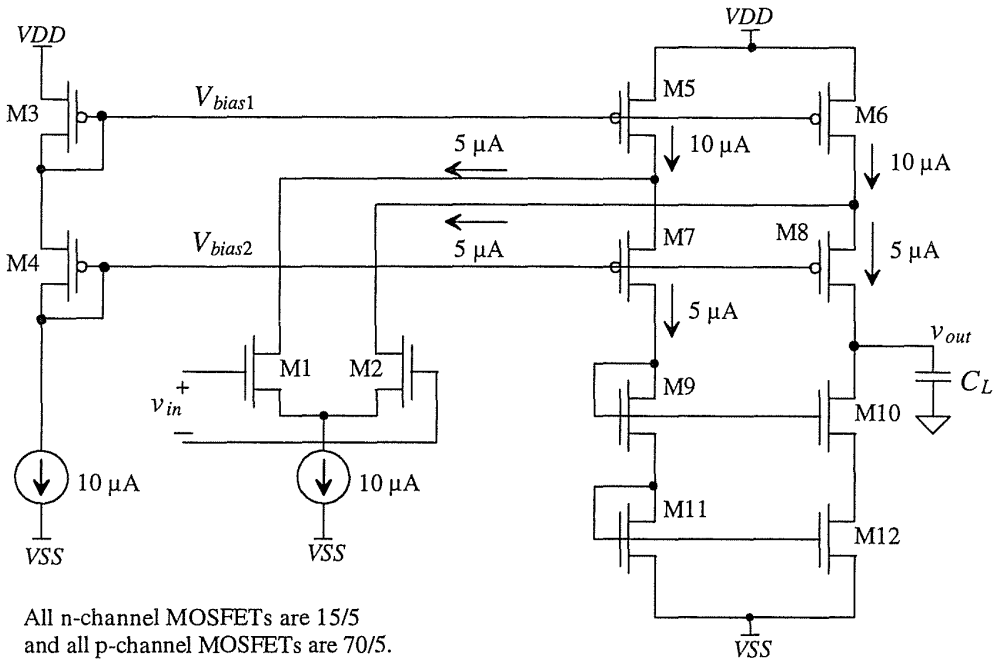


Figure 25.42 Folded-cascode OTA.

To understand the operation of the folded-cascode OTA, consider Fig. 25.42 without the diff-amp (M1/M2) in the circuit. Without the diff-amp present in the circuit, 10 μA flows in all MOSFETs. MOSFETs M3 and M4 provide the DC bias voltages to M5-M8. Note that the cascoded MOSFETs (M5-M12) are not biased for wide-swing operation. A wide-swing biasing circuit could replace M3/M4, and M9-M12 could be replaced with a wide-swing current mirror. Biasing for wide-swing operation increases the output voltage swing. When the diff-amp is added back into the circuit, it steals 5 μA from M7-M12, reducing their drain currents to 5 μA.

Applying an AC input voltage, v_{in}, causes the diff-amp differential drain current to become $g_m v_{in}$ (g_m is the transconductance of the diff-amp). This AC differential drain current is mirrored in the cascoded MOSFETs M7 through M12. The output voltage of the OTA is then

$$v_{out} = g_m v_{in} \cdot R_o \tag{25.55}$$

where

$$R_o = (\text{R looking into drain of M10}) || (\text{R looking into drain of M8})$$
$$= [r_{o10}(1 + g_{m10} r_{o12})] || [r_{o8}(1 + g_{m8} r_{o6})] \tag{25.56}$$

The gain of the folded-cascode OTA is given by

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$$\frac{v_{out}}{v_{in}} = g_m R_o \tag{25.57}$$

Using the values shown in Fig. 25.42, g_m = 38.7 μA/V, r_{o6} = 1.67 MΩ, $r_{o8} = r_{o10} = r_{o12}$ = 3.33 MΩ, g_{m8} = 50 μA/V, g_{m10} = 38.7 μA/V, we find that the value of R_o is 170 MΩ and $|v_{out}/v_{in}|$ is 6,500 V/V.

The dominant pole of the OTA is located at $1/2\pi R_o C_L$. Parasitic poles exist at the sources of M7/M8 and M9/M10. These parasitic poles should be larger than the unity gain frequency ($f_u = g_m/2\pi C_L$) of the OTA. For the op-amp of Fig. 25.42, setting the unity gain frequency to 1 MHz results in C_L = 6.1 pF.

An op-amp can be made using the folded-cascode OTA and source-follower output buffer (Fig. 25.43). The value of the current source, I_{SF} , used in the source-follower depends on the amount of current sinking capability required of the op-amp. For example, if the minimum-load resistance the op-amp will see is 10 kΩ and *VSS* = – 2.5 V, then the current source should be at least 2.5/10 kΩ or 250 μA. In other words, the op-amp can sink 250 μA of current. When the op-amp is sourcing current, M15 must supply a current to the current source, I_{SF} , and a current to the load. The source-follower will not degrade the frequency performance of the OTA. However, the maximum output voltage will be limited to less than $VDD - V_{THN15}$.

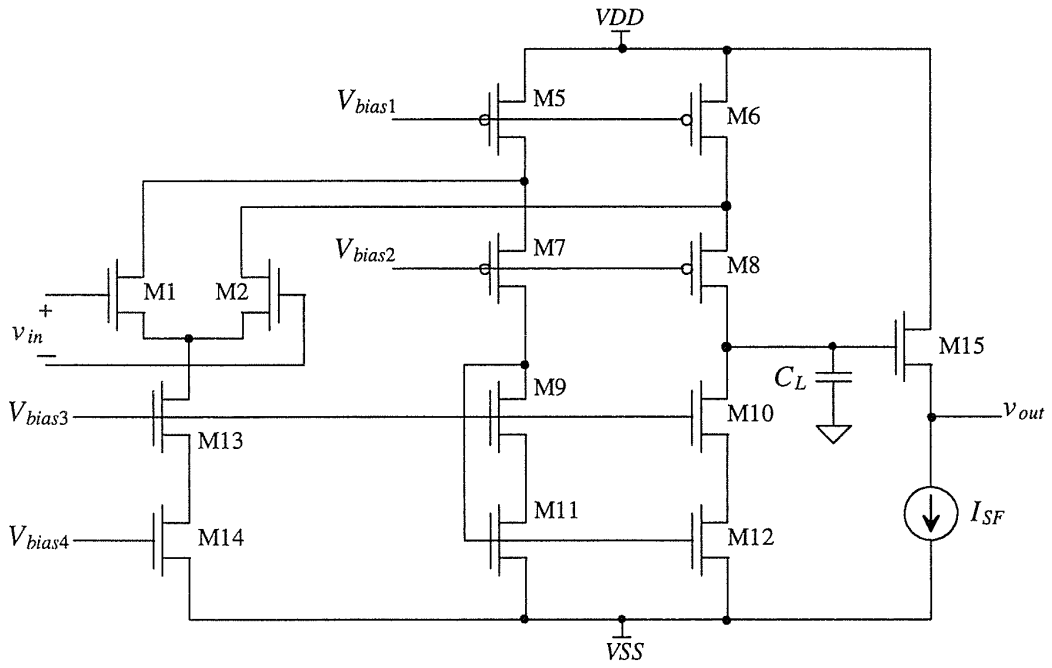


Figure 25.43 Folded-cascode op-amp.

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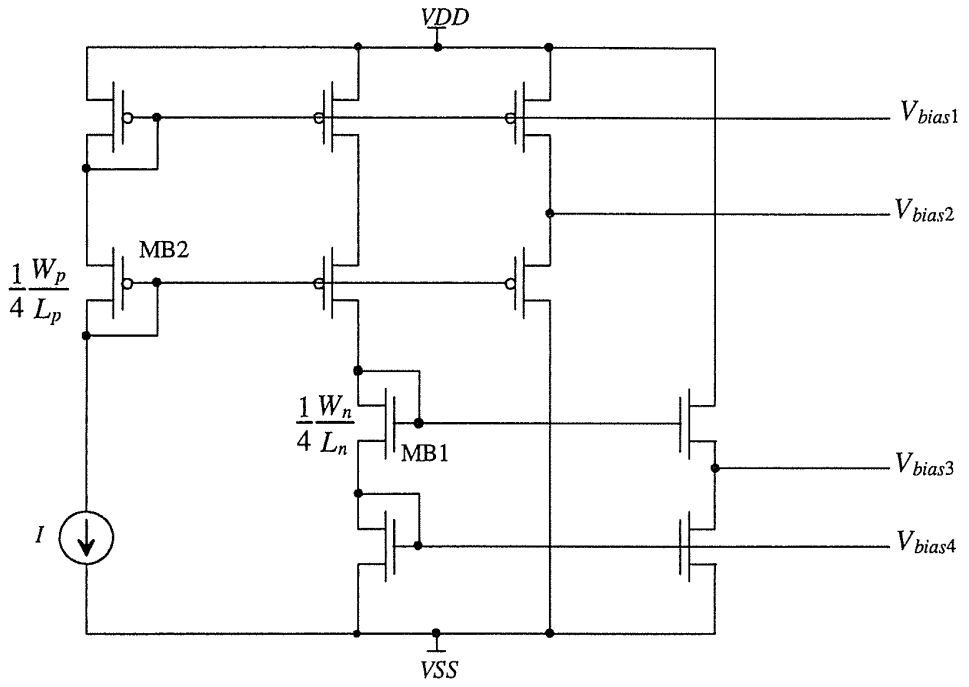


Figure 25.44 Biasing circuit for the op-amp of Fig. 25.43.

The bias voltages can be generated using the circuit of Fig. 25.44. This circuit is basically two wide-swing current mirrors based on the configuration given in Fig. 20.6. MB1 and MB2 are sized one-fourth the size of the other MOSFETs, as was discussed in Ch. 20. If, in Figs. 25.43 and 25.44, I = 10 μA and the unmarked n-channels are 15/5 and the unmarked p-channels are 70/5, then MB1 can be sized 30/40 and MB2 can be sized 35/10. This biasing scheme causes 10 μA to flow in MOSFETs M13, M14, M5, M6, and all MOSFETs in the biasing circuit. MOSFETs M1, M2, and M7-M12 have 5 μA of drain current. Note that this biasing scheme gives the maximum voltage swing on the output of the OTA (i.e., the drains of M8 and M10).

Wide-Swing Folded-Cascode OTA

A major advantage of the folded-cascode OTA of Fig. 25.42 is that the positive CMR extends beyond *VDD*, while the negative CMR is limited by the minimum voltage across the input diff-amp. Figure 25.45 shows a wide-swing folded-cascode OTA where the input CMR extends beyond the power supply rails (however, the output does not). The input diff-amp is the wide-swing type discussed in Ch. 24 (Fig. 24.27). If we use our familiar sizes of 15/5 and 70/5 for the n- and p-channel MOSFETs together with the bias circuit of Fig. 25.44 (with 10 μA biasing current), then a current of 10 μA flows in M5, M6, M11-M14, M17, and M18 (under DC conditions and assuming both diff-amps are on). The remaining MOSFETs in the circuit conduct 5 μA. SPICE simulation

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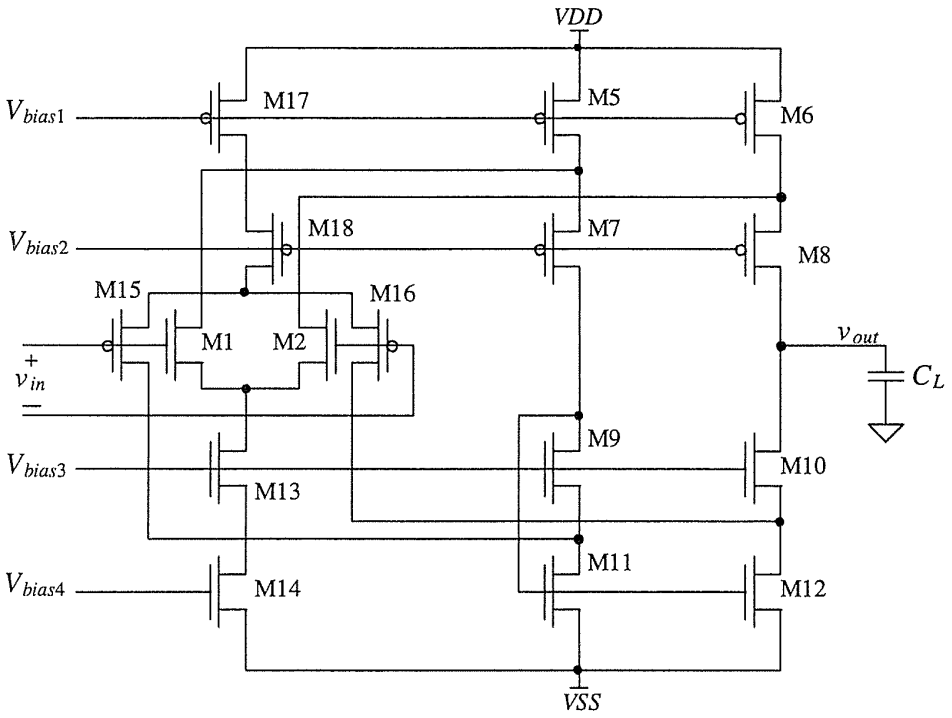


Figure 25.45 Wide-swing folded-cascode OTA.

results using this OTA in a unity gain configuration with *VDD* = 5 and *VSS* = 0 are shown in Fig. 25.46. The input voltage in this figure was swept from – 1 to 6 V. Note how the output stage of the OTA limits the maximum and minimum output voltages.

Compensation of the wide-swing folded-cascode OTA follows the procedure used to compensate the wide-swing OTA of Fig. 25.30. The problem of having one or both diff-amps on exists with this configuration as well. An additional problem exists with this configuration, that is, the low-frequency gain is not constant. Nevertheless, this configuration finds extensive use in analog applications. With both diff-amps conducting and a load capacitance of 1 pF, there is a 10 MHz unity gain frequency, with a 70° phase margin and an open-loop gain of 6500 (76 dB). The bias voltages or the size of the MOSFETs M5-M12 should be adjusted to compensate for the larger DC currents when one diff-amp is off. In other words, it is desirable to have wide-swing operation where the drain-source voltages of M5/M6 or M11/M12 are small (equal to the excess gate voltage). But if these voltages are too small, then M5/M6 or M11/M12 will approach the triode region and the gain will decrease.

The constant g_m stage discussed in Ch. 24 can be used as the input diff-amp stage for the wide-swing folded cascode. This solves the problem of varying transconductance for compensating the OTA, but the problem of nonconstant low-frequency gain remains.

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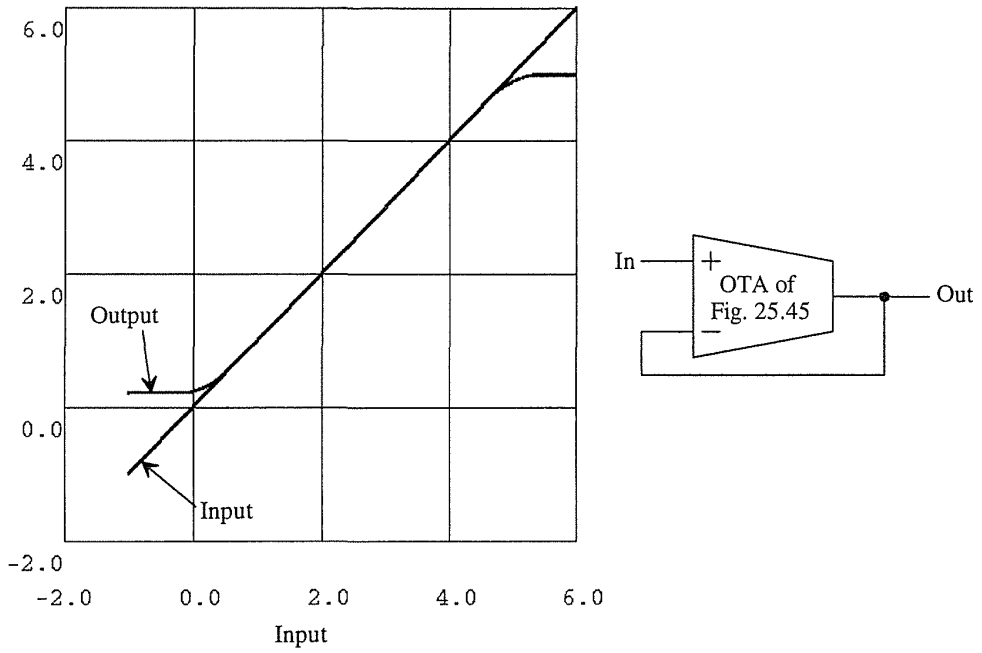


Figure 25.46 DC characteristics of wide-swing OTA of Fig. 25.45 in the unity gain configuration.

Folded-Cascode OTA with Output Buffer

In many applications, the OTA must drive a resistive/capacitive load or a large capacitive load. In these situations, a buffer between the load and OTA is used to ensure that the gain of the OTA is not degraded. Figure 25.47 shows one example of an output buffer that employs source followers. The output MOSFETs M03 and M04 are source followers used to drive the load. MOSFET M01 is simply a current source, while M02 is a p-channel source follower. The source-gate voltage of M02 is selected to bias both M03 and M04 on, that is, $V_{SG2} > V_{THN} + V_{THP}$. The gain through the buffer is approximately unity so that the compensation capacitance C_c does not have to be changed when the buffer is added to the OTA. The main drawback of this configuration is the limited output swing. The maximum output voltage is $VDD - V_{THN}$ (with body effect), while the minimum output voltage is $VSS + V_{THP}$.

A second example of a folded-cascode output buffer is seen in Fig. 25.48. This output buffer configuration is essentially the same as that shown in Fig. 25.41. The gate-drain connected MOSFETs M07 and M08 can be thought of as zero-canceling resistors (i.e., $R_z = 1/g_{m07} \| 1/g_{m08}$). Compensation follows the same procedure used for the two-stage op-amp discussed in the beginning of the chapter. Normally, since the gain of the output buffer can be low, the output MOSFETs, M05 and M06, can be sized with minimum or near-minimum lengths. This has the effect of increasing the output drive capability. This buffer has the added advantage that the outputs can approach the supply voltages.

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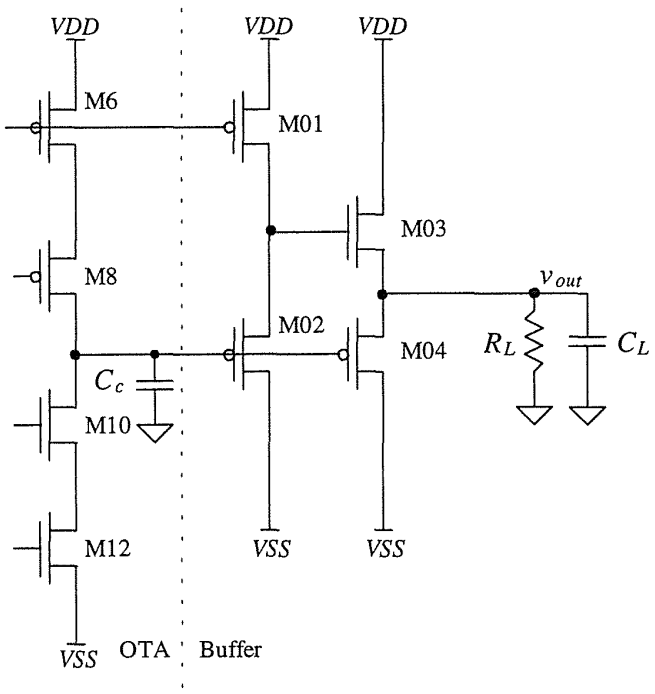


Figure 25.47 Output buffer for use with a folded-cascode OTA (unity gain).

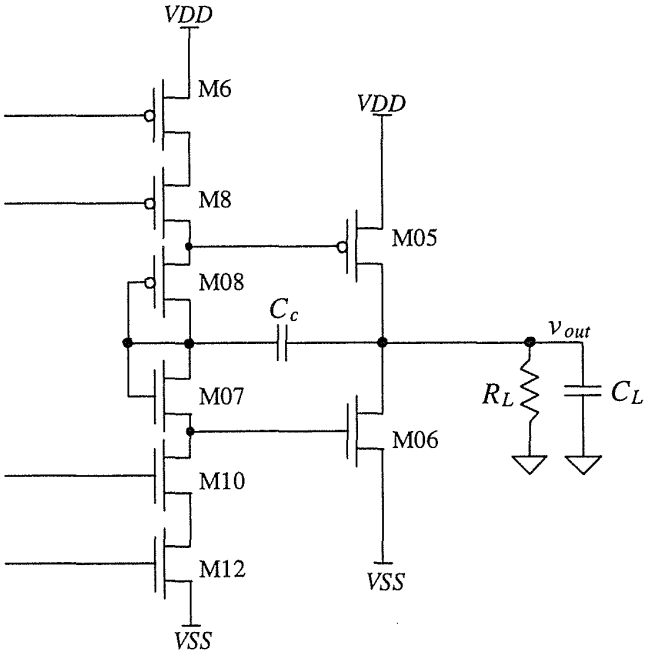


Figure 25.48 Output buffer for use with a folded-cascode OTA (with gain).

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Figure 25.49 shows a wide-swing folded-cascode OTA, with output buffer based on floating current sources [7]. This configuration is very useful in low-supply voltage op-amp design. To illustrate the operation and biasing of this op-amp, let's assume that the biasing circuit of Fig. 25.44 is used with I = 10 μA, 15/5 n-channels, 70/5 p-channels. MB2 is sized 15/20 and MB1 is 35/10. The generation of the bias voltages V_{biasp} and V_{biasn} will be discussed momentarily. With these sizes, and assuming both diff-amps are conducting current, 10 μA flows in M17/M18, M13/M14, M5/M6, and M11/12. A current of 5 μA flows in M1/M2, M15/M16, M7/M8, and M9/M10. A current of 100 μA flows in MO1/MO2, and a current of 2.5 μA flows in MC1-MC4. The current that flows in M5/M6 and M11/M12 is mirrored in MO1 and MO2.

The floating current sources MC1/MC2 and MC3/MC4 form a positive feedback loop with a gain of 1. The resistance looking into the sources of these parallel MOSFETs is the output resistance of the MOSFETs in series with the output resistance of the cascode MOSFETs of the folded-cascode OTA.

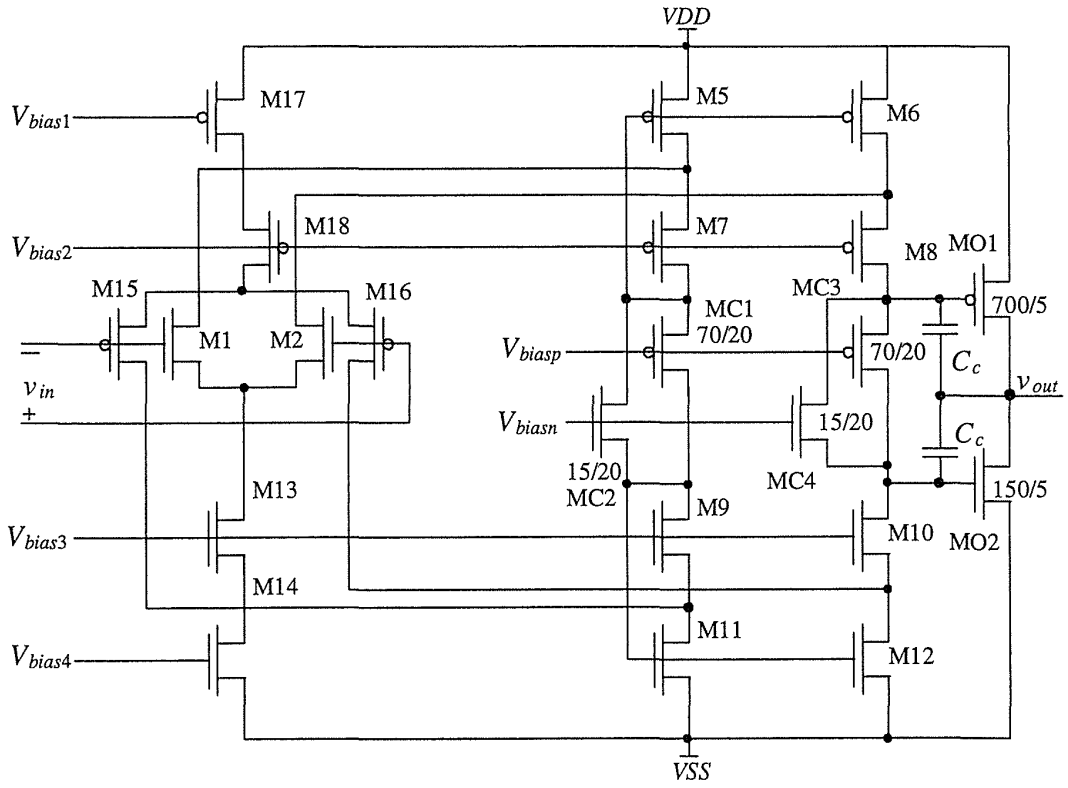


Figure 25.49 Wide-swing folded-cascode OTA with output buffer (an op-amp).

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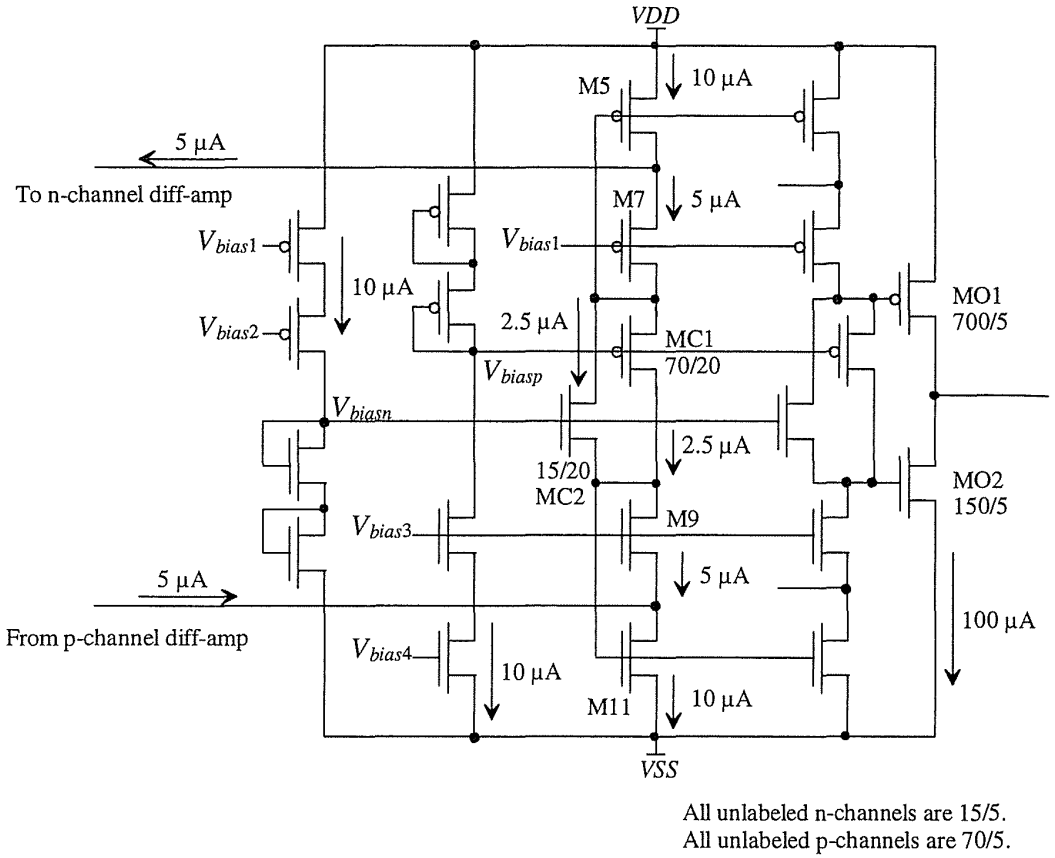


Figure 25.50 Simplified schematic of biasing circuitry for the op-amp of Fig. 25.49.

The schematic of the biasing circuit is shown in Fig. 25.50. The reason for sizing MC1-MC4 one-fourth the other MOSFETs now becomes obvious: they conduct 2.5 μA of current. An interesting situation occurs when one of the diff-amps on the input of the op-amp shuts off. If the p-channel diff-amp were to turn off, as a result of the input signal going outside the p-diff-pairs CMR, then the 5 μA of current flowing into the drain of M11 from the p-channel diff-amp would become zero. This would cause the current flowing in M01 and M02 to become unbalanced (i.e., 100 μA of current flowing in MO1 and 50 μA of current flowing in MO2). However, without a DC load current, we know that these currents must be equal. The result is an offset voltage on the input of the op-amp that will result in balanced currents in MO1 and MO2. Because of the very large gain of this topology, this offset voltage is usually negligible in comparison to the offsets resulting from device mismatches. Device matching is critical for low-distortion amplifier design, and in many cases the device matching will restrict the use of more elegant circuit structures (e.g., the constant transconductance diff-amp).

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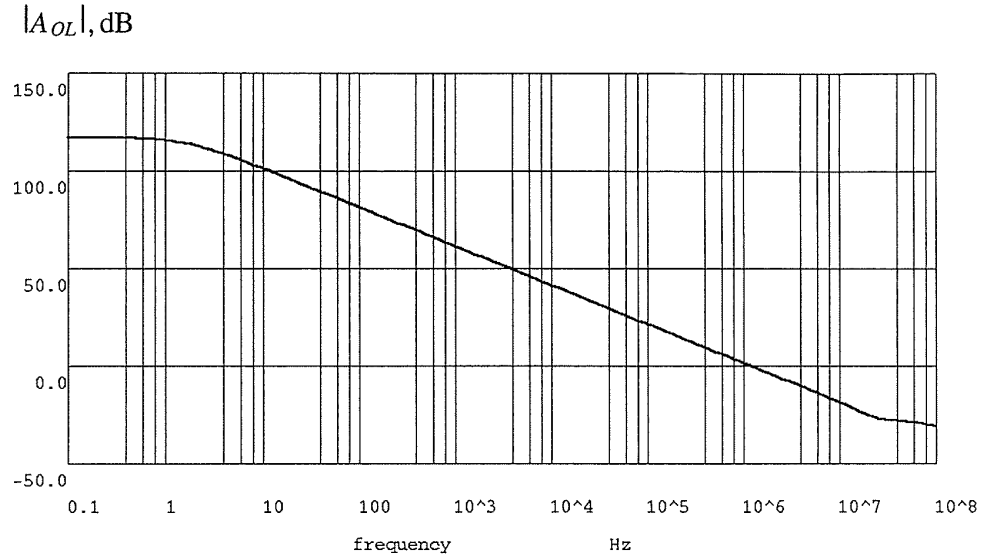


Figure 25.51 Open-loop-compensated gain of the op-amp of Fig. 25.49.

The open-loop compensated gain of the op-amp of Fig. 25.49 is shown in Fig. 25.51. The op-amp was compensated with two 5 pF capacitors. The open-loop DC gain of this configuration is 700,000 V/V. Simulating the characteristics of an op-amp with such a large gain requires that the RELTOL, VNTOL, and ABSTOL remain at their default values or less. Also, the DC stability scheme of Fig. 25.7 may not work well for high-gain op-amps because of the presence of feedback in the circuit. The scheme shown in Fig. 25.52 can be used to simulate the open-loop gain of an op-amp. The value of V_{bias} is changed until all MOSFETs in the op-amp are biased into the saturation region. For the simulation of the op-amp of Fig. 25.49, a 1 V (AC)/2.5 V (DC) voltage source was connected to the positive, or noninverting, input of the op-amp. After several simulation runs, it was found that a 2.49995 V bias on the minus, or inverting, input of the op-amp caused all MOSFETs to operate in the saturation region.

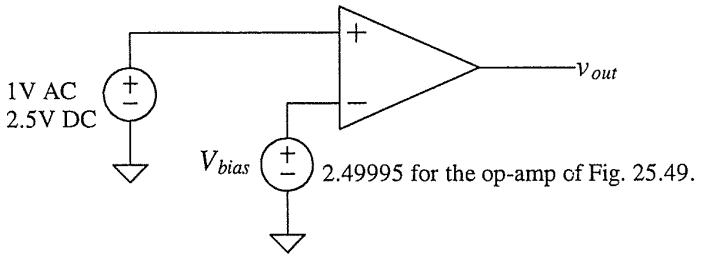


Figure 25.52 Simulating the open-loop response of a high-gain op-amp.

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25.3 The Differential Output Op-Amp

The differential output op-amp symbol is shown in Fig. 25.53. The open-loop gain of the op-amp is given in terms of the inputs and outputs by

$$A_{OL} = \frac{v_{o+} - v_{o-}}{v_+ - v_-} \tag{25.58}$$

This should be compared to the single-ended output op-amp (the op-amp we have been discussing up to this point), which has a gain given by

$$A_{OL} = \frac{v_{o+}}{v_+ - v_-} \tag{25.59}$$

If we ignore v_{o-}, then the differential output op-amp behaves just like a single-ended op-amp. For linear applications the op-amp is used with a feedback network, the inputs are related by

$$v_+ \approx v_- \tag{25.60}$$

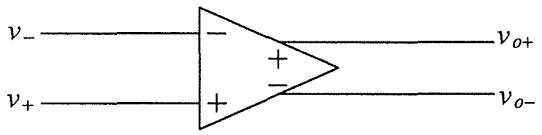


Figure 25.53 Differential output op-amp.

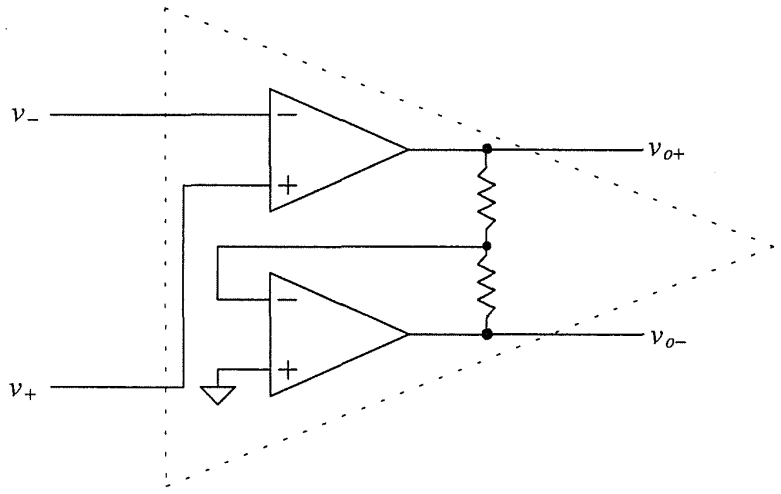


Figure 25.54 Formation of a differential output op-amp using two single-ended op-amps.

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while the outputs are related by

$$v_{o+} \approx -v_{o-} \tag{25.61}$$

We can use two single-ended op-amps to form a differential output op-amp (Fig. 25.54). This implementation works well for low frequencies. However, because the op-amps are in different topologies, the phase response of each op-amp is different. This means Eq. (25.61) will not hold for higher (> 1 kHz) frequencies because the time delays through each configuration are sufficiently different.

The importance of using differential output op-amps can be explained with the help of Fig. 25.55. This figure shows a cascade of differential output op-amps, without feedback network. The stray capacitance between the interconnecting metal lines (the metal lines that carry the signals between op-amps) and the substrate or any other noise source are shown. If the metal lines are run close to one another, then the noise voltage will couple even amounts (ideally) of noise into each signal wire. Since the diff-amp, on the input of the op-amp, rejects common signals (signals that are present on both inputs), the coupled noise is not passed to the next op-amp in the string. Variations on the power supply rails are rejected as well. If the differential op-amp is symmetric, then changes on the power supply couple evenly into both outputs, having little effect on the difference, or desired signal, coming out of the op-amp. For these reasons (i.e., good coupled noise rejection and PSRR, the differential op-amp is a necessity in any mixed-signal integrated circuit. (Mixed-signal means that both analog and digital circuits are present on the chip - digital logic is great at generating noise.)

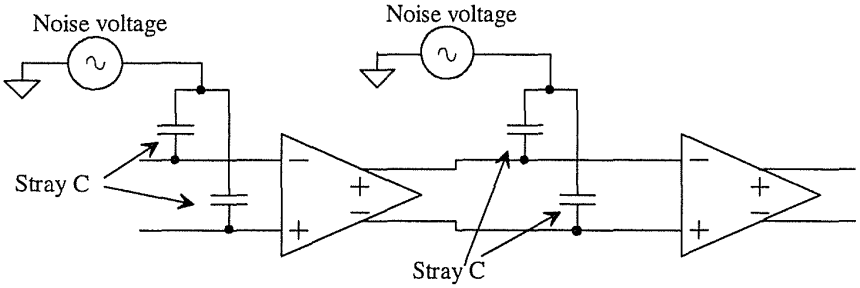


Figure 25.55 Differential output op-amps showing parasitic capacitance and noise.

Normally, the average of the op-amp outputs is called the common-mode output voltage and in terms of the supply voltages, is given by

$$V_{CM} = \frac{VDD + VSS}{2} \tag{25.62}$$

For example, if VDD = 2.5 V and VSS = – 2.5 V, then both outputs are referenced to the common-mode voltage 0 V (ground). If VDD = 5 V and VSS = 0, then V_{CM} = 2.5 V. Figure 25.56a shows a simple differential output op-amp gain configuration (inverting or noninverting, depending on which output is used as the positive output). Since the input voltages to the circuit are equal, the output voltages of the op-amp should remain

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at V_{CM}. However, if $v_{o+} = v_{o-} = VDD$ or $v_{o+} = v_{o-} = VSS$ or $v_{o+} = v_{o-}$ = anything, then $v_+ = v_-$ (this is a problem). Equation (25.61) can be written to include the common-mode output voltage:

$$v_{o+} + V_{CM} \approx -v_{o-} + V_{CM} \tag{25.63}$$

To hold the common-mode output voltage of the op-amp at a known voltage, that is, V_{CM}, the configuration of Fig. 25.56b is used. A circuit called "common-mode feedback" (CMFB) is used to sense the average value of the op-amp outputs (that is, V_{CM}). The output of the CMFB circuit is fed back into the op-amp to adjust V_{CM} to the correct value, that is, the value given by Eq. (25.62). The op-amp of Fig. 25.54 has its V_{CM} set by the connection of the "+" input of the bottom op-amp. In this figure, $V_{CM} = 0$ V, and so it can be concluded that this configuration works with $VDD = -VSS$.

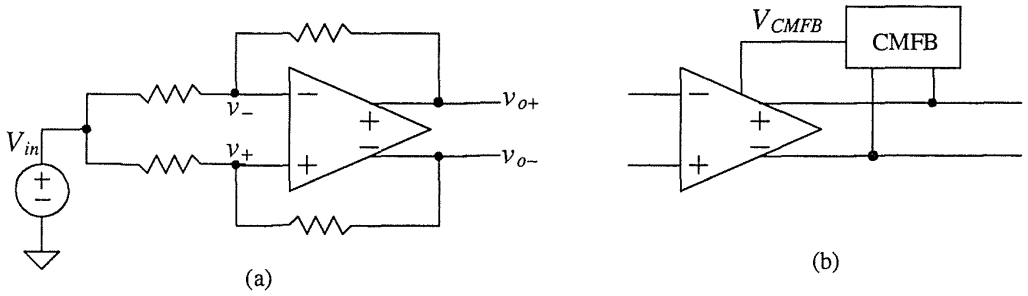


Figure 25.56 (a) Simple gain configuration using differential output op-amp and (b) the use of a common mode feedback circuit to adjust the common-mode output voltage.

25.3.1 Fully Differential Folded-Cascode OTA

The fully differential (both inputs and outputs) folded-cascode OTA is shown in Fig. 25.57. The main difference between this OTA and the single-ended OTA of Fig. 25.43 is that the gate of M11 is now tied to V_{bias4} where, as before, it was tied to the drain of M9. The drains of M9 and M7 are now the "–" output of the OTA. Although this change is subtle, it drastically affects the DC biasing of the OTA.

The currents through M7-M12 are now 10 μA. The current through M5 and M6 is 15 μA. The common-mode feedback circuit should adjust the gate potential of M5 and M6, so that they provide the 15 μA of current to M1/M2 and M7-M12. For reasons that will be clear when we discuss the CMFB circuit, the sizes of M5 and M6 are increased to 1.5 times the size of the other p-channel MOSFETs used in the circuit. The biasing circuit of Fig. 25.44 can be used if V_{bias2} is tied to the gate of MB2, and MB2 is resized to the *W/L* of the other p-channel MOSFETs in the circuit. The change lowers the value of V_{bias2} and the maximum output swing of the OTA. Lowering V_{bias2} allows the voltage on the drains of M5 and M6 to vary without letting them go into the triode region. This is important for proper operation of the CMFB circuit.

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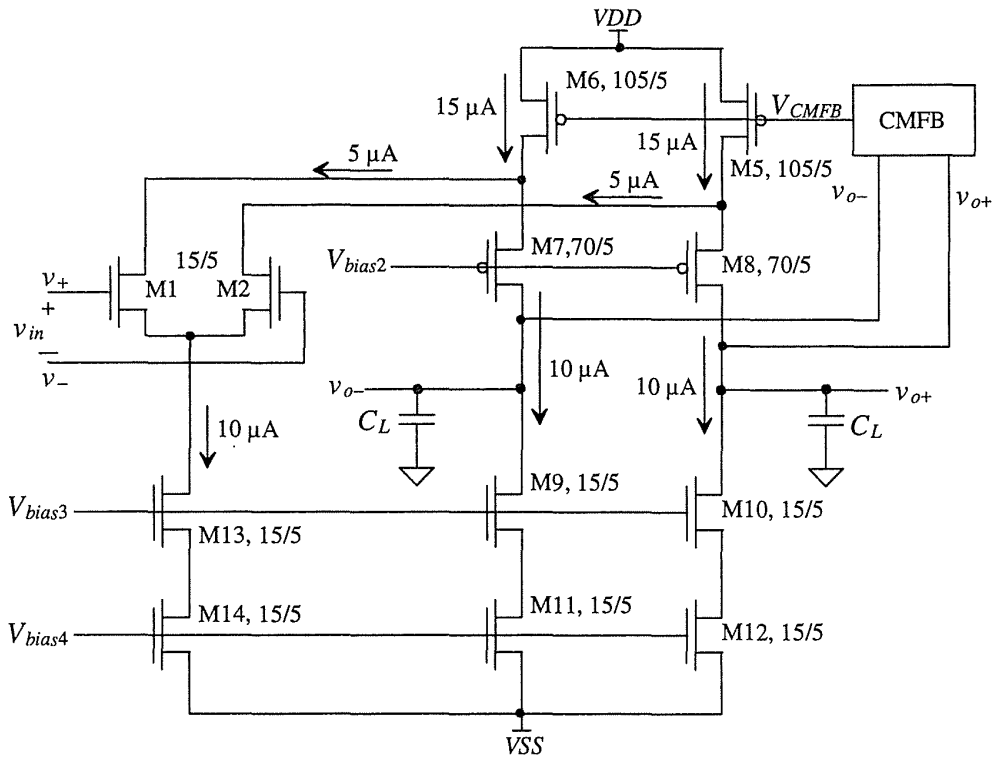


Figure 25.57 Fully differential folded-cascode OTA.

Compensation of the OTA is accomplished in the same manner as the single-ended OTA except now two load capacitances are required, one for each output.

The CMFB Circuit

A common-mode feedback circuit is shown in Fig. 25.58. The inputs to the circuit are v_{o+} and v_{o-} of the OTA, while the output is V_{CMFB}. The unique aspect of this circuit is its rejection of a difference-mode signal on its inputs and amplification of the common-mode signal. This is exactly the opposite of what a single diff-amp does. To be exact, the CMFB circuit amplifies the difference between the average of the outputs, $(v_{o+} + v_{o-})/2$ and V_{CM}. Through the use of feedback, through the OTA, the averages of the outputs and V_{CM} are made equal. This is similar to how feedback is used to set the inputs of an op-amp, v_+ and v_-, equal. We will cover the feedback mechanism further during the discussion of compensating the CMFB circuit. The MOSFETs MF1/MF2 and MF3/MF4 are simply current sources (10 μA for the sizes and currents shown in Fig. 25.57). In the following discussion, we will assume *VSS* = 0, *VDD* = +5 V, and V_{CM} = 2.5 V.

To understand the operation of the circuit, let's first consider the DC case when both v_{o+} and v_{o-} are 2.5 V. (This is what we ultimately want, that is, both outputs' DC component equal to the common-mode voltage.) The gates of MF5-MF8 are at 2.5 V,

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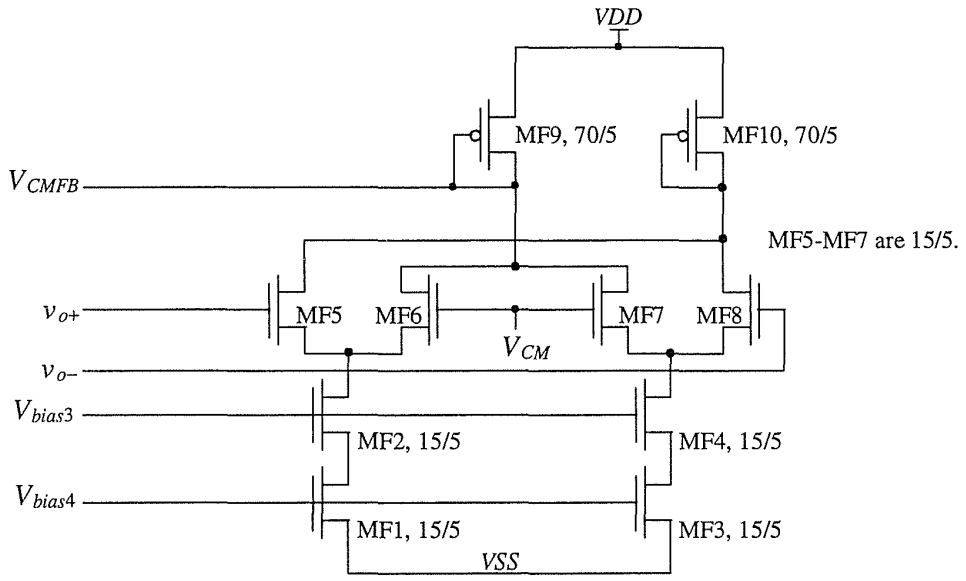


Figure 25.58 Common-mode feedback circuit.

and their drain currents are 5 μA. The current through MF9 is 10 μA. This current sets the V_{SG} of MF9. Since MOSFETs M5 and M6 of the OTA are 1.5 times the size of MF9, a current of 15 μA flows in these MOSFETs. This is the current required by M1/M2 and M7-M12, and so the CMFB circuit output doesn't change. Mismatches in the MOSFETs used in either the CMFB circuit or the OTA will result in an offset voltage.

If v_{o+} and v_{o-} go above V_{CM}, then the drain currents of MF6 and MF7 start to decrease. This causes V_{CMFB} to increase toward *VDD*. The increase in V_{CMFB} causes the drain currents of M5 and M6 to decrease. Since the current through M9-M12 is constant, the result is a decrease in the average output voltages. A similar argument can be made for the case when v_{o+} and v_{o-} are below V_{CM}; that is, the average output voltage increases because the current flowing in MF9 increases. Next consider the correct possible outputs v_{o+} = 3.5 V and v_{o-} = 1.5 V. These voltages lie outside the CMR range of the CMFB diff-amps. An incremental change in the inputs to the OTA can cause the outputs to become unbalanced. For example, if v_{o+} = 3.0 V and v_{o-} = 1.5 V then V_{CMFB} doesn't change (assuming the diff-pair CMR is a few-hundred mV). However, through the use of feedback around the OTA, either resistive (for an OTA with buffer) or capacitive feedback, the outputs will change until the OTA inputs are equal (i.e., $v_+ = v_-$), which can occur even if the outputs are unbalanced (i.e., $v_{o+} - v_{o-}$ is correct, but v_{o+} does not equal $-v_{o-}$).

One solution to increasing the CMFB circuit's CMR is to increase the lengths of MF5 through MF8. This decreases the transconductance of the diff-amp and thus lowers the gain of the CMFB circuit. Low CMFB circuit gain makes balancing the

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outputs more difficult. Also the circuit's 3-dB frequency decreases, which can affect the compensation of the CMFB/OTA combination.

Figure 25.59 shows an alternative CMFB circuit [8], which operates over wide output voltage swings. In some cases, the buffers can be implemented using source-followers. The average of v_{o+} and v_{o-} is generated with the help of the resistor/capacitor combination and applied to the gate of M1. This scheme ensures fully balanced outputs over a voltage range limited by the CMR of the buffers.

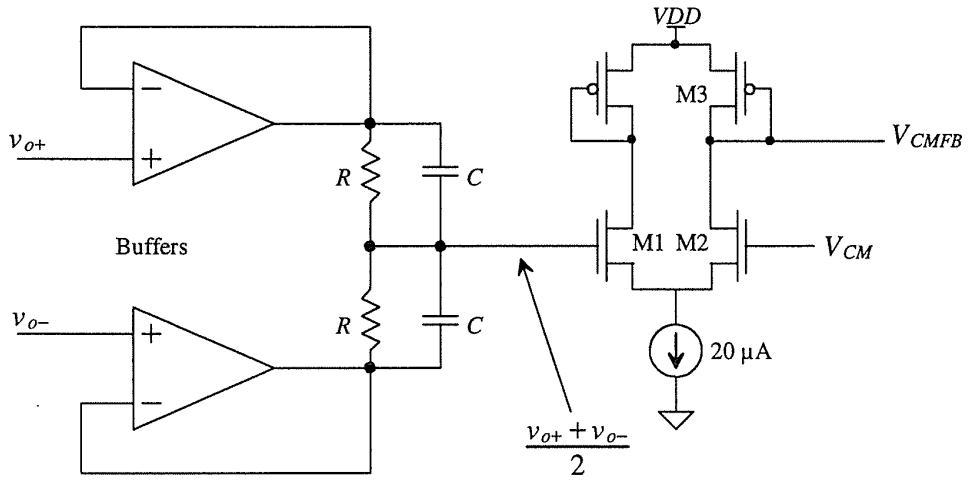


Figure 25.59 Improved range CMFB circuit.

A simple method of changing a single-ended input signal referenced to ground into a signal usable in a differential system is shown in Fig. 25.60. The p-channel MOSFETs perform two functions: (1) DC level shifting (adding V_{SG} of the p-channel

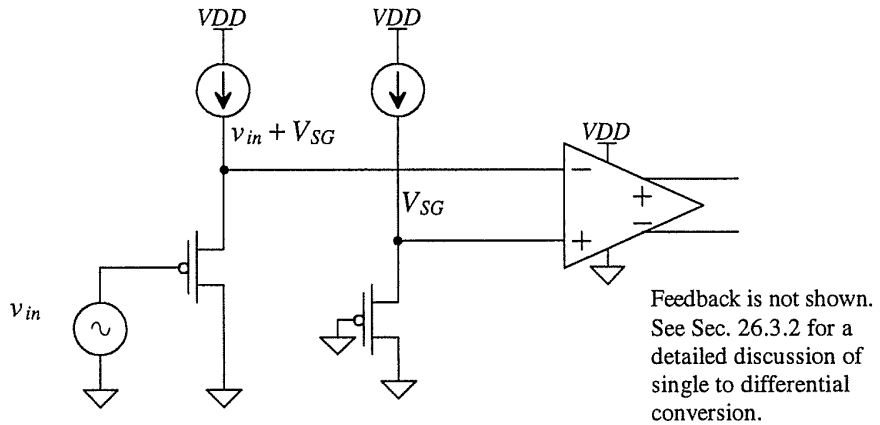


Figure 25.60 Circuit used to change a single-ended input signal into a differential signal.

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MOSFETs to the input signal) and (2) buffering the input signal. Note that the value of V_{SG} is not critical - it simply moves the input signal into the CMR of the op-amp. The output DC level of the op-amp is determined by the CMFB circuit. (V_{SG} should be close to V_{CM} if resistive feedback is used in order to reduce the amplifier input DC current.)

Compensating the CMFB Circuit

The CMFB circuit combined with the folded-cascode OTA forms a feedback loop. As with any feedback loop, we must ensure stability. If we apply a common AC signal (let's call it v_{oc}) to both inputs of the CMFB amplifier of Fig. 25.58, the resulting gain is

$$\frac{v_{CMFB}}{v_{oc}} = \frac{g_{m5}}{g_{m9}} \approx 1 \tag{25.64}$$

where g_{m5} is the small-signal transconductance of MF5, MF6, MF7, or MF8 and g_{m9} is the small-signal transconductance of MF9. The bandwidth of this configuration is very wide. This is important since we do not want any phase shift through the CMFB circuit to degrade the phase-margin of the feedback loop. To actually understand the feedback mechanism present, consider the simplified drawing of the OTA/CMFB circuit shown in Fig. 25.61. One side of the folded-cascode amplifier is shown, and the CMFB circuit is drawn as a gain block. The gain from the gate of M5 to the output (the drain of M8) is $g_{m5} \cdot R_o$, where R_o is output resistance of the cascode configuration given by Eq. (25.56). If the bandwidth of the CMFB amp is wide compared to the OTA and the gain is approximately one, then the same load capacitance used to compensate the OTA can be used to compensate the CMFB amp.

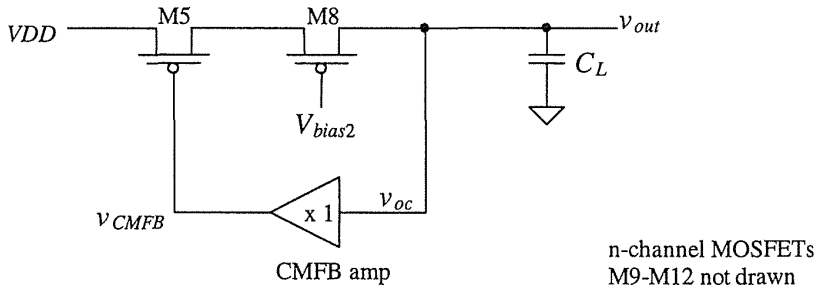


Figure 25.61 Feedback circuit resulting from addition of the CMFB circuit.

Simulation results for the fully differential folded-cascode OTA of Fig. 25.57, using a C_L of 6.1 pF (f_u = 1 MHz) on each output, are shown in Fig. 25.62. For these simulations, *VDD* = 5 V, *VSS* = 0, and v_+ = 2.5 V (DC) + AC, while v_- = 2.5 V + AC@180° phase. Interdigitated layout was employed in the folded-cascode section to increase matching. The folded-cascode OTA with common-source output buffers is shown, drawn slightly different than Fig. 25.57, in Fig. 25.63. The CMFB circuit inputs can now be connected to the outputs of the source followers. Layout of the fully-differential folded-cascode OTA is shown in Fig. 25.64. The bias voltages are supplied on poly1.

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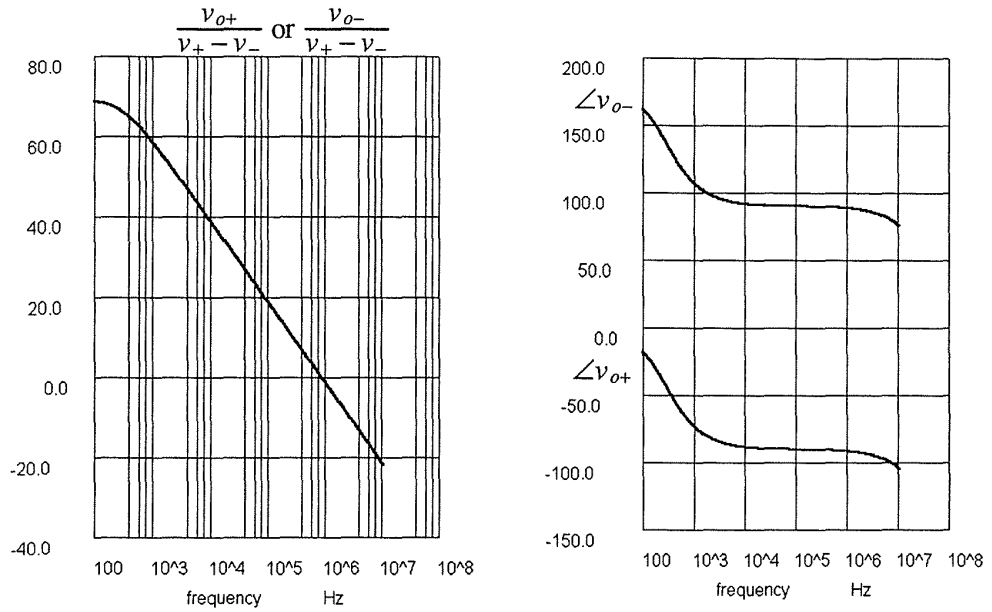


Figure 25.62 Magnitude and phase responses of the folded-cascode OTA of Fig. 25.57.

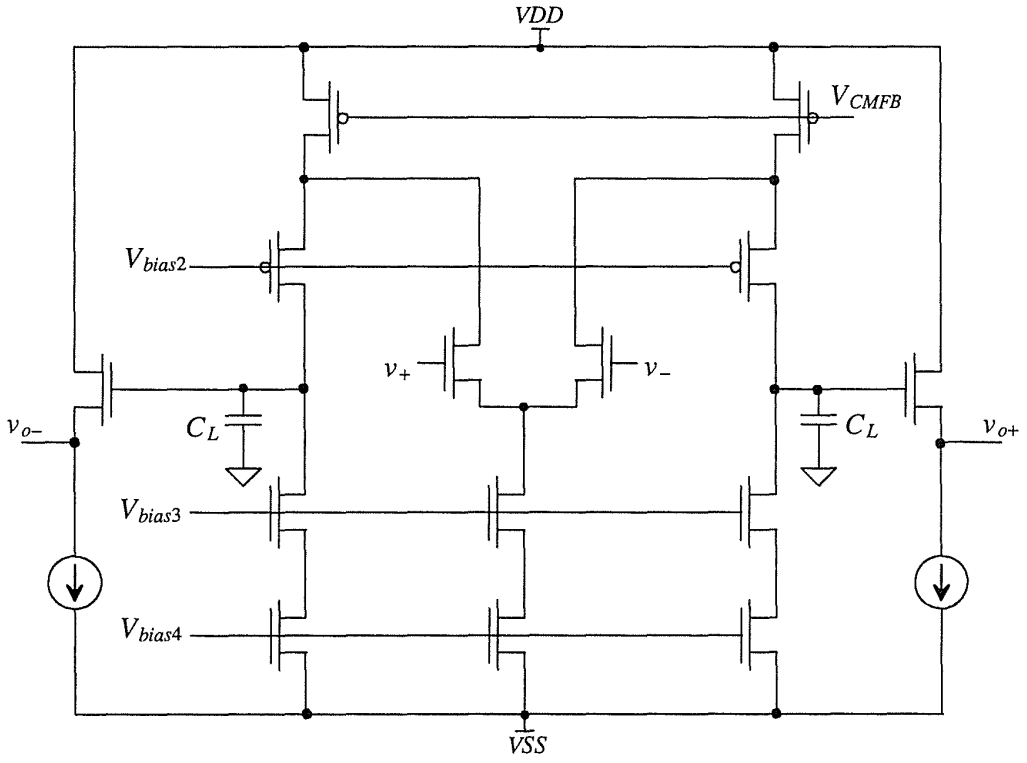


Figure 25.63 Fully differential folded-cascode op-amp.

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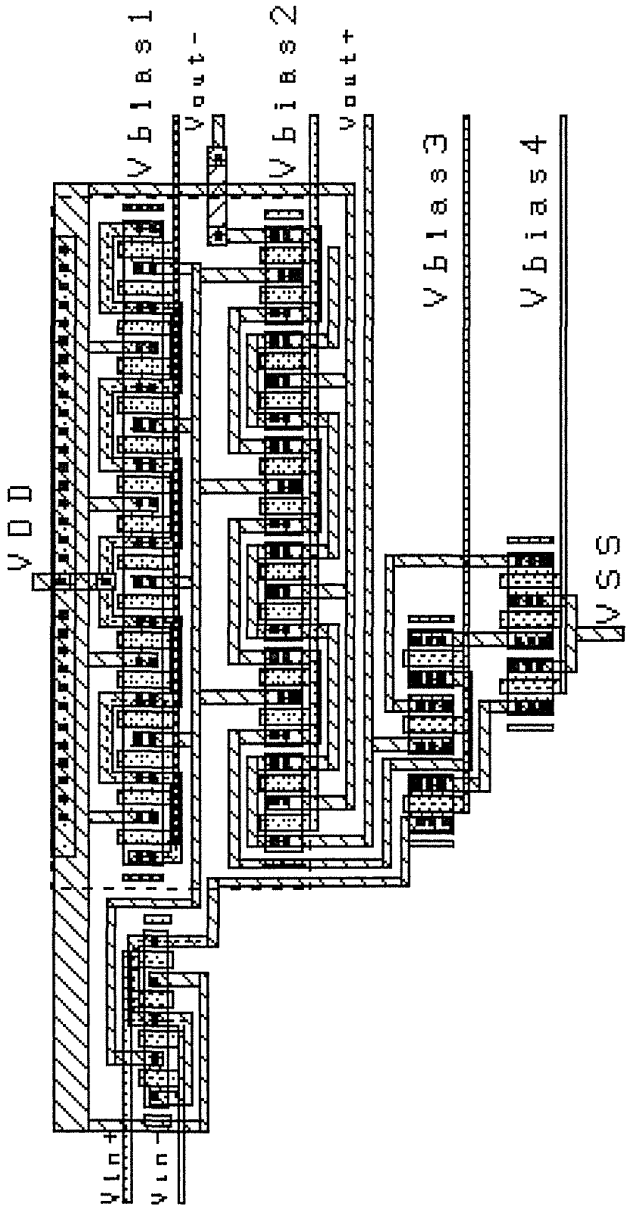


Figure 25.64 Layout of the folded-cascode OTA.

A buffered differential op-amp topology is seen in Fig. 25.65 without the input diff-amp drawn. This topology uses the floating current sources discussed in Sec. 25.2.2. The middle string of MOSFETs shown in this figure are used for biasing. However, if the diff-amps source or sink current into the outer MOSFETs, in this section of the op-amp, the biasing can be affected to the point where the op-amp doesn't

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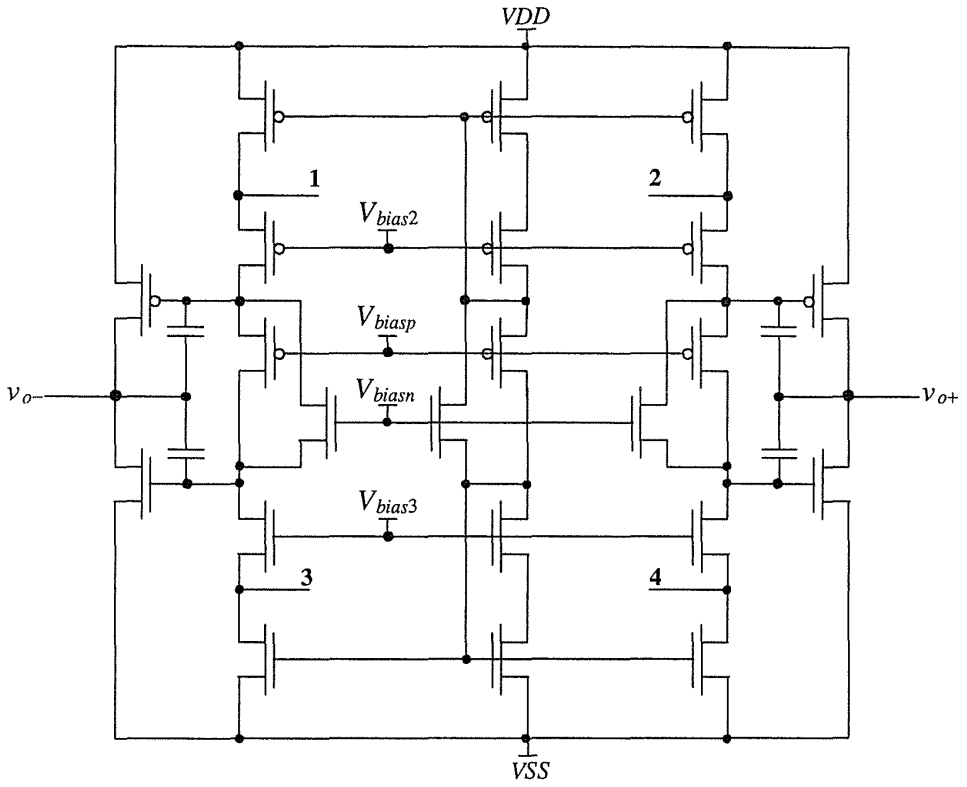


Figure 25.65 Buffered differential output op-amp using floating current sources. Note that the output buffers will not operate class AB when one of the diff-amps is off.

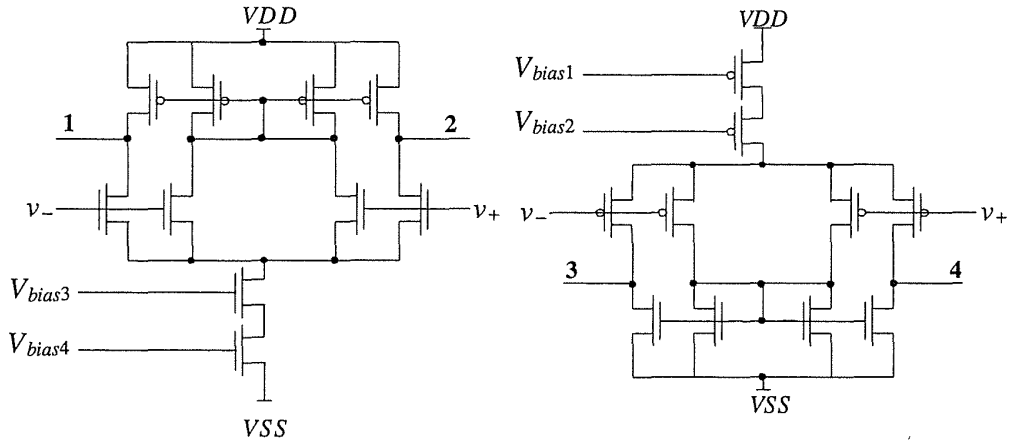


Figure 25.66 Input diff-amps for the op-amp of Fig. 25.65.

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function. For this reason, the diff-amps shown in Fig. 25.66 are used. The node numbers in this figure correspond to the labeled nodes in Fig. 25.65. These diff-amps do not source or sink a current; for DC biasing purposes, therefore the diff-amps can be connected directly to the folded-cascode section of Fig. 25.65 without any interaction.

The final component required in the design of this op-amp is the CMFB circuit Fig. 25.67. Since the outputs of the op-amp are buffered, we can connect the outputs directly to the averaging resistors. When the outputs are balanced, the CMFB circuit does not source or sink a current and thus does not affect the folded-cascode section. However, if the average of the outputs is above V_{CM}, then the outputs source a current, shifting the average output voltage lower until the outputs are balanced (i.e., $v_{o+} = -v_{o-}$).

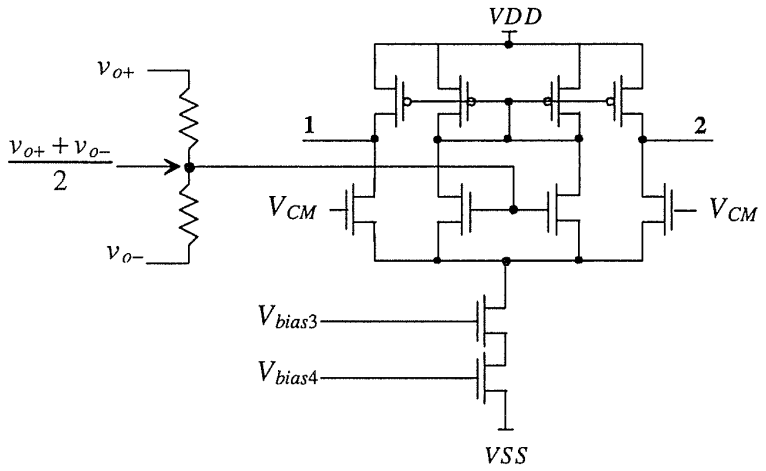


Figure 25.67 Common-mode feedback circuit for the op-amp of Fig. 25.65.

25.3.2 Gain Enhancement

Up to this point, the only method we have had to increase the gain of an op-amp is decreasing the biasing currents. The problem with lowering the bias currents is that our unity gain frequency drops (more on this at the end of the section). In addition, the gain of an op-amp is ultimately limited to the gain of the MOSFET in the subthreshold region (see Fig. 22.15). Gain-enhancement techniques help to overcome these limitations.

Gain-enhancement can be demonstrated with the help of Fig. 25.68 [9]. Without the OTA present, the gain of this cascode amplifier is $g_{m1} \cdot R_o$ where R_o is the resistance looking into the drain of M2, that is, $r_{o2}(1 + g_{m2} \cdot r_{o1})$; see Eq. (20.12). With the OTA in place, the output resistance becomes

$$R_{oGE} = r_{o2}[1 + (1 + A_{OTA})g_{m2}r_{o1}] \tag{25.65}$$

where A_{OTA} is the voltage gain of the OTA. The gain of the cascode configuration with gain enhancement is

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$$A_{vGE} \approx A_{OTA} \cdot (g_{m1} \cdot R_o) \tag{25.66}$$

Adding the OTA to the circuit increased the gain of the configuration by A_{OTA}. We can apply this technique to increase the gain of the fully differential folded-cascode OTA of the last section but not to a single-ended output op-amp. Because of the lack of CMFB in single-ended output op-amps, the DC biasing becomes too difficult to implement in most cases.

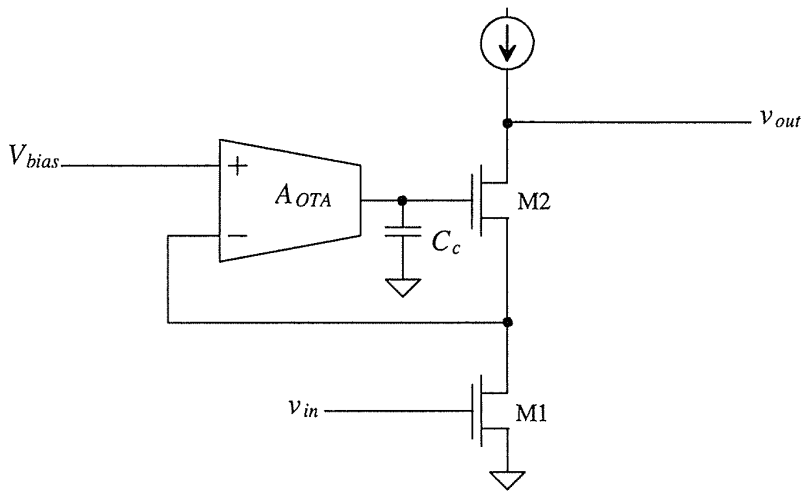


Figure 25.68 Use of gain enhancement to increase cascode open-circuit gain.

Figure 25.69 shows the op-amp of Fig. 25.57 (or Fig. 25.63 without output buffers) implemented using gain-enhancement techniques. To keep things simple, we have used the same DC biasing voltages, those generated with the circuit of Fig. 25.44. In practice, the biasing voltages would be changed since now the sources of M7/M8 are held at V_{bias2}. The wide-swing OTA of Fig. 25.30 was used in this amplifier simply because it has already been characterized in the chapter. The gain of the OTA is 240 V/V (47 dB). The cascode amplifier without gain enhancement had an open-loop gain, from Fig. 25.62, of 68 dB (single-ended output) and 74 dB (double-ended output). We can estimate the open-loop gain of the OTA of Fig. 25.62 as 68 dB + 47 dB, or 115 dB. Note that since we have not changed the transconductance of the input diff-amp, we can still compensate the OTA with a 6.1 pF for a unity gain frequency of 1 MHz. The gain enhancement simply shifts the open-loop 3 dB frequency of the OTA downward. Simulation results are shown in Fig. 25.70.

High-Speed CMOS Op-Amp Design

Up to this point we have not been concerned about designing an op-amp for high-speed operation. The unity gain frequency of the OTAs we have discussed thus far is given by $g_m/2\pi C_L$ where g_m is the transconductance of the input diff-amp and C_L is the load capacitance used to compensate the OTA. We might conclude that simply by increasing

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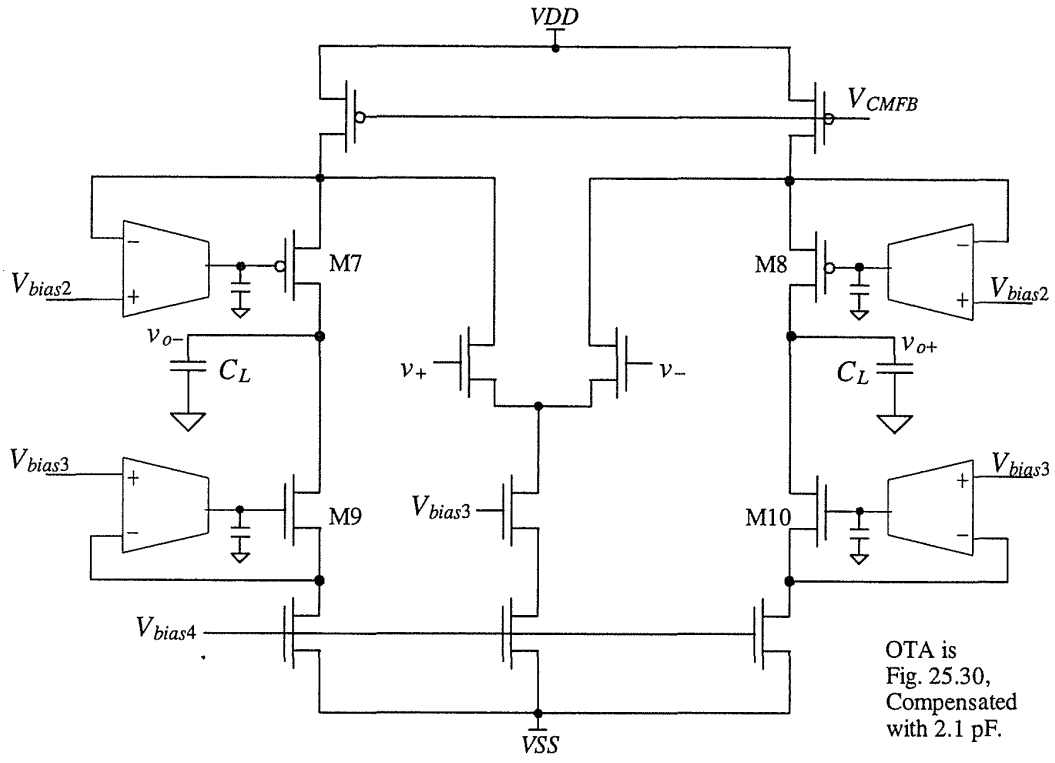


Figure 25.69 Fully differential folded-cascode OTA with gain enhancement.

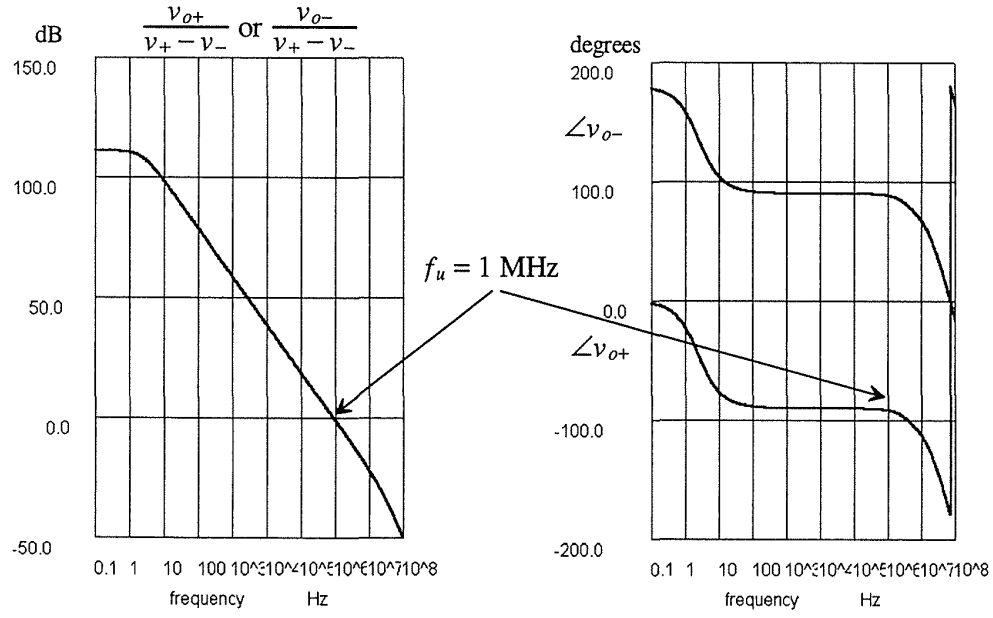


Figure 25.70 Simulation results for the op-amp of Fig. 25.69.

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the width of the input diff-pair, possibly to several thousand μm, we can increase the unity gain frequency. While this is true to a point, the intrinsic speed of the MOSFET limits the practical unity gain frequency. (Every MOSFET introduces a parasitic pole into the overall transfer function of the op-amp.) In Ch. 9 we discussed the unity gain frequency of a MOSFET, f_T. This frequency f_T is determined by the point where the gate current and drain current of the MOSFET are equal and is given by

$$f_T = \frac{3 \cdot KP}{4\pi \cdot C'_{ox} L^2} \cdot (V_{GS} - V_{THN}) \tag{25.67}$$

The channel length, L, and V_{GS}, can be used to increase f_T. For high-speed operation, the minimum channel length should be used. In the CN20 process, this means that all MOSFETs used in an amplifier should have a channel length of 2 μm. The gate-source voltage of a MOSFET should also be large. However, as we know, increasing the gate-source voltage of a MOSFET decreases the input CMR and output voltage swing. A reasonable value of $V_{GS} - V_{THN}$ for high-speed operation is 0.5 V.

The folded-cascode OTA of Fig. 25.57 can be implemented using 1000/2 MOSFETs and increasing the biasing current to 1 mA. MOSFETs M5 and M6 are 1500/2 because they supply 1.5 mA. Note that the CMFB circuit can be scaled down to reduce power dissipation; for example, the MOSFETs used in this circuit can be 100/2. With a 5 pF compensation capacitor, the simulation results are shown in Fig. 25.71. The open-loop gain is 48 dB (250), while the unity gain frequency is 70 MHz. The low value of open-loop gain is the result of using a 2 μm device with a λ of approximately 0.8 V^{-1} and a large biasing current (1 mA).

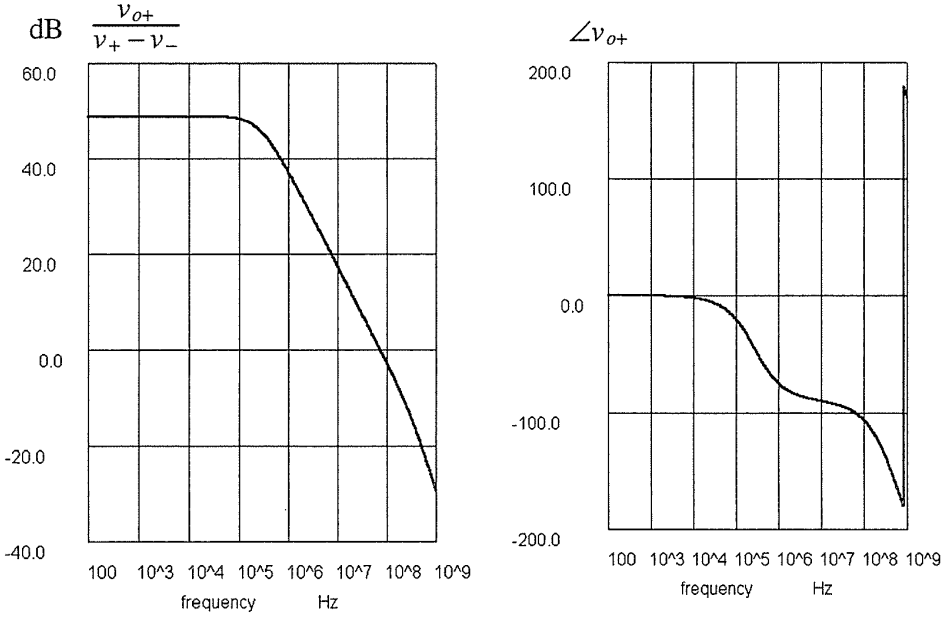


Figure 25.71 Simulation results of OTA shown in Fig. 25.57 using 1000/2 devices.

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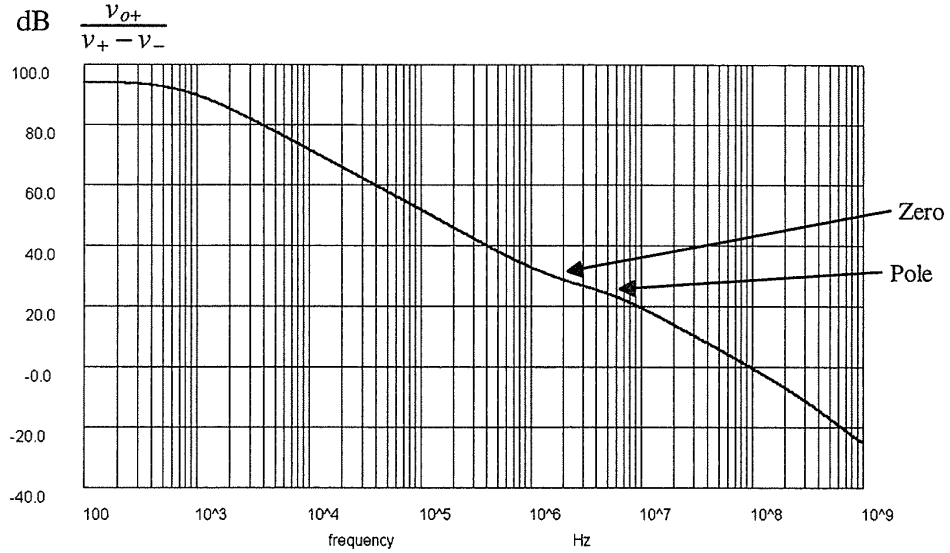


Figure 25.72 Simulation of uncompensated OTA shown in Fig. 25.69 using 1000/2 devices. (This OTA is stable without a compensation capacitor.)

The gain of this OTA can be increased using the gain-enhancement technique shown in Fig. 25.69. With gain enhancement we would expect the low-frequency gain to become 48 dB + 47 dB (the gain of the OTA of Fig. 25.30), or 95 dB. The open-loop, uncompensated gain of the gain-enhanced OTA is shown in Fig. 25.72.

Several characteristics of this plot deserve comment. First, the OTA used to enhance the gain, Fig. 25.30, does not need to be a wide-bandwidth stage. In fact, as long as its unity gain frequency is greater than the nonenhanced 3-dB bandwidth of the main OTA (simulation results shown in Fig. 25.71), the added OTA will not affect the gain. In other words, the OTA of Fig. 25.30 with 2.1 pF compensation capacitor has an f_u of 2.3 MHz. As long as the 3-dB bandwidth of the folded-cascode OTA without enhancement is smaller than 2.3 MHz, the added OTA will not affect the low-frequency gain. From Fig. 25.71 the 3-dB frequency of the nonenhanced OTA is approximately 200 kHz, which is less than the 2.3 MHz (f_u) of the added OTA.

Next we should notice that a pole and zero occur at almost the same frequency. This is called a doublet [10]. Although the phase margin is not degraded from the presence of this doublet, the settling time can be affected. With the use of gain enhancement, the settling time is improved (shortened). The feedback loop formed with the added OTA helps to decrease the time it takes the error signal to propagate back through the overall amplifier. Since the added OTAs form localized feedback loops on the outputs of the amplifiers, the error signal can get fed back with less delay. Adding the compensation capacitor of 5 pF to the gain-enhanced OTA gives the simulation results shown in Fig. 25.73. Keeping in mind that this op-amp was designed with a 2 μm process, we see that the results are impressive: a low-frequency gain of 94 dB (50,000) and a unity gain frequency of 30 MHz.

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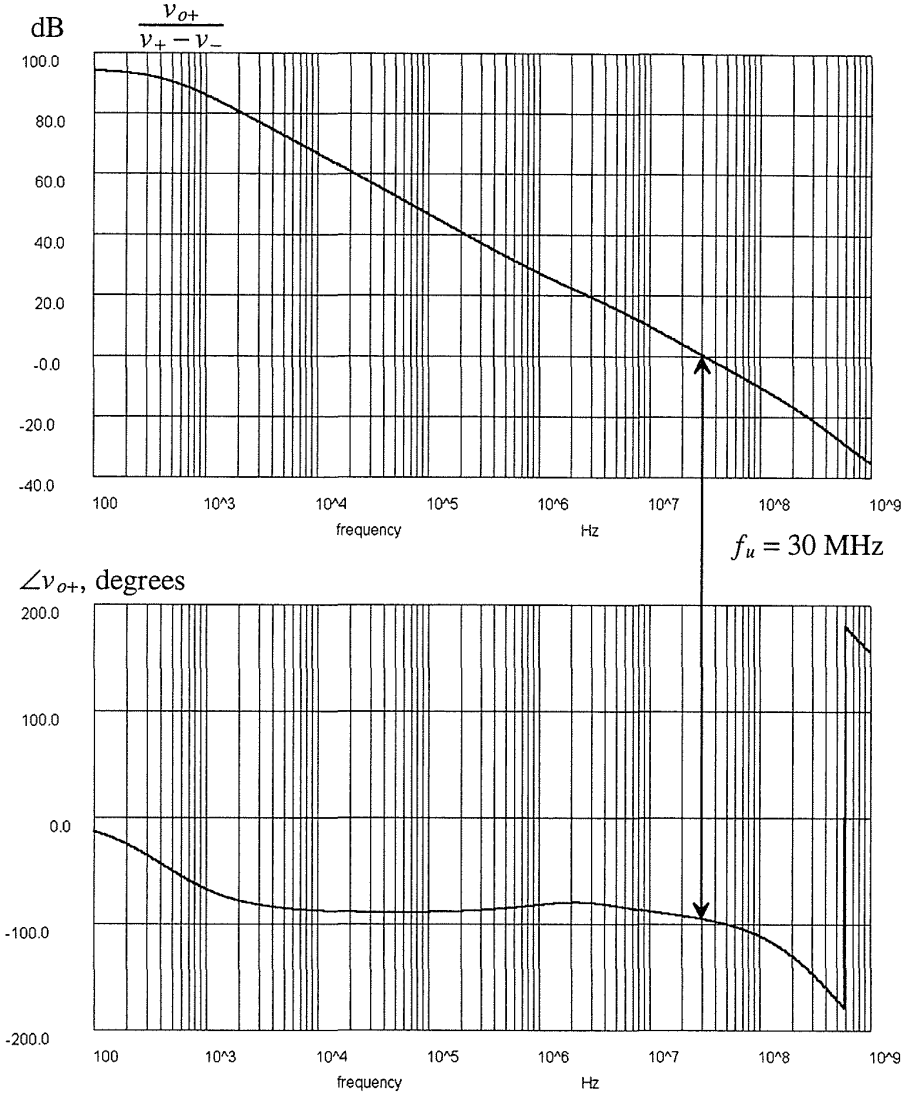


Figure 25.73 Simulation results of the fully differential OTA of Fig. 25.69 (see text for description).

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PROBLEMS

25.1 Calculate the gain of the op-amp shown in Fig. 25.3 if the resistor is replaced with a 1 μA current source.

25.2 Determine the maximum output source and sink currents for the op-amp of Fig. 25.11 for a maximum V_{GS} (of M9) or V_{SG} (of M10) of 1.5 V.

25.3 Referring to the op-amp of Fig. 25.11, determine the small-signal resistance looking into

(a) the sources of M1 and M2 (neglect body effect)

(b) the drain of M6

(c) the source of M7

(d) the drains of M1 and M2

(e) the sources of M9 and M10 (neglect body effect).

25.4 What is the small-signal resistance to ground at the drains of M1/M3, M4/M2, and M7/M91 in Fig. 25.11?

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25.5 If the drain current of M6, in Fig. 25.11, is reduced to 5 μA, what are the drain currents in M3, M4, M7, and M9?

25.6 If width of M7, in Fig. 25.11, is increased to 140 μm, how would M8 be resized? With these sizes, what quiescent current would flow in M9 and M10?

25.7 Derive Eq. (25.24).

25.8 Assume that an op-amp is needed that will always be used with feedback to get a gain of ten. Suggest a modification to Eq. (25.13) for compensating this op-amp. Suggest a circuit configuration, based on Fig. 25.7, that will allow simulating the stability of the op-amp.

25.9 Simulate the operation of the op-amp of Fig. 25.11 with SPICE and verify the results shown in Fig. 25.12.

25.10 Simulate the operation of the op-amp of Fig. 25.11 and determine the input offset voltage, the output voltage swing, the CMRR, the power dissipation, PSRR, and the slew-rate limitations.

25.11 If the OTA of Fig. 25.22 is made using 15/5 n-channels, 70/5 p-channels, and biased with a 10 μA current source, determine the small-signal, low-frequency gains $i_{out}/(v_{I2} - v_{I1})$ and $v_{out}/(v_{I2} - v_{I1})$.

25.12 Repeat Ex. 25.1 if the bottom of the 100k resistor in Fig. 25.24 is connected to –2.5 V.

25.13 Repeat Ex. 25.2 using the high-pass transconductor-C filter shown in Fig. 25.27. The capacitor value remains 8.75 pF.

25.14 If the OTA of Fig. 25.29 is made using 15/5 n-channels, 70/5 p-channels, and biased with a 10 μA current source, determine the small-signal, low-frequency gains $i_{out}/(v_{I2} - v_{I1})$ and $v_{out}/(v_{I2} - v_{I1})$.

25.15 If the minimum voltage across the current sources in Fig. 25.30 is 0.3 V, estimate the input CMR if $VDD = 5$ and $VSS = 0$.

25.16 Discuss, in your own words, the problems with compensating the OTA of Fig. 25.30.

25.17 Determine, using hand-calculations, the small-signal, low-frequency voltage gains of the OTA shown in Fig. 25.30 with V_{CM}= 0.8 V, 2.5 V, and 4.2V.

25.18 Redesign the regulator of Ex. 25.3 so that the output voltage is 2.0 V. Show all hand calculations, a schematic for your design, and estimate the phase margin.

25.19 If the 10 μA bias current of Fig. 25.42 is changed to 1 μA, what happens to the currents in the folded-cascode OTA? What is the small-signal voltage gain with 1 μA bias current?

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25.20 How can the biasing circuit of Fig. 25.44 be simplified? (Hint: Two of the MOSFETs are not necessary.)

25.21 Label the DC biasing currents on the schematic of the wide-swing folded-cascode OTA of Fig. 25.45 if the biasing circuit of Fig. 25.44 is used with I = 1 μA, MB1 is sized 15/20, MB2 is sized 35/10, and all other MOSFETs are sized 70/5 (p-channels) and 15/5 (n-channels).

25.22 Estimate the small-signal gains, i_{out}/v_{in} and v_{out}/v_{in},of the OTA described in Problem 25.21. What size of load capacitance would be needed to compensate the op-amp for an f_u of 1 MHz?

25.23 Design an output buffer for the OTA of Problem 21 that can source or sink 100 μA. Assume, for your design, that $VDD = -VSS = -2.5$ V and that the output voltage swing is +/– 1 V.

25.24 Verify the operation of the op-amp design of Problem 25.21 with SPICE. Show a plot similar to Fig. 25.46 with the op-amp driving a 10k resistor. Using SPICE, the phase margin of your design with and without the 10k load resistor.

25.25 Figure P25.25 shows a floating current source made using MC1 and MC2. Determine the size of MC1/MC2 so that 30 μA flows in M5 and M9.

25.26 If the minimum voltage between the drain and source of any MOSFET in Fig. 25.49 is 0.4 V, estimate the minimum *VDD* possible for the op-amp assuming $VSS = 0$. Comment on the problems of operating the op-amp at this voltage.

25.27 Discuss the purpose of the CMFB circuit in differential input/output op-amps.

25.28 Determine the CMR of the CMFB circuit of Fig. 25.58. For the CMFB circuit of Fig. 25.59, does the CMR of the diff-amp affect the operation of the circuit? Why or why not?

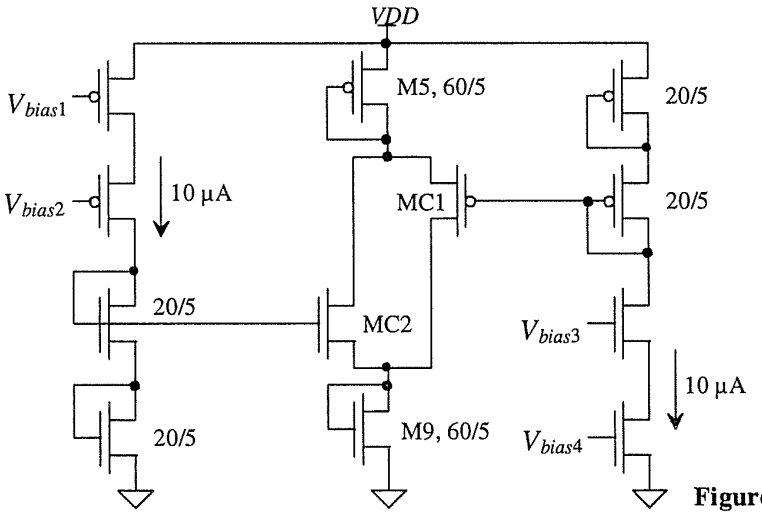


Figure P25.25

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Part
IV

Mixed-Signal Circuits

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Chapter

26

Nonlinear Analog Circuits

The past six chapters have presented the design of linear analog circuits, circuits whose input signals are linearly related to the circuits' output signals. In this chapter, we discuss several circuits that are not purely analog or digital. We term these circuits *nonlinear analog circuits* (the inputs are not linearly related to the outputs). In particular, we will discuss voltage comparator analysis and design, adaptive biasing, and analog multiplier design.

26.1 Basic CMOS Comparator Design

The schematic symbol and basic operation of a voltage comparator are shown in Fig. 26.1. The comparator can be thought of as a decision-making circuit. If the +, v_+, input of the comparator is at a greater potential than the –, v_- , input, the output of the comparator is a logic 1, whereas if the + input is at a potential less than the – input, the output of the comparator is at a logic 0. Although the basic op-amp of the last chapter can be used as a voltage comparator, in some less demanding low-frequency or speed applications, we will not consider the op-amp as a comparator. Instead, we will discuss practical comparator design and analysis where propagation delay and sensitivity are important.

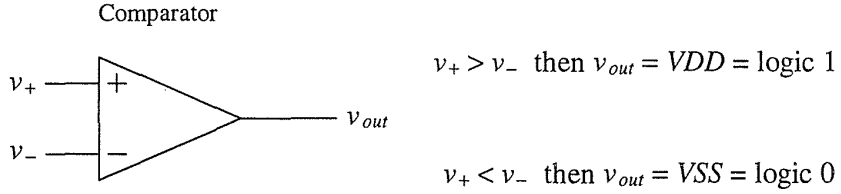


Figure 26.1 Comparator operation.

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A block diagram of a high-performance comparator is shown in Fig. 26.2. The comparator consists of three stages; the input preamplifier, a positive feedback or decision stage, and an output buffer. The preamp stage (or stages) amplifies the input signal to improve the comparator sensitivity (i.e., increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise coming from the positive feedback stage (*this is important*). The positive feedback stage is used to determine which of the input signals is larger. The output buffer amplifies this information and outputs a digital signal. Designing a comparator can begin with considering input common-mode range, power dissipation, propagation delay, and comparator gain. We will develop a basic comparator design using a procedure similar to the last chapter's development of the basic op-amp.

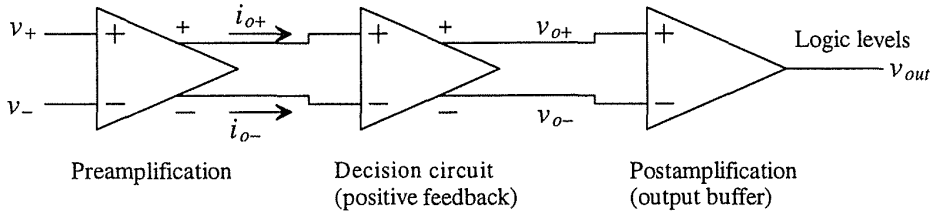


Figure 26.2 Block diagram of a voltage comparator.

Preamplification

For the preamplification stage, we chose the circuit of Fig. 26.3. This circuit is a differential amplifier with active loads. The sizes of M1 and M2 are set by considering the diff-amp transconductance and the input capacitance. The transconductance sets the gain of the stage, while the input capacitance of the comparator is determined by the size of M1 and M2. We will concentrate on speed in this design, and therefore we will set the channel lengths of the MOSFETs to 2 μm. (Channel length modulation gives rise to an unwanted offset voltage.) Notice that there are no high-impedance nodes in this circuit, other than the input and output nodes. Using the sizes given in the schematic, we can relate the input voltages to the output currents by

$$i_{o+} = \frac{g_m}{2}(v_+ - v_-) + \frac{I_{SS}}{2} = I_{SS} - i_{o-} = 20\ \mu\text{A} - i_{o-} \tag{26.1}$$

where, for the present case,

$$g_m = g_{m1} = g_{m2} = \sqrt{2\frac{10}{2} \cdot 50\frac{\mu\text{A}}{\text{V}^2} \cdot 10\mu\text{A}} = 71\ \frac{\mu\text{A}}{\text{V}} \tag{26.2}$$

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In other words, if v_+ is 10 mV greater than v_-, the output currents, i_{o+} and i_{o-}, are 10.35 μA and 9.65 μA, respectively. To further increase the gain of the first stage, we can size up the widths of MOSFETs M3 and M4 relative to the widths of M31 and M41.

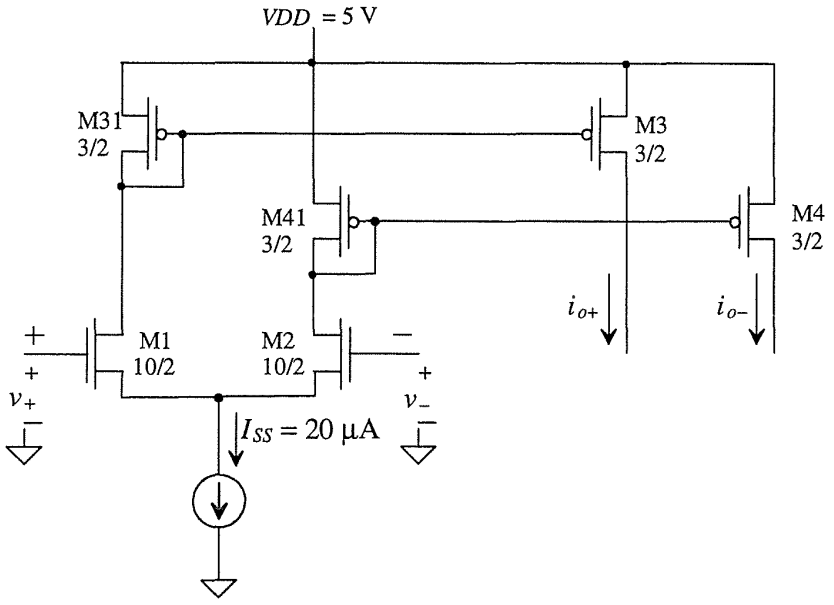


Figure 26.3 Preamplification stage of comparator.

Decision Circuit

The decision circuit is the heart of the comparator and should be capable of discriminating mV level signals. We should also be able to design the circuit with some hysteresis (see Ch. 18) for use in rejecting noise on a signal. The circuit used in the present comparator is shown in Fig. 26.4 [1]. The circuit uses positive feedback from the cross-gate connection of M6 and M7 to increase the gain of the decision element.

Let's begin by assuming that i_{o+} is much larger than i_{o-} so that M5 and M7 are on and M6 and M8 are off. We will also assume that $\beta_5 = \beta_8 = \beta_A$ and $\beta_6 = \beta_7 = \beta_B$. Under these circumstances, v_{o-} is approximately 0 V and v_{o+} is

$$v_{o+} = \sqrt{\frac{2i_{o+}}{\beta_A}} + V_{THN} \tag{26.3}$$

If we start to increase i_{o-} and decrease i_{o+}, switching takes place when the drain-source voltage of M7 is equal to V_{THN} of M6. At this point, M6 starts to take current away from M5. This decreases the drain-source voltage of M5 and thus starts to turn M7 off. If we assume that the maximum value of v_{o+} or v_{o-} is equal to $2V_{THN}$, then M6 and M7 operate,

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$\beta_A = \beta_5 = \beta_8$

$\beta_B = \beta_6 = \beta_7$

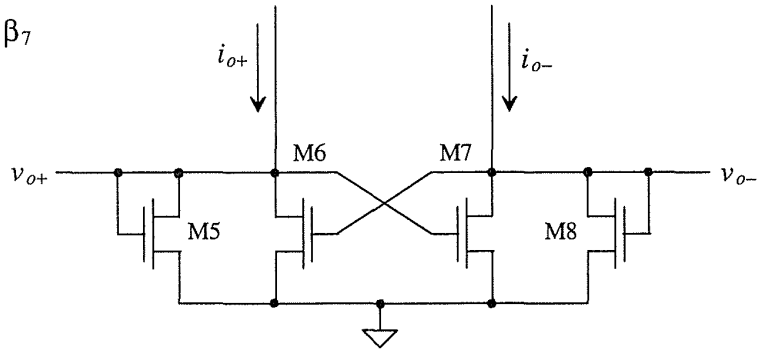


Figure 26.4 Positive feedback decision circuit.

under steady-state conditions, in either cutoff or the triode regions. Under these circumstances, the voltage across M7 reaches V_{THN}, and thus M7 enters the saturation region, when the current through M7 is

$$i_{o-} = \frac{\beta_B}{2}(v_{o+} - V_{THN})^2 = \frac{\beta_B}{\beta_A} \cdot i_{o+} \tag{26.4}$$

This is the point at which switching takes place; that is, M7 shuts off and M6 turns on. If $\beta_A = \beta_B$, then switching takes place when the currents, i_{o+} and i_{o-}, are equal. Unequal βs cause the comparator to exhibit hysteresis. A similar analysis for increasing i_{o+} and decreasing i_{o-} yields a switching point of

$$i_{o+} = \frac{\beta_B}{\beta_A} \cdot i_{o-} \tag{26.5}$$

Relating these equations to Eq. (26.1) yields the switching point voltages (review Ch. 18), or

$$V_{SPH} = v_+ - v_- = \frac{I_{SS}}{g_m} \cdot \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1} \text{ for } \beta_B \geq \beta_A \tag{26.6}$$

and

$$V_{SPL} = -V_{SPH} \tag{26.7}$$

For the present design under development, we will use 3 μm and 2 μm device widths and lengths (no hysteresis and the offset voltage is not important).

Example 26.1

For the circuit shown in Fig. 26.5, estimate and simulate the switching point voltages for two designs: (1) $W_5 = W_6 = W_7 = W_8 = 3$ μm with $L = 2$ μm and (2) $W_5 = W_8 = 3$ μm and $W_6 = W_7 = 4$ μm with $L = 2$ μm.

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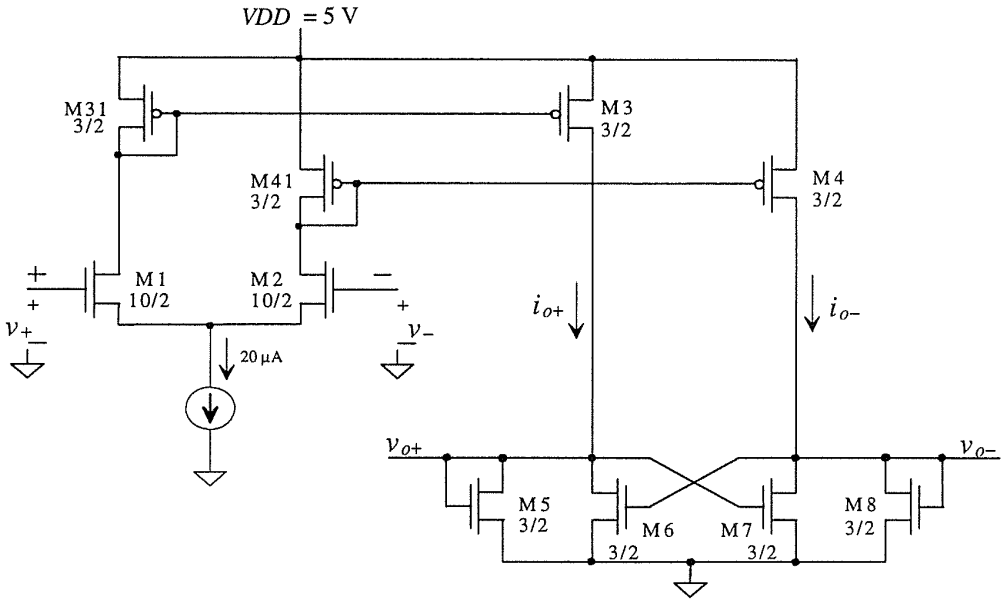


Figure 26.5 Schematic of preamp and decision circuit.

For the first case

$$\beta_A = \beta_B = 50 \frac{\mu A}{V^2} \cdot \frac{3\ \mu m}{2\ \mu m}$$

so that $V_{SPH} = V_{SPL} = 0$. In other words, the comparator does not exhibit hysteresis.

Simulation results are shown in Fig. 26.6. The input v_- is set to 2.5 V while the input v_+ is swept from 2.0 to 3.0 V. Note that the amplitudes of v_{o+} and v_{o-} are limited to approximately $2V_{THN}$.

For the second case

$$\beta_A = 50 \frac{\mu A}{V^2} \cdot \frac{3\ \mu m}{2\ \mu m} \text{ and } \beta_B = 50 \frac{\mu A}{V^2} \cdot \frac{4\ \mu m}{2\ \mu m}$$

or $\beta_B = 1.33\beta_A$. Using Eqs. (26.6) and (26.7) with $I_{SS} = 20$ μA and $g_m = 71$ μA/V, we get

$$V_{SPH} = -V_{SPL} = 40 \text{ mV}$$

The simulation results are shown in Fig. 26.7. Fig. 26.7a shows a sweep of v_+ from 2.4 to 2.6 V, with v_- held at 2.5 V. Since V_{SPH} is 40 mV the decision circuit switches states when v_+ is 40 mV above v_- (i.e. when $v_+ = 2.54$ V). The case of v_+ being swept from 2.6 to 2.4 V is shown in part (b) of the figure. Switching occurs in this situation when $v_+ = 2.46$ V, or 40 mV less than 2.5 V. ■

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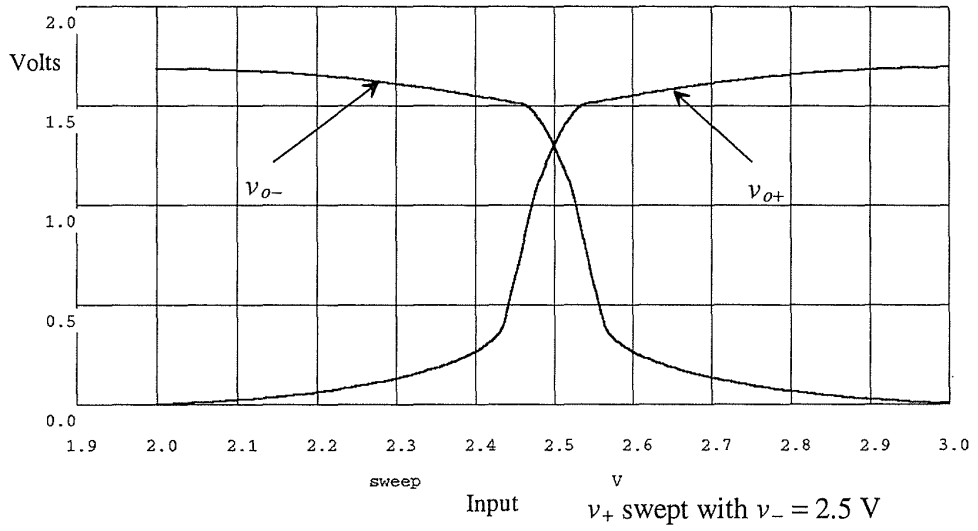


Figure 26.6 Simulation results for case 1 of Ex. 26.1.

Output Buffer

The final component in our comparator design is the output buffer or postamplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or 5 V). The output buffer should accept a differential input signal and not have slew-rate limitations.

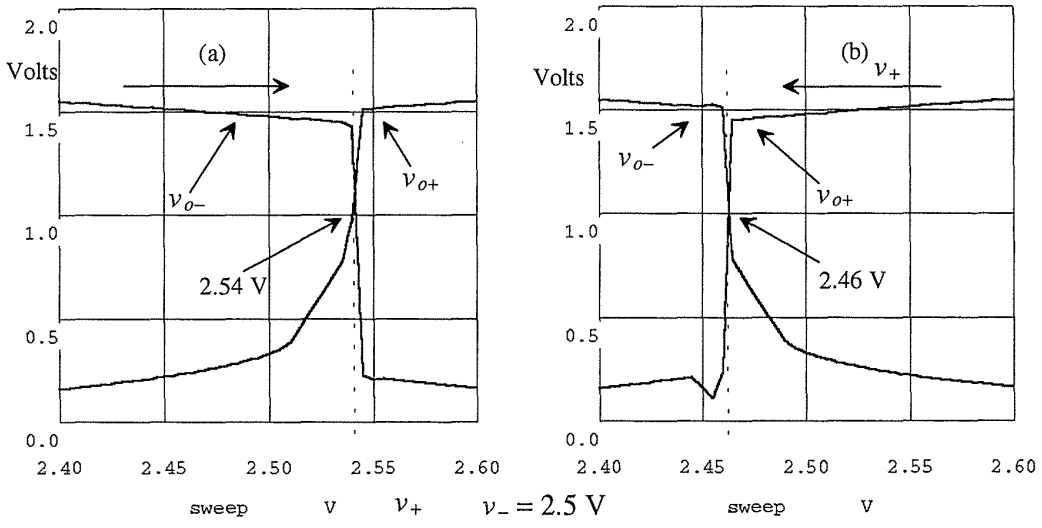


Figure 26.7 Simulation results for case 2 of Ex. 26.2.

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The circuit used as an output buffer in our basic comparator design is shown in Fig. 26.8. This circuit is a self-biasing differential amplifier [2]. An inverter was added on the output of the amplifier as an additional gain stage and to isolate any load capacitance from the self-biasing differential amplifier. A DC sweep of this amplifier configuration is shown in Fig. 26.9. The input v_{o+} is swept from 1 to 4 V, while v_{o-} is held at 1 to 3.5 V in 0.5 V increments. It is apparent that the inputs, v_{o+} and v_{o-}, should lie within 1.5 and 3 V for linear operation of the output buffer. Comparing this result with the output of the positive feedback circuit, which varies from 0 to 1.5 V, we see a problem in connecting the decision circuit directly to the output buffer. To shift the output of the decision circuit up approximately 1 V, the circuit of Fig. 26.10 is used. The MOSFET M17 is added in series with the decision circuit to increase the average voltage out of the decision circuit. The size of the MOSFET is somewhat arbitrary. We will set W_{17}/L_{17} = 100 μm/2 μm so that the output of the decision circuit is increased by approximately V_{THN}. The complete schematic of the comparator is shown in Fig. 26.11. Unlabeled MOSFETs are 3 μm/ 2 μm.

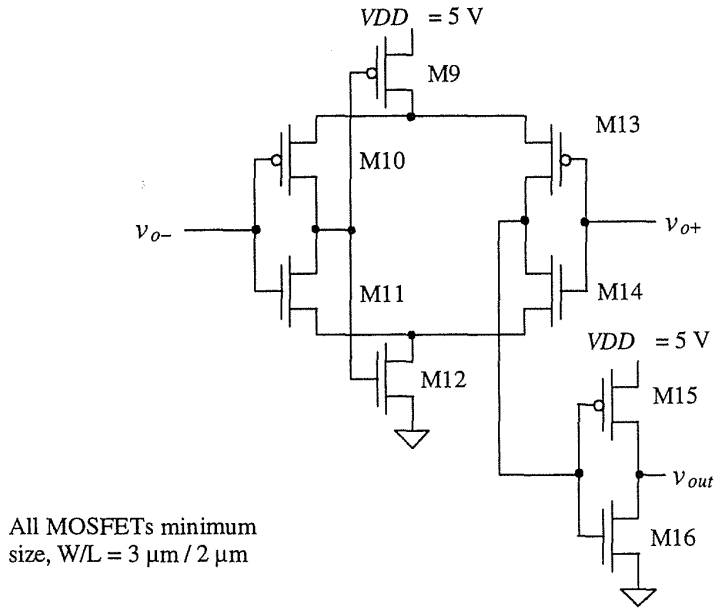


Figure 26.8 A self-biasing differential amplifier used as the comparator output buffer.

26.1.1 Characterizing the Comparator

Comparator Gain and Offset

With v_- held at 2.5 V, the v_+ input of the comparator is swept from 2.49 to 2.51 V, with the result shown in Fig. 26.12. An important parameter of a comparator is its offset voltage. From this figure we can see that the systematic offset voltage is approximately 1 mV. The next chapter will discuss dynamic methods of eliminating the offset voltage.

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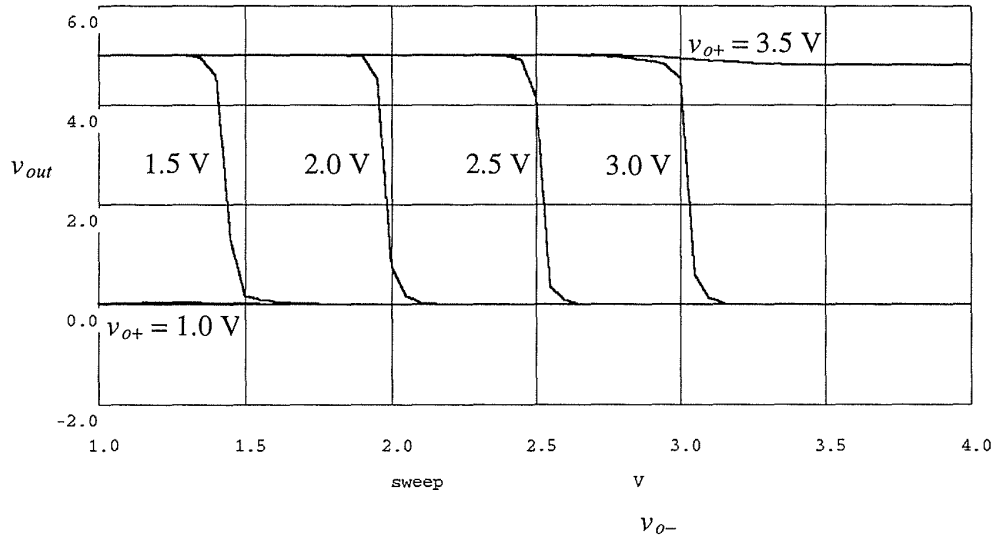


Figure 26.9 DC sweep of the self-biasing amplifier of Fig. 26.8.

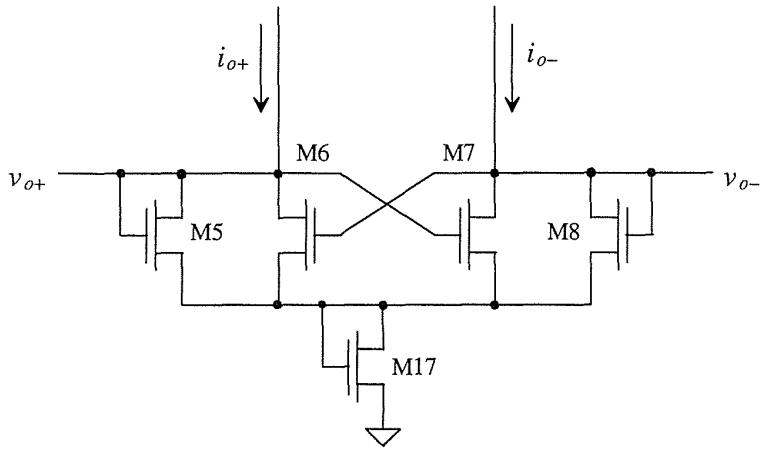


Figure 26.10 Use of a large MOSFET, M17, to level shift the output of the decision circuit.

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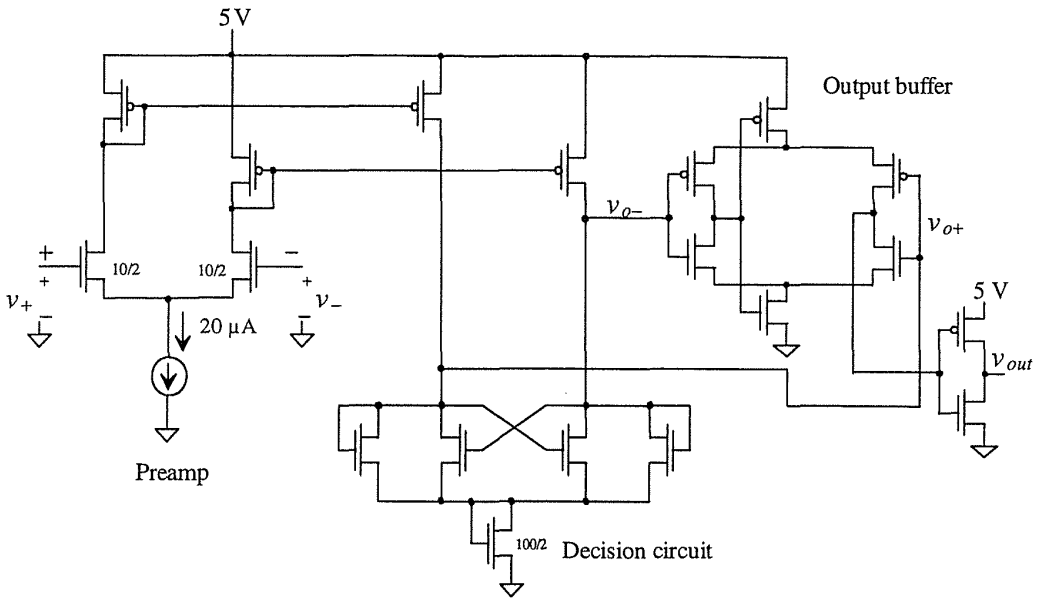


Figure 26.11 Complete schematic of comparator.

If we take the derivative of the transfer curves, the gain of the comparator and thus the smallest difference that can be discriminated between v_+ and v_- become known. Figure 26.13 shows the gain of the comparator at about 2,000 so that approximately 2.5 mV is needed to make the comparator output change logic levels. The comparator gain can be increased by increasing the transconductance of the preamp, that is, by increasing the widths of M1 and M2 or by adding additional inverters. Adding another gain stage to the preamp will also increase the comparator overall gain.

Transient Response

The transient response of a comparator can be significantly more difficult to characterize than the DC characteristics. Let's begin by considering v_- = 2.5 V DC, with the v_+ input to the comparator a 10 ns wide pulse and an amplitude varying from 2.49 to 2.51 V. This is termed a narrow pulse with a 10 mV overdrive; we are driving the + input of the comparator 10 mV over the negative input. The simulation results for these inputs are shown in Fig. 26.14. If the pulse amplitude or width is reduced much beyond this, the comparator does not make a full transition. Notice how the simulation starts at 200 ns.

Although these results are interesting, they are not practically useful in some situations. In few cases will the comparator discriminate a signal similar to that of Fig. 26.14a. A better indication of comparator performance is to apply a signal that starts at a voltage where one side of the differential amplifier is cut off and to finish at a voltage slightly larger than the reference voltage (2.5 V in the above example). Applying a 0 to 2.51 V pulse to the v_+ input will cause M1, M3, and M31 to be initially off and then

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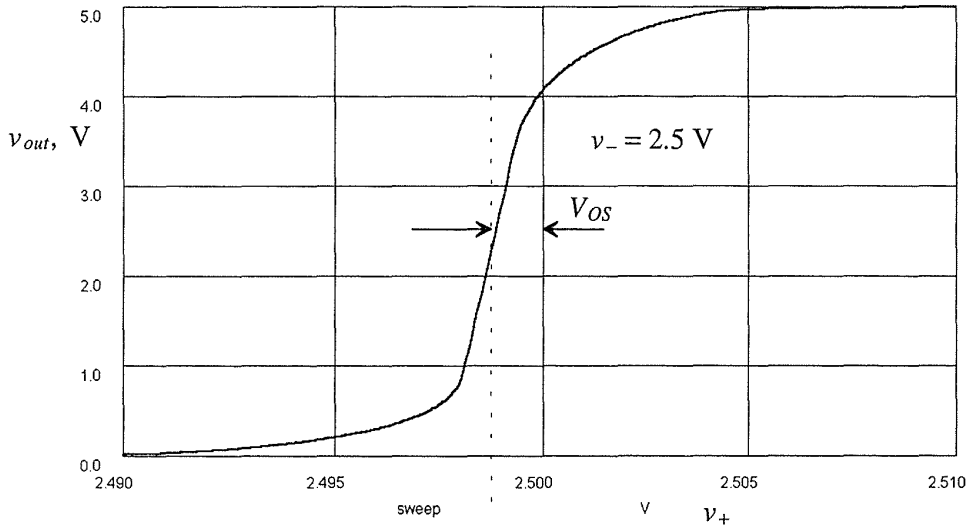


Figure 26.12 DC characteristics of the comparator of Fig. 26.11 with −input connected to 2.5 V.

turn on. The comparator nodes must be charged over a voltage range of 0 to 2.51 V input, wider than the 2.49 to 2.51 V example of Fig. 26.13. In order to keep one side of the preamp from turning off, the circuit of Fig. 26.15 can be used. The diode connected MOSFETs ensure that the voltage between the drains of M31 and M41 are always within a V_{THN} of one another. This configuration is sometimes referred to as a clamped input stage.

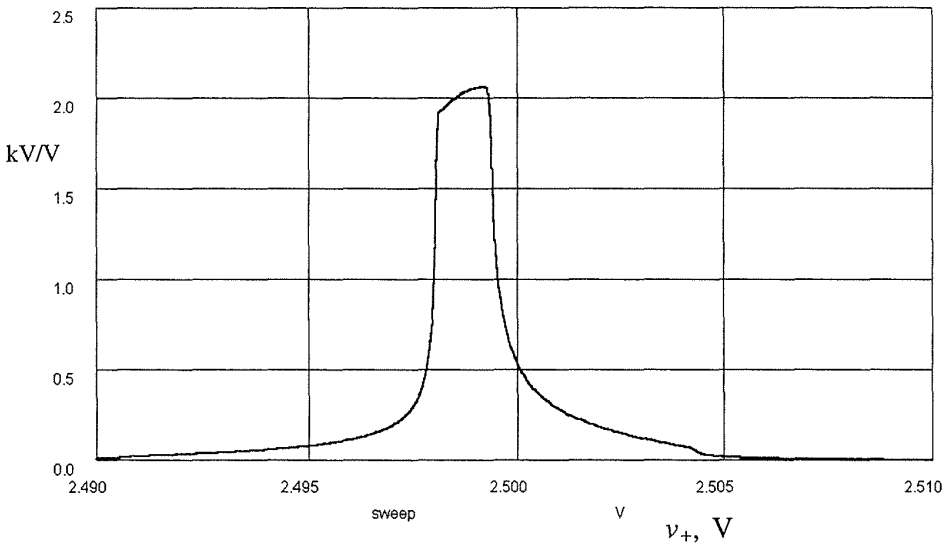


Figure 26.13 Comparator gain as a function of input voltage.

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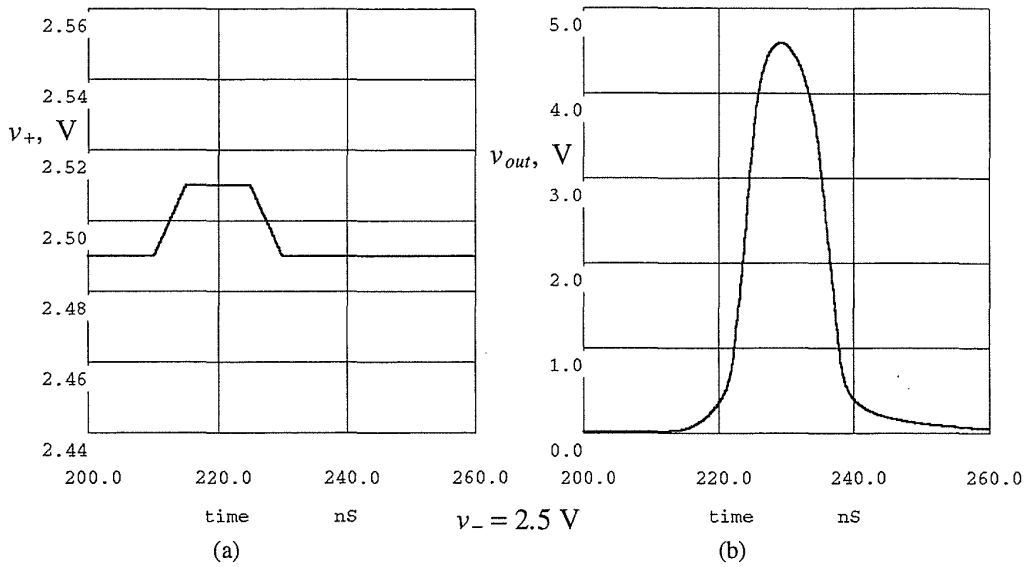


Figure 26.14 Comparator input (a) and corresponding output (b) Inverting input held at 2.5 V potential.

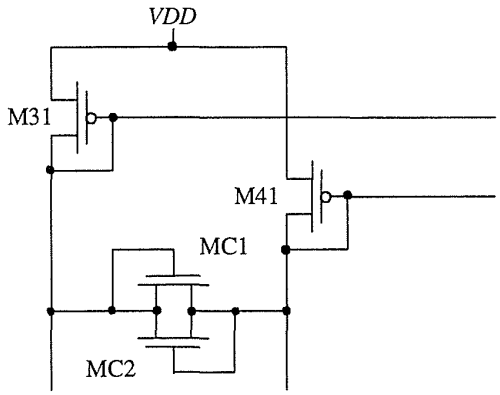


Figure 26.15 Using MOSFETs to keep active loads of preamp from shuting off.

Propagation Delay

Ideally, the propagation delay (the time difference between the input, v_+, crossing the reference voltage, v_-, and the output changing logic states) is zero. For the comparator of Fig. 26.11 with simulation results shown in Fig. 26.14, the delay of the comparator is approximately 10 ns (or less with an overdrive). This should be compared with the delay of an op-amp used as a comparator, which may be several hundred nanoseconds.

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Another interesting fact about comparator design is that the delay of a comparator can be reduced by cascading gain stages. In other words, the delay of a single high-gain stage is in general longer than the delay of several low-gain stages.

Minimum Input Slew Rate

The last characteristic we will discuss is the minimum input slew rate of a comparator. If the input signals to the comparator vary at a slow rate (e.g., a sine wave generated from the AC line), the output of the comparator may very well oscillate while the comparator is trying to decide what state it should be in. If a comparator is to be used with slow, varying signals or in a noisy environment, the decision circuit should have hysteresis. The minimum slew rate is difficult to simulate with SPICE because of the slow and fast varying signals present at the same instant of time.

Improvements in Sensitivity and Speed

Improvements in comparator sensitivity and speed can be directly related to improvements in the preamplifier. A derivation (similar to that given in Ch. 11 for minimum delay through an inverter string driving a load capacitance, C_L) of the number of stages, N, needed in a preamplifier to reach minimum delay for a given load capacitance and input capacitance results in

$$N = \ln \frac{C_L}{C_{in}} \tag{26.8}$$

In the derivation of this equation, it was assumed that the driving resistance of any stage is $1/g_{mn}$ (the transconductance of the nth differential amplifier stage). In practice, Eq. (26.8) is of little use because one side of the differential amplifier can be off. For this reason (and others such as size and power draw), comparators with more than two or three preamp stages are not common. Figure 26.16 shows a two-stage preamp with decision circuit.

Clocked Comparators

Figures 26.17 [3] and 26.18 [4] show two clocked comparators used in analog-to-digital converter design. The use of a clock pulse can greatly improve comparator performance and speed.

The clocked comparator shown in Fig. 26.17 is a clocked version of the comparator of Fig. 26.11. The use of a clock eliminates the need for an output buffer used in level shifting the output of the decision circuit. When $\overline{LATCH}$ is high, the comparator behaves like the preamp and decision circuit of Fig. 26.11. The output of the decision circuit is dependent on the input signals. When $\overline{LATCH}$ is taken low, ML1 shuts off, effectively latching the outputs at a logic high or low. That is, the comparator stops comparing and remembers the status of the inputs at the instant $\overline{LATCH}$ is switched low.

This comparator has the unwanted characteristic of continuously drawing power. Adding a MOSFET switch, similar to ML1 in series with the decision circuit, in series

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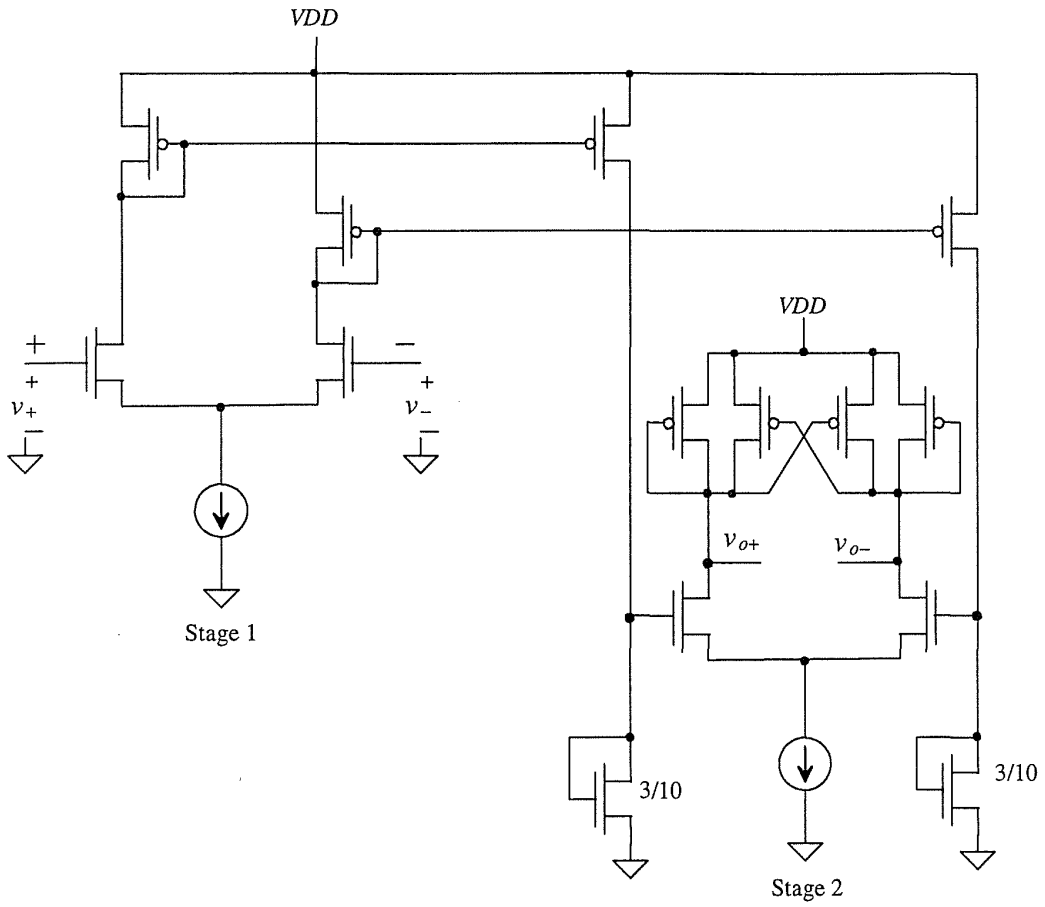


Figure 26.16 Two-stage preamp with decision circuit.

with the preamp current source can significantly reduce power draw. Under DC conditions, the comparator doesn't draw power when $\overline{LATCH}$ is low with this switch added.

The second clocked comparator design shown in Fig. 26.18 is based on the regenerative latch. Again, the comparator is made up of three stages: preamp, positive feedback decision circuit, and output buffers. The regenerative latch (cross-coupled inverters) is made up of M1 through M4. When *Latch* is low, the p-channels, M1 and M2, of the latch are isolated from the n-channels, M3 and M4. In addition, the outputs of the decision circuit are pulled high, that is, the outputs of the comparator are low, $Q = \overline{Q} = 0$. When *Latch* signal transitions high, the regenerative action of the latch combined with the preamplifier causes an imbalance in the decision circuit, forcing the outputs into a state determined by v_+ and v_-.

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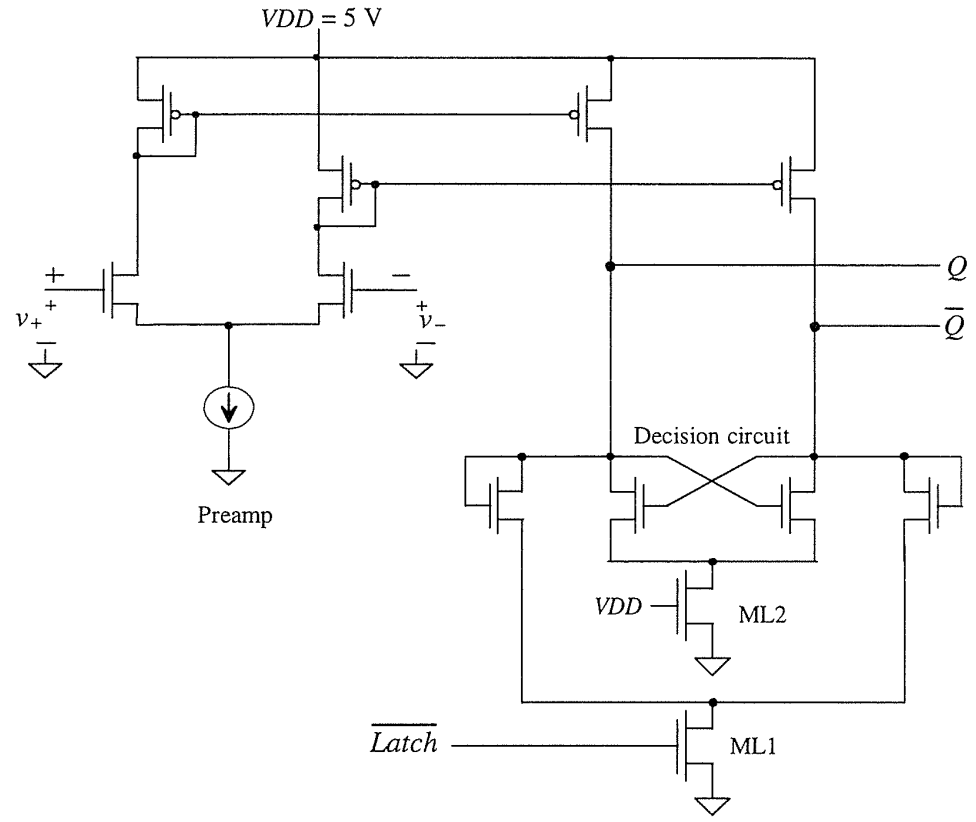


Figure 26.17 Clocked comparator.

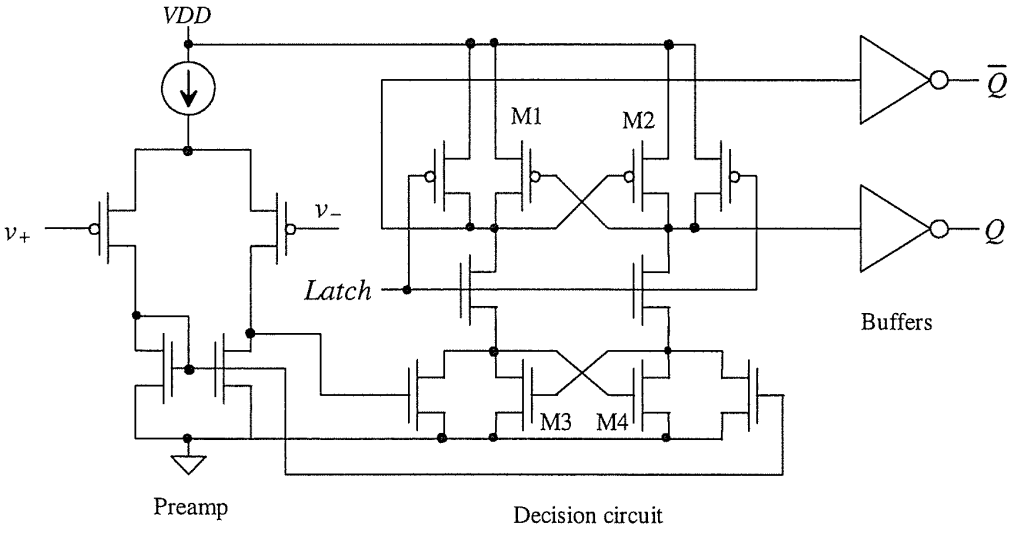


Figure 26.18 Clocked comparator based on the basic latch.

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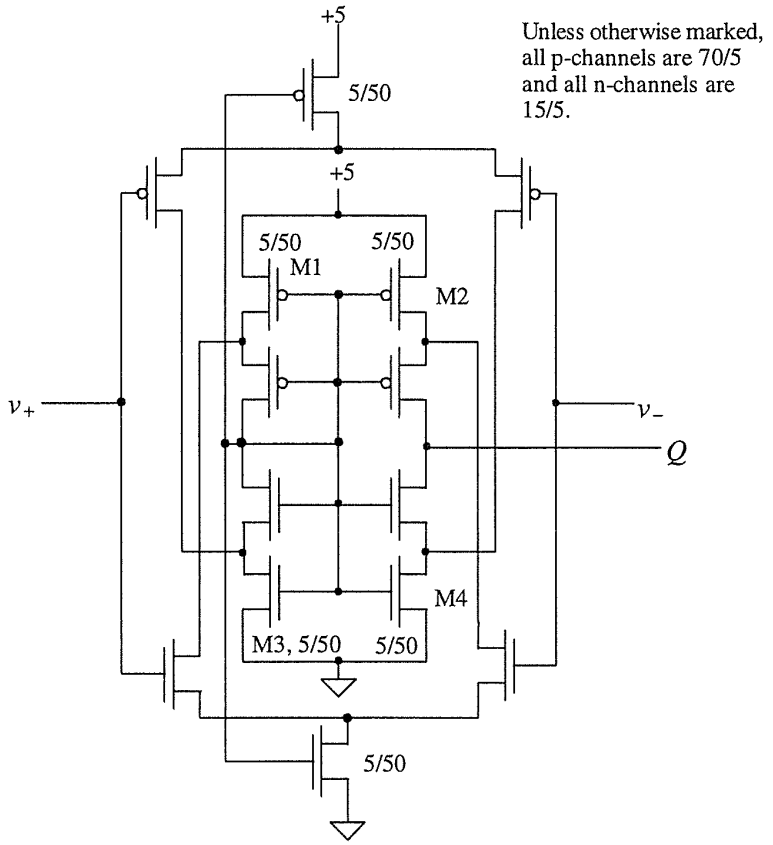


Figure 26.19 Self-biased comparator.

Self-Biasing Comparator

For the final example of a comparator, consider the self-biased comparator shown in Fig. 26.19 [2]. This circuit operates similar to the self-biased differential amplifier of Fig. 26.8 but with a larger gain and wider input common-mode range. The DC characteristics of the comparator are shown in Fig. 26.20. Note that because of the high gain of this comparator configuration, the delay tends to be longer (hundreds of ns) than the other configurations we discussed. The delay can be reduced, at the price of gain and more power dissipation, by decreasing the widths of M1 through M4 (operating M1 through M4 in the triode region) and by using minimum channel lengths.

26.2 Adaptive Biasing

Adaptive biasing can reduce power dissipation in an amplifier while at the same time increasing output current drive capability [5,6]. Figure 26.21 can be used to help illustrate the idea. When v_{I1} and v_{I2} are equal, the current sources I_{SS1} and I_{SS2} are zero (an open). The diff-amp DC tail current is simply I_{SS}, the same as an ordinarily biased

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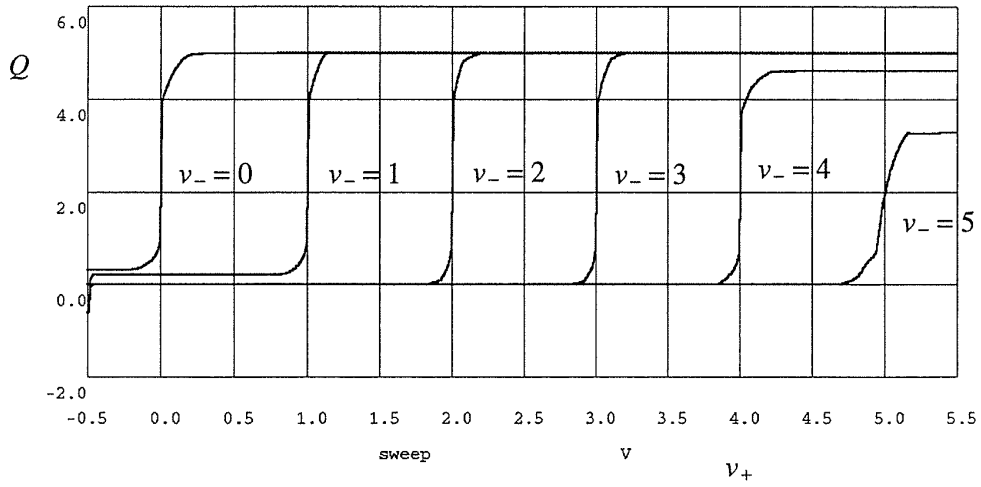


Figure 26.20 DC sweep for the self-biased comparator of Fig. 26.19.

If $v_{I1} = v_{I2}$ then $I_{SS1} = I_{SS2} = 0$.

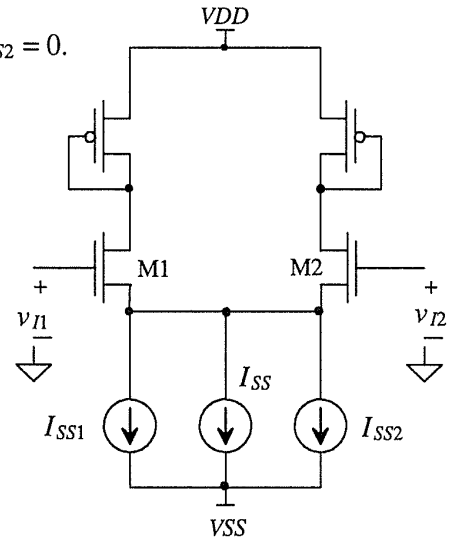


Figure 26.21 Adaptively biased diff-amp.

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diff-amp. If v_{I1} becomes larger than v_{I2}, the current source I_{SS1} increases above zero, effectively increasing the diff-amp DC bias current. Similarly, if v_{I2} becomes larger than v_{I1}, the current source I_{SS2} increases above zero. The diff-amp output current is normally limited to I_{SS} when one side of the diff-amp shuts off. However, now the maximum output current is limited to either $I_{SS} + I_{SS1}$ or $I_{SS} + I_{SS2}$. Power dissipation can be reduced using an adaptive bias, and slew-rate problems can be eliminated.

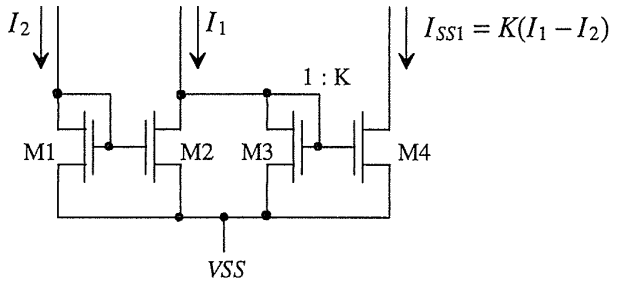


Figure 26.22 Current diff-amp used in adaptive biasing.

The current diff-amp of Fig. 26.22 can be used to implement the current source I_{SS1} or I_{SS2}. If the currents I_1 and I_2 are equal, then zero current flows in M3 and M4. Also, if I_2 is greater than I_1, zero current flows in M3 and M4. If I_1 is larger than I_2, the difference between these two currents $(I_1 - I_2)$ flows in M3. Since M4 is K times wider than M3, a current of $K(I_1 - I_2)$ flows in M4 (normally $K < 1$). Two of these diff-amps are needed to implement the adaptive biasing of the diff-amp of Fig. 26.21.

Figure 26.23 shows the implementation of adaptive biasing into the diff-amp of Fig. 26.21. P-channel MOSFETs are added adjacent to M3 and M4 to mirror the currents through M1 and M2 (I_1 and I_2). The maximum total current available through M1 occurs when M2 is off. Positive feedback exists through the loop M1, M3, M5-M7. Initially, when M2 shuts off, the current in M1 and M3 is I_{SS}. This is mirrored in M5 and M6, and thus I_{SS1} becomes $K \cdot I_{SS}$. At this particular instance in time, the tail current, which flows through M1, is now $I_{SS} + K \cdot I_{SS}$. However, provided the MOSFETs M1, M3 - M7 remain in saturation, this current circles back around the positive feedback loop and increases by K. This continues, resulting in a final or total tail current of

$$I_{tot} = I_{SS} \cdot (1 + K + K^2 + K^3 + \ldots) \tag{26.9}$$

If $K < 1$, this geometric series can be written as

$$I_{tot} = \frac{I_{ss}}{1 - K} \tag{26.10}$$

Setting $K = 0$ (MOSFET M7 doesn't exist) results in no adaptive biasing and a total tail current of I_{SS}. Setting $K = 1/2$ (M7 half the size of M6) results in a total available tail current of $2 \cdot I_{SS}$. Since the tail current limits the slew rate, when the diff-amp is driving

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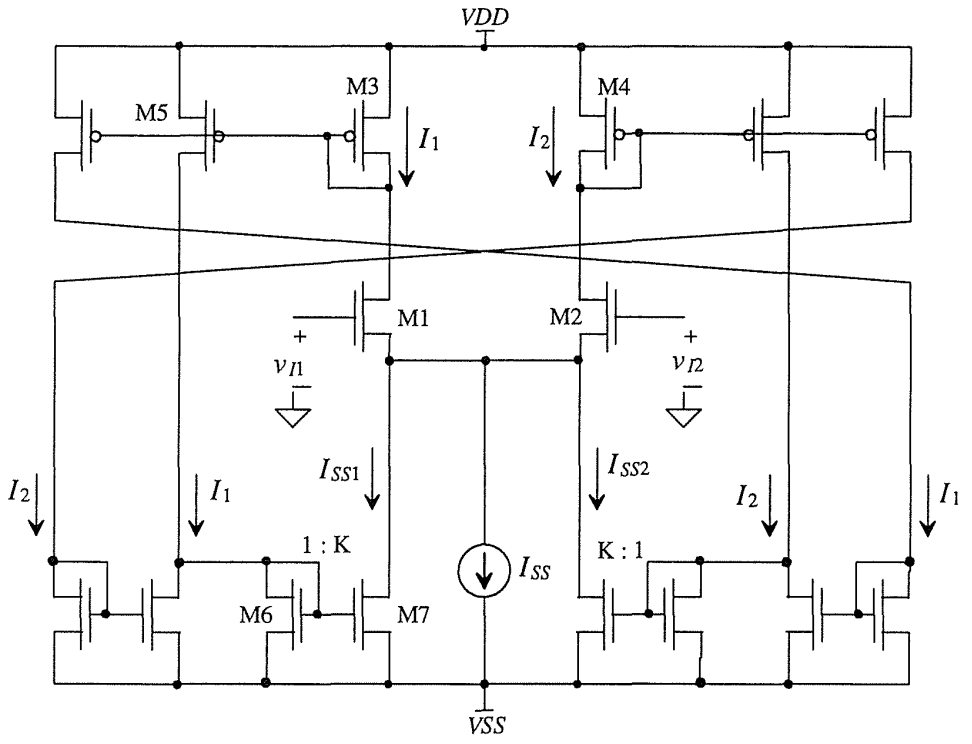


Figure 26.23 Adaptively biased diff-amp.

a capacitive load, making K equal to one eliminates slew-rate limitations while at the same time not increasing static power dissipation. In practice, shuting off one side of the diff-pair, M1/M2, is difficult since the adaptive biasing has the effect of lowering the source potentials of the diff-pair, keeping both MOSFETs on. Adaptive biasing can be used in a comparator where M1 or M2 can shut off. However, the static power dissipation will be large, and therefore there is no benefit over the comparators discussed earlier in the chapter. When applying adaptive biasing to an OTA design, the value of K should be unity or less. [Using a K of 1 or 2 can still result in a finite I_{tot} since the MOSFETs have a finite output resistance and since the MOSFETs in the diff-pair will not shut off, as was assumed in the derivation of Eq. (26.10)]. An adaptively biased OTA is shown in Fig. 26.24 [5].

A final example of an adaptive voltage-follower amplifier is shown in Fig. 26.25 [6]. This amplifier can only source current to a load. If v_{in} and v_{out} are equal, the current that flows in M1 and M2 is $I_{SS} + I_{D6}$. If v_{in} is increased, the current in M1 and M3 increases. This causes the currents in M4 - M6 to increase, effectively increasing the tail current of the diff-pair. The result is a large current available to drive the load. Note that M7 can be sized larger than the other MOSFETs to increase maximum output current.

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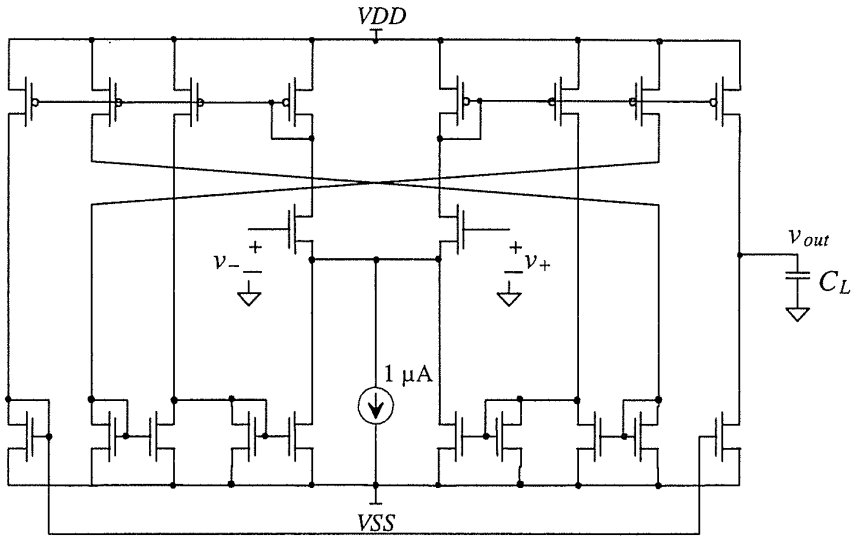


Figure 26.24 Adaptively biased OTA [5].

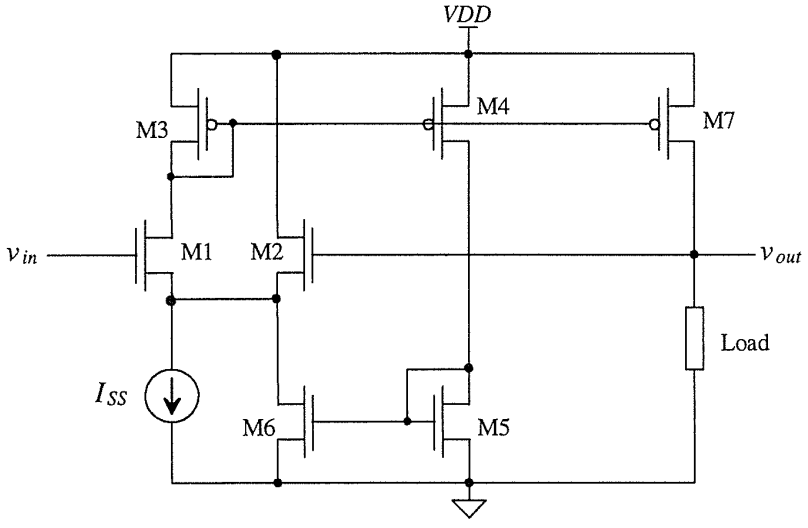


Figure 26.25 Adaptive voltage follower [6].

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26.3 Analog Multipliers

Analog multipliers find extensive use in communication systems. Figure 26.26 shows the voltage characteristics of a four-quadrant multiplier [7]. This multiplier is termed a four-quadrant multiplier because both inputs can be either positive or negative. The ideal output of the multiplier is related to the inputs by

$$v_{out} = K_m \cdot v_x v_y \tag{26.11}$$

where K_m is the multiplier gain with units of V^{-1}. In reality, imperfections exist in the multiplier gain, resulting in offsets and nonlinearities. The output of the multiplier can be written as [7]

$$v_{out} = K_m(v_x + V_{OSx})(v_y + V_{OSy}) + V_{OSout} + v_x^n + v_y^m \tag{26.12}$$

where V_{OSx}, V_{OSy}, and V_{OSout} are the offset voltages associated with the x-, y-inputs, and the output, respectively. The terms v_x^n and v_y^m represent nonlinearities in the multiplier. Normally, these nonlinearities are specified in terms of the total harmonic-distortion or

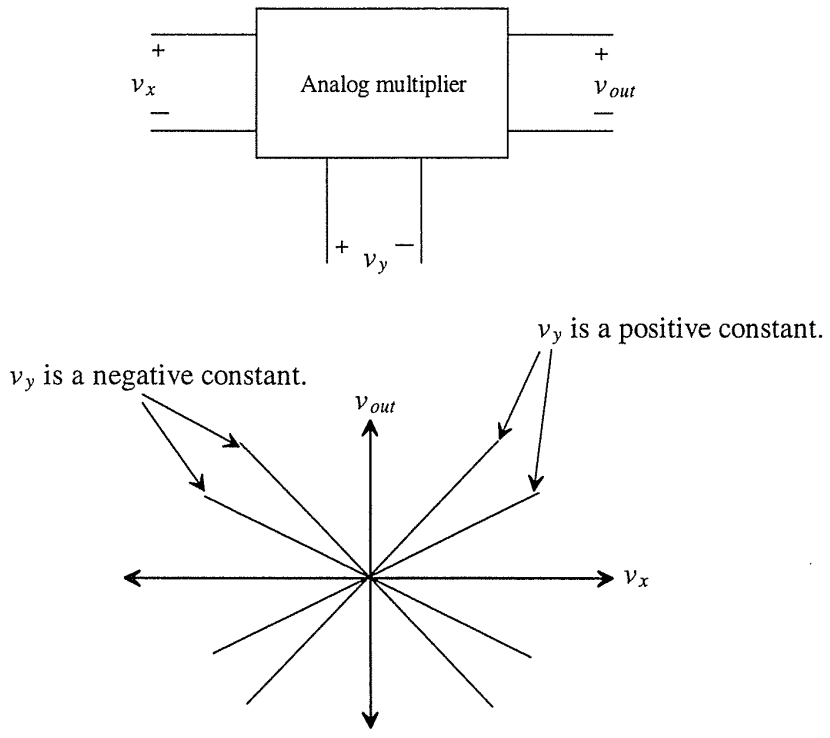


Figure 26.26 Operation of a four-quadrant analog multiplier.

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by specifying the maximum deviation in percentages between a straight line and the actual characteristic curves shown in Fig. 26.26 over some range of input voltages.

Although many different techniques exist for implementing analog multipliers in CMOS [8], we will concentrate on a technique useful in high- and low-frequency multiplication [9, 10].

26.3.1 The Multiplying Quad

A CMOS multiplier employing a multiplying quad (M1 - M4) is shown in Fig. 26.27. The multiplying quad operates in the triode region, and thus MOSFETs M1-M4 can be thought of as resistors. For the moment we will not consider the biasing of the quad. The negative output voltage of the multiplier is given by

$$v_{o-} = -R \cdot (i_{D1} + i_{D2}) \tag{26.13}$$

while the positive output voltage is

$$v_{o+} = -R \cdot (i_{D3} + i_{D4}) \tag{26.14}$$

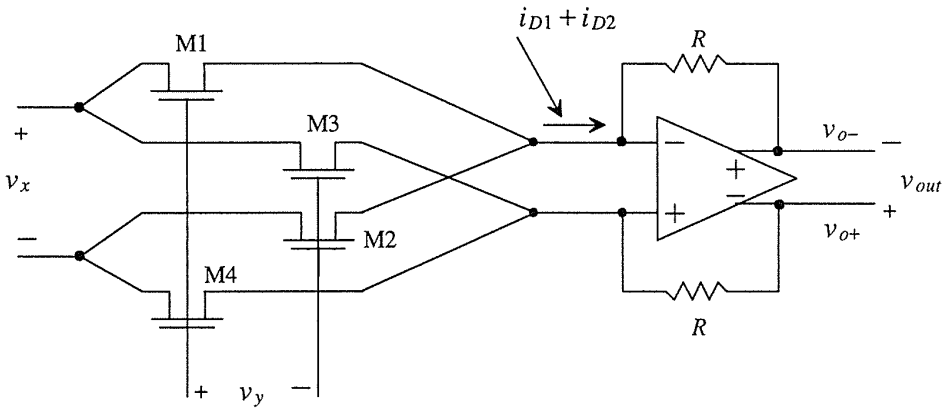


Figure 26.27 CMOS analog multiplier.

The output voltage of the multiplier is

$$v_{out} = v_{o+} - v_{o-} = R \cdot (i_{D1} + i_{D2} - i_{D3} - i_{D4}) \tag{26.15}$$

A simplified schematic of the multiplying quad with biasing is shown in Fig. 26.28. The op-amp inputs are at an AC virtual ground and at a DC voltage of V_{CM} (the op-amp output common-mode voltage). In order to minimize the DC input current on the x-axis inputs, the common-mode DC voltage on this input is set to V_{CM}. The DC biasing voltage on the y-input is set to a value large enough to keep the quad in triode. The input signals have been broken into two parts (e.g., $v_x/2$ and $-v_x/2$) to maintain generality. In practice, the minus inputs can be connected directly to the bias voltages

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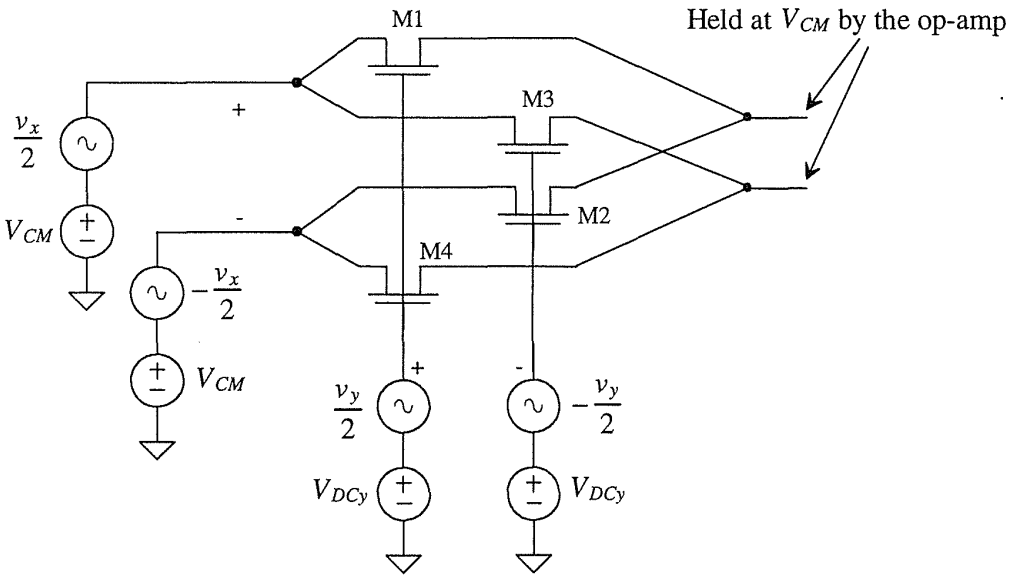


Figure 26.28 Biasing of the multiplying quad.

at the cost of large-signal linearity. (The input is not truly differential in this situation.) However, as discussed earlier, a fully differential system has much better coupled noise immunity.

Using Eq. (A.5) and noticing that the DC gate-source voltage of all MOSFETs is the same, the drain currents can be written as

$$i_{D1} = \beta_1\left[\left(V_{GS} + \frac{v_y}{2} - V_{THN1}\right)\left(\frac{v_x}{2}\right) - \frac{1}{2}\left(\frac{v_x}{2}\right)^2\right] \tag{26.16}$$

$$i_{D2} = \beta_2\left[\left(V_{GS} - \frac{v_y}{2} - V_{THN2}\right)\left(-\frac{v_x}{2}\right) - \frac{1}{2}\left(-\frac{v_x}{2}\right)^2\right] \tag{26.17}$$

$$i_{D3} = \beta_3\left[\left(V_{GS} - \frac{v_y}{2} - V_{THN3}\right)\left(\frac{v_x}{2}\right) - \frac{1}{2}\left(\frac{v_x}{2}\right)^2\right] \tag{26.18}$$

$$i_{D4} = \beta_4\left[\left(V_{GS} + \frac{v_y}{2} - V_{THN4}\right)\left(-\frac{v_x}{2}\right) - \frac{1}{2}\left(-\frac{v_x}{2}\right)^2\right] \tag{26.19}$$

We can design so that $\beta = \beta_1 = \beta_2 = \beta_3 = \beta_4$. We can use Eq. (26.15) together with Eqs. (26.16) - (26.19) to rewrite the output voltage of the multiplier as

$$v_{out} = R\beta \cdot \left(\frac{v_x}{2}\right)\left[\frac{v_y}{2} - V_{THN1} + \frac{v_y}{2} + V_{THN2} + \frac{v_y}{2} + V_{THN3} + \frac{v_y}{2} - V_{THN4}\right] \tag{26.20}$$

We can see that if V_{THN1} = (V_{THN2} or V_{THN3}) and V_{THN4} = (V_{THN3} or V_{THN2}), this equation can be rewritten as

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$$v_{out} = R\beta \cdot v_x v_y \tag{26.21}$$

The source of a MOSFET (the terminal we label "source" depends on which way current flows in the MOSFET) in the multiplying quad is connected either to the op-amp or to the x inputs. When the sources of the MOSFETs are connected to the op-amp, all the MOSFETs in the multiplying quad have the same threshold voltage. (Since the source of each MOSFET is tied to the same potential, the body effect changes each MOSFET's threshold voltage by the same amount.) If the + x-input is sinking a current, then the sources of M1 and M3 are the "+" x-input and thus $V_{THN1} = V_{THN3}$. In any case, the threshold voltages of the MOSFETs cancel and Eq. (26.21) holds. Comparing Eqs. (26.21) and (26.11) results in defining the gain of this multiplier as

$$K_m = R \cdot \beta \tag{26.22}$$

Simulating the Operation of the Multiplier

Simulating the performance and understanding the analog multiplier operation is an important step in the design process. The design of a multiplier consists of designing the op-amp, selecting the sizes of the multiplying quad, and designing the biasing network. Since we covered the design of differential input/output op-amps in the last chapter, it will not be covered here. In order to simulate the performance of a multiplier in SPICE without including the limitations of the op-amp, the simple model shown in Fig. 26.29 will be used. The sum of the multiplying factors associated with the voltage-controlled voltage sources, E1 and E2, is the open-loop gain of the op-amp. A typical SPICE statement for these VCVS (voltage-controlled voltage source) where the op-amp open loop gain is 20,000 is

```
E1      Voplus 8 4 3   1E4
E2      8 Vominus 4 3  1E4
```

where the nodes correspond to those labeled in Fig. 26.29.

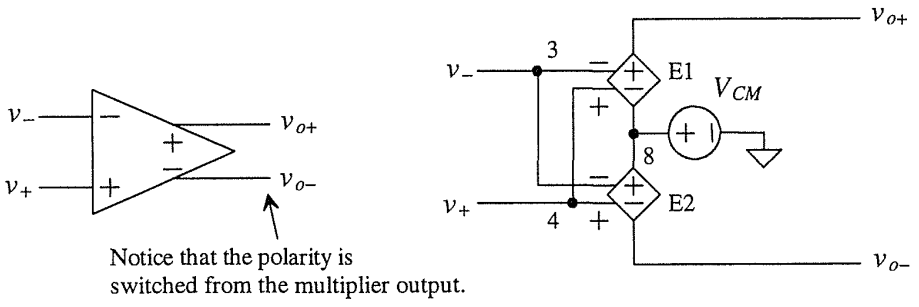


Figure 26.29 SPICE modeling a differential input/output op-amp with common-mode voltage.

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The next problem we encounter in simulating the operation of the multiplier is implementing the differential voltages (e.g. $\pm v_x/2$), in addition to the DC biasing voltages. The setup shown in Fig. 26.20 will be used to implement the biasing and the differential voltage sources. The op-amp common-mode output voltage, V_{CM}, and the x input voltage are set to 1.5 V. The lower this voltage, the easier it is to bias the multiplying quad into the triode region. On the other hand, a reduction in the value of V_{CM} limits the op-amp output voltage swing and thus the multiplier output range. The size of the multiplying quad was set to 10/2. The larger the *W/L* ratio of the MOSFETs used in this quad, the easier it is to keep the quad in the triode region. On the other hand, using a large *W/L* increases the required input current. The channel length can be increased to ensure the device operates as a long channel device and follows Eq. (A.5). Since the quad is part of the feedback around the op-amp, long channel devices do not affect the speed. The DC voltage at the y-inputs was set to 3.5 V as a compromise between keeping the multiplying quad in triode and the y-input voltage range. The gain of the multiplier in Fig. 26.30 is, from Eq. (26.22),

$$K_m = 20\text{k}\cdot 50\frac{\mu\text{A}}{\text{V}^2}\cdot\frac{10}{2} = 5\ \text{V}^{-1}$$

A DC sweep showing the operation of the multiplier is shown in Fig. 26.31. The x-input, v_x, was swept from –1 to +1, while at the same time the y-input was stepped from –1 to 1 V in 0.5 V increments. Keeping in mind that the output of the multiplier is $v_{o+} - v_{o-}$, we can understand the data presented in Fig. 26.31 by considering

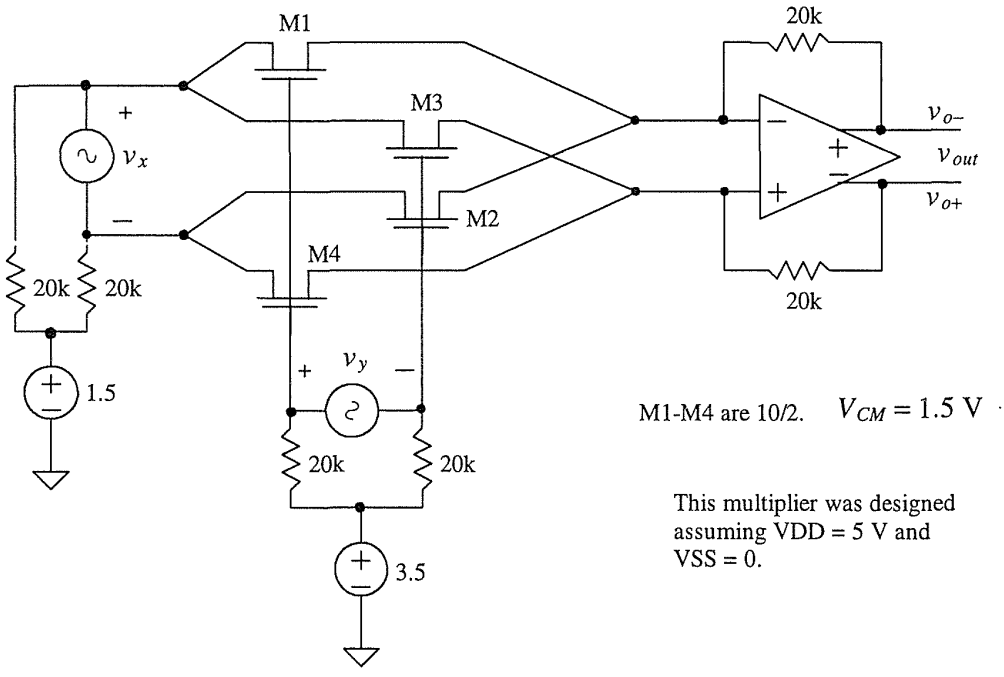


Figure 26.30 SPICE simulation schematic.

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points A and B. At point A the y-input is 1 V while the x-input is 0.2 V. The output voltage of the multiplier is the product of the multiplier gain and these two voltages (i.e., 5·1·0.2 = 1 V). The output voltage at point B is 5·(–0.5)·(–0.6) = 1.5 V. Note that this figure was generated using an almost ideal op-amp. The characteristics do not show the limitations of the op-amp. In particular, the limited output swing. Below is the SPICE netlist used to generate this plot.

```
*** Top Level Netlist ***
E1      Voplus 8 4 3    1E4
E2      8 Vominus 4 3  1E4
M1      7 5 4 0 CMOSNB  L=2u W=10u
M2      11 6 4 0 CMOSNB  L=2u W=10u
M3      7 6 3 0 CMOSNB  L=2u W=10u
M4      11 5 3 0 CMOSNB  L=2u W=10u
R10     10 7 20k
R7      10 11 20k
R8      9 5 20k
R9      9 6 20k
Rfn     Vominus 4 20k
Rfp     Voplus 3 20k
VCM     8 0     DC 1.5 AC 0 0
VCMx    10 0    DC 1.5 AC 0 0
VDCy    9 0     DC 3.5 AC 0 0
Vx      7 11    DC 0 AC 1 0
Vy      5 6     DC 1 AC 0 0

.MODEL CMOSNB NMOS LEVEL=4
+VFB=-9.73820E-01, LVFB=3.67458E-01,WVFB=-4.72340E-02
see Appendix A for a complete BSIM listing

***** End of spice models and macro models *****
.OPTION ABSTOL=1u RELTOL=0.01 VNTOL=1mv
```

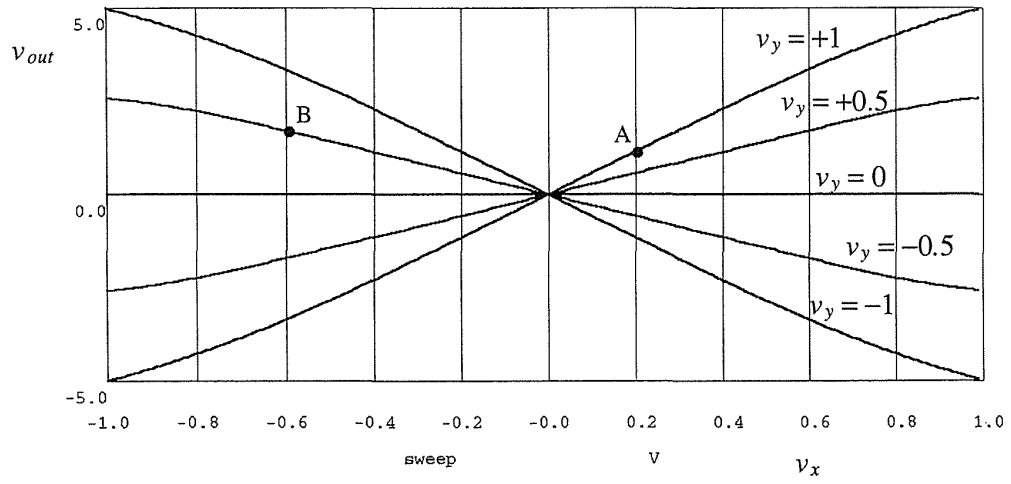


Figure 26.31 DC characteristics of the multiplier of Fig. 26.30.

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```
.probe
.DC Vx -1 1 .01 Vy -1 1 .5
.plot dc all
.print dc all
.end
```

26.3.2 Level Shifting

Now that we have discussed the basic operation of the multiplier, the next step is to design the level-shifting stages. Level-shifting stages are used to implement the biasing batteries shown in Fig. 26.28 for both the x- and y-inputs. Before we complete the initial design of our basic multiplier, let's discuss general-level shifting and single-ended to differential conversion since they have many applications in single-supply chip design.

Consider the basic p-channel source-follower circuits shown in Fig. 26.32 without the body effect. The source-gate voltages of the p-channel MOSFETs are used to shift the input signals, which are referenced to ground, upward. This circuit could be useful in implementing the x-input level shifter in our analog multiplier. The x-inputs can actually go negative by V_{THP} before M1 or M2 goes into the triode. The main drawback of using this circuit is the lack of common-mode rejection on the inputs. Also, if we try to drive the circuit single-ended, that is, the minus input connected to ground, the outputs of the circuit are not truly differential. This problem is encountered in any single-ended to differential-ended conversion, including those circuits made using diff-amps. Normally, the best method of designing a single-ended to differential-ended converter is to use a high-gain differential input/output op-amp with feedback. This configuration keeps the signal levels across the input of the op-amp small. Figure 26.33 shows two op-amp configurations, which are useful in single- to

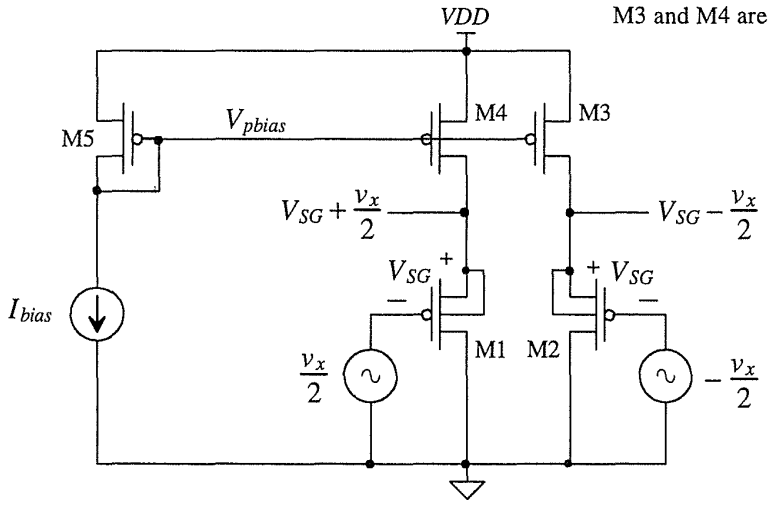


Figure 26.32 Level shifting using p-channel source followers.

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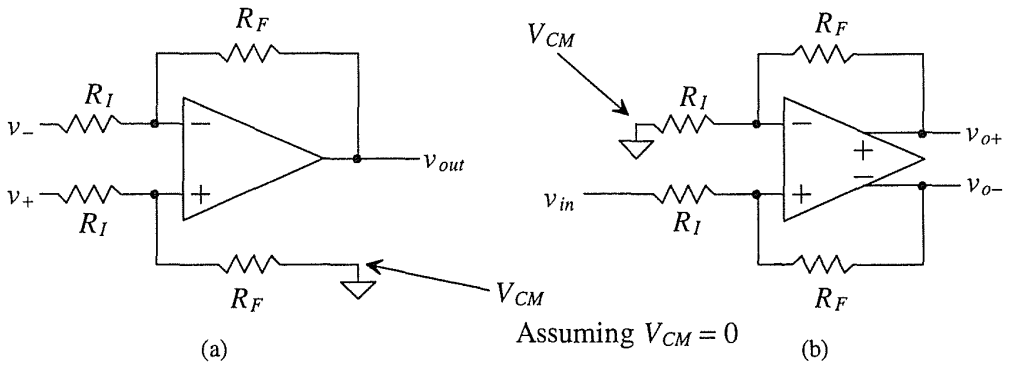


Figure 26.33 (a) Differential to singled ended converter and (b) single to differential-ended converter.

differential-ended (and vice-versa) conversion. The input/output relationship of the differential- to single-ended amplifier of Fig. 26.33a is

$$v_{out} = \frac{R_F}{R_I}(v_+ - v_-) \tag{26.23}$$

The relationship between the input and outputs of the single-ended to differential amplifier of Fig. 26.33b is

$$v_{o+} - v_{o-} = \frac{R_F}{R_I} \cdot v_{in} \tag{26.24}$$

In this figure, we assumed a common-mode voltage of zero (ground). Figure 26.34 shows how the single- to differential-ended converter would be connected if the amplifier was used in a system with a single supply. It is important that all common-mode voltages used in the circuit have the same temperature coefficient. This avoids input DC current and keeps the output of the op-amp from moving toward *VDD*

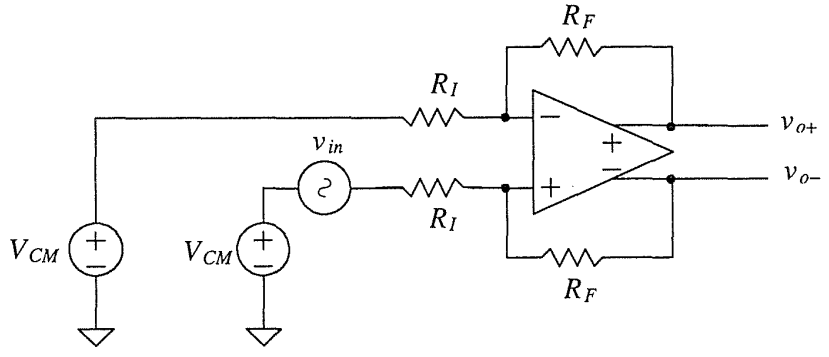


Figure 26.34 Implementation of a single- to differential-ended converter in single-supply system.

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or ground. For example, if we were to use p-channel source-followers to generate the V_{CM} on the inputs of the amplifier, then we would also use a source follower to generate the op-amp V_{CM}. This idea will be explained in greater detail when we discuss the design of the x-input level-shifing network in our basic multiplier.

Another level-shifting circuit (also known as a floating battery) is shown in Fig. 26.35 [11]. The battery voltage generated by this circuit is given by

$$V_B = V_{SG1} + V_{SG2} \tag{26.25}$$

The small-signal resistance of the battery (i.e., the resistance between the drain and source of M2) is $1/g_{m2}$. Normally, to keep $1/g_{m2}$ small, β_2 is made large. This results in a V_{SG2} of approximately V_{THP}, and therefore the size of M1 is adjusted to achieve the desired battery voltage. A potential problem exists with this configuration in its current state. Current can only flow from the source of M2 to its drain. This means that an input signal connected to the drain of M2 cannot source a current. Adding the current source, I_2, as shown in Fig. 26.36a helps solve this problem at the cost of an input current - the current I_2 flows in v_{in} under steady-state conditions. Adding the source-follower, M3, shown in Fig. 26.36b eliminates input current. Using the source-follower shifts the DC output voltage up by V_{SG3}. The major benefit of these configurations is that the input voltage can go negative by V_{THP} and M1 or M3 will remain in the saturation region. If we assume that β_2 and β_3 are large, then $V_{SG3} = V_{SG2} = V_{THP}$. The DC output voltage, for the circuit of Fig. 26.36b, used to shift an input signal upward is

$$V_{DC} = V_{SG1} + 2V_{THP} \tag{26.26}$$

Input Level Shifting for the Multiplier of Figure 26.27 and 26.28

In the following discussion, we are assuming that the multiplier has to be DC coupled, the inputs are referenced to ground, and only a single supply voltage is used. The biasing design can be greatly simplified if these conditions do not hold. For example, if the inputs can be AC coupled, a simple resistive or MOSFET divider can be used to set

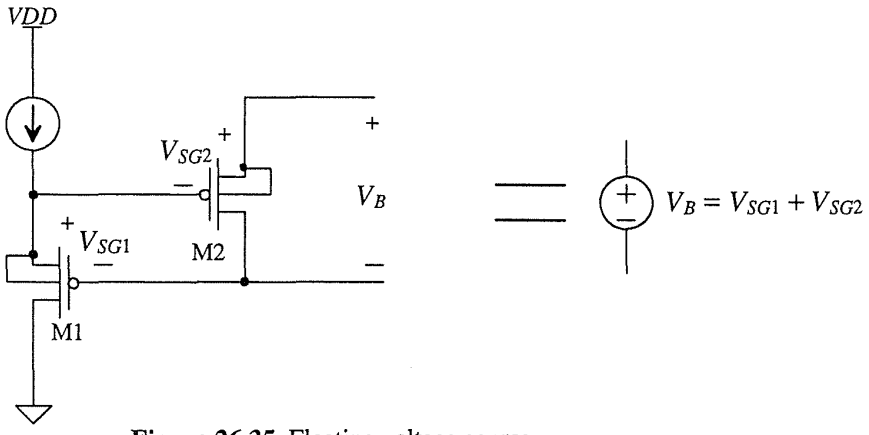


Figure 26.35 Floating voltage source.

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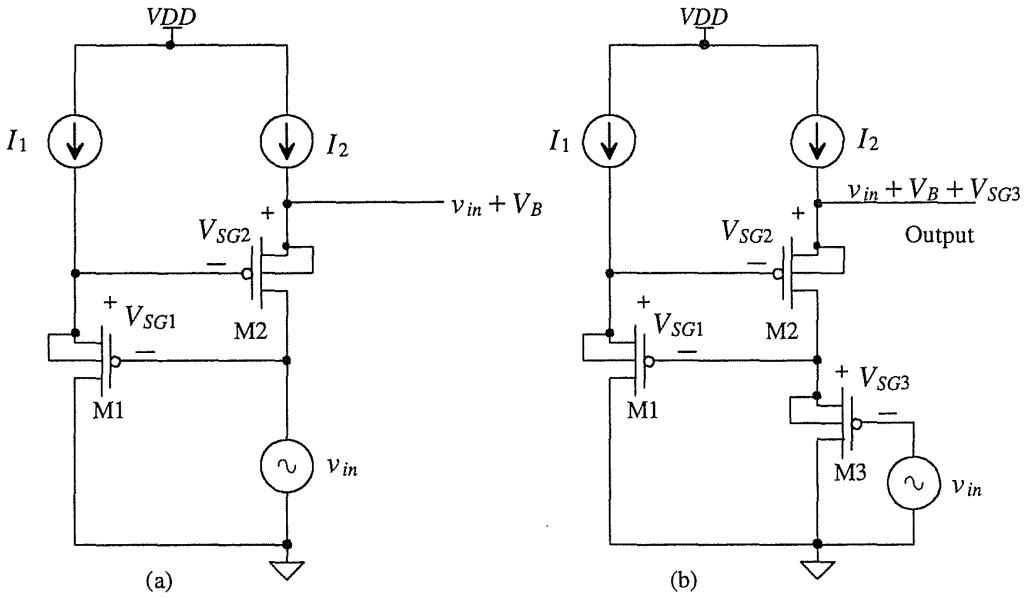


Figure 26.36 Adding input voltage source to battery: (a) with input current and (b) without input current.

the DC operating conditions while the input AC signals can be connected through a capacitor. If the inputs are referenced to, say V_{CM} (which is what would occur if the inputs signals are supplied by a differential input/output op-amp), then diff-amps can be used to generate the bias voltages since the input signals now lie within the CMR of a diff-amp.

The complete analog multiplier with level-shifting stages is shown in Fig. 26.37. Current sources M7 and M8 are biased to source 500 μA of current. The nominal V_{SG} of MOSFETs M5 and M6 is 1.5 V. A channel length of 2 μm was used in all MOSFETs used in the level-shifting networks for high-speed operation. MOSFETs M9 and M10 are used to generate the V_{CM} for the op-amp (the voltage used at the gates of MF6 and MF7 in Fig. 25.50). This guarantees that the DC reference on the x-inputs and the output of the op-amp are the same voltage and track with temperature. This eliminates DC input current through the multiplying quad and keeps the op-amp output from railing at *VDD* or ground. Using the same circuit (in this case a source follower) for the DC reference on the inputs and the outputs is very *important*. Note that in a dual supply system, where ground is the common-mode voltage, temperature drift and op-amp output wander are not a concern.

The y-input level-shifting network shifts the y-inputs, which are referenced to ground up to nominally 3.6 V. MOSFETs M11 through M20 are biased at 50 μA with a corresponding source-gate voltage of 1.2 V. This level-shifting configuration is wide-band since all MOSFETs are operated in the source-follower configuration. Also,

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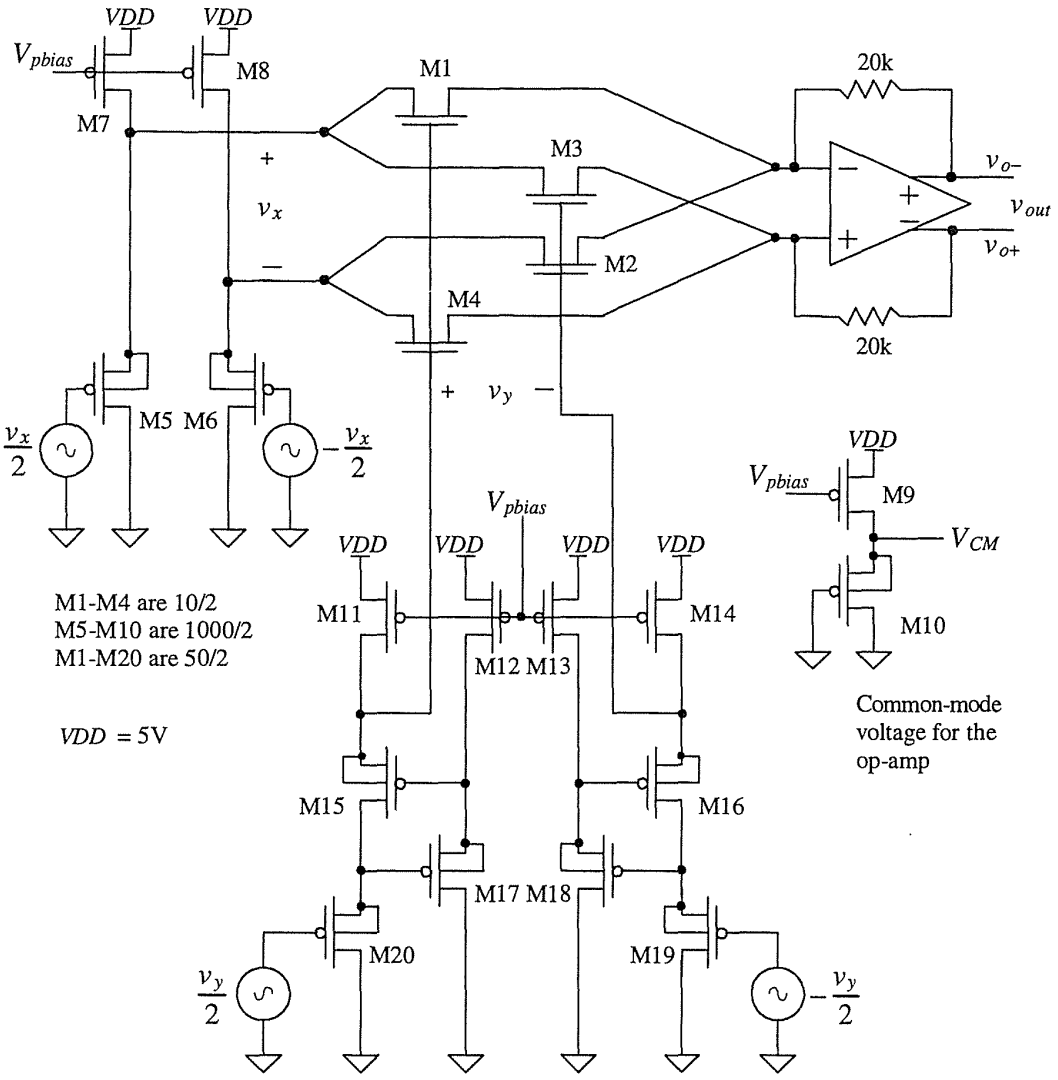


Figure 26.37 Complete analog multiplier.

in both level-shifting networks, the body effect is eliminated by laying out each MOSFET in its own well.

The multiplier output is shown in Fig. 26.38. Note that because the gain of the source-followers is less than one, the overall gain of the multiplier is less than five, which is what we predicted earlier with the simple battery implementation of Fig. 26.30.

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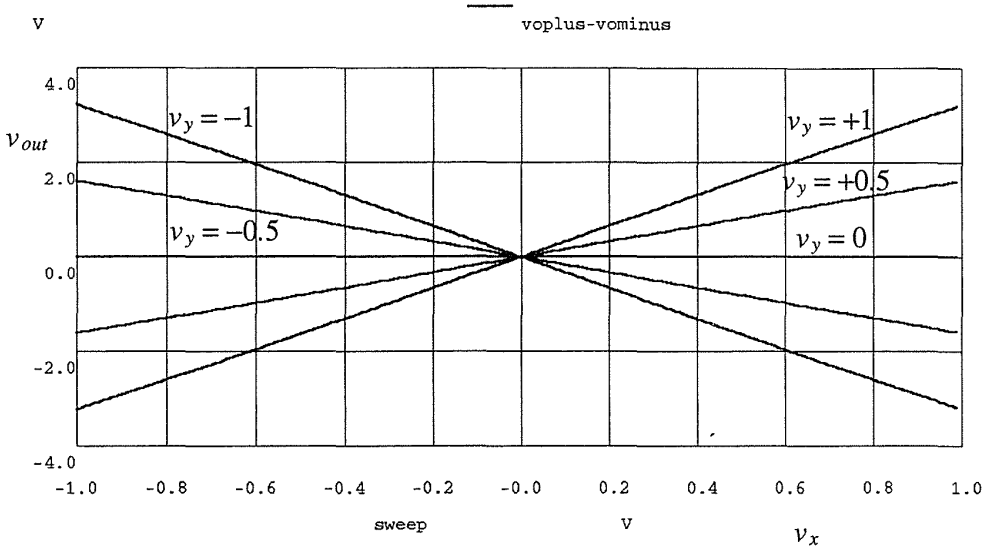


Figure 26.38 Simulation results for the multiplier shown in Fig. 26.37.

26.3.3 Multiplier Design Using Squaring Circuits

An analog multiplier can be designed based on the difference between the sum of two voltages squared and the difference of two voltages squared [12], or

$$V_o = (V_1 + V_2)^2 - (V_1 - V_2)^2 = 4V_1V_2 \tag{26.27}$$

The basic sum-squaring and difference-squaring circuits are shown in Fig. 26.39. MOSFETs M1 and M4 are source-followers, while MOSFETs M2 and M4 are called squaring MOSFETs. This circuit is designed so that $\beta_1 = \beta_4 = \beta_{14}$, $\beta_2 = \beta_3 = \beta_{23}$ and $\beta_{14} >> \beta_{23}$. This makes almost all of the DC bias currents, I_{S12} and I_{S34}, flow in the MOSFETs M1 and M4, respectively. The squaring current, I_{SQ}, assuming that zero current flows through the resistor when both inputs are zero volts (or whatever the common-mode voltage when a single supply is used), is given by

$$I_{SQ(a)} = \frac{\beta_{23}}{4}(V_1 + V_2)^2 \tag{26.28}$$

Similarly, the squaring current in the difference-square circuit of Fig. 26.39b is given by

$$I_{SQ(b)} = \frac{\beta_{23}}{4}(V_1 - V_2)^2 \tag{26.29}$$

The output voltage of the sum-square circuit is given by

$$V_{o-} = VDD - I_{SQ(a)}R \tag{26.30}$$

while the output voltage of the difference-square circuit is given by

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$$V_{o+} = VDD - I_{SQ(b)}R \tag{26.31}$$

A multiplier is formed by taking the difference between these voltages. The output voltage of the multiplier of Fig. 26.39 is given by

$$V_{out} = V_{o+} - V_{o-} = R\frac{\beta_{23}}{4}\left[(V_1 + V_2)^2 - (V_1 - V_2)^2\right] \tag{26.32}$$

or, using Eq. (26.27)

$$V_{out} = R\beta_{23} \cdot V_1 V_2 \tag{26.33}$$

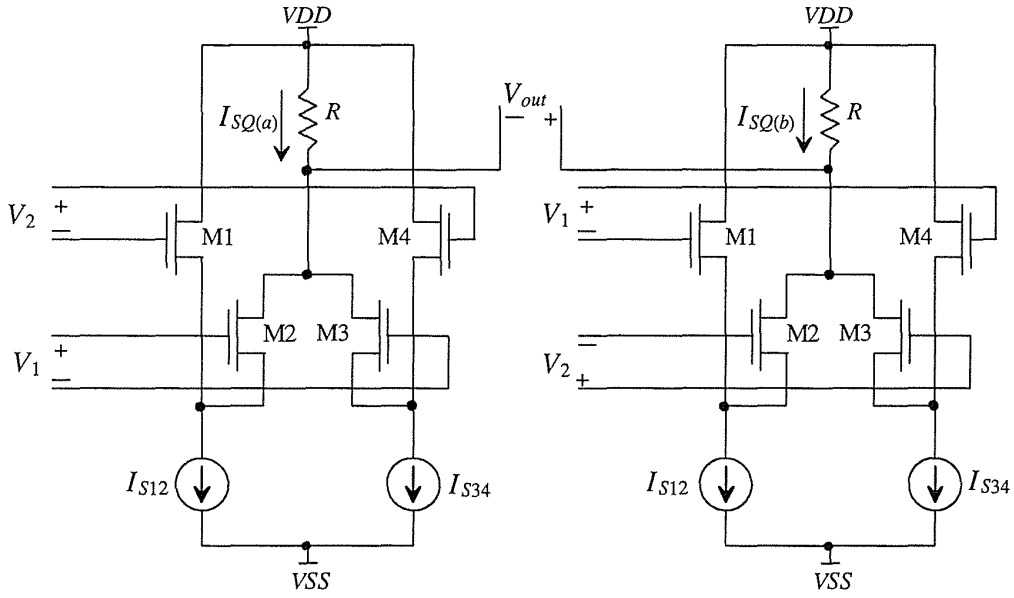


Figure 26.39 (a) Sum-squaring circuit and (b) difference squaring circuit.

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PROBLEMS

26.1 A very important component of a comparator is its offset voltage. The offset voltage of a comparator can be modeled as a DC voltage source in series with the gate of the MOSFET used in the input diff-pair (Fig. P26.1). Regenerate Fig. 26.6, including an offset voltage of 10 mV. Comment on the effects of an offset voltage on this plot.

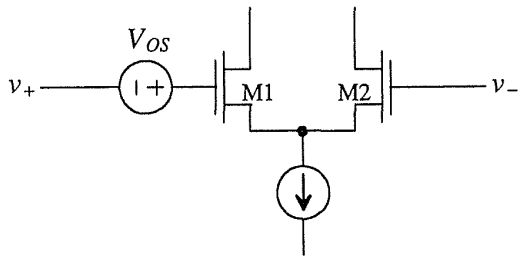


Figure P26.1

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26.2 What is the input capacitance of the comparator shown in Fig. 26.11? How is the gain of the comparator affected by using a decision circuit with hysteresis?

26.3 Design and simulate the operation of a comparator with 100 mV hysteresis.

26.4 To determine the sensitivity of a comparator, the amplitude of a wide-input pulse is reduced until the output of the comparator does not make a full logic transition. Determine the minimum sensitivity of the comparator of Fig. 26.11 using SPICE. Note: In practice, making sensitivity measurements is very difficult. The comparator will oscillate, and coupled noise will affect the measurement.

26.5 Simulate the operation of the comparator shown in Fig. 26.18.

26.6 Discuss the benefits and problems of using the output buffer shown in Fig. P26.6 in conjunction with the preamp and decision circuit of Fig. 26.5.

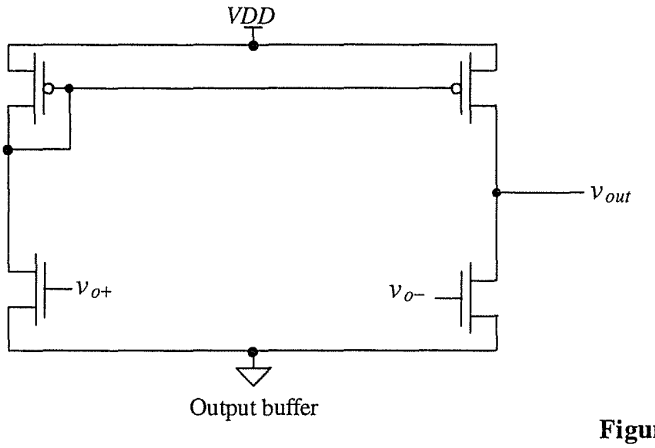


Figure P26.6

26.7 Can the self-biased comparator be used as a wide-swing op-amp? If so, how would the op-amp be compensated?

26.8 Sketch the schematic of an adaptive voltage follower that can source or sink current.

26.9 Discuss the benefits and problems of using long channel lengths in the multiplying quad of Fig. 26.30.

26.10 Verify, using SPICE and the differential input/output model shown in Fig. 26.29, the operation of the converters shown in Fig. 26.33. Apply sine waves to the inputs and perform a SPICE transient analysis.

26.11 Design and simulate the operation of a level-shifting circuit that will shift input signals referenced at ground up nominally 1.5 V. Comment on the frequency response of your design.

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Chapter

27

Dynamic Analog Circuits

Chapter 14 discussed dynamic digital circuits, which are useful in reducing power dissipation and the number of MOSFETs used to perform a given circuit operation. Dynamic analog circuits exploit the fact that information can be stored on a capacitor or gate capacitance of a MOSFET for a period of time. In this chapter, we will discuss analog circuits such as sample and holds, current mirrors, amplifiers, and filters using dynamic techniques.

27.1 The MOSFET Switch

A fundamental component of any dynamic circuit (analog or digital) is the switch (Fig. 27.1). An important attribute of the switch, in CMOS is that under DC conditions the gate of the MOSFET does not draw a current. Therefore, neglecting capacitances from the gate to the drain/source, we find that the gate control signal does not interfere with information being passed through the switch. Figure 27.2 shows the small-signal resistance of the switches of Fig. 27.1 plotted against drain-source voltage. The benefits of using the CMOS transmission gate are seen from this figure, namely, lower overall resistance. Another benefit of using the CMOS TG is that it can pass a logic high or a

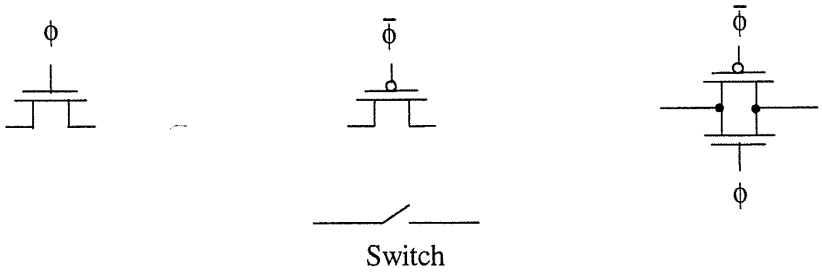


Figure 27.1 MOSFETs used as switches.

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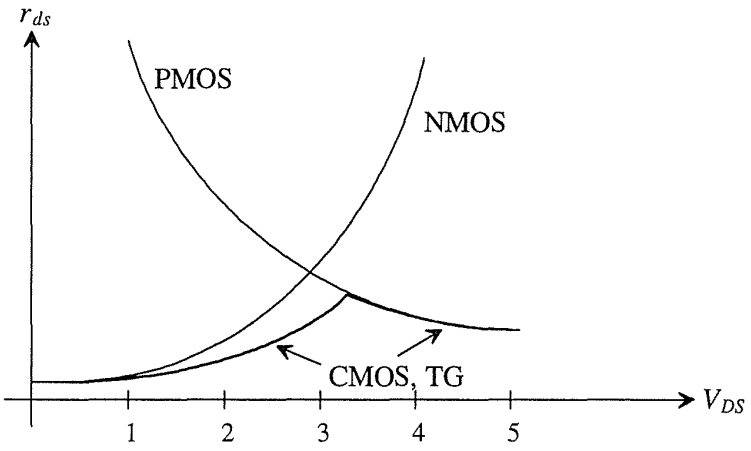


Figure 27.2 Small-signal on-resistance of MOSFET switches [1].

logic low without a threshold voltage drop. The largest voltage an n-channel switch can pass is $VDD - V_{THN}$, while the lowest voltage a p-channel switch can pass is V_{THP}.

While MOS switches may offer substantial benefits, they are not without some detraction. Two nonideal effects typically associated with these switches may ultimately limit the use of MOS switches in some applications (particularly sampled-data circuits such as data converters). These two effects are known as charge injection and clock feedthrough.

Charge Injection

Charge injection can be understood with the help of Fig. 27.3. When the MOSFET switch is on and V_{DS} is small, the charge under the gate oxide resulting from the inverted channel is (from Ch. 5) Q'_{ch}. When the MOSFET turns off, this charge is injected onto the capacitor and into v_{in}. Since v_{in} is assumed to be a low-impedance, source-driven node, the injected charge has no effect on this node. However, the charge injected onto C_{load} results in a change in voltage across it.

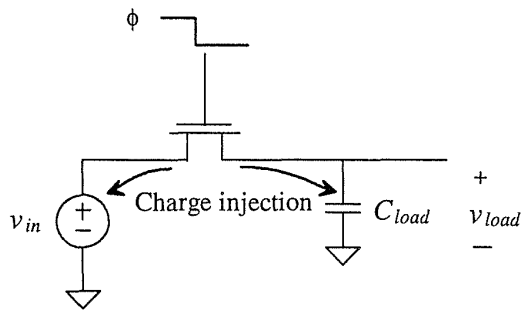


Figure 27.3 Simple configuration using an NMOS switch to show charge injection.

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Although the charge injection mechanism is itself a complex one, many studies have sought to characterize and minimize its effects [2-4]. It has been shown, that if the clock signal turns off fast, the channel charge distributes fairly equally between the adjacent nodes. Thus, half of the channel charge is distributed onto C_{load}. From Ch. 5, the charge/unit area of an inverted channel can be approximated as

$$Q_I'(y) = C_{ox}' \cdot (V_{GS} - V_{THN}) \tag{27.1}$$

The total charge in the channel must then be multiplied by the area of the channel resulting in

$$Q_I(y) = C_{ox}' \cdot W \cdot L \cdot (V_{GS} - V_{THN}) \tag{27.2}$$

Therefore, the change in voltage across C_{load} (if an NMOS switch is used) is

$$\Delta v_{load} = -\frac{C_{ox}' \cdot W \cdot L \cdot (V_{GS} - V_{THN})}{2C_{load}} \tag{27.3}$$

which can be written as

$$\Delta v_{load} = -\frac{C_{ox}' \cdot W \cdot L \cdot (VDD - v_{in} - V_{THN})}{2C_{load}} \tag{27.4}$$

if it is assumed that the clock swings between V_{DD} and V_{SS}. The threshold voltage can also be substituted into Eq. (27.4) to form

$$\Delta v_{load} = -\frac{C_{ox}' \cdot W \cdot L \cdot (V_{DD} - v_{in} - [V_{THN0} + \gamma(\sqrt{|2\phi_F| + v_{in} - V_{SS}} - \sqrt{|2\phi_F|})])}{2C_{load}} \tag{27.5}$$

Note that Eq. 27.5 illustrates the problem associated with charge injection. The change in voltage across C_{load} is nonlinear with respect to v_{in} due to the threshold voltage. Thus, it can be said that if the charge injection is signal dependent, harmonic distortion results. In sampled-data systems, charge injection will result in nonlinearity errors. In the case where the charge injection is signal independent, a simple offset occurs which is much easier to manage than harmonic distortion. These will be discussed in more detail in Chs. 28 and 29, but it should be obvious here that charge injection effects should be minimized as much as possible.

Capacitive Feedthrough

Consider the schematic of the NMOS switch shown in Fig. 27.4. Here the capacitances between the gate/drain and gate/source of the MOSFET are modeled with the assumption that the MOSFET is operating in the triode region. When the gate clock signal, ϕ, goes high, the clock signal feeds through the gate/drain and gate/source capacitances. However, as the switch turns on, the input signal, v_{in}, is connected to the load capacitor through the NMOS switch. The result is that C_{load} is charged to v_{in} and the capacitive feedthrough has no effect on the final value of v_{out}. However, now consider what happens when the clock signal makes the transition low, that is, the n-channel MOSFET turns off. A capacitive voltage divider exists between the

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gate-drain (source) capacitance and the load capacitance. As a result, a portion of the clock signal, ϕ, appears across C_{load} as

$$\Delta v_{load} = \frac{C_{overlap} \cdot (V_{DD} - V_{SS})}{C_{overlap} + C_{load}} \tag{27.6}$$

where $C_{overlap}$ is the overlap capacitance value,

$$C_{overlap} = C'_{ox} \cdot W \cdot LD \tag{27.7}$$

and LD is the length of the gate that overlaps the drain/source.

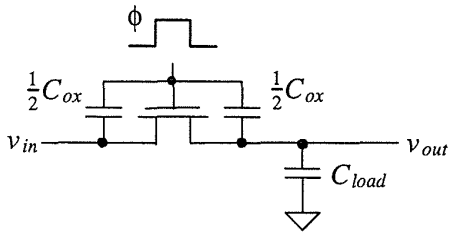


Figure 27.4 Illustration of capacitive feedthrough.

Reduction of Charge Injection and Clock Feedthrough

Many methods have been reported that reduce the effects of charge injection and capacitive feedthrough. One of the most widely used is the dummy switch [4, 5], as seen in Fig. 27.5. Here, a switch with its drain and source shorted is placed in series with the desired switch M1. Notice that the clock signal controlling the dummy switch is the complement of the signal controlling M1, and in addition, should also be slightly delayed.

When M1 turns off, half the channel charge is injected toward the dummy switch, thus explaining why the size of M2 is one-half that of M1. Although M2 is effectively shorted, a channel can still be induced by applying a voltage on the gate. Therefore, the charge injected by M1 is essentially matched by the charge induced by M2, and the overall charge injection is canceled. Note what happens when M2 turns

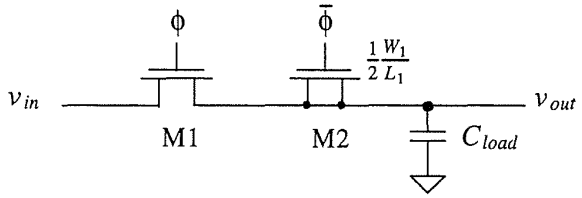


Figure 27.5 Dummy switch circuit used to minimize charge injection.

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off. It will inject half of its charge in both directions. However, since the drain and source are shorted and M1 is on, all the charge from M2 will be injected onto the low-impedance, voltage-driven source which is also charging C_{load}. Therefore, M2 charge injection will not affect the value of voltage on C_{load}.

Another method used to counteract charge injection and clock feedthrough is to replace the switch with a CMOS transmission gate (TG). This will result in lower changes in v_{out} because the complementary signals used will act to cancel each other. However, this approach requires precise control on the complementary clocks (the clocks must be switched at exactly the same time) and assumes that the input signal, v_{in}, will be small, since the symmetry of the turn-on and turn-off waveforms are dependent on the input signal.

Fully differential circuit topologies are used to cancel these effects to a first order, as seen in Fig. 27.6. Since the nonideal charge injection and clock feedthrough effects appear as a common-mode signal to the amplifier, they will be reduced by the CMRR of the amplifier. However, the second-order effects resulting from the input signal amplitude dependence will ultimately limit the dynamic range of operation, neglecting coupled and inherent noise in the dynamic circuits. This subject will be discussed in more detail in the next sections.

kT/C Noise

In Ch. 7 we saw that the maximum RMS output noise generated from a simple *RC* circuit was $\sqrt{kT/C}$ (see Ex. 7.7). If we think of the MOSFET in Fig. 27.7 as a resistor (when the MOSFET is on), then we can add this RMS noise source in series with the output of the capacitor. The noise can be regarded as a sampled voltage onto the capacitor each time the switch is turned on. The RMS noise generated when using a 1 pF capacitor is 64 μV, while a 100 fF capacitor results in a noise voltage of 200 μV. In other words, the larger the capacitor, the smaller the noise voltage sampled on to the storage capacitor. For high-speed systems, it is desirable to use small capacitors since they take less time to charge. When designing a high-speed/low-noise circuit tradeoffs must be made when selecting the capacitor size.

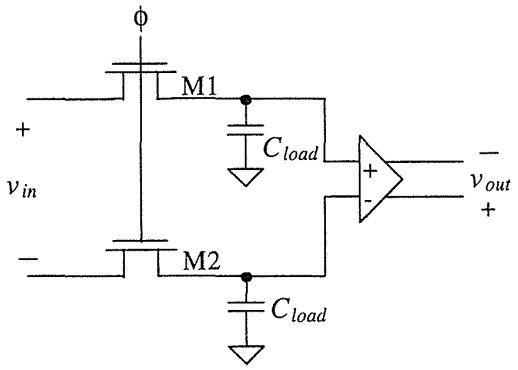


Figure 27.6 Use of a fully differential circuit to minimize charge injection and clock feedthrough.

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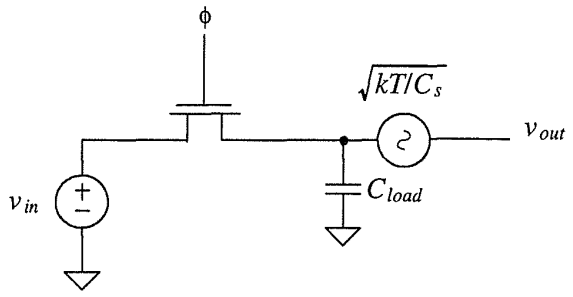


Figure 27.7 How kT/C noise adds to a sampled signal.

Sample-and-Hold Circuits

An important application of the switch is in the sample-and-hold circuit. The sample-and-hold circuit finds extensive use in data converter applications as a sampling gate. A variety of topologies exist, each with their own benefits. The simplest is shown in Fig. 27.8. A narrow pulse is applied to the gate of the MOSFET, enabling v_{in} to charge the hold capacitor, C_H. The width of the strobing gate pulse should allow the capacitor to fully charge before being removed. The op-amp simply acts as a unity gain buffer, isolating the hold capacitor from any external load. This circuit suffers from the clock feedthrough and charge injection problems mentioned in the previous discussion.

Figure 27.9 shows a fully differential sample-and-hold circuit and associated clock waveforms that eliminate clock feedthrough and charge injection to a first order [6]. The switches in this figure are closed when their controlling clock signals are high. The basic operation can be understood by considering the state of the circuit at t_0. At this time, the input signals charge the sampling capacitors. The bottom plates of the capacitors (poly1) are tied directly to the input signals, for reasons that will be explained below. The op-amp is operating in a unity-follower configuration in which both inputs of the op-amp are held at V_{CM}. At this particular instance in time, prior to t_1, the amplifier is said to be operating in the sample mode of operation.

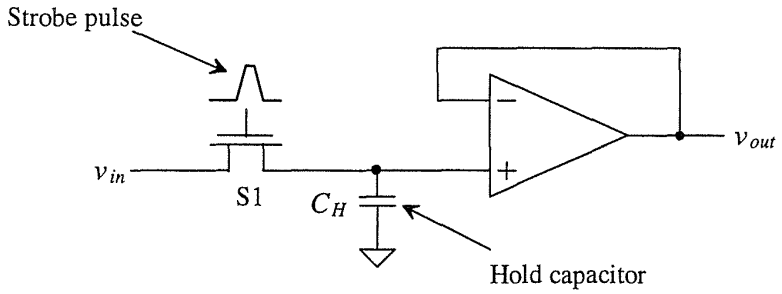


Figure 27.8 A basic sample-and-hold circuit.

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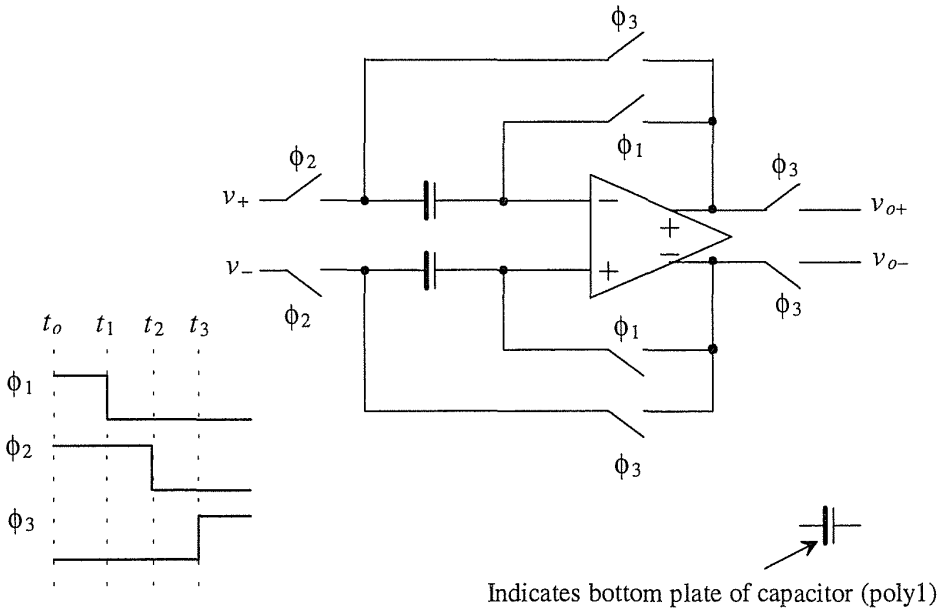


Figure 27.9 Sample-and-hold using differential topology [6].

At t_1 the ϕ_1 switches turn off. The resulting charge injection and clock feedthrough appear as a common-mode signal on the inputs of the op-amp and are ideally rejected. Since the top plates of the hold capacitors (the inputs to the op-amp) are always at V_{CM}, at this point in time the charge injection and clock feedthrough are independent of the input signals. The result is an increase in the dynamic range of the sample-and-hold (the minimum measurable input signal decreases). The voltage on the inputs of the op-amp (the top plate of the capacitor) between t_1 and t_2 is $V_{OFF1} + V_{CM}$, a constant voltage. Note that the op-amp is operating open loop at this time so that the time between t_1 and t_3 should be short.

At t_2 the ϕ_2 switches turn off. At this point in time, the voltages on the bottom plates of the sampling capacitors are v_+ and v_- for the + and – inputs of the circuit, respectively. The voltages on the top plates of the capacitors are $V_{OFF1} + V_{OFF2} + V_{CM}$ (assuming the storage capacitors are much larger than the input capacitance of the op-amp). The term V_{OFF2} is ideally a constant that results from the charge injection and capacitive feedthrough from the ϕ_2 switches turning off. The time between t_1 and t_2 should be short compared to variations in the input signals.

At time t_3 the ϕ_3 switches turn on and the op-amp behaves like a voltage follower, and the circuit is said to be in the hold mode of operation. The charge injection and clock feedthrough resulting from the ϕ_3 switches turn on cause the top

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plate of the capacitor to become $V_{OFF1} + V_{OFF2} + V_{OFF3} + V_{CM}$, again assuming that the storage capacitors are much larger than the input capacitance of the op-amp. The outputs of the sample-and-hold are v_+ and v_-, assuming infinite op-amp gain since these offsets appear as a common-mode voltage on the input of the op-amp. Note that the terms V_{OFF2} and V_{OFF3} are dependent on the input signals.

The reason for connecting the input signals to the bottom plate of the capacitor can be explained with the help of Fig. 27.10. This figure is a simplified, single-ended version of Fig. 27.9 where the capacitance, C_p, is the parasitic capacitance from the bottom plate to the substrate. With regard to Fig. 27.10a, coupled noise from the substrate sees either the input voltage from the op-amp driving the sample-and-hold (in the sample mode) or the output voltage of the op-amp used in the sample-and-hold itself (in the hold mode). Since the op-amps in either mode directly set this voltage, the substrate noise will, ideally, have little effect on the circuit operation. In Fig. 27.10b, coupled substrate noise feeds directly into the input of the op-amp and can thus drastically affect the output of the sample-and-hold. Another more subtle problem occurs in the circuit of Fig. 27.10b. When the circuit makes the transition to the hold mode at t_3, the output of the op-amp should quickly change to the voltage sampled on the input capacitors. The time it takes the output of the op-amp to change and settle to this final voltage is called the *settling time*. The parasitic capacitance on the input of the op-amp reduces the feedback factor from unity to $C_H/(C_p + C_H)$. This slows the settling time and causes a gain error in the circuit's transfer function. For these reasons, the parasitic capacitance on the top plate of the capacitor should be small. Nothing should be laid out over or in near proximity of poly2.

Another improvement of the basic S/H circuit can be seen in Fig. 27.11 [7, 8]. Here, two amplifiers buffer the input and the output. Notice that switch S_2 ensures that amplifier A1 is stable while in hold mode. If the switch were not present, A1 would be open loop during hold mode and would swing to one of the rails. During the next

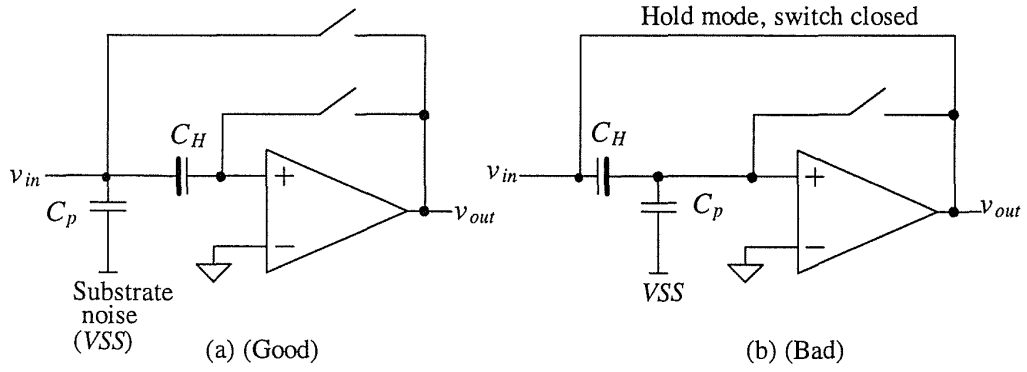


Figure 27.10 Explanation for connecting the bottom plate of the capacitor to the input.

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sample mode, it would then be slew limited while going from the supply to the value of v_{in}. However, with the addition of S_2, the output of A1 tracks v_{in} even while in hold mode. The switch S_3 also disconnects A1 from the output during hold mode.

This S/H has its disadvantages, however. The capacitor is still subjected to charge injection and clock-feedthrough problems. In addition, during sample mode, the circuit may become unstable since there are now two amplifiers in the single-loop feedback structure. Although compensation capacitors can be added to stabilize its performance, the size and placement of the capacitors are purely dependent on the type and characteristics of the op-amps.

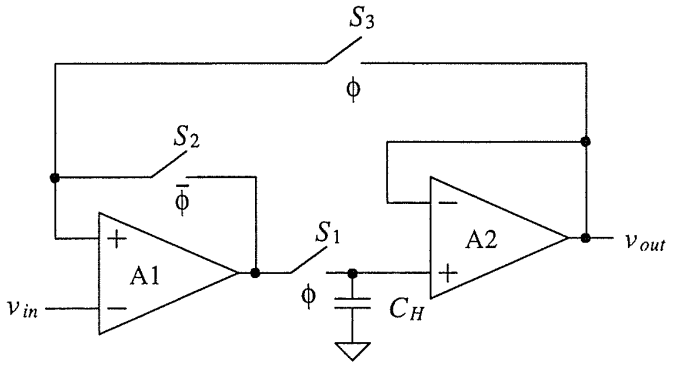


Figure 27.11 A closed-loop S/H circuit.

Another S/H circuit is seen in Fig. 27.12 [7,9]. Here, a transconductance amplifier is used to charge the hold capacitor. A control signal turns the amplifier, A1, on or off digitally, thus eliminating the need for the switches S_2 and S_3 (from Fig. 27.11). Since CMOS op-amps are well suited for high-output impedance applications, this configuration would seem to be a popular one. However, the speed of this topology is dictated by the maximum current output of the transconductance amplifier and the size of the hold capacitor.

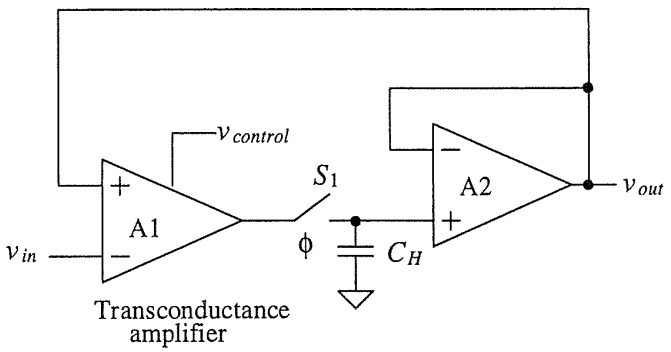


Figure 27.12 A closed-loop S/H circuit using a transconductance amplifier.

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An even better S/H circuit can be seen in Fig. 27.13 [7, 8]. The advantage of this circuit may not be completely obvious and warrants further explanation. First, notice that the hold capacitor is actually in the feedback path of the amplifier, A2, with one side connected to the output of the amplifier and the other connected to a virtual ground. When switch S_1 turns off, any charge injected onto the hold capacitor will result in a slight change in the output voltage. However, now that one side of the switch is at virtual ground, the change in voltage is no longer dependent on the threshold voltage of the switch itself. Therefore, the charge injection will be independent of the input signal and will result as a simple offset at the output. An offset error is much easier to tolerate than a nonlinearity error, as will be seen in Chs. 28 and 29.

When sampling, S_1 is closed and S_2 is open, and the equivalent circuit is simply a low-pass filter with a buffered input. The overall transfer function becomes

$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1} \cdot \frac{1}{(sR_2C_H + 1)} \tag{27.8}$$

Therefore, this circuit performs a low-pass filter function while sampling. The buffer A1 can be eliminated when we desire a low-input impedance. Once hold mode commences, the output will stay constant at a value equal to v_{in}, while the switch S_2 isolates the input from the hold capacitor. One important issue to note here is that A2 will need to be a buffered CMOS amplifier because of the resistive load attached at v_{out} during hold mode. Notice also that during both sample mode and hold mode, there is only one op-amp in each feedback loop, so this S/H topology is much more stable than the closed-loop structure introduced in Fig. 27.12.

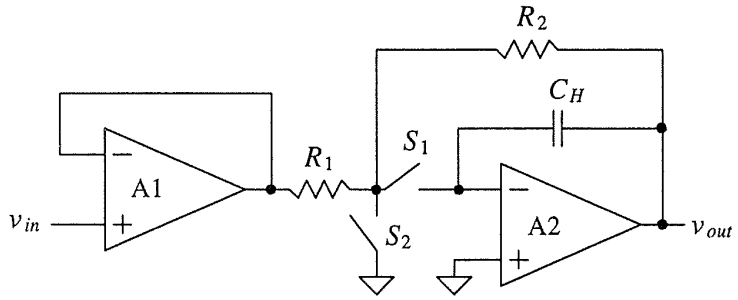


Figure 27.13 A closed-loop S/H circuit using a transconductance amplifier.

27.2 Switched-Capacitor Circuits

Consider the circuit shown in Fig. 27.14a [10, 11]. This dynamic circuit, named a switched-capacitor resistor, is useful in simulating a large value resistor, generally > 1 MΩ. The clock signals ϕ_1 and ϕ_2 form two phases of a nonoverlapping clock signal with frequency f_{clk} and period T (see Ch. 14). Let's begin by considering the case when

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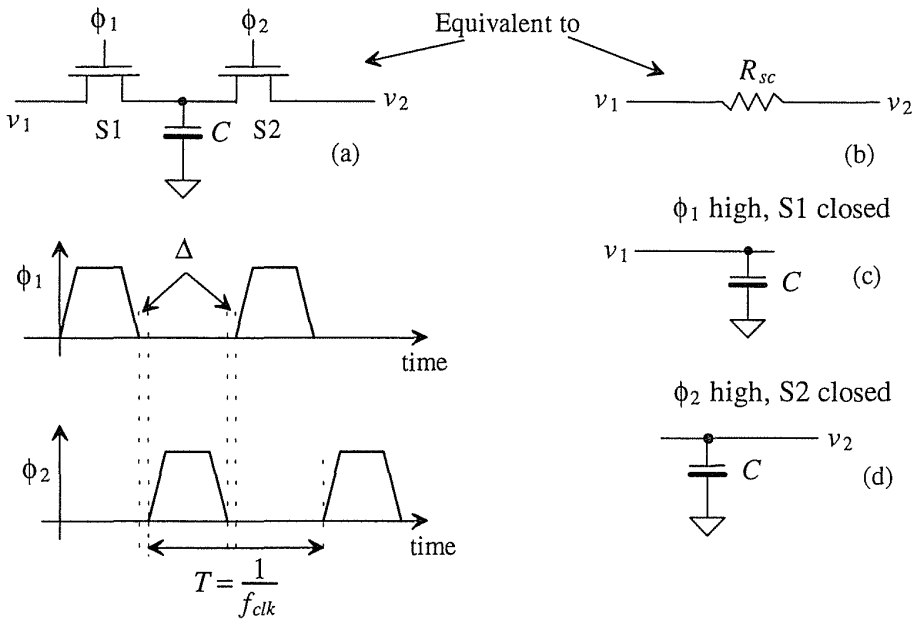


Figure 27.14 Switched-capacitor resistor (a) and associated waveforms, and (b, c, d) the equivalent circuits.

S1 is closed. When ϕ_1 is high, the capacitor C is charged to v_1. The charge, q_1, stored on the capacitor during this interval, Fig. 27.14c, is

$$q_1 = Cv_1 \tag{27.9}$$

while if S2 is closed, the charge stored on the capacitor is

$$q_2 = Cv_2 \tag{27.10}$$

If v_1 and v_2 are not equal, keeping in mind that S1 and S2 cannot be closed at the same time due to the nonoverlapping clock signals, then a charge equal to the difference between q_1 and q_2 is transferred between v_1 and v_2 during each interval T. The difference in the charge is given by

$$q_1 - q_2 = C(v_1 - v_2) \tag{27.11}$$

If v_1 and v_2 vary slowly compared to f_{clk}, then the average current transferred in an interval T is given by

$$I_{avg} = \frac{C(v_1 - v_2)}{T} = \frac{v_1 - v_2}{R_{sc}} \tag{27.12}$$

where the resistance of the switched-capacitor circuit is given by

$$R_{sc} = \frac{T}{C} = \frac{1}{Cf_{clk}} \tag{27.13}$$

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In general, the signals v_1 and v_2 should be bandlimited to a frequency at least ten times less than f_{clk} (more on this later).

Example 27.1

Using switched-capacitor techniques, implement the circuit shown in Fig. 27.15a so that the product of RC is 1 ms, that is, the 3-dB frequency of $|v_{out}/v_{in}|$ is 159 Hz.

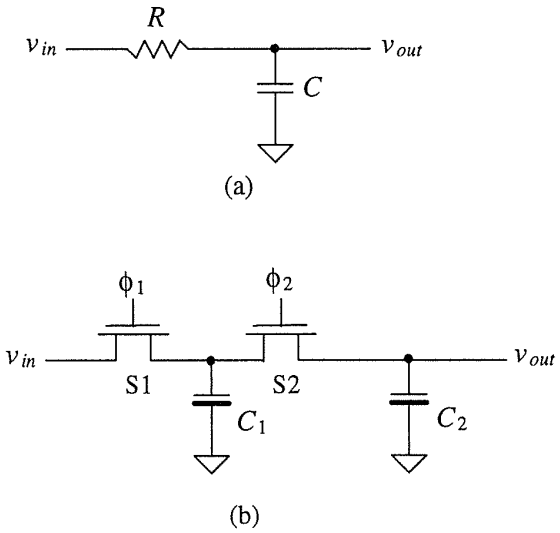


Figure 27.15 (a) Circuit used in Ex. 27.1 and (b) its implementation using a SC resistor.

The switched-capacitor implementation of this circuit is shown in Fig. 27.15b. The product of RC may now be written in terms of Eq. (27.5) as

$$RC_2 = \frac{C_2}{C_1} \cdot \frac{1}{f_{clk}} \tag{27.14}$$

This result is important! The product RC_2 is determined by f_{clk}, which may be an accurate frequency derived from a crystal oscillator and the ratio of C_2 to C_1, which will be within 1 percent on a chip. This means that even if the values of the capacitors change by 20 percent from wafer to wafer, the ratio of the capacitors relative to one another, on the same wafer, will remain constant within 1 percent.

It is also desirable to keep C_1 larger than the associated parasitics present in the circuit (e.g., depletion capacitances of the source/drain implants and the stray capacitances to substrate). For the present example, we will set C_1 to 1 pF. The selection of f_{clk} is usually determined by what is available. For the present design, a value of 100 kHz will be used. This selection assumes that the energy present in v_{in} at frequencies above 10 kHz is negligible. The value of C_2 is determined solving Eq. (27.14) and is 100 pF. Note that the value of the

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switched-capacitor resistor is 10 MΩ. Implementing this resistor in the CN20 process using n-well would require 4,000 squares! The resulting delay through the n-well resistor, because of the capacitance to substrate, may cause a significant phase error in the transfer function as well. ■

27.2.1 Switched-Capacitor Integrator

Because the switched-capacitor resistor of Fig. 27.14a is sensitive to parasitic capacitances, it finds little use in mainly switched-capacitor circuits. Consider the circuit of Fig. 27.16a. This circuit is a switched-capacitor integrator and is the heart of the circuits we will be discussing in the remainder of the section [11]. The portion of the circuit consisting of switches S1 through S4 and C_I forms a switched-capacitor resistor with a value given by

$$R_{sc} = \frac{1}{C_I f_{clk}} \tag{27.15}$$

The equivalent continuous time circuit for the switched-capacitor integrator is shown in Fig. 27.16b. Notice that v_{in} is now negative. It may be helpful in the following discussion to remember that the combination of switches and C_I of the switched-capacitor integrator can be thought of as a simple resistor. The transfer function of the switched-capacitor integrator is given by

$$\frac{v_{out}}{v_{in}} = \frac{1/j\omega C_F}{R_{sc}} = \frac{1}{j\omega\left(\frac{C_F}{C_I} \cdot \frac{1}{f_{clk}}\right)} \tag{27.16}$$

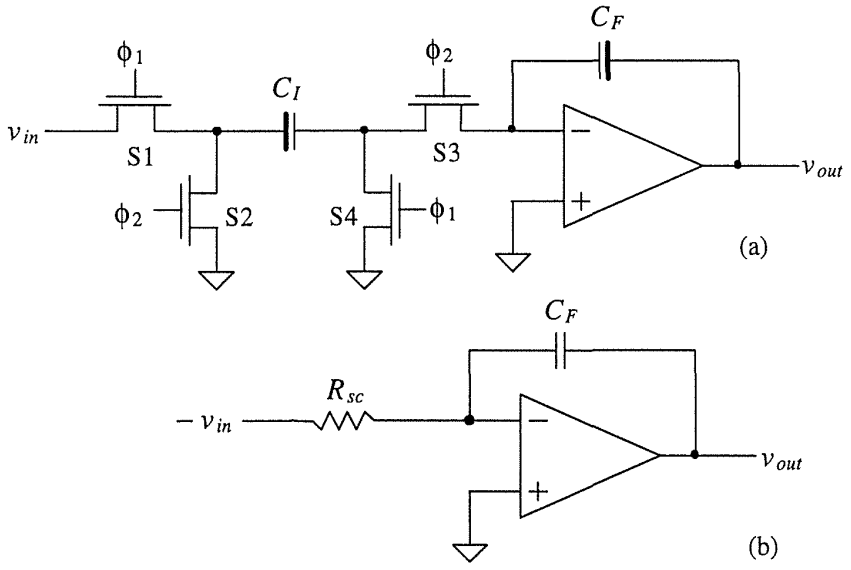


Figure 27.16 (a) A stray insensitive switched-capacitor integrator (noninverting) and (b) the equivalent continuous time circuit.

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Again, the ratio of capacitors is present, allowing the designer to precisely set the gain of the amplifier and the integration time constant.

As we mentioned, the switched-capacitor integrator is not sensitive to parasitic or stray capacitances. This can be understood with the use of Fig. 27.17. First, if we realize that C_{p2} (the parasitic capacitance from the right side of C_I to ground) is always connected to ground either through S4 or by the virtual ground on the inverting input of the op-amp, it cannot store a charge (both sides of C_{p2} are connected to ground). The capacitance C_{p1} is charged to v_{in} when S1 is closed and then discharged to ground when S2 closes. Since none of the charge stored on C_{p1} when S1 is closed is transferred to C_I, it does not affect the integrating function. A practical minimum for C_I is 100 fF in the CN20 process.

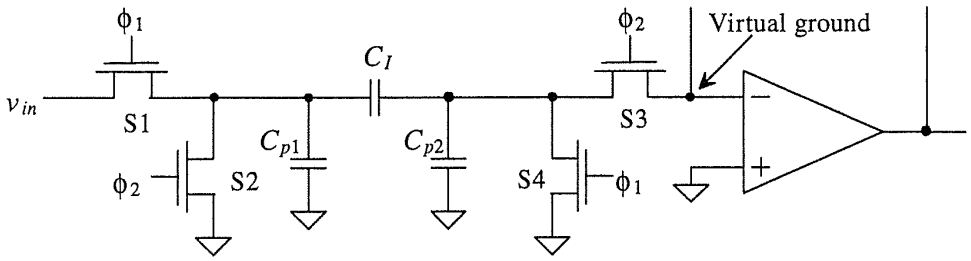


Figure 27.17 Parasitic capacitances associated with a switched-capacitor resistor.

The inverting integrator configuration is shown in Fig. 27.18. Note the simple change of clock signals (S1 and S2) from Fig. 27.16 (the noninverting configuration). The gain of this configuration is given by

$$\frac{v_{out}}{v_{in}} = -\frac{1}{j\omega\left(\frac{C_F}{C_I}\cdot\frac{1}{f_{clk}}\right)} \tag{27.17}$$

An example of a switched-capacitor integrator circuit that combines input signals is shown in Fig. 27.19a. Remembering that each switched-capacitor section can be thought of as a resistor, we note that the relationship between the inputs and output is

$$v_{out} = \frac{v_1}{j\omega\left(\frac{C_F}{C_1}\frac{1}{f_{clk}}\right)} + \frac{v_2}{j\omega\left(\frac{C_F}{C_2}\frac{1}{f_{clk}}\right)} - \frac{v_3}{j\omega\left(\frac{C_F}{C_3}\frac{1}{f_{clk}}\right)} \tag{27.18}$$

Figure 27.19b shows how redundant switches can be combined to reduce the number of devices used. Used alone, the basic integrator has the practical problem of integrating not only the input signal but also the offset voltage of the op-amp. In many applications, a reset switch or resistor is placed across the feedback capacitor (Fig. 27.19b). An example of a lossy integrator circuit useful in first-order filter design is shown in Fig. 27.20. The transfer function of this circuit is given by

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$$\frac{v_{out}}{v_{in}} = \frac{R_4}{R_3}\left(\frac{1+j\omega R_3 C_1}{1+j\omega R_4 C_2}\right) = \frac{C_3}{C_4}\left(\frac{1+j\omega\left(\frac{C_1}{C_3}\cdot\frac{1}{f_{clk}}\right)}{1+j\omega\left(\frac{C_2}{C_4}\cdot\frac{1}{f_{clk}}\right)}\right) \tag{27.19}$$

For low-frequency input signals (low frequencies compared to the pole and zero given in Eq. (27.19), the gain of the lossy integrator is simply

$$\frac{v_{out}}{v_{in}} = \frac{C_3}{C_4} \tag{27.20}$$

which is again a precise number due to the ratio of the capacitors. Also note that the switched-capacitor resistor in the feedback loop is stray insensitive. The left side of C_4 is always connected to 0 V, while the right side is either connected to ground or to the output of the op-amp.

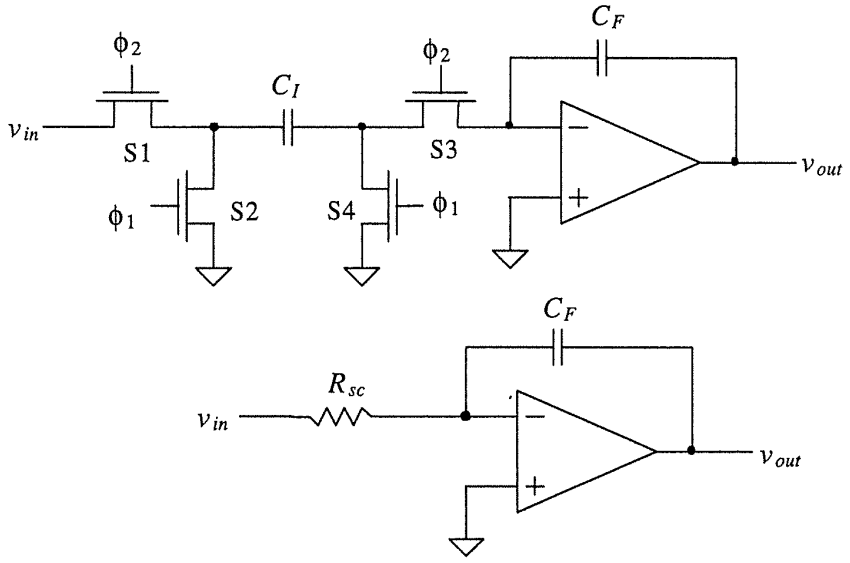


Figure 27.18 A stray insensitive switched-capacitor integrator (inverting).

Example 27.2

Design a switched-capacitor filter with the transfer characteristics shown in Fig. Ex27.2.

We can see that this transfer function has a pole at 500 Hz and a zero at 5 kHz. The lossy integrator of Fig. 27.20 will be used to realize this filter. The low-frequency gain of this circuit is 10 (20 dB). Using Eq. (27.20), we have

$$\frac{C_3}{C_4} = 10$$

while the pole and zero locations are given by

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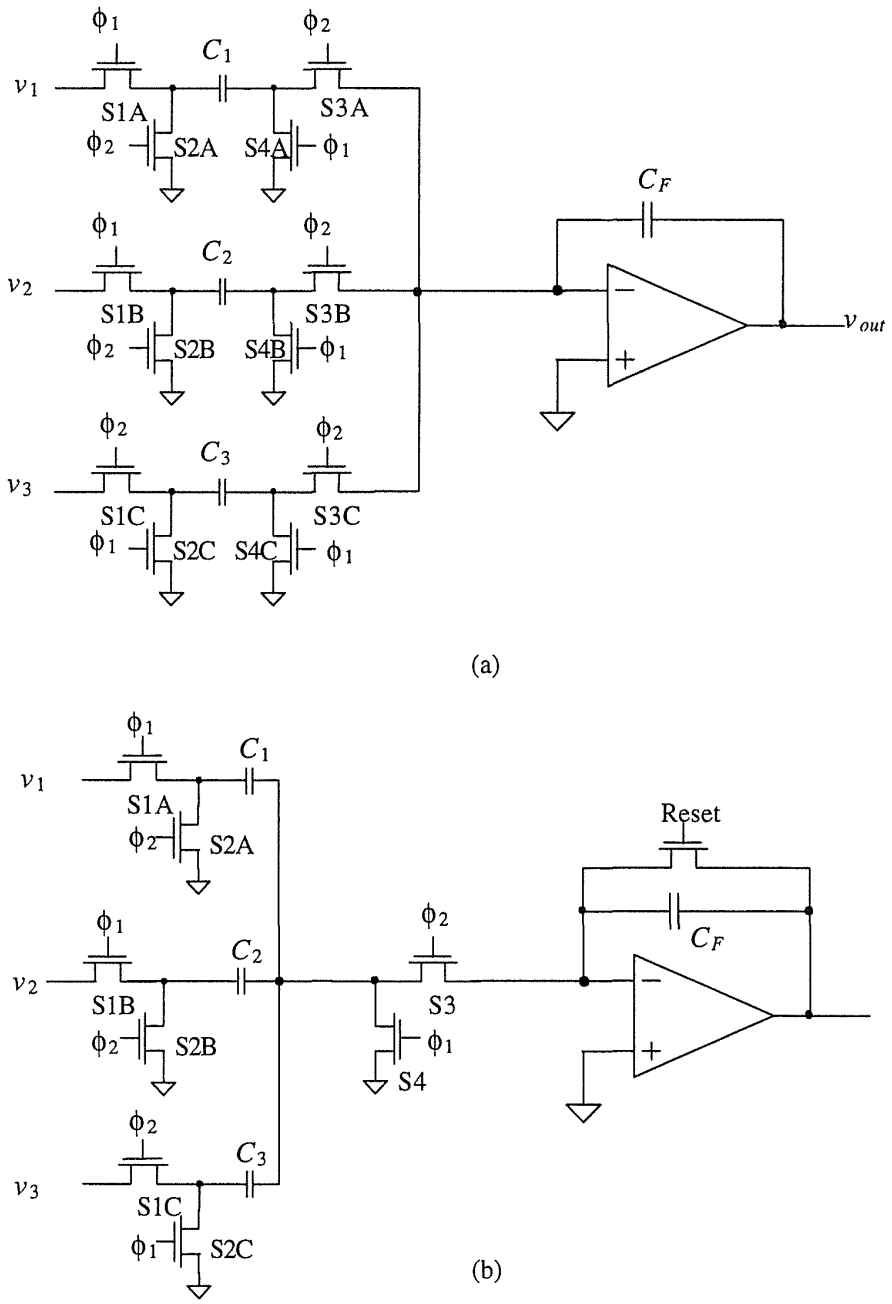


Figure 27.19 (a) Switched-capacitor implementation of a summing integrator and (b) practical implementation of the circuit combining switches and adding reset.

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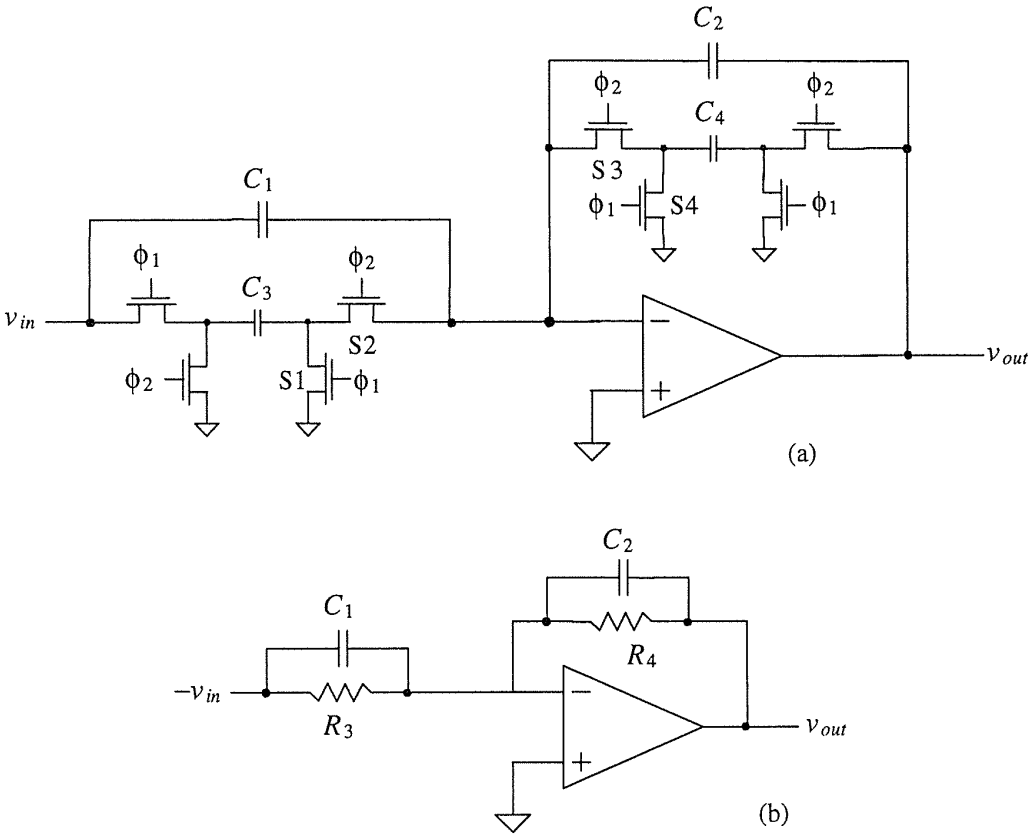


Figure 27.20 Lossy integrator (a) switched-capacitor implementation and (b) continuous time circuit.

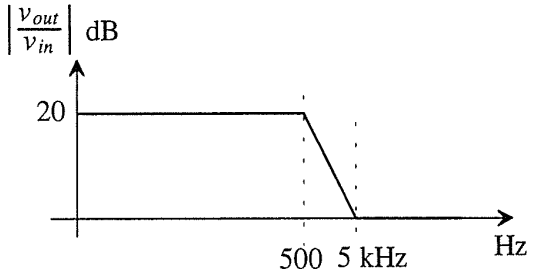


Figure Ex27.2

$$f_p = \frac{1}{2\pi\left(\frac{C_2}{C_4}\cdot\frac{1}{f_{clk}}\right)} = 500 \text{ and } f_z = \frac{1}{2\pi\left(\frac{C_1}{C_3}\cdot\frac{1}{f_{clk}}\right)} = 5 \text{ kHz}$$

If we set f_{clk} to 100 kHz and C_4 to 100 fF, then C_3 = 1.0 pF, C_2 = 3.2 pF, and C_1 = 3.2 pF. ■

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We will now develop an exact relationship between the switching frequency, f_{clk}, and the signal frequency ω [12,13]. Referring to Fig. 27.21, we can write the output of the integrator as the sum of the previous output voltage, $v_{out(n)}$, at a time nT and the contribution from the current sample as

$$v_{out(n+1)} = v_{out(n)} + \frac{C_I}{C_F} \cdot v_{in(n)} \tag{27.21}$$

Since a delay in the time domain of T corresponds to a phase shift of ωT in the frequency domain, we can take the Fourier transform of this equation and get

$$e^{j\omega T} v_{out}(j\omega) = v_{out}(j\omega) + \frac{C_I}{C_F} \cdot v_{in}(j\omega) \tag{27.22}$$

Solving this equation for v_{out}/v_{in} gives

$$\frac{v_{out}}{v_{in}}(j\omega) = \frac{C_I}{C_F}\left(\frac{1}{e^{j\omega T} - 1}\right) = \frac{C_I}{C_F}\left(\frac{e^{-j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}\right) = \frac{C_I}{C_F}\left[\frac{1}{z-1}\right] \tag{27.23}$$

where $z = e^{j\omega T}$. Remembering $f_{clk} = 1/T$ and $\omega = 2\pi f$, we get

$$\frac{v_{out}}{v_{in}}(j\omega) = \frac{1}{j\omega\left(\frac{C_F}{C_I} \cdot \frac{1}{f_{clk}}\right)}\left(\frac{\frac{\pi f}{f_{clk}}}{\sin\frac{\pi f}{f_{clk}}} \cdot e^{-j\pi f/f_{clk}}\right) \tag{27.24}$$

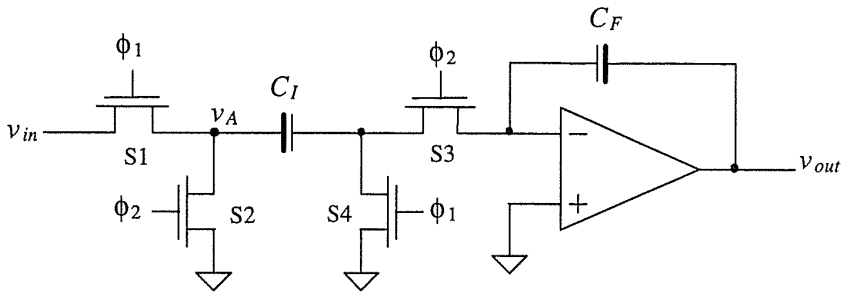
Ideally, the term on the right in parentheses is unity. This occurs when f is much less than f_{clk}. This equation describes how the magnitude and phase of the integrator are affected by finite f_{clk}.

Capacitor Layout

An important step in the implementation of any switched-capacitor design is the layout of the capacitors. Normally, a unit size capacitor is laid out and then replicated to the desired capacitance. For the previous example, the unit size capacitance would be nominally 100-fF; see Fig. 27.22 (Fig. 7.10)[1]. Again, the absolute value of the capacitors isn't important; rather, the important value is the ratio. A total of 32 of these unit size capacitors would be used to achieve the larger nominally 3.2 pF capacitors in the previous example (see Fig. 27.23). Using this approach eliminates errors due to uneven patterning of poly to a first order. A p+ guard ring is placed around the capacitor to help reduce coupled substrate noise. Substrate noise can also be reduced by laying the capacitor out over an n-well that is tied to *VDD*. Injected minority carriers are collected either by the p+ or the n-well (or a combination of both). If matching of the capacitors is critical, schemes that use a common-centroid layout can be used. Also, as was discussed in Ch. 20, dummy poly strips or capacitors can be placed around the array of capacitors so that the edge differences from underetching poly are eliminated.

[1] Note that here we are assuming that a circle can be accurately reproduced on the reticle and patterned on the wafer. In practice, effects such as the finite e-beam size (and the granularity of the grid) used to make the reticle can make this assumption questionable.

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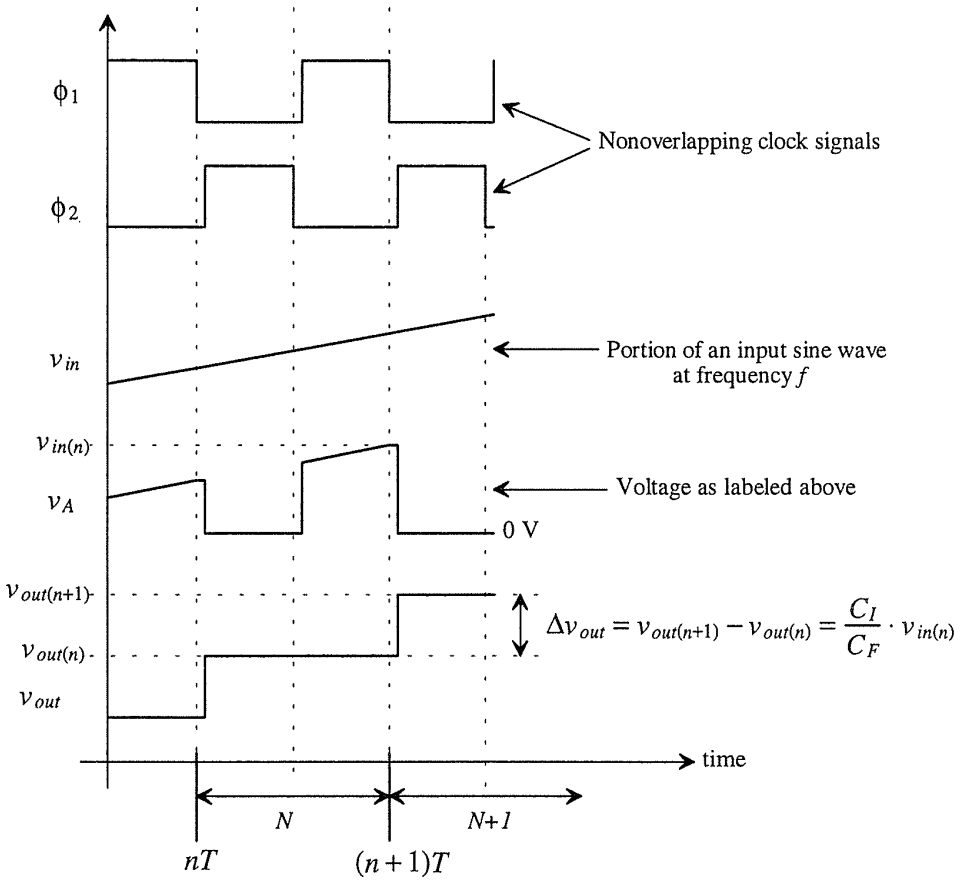
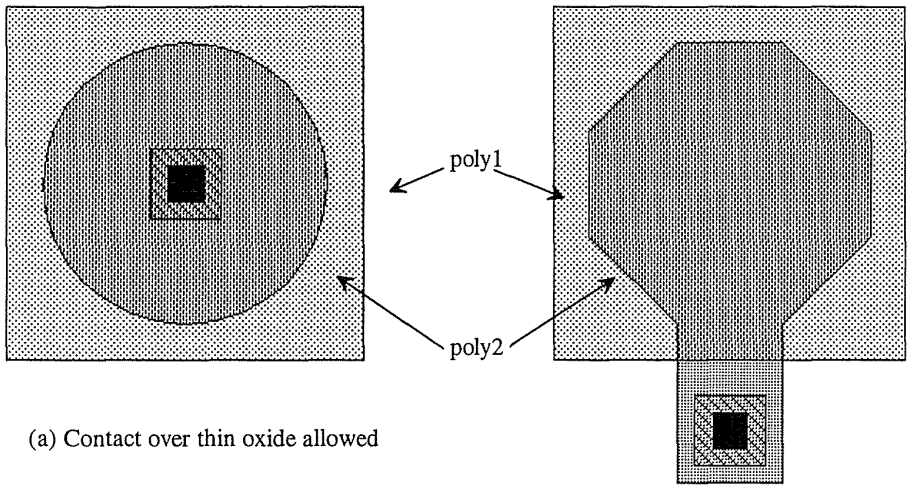


Figure 27.21 Switched-capacitor integrator used to determine the relationship between input frequency and switch clock frequency.

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(a) Contact over thin oxide allowed

(b) Contact over thin oxide not allowed

Figure 27.22 Layout of a nominally 100 fF capacitor unit cell.

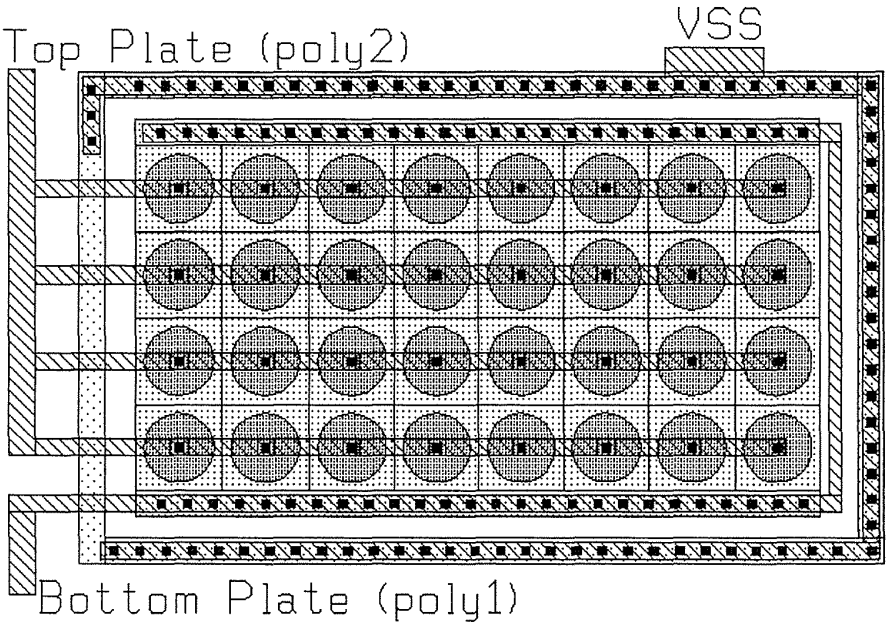


Figure 27.23 Layout of a 3.2 pF capacitor using a 100 fF unit cell.

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Implementing Ladder Filters

Consider the ladder low-pass filter shown in Fig. 27.24. The doubly terminated structure is used to reduce sensitivity to component variations [14]. The resistors R_1 and R_5 will be implemented using switched-capacitor techniques along with the inductor and capacitors shown in the schematic. With regard to the notation shown in the figure, the voltage across L_3 and the current through L_3 are labeled v_3 (= v_2 – v_4) and i_3, respectively. Also, we will define the product of the current through the inductor with a scaling resistance, R_s (normally R_s = 1 Ω) as the inductor scaled voltage. This can be written for L_3 as

$$v_3' = i_3 \cdot R_s \tag{27.25}$$

For the capacitor C_2 in Fig. 27.24, we can write

$$v_2 = \frac{i_2}{j\omega C_2} = \frac{1}{j\omega C_2}(i_1 - i_3) = \frac{v_s}{j\omega C_2 R_1} - \frac{v_2}{j\omega C_2 R_1} - \frac{v_3'}{j\omega C_2 R_s} \tag{27.26}$$

which results in a summing integrator, that is, C_2 is replaced with a switched-capacitor summing integrator (see Fig. 27.25a). The value of the capacitors in this figure is determined using

$$C_2 R_1 = \frac{C_{F2}}{C_{21}} \cdot \frac{1}{f_{clk}} \tag{27.27}$$

$$C_2 R_s = \frac{C_{F2}}{C_{22}} \cdot \frac{1}{f_{clk}} \tag{27.28}$$

For the inductor L_3 we can write

$$v_3' = R_s \cdot i_3 = \frac{v_2}{j\omega L_3/R_s} - \frac{v_4}{j\omega L_3/R_s} \tag{27.29}$$

This is again a summing integrator (see Fig. 27.25b). The value of the components in this figure are determined by solving

$$\frac{L_3}{R_s} = \frac{C_{F3}}{C_{31}} \cdot \frac{1}{f_{clk}} \tag{27.30}$$

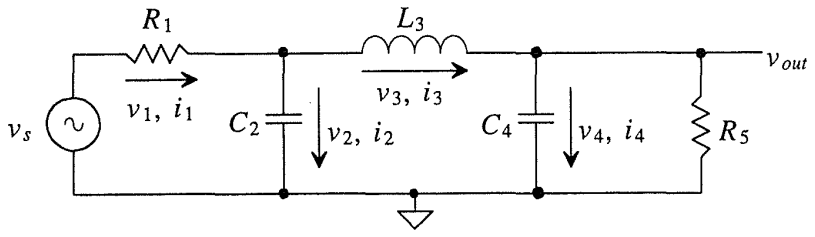


Figure 27.24 Doubly terminated low-pass ladder filter.

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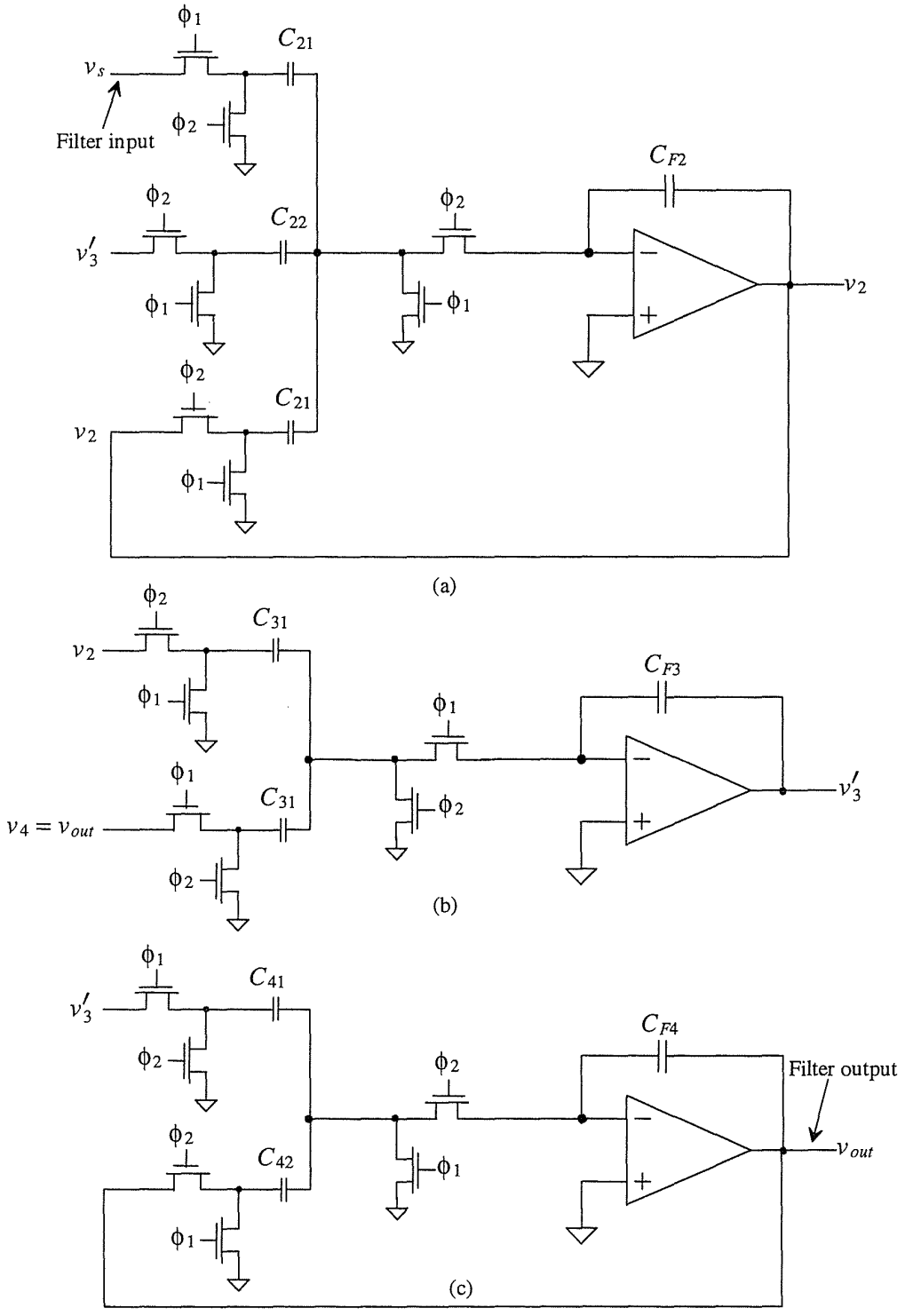


Figure 27.25 (a) Switched-capacitor implementation of R1 and C2 in Fig. 27.24, (b) Switched-capacitor implementation of L3 in Fig. 27.24, and (c) implementation of C4, R5.

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Notice that we have switched the phase of the clock signals, ϕ_1 and ϕ_2, in Fig. 27.25b from Fig. 27.25a (look at the switches directly adjacent to the op-amp). This makes the output of the circuit in (a) immediately available to the input of (b) without a time delay, T (= $1/f_{clk}$). For the voltage v_4 (= v_{out}), we can write

$$v_4 = \frac{i_3 - i_5}{j\omega C_4} = \frac{v_3'}{j\omega C_4 R_s} - \frac{v_{out}}{j\omega C_4 R_5} = v_{out} \tag{27.31}$$

where

$$C_4 R_s = \frac{C_{F4}}{C_{41}} \cdot \frac{1}{f_{clk}} \tag{27.32}$$

and

$$C_4 R_5 = \frac{C_{F4}}{C_{42}} \cdot \frac{1}{f_{clk}} \tag{27.33}$$

The implementation of this section of the ladder filter is shown in Fig. 27.25c. Again, notice that the clock phases have been switched from the previous section of the filter. The complete filter of Fig. 27.24 is realized by combining the three sections (one section for each reactive component) shown in Fig. 27.25.

Op-Amp Settling Time

Figure 27.26 shows an op-amp configuration in which the op-amp can source or sink current to a switched-capacitor and a feedback capacitor. The time it takes to charge and discharge these capacitors is important since it directly affects the maximum switched capacitor clocking frequency, f_{clk}. The slew-rate limitations of the op-amp have been discussed in detail already. Let's now consider the limitations due to op-amp finite bandwidth. The closed-loop gain of the op-amp is given by

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL} \cdot \beta} \tag{27.34}$$

while the open-loop gain of an op-amp is given, with units of A/A, V/V, V/A, or A/V, by

$$A_{OL} = \frac{A_{OL}(0)}{1 + j\frac{f}{f_{3dB}}} \tag{27.35}$$

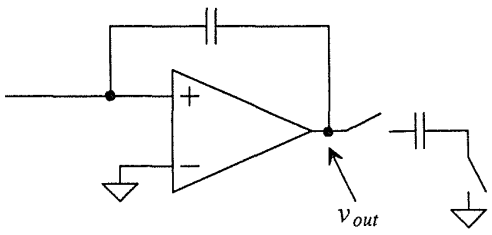


Figure 27.26 Charging and discharging a switched capacitor.

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Combining these equations and assuming $1 >> 1/[\beta \cdot A_{OL}(0)]$, we get

$$A_{CL} = \frac{\frac{1}{\beta}}{1 + j\frac{f}{f_u \cdot \beta}} \tag{27.36}$$

where $f_{3dB} \cdot A_{OL}(0) = f_u$, where f_u may have units of Hz, Hz/Ω, or Hz·Ω ($f_u\beta$ is in Hz). The closed-loop gain reduces to a simple single-pole transfer function. The low-frequency gain of the circuit is $1/\beta$, while the product of f_u and β gives the circuit time constant of

$$\tau = \frac{1}{2\pi f_u \cdot \beta} \tag{27.37}$$

keeping in mind the unity-gain frequency of the op-amp, f_u, is a strong function of the load capacitance. For a step-input to the op-amp, a common occurrence in switched-capacitor circuits (Fig. 27.21), the output voltage of the op-amp, again neglecting slew-rate limitations, is given by

$$v_{out} = V_{outfinal}(1 - e^{-t/\tau}) \tag{27.38}$$

For the output voltage of the op-amp to settle to less than 1 percent of its final value requires 5τ. A "rule-of-thumb" estimate for the settling time is simply $1/(f_u \cdot \beta)$.

Differential Output Op-Amps

As mentioned previously, fully differential op-amps are a necessity in any modern mixed-signal CMOS integrated circuit design, including switched-capacitor circuits. The benefits of fully differential design can be summarized and listed as follows.

1. *Input common-mode voltage remains at V_{CM}.* This benefit eases the requirements on the CMR of the diff-amp used in an op-amp. For example, if V_{CM} is 2.5 V, the inputs of the op-amp will remain at 2.5 V. This holds for all fully differential circuit topologies using the differential output op-amp. An example of an application where a fully differential op-amp is not used in a fully differential topology is the single to differential converter shown in Fig. 26.33b. For this circuit, the inputs to the op-amp will not remain at V_{CM}.

2. *A doubling in the output voltage swing.* This point can be understood by considering the case when $VDD = -VSS = 2.5$ V and $V_{CM} = 0$. For a single-ended output op-amp, the maximum output voltage is 2.5 V. However, for the differential-output op-amp when v_{o+} is 2.5 V, we have a v_{o-} of –2.5 V, giving a total output voltage of $v_{o+} - v_{o-}$ or 5 V. The result is an increase in the dynamic range of circuits employing fully differential signal paths.

3. *A reduction in harmonic distortion.* The even order harmonic distortion terms are canceled in a fully differential topology when we take the difference in the + and – output voltages.

4. *Substrate and coupled noise rejection.* Ideally, since the output signal lines are laid out close to one another, noise introduced from the substrate or other signal

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lines appears as a common signal on the outputs of the op-amp and is eliminated when we take the difference between the two signals.

A fully differential op-amp (actually an OTA) topology useful in switched-capacitor circuits is shown in Fig. 27.27. This configuration is based on the topology given in [15]. The input diff-amp is the class AB source cross-coupled pair discussed in Ch. 24 that eliminates slew-rate limitations. Wide-swing current mirrors are employed to increase output voltage swing and for operation at lower power suppy voltages (e.g., 3.3 V). Note that one of the major problems of using the source cross-coupled pair, discussed in Ch. 24, was the small-input common-mode range. However, after reviewing number 1 above, we see that this is not a concern in a fully differential topology. Again, the main drawbacks of using the source cross-coupled pair are the increase in power dissipation (assuming the same biasing currents) and noise (thermal and 1/f).

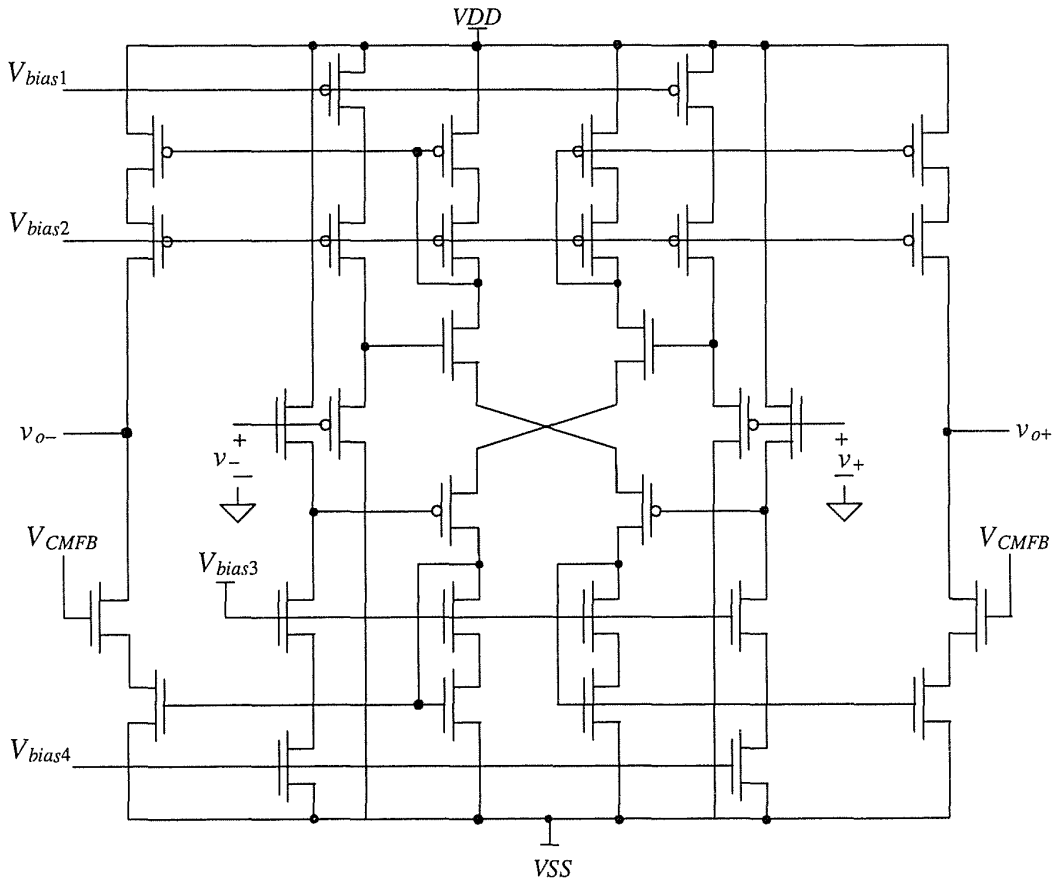


Figure 27.27 Fully differential op-amp topology, without slew-rate limitations, useful in switched-capacitor circuits.

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The common-mode-feedback-circuit can be implemented using the continuous time techniques that were discussed in Ch. 25 or using switched-capacitor techniques [15] (see Fig. 27.28). The clock signals in this figure are, again, nonoverlapping. When the ϕ_1 switches are closed, the charge stored on the two C_1 capacitors is $2C_1(V_{CM} - V_{bias3})$, while the charge stored on the C_2 capacitors is $C_2(v_{o+} - V_{CMFB}^{\phi_1}) + C_2(v_{o-} - V_{CMFB}^{\phi_1})$, or simply

$$2C_2\left[\frac{v_{o+} + v_{o-}}{2} - V_{CMFB}^{\phi_1}\right] \tag{27.39}$$

where $V_{CMFB}^{\phi_1}$ is the output of the CMFB circuit when the ϕ_1 switches are closed. When the ϕ_2 switches close, since charge must be conserved, we can write

$$2C_2\left[\frac{v_{o+} + v_{o-}}{2} - V_{CMFB}^{\phi_1}\right] + 2C_1(V_{CM} - V_{bias3}) = (C_1 + C_2)\left[(v_{o+} - V_{CMFB}^{\phi_2}) + (v_{o-} - V_{CMFB}^{\phi_2})\right] \tag{27.40}$$

and

$$C_1(V_{CM} - \frac{v_{o+} + v_{o-}}{2} + V_{CMFB}^{\phi_2} - V_{bias3}) + C_2(V_{CMFB}^{\phi_2} - V_{CMFB}^{\phi_1}) = 0 \tag{27.41}$$

When the outputs of the op-amp are balanced, $V_{CMFB}^{\phi_2} = V_{CMFB}^{\phi_1} = V_{bias3}$, and the average of the outputs, that is, $(v_{o+} + v_{o-})/2$, is equal to the common-mode voltage V_{CM}. If the average of the outputs is greater than V_{CM}, then $V_{CMFB}^{\phi_2}$ becomes greater than $V_{CMFB}^{\phi_1}$, having the effect of lowering the average output voltages while the opposite is true if the average of the outputs is less than V_{CM}. The maximum size of C_2 is based on how much loading can be tolerated on the output of the OTA, while the size of C_1 is determined by the desired response needed in the CMFB circuit. Generally, C_1 is around one-tenth of C_2. The minimum size of the capacitors is set by charge injection and kT/C noise considerations. Note that the switches connected to v_{o+} and v_{o-} can be TGs, so that the circuit can operate from *VDD* to *VSS*.

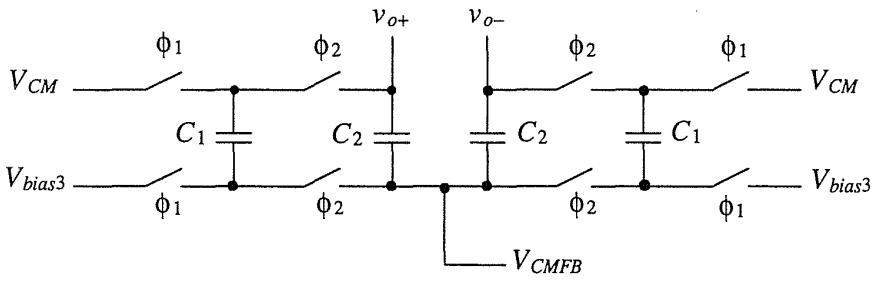


Figure 27.28 A switched-capacitor CMFB circuit.

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27.3 Circuits

This section presents several examples of dynamic circuits.

Reducing Offset Voltage of an Op-Amp

The op-amp offset voltage can be modeled by adding a DC voltage in series with the noninverting input of the op-amp; see Fig. 27.29a [16]. The basic idea behind eliminating the offset voltage is shown in Fig. 27.29b. A capacitor is charged to a voltage equal and opposite to the comparator offset voltage. The dynamic analog circuit shown in Fig. 27.30 is used to help eliminate the effects of the offset voltage. Note that for this method to be effective *the op-amp must be stable* in the unity gain configuration. The clock signals ϕ_1 and ϕ_2 are the nonoverlapping clock signals discussed in Ch. 14. A nonoverlapping clock keeps switches S1, S2, and S3 from being on at the same time as switches S4 and S5. Let's consider the case shown in Fig. 27.30b where ϕ_1 is high and ϕ_2 is low. The op-amp, via the negative feedback, forces its output to zero volts. Doing so the capacitor is charged, in the polarity shown, to V_{OS}. Note that under these conditions the op-amp is removed from the inputs. When ϕ_2 is high and ϕ_1 is low, Fig. 27.30c, the op-amp functions normally, assuming the storage capacitance C is much larger than the input capacitance of the comparator.

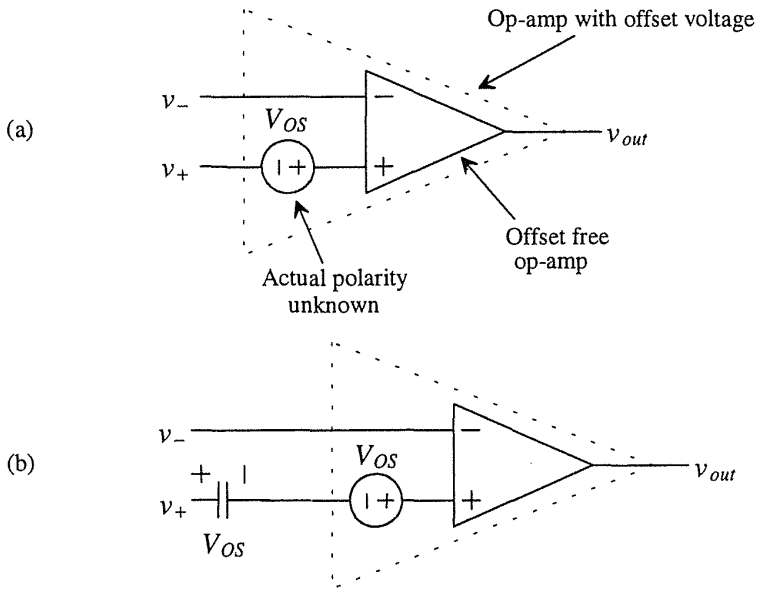


Figure 27.29 (a) Offset voltage of an op-amp modeled by a DC voltage source in series with the noninverting input of the op-amp and (b) using a capacitor to cancel the offset voltage.

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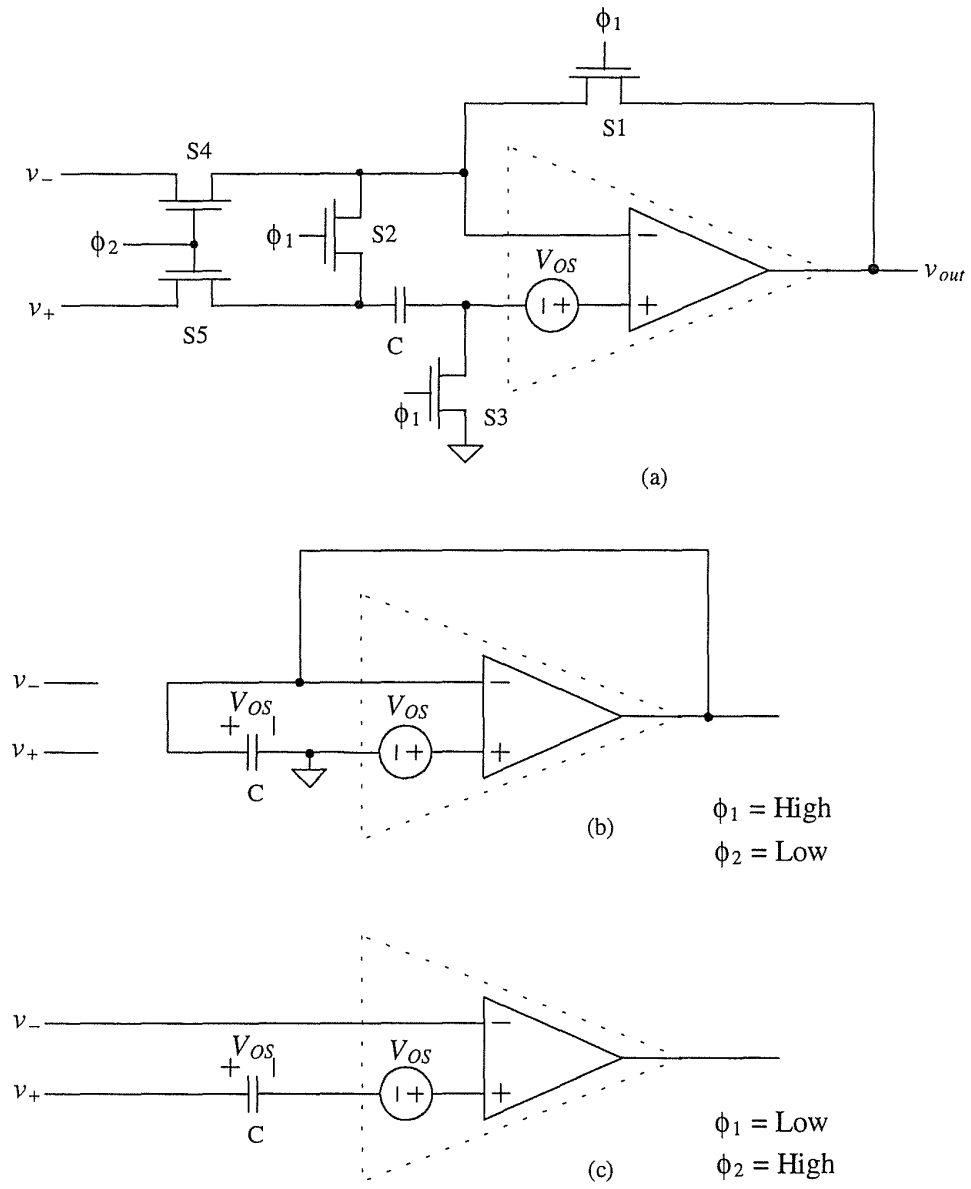


Figure 27.30 Dynamic reduction of the offset voltage.

Dynamic Comparator

Before we present a dynamic comparator, let's consider the *RC* switch circuit of Fig. 27.31a. When node A is connected to +5 V, node B is connected to ground. Consider what happens when the switches change positions, that is, when node A is connected to ground and the switch at node B is connected to an open. At the moment just after switching takes place, the potential at node B becomes – 5 V. In other words, the

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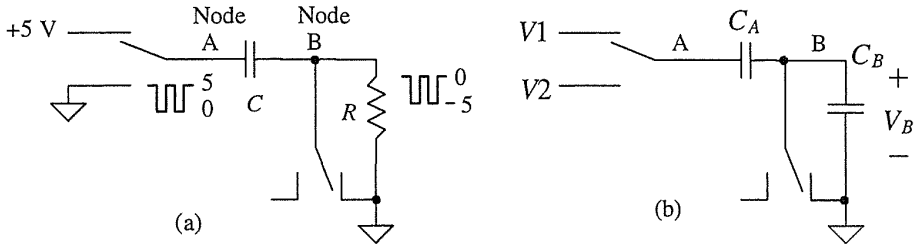


Figure 27.31 Circuits used to illustrate switching in dynamic circuits.

voltage across the capacitor does not change instantaneously. If node A is connected back to + 5 V and node B is connected back to ground a short time compared to the product of R and C, then the voltage across the capacitor remains +5 V.

A more useful circuit for CMOS is shown in Fig. 27.31b. If the switch across C_B is connected to ground when node A is connected to $V1$, then V_B, when the switches change positions, is given by

$$V_B = (V2 - V1) \cdot \frac{C_A}{C_A + C_B} \tag{27.42}$$

Figure 27.32 shows a dynamic comparator based on the inverter [17]. When ϕ_1 is high the voltage on the v_- input is connected to node A, while the voltage on node B is set via S3 so that the input and output voltages of the inverter are equal. (The inverter is operating as a linear amplifier where both M1 and M2 are in the saturation regions.) When ϕ_2 goes high (ϕ_1 is low since the clocks are nonoverlapping), the v_+ input is connected to node A. If C_A is much larger than the input capacitance of the inverter (C_B), then the voltage change on the input of the inverter (V_B) is

$$v_{in} = v_+ - v_- \tag{27.43}$$

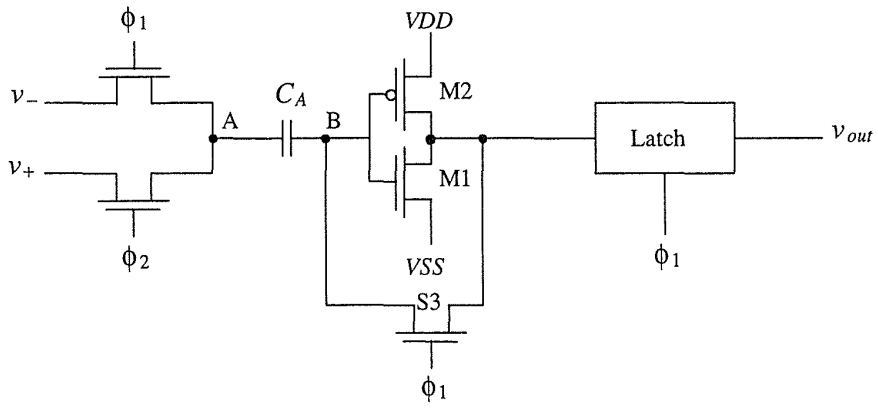


Figure 27.32 A dynamic comparator.

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Provided the gain of the inverter is large, this change causes the inverter output to rail, that is, go to either *VDD* or *VSS*. The output is then latched and available during ϕ_1. The gain of the comparator can be increased by using additional inverter stages.

Another high-performance dynamic comparator configuration is based on the dynamic latch shown in Fig. 27.33 [18]. This latch is used as the positive feedback stage of the comparator. The offset-voltage of the comparator is reduced, using either input offset storage (IOS) or output offset storage (OOS) around the comparator preamp. Figure 27.34 shows the two types of offset cancellation techniques. In the IOS configuration, the preamp must be stable in the unity feedback configuration. Also, the MOSFETs of the preamp must remain in saturation when the offset voltage is stored on the capacitors. If a differential amplifier is used as the preamp this condition is easily met.

The size of the storage capacitors is based on three important considerations: (1) preamp or latch input capacitance, (2) charge injection and (3) kT/C noise. For the IOS scheme the input storage capacitance must be much larger than the input capacitance of the preamp, so that the storage capacitors don't attenuate the input signals. For example, if the storage capacitors have the same capacitance value as the input capacitance of the preamp, then one-half of the input signals reaches the preamp. For the OOS scheme the storage capacitors should be much larger than the input capacitance of the dynamic latch.

Dynamic Current Mirrors

The use of dynamic techniques can significantly reduce the effects of threshold voltage mismatches in current mirrors. Consider the circuit of Fig. 27.35. When ϕ_1 is high and

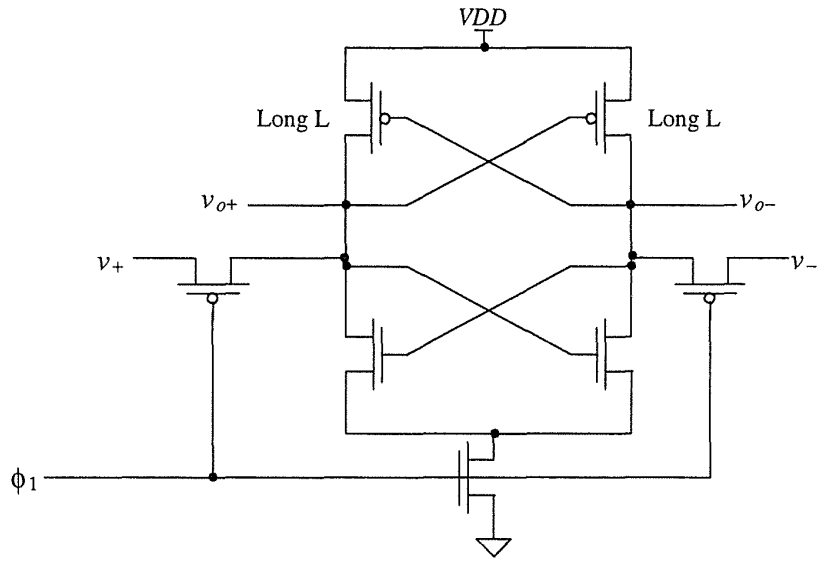


Figure 27.33 Dynamic CMOS latch.

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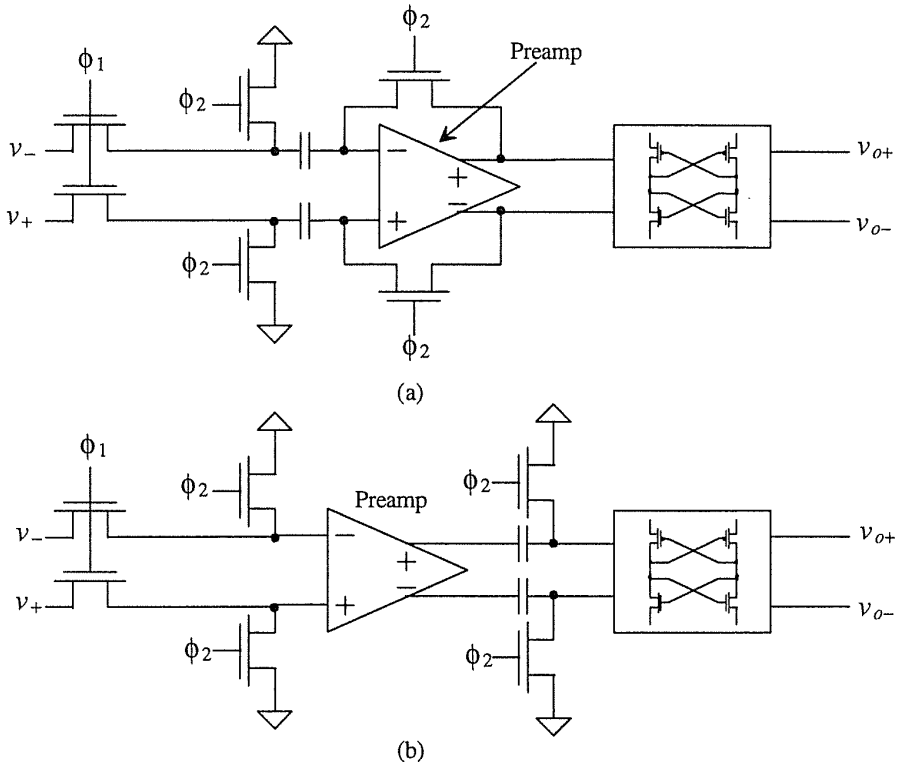


Figure 27.34 (a) Input offset storage (IOS) and (b) Output offset storage (OOS).

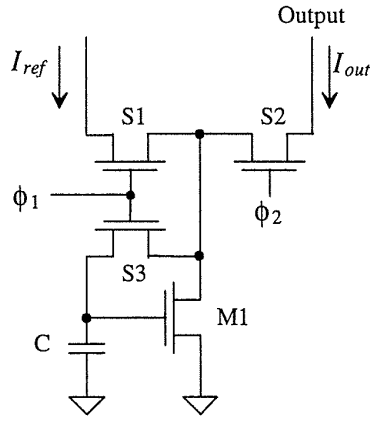


Figure 27.35 Dynamic biasing of a current mirror.

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ϕ_2 is low (again, these clock signals are nonoverlapping), switches S1 and S3 are on while switch S2 is off. A current I_{ref} flows through M1, setting its gate-source voltage. This information [the gate-source voltage (actually the charge) of M1] is stored on C. When S2 closes with S1 and S3 off a current I_{out} equal to I_{ref}, neglecting channel length modulation, flows. This circuit behaves like a current source when ϕ_2 is high and as an open when ϕ_2 is low. The circuit shown in Fig. 27.36 shows a dynamic current mirror that operates continuously. When ϕ_1 is high, M2 sinks current, and when ϕ_2 is high, M1 sinks current. These circuits are useful in eliminating the mismatch effects, and thus differences in the output currents, resulting from threshold voltage and transconductance parameter differences between devices. Since a single-reference current can be used to program the current in a string of current mirrors, only the finite output resistance of the mirrors will cause current differences.

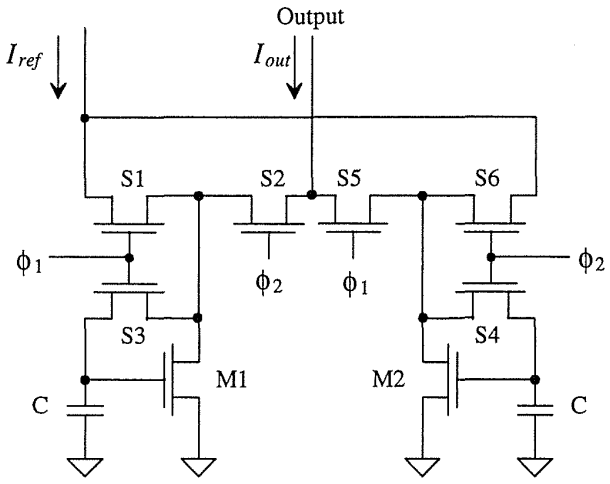


Figure 27.36 Dynamic current mirror that operates during both clock phases.

Dynamic Amplifiers

Figure 27.37 shows a dynamic amplifier. The circuit amplifies when ϕ is low and dynamically biases M1 and M2, and therefore does not amplify, when ϕ is high. If C1 and C2 are large compared to the input capacitance of M1 and M2, then the input AC signal, v_{in}, is applied to both gates. This biasing scheme makes the amplifier less sensitive to threshold and power supply variations. Other dynamic amplifier configurations exist, which have differential inputs and operate over both clock cycles [19].

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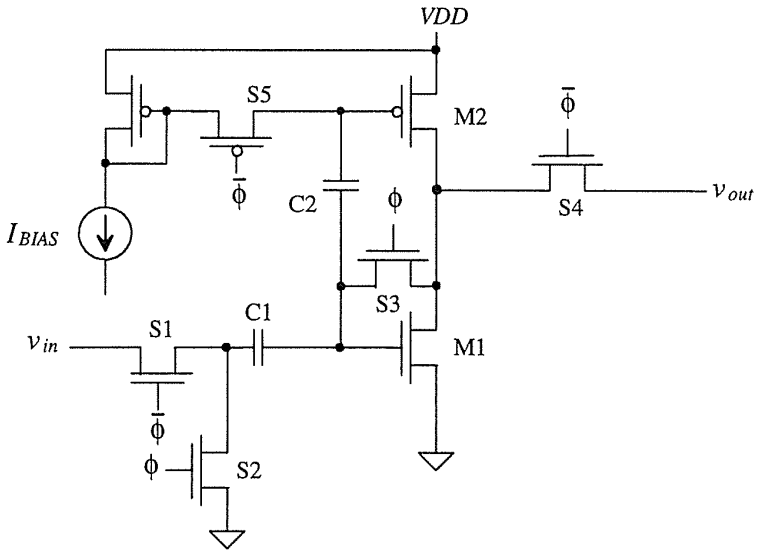


Figure 27.37 Dynamic amplifier used to reduce biasing sensitivity to power supply and threshold voltage.

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PROBLEMS

27.1 Using SPICE simulations, show the effects of clock feedthrough on the voltage across the load capacitor for the switch circuits shown in Fig. P27.1. How does this voltage change if the capacitor value is increased to 100fF ?

27.2 Assuming the small-signal on resistance of a MOSFET ("on" means the MOSFET is operating in the triode region) is given by

$$r_{ds} = \frac{1}{\beta(V_{GS} - V_{THN})}$$

plot, by hand, the small-signal on resistances of minimum size, p-channel, n-channel, and transmission-gate switches. The resulting plot should look similar to Fig. 27.2.

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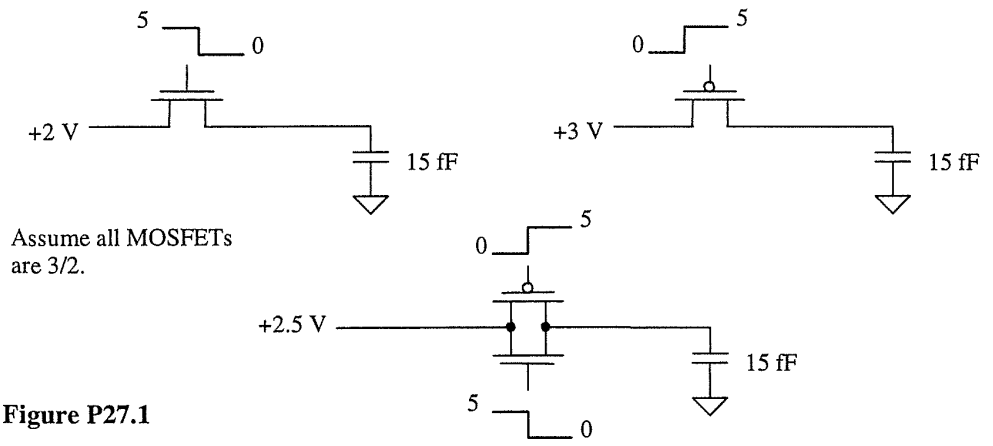


Figure P27.1

27.3 Make a table comparing capacitor size with kT/C noise for capacitor values from 10 fF to 10 pF.

27.4 Sketch the single-ended (output) version of the sample-and-hold amplifier shown in Fig. 27.9 and describe, using timing diagrams, the operation of the circuit.

27.5 Figure P27.5 shows the implementation of a single-ended to differential sample-and-hold. Describe the operation of this circuit using timing diagrams with various input voltages.

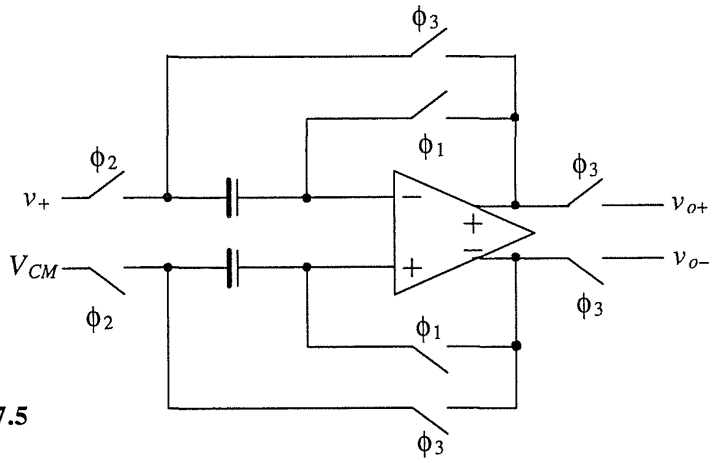


Figure P27.5

27.6 Show that the switched-capacitor circuits shown in Fig. P27.6 behave like resistors, for $f << f_{clk}$, with the resistor values shown.

27.7 Comment on the selection of the bottom plate of the capacitor shown in Fig. 27.14a.

27.8 Comment on the selection of the bottom plate of the capacitor shown in Fig. 27.16.

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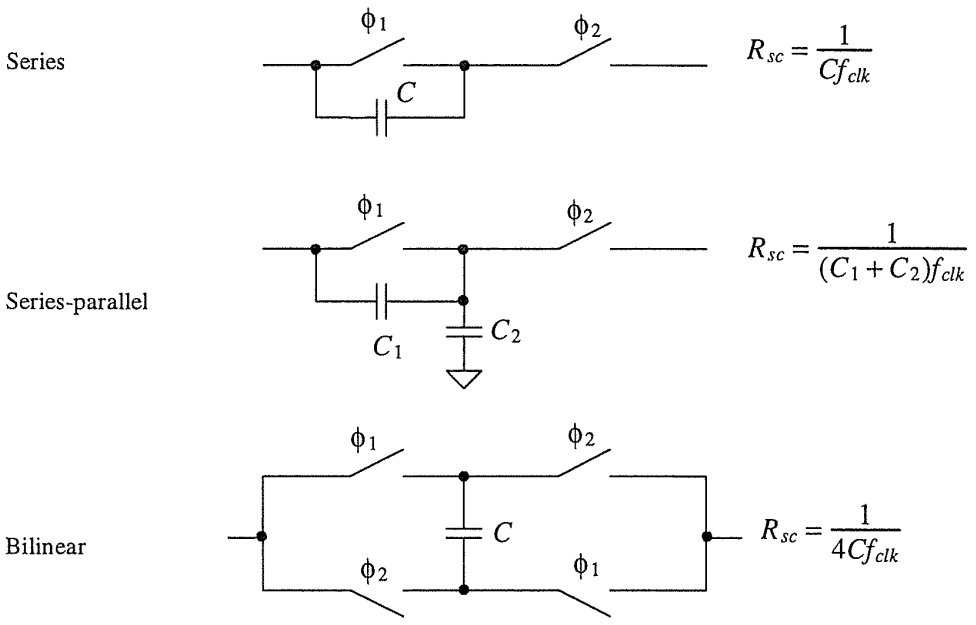


Figure P27.6

27.9 Sketch the schematic, similar in form to Fig. 27.16, of the fully differential switched-capacitor integrator made using a differential input/output op-amp. What is the transfer function of this topology?

27.10 Repeat Ex. 27.2 if the low-frequency gain is 40 dB and the zero is located at 50 kHz.

27.11 Using the results given in Eq. (27.24), plot the magnitude of v_{out}/v_{in} against f/f_{clk}. Comment on the resulting plot.

27.12 An important consideration in SC circuits is the slew-rate requirements of the op-amps used. In the derivation in Fig. 27.21, we assumed that a voltage source was connected to the input of the circuit. In reality, the input of the circuit is provided by an op-amp. When ϕ_1 goes high, in this figure, the capacitor C_I is charged to the input voltage v_{in} (= v_A). If C_I is 5 pF and f_{clk} is 100 kHz, estimate the minimum slew-rate requirements for the op-amp providing v_{in}.

27.13 Suppose the op-amp in Problem 27.12 is used with a feedback factor of 0.5. Estimate the minimum unity gain frequency, f_u, that the op-amp must possess.

27.14 Simulate the operation of the dynamic latch shown in Fig. 27.33.

27.15 Simulate the operation of the current mirror shown in Fig. 27.36.

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Chapter

28

Data Converter Fundamentals

Data converters play an important role in an ever-increasing digital world. As more products perform calculations in the digital or discrete time domain, more sophisticated data converters must translate the digital data to and from our inherent analog world. This chapter introduces concepts of data conversion and sampling which surround this useful circuit.

28.1 Analog Versus Discrete Time Signals

Analog-to-digital converters, also known as A/Ds or ADCs, convert analog signals to discrete time or digital signals. Digital-to-analog converters (D/As or DACs) perform the reverse operation. Figure 28.1 illustrates these two operations. In order to understand the functionality of these data converters, it would be wise first to compare the characteristics of analog versus digital signals.

Examine Fig. 28.1. The original analog signal (a) is filtered by an anti-aliasing filter to remove any high-frequency harmonics that may cause an effect known as aliasing (see Sec. 28.5). The signal is sampled and held and then converted into a digital signal (b). Next the DAC converts the digital signal back into an analog signal

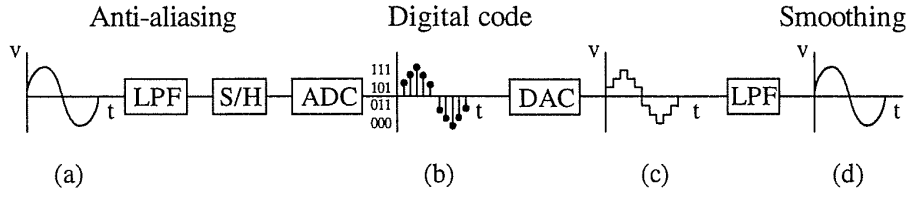


Figure 28.1 Signal characteristics caused by A/D and D/A conversion.

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(c). Note that the output of the DAC is not as "smooth" as the original signal. A low-pass filter returns the analog signal back to its original form (plus phase shift introduced from the conversions) after eliminating the higher order harmonics caused by the conversion. This example illustrates the main differences between analog and digital signals. Whereas the analog signal in Fig. 28.1a is *continuous* and *infinite* valued, the digital signal in (b) is *discrete* with respect to time and *quantized.* The term *continuous-time signal* refers to a signal whose response with respect to time is uninterrupted. Simply stated, the signal has a continuous value for the entire segment of time for which the signal exists. By referring to the analog signal as infinite valued, we mean that the signal can possess any value between the parameters of the system. For example, in Fig. 28.1a, if the peak amplitude of the sine wave was + 5V, then the analog signal can be any value between –5 and 5 V (such as 2.4758393848 V). Of course, measuring all the values between –5 and 5 V would require a piece of laboratory equipment with infinite precision.

The digital signal, on the other hand, is discrete with respect to time. This means that the signal is defined for only certain or discrete periods of time. A signal that is quantized can only have certain values (as opposed to an infinitely valued analog signal) for each discrete period. The signal illustrated in Fig. 28.1b illustrates these qualities.

28.2 Converting Analog Signals to Digital Signals

We have already established the differences between analog and digital signals. How is it possible to convert from an analog signal to a digital signal? An example will illustrate the process.

You live in Moscow, Idaho, where the weather in the winter stays between 0 °F and 50 °F (Fig. 28.2a). Suppose you had a thermometer that contained only two readings on it, hot and cold, and that you wanted to record the weather patterns and plot the results. The two quantization levels can be correlated with the actual temperature as follows:

If $0\ °F \leq T < 25\ °F$	Temperature is recorded as cold
If $25\ °F \leq T < 50\ °F$	Temperature is recorded as hot

You take a measurement every day at noon and plot the results after one week. From Fig. 28.2b, it is apparent that your discretized version of the weather is not an accurate representation of the actual weather.

Now suppose that you find another thermometer that contains four possible temperatures (hot, warm, cool, and cold) and that you increase the number of readings to two per day. The result of this reading is seen in Fig. 28.3a. The quantization levels represent four equal bands of temperature as seen below:

If $0\ °F \leq T < 12.5\ °F$	Temperature is recorded as cold

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If $12.5\ °F \leq T < 25\ °F$	Temperature is recorded as cool
If $25\ °F \leq T < 37.5\ °F$	Temperature is recorded as warm
If $37.5\ °F \leq T < 50\ °F$	Temperature is recorded as hot

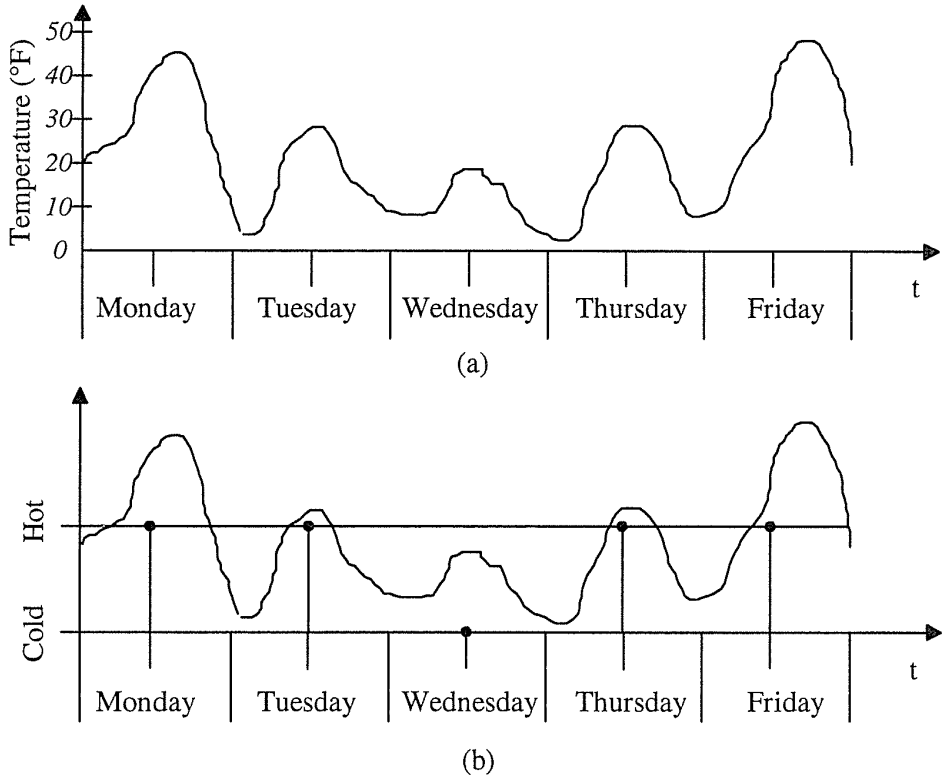


Figure 28.2 (a) An analog signal representing the temperature in Moscow, and (b) a digital representation of the analog signal taking one sample per day with two quantization levels.

Here, the digital version of the weather still looks nothing like the actual weather pattern, but the critical issues in digitizing an analog signal should be apparent. The actual weather pattern is the analog signal. It is continuous with respect to time, and its value can be between 0 °F and 50 °F (even 33.9638483920398439 °F!). The accuracy of the digitized signal is dependent on two things: the number of samples taken and the resolution, or number of quantization levels, of the converter. In our example, we need to increase both the number of samples and the resolution of thermometer.

Suppose that finally we obtain a thermometer with 25 temperature readings and that we now take a reading eight times per day. Each of the 25 quantization levels now represents a 2 °F band of temperature. From Fig. 28.3b, we can see that the digital version of the weather is approaching that of the actual analog signal. If we kept

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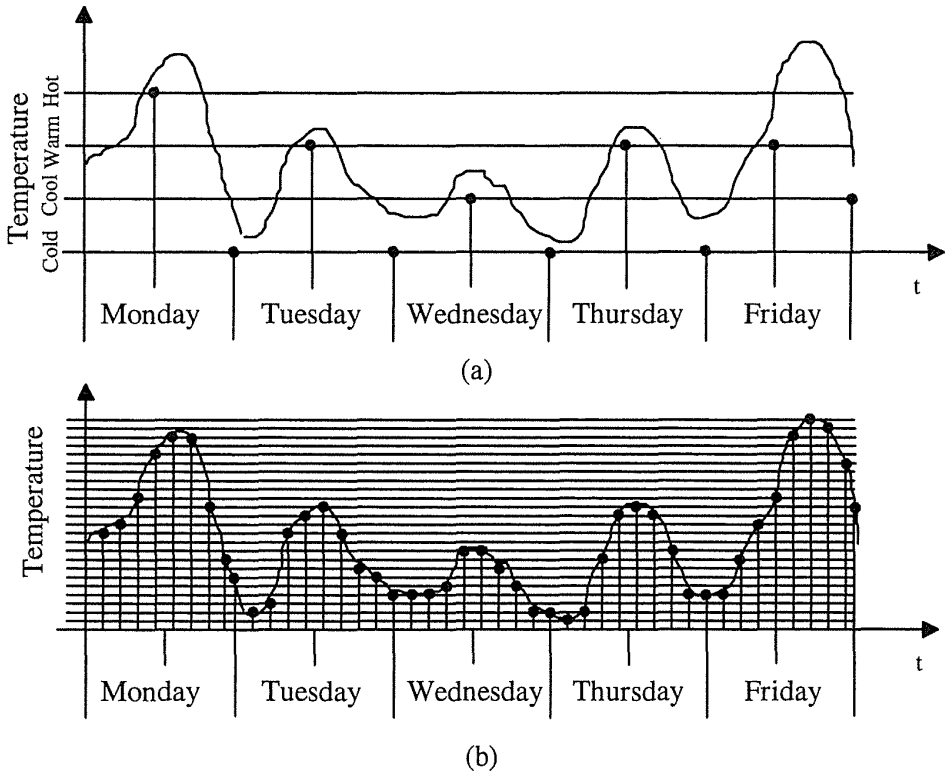


Figure 28.3 Digital representation of the temperature taking (a) two samples per day with four quantization levels and (b) nine samples per day with 25 quantization levels.

increasing both sampling time and resolution, the difference between the analog and the digital signals would become negligible. This brings up another critical issue. How many samples should one take in order to accurately represent the analog signal?

Suppose a sudden rainstorm swept through Moscow and caused a sharp decrease in temperature before returning to normal. If that storm had occurred between our sampling times, our experiment would not have shown the effects of the storm. Our sampling time was too slow to catch the change in the weather. If we had increased the number of samples, we would have recognized that something happened which caused the temperature to drop dramatically during that period.

As it turns out, the *Nyquist Criterion* defines how fast the sampling rate needs to be to represent an analog signal accurately. This criterion requires that the sampling rate be at least two times the highest frequency contained in the analog signal. In our example, we need to know how quickly the weather can change and then take samples twice as fast as that value. The Nyquist Criterion can be described as

$$F_{sampling} = 2\,F_{MAX} \tag{28.1}$$

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where $F_{sampling}$ is the sampling frequency required to accurately represent the analog signal and F_{MAX} is the highest frequency of the sampled signal.

How much resolution should we use to represent the analog signal accurately? There is no criterion for this specification. Each application will have its own requirements. In our weather example, if we were only interested in following general trends, then the 25 quantization levels would more than suffice. However, if we were interested in keeping an accurate record of the temperature to within ±0.5 °F, we would need to double the resolution to 50 quantization levels so that each quantization level would correspond to each degree ±0.5 °F (Fig. 28.4).

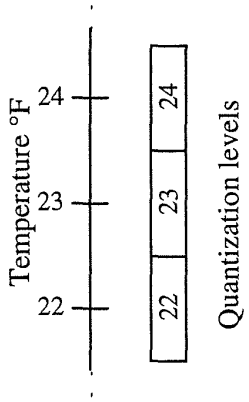


Figure 28.4 Quantization levels overlap actual temperature by ± ½ °F.

28.3 Sample-and-Hold (S/H) Characteristics

Sample-and-hold (S/H) circuits are critical in converting analog signals to digital signals. The behavior of the S/H is analogous to that of a camera. Its main function is to "take a picture" of the analog signal and hold its value until the ADC can process the information. It is important to characterize the S/H circuit when performing data conversion. Ignoring this component can result in serious error, for both speed and accuracy can be limited by the S/H. Ideally, the S/H circuit should have an output similar to that shown in Fig. 28.5a. Here, the analog signal is instantly captured and held until the next sampling period. However, a finite amount of time is required for the sampling to occur. During the sampling period, the analog signal may continue to vary; thus, another type of circuit is called a track-and-hold, or T/H. Here, the analog signal is "tracked" during the time required to sample the signal, as seen in Fig. 28.5b. It can be seen that S/H circuits operate in both static (hold mode) and dynamic (sample mode) circumstances. Thus, characterization of the S/H will be discussed in the context of these two categories. Figure 28.6 presents a summary of the major errors associated with a S/H [1-5]. A discussion of each error follows.

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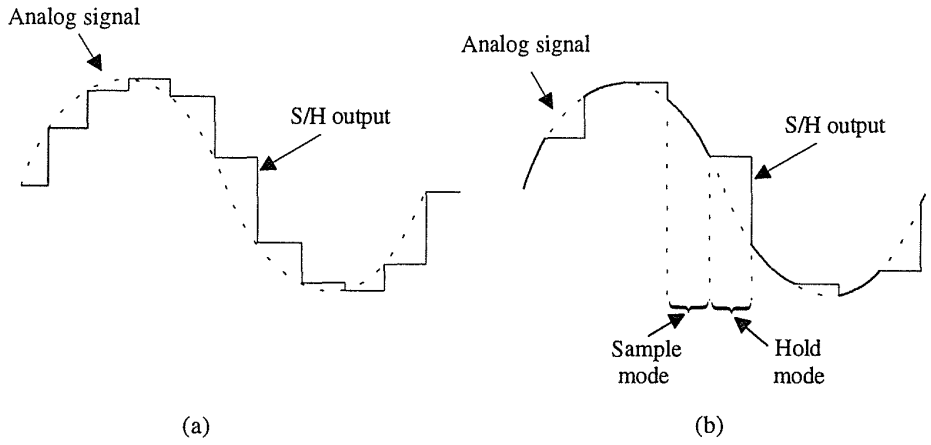


Figure 28.5 The output of (a) an ideal S/H circuit and (b) a track-and-hold (T/H).

Sample Mode

Once the sampling command has been issued, the time required for the S/H to track the analog signal to within a specified tolerance is known as *acquisition time*. In the worst-case scenario, the analog signal would vary from zero volts to its maximum value, $v_{IN(max)}$. And the worst-case acquisition time would correspond to the time required for the output to transition from zero to $v_{IN(max)}$. Since most S/H circuits use amplifiers as buffers (as seen in Fig. 28.7), it should be obvious that the acquisition will be a function of the amplifier's own specifications. For example, notice that if the input changes very quickly, then the output of the T/H could be limited by the amplifier's slew rate. The amplifier's stability is also extremely critical. If the amplifier is not compensated correctly, and the phase margin is too small, then a large *overshoot* will occur which requires a longer *settling time* for the S/H to settle within the specified tolerance. The error tolerance at the output of the S/H is also dependent on the amplifier's *offset*, *gain*

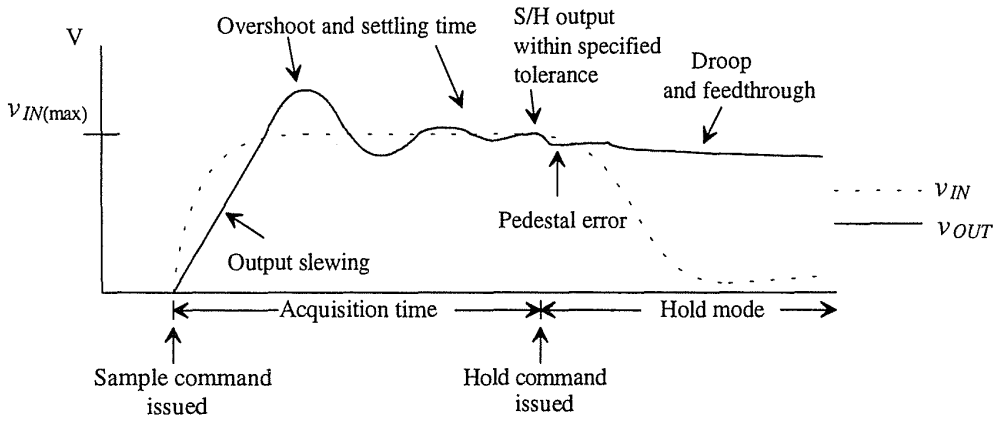


Figure 28.6 Illustration of typical errors associated wth a S/H.

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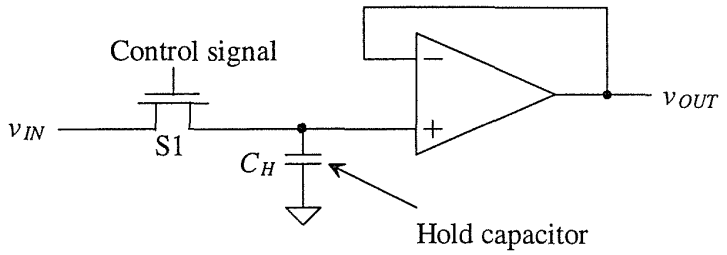


Figure 28.7 Track-and-hold circuit using an output buffer.

error (ideally, the S/H should have a gain of 1) and *linearity* (the gain of the S/H should not vary over the input voltage range).

Hold Mode

Once the hold command is issued, the S/H faces other errors. Pedestal error occurs as a result of charge injection (introduced in Sec. 27.1) and clock feedthrough. Part of the charge built up in the channel of the switch is distributed onto the capacitor, thus slightly changing its voltage. Also, the clock couples onto the capacitor via overlap capacitance between the gate and the source or drain. Another error that occurs during the hold mode is called *droop*. This error is related to the leakage of current from the capacitor due to parasitic impedances and to the leakage through the reverse-biased diode formed by the drain of the switch. This diode leakage can be minimized by making the drain area as small as can be tolerated. Although the input impedance of the buffer amplifier is very large, the switch has a finite OFF impedance through which leakage can occur. Current can also leak through the substrate. The key to minimizing droop is to increase the value of the sampling capacitor. The tradeoff, however, will be the increased time required to charge the capacitor to the value of the input signal.

Aperture Error

A transient effect that introduces error occurs between the sample and the hold modes. A finite amount of time, referred to as aperture time, is required to disconnect the capacitor from the analog input source. The aperture time actually varies slightly as a result of noise on the hold control signal and the value of the input signal, since the switch will not turn off until the gate voltage becomes less than the value of the input voltage less one threshold voltage drop. This effect is called *aperture uncertainty* or *aperture jitter*. As a result, if a periodic signal was being sampled repeatedly at the same points, slight variations in the hold value would result, thus creating *sampling error*. Figure 28.8 illustrates this effect. Note that the amount of aperture error is directly related to the frequency of the signal and that the worst-case aperture error occurs at the zero crossing, where *dV/dt* is the greatest. This assumes that the S/H circuit is capable of sampling both positive and negative voltages (bipolar). The amount

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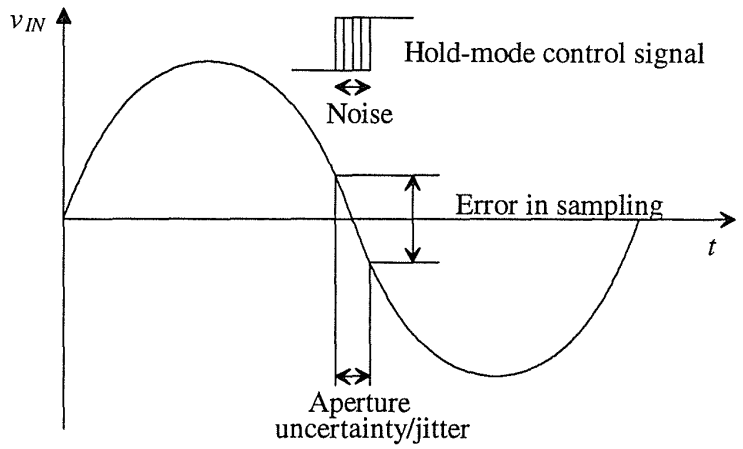


Figure 28.8 Aperture error.

of error that can be tolerated is directly related to the resolution of the conversion. Aperture error will be discussed again in Sec. 28.5 as it relates to the error in an ADC.

Example 28.1

Find the maximum sampling error for a S/H circuit that is sampling a sinusoidal input signal that could be described as

$$v_{IN} = A \sin 2\pi ft$$

where A is 2 V and f = 100 kHz. Assume that the aperture uncertainty is equal to 0.5 ns.

The sampling error due to the aperture uncertainty can be thought of as a slew rate such that

$$\frac{dV}{dt} = \frac{d}{dt} A \sin 2\pi ft = 2\pi fA \cos 2\pi ft$$

with maximum slewing occurring when the cosine term is equal to 1. Therefore,

$$\frac{dV}{dt}(max) = 2\pi fA = (2\pi \cdot 100 \text{ kHz})(2 \text{ V})$$

and the maximum sampling error is

$$Maximum\ Sampling\ Error = dV(max) \quad \text{or}$$

$$(0.5 \times 10^{9} \text{ s})(2\pi \cdot 100 \text{ kHz})(2 \text{ V}) = 0.628 \text{ mV} \ \blacksquare$$

28.4 Digital-to-Analog Converter (DAC) Specifications

Probably the most popular digital-to-analog converter application is the digital audio compact disc player. Here digital information stored on the CD is converted into music

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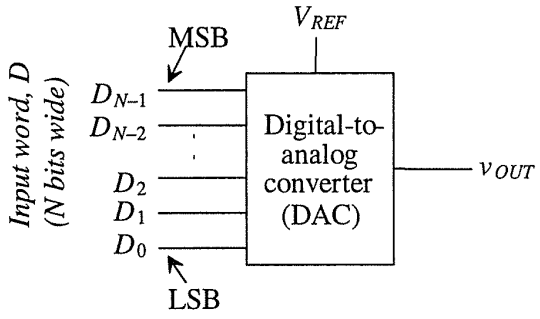


Figure 28.9 Block diagram of the digital-to-analog converter.

via a high-precision DAC. Many characteristics define a DAC's performance. Each characteristic will be discussed before we look at the basic architectures in Ch. 29. This "top-down" approach will allow a smoother transition from the data converter characteristics to the actual architectures, since most data converters have similar performance limitations. A discussion of some of the basic definitions associated with DACs follows. It should be noted that DACs and ADCs can use either voltage or current as its analog signal. For purposes of describing specifications, it will be assumed that the analog signal is a voltage.

A block diagram of a DAC can be seen in Fig. 28.9. Here an N-bit digital word is mapped into a single analog voltage. Typically, the output of the DAC is a voltage that is some fraction of a reference voltage (or current), such that

$$v_{OUT} = FV_{REF} \tag{28.2}$$

where v_{OUT} is the analog voltage output, V_{REF} is the reference voltage, and F is the fraction defined by the input word, D, that is N bits wide. The number of input combinations represented by the input word D is related to the number of bits in the word by

$$\text{Number of input combinations} = 2^N \tag{28.3}$$

A 4-bit DAC has a total of 2^4 or 16 total input values. A converter with 4-bit resolution must be able to map a change in the analog output which is equal to 1 part in 16. The maximum analog output voltage for any DAC is limited by the value of some reference voltage, V_{REF}. If the input is an N-bit word, then the value of the fraction, F, can be determined by,

$$F = \frac{D}{2^N} \tag{28.4}$$

Therefore, if a 3-bit DAC is being used, the input, D, is $100 = 4_{10}$, and V_{REF} is 5 V, then the value of F is

$$F = \frac{100}{2^3} = \frac{4}{8} \tag{28.5}$$

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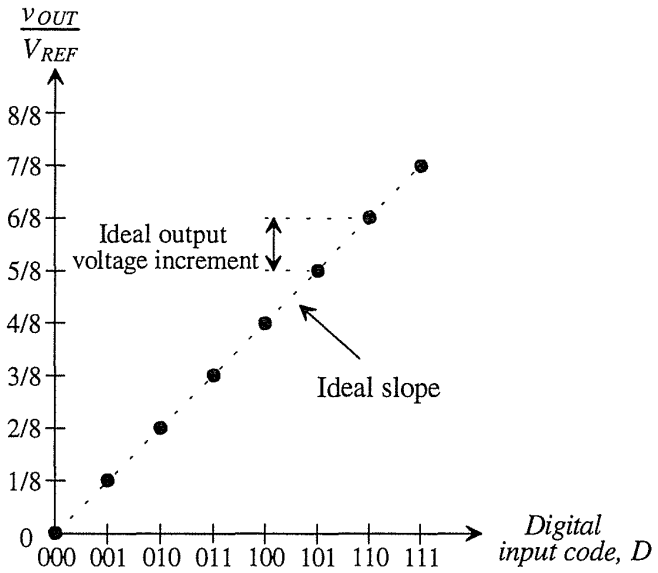


Figure 28.10 Ideal transfer curve for a 3-bit DAC.

and the analog voltage that appears at the output becomes,

$$v_{OUT} = \frac{4}{8}(5) = 2.5 \text{ V} \tag{28.6}$$

By plotting the input word, D, versus v_{OUT} as D is incremented from 000 to 111, the *transfer curve* seen in Fig. 28.10 would be generated. The y-axis has been normalized to V_{REF}; therefore, the graduated marks also represent F by Eq. (28.2). Some important characteristics need to be discussed here. First, notice that the transfer curve is not continuous. Since the input is a digital signal, which is inherently discrete, the input signal can have only eight values that must correspondingly produce eight output voltages. If a straight line connected each of the output values, the slope of the line would ideally be one increment/input code value. Also note that the maximum value of the output is 7/8. Since the case where D = 000 has to result in an analog voltage of 0 V, and a 3-bit DAC has eight possible analog output voltages, then the analog output will increase from 0 V to only 7/8 V_{REF}.

Again, using Eq. (28.2), this means that the maximum analog output that can be generated by the 3-bit DAC is

$$v_{OUT(\max)} = \frac{7}{8} \cdot V_{REF} \tag{28.7}$$

This maximum analog output voltage that can be generated is known as *full-scale voltage*, V_{FS}, and can be generalized to any N-bit DAC as

$$V_{FS} = \frac{2^N - 1}{2^N} \cdot V_{REF} \tag{28.8}$$

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The *least significant bit* (*LSB*) refers to the rightmost bit in the digital input word. The LSB defines the smallest possible change in the analog output voltage. The LSB will always be denoted as D_0. One LSB can be defined as

$$1\ LSB = \frac{V_{REF}}{2^N} \tag{28.9}$$

In the previous case of the 3-bit DAC, 1 LSB = 5/8 V, or 0.625 V. Generating an output in multiples of 0.625 V may not seem difficult, but as the number of bits increases, the voltage value of one LSB decreases.

The *most significant bit* (*MSB*) refers to the leftmost bit of the digital word, *D*. In the previous example, $D = 100$ or $D_2D_1D_0$, with D_2 being the MSB. Generalizing to the *N*-bit DAC, the MSB would be denoted as D_{N-1}. (Since the LSB is denoted as bit 0, the MSB is denoted as *N*-1.) Note that when discussing DACs, the MSB causes the output to change by 1/2 V_{REF}.

When discussing data converters, the term *resolution* describes the smallest change in the analog output with respect to the value of the reference voltage, V_{REF}. This is slightly different from the definition of LSB in that resolution is typically given in terms of bits.

Example 28.2

Find the resolution for a DAC if the output voltage is desired to change in 1 mV increments while using a reference voltage of 5 V.

The DAC must resolve

$$\frac{1\text{ mV}}{5\text{ V}} = 0.0002 \text{ or } 0.02\% \text{ adjustability}$$

Therefore, the *accuracy* required will be

$$\frac{1}{2^N} = 0.0002 \tag{28.10}$$

and solving *N* for the resolution yields

$$N = \text{Log}_2\left(\frac{5\text{ V}}{1\text{ mV}}\right) = 12.29 \text{ bits}$$

which means that a 13-bit DAC will be needed to produce the accuracy capable of generating 1 mV changes in the output using a 5 V reference. ■

Example 28.3

Find the number of input combinations, values for 1 LSB, the percentage accuracy, and the full-scale voltage generated for a 3-bit, 8-bit, and 16-bit DAC, assuming that $V_{REF} = 5$ V.

Using Eqs. (28.3), (28.8), (28.9), and (28.10), we can generate the following information:

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Resolution	Input combinations	1 LSB	% accuracy	V_{FS}
3	8	0.625 V	12.5	4.375 V
8	256	19.5 mV	0.391	4.985 V
16	65,536	76.29 μV	0.00153	4.9999 V

The value of 1 LSB for an 8-bit converter is 18.5 mV, while 1 LSB for a 16-bit converter is 76.3 μV (a factor of 256)! Increasing the resolution by 1 bit increases the accuracy by a factor of 2. The precision required to map the analog signal at high resolutions is very difficult to achieve. We will examine some of these issues as we examine the limitations of the data converter in Ch. 29.

Notice that the value of $v_{OUT(\max)}$ approaches that of V_{REF} as N increases, but according to Eq. (28.8), $v_{OUT(max)}$ will never equal V_{REF}. However, at high resolutions, $v_{OUT(max)}$ would probably be close enough to V_{REF} to suit any application. ■

Differential Nonlinearity

As seen in the ideal DAC in Fig. 28.10, each adjacent output increment should be exactly one-eighth. Since the y-axis is normalized, the values for the increment heights will be unitless. However, the increment heights can be easily converted to volts by multiplying the height by V_{REF}. This corresponds to the ideal increment corresponding to 0.625 V = 1 LSB (assuming V_{REF} = 5 V).

Nonideal components cause the analog increments to differ from their ideal values. The difference between the ideal and nonideal values is known as *differential nonlinearity*, or *DNL* and is defined as

DNL_n = Actual increment height of transition n – Ideal increment height (28.11)

where n is the number corresponding to the digital input transition. The DNL specification measures how well a DAC can generate uniform analog LSB multiples at its output.

Example 28.4

Determine the DNL for the 3-bit nonideal DAC whose transfer curve is shown in Fig. 28.11. Assume that V_{REF} = 5 V.

The actual increment heights are labeled with respect to the ideal increment height, which is 1 LSB, or 1/8 of $\frac{v_{OUT}}{V_{REF}}$. Notice that there is no increment corresponding to 000, since it is desirable to have zero output voltage with a digital input code of 000. The increment height corresponding to 001, however, is equal to the corresponding height of the ideal case seen in Fig. 28.10; therefore, $DNL_1 = 0$. Similarly, DNL_2 is also zero since the increment associated with the transition at 010 is equal to the ideal height. Notice that the 011

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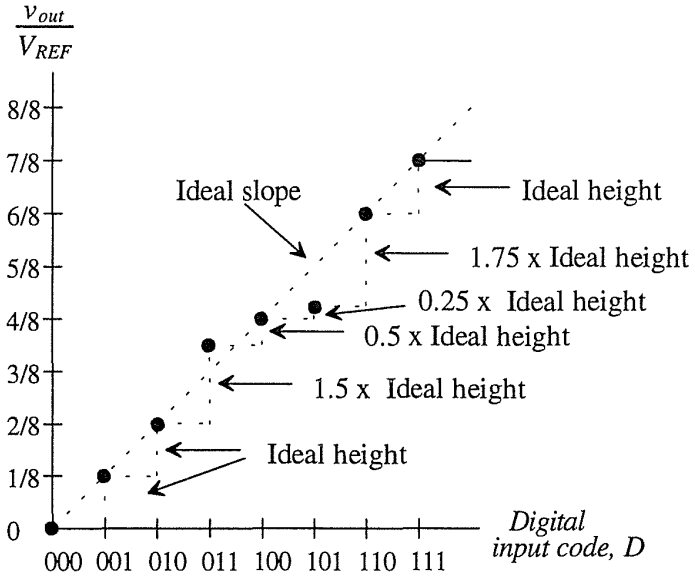


Figure 28.11 Example of differential nonlinearity for a 3-bit DAC.

increment, however, is not equal to the ideal curve but is 3/16, or 1.5 times the ideal height.

$$DNL_3 = 1.5 \text{ LSB} - 1 \text{ LSB} = 0.5 \text{ LSB}$$

Since we have already determined in Eq. (28.9) that for a 3-bit DAC, 1 LSB = 0.625 V, we can convert the DNL_3 to volts as well. Therefore, DNL_3 = 0.5 LSB = 0.3125 V. However, it is popular to refer to DNL in terms of LSBs. The remainder of the digital output codes can be characterized as follows:

$$DNL_4 = 0.5 \text{ LSB} - 1 \text{ LSB} = -0.5 \text{ LSB}$$

$$DNL_5 = 0.25 \text{ LSB} - 1 \text{ LSB} = -0.75 \text{ LSB}$$

$$DNL_6 = 1.75 \text{ LSB} - 1 \text{ LSB} = 0.75 \text{ LSB}$$

$$DNL_7 = 1 \text{ LSB} - 1 \text{ LSB} = 0$$

If we were to plot the value of DNL (in LSBs) versus the input digital code, Fig. 28.12 would result. The DNL for the entire converter used in this illustration is ±0.75 LSB since the overall error of the DAC is defined by its worst-case DNL. ■

Generally, a DAC will have less than ±½ LSB of DNL if it is to be *N*-bit accurate. A 5-bit DAC with 0.75 LSBs of DNL actually has the resolution of a 4-bit DAC. If the DNL for a DAC is less than – 1 LSBs, then the DAC is said to be *nonmonotonic*, which means that the analog output voltage does not always increase as the digital input code is incremented. A DAC should always exhibit *monotonicity* if it is to function without error.

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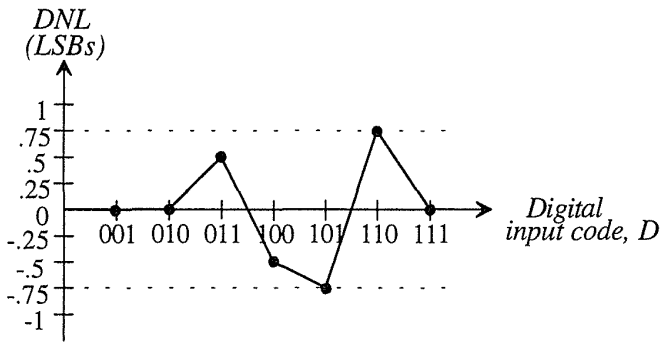


Figure 28.12 DNL curve for the nonideal 3-bit DAC.

Integral Nonlinearity

Another important static characteristic of DACs is called *integral nonlinearity* (*INL*). Defined as the difference between the data converter output values and a reference straight line drawn through the first and last output values, INL defines the linearity of the overall transfer curve and can be described as

INL_n = Output value for input code n – Output value of the reference line at that point

(28.12)

An illustration of this measurement is presented in Fig. 28.13. It is assumed that all other errors due to offset and gain (these will be discussed shortly) are zero. An example follows shortly.

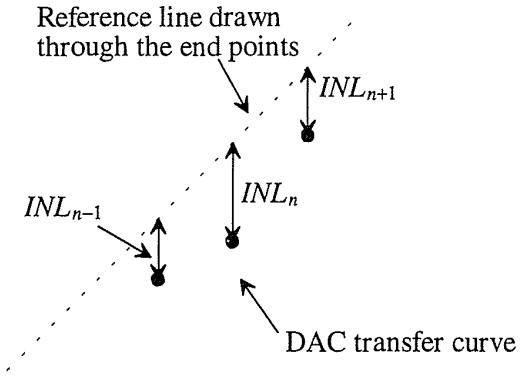


Figure 28.13 Measuring the INL for a DAC transfer curve.

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It is common practice to assume that a converter with N-bit resolution will have less than ±½ LSB of DNL and INL. The term, *½ LSB*, is a common term that typically denotes the maximum error of a data converter (both DACs and ADCs). For example, a 13-bit DAC having greater than ±½ LSB of DNL or INL actually has the resolution of a 12-bit DAC. The value of ½ LSB in volts is simply

$$0.5\ LSB = \frac{V_{REF}}{2^{N+1}} \tag{28.13}$$

Example 28.5

Determine the INL for the nonideal 3-bit DAC shown in Fig. 28.14. Assume that $V_{REF} = 5$ V.

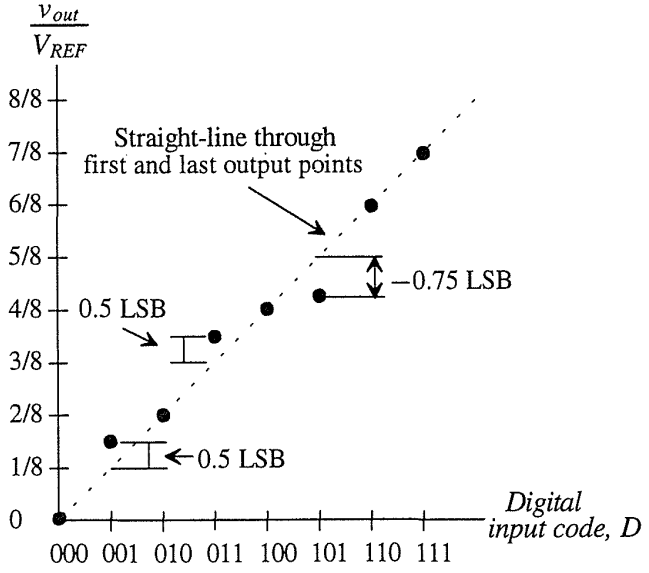


Figure 28.14 Example of integral nonlinearity for a DAC.

First, a reference line is drawn through the first and last output values. The INL is zero for every code in which the output value lies on the reference line; therefore, $INL_2 = INL_4 = INL_6 = INL_7 = 0$. Only outputs corresponding to 001, 011, and 101 do not lie on the reference. Both the 001 and the 011 transitions occur ½ LSB higher than the straight-line values; therefore, $INL_1 = INL_3 = 0.5$ LSB. By the same reasoning, $INL_5 = -0.75$ LSB. Therefore, the INL for the DAC is considered to be its worst-case INL of +0.5 LSB and – 0.75 LSB. The INL plot for the nonideal 3-bit DAC can be seen in Fig. 28.15. ■

It should be noted that other methods are used to determine INL. One method compares the output values to the ideal reference line, regardless of the positions of the first and last output values. If the DAC has an offset voltage or gain error, this will be

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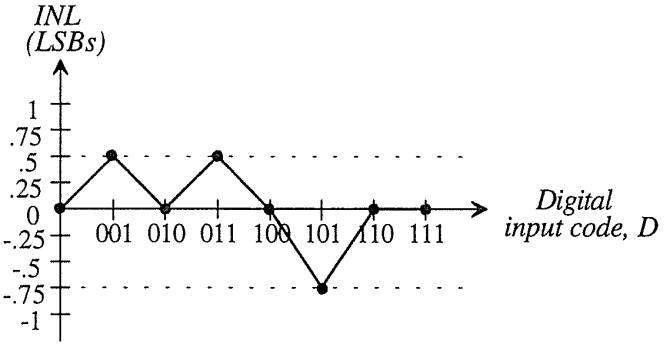


Figure 28.15 INL curve for the nonideal 3-bit DAC.

included in the INL determination. Usually, the offset and gain errors are determined as separate specifications.

Another method, described as the "best-fit" method, attempts to minimize the INL by constructing the reference line so that it passes as closely as possible to a majority of the output values. Although this method does minimize the INL error, it is a rather subjective method that is not as widely used as drawing the reference line through the first and last output values.

Offset

The analog output should be 0 V for $D = 0$. However, an offset exists if the analog output voltage is not equal to zero. This can be seen as a shift in the transfer curve as illustrated in Fig. 28.16. This specification is similar to the offset voltage for an operational amplifier except that it is not referred to the input.

Gain Error

A gain error exists if the slope of the best-fit line through the transfer curve is different from the slope of the best-fit line for the ideal case. For the DAC illustrated in Fig. 28.17, the gain error becomes

$$\text{Gain error} = \text{Ideal slope} - \text{Actual slope} \tag{28.14}$$

Latency

This specification defines the total time from the moment that the input digital word changes to the time the analog output value has settled to within a specified tolerance. Latency should not be confused with settling time, since latency includes the delay required to map the digital word to an analog value plus the settling time. It should be noted that settling time considerations are just as important for a DAC as they are for a S/H or an operational amplifier.

Signal-to-Noise Ratio (SNR)

Signal-to-noise (SNR) is defined as the ratio of the signal power to the noise at the analog output. In amplifier applications, this specification is typically measured using a

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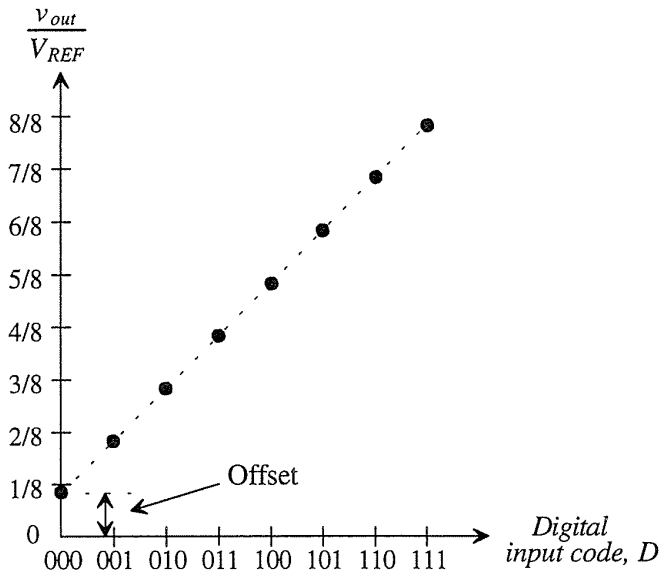


Figure 28.16 Illustration of offset error for a 3-bit DAC.

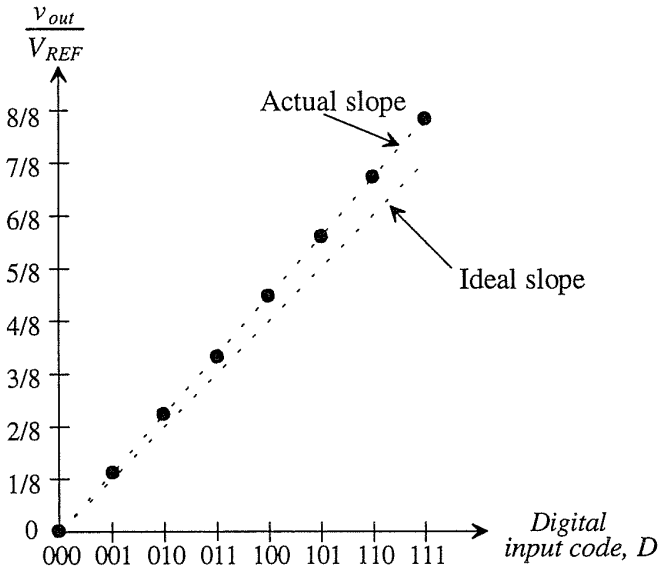


Figure 28.17 Illustration of gain error for a 3-bit DAC.

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sinewave input. For the DAC, a "digital" sinewave is generated through instrumentation or through an A/D. The SNR can reveal the true resolution of a data converter as the effective number of bits can be quantified mathematically. A detailed derivation of the SNR is presented in Sec. 28.6, on the discussion of ADC specifications.

Dynamic Range

Dynamic range is defined as the ratio of the largest output signal over the smallest output signal. For both DACs and ADCs, the dynamic range is related to the resolution of the converter. For example, an N-bit DAC can produce a maximum output of 2^N–1 multiples of LSBs and a minimum value of 1 LSB. Therefore, the dynamic range in decibels is simply

$$DR = 20\text{Log}\left(\frac{2^N - 1}{1}\right) \text{ dB} \tag{28.15}$$

A 16-bit data converter has a dynamic range of 96.33 dB.

28.5 Analog-to-Digital Converter (ADC) Specifications

Many of the specifications that describe the ADC are similar to those that describe the DAC. However, there are subtle differences. Since the DAC is converting a discrete signal into an analog representation that is also limited by the resolution of the converter, a fixed number of inputs and outputs are generated. However, with the ADC, the input is an analog signal with an infinite number of values, which then has to be quantized into an N-bit digital word (Fig. 28.18). This process is much more difficult than the digital-to-analog process. In fact, many ADC architectures use a DAC as a critical component.

For example, in the previous discussion of DACs, it was determined that for a 16-bit DAC, the converter would need to generate output voltages in multiples of 78 μV. However, for the ADC, the converter needs to resolve differences in the analog signal of 78 μV. This means that the ADC must be able to detect changes in the input

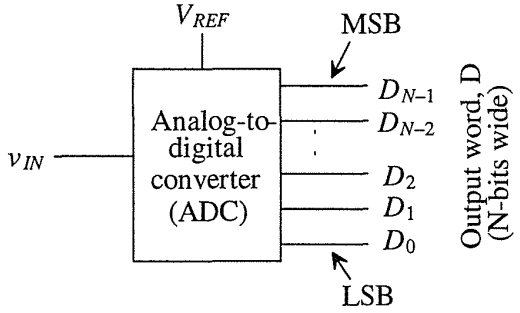


Figure 28.18 Block diagram of the digital-to-analog converter.

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signal on the order of 1 part in 65,536! In contrast, the DAC had a finite number of input combinations (2^N). The ADC, however, has to "quantize" the infinite-valued analog signal into many segments so that

$$\text{Number of quantization levels} = 2^N \tag{28.16}$$

This distinction is subtle but must be recognized to understand the differences between the two types of conversion.

Examine Fig. 28.19a. The digital output, D, of an ideal, 3-bit ADC is plotted versus the analog input, v_{IN}. Note the difference in the transfer curve for the ADC versus the DAC (Fig. 28.10). The y-axis is now the digital output, and the x-axis has been normalized to V_{REF}. Since the input signal is a continuous signal and the output is discrete, the transfer curve of the ADC resembles that of a staircase. Another fact to observe is that the 2^N quantization levels correspond to the digital output codes 0 to 7. Thus, the maximum output of the ADC will be 111 (2^N-1), corresponding to the value for which $\frac{v_{IN}}{V_{REF}} \geq \frac{7}{8}$. Figure 28.19b corresponds to the error caused by the quantization.

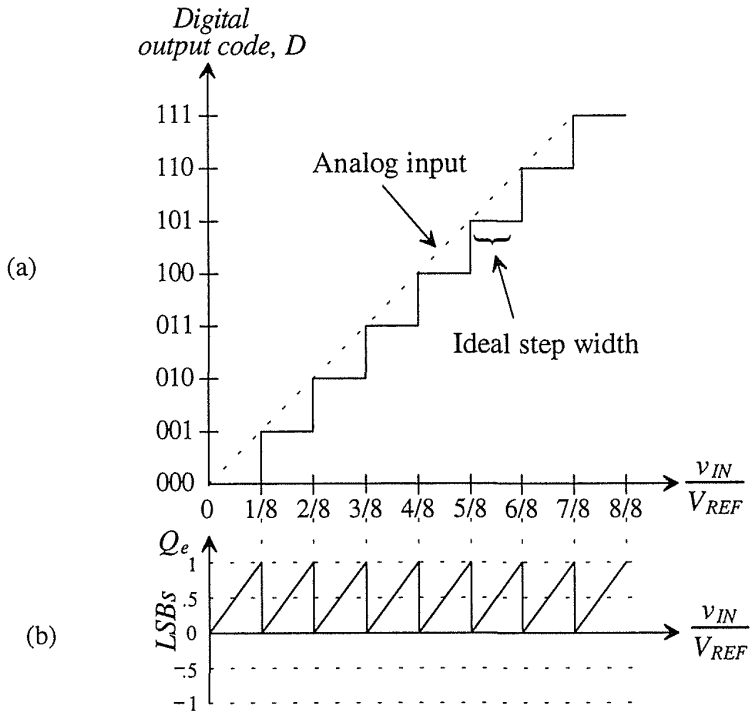


Figure 28.19 (a) Transfer curve for an ideal ADC and (b) its corresponding quantization error.

The value of 1 LSB for this ADC can be calculated using Eq. (28.9) and is the ideal step width (1/8) in Fig. 28.19 (versus the height for the DAC) multiplied by V_{REF}. Therefore, assuming that V_{REF} = 5V,

$$1 \text{ LSB} = 0.625 \text{ V} \tag{28.17}$$

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Quantization Error

Since the analog input is an infinite valued quantity and the output is a discrete value, an error will be produced as a result of the quantization. This error, known as *quantization error*, Q_e, is defined as the difference between the actual analog input and the value of the output (staircase) given in voltage. It is calculated as

$$Q_e = v_{IN} - V_{staircase} \tag{28.18}$$

where the value of the staircase output, $V_{staircase}$, can be calculated by

$$V_{staircase} = D \cdot \frac{V_{REF}}{2^N} = D \cdot V_{LSB} \tag{28.19}$$

where D is the value of the digital output code and V_{LSB} is the value of 1 LSB in volts, in this case 0.625 V. We can also easily convert the value of Q_e in units of LSBs. In Fig. 28.19a, Q_e can be generated by subtracting the value of the staircase from the dashed line. The result can be seen in Fig. 28.19b. A sawtooth waveform is formed centered about ½ LSBs. Ideally, the magnitude of Q_e will be no greater than one LSB and no less than 0. It would be advantageous if the quantization error were centered about zero so that the error would be at most ±½ LSBs (as opposed to +1LSB). This is easily achieved as seen in Fig. 28.20a and b. Here, the entire transfer curve is shifted to the left by ½ LSB, thus making the codes centered around the LSB increments on the x-axis. This drawing illustrates that at best, an ideal ADC will have quantization error of ±½ LSB.

In shifting this curve to the left, notice that the first code transition occurs when $\frac{v_{IN}}{V_{REF}} \geq \frac{1}{16}$. Therefore, the range of $\frac{v_{IN}}{V_{REF}}$ for the digital output corresponding to 000 is half as wide as the ideal step width. The last code transition occurs when $\frac{v_{IN}}{V_{REF}} \geq \frac{13}{16}$ (between 6/8 and 7/8). Note that the step width corresponding to this last code transition is 1.5 times larger than the ideal width and that the quantization error extends up to 1 LSB when $\frac{v_{IN}}{V_{REF}} = 1$. However, the converter would be considered to be out of range once $\frac{v_{IN}}{V_{REF}} \geq \frac{15}{16}$ (halfway between 7/8 and 8/8), so the problem is moot.

Differential Nonlinearity

Differential nonlinearity for an ADC is similar to that defined for a DAC. However, for the ADC, DNL is the difference between the actual code *width* of a nonideal converter and the ideal case. Figure 28.21 illustrates the transfer curve for a nonideal 3-bit ADC. The values for the DNL can be solved as follows:

$$\text{DNL} = \text{Actual step width} - \text{Ideal step width} \tag{28.20}$$

Since the step widths can be converted to either volts for LSBs, DNL can be defined using either units. The value of the ideal step is 1/8. Converting to volts, this becomes

$$V_{idealstepwidth} = \frac{1}{8} \cdot V_{REF} = 0.625\ V = 1\ \text{LSB} \tag{28.21}$$

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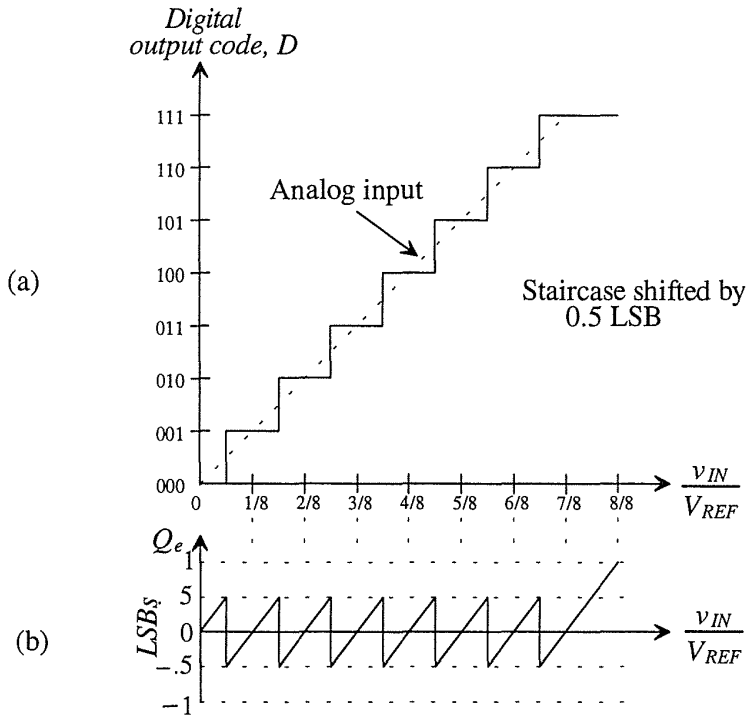


Figure 28.20 (a) Transfer curve for an ideal 3-bit ADC with (b) quantization error centered about zero.

Example 28.6

Using Fig. 28.21a, calculate the differential nonlinearity of the 3-bit ADC. Assume that $V_{REF} = 5$ V. Draw the quantization error, Q_e, in units of LSBs.

The DNL of the converter can be calculated by examining the step width of each digital output code. Since the ideal step width of the 000 transition is ½ LSB, then $DNL_0 = 0$. Also note that the step widths associated with 001 and 011 are equal to 1 LSB; therefore, both DNL_1 and DNL_4 are zero. However, the remaining values code widths are not equal to the ideal value but can be calculated as

$$DNL_2 = 1.5 \text{ LSB} - 1 \text{ LSB} = 0.5 \text{ LSB}$$

$$DNL_3 = 0.5 \text{ LSB} - 1 \text{ LSB} = -0.5 \text{ LSB}$$

$$DNL_5 = -0.5 \text{ LSB}$$

$$DNL_6 = 0.5 \text{ LSB}$$

$DNL_7 = 0$ LSB (since the ideal step width is 1.5 LSB wide at this code transition)

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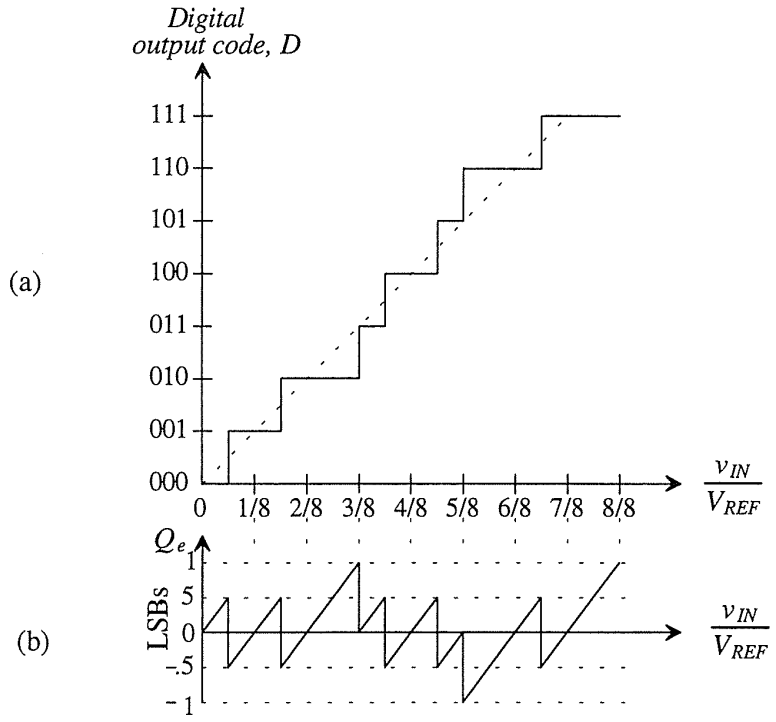


Figure 28.21 (a) Transfer curve for a nonideal 3-bit ADC used in Ex. 28.4 with (b) quantization error illustrating differential nonlinearity.

The overall DNL for the converter used in this illustration is ±0.5 LSB. Note that the quantization error illustrated in Fig. 28.21b is directly related to the DNL. As DNL increases in either direction, the quantization error worsens. Each "tooth" in the quantization error waveform should ideally be the same size. ■

Missing Codes

It is of interest to note the consequences of having a DNL that is equal to –1 LSB. Figure 28.22 illustrates an ADC for which this is true. The total width of the step corresponding to 101 is completely missing; thus, the value of DNL_5 is –1 LSB. Any ADC possessing a DNL that is equal to –1 LSB is guaranteed to have a missing code. Notice that the step width corresponding to 010 is 2 LSBs and that the value for DNL_2 is +1 LSB. However, there is not a missing code corresponding to 011, since the step width of code 011 is dependent on the 100 transition. Therefore, an ADC having a DNL greater than +1 LSB is not guaranteed to have a missing code, though in all probability a missing code will occur.

Integral Nonlinearity

Integral nonlinearity (INL) is defined similarly to that for a DAC. Again, a "best-fit" straight line is drawn through the end points of the first and last code transition, with

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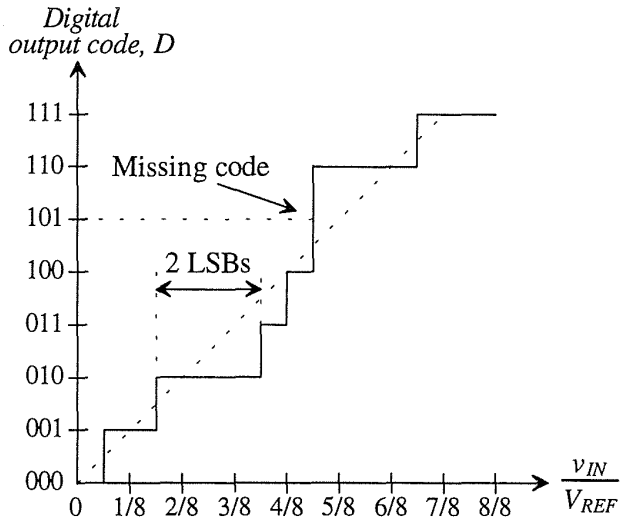


Figure 28.22 Transfer curve for a nonideal 3-bit ADC with a missing code.

INL being defined as the difference between the data converter code transition points and the straight line with all other errors set to zero.

Example 28.7

Determine the INL for the ADC whose transfer curve is illustrated in Fig. 28.23a. Assume that V_{REF} = 5 V. Draw the quantization error, Q_e, in units of LSBs.

By inspection, it can be seen that all of the transition points occur on the best-fit line except for the transitions associated with code 011 and 110. Therefore,

$$INL_0 = INL_1 = INL_2 = INL_4 = INL_5 = INL_7 = 0$$

The INL corresponding to the remaining codes can be calculated as

$$INL_3 = 3/8 - 5/16 = 1/16 \text{ or } 0.5 \text{ LSB}$$

Similarly, INL_6 can be calculated in the same manner and is found to be – 0.5 LSB. Thus, the overall INL for the converter is the maximum value of INL corresponding to ±0.5 LSB.

The INL can also be determined by inspecting the quantization error in Fig. 28.23b. Here, the INL will be the magnitude of the quantization error which lies outside the ±½ LSB band of Q_e. It can be seen that Q_e = 1 LSB, corresponding to the point at which INL = 0.5 LSB for digital output code 011, and that Q_e = –1 LSB at the output code corresponding to INL = – 0.5 LSB for digital output code 110. ■

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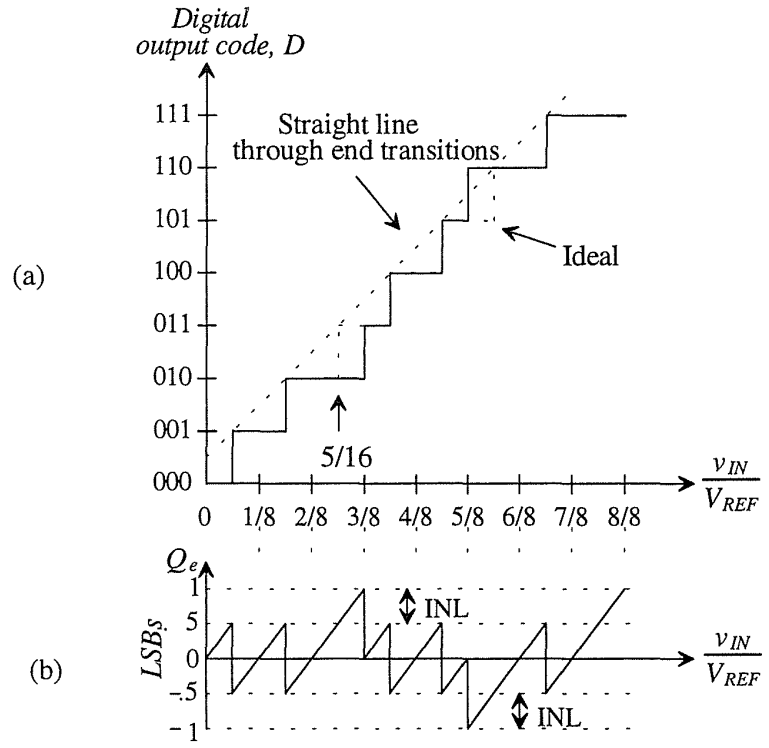


Figure 28.23 (a) Transfer curve of a nonideal 3-bit ADC and (b) its quantization error illustrating INL.

Offset and Gain Error

Offset and gain error are identical to the DAC case. *Offset error* occurs when there is a difference between the value of the first code transition and the ideal value of ½ LSBs. As seen in Fig. 28.24a, the offset error is a constant value. Note that the quantization error becomes ideal after the initial offset voltage is overcome. *Gain error* or *scale factor error*, seen in Fig. 28.24b, is the difference in the slope of a straight line drawn through the transfer characteristic and the slope of 1 of an ideal ADC. Causes of offset and gain error are discussed in Ch. 29, but it is important here to understand their overall effects on ADC transfer curves.

So far, we have examined only the DC characteristics of an ADC. However, examining the dynamic aspects of the converter will lead to a whole new set of errors. Sampling is inherently a dynamic process since the accuracy of the sample is dependent on the speed of the analog signal. Many effects that occur during sampling limit the overall performance of the converter.

Aliasing

As mentioned earlier in the chapter, the Nyquist Criterion requires that a signal be sampled at least two times the highest frequency contained in the signal. What would

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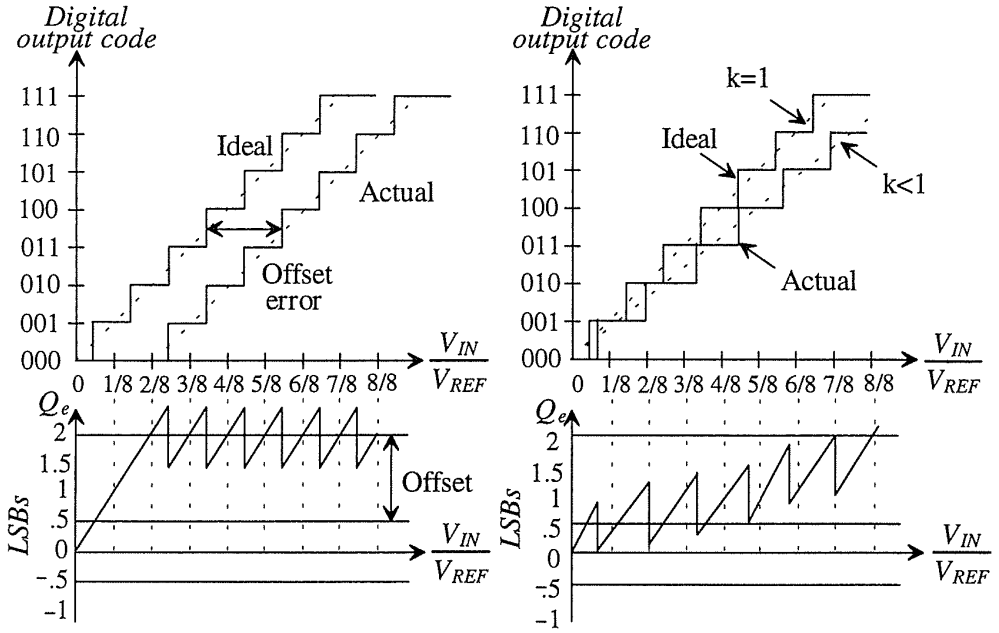


Figure 28.24 Transfer curve illustrating (a) offset error and (b) gain error.

happen if this criterion were ignored and the sampling rate was actually less than that amount? A phenomenon known as aliasing would occur.

Examine Fig. 28.25. Here, an analog signal is being sampled at a rate slower than the Nyquist Criterion requires. As a result, it appears that a totally different signal of lower frequency (the dashed line) is being sampled. The lower frequency signal is an "alias" of the original signal, and its frequency can be calculated as

$$f_{alias} = f_{actual} - f_{sample} \tag{28.22}$$

where f_{actual} is the frequency of the analog signal, f_{sample} is the sampling frequency, and f_{alias} is the frequency of the alias signal.

Aliasing can be eliminated either by sampling at higher frequencies or by filtering the analog signal before sampling and removing any frequencies that are greater than one-half the sampling frequency. It is good practice to filter the analog signal before sampling to eliminate any unknown higher order harmonics or noise that could result in aliasing.

A frequency domain analysis may further illustrate the concepts of aliasing. Figure 28.26 shows the analog signal, the *sampling function* (represented by a unit impulse train) and the resulting sampled signal in both the time and frequency domains. The analog signal in Fig. 28.26a is represented as a simple band-limited signal with center frequency, f_o. This simply means that the signal is contained within the frequency range shown. In Fig. 28.26b, the sampling function is shown in both the time

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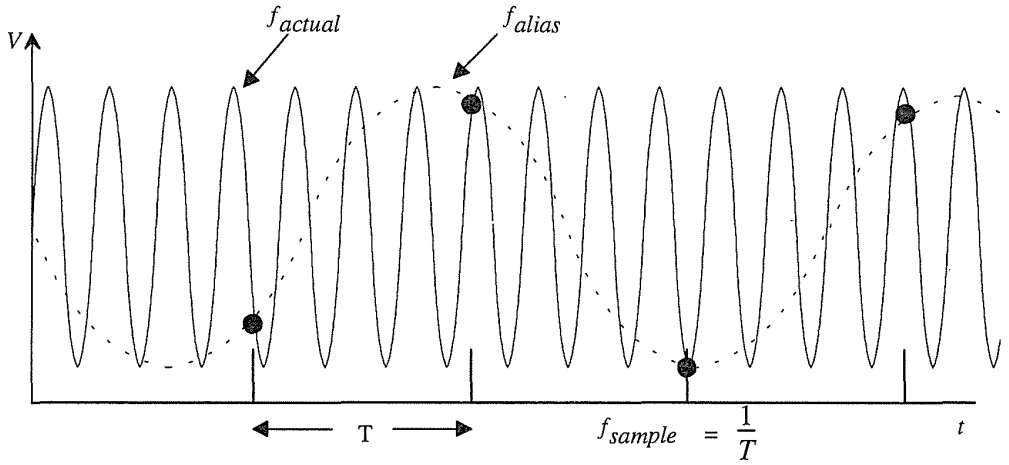


Figure 28.25 Illustration of aliasing caused by undersampling.

and frequency domain. The sampling function simply represents the action of sampling at discrete points in time. The frequency domain version of the sampling function is similar to its time domain counterpart, except that the x-axis is now represented as $f = 1/T$. Since each of the impulses has a value of 1, the resulting sampled signal shown in Fig. 28.26c is the impulse function multiplied by the amplitude of the analog signal at each discrete point in time. Remembering that multiplication in the time domain is equivalent to convolution in the frequency domain, we note that the frequency domain representation of the sampled signal reveals that the overall signal consists of multiple versions of the band-limited signal at multiples of the sampling frequency.

Note in Fig. 28.26b that as the sampling time increases, the sampling frequency decreases and the impulses in the frequency domain become more closely spaced. This results in 28.26d, which illustrates the aliasing as the multiple versions of the band-limited signal begin to overlap. One could also filter the signal "post-sampling" and eliminate the frequencies for which overlap occurs. The point at which the spectra overlap is called the *folding frequency.*

As mentioned earlier, the solutions to aliasing are higher sampling frequency and filtering. Focusing on just one of the solutions may worsen the situation for several reasons. Some noise signals are wide band, which means that they have a large bandwidth. Attempting to increase only the sampling frequency to eliminate the aliasing effects of the noise would be a practical impossibility, not to mention a costly one. However, simply filtering the input signal and the sampled signal will add delays to the overall conversion and increase the expense of the circuit. It is best to use a combination of the two to minimize the problem most efficiently.

Signal-to-Noise Ratio

Signal-to-noise (SNR) ratios of ADCs represent the value of the largest RMS input signal into the converter over the RMS value of the noise. Typically given in dB, the expression for SNR is

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$$SNR = 20\text{Log}(\frac{v_{in(max)}}{v_{noise}}) \tag{28.23}$$

If it is assumed that the input signal is a sinewave with a peak-to-peak value equal to the full-scale reference voltage of the converter, then the RMS value for $v_{in(max)}$ becomes

$$v_{in(max)} = \frac{V_{REF}}{2\sqrt{2}} = \frac{2^N(V_{LSB})}{2\sqrt{2}} \tag{28.24}$$

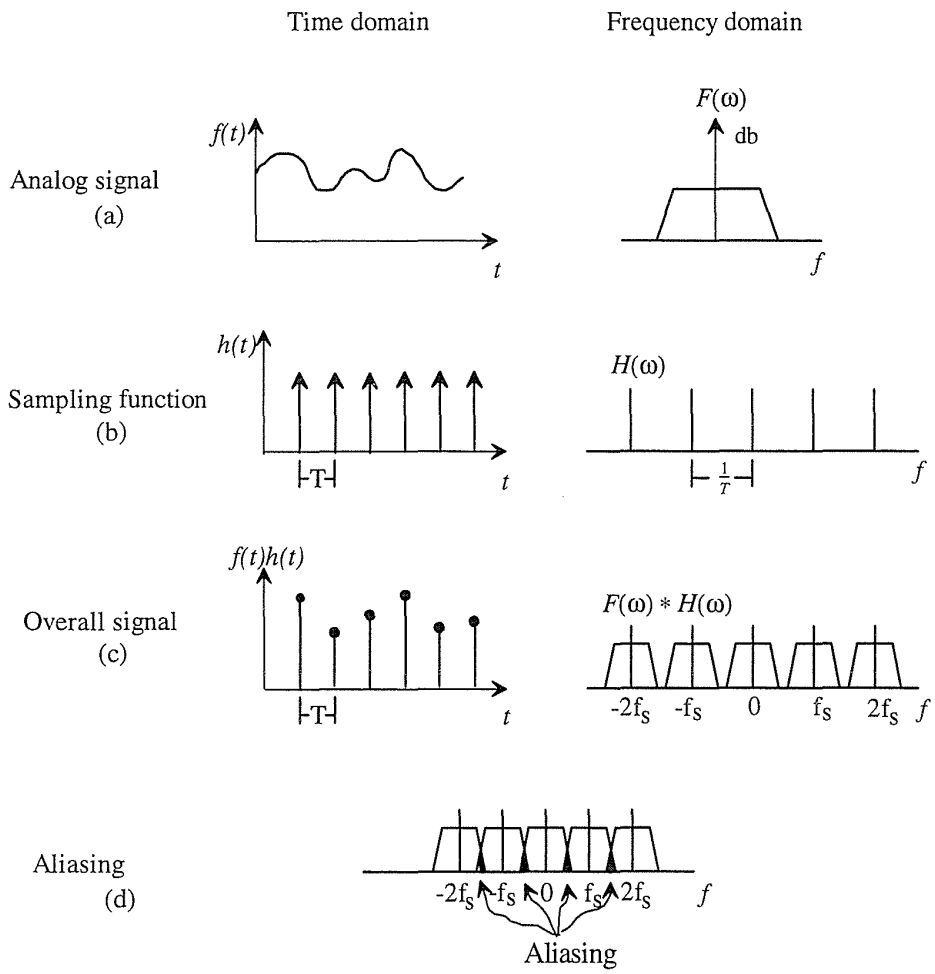


Figure 28.26 Illustration of aliasing in the time and frequency domain. (a) The analog signal; (b) the sampling function; (c) the overall signal; and (d) aliasing in the frequency domain.

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where V_{LSB} is the voltage value of 1 LSB. The value of the noise (if the data converter is considered to be ideal) will be equivalent to the RMS value of the error signal, Q_e (in volts), shown in Fig. 28.20b. The RMS value of Q_e can be calculated to be

$$Q_{e,RMS} = \frac{V_{LSB}}{\sqrt{12}} \tag{28.25}$$

Therefore, the SNR for the ideal ADC will be the ratio of these two RMS values.

$$SNR = 20\text{Log}\frac{\frac{2^N(V_{LSB})}{2\sqrt{2}}}{\frac{V_{LSB}}{\sqrt{12}}} \tag{28.26}$$

which can be written in terms of N as simply

$$SNR = 20N\text{Log}(2) + 20\text{Log}\sqrt{12} - 20\text{Log}(2\sqrt{2}) = 6.02N + 1.76 \tag{28.27}$$

Equation (28.27) is an important one relating SNR to the resolution of the ADC. For 16-bit data conversion, one must design a circuit that will have a SNR of (6.02)(16) + 1.76 = 98.08 dB! Equation (28.7) can also be used in calculating the *signal-to-noise plus distortion ratio*, also known as *SNRD*. Since the output data is digital, we cannot use a spectrum analyzer to calculate this ratio, but must instead use a *Discrete Fourier Transform* (*DFT*) and examine the data in the digital domain.

Another useful application of Eq. (28.19) is the determination of effective number of bits given a system with a known SNR or SNRD. For example, if a 16-bit ADC yielded an SNRD of 88 dB, then the effective resolution of the converter would be

$$N = \frac{88 - 1.76}{6.02} = 14.32 \text{ bits} \tag{28.28}$$

and the ADC would be producing the resolution equivalent to that of a 14-bit converter.

Aperture Error

The aperture error described in Sec. 28.3 (S/H) should be related to the errors associated with the ADC. In the previous discussion, the aperture error resulted in sampling error (Fig. 28.8). However, now that ADC characteristics have been discussed, we can relate the sampling error to the ADC. Since we know that the maximum errors associated with an ADC are related to ½ LSB, we can assume that the maximum sampling error associated with the aperture uncertainty can be no larger than ½ LSB.

Example 28.8

Find the maximum resolution of an ADC which can use the S/H described in Ex. 28.1 while maintaining a sampling error less than ½ LSB.

Since it was determined that the maximum sampling error produced by the given aperture uncertainty was 0.628 mV, we can relate this value to the highest resolution of an ADC by assuming that 0.628 mV will be less than or equal ½ LSB. Therefore,

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$$0.628 \text{ mV} \leq .5\ LSB = \frac{V_{REF}}{2^{N+1}} = \frac{5}{2^{N+1}}$$

or

$$2^{N+1} \leq 7961.8$$

which, solving for N (limited to an integer), yields a maximum resolution of 11 bits. ■

28.6 Mixed-Signal Layout Issues

Naturally, analog ICs are more sensitive to noise than digital ICs. For any analog design to be successful, careful attention must be paid to layout issues, particularly in a digital environment. Sensitive analog nodes must be protected and shielded from any potential noise sources. Grounding and power supply routing must also be considered when using digital and analog circuitry on the same substrate. Since a majority of ADCs use switches controlled by digital signals, separate routing channels must be provided for each type of signal.

Techniques used to increase the success of mixed-signal designs vary in complexity and priority. Strategies regarding systemwide minimization of noise should always be considered foremost. A mixed-signal layout strategy can be modeled as seen in Fig. 28.27. The lowest issues are foundational and must be considered before each succeeding step. The successful mixed-signal design will always minimize the effect of the digital switching on the analog circuits.

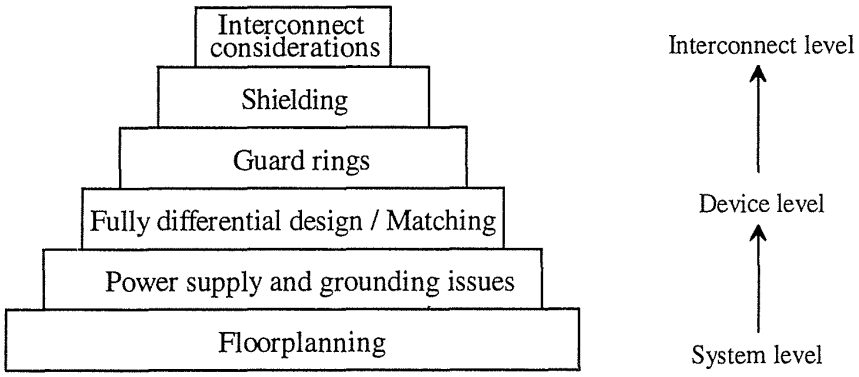


Figure 28.27 Mixed-signal layout strategy.

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Floorplanning

The placement of sensitive analog components can greatly affect a circuit's performance. Many issues must be considered. In designing a mixed-signal system, strategies regarding the "floorplan" of the circuitry should be thoroughly analyzed well before the layout is to begin.

The analog circuitry should be categorized by the sensitivity of the analog signal to noise. For example, low-level signals or high-impedance nodes typically associated with input signals are considered to be sensitive nodes. These signals should be closely guarded and shielded especially from digital output buffers. High-swing analog circuits such as comparators and output buffer amplifiers should be placed between the sensitive analog and the digital circuitry.

The digital circuitry should also be categorized by speed and function. Obviously, since digital output buffers are usually designed to drive capacitive loads at very high rates, they should be kept farthest from the sensitive analog signals. Next, the high and lower speed digital should be placed between the insensitive analog and the output buffers. An example of this type of strategy can be seen in Fig. 28.28 [6]. Notice that *the sensitive analog is as far away as possible from the digital output buffers* and that the least sensitive analog circuitry is next to the least offensive digital circuitry.

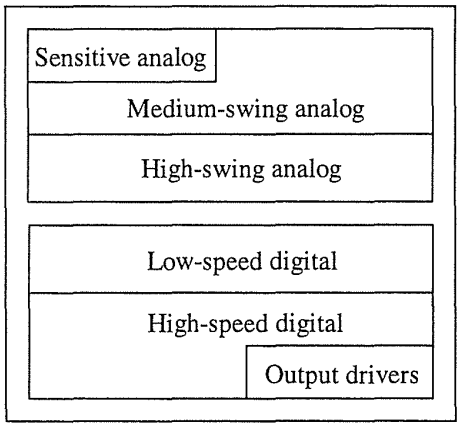


Figure 28.28 Example of a mixed-signal floorplan [6].

Power Supply and Grounding Issues

Whenever analog and digital circuit reside together on the same die, danger exists of injecting noise from the digital system to the sensitive analog circuitry through the power supply and ground connections. Much of the intercoupling can be minimized by carefully considering how power and ground are supplied to both the analog and digital circuits.

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Examine Fig. 28.29a. Here, analog and digital circuitry share the same routing to a single pad for power and ground. The resistors, R_{I1} and R_{I2}, represent the small, nonnegligible resistance of the interconnect to the pad. The inductors, L_{B1} and L_{B2}, represent the inductance of the bonding wire which connects the pads to the pin on the lead frame. Since digital circuitry is typified by high amounts of transient currents due to switching, a small amount of resistance associated with the interconnect can result in significant voltage spikes. Low-level analog signals are very sensitive to such interference, thus resulting in a contaminated analog system. Another significant voltage spike can occur due to the inductance of the bonding wire. Since the voltage across the inductor is proportional to the change in current through it, voltage spikes equating to hundreds of millivolts can result! Both of these voltage effects are true for both the power and ground connection.

One way to reduce the interference, seen in Fig. 28.29b, is to prohibit the analog and digital circuit from sharing the same interconnect. The routing for the supply and ground for both the analog and digital sections are provided separately. Although this

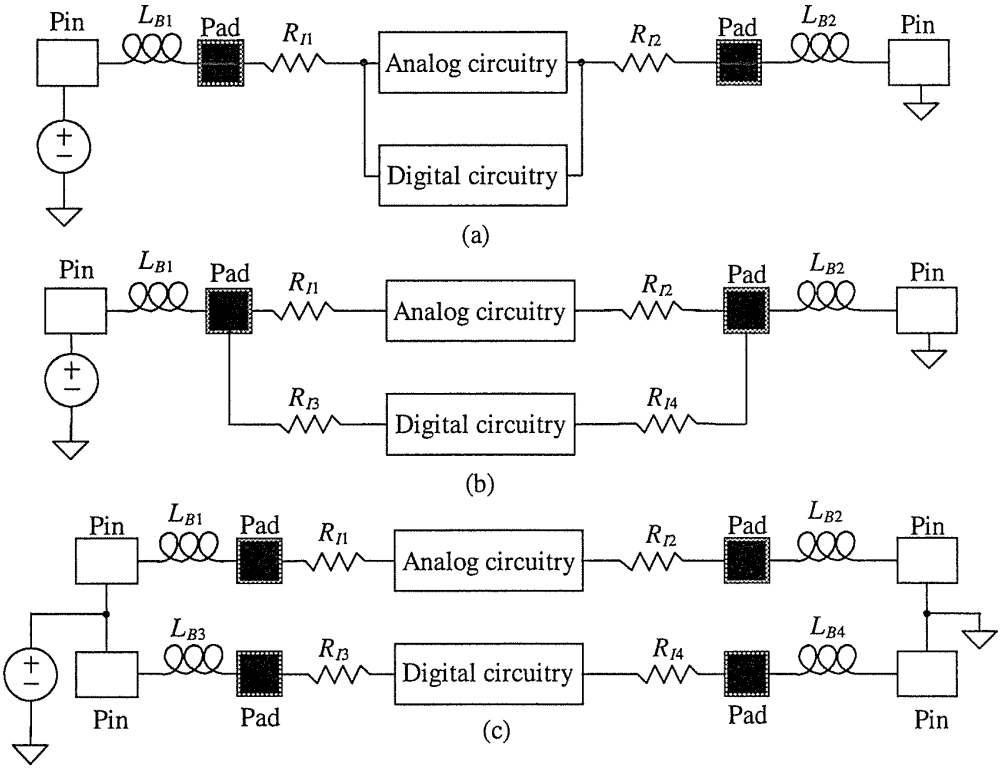


Figure 28.29 Power and ground connection examples, (a) poor noise immunity and (b) better noise immunity, and (c) using separate power and ground pins to achieve even better immunity.

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eliminates the parasitic resistance due to the common interconnect, there is still a common inductance due to the bonding wire which causes interference.

Another method that minimizes interference even more than the previous case is seen in Fig. 28.29c. *By using separate pads and pins, the analog and the digital circuits are completely decoupled.* The current through the analog interconnect is much less abrupt than the digital; thus, the analog circuitry now has a "quiet" power and ground. However, this technique is dependent on whether extra pins and pads are available for this use. The separate power supply and ground pins are then connected externally. *It is not wise to use two separate power supplies because if both types of circuits are not powered up simultaneously, latch-up could easily result.*

In cases presented in Fig. 28.29b and c, *the resistance associated with the analog connection to ground or supply can be reduced by making the power supply and ground bus as wide as feasible.* This reduces the overall resistance of the metal run, thus decreasing the voltage spikes that occur across the resistor. The inductor itself is impossible to eliminate, though it can be minimized with careful planning. Since the length of the bonding wire is dependent on the distance from the pad to the lead frame, *one could reduce the effect of the wire inductance by reserving pins closest to the die for sensitive connections such as analog supply and ground.* This, again, illustrates the importance of floorplanning.

Fully Differential Design

Fully differential operational amplifiers were presented in Ch. 25, and Fig. 28.30 was first presented in Sec. 25.3. The noise source represents the noise from digital circuitry coupled through the parasitic stray capacitors. If equal amounts of noise are injected into the differential amplifiers, then the common-mode rejection inherent in the amplifiers will eliminate most or all of the noise. This, of course, is dependent on the symmetry of the amplifiers, meaning that the matching of the transistors in the amplifier becomes crucial. Therefore, *in a mixed-signal environment, layout techniques should be used to improve matching.* Common-centroid and interdigitated techniques were discussed in Secs. 20.1.6 and 24.1.4.

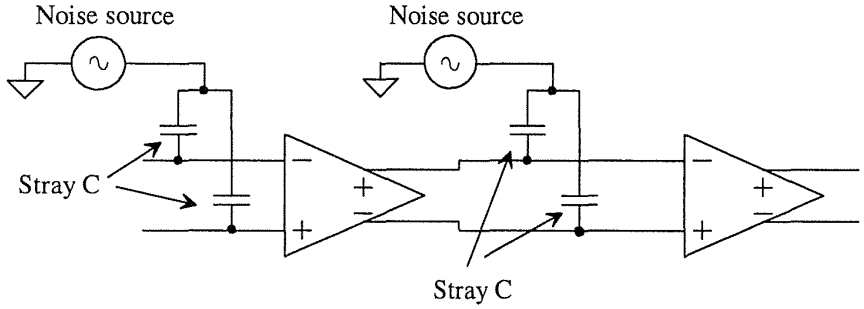


Figure 28.30 Differential output op-amps showing parasitic coupling to noise sources.

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Guard Rings

Guard rings, discussed previously in Secs. 7.2.1 and 11.3.1, should be used wisely throughout a mixed-signal environment. Circuits that process sensitive signals should be placed in a separate well with guard rings attached to the analog *VDD* supply. In the case of the CN20 process, the n-type devices outside the well should have guard rings attached to analog *VSS* placed around them as well. Digital circuits should be placed in their own well with guard rings attached to digital *VDD*. Guard rings placed around the n-channel digital devices will also help minimize the amount of noise transmitted from the digital devices.

Shielding

A number of techniques exist which can shield sensitive, low-level analog signals from noise resulting from digital switching. A shield can take the form of a layer tied to analog ground placed between two other layers, or it can be a barrier between two signals running in parallel.

If at all possible, one should avoid crossing sensitive analog signals, such as low-level analog input signals, with any digital signals. The parasitic capacitance coupling the two signal lines can be as much as a couple of fF, depending on the process. If it cannot be avoided, then attempt to carry the digital signal using the top layer of metal (such as metal2). If the analog signal is an input signal, then it will most likely be carried by the poly layer. A strip of metal1 can be placed between the two layers and connected to analog ground (see Fig. 28.31).

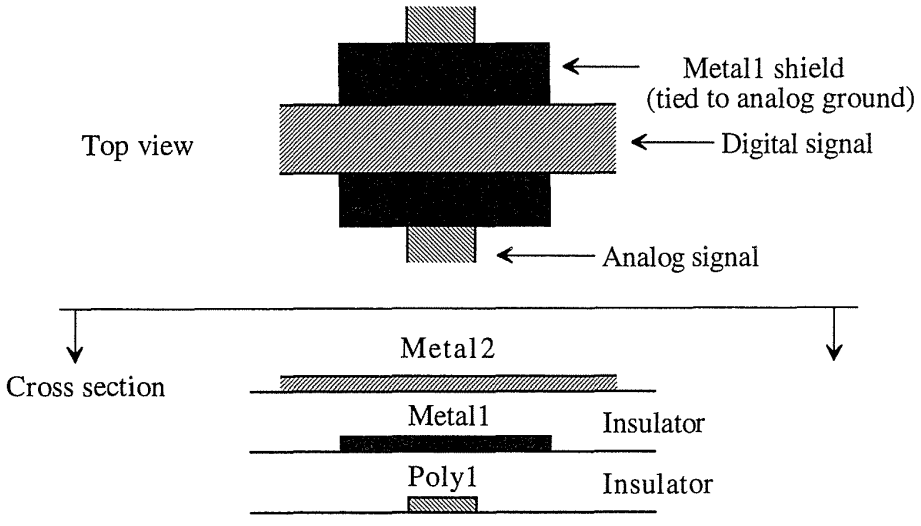


Figure 28.31 Shielding a sensitive analog signal from a digital signal crossover using a metal 1 shield layer.

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Another situation that should be avoided is running interconnect containing sensitive analog signals parallel and adjacent to any interconnect carrying digital signals. Coupling occurs due to the parasitic capacitance between the lines. If this situation cannot be avoided, then an additional line connected to analog ground should be placed between the two signals, as seen in Fig. 28.32. This method can also be used to partition the analog and digital sections of the chip.

In addition, the n-well can be used as a bottom-plate shield to protect analog signals from substrate noise. Poly resistors (or capacitors) used for sensitive analog signals can be shielded by placing an n-well beneath the components and connecting the well to analog *VDD*.

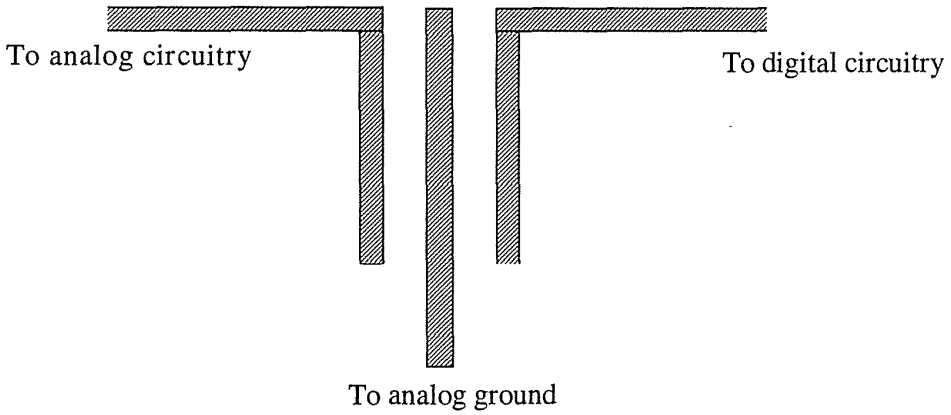


Figure 28.32 Use of a dummy metal strip to provide shielding to two parallel signals.

Other Interconnect Considerations

Finally, some other layout strategies will incrementally improve the performance of the analog circuitry. However, if the previous strategies are not followed, these suggestions will be useless. *When routing the analog circuitry, minimize the lengths of current carrying paths.* This will simply reduce the amount of voltage drop across the path due to the metal1 or metal2 resistance. *Contacts should also be used very liberally whenever changing layers.* Not only does this minimize resistance in the path, but it also improves fabrication reliablity. *Avoid using poly to route current carrying signal paths.* Not only is the poly higher in resistance value, but also the additional contact resistance required to change layers will not be insignificant. If the poly is made wider to lower the resistance, additional parasitic capacitance will be added to the node. *Use poly to route only high-impedance gate nodes that carry virtually no current.*

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PROBLEMS

28.1 Determine the number of quantization levels needed if one wanted to make a digital thermometer that was capable of measuring temperatures to within 0.1 °C accuracy over a range from – 50 °C to 150 °C. What resolution of ADC would be required?

28.2 Using the same thermometer as above, what sampling rate, in samples per second, would be required if the temperature displayed a frequency of $15°\cdot\sin(0.01\cdot 2\pi t)$?

28.3 Determine the maximum droop allowed in a S/H used in a 16-bit ADC assuming that all other aspects of both the S/H and ADC are ideal. Assume $V_{ref} = 5$ V.

28.4 A S/H circuit settles to within 1 percent of its final value at 5 μs. What is the maximum resolution and speed with which an ADC can use this data assuming that the ADC is ideal?

28.5 A digitally programmable signal generator uses a 14-bit DAC with a 10 volt reference to generate a DC output voltage. What is the smallest incremental change at the output that can occur? What is the DAC's full-scale value? its accuracy?

28.6 Determine the maximum DNL (in LSBs) for a 3-bit DAC which has the following characteristics. Does the DAC have 3-bit accuracy? If not, what is the resolution of the DAC having this characteristic?

Digital Input	Voltage Output
000	0 V
001	0.625 V
010	1.5625 V
011	2.0 V
100	2.5 V

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101	3.125 V
110	3.4375 V
111	4.375 V

28.7 Repeat Problem 28.6 calculating the INL (in LSBs).

28.8 A DAC has a reference voltage of 1,000 V and has its maximum INL measured to be 2.5 mV. What is the maximum resolution of the converter assuming that all the other characteristics of the converter are ideal?

28.9 Determine the INL and DNL for a DAC that has a transfer curve shown in Fig. P28.9.

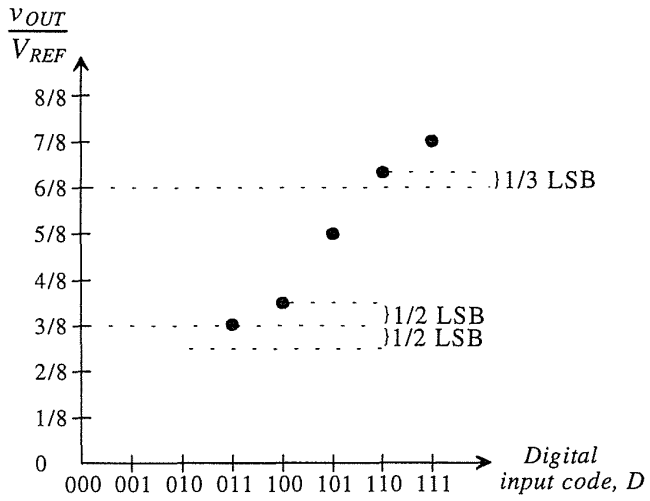


Figure P28.9

28.10 A DAC has a full-scale voltage of 4.97 V using a 5 V reference, and its minimum output voltage is limited by the value of one LSB. Determine the resolution and dynamic range of the converter.

28.11 Prove that the RMS value of the quantization noise shown in Fig. 28.20b is as stated in Eq. (28.26).

28.12 An ADC has a stated SNR of 94 dB. Determine the effective number of bits of resolution of the converter.

28.13 Discuss the methods used to prevent aliasing and the advantages and disadvantages of each.

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Chapter

29

Data Converter Architectures

Applications such as wireless communications and digital audio and video have created the need for cost-effective data converters that will achieve higher speed and resolution. The needs required by digital signal processors continually challenge analog designers to improve and develop new ADC and DAC architectures. There are many different types of architectures, each with unique characteristics and different limitations. This chapter presents a basic overview of the more popular data converter architectures and discusses the advantages and disadvantages of each along with their limitations.[1]

Now that we have defined the operating characteristics of ADCs, a more detailed examination of the basic architectures will be discussed using a top-down approach. Since many of the converters use op-amps, comparators, and resistor and capacitor arrays, the top-down approach will allow a broader discussion of the key component limitations in later sections.

29.1 DAC Architectures

A wide variety of DAC architectures exist, ranging from very simple to complex. Each, of course, has its own merits. Some use voltage division, whereas others employ current steering and even charge scaling to map the digital value into an analog quantity.

29.1.1 Digital Input Code

In many cases, the digital signal is not provided in binary code but is any one of a number of codes: binary, BCD, thermometer code, Gray code, sign-magnitude, two's complement, offset binary, and so on. (See Fig. 29.1 for a comparison of some of the more commonly used digital input codes.) For example, it may be desirable to allow only one bit to change value when changing from one code to the next. If that is the case, a Gray code will suffice. The thermometer code is used quite frequently and can

[1] Much of the material in this chapter is based on course notes provided by Dr. Terry Sculley, of Crystal Semiconductor Corporation, Austin, Texas.

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Decimal	Binary	Thermometer	Gray	Two's Complement
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

Figure 29.1 Comparison of digital input codes.

also be seen in Fig. 29.1. Notice that it requires $2^N - 1$ bits to represent an N-bit word. The code used is purely dependent on the application, and the reader should be aware that many types of codes are available.

29.1.2 Resistor String

The most basic DAC is seen in Fig. 29.2a. Comprised of a simple resistor string of 2^N identical resistors and switches, the analog output is simply the voltage division of the resistors at the selected tap. Note that a N:2^N decoder will be required to provide the 2^N signals controlling the switches. This architecture typically results in good accuracy, provided that no output current is required and that the values of the resistors are within the specified error tolerance of the converter. One big advantage of a resistor string is that the output will always be guaranteed to be monotonic.

One problem with this converter is that the converter output is always connected to $2^N - 1$ switches that are off and one switch that is on. For larger resolutions, a large parasitic capacitance appears at the output node, resulting in slower conversion speeds. A better alternative for the resistor string DAC is seen in Fig. 29.2b. Here, a binary switch array ensures that the output is connected to at most N switches that are on and N switches that are off, thus increasing the conversion speed. The input to this switch array is a binary word since the decoding is inherent in the binary tree arrangement of the switches.

Another problem with the resistor string DAC is the balance between area and power dissipation. An integrated version of this converter will lead to a large chip area for higher bit resolutions because of the large number of passive components needed. Active resistors such as the N-well resistor can be used for low-resolution applications. However, as the resolution increases, the relative accuracy of the resistors becomes an important factor. Although the value of R could always be made small to minimize the

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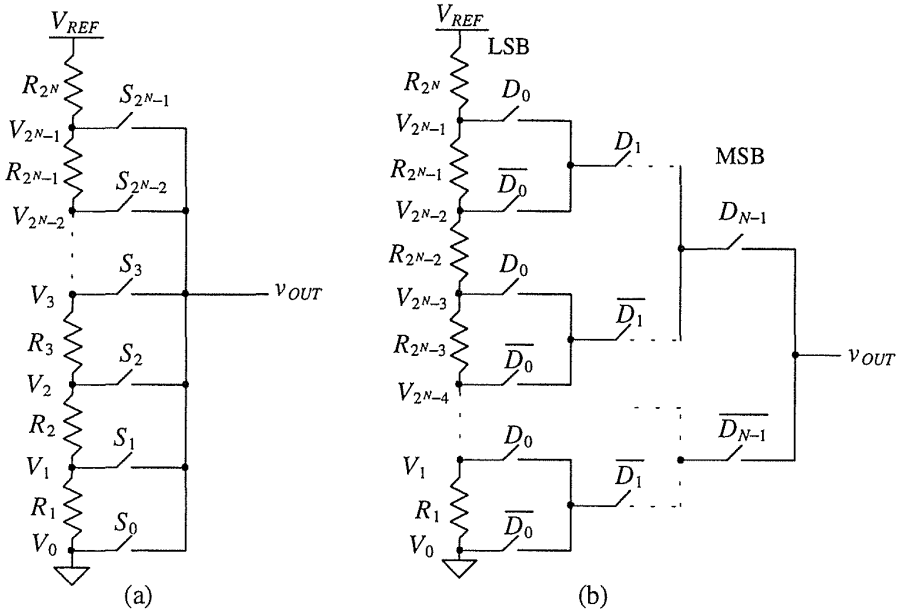


Figure 29.2 (a) A simple resistor string DAC and (b) use of a binary switch array to lower the output capacitance.

chip area required, power dissipation would then become the critical issue as current flows through the resistor string at all times.

Example 29.1

Design a 3-bit resistor string ladder using a binary switch array. Assume that $V_{REF} = 5$ V and that the maximum power dissipation of the converter is to be 5 mW (not including the power required by the digital logic). Determine the value of the analog voltage for each of the possible digital input codes.

The power dissipation will determine the current flowing through the resistor string by

$$I_{MAX} = \frac{5 \times 10^{-3}\ \text{W}}{5\ \text{V}} = 1\ \text{mA}$$

Since a 3-bit converter will have eight resistors, the value of R is

$$R = \frac{1}{8} \cdot \frac{5\ \text{V}}{1\ \text{mA}} = 625\ \Omega$$

The converter can be seen in Fig. 29.3. Examine the switch array if the input code is $D_2D_1D_0 = \underline{100}$ or 4_{10}. Since D_2 is high, the top switch will be closed and the lower switch, $\overline{D_2}$, will be open. In the row corresponding to D_1, since $D_1 = 0$, both of the switches marked $\overline{D_1}$ will be closed and the other two will be open. The LSB controls the largest number of switches; therefore, since D_0 is low, all

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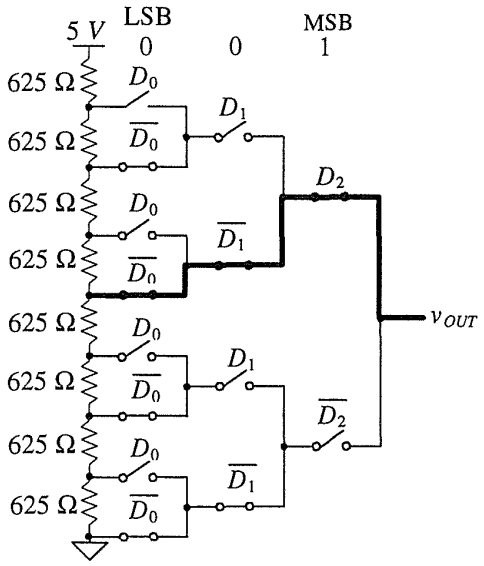


Figure 29.3 A 3-bit resistor string DAC used in Ex. 29.1

the $\overline{D_0}$ switches will be closed and all the D_0 switches will be open. There should be only one path connecting a single tap on the resistor string to the output. This is bolded, with the resistor string tapped in the middle of the string. Therefore, $v_{OUT} = ½\ V_{REF} = 2.5$ V. The remaining outputs can be seen in Fig. 29.4. ■

$D_2D_1D_0$	v_{OUT}
000	0
001	0.625
010	1.25
011	1.875
100	2.5
101	3.125
110	3.75
111	4.375

Figure 29.4 Output voltages generated from the 3-bit DAC in Ex. 29.1.

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Mismatch Errors Related to the Resistor String DAC

The accuracy of the resistor string is obviously related to matching between the resistors, which ultimately determines the INL and DNL for the entire DAC. Suppose that the i-th resistor, R_i, has a mismatch error associated with it so that

$$R_i = R + \Delta R_i \tag{29.1}$$

where R is the ideal value of the resistor and ΔR_i is the mismatch error. Also suppose that the mismatches were symmetrical about the string so that the sum of all the mismatch terms were zero, or

$$\sum_{i=1}^{2^N} \Delta R_i = 0 \tag{29.2}$$

The value of the voltage at the tap associated with the i-th resistor should ideally be

$$V_{i,ideal} = \frac{(i)V_{REF}}{2^N}, \text{ for } i = 0, 1, 2, ..., 2^N - 1 \tag{29.3}$$

However, including the mismatch, the actual value of the i-th voltage will be the sum of all the resistances up to and including resistor i, divided by the sum of all the resistances in the string. This can be represented by

$$V_i = V_{REF} \cdot \frac{\sum_{k=1}^{i} R_k}{\sum_{k=1}^{2^N} R_k} = V_{REF} \cdot \frac{\sum_{k=1}^{i} R + \Delta R_k}{2^N R} \tag{29.4}$$

The denominator does not include any mismatch error since it was assumed that the mismatches sum to zero as defined in Eq. (29.2). Notice that there is no resistor, R_0, corresponding to V_0 (see Fig. 29.2), and it is assumed that V_0 is ground. Equation (29.4) can be rewritten as

$$V_i = \frac{V_{REF}}{2^N R}\left[(i)R + \sum_{k=1}^{i} \Delta R_k\right] = \frac{(i)V_{REF}}{2^N} + \frac{V_{REF}}{2^N R}\sum_{k=1}^{i} \Delta R_k \tag{29.5}$$

or finally, the value of the voltage at the i-th tap is

$$V_i = V_{i,ideal} + \frac{V_{REF}}{2^N} \cdot \sum_{k=1}^{i} \frac{\Delta R_k}{R} \tag{29.6}$$

Equation (29.6) is not of much importance by itself, but it can be used to help determine the nonlinearity errors.

Integral Nonlinearity of the Resistor String DAC

Integral nonlinearity (INL) is defined as the difference between the actual and ideal switching points, or

$$INL = V_i - V_{i,ideal} \tag{29.7}$$

and plugging in Eqs. (29.6) and (29.3) into (29.7) yields,

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$$INL = \frac{V_{REF}}{2^N} \cdot \sum_{k=1}^{i} \frac{\Delta R_k}{R} \tag{29.8}$$

Equation (29.8) is a general expression for the INL for a given resistor, R_i, and requires that the mismatch of all the resistances used in the summation are known. However, this equation does not illuminate how to determine the *worst-case* or maximum INL for a resistor string.

Intuitively, one would think that the worst-case INL would occur at the top of the resistor string (i=2^N) with all the ΔR_k's at their maximum values. However, the previous derivation was performed with the assumption that the mismatches summed to zero. With this restriction, the maximum INL will occur at the midpoint of the string corresponding to $i = 2^{N-1}$, corresponding to the case where the MSB was a one and all other bits were zero. Another condition that will ensure a worst-case scenario will be to consider the lower half resistors at their maximum positive mismatch value and upper half resistors at their maximum negative mismatch value, or vice versa.

If the resistors on a string were known to have 2 percent matching, then ΔR_k would be constrained to the bounds of

$$-0.02R \le \Delta R_k \le 0.02R \tag{29.9}$$

and the worst-case INL (again, assuming 2 percent matching) using Eq. (29.8) would be,

$$|INL|_{max} = \frac{V_{REF}}{2^N} \cdot \sum_{k=1}^{2^{N-1}} \frac{\Delta R_k}{R} = \frac{V_{REF}}{2^N} \cdot \frac{2^{N-1} \cdot 0.02R}{R} = 0.01 \cdot V_{REF} \tag{29.10}$$

Note that Eq. (29.10) has units of volts, which can easily be converted to LSBs. We can use Eq. (29.10) to determine the effective resolution of a DAC using a resistor string, as will be seen in the next example.

Because the worst-case analysis was performed, the maximum INL occurs at the middle of the string. We can improve this specification on paper by using the "best-fit" approach to measuring INL. In this case, the reference line is simply shifted up slightly (refer to Ch. 28) so that it no longer passes through the end points, but instead minimizes the INL.

Example 29.2

Determine the effective number of bits for a resistor string DAC, which is assumed to be limited by the INL. The resistors are passive poly resistors with a known relative matching of 1 percent and V_{REF} = 5 V.

Using Eq. (29.10), the maximum INL will be

$$|INL|_{max} = 0.005 \cdot V_{REF} = 0.025 \text{ V}$$

Since we know that this maximum INL should be equal to ½ LSB in the worst case,

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$$\frac{1}{2}LSB = \frac{5}{2^{N+1}} = 0.025 \text{ V}$$

and solving for N yields

$$N = \log_2\left(\frac{5}{0.025}\right) - 1 = 6.64 \text{ bits}$$

This means that the resolution for a DAC containing a resistor string matched to within 1 percent will be, at most 6 bits. ■

Differential Nonlinearity of the Worst-Case Resistor String DAC

Resistor string matching is not as critical when determining the DNL. Remembering that the definition of DNL is simply the actual height of the stair-step in the DAC transfer curve minus the ideal step height, we can write this in terms of the voltages at the taps of adjacent resistors on the string. Using Eq. (29.5), we can express this as,

$$|V_i - V_{i-1}| = \left|\left[\frac{(i)V_{REF}}{2^N} + \frac{V_{REF}}{2^N}\cdot\sum_{k=1}^{i}\frac{\Delta R_k}{R}\right] - \left[\frac{(i-1)V_{REF}}{2^N} + \frac{V_{REF}}{2^N}\cdot\sum_{k=1}^{i-1}\frac{\Delta R_k}{R}\right]\right|$$

which can be simplified to

$$|V_i - V_{i-1}| = \left|\frac{V_{REF}}{2^N}\left(1 + \frac{\Delta R_i}{R}\right)\right| \tag{29.11}$$

The DNL can then be determined by subtracting the ideal step height from Eq. (29.11),

$$DNL_i = \left|\frac{V_{REF}}{2^N}\left(1 + \frac{\Delta R_i}{R}\right) - \frac{V_{REF}}{2^N}\right| = \left|\frac{V_{REF}}{2^N}\cdot\frac{\Delta R_i}{R}\right| \tag{29.12}$$

and the maximum DNL will occur at the value of i for which ΔR is at its maximum value. If it is assumed once again that the resistors are matched to within 2 percent, the worst-case DNL will be

$$DNL_{max} = \left|0.02 \cdot \frac{V_{REF}}{2^N}\right| = 0.02\ LSB \tag{29.13}$$

which is well below the ½ LSB limit. The INL is obviously the limiting factor in determining the resolution of a resistor string DAC since its maximum value is 2^N times larger than the DNL.

29.1.3 *R*-2*R* Ladder Networks

Another DAC architecture that incorporates fewer resistors is called the R-$2R$ ladder network [1]. This configuration consists of a network of resistors alternating in value of R and $2R$. Figure 29.5 illustrates an N-bit R-$2R$ ladder. Starting at the right end of the network, notice that the resistance looking to the right of any node to ground is $2R$. The digital input determines whether each resistor is switched to ground (noninverting input) or to the inverting input of the op-amp. Each node voltage is related to V_{REF}, by a binary-weighted relationship caused by the voltage division of the ladder network. The total current flowing from V_{REF} is constant, since the potential at the bottom of each

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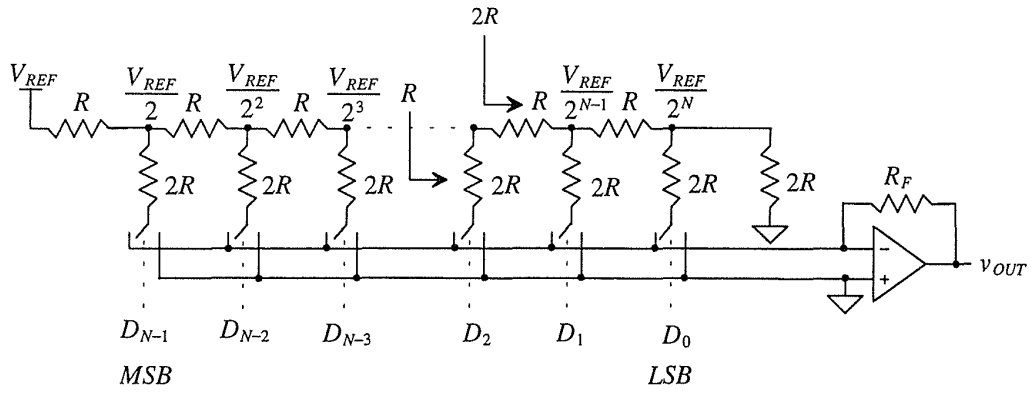


Figure 29.5 An *R*-2*R* digital-to-analog converter.

switched resistor is always zero volts (either ground or virtual ground). Therefore, the node voltages will remain constant for any value of the digital input.

The output voltage, v_{OUT}, is dependent on currents flowing through the feedback resistor, R_F, such that

$$v_{OUT} = -i_{TOT} \cdot R_F \tag{29.14}$$

where i_{TOT} is the sum of the currents selected by the digital input by

$$i_{TOT} = \sum_{k=0}^{N-1} D_k \cdot \frac{V_{REF}}{2^{N-k}} \cdot \frac{1}{2R} \tag{29.15}$$

where D_k is the k-th bit of the input word with a value that is either a 1 or a 0.

This architecture, like the resistor string architecture, requires matching to within the resolution of the converter. Therefore, the switch resistance must be negligible, or a small voltage drop will occur across each switch, resulting in an error. One way to eliminate this problem is to add dummy switches. Assume that the resistance of each switch connected to the 2*R* resistors is ΔR, as seen in Fig. 29.6. Dummy switches with one-half the resistance of the real switches are "hard-wired" so that they are always on and placed in series with each of the horizontal resistors. The total resistance of any horizontal branch, R', is

$$R' = R + \frac{\Delta R}{2} \tag{29.16}$$

The resistance of any vertical branch is $2R + \Delta R$, which is twice the value of the horizontal branch. Therefore, a $R' - 2R'$ relationship is maintained. Of course, a dummy switch equal to the switch size of a 2*R* switch will have to be placed in series with the terminating resistor as well.

Example 29.3

Design a 3-bit DAC using a *R*-2*R* architecture with R = 1 kΩ, R_F = 2 kΩ, and V_{REF} = 5 V. Assume that the resistances of the switches are negligible.

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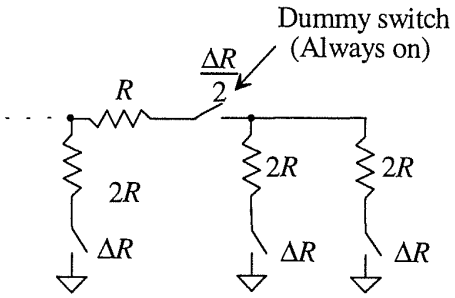


Figure 29.6 Use of dummy switches to offset switch resistance.

Determine the value of i_{TOT} for each digital input and the corresponding output voltage, v_{OUT}.

Figure 29.7 shows the 3-bit DAC for a digital input of 001. The voltages at each node in the resistor network are labeled. For each switch, if the digital input bit is a 0, then the resistor is attached to the ground. If the bit is a 1, then the resistor is attached to the virtual ground of the inverting input and current flows to the output of the op-amp. Therefore, for $D_2D_1D_0$ = 000, all the switches are connected to ground and no current flows through the feedback resistor and the output voltage, v_{OUT}, is zero.

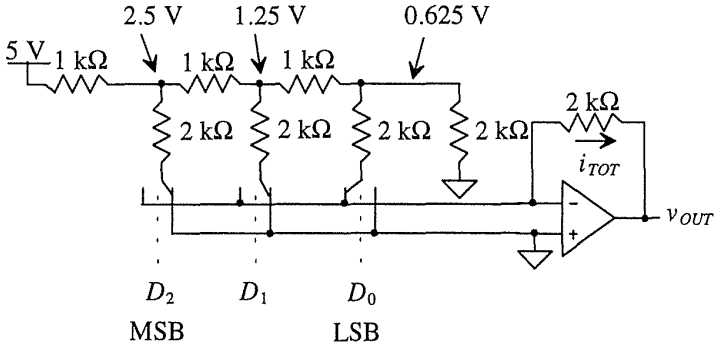


Figure 29.7 A 3-bit *R*-2*R* digital-to-analog converter used in Ex. 29.3.

When $D_2D_1D_0$ = 001, the rightmost resistor is switched to the op-amp inverting input and the other two resistors remain attached to ground. Therefore, the total current flowing through the feedback resistor will simply be the current through the rightmost resistor, which is defined by Eq. (29.15) as

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$$\frac{V_{REF}}{8} \cdot \frac{1}{2000} = 0.3126 \text{ mA}$$

and the output voltage, by Eq. (29.14) becomes,

$$v_{OUT} = -(0.3126 \text{ mA})(2000\ \Omega) = -0.625 \text{ V}$$

which is to be expected. The other values for the output voltage can be calculated using Eqs. (29.14) and (29.15) and are seen in Fig. 29.8. ■

$D_2D_1D_0$	i_{TOT} (mA)	v_{OUT} (V)
000	0	0
001	0.3125	– 0.625
010	0.625	– 1.25
011	0.625 + 0.3125 = 0.9375	– 1.875
100	1.25	– 2.5
101	1.25 + 0.3125 = 1.5625	– 3.125
110	1.25 + 0.625 = 1.875	– 3.75
111	1.25 + 0.625 + 0.3125 = 2.1875	– 4.375

Figure 29.8 Output voltages generated from the 3-bit DAC in Example 29.3.

29.1.4 Current Steering

In the previous section, a voltage was converted into a current, which then generated a voltage at the output. Another DAC method uses current throughout the conversion. Known as *current steering*, this type of DAC requires precision current sources that are summed in various fashions.

Figure 29.9 illustrates a generic current steering DAC. This configuration requires a set of current sources, each having a unit value of current, I. Since there are no current sources generating i_{OUT} when all the digital inputs are zero, the MSB, D_{2^N-2}, is offset by two bits instead of one. For example, for a 3-bit converter, seven current sources will be needed, labeled from D_0 to D_6. The binary signal controls whether or not the current sources are connected to either i_{OUT} or some other summing node (in this case ground). The output current, i_{OUT}, has the range of

$$0 \le i_{OUT} \le (2^N - 1) \cdot I \tag{29.17}$$

and can be any integer multiple of I in between. An interesting issue to note is the format of the digital code required to drive the switches. Since there are $2^N - 1$ current sources, the digital input will be in the form of a *thermometer code*. This code will be all 1's from the LSB up to the value of the k-th bit, D_k, and all 0's above it. The point at

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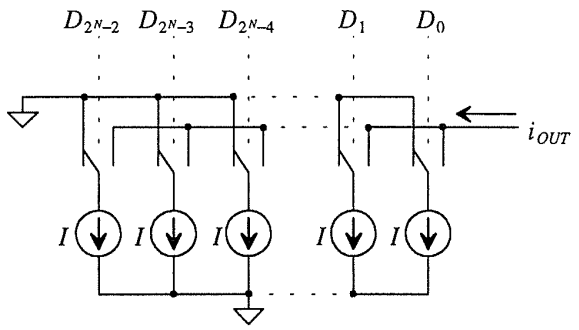


Figure 29.9 A generic current steering DAC.

which the input code changes from all 1's to all 0's "floats" up or down and resembles the action of a thermometer, hence the name. Typically, a thermometer encoder is used to convert binary input data into a thermometer code.

Another current steering architecture is seen in Fig. 29.10. This architecture uses binary-weighted current sources, thus requiring only N current sources of various sizes versus $2^N - 1$ sources in the previous example. Since the current sources are binary weighted, the input code can be a simple binary number with no thermometer encoder needed.

One advantage of the current steering DACs is the high-current drive inherent in the system. Since no output buffers are necessary to drive resistive loads, these DACs typically are used in high-speed applications. Traditionally, high-speed current steering DACs have been fabricated using bipolar technology. However, the ability to generate matched current mirrors makes CMOS an enticing alternative. Of course, the precision needed to generate high resolutions is dependent on how well the current sources can be matched or the degree to which they can be made binary weighted. For example, if a 13-bit DAC was designed using these architectures, there would have to be 8,191 current sources resident on the chip - not an insignificant amount. For the

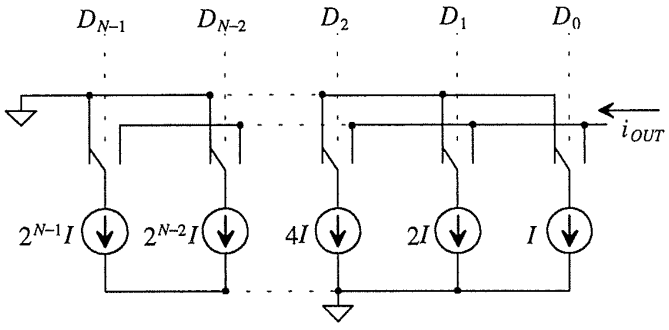


Figure 29.10 A current steering DAC using binary-weighted current sources.

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binary-weighted sources, only 13 current sources would be needed. Yet the size of the largest current source would have to be 4096 or 2^{N-1} times larger than the smallest. Even if the unit current, I, was chosen to be 5 μA, the largest current source would be 20.48 mA!

Another problem associated with this architecture is the error due to the switching. Since the current sources are in parallel, if one of the current sources is switched off and another is switched on, a "glitch" could occur in the output if the timing was such that both of them were on or both were off for an instant. While this may not seem significant, if the converter is switching from 0111111 to 10000000, the output will spike toward ground and then back to the correct value if all the switches turn off for an instant. If the DAC is driving a resistive load and the output current is converted to a voltage, a substantial voltage spike will occur at the output.

Example 29.4

Construct a table showing the thermometer code necessary to generate the output shown in Fig. 29.11a for a 3-bit current steering DAC using unit current sources.

The thermometer code can be seen in Fig. 29.11b. When the code is all zeros, the output is zero volts. Therefore, only 7 bits are needed to represent the 2^N or 8 states of a 3-bit DAC. Note how the interface between all 1's and all 0's actually resembles the output signal itself. ■

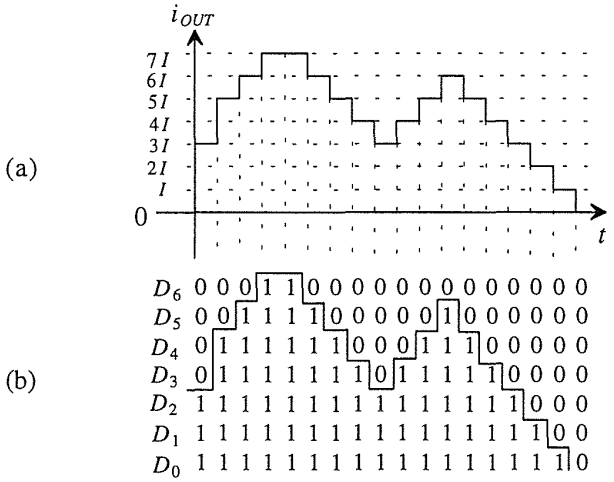


Figure 29.11 (a) Output of a 3-bit current steering DAC and (b) the thermometer code input.

Mismatch Errors Related to Current Steering DACs

Analysis of the mismatch associated with the current sources is similar to the resistor string analysis. It is assumed that each current source in Fig. 29.9 is

$$I_k = I + \Delta I_k \text{ for } k = 1, 2, 3, ..., 2^N - 1 \qquad (29.18)$$

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where I is the ideal value of the current and ΔI_k is the error due to mismatch. If it is again assumed that the ΔI_K terms sum to zero and that one-half of the current sources contain the maximum positive mismatch, ΔI_{max}, and the other half contains the maximum negative mismatch, $-\Delta I_{max}$, (or vice versa), then the worst-case condition will occur at midscale with the actual output current being

$$I_{out} = \sum_{k=1}^{2^{N-1}} (I + \Delta I_k) = 2^{N-1} \cdot I + 2^{N-1} \cdot |\Delta I|_{max} = I_{out,ideal} + 2^{N-1} \cdot |\Delta I|_{max} \quad (29.19)$$

Since the INL is simply the actual output current minus the ideal, the worst-case INL will be

$$|INL|_{max} = 2^{N-1} \cdot |\Delta I|_{max,INL} \quad (29.20)$$

The term, $|\Delta I|_{max,INL}$ represents the maximum current source mismatch error that will keep the INL less than ½ LSB. Each current source represents the value of 1 LSB; therefore, ½ LSB is equal to 0.5 I. Since the maximum INL should correspond to the ½ LSB, equating Eq. (29.20) to ½ I results in the value for $|\Delta I|_{max,INL}$,

$$|\Delta I|_{max,INL} = \frac{0.5I}{2^{N-1}} = \frac{I}{2^N} \quad (29.21)$$

Equation (29.21) illustrates the difficulty of using this architecture at high resolutions. If the value of I is set to be 5 μA, and the N is desired to be 12 bits, then the value of $\Delta I_{max,INL}$ becomes

$$|\Delta I|_{max,INL} = \frac{5 \times 10^{-6}}{2^{12}} = 1.221 \text{ nA!} \quad (29.22)$$

which means that each of the 5 μA current sources must lie between the bounds of,

$$4.99878\ \mu A \le I_k \le 5.001221\ \mu A \quad (29.23)$$

to achieve a worst-case INL, which is within ½ LSB error.

The DNL is easily obtained since the step height in the transfer curve is equivalent to the value of the ideal current source, I. The maximum difference between any two adjacent values of output current will be simply the value of the single source, I_k, which contains the largest mismatch error for which the DNL will be less than ½ LSB, $|\Delta I|_{max,DNL}$:

$$I_{out(x)} - I_{out(x-1)} = I_k + |\Delta I|_{max,DNL} \quad (29.24)$$

Therefore, the DNL is simply

$$|DNL|_{max} = I_k + |\Delta I|_{max,DNL} - I_k = |\Delta I|_{max,DNL} \quad (29.25)$$

Equating the maximum DNL to the value of ½ LSB,

$$|\Delta I|_{max,DNL} = \tfrac{1}{2}\, LSB = \tfrac{1}{2} I \quad (29.26)$$

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which is much easier to attain than the requirement for the INL.

For the binary-weighted current sources seen in Fig. 29.10, a slightly different analysis is needed to determine the requirements for INL and DNL. In this case, it will be assumed that the current source corresponding to the MSB (D_{N-1}) has a maximum positive mismatch error value and the remainder of the bits (D_0 to D_{N-2}) contain a maximum negative mismatch error, so that the sum of all the errors equals zero. Therefore, the INL is

$$|INL|_{max} = 2^{N-1}(I + |\Delta I|_{max,INL}) - 2^{N-1} \cdot I = 2^{N-1} \cdot |\Delta I|_{max,INL} \qquad (29.27)$$

which is equivalent to the value of the current steering array in Fig. 29.9.

The DNL is slightly different because of the binary weighting of the current sources. One cannot add a single current source with each incremental increase in the digital input code. However, the worst-case condition for binary-weighted arrays tends to occur at midscale when the code transitions from 011111....111 to 100000....000. The worst-case DNL at this point is

$$DNL_{max} = \left[2^{N-1} \cdot (I + |\Delta I|_{max,DNL}) - \sum_{k=1}^{N-1} 2^{k-1} \cdot (I - |\Delta I|_{max,DNL}) \right] - I \qquad (29.28)$$

which can be written as

$$DNL_{max} = 2^{N-1} \cdot (I + |\Delta I|_{max,DNL}) - (2^{N-1} - 1) \cdot (I - |\Delta I|_{max,DNL}) - I = (2^N - 1) \cdot |\Delta I|_{max,DNL} \qquad (29.29)$$

and setting this value equal to ½ LSB and solving for ΔI_{max},

$$|\Delta I|_{max,DNL} = \frac{0.5I}{2^N - 1} = \frac{I}{2^{N+1} - 2} \qquad (29.30)$$

Therefore, the DNL requirements for the binary-weighted current source array is more stringent than the INL requirements.

One interesting issue regarding the previous derivation is that the challenging accuracy requirements in Eq. (29.30) are placed only on the MSB current source. For each of the remaining binary-weighted sources, the DNL requirements become more relaxed. This is simply because the size of the MSB source is equivalent to all the other sources combined, and so its value plays the most important role in the DAC's accuracy.

Example 29.5

Determine the tolerance of the MSB current source on a 10-bit binary-weighted current source array with a unit current source of 1 μA, which will result in a worst-case DNL that is less than ½ LSB.

Since Eq. (29.30) defines the maximum $|\Delta I|$ needed to keep the DNL less than ½ LSB, we must first use this equation,

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$$|\Delta I|_{max,DNL} = \frac{1 \times 10^{-6}}{2^{11} - 2} = 0.4888 \text{ nA}$$

For a 10-bit DAC, the MSB current source will have a value that is 2^9 times larger than the unit current source, or 0.512 mA. Therefore, the range of values for which this array will have a DNL that is less than ½ LSB is

$$0.51199995 \text{ mA} \leq I_{MSB} \leq 0.5120004888 \text{ mA} \blacksquare$$

29.1.5 Charge Scaling DACs

A very popular DAC architecture used in CMOS technology is the charge scaling DAC. Shown in Fig. 29.12a, a parallel array of binary-weighted capacitors, totaling $2^N C$, is connected to an op-amp. The value, C, is a unit capacitance of any value. After initially being discharged, the digital signal switches each capacitor to either V_{REF} or ground, causing the output voltage, v_{OUT}, to be a function of the voltage division between the capacitors.

Since the capacitor array totals $2^N C$, if the MSB is high and the remaining bits are low, then a voltage divider occurs between the MSB capacitor and the rest of the array. The analog output voltage, v_{OUT}, becomes

$$v_{OUT} = V_{REF} \cdot \frac{2^{N-1}C}{(2^{N-1} + 2^{N-2} + 2^{N-3} + \ldots + 4 + 2 + 1 + 1)C} = V_{REF} \cdot \frac{2^{N-1}C}{2^N C} = \frac{V_{REF}}{2} \tag{29.31}$$

which confirms the fact that the MSB changes the output of a DAC by ½ V_{REF}. Figure 29.12b shows the equivalent circuit under this condition. The ratio between v_{OUT} and V_{REF} due to each capacitor can be generalized to

$$v_{OUT} = \frac{2^k C}{2^N C} \cdot V_{REF} = 2^{k-N} \cdot V_{REF} \tag{29.32}$$

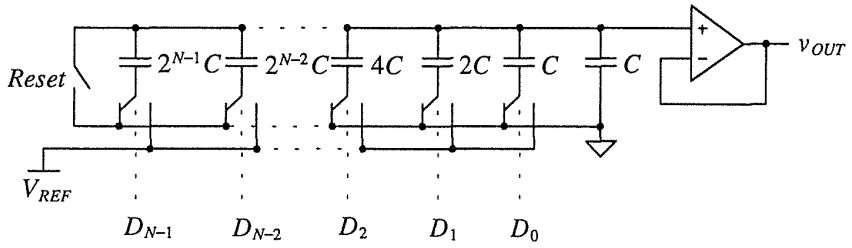
where it is assumed that the k-th bit, D_k, is 1 and all other bits are zero. Superposition can then be used to find the value of v_{OUT} for any digital input word by

$$v_{OUT} = \sum_{k=0}^{N-1} D_k 2^{k-N} \cdot V_{REF} \tag{29.33}$$

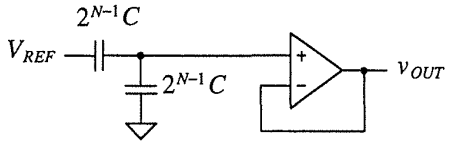
One limitation of this architecture as shown in Fig. 29.12a is the existence of a parasitic capacitance at the top plate of the capacitor array due to the op-amp. This will prohibit its use as a high-resolution data converter. A better implementation would include the use of a parasitic insensitive, switched-capacitor integrator (see Ch. 27) as the driving circuit. However, the capacitor array itself is the critical component of this data converter and is used in charge redistribution ADCs (Sec. 29.2.5).

The INL and DNL calculations for the binary-weighted capacitor array are identical to those for the binary-weighted current source array, except the unit current source, I, and its corresponding error term, ΔI, are replaced by C and ΔC in Eqs. (29.27) – (29.30).

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(a)



(b)

Figure 29.12 (a) A charge scaling DAC, (b) the equivalent circuit with the MSB = 1, and all other bits set to zero.

Example 29.6

Design a 3-bit charge scaling DAC and find the value of the output voltage for $D_2D_1D_0 = 010$ and 101. Assume that $V_{REF} = 5$ V and $C = 0.5$ pF.

The 3-bit DAC can be seen in Fig. 29.13a. The equivalent circuits for the capacitor array can be seen in Fig. 29.13b and c. The value of the output voltage can be calculated by either using Eq. (29.32) or the equivalent circuits and performing the voltage division. For $D = 010$, the equivalent circuit in Fig. 29.13b yields

$$v_{OUT} = V_{REF} \cdot (\frac{1}{4}) = 1.25 \text{ V}$$

Using Eq. (29.33) to calculate v_{OUT} for $D = 101$ yields

$$v_{OUT} = \sum_{k=0}^{N-1} D_k 2^{k-N} \cdot V_{REF} = [1 \cdot (2^{-3}) + 0 \cdot (2^{-2}) + 1 \cdot (2^{-1})] \cdot 5 = \left(\frac{1}{8} + \frac{1}{2}\right) \cdot 5 = 3.125 \text{ V}$$

which is the result expected. ■

Layout Considerations for a Binary-Weighted Capacitor Array

One problem with this converter is the need for precisely ratioed capacitors. As the number of bits increase, the ratio of the MSB capacitor to the LSB capacitor becomes more difficult to control. For example, Fig. 29.14a shows a 3-bit binary capacitor array

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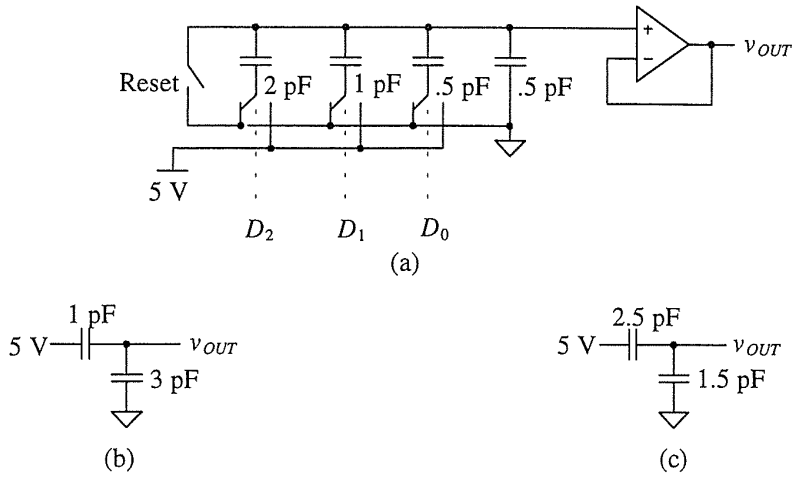


Figure 29.13 (a) A 3-bit charge scaling DAC used in Ex. 29.6 and the equivalent circuits inputs equal to (b) 010 (c) 101.

using three capacitors. When the capacitor is fabricated, *undercutting* of the mask [2, 3] will cause an error in the ratio of the capacitors, causing potentially large DNL and INL errors as N increases.

One solution to this problem is seen in Fig. 20.14b. Here, each capacitor in the array is constructed out of a unit capacitance. Undercutting then affects all the capacitors in the same way, and the ratio between capacitors is maintained. Another problem that affects even this layout strategy is a nonuniform oxide growth. Gradient errors will result in errors in the ratios of the capacitors. Figure 29.14c illustrates another layout strategy that overcomes this issue. The capacitors are laid out in a common-centroid scheme so that the first-order oxide errors average out to be the same for each capacitor.

The Split Array

The charge scaling architecture is very popular among CMOS designers because of its simplicity and relatively good accuracy. Although a linear capacitor is required using poly2, high resolutions in the 10 to 12-bit range can be achieved. Passive, double-poly capacitors have good matching accuracy as well. However, as the resolution increases, the size of the MSB capacitor becomes a major concern. For example if the unit capacitor, C, was chosen to be 0.5 pF, and a 16-bit DAC was to be designed, the MSB capacitor would need to be

$$C_{MSB} = 2^{N-1} \cdot 0.5 \text{ pF} = 16.384 \text{ nF} \tag{29.34}$$

Based on our 2 μm process parameters, the capacitance between poly1 and poly2 is nominally 500 aF/μm^2. Therefore, the area required for this one capacitor is over 30 million square microns!

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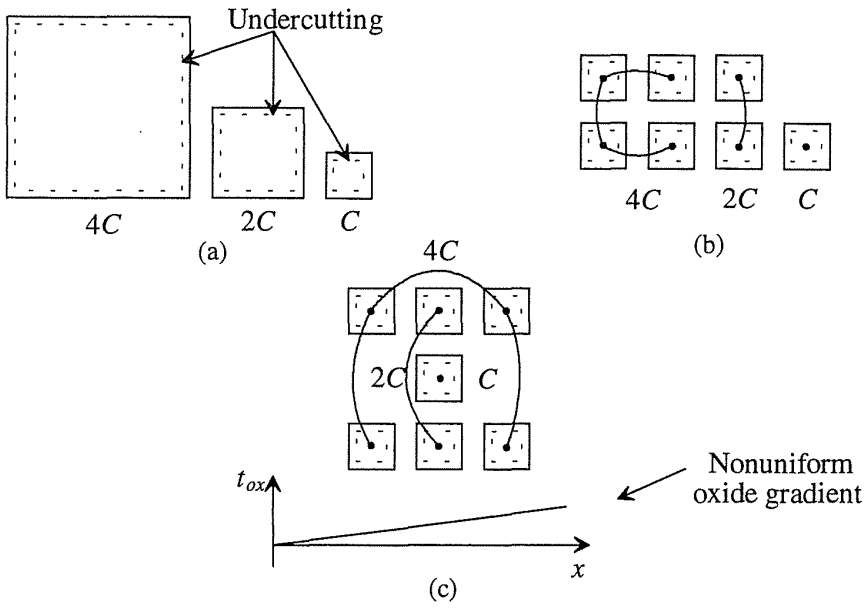


Figure 29.14 Layout of a binary-weighted capacitor array using (a) single capacitors (b) unit capacitors to minimize undercutting effect, and (c) common-centroid to minimize oxide gradients.

One method to reduce the size of the capacitors is to use a split array. A 6-bit example of the array is pictured in Fig. 29.15. This architecture [1] is slightly different from the charge scaling DAC pictured in Fig. 29.13 in that the output is taken off a different node and an additional attenuation capacitor is used to separate the array into a LSB array and a MSB array. Note that the LSB, D_0, now correponds to the leftmost switch and that the MSB, D_5, corresponds to the rightmost switch. The value of the attenuation capacitor can be found by

$$C_{atten} = \frac{sum\ of\ the\ LSB\ array\ capacitors}{sum\ of\ the\ MSB\ array\ capacitors} \cdot C \tag{29.35}$$

where the sum of the MSB array is equal to the sum of LSB capacitor array minus C. The value of the attenuation capacitor should be such that the series combination of the attenuation capacitor and the LSB array, assuming all bits are zero, is equal to *C*.

Example 29.7

Using the 6-bit charge scaling DAC shown in Fig. 29.15, (a) show that the output voltage will be $\frac{1}{2} \cdot V_{REF}$ if (a) $D_5D_4D_3D_2D_1D_0 = 100000$ and (b) the output will be $\frac{1}{64} \cdot V_{REF}$ if $D_5D_4D_3D_2D_1D_0 = 000001$.

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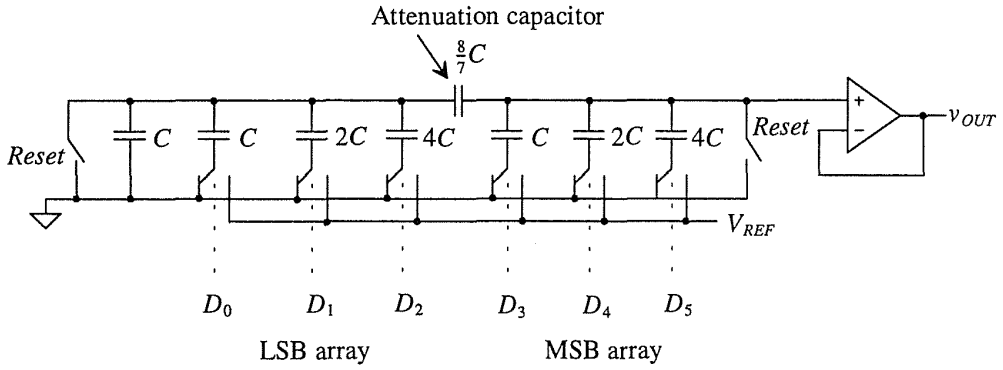


Figure 29.15 A charge scaling DAC using a split array.

(a) If $D_5 = 1$ and the remaining bits are all zero, then the equivalent circuit for the DAC can be represented by Fig. 29.16a. The expression for the output voltage then becomes

$$v_{OUT} = \frac{4}{\left(\frac{8}{7}\|8\right)+3+4} \cdot V_{REF} = \frac{1}{2} \cdot V_{REF}$$

(b) For the second case, the equivalent circuit can be seen in Fig. 29.16b. The intermediate node voltage, V_A, is simply the voltage division between C and the remainder of the circuit, or

$$V_A = V_{REF} \cdot \frac{1}{\left(7+\frac{\frac{8}{7}\cdot 7}{\frac{8}{7}+7}\right)+1} = \frac{1}{8+\frac{56}{57}} \cdot V_{REF} \tag{29.36}$$

The output voltage can be written as

$$v_{OUT} = V_A \cdot \frac{\frac{8}{7}}{\frac{8}{7}+7} = \frac{8}{57} \cdot V_A \tag{29.37}$$

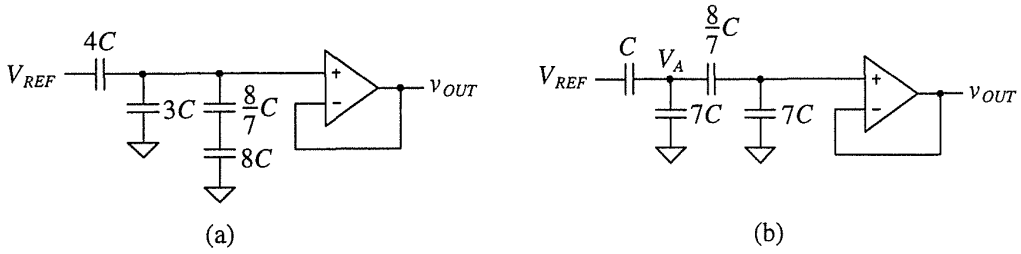


Figure 29.16 Equivalent circuits for Example 29.7.

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Plugging Eq. (29.36) into Eq. (29.37) yields

$$v_{OUT} = V_{REF} \cdot \frac{8}{(8 \cdot 57) + 56} = \frac{V_{REF}}{64} \tag{29.38}$$

which is the desired result. ■

29.1.6 Cyclic DAC

The cyclic DAC uses only a couple of simple components to perform the conversion. As seen in Fig. 29.17, a summer adds V_{REF} or ground to the feedback signal depending on the input bits. An amplifier with a gain of 0.5 feeds the output voltage back to the summer such that the output at the end of each cycle is dependent on the value of the output during the cycle before. Notice that the input bits must be read in a serial fashion. Therefore, the conversion is performed one bit at a time, resulting in N cycles required for each conversion. The voltage output at the end of the n-th cycle of the conversion can be written as

$$v_{OUT}(n) = \left(D_{n-1} \cdot V_{REF} + \frac{1}{2} \cdot v_A(n-1) \right) \cdot \frac{1}{2} \tag{29.39}$$

with a condition such that the output of the S/H is initially zero [$v_A(0) = 0$ V].

The accuracy of this converter is dependent on several factors. The gain of the 0.5 amplifier needs to be highly accurate (to within the accuracy of the DAC) and is usually generated with passive capacitors. Similiarly, the summer and the sample-and-hold also need to be N-bit accurate. Limitations of the converter due to these fundamental building blocks will be discussed in more detail in Sec. 29.3. Since this converter uses a pseudo-"sampled-data" approach, implementing this architecture using switched capacitors is relatively easy.

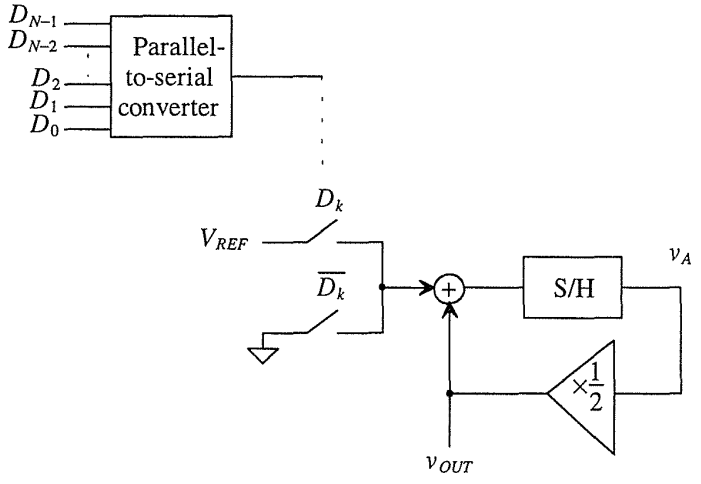


Figure 29.17 A cyclic digital-to-analog converter.

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Example 29.8

Show the value of the output voltage at the end of each cycle for a 6-bit cyclic DAC with an input value of $D_5D_4D_3D_2D_1D_0 = 110101$. Assume that $V_{REF} = 5$ V.

We can predict the value of the output based on our previous experience with DACs. The digital input 110101 corresponds to 53_{10}. Therefore, the output voltage due to this input should be

$$v_{OUT} = \frac{53}{64} \cdot V_{REF} = 4.140625 \text{ V}$$

Now examine the cyclic converter in Fig. 29.17. By performing a 6-bit conversion and using Eq. (29.39), the outputs occurring at the end of each cycle can be seen in Fig. 29.18.

The output voltage at the end of the sixth cycle is precisely what was predicted. Note that had this been a 3-bit conversion, the output voltage at the end of cycle 3 would correspond to the value of the 3-bit DACs studied previously with an input of 101. ■

Cycle Number, n	D_{n-1}	$v_A(n\text{-}1)$	$v_{OUT}(n)$
1	1	0	½ (5 + 0) = 2.5 V
2	0	5	½ (0 + 2.5) = 1.25 V
3	1	2.5	½ (5 +1.25) = 3.125 V
4	0	6.25	½ (0 + 3.125) = 1.5625 V
5	1	3.125	½ (5 + 1.5625) = 3.28125 V
6	1	6.5625	½ (5 + 3.28125) = 4.140625 V

Figure 29.18 Output from the 6-bit cyclic DAC used in Ex. 29.8.

29.1.7 Pipeline DAC

The cyclic converter presented in the last section takes N clock cycles per N-bit conversion. Instead of recycling the output back to the input each time, we could extend the cyclic converter to N stages, where each stage performs one bit of the conversion. This extension of the cyclic converter is called a *pipeline* DAC and is seen in Fig. 29.19. Here, the signal is passed down the "pipeline," and as each stage works on one conversion, the previous stage can begin processing another. Therefore, an initial N clock cycle delay is experienced as the signal makes its way down the pipeline the very first time. However, after the N clock cycle delay, a conversion takes place at every clock cycle.

Besides the N clock cycle delay, this architecture can be very fast. However, the amplifier gains must be very accurate to produce high resolutions. Also, this

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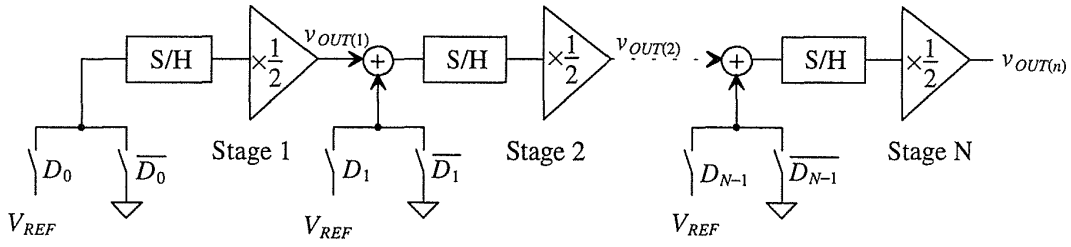


Figure 29.19 A pipeline digital-to-analog converter.

architecture uses N times more circuitry than that of the cyclic, so there is a tradeoff between speed and chip area. The output voltage of the n-th stage in the converter can be written as

$$v_{OUT(n)} = [D_{n-1} \cdot V_{REF} + v_{OUT(n-1)}] \cdot \frac{1}{2} \tag{29.40}$$

The operation of each stage in the pipeline can be summarized as follows: if the input bit is a 1, add V_{REF} to the output of the previous stage, divide by two, and pass the value to the next stage. If the input bit is a 0, simply divide the output of the previous stage by two and pass along the resulting value.

Example 29.9

Find the output voltage for a 3-bit pipeline DAC for three cases: $D_A = 001$, $D_B = 110$, and $D_C = 101$ and show that the conversion time to perform all three conversions is five clock cycles using the pipeline approach. Assume that $V_{REF} = 5$ V.

The first stage will operate on the LSBs of each word; the second stage will operate on the middle bits; and the last stage, the MSBs. Based on the pipeline strategy, once the LSB of the first input word is performed and passed on, the LSB of the second word, D_B, can begin its conversion. Similarly, once the LSB of the second stage is completed and passed on, the LSB of the third word, D_C, can begin. The conversion cycle for all three input words will produce the output shown in Fig. 29.20. The items that are in bold are associated with the first input word, D_A, whereas the italicized numbers represent the values associated with D_B and the underlined items, D_C.

The first output of the DAC is not valid until the end of the third clock cycle and should look familiar as the 3-bit DAC output for an input word of $D_2D_1D_0 = 001$. The following two clock cycles that produce outputs for $D_2D_1D_0$ equal 110 and 101, respectively. ■

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Clock Cycle	$v_{OUT(1)}$	$v_{OUT(2)}$	$v_{OUT(3)}$	D_0	D_1	D_2
1	**2.5**	0	0	**1**	0	0
2	*0*	**1.25**	0	*0*	**0**	0
3	2.5	*2.5*	**0.625**	1	*1*	**0**
4		1.25	*3.75*		0	*1*
5			3.125			1

Figure 29.20 Output from the 3-bit pipeline DAC used in Example 29.9.

29.2 ADC Architectures

A survey of the field of current A/D converter research reveals that a majority of effort has been directed to four different types of architectures: pipeline, flash-type, successive approximation, and oversampled ADCs. Each has benefits that are unique to that architecture and span the spectrum of high speed and resolution.

Since the ADC has a continuous, infinite-valued signal as its input, the important analog points on the transfer curve x-axis for an ADC are the ones that correspond to changes in the digital output word. These input transitions determine the amount of INL and DNL associated with the converter.

29.2.1 Flash

Flash or parallel converters have the highest speed of any type of ADC. As seen in Fig. 29.21, they utilize one comparator per quantization level ($2^N - 1$) and 2^N resistors (a resistor string DAC). The reference voltage is divided into 2^N values, each of which is fed into a comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators. A thermometer code will exhibit all zeros for each resistor level if the value of v_{IN} is less than the value on the resistor string, and ones if v_{IN} is greater than or equal to voltage on the resistor string. A simple $2^N - 1$:N digital thermometer decoder circuit converts the compared data into an N-bit digital word. The obvious advantage of this converter is the speed with which one conversion can take place. Each clock pulse generates an output digital word. The advantage of having high speed, however, is counterbalanced by the doubling of area with each bit of increased resolution. For example, an 8-bit converter requires 255 comparators, but a 9-bit ADC requires 511! Flash converters have traditionally been limited to 8-bit resolution with conversion speeds of 10 – 40 Ms/s using CMOS technology [4–6]. The disadvantages of the Flash ADC are the area and power requirements of the $2^N - 1$ comparators. The speed is limited by the switching of the comparators and the digital logic.

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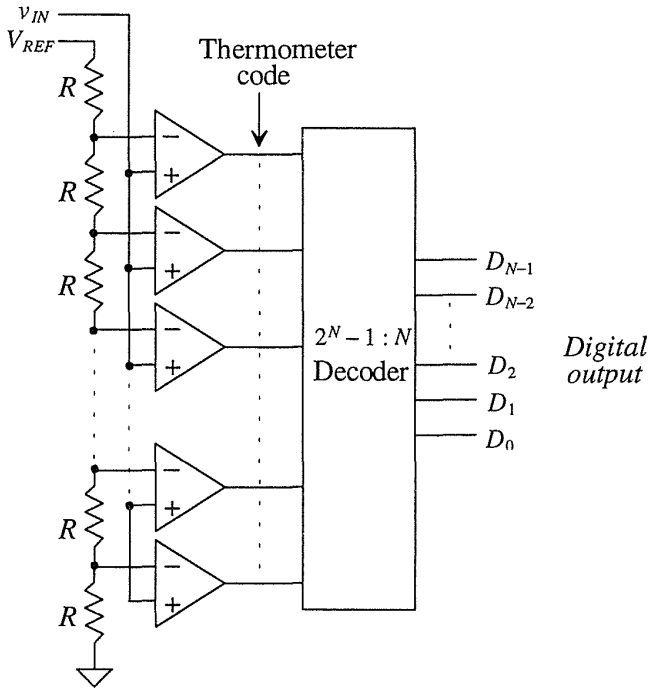


Figure 29.21 Block diagram of a Flash ADC.

Example 29.10

Design a 3-bit Flash converter, listing the values of the voltages at each resistor tap, and draw the transfer curve for v_{IN} = 0 to 5 V. Assume V_{REF} = 5 V. Construct a table listing the values of the thermometer code and the output of the decoder for v_{IN} = 1.5, 3.0, and 4.5 V.

The 3-bit converter can be seen in Fig. 29.22. Since the values of all the resistors are equal, the voltage of each resistor tap, V_i, will be $V_i = V_{REF}\left(\frac{i}{8}\right)$ where i is the number of the resistor in the string for i = 1 to 7. Obviously, V_1 = 0.625 V, V_2 = 1.25 V, V_3 = 1.875 V, V_4 = 2.5 V, V_5 = 3.125, V_6 = 3.75 V, V_7 = 4.375 V. Therefore, when v_{IN} first becomes equal or greater than each of these values, a transition will occur in the transfer curve. The transfer curve can be seen in Fig. 29.23 and should look similar to those seen in Ch. 28. The quantization levels and their corresponding thermometer codes can be summarized as seen in Fig. 29.24.

The transfer curve of this ADC corresponds to the ADC with quantization error centered about + ½ LSB, as discussed in Ch. 28 (Fig. 28.20). To shift the curve by ½ LSB so that the code transitions occur around the LSB values and the

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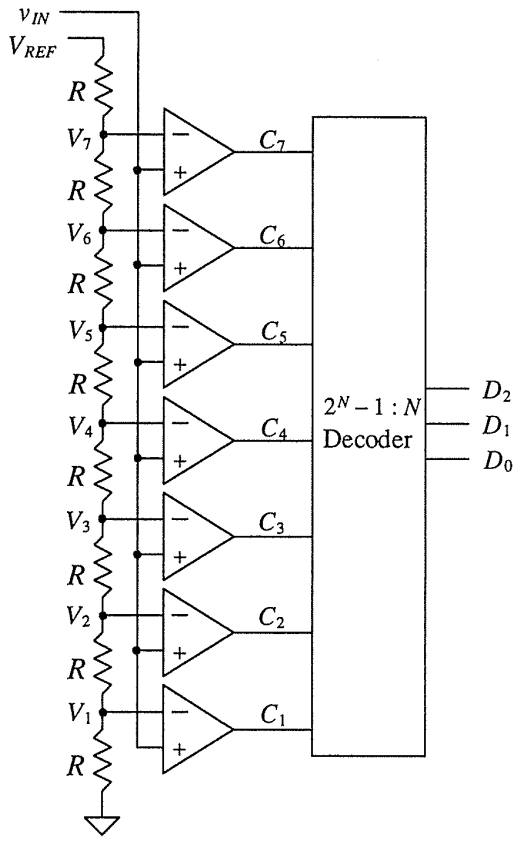


Figure 29.22 Three-bit Flash A/D converter to be used in Ex. 29.10.

quantization error is centered around 0 LSB, the value of the last resistor in the string would have to be adjusted to $\frac{R}{2}$ and the value of the MSB resistor, closest to the reference voltage, would have to be made $1.5R$. Then the first code transition would occur at v_{IN} = 0.3125 V, and the last code transition would occur at v_{IN} = 4.0625 and so the transfer curve would exactly match that of Fig. 28.20.

Based on Fig. 29.24, when v_{IN} = 1.5 V, only comparators C_1 and C_2 will have outputs of 1, since both V_1 and V_2 are less than 1.5 V. The remaining comparator outputs will be 0 since V_3 through V_8 will be greater than 1.5 V, thus generating the thermometer code, 0000011. The encoder must then convert this into a 3-bit digital word, resulting in 010. The same reasoning can be used to construct the data shown in Fig. 29.25. It should be obvious that if the polarity of the comparators were reversed, the thermometer code would be inverted. ■

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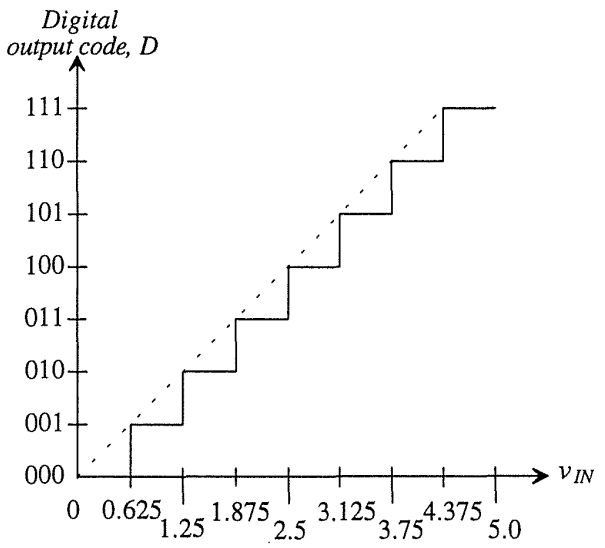


Figure 29.23 Transfer curve for the 3-bit Flash converter in Example 29.10.

v_{IN}	$C_7C_6C_5C_4C_3C_2C_1$	$D_2D_1D_0$
$0 \le v_{IN} < 0.625$ V	0000000	000
0.625 V $\le v_{IN} < 1.25$ V	0000001	001
1.25 V $\le v_{IN} < 1.875$ V	0000011	010
1.875 V $\le v_{IN} < 2.5$ V	0000111	011
2.5 V $\le v_{IN} < 3.125$ V	0001111	100
3.125 V $\le v_{IN} < 3.75$ V	0011111	101
3.75 V $\le v_{IN} < 4.375$ V	0111111	110
$4.375 \le v_{IN}$	1111111	111

Figure 29.24 Code transitions for the Flash ADC used in Ex. 29.10.

Accuracy Issues for the Flash ADC

Accuracy is dependent on the matching of the resistor string and the input offset voltage of the comparators. From Sec. 26.1, we know that an ideal comparator should switch at the point at which the two inputs, v_+ and v_-, are the same potential. However, the offset voltage V_{os}, prohibits this from occurring as the comparator output switches state as follows:

$$v_o = 1 \qquad \text{when } v_+ \ge v_- + V_{os} \tag{29.41}$$

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v_{IN}	$C_7C_6C_5C_4C_3C_2C_1$	$D_2D_1D_0$
1.5	0000011	010
3.0	0001111	100
4.5	1111111	111

Figure 29.25 Output for the Flash ADC used in Ex. 29.10.

$$v_o = 0 \qquad \text{when } v_+ < v_- + V_{os} \tag{29.42}$$

The resistor string DAC was analyzed and presented in Sec. 29.1.2; the voltage on the i-th tap of the resistor string was found to be

$$V_i = V_{i,ideal} + \frac{V_{REF}}{2^N} \cdot \sum_{k=1}^{i} \frac{\Delta R_k}{R} \tag{29.43}$$

where $V_{i,ideal}$ is the voltage at the i-th tap if all the resistors had an ideal value of R. The term, ΔR_k, is the value of the resistance error (difference from ideal) due to the mismatch. Note that for the resistor string DAC, the sum of the mismatch terms plays an important factor in the overall voltage at each tap.

The switching point for the i-th comparator, $V_{sw,i}$, then becomes

$$V_{sw,i} = V_i + V_{os,i} \tag{29.44}$$

where $V_{os,i}$ is the input referred offset voltage of the i-th comparator. The INL for the converter can then be described as

$$INL = V_{sw,i} - V_{sw,ideal} = V_{sw,i} - V_{i,ideal} \tag{29.45}$$

which becomes

$$INL = \frac{V_{REF}}{2^N} \cdot \sum_{k=1}^{i} \frac{\Delta R_k}{R} + V_{os,i} \tag{29.46}$$

The worst-case INL will occur at the middle of the string ($i = 2^{N-1}$) as described in Sec. 29.1.2 and Eq. (29.10). Including the offset voltage, the maximum INL will be

$$|INL|_{max} = \frac{V_{REF}}{2^N} \cdot \sum_{k=1}^{2^{N-1}} \frac{\Delta R_k}{R} + |V_{os,i}|_{max} = V_{REF} \cdot \frac{2^{N-1}}{2^N R} \cdot |\Delta R_k|_{max} + |V_{os,i}|_{max} \tag{29.47}$$

which can be rewritten as

$$|INL|_{max} = \frac{V_{REF}}{2} \cdot \left|\frac{\Delta R_k}{R}\right|_{max} + |V_{os,i}|_{max} \tag{29.48}$$

where it is assumed that the maximum positive mismatch occurs in all the resistors in the lower half of the string and the maximum negative mismatch occurs in the upper

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half (or vice versa) and that the comparator at the i-th tap contains the maximum offset voltage, $|V_{os,i}|_{max}$. Notice that the offset contributes directly to the maximum value for the INL. This explains another limitation to using Flash converters at high resolutions. The offset voltage alone can make the INL greater than ½ LSB.

Example 29.11

If a 10-bit Flash converter is designed, determine the maximum offset voltage of the comparators which will make the INL less than ½ LSB. Assume that the resistor string is perfectly matched and $V_{REF} = 5$ V.

Equation (29.48) requires that the offset voltage be equal to ½ LSB. Therefore,

$$|V_{os}|_{max} = \frac{5}{2^{11}} = 2.44 \text{ mV} \quad \blacksquare$$

The DNL calculation for the Flash converter is also attained using the analysis first presented in Sec. 29.1.2. Using the definition of DNL,

$$DNL = V_{sw,i} - V_{sw,i-1} - 1 \text{ LSB (in volts)} \tag{29.49}$$

Plugging in Eq. (29.44),

$$DNL = V_i + V_{os,i} - V_{i-1} - V_{os,i-1} - 1 \text{ LSB} \tag{29.50}$$

which can be written by using Eq. (29.6) as

$$DNL = V_{i,ideal} - V_{i-1,ideal} + \frac{V_{REF}}{2^N} \cdot \frac{\Delta R_i}{R} + V_{os,i} - V_{os,i-1} - 1 \ LSB \tag{29.51}$$

which becomes

$$DNL = \frac{V_{REF}}{2^N} \cdot \frac{\Delta R_i}{R} + V_{os,i} - V_{os,i-1} \tag{29.52}$$

The maximum DNL will occur assuming ΔR_i is at its maximum, $V_{os,i}$ is at its maximum positive value, and $V_{os,i-1}$ is at its maximum negative voltage. Thus,

$$|DNL|_{max} = \frac{V_{REF}}{2^N} \cdot \left|\frac{\Delta R_i}{R}\right|_{max} + 2|V_{os}|_{max} \tag{29.53}$$

which assumes that the maximum offset voltage in the positive and negative directions are symmetrical. Therefore, both resistor string matching and offset voltage affect the DNL of the converter.

29.2.2 The Two-Step Flash ADC

Another type of Flash converter is called the two-step Flash converter or a parallel, feed-forward ADC [7–10]. The basic block diagram of a two-step converter is seen in Fig. 29.26. The converter is separated into two complete Flash ADCs with feed-forward circuitry. The first converter generates a rough estimate of the value of the input, and the second converter performs a fine conversion. The advantages of this architecture are that the number of comparators is greatly reduced from that of the Flash converter -

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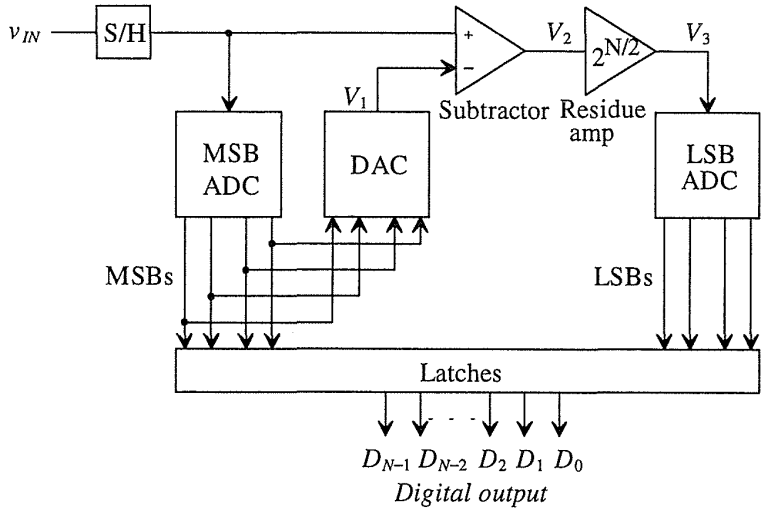


Figure 29.26 Block diagram of a two-step Flash ADC.

from $2^N - 1$ comparators to $2(2^{N/2} - 1)$ comparators. For example, an 8-bit Flash converter requires 255 comparators, while the two-step Flash requires only 30. The tradeoff is that the conversion process takes two steps instead of one, with the speed limited by the bandwidth and settling time required by the residue amplifier and the summer. The conversion process is as follows:

1. After the input is sampled, the most significant bits (MSBs) are converted by the first Flash ADC.
2. The result is then converted back to an analog voltage with the DAC and subtracted with the original input.
3. The result of the subtraction, known as the *residue*, is then multiplied by $2^{N/2}$ and input into the second ADC. The multiplication not only allows the two ADCs to be identical, but also increases the quantum level of the signal input into the second ADC.
4. The second ADC produces the least significant bits through a Flash conversion.

Some architectures use the same set of comparators in order to perform both steps. The multiplication mentioned in step 3 can be eliminated if the second converter is designed to handle very small input signals. The accuracy of the two-step ADC is dependent primarily on the linearity of the first ADC.

Figure 29.27 illustrates the two-step nature of the converter. A more intuitive approach can be explained with this picture. The first conversion identifies the segment in which the analog voltage resides. This is also known as a *coarse conversion* of the MSBs. The results of the coarse conversion are then multiplied by $2^{N/2}$ so that the segment within which V_{IN} resides will be scaled to the same reference as the first

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conversion. The second conversion is known as the *fine conversion* and will generate the final LSBs using the same Flash approach. One can see why the accuracy of the first converter is so important. If the input value is close to the boundary between two coarse segments and the first ADC is unable to choose the correct coarse segment, then the second conversion will be completely erroneous. The following example further illustrates the two-step algorithm.

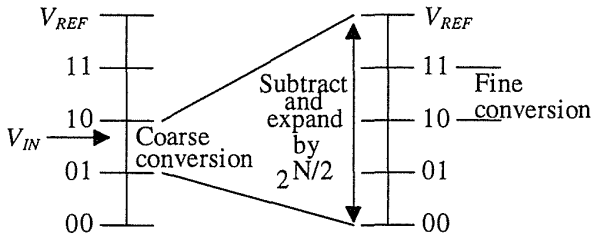


Figure 29.27 Coarse and fine conversions using a two-step ADC.

Example 29.12

Assume that the two-step ADC shown in Fig. 29.26 has four bits of resolution. Make a table listing the MSBs, V_1, V_2, V_3, and the LSBs for V_{IN} = 2, 4, 9, and 15 V assuming that V_{REF} = 16 V.

Since V_{REF} was conveniently made 16 V, each LSB will be 1 V. If V_{IN} = 2 V, the output of the first 2-bit Flash converter will be 00 since V_{REF} = 16 V and each resistor drops 4 V. The output of the 2-bit DAC, V_1, will therefore be 0, resulting in V_2 = 2 V. The multiplication of V_2 by the 4 results in V_3 = 8 V. Remember that each 2-bit Flash converter resembles that of Fig. 29.21. The thermometer code from the second Flash converter will be 0011, which results in 10 as the LSBs. The other values can be calculated as seen in Fig. 29.28. ■

V_{IN}	D_3D_2 (MSBs)	V_1	V_2	V_3	D_1D_0 (LSBs)
2	00	0	2	8	10
4	01	4	0	0	00
9	10	8	1	4	01
15	11	12	3	12	11

Figure 29.28 Output for the Flash ADC used in Ex. 29.12.

Accuracy Issues Related to the Two-Step Flash Converters

As stated previously, the overall accuracy of the converter is dependent on the first ADC. The second Flash must have only the accuracy of a stand-alone Flash converter. This means that if an 8-bit two-step Flash converter contains two 4-bit Flash converters, the second Flash needs only to have the resolution of a 4-bit Flash, which is not difficult

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to achieve. However, the first 4-bit Flash must have the accuracy of an 8-bit Flash, meaning that the worst-case INL and DNL for the first bit Flash must be less than ±½ LSB for an 8-bit ADC. Thus, the resistor matching and comparators contained in the first ADC must possess the accuracy of the overall converter. Refer to Sec. 29.2.1 for derivations on INL and DNL for a Flash. The DAC must also be accurate to within the resolution of the ADC.

Accuracy Issues Related to the Operational Amplifiers

With the addition of the summer and the amplifier, other sources of accuracy errors are present in this converter. The summer and the amplifier must add and amplify the signal to within ±½ LSB of the ideal value. It is quite difficult to implement standard operational amplifiers within high-resolution data converters because of these accuracy requirements. The nonideal characteristics of the op-amp are well known and in many cases alone limit the accuracy of the data converter. In this case, the amplifier is required to multiply the residue signal by some factor of two. Although this may not seem difficult at first glance, a closer examination will reveal a dependency on the open-loop gain.

Suppose that the amplifier was being used in a 12-bit, two-step data converter. Remember that in order for a data converter to be N-bit accurate, the INL and DNL need to be kept below ±½ LSB and one-half of an LSB can be defined as

$$0.5 \text{ LSB} = \frac{V_{REF}}{2^{N+1}} \tag{29.54}$$

Since the output of the amplifier gets quantized to 6 bits, the amplifier would need to be 6-bit accurate, resulting in an accuracy of

$$\text{Accuracy} = \frac{1}{2^{6+1}} = \frac{1}{128} = 0.0078 = 0.78\% \tag{29.55}$$

And suppose that a feedback amplifier with a gain of 64, or $2^{N/2}$, is used as the residue amplifier. The gain would need to be within the following range:

$$63.5 \text{ V/V} < A_{CL} < 64.5 \text{ V/V} \tag{29.56}$$

where A_{CL} is the closed-loop gain of the amplifier. Already, one can see why operational amplifiers are not used for high-accuracy applications. Designing an op-amp with a high degree of gain accuracy is very difficult.

Generalizing this concept for an N-bit application will require knowledge of feedback theory discussed in Ch. 23. The closed-loop gain of the amplifier is expressed as

$$A_{CL} = \frac{v_o}{v_i} = \frac{A_{OL}}{1 + A_{OL}\beta} \tag{29.57}$$

where A_{OL} is the open-loop gain of the amplifier and β is the feedback factor. Also, from Ch. 23, it is known that as A_{OL} increases in value, the closed-loop gain, A_{CL},

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approaches the value of $\frac{1}{\beta}$. Therefore, if it is assumed that the closed-loop gain of the amplifier will be equal to the ideal value of $\frac{1}{\beta}$ plus some maximum deviation from the ideal, ΔA, then,

$$A_{CL} = \frac{v_o}{v_i} = \frac{A_{OL}}{1 + A_{OL}\beta} = \frac{1}{\beta} + \Delta A \tag{29.58}$$

and the value of ΔA will be equal to ½ LSB and $\frac{1}{\beta}$ is the desired value of the closed-loop gain (usually some factor of 2^N). Therefore, the right two terms of Eq. (29.58) can be solved for the open-loop gain of the amplifier such that

$$|A_{OL}| = \frac{1}{\beta}(2^{N+1} + 1) \approx \frac{2^{N+1}}{\beta} \tag{29.59}$$

Equation (29.59) relates the open-loop gain of an amplifier to the resolution and closed-loop gain of the data converter. If the op-amp is to be used as a gain of 64, but is required to amplify signals with 6-bit accuracy, then the open-loop gain of the amplifier must be at least

$$|A_{OL}| \geq \frac{2^{N+1}}{\beta} = 128 \cdot 64 = 8,192 \text{ V/V} \tag{29.60}$$

This is certainly an achievable specification. However, notice that for every bit increase in resolution the open-loop gain requirement doubles. This is one reason why two-step Flash converters are limited in resolution to around 12 bits [9–12].

Linearity of the amplifier is another aspect of amplifier performance that must be considered when designing ADCs. The amplifier must be able to linearly amplify the input signal over an input voltage range to within ½ LSB of the number bits that its output is quantized. This means that if the amplifier is used in a 12-bit, two-step ADC, the slope of the transfer curve must be within 6-bit accuracy of the ideal. If the amplifier is not designed correctly, nonlinearity is introduced as devices in the amplifier go into nonsaturation. Harmonic distortion occurs, resulting in an error within the ADC.

Linearity is typically measured in terms of total harmonic distortion, or THD, (refer to Sec. 22.3). However, the transfer curve illustrates the limitation more effectively. Figure 29.29 shows a transfer curve of an op-amp with a gain of two. The ideal transfer curve is shown if the input range is known to be between – 1 and 1 V. The actual transfer curve shows nonlinearity introduced at both ends of the input range. In order for the amplifier to be N-bit accurate, the slope of the actual transfer curve may not vary from the ideal by more than the accuracy required at the output of the amplifier. Note also in Fig. 29.29 the subtle difference between a gain error and nonlinearity. However, a gain error is much less harmful to an ADC's performance than harmonic distortion.

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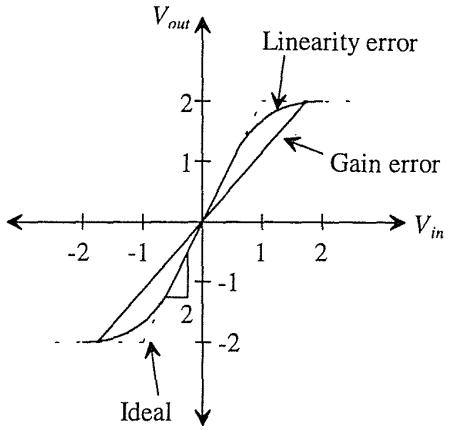


Figure 29.29 An op-amp transfer curve that distinguishes between gain error and linearity error.

29.2.3 The Pipeline ADC

After examining the two-step ADC, one might wonder whether there is such a converter as a three-step or four-step ADC. In actuality, one could divide the number of conversions into many steps. The pipeline ADC is an *N*-step converter, with 1-bit being converted per stage. Able to achieve high resolution (10–13 bits) at relatively fast speeds [11–15], the pipeline ADC consists of *N* stages connected in series (Fig. 29.30). Each stage contains a 1-bit ADC (a comparator), a sample-and-hold, a summer, and a gain of two amplifier. Each stage of the converter performs the following operation:

1. After the input signal has been sampled, compared it to $\frac{V_{REF}}{2}$. The output of each comparator is the bit conversion for that stage.
2. If $V_{IN} > \frac{V_{REF}}{2}$ (comparator output is 1), $\frac{V_{REF}}{2}$ is subtracted from the held signal and pass the result to the amplifier . If $V_{IN} < \frac{V_{REF}}{2}$ (comparator output is 0), then pass the original input signal to the amplifier. The output of each stage in the converter is referred to as the *residue*.
3. Multiply the result of the summation by 2 and pass the result to the sample-and-hold of the next stage.

A main advantage of the pipeline converter is its high throughput. After an initial delay of *N* clock cycles, one conversion will be completed per clock cycle. While the residue of the first stage is being operated on by the second stage, the first stage is free to operate on the next samples. Each stage operates on the residue passed down from the previous stage, thereby allowing for fast conversions. The disadvantage is having the initial *N* clock cycle delay before the first digital output appears. The severity of this disadvantage is, of course, dependent on the application.

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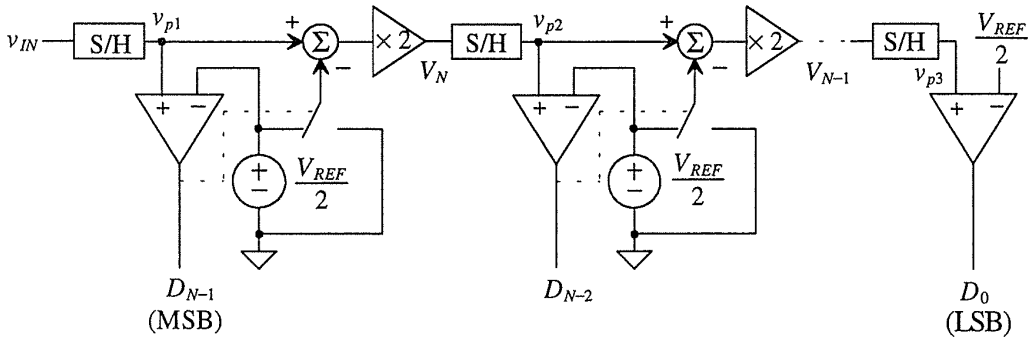


Figure 29.30 Block diagram of a pipeline ADC.

One interesting aspect of this converter is its dependency on the most significant stages for accuracy. A slight error in the first stage propagates through the converter and results in a much larger error at the end of the conversion. Each succeeding stage requires less accuracy than the one before, so special care must be taken when considering the first several stages.

Example 29.13

Assume the pipline converter shown in Fig. 29.30 is a 3-bit converter. Analyze the conversion process by making a table of the following variables: D_2, D_1, D_0, V_2, V_1, for v_{IN} = 2, 3, and 4.5 V. Assume that V_{REF} = 5 V. Where V_3 is the residue voltage out of the first stage and V_2 is the residue voltage out of the second stage.

The output of the first comparator, $D_2 = 0$, since $v_{IN} < 2.5$ V. Since $D_2 = 0$, $V_3 = 2(2) = 4$ V. Passing this voltage down the pipeline, since $V_3 > 2.5$ V, $D_1 = 1$ and V_2 becomes

$$V_1 = \left(V_2 - \frac{V_{REF}}{2}\right) \times 2 = 3 \text{ V}$$

The LSB, $D_0 = 1$, since $V_2 > 2.5$ V, and the digital output corresponding to V_{IN} = 2 V, is $D_2D_1D_0 = 011$. The actual digital outputs are simply the comparator outputs, and the data can be completed as seen in Fig. 29.31. ■

v_{IN}	V_3 (V)	V_2 (V)	Digital Out ($D_2D_1D_0$)
2.0	4.0	3.0	011
3.0	1.0	2.0	100
4.5	4.0	3.0	111

Figure 29.31 Output for the pipeline ADC used in Ex. 29.13.

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Accuracy Issues Related to the Pipeline Converter

The 1-bit per stage ADC can be analyzed by examining the switching point of each comparator for the ideal and nonideal case. Using Fig. 29.30, and assuming all the components are ideal, let $v_{IN,1}$ represents the value of the input voltage when the first comparator switches. This occurs when

$$v_{IN,1} = \frac{1}{2}V_{REF} \tag{29.61}$$

The positive input voltage on the second comparator, v_{p2}, can be written in terms of the previous stage, or

$$v_{p2} = [v_{IN} - \tfrac{1}{2} \cdot D_{N-1} \cdot V_{REF}] \cdot 2 \tag{29.62}$$

where D_{N-1} is the MSB output from the first comparator and is either a 1 or a 0. The second comparator switches when $v_{p2} = \frac{1}{2}V_{REF}$. The value of v_{IN} at this point, denoted as $v_{IN,2}$, is

$$v_{IN,2} = \tfrac{1}{2} \cdot D_{N-1} \cdot V_{REF} + \tfrac{1}{4}V_{REF} \tag{29.63}$$

Continuing on in a similar manner, we can write the value of the voltage on the positive input of the third comparator in terms of the previous two stages as

$$v_{p3} = \left[[v_{IN} - \frac{1}{2} \cdot D_{N-1} \cdot V_{REF}] \cdot 2 - [\frac{1}{2} \cdot D_{N-2} \cdot V_{REF}] \right] \cdot 2 \tag{29.64}$$

and the third comparator will switch when $v_{p3} = \frac{1}{2}V_{REF}$, which corresponds to the point at which v_{IN} becomes

$$v_{IN,3} = \tfrac{1}{2} \cdot D_{N-1} \cdot V_{REF} + \tfrac{1}{4} \cdot D_{N-2} \cdot V_{REF} + \tfrac{1}{8}V_{REF} \tag{29.65}$$

By now, a general trend can be recognized and the value of v_{IN} can be derived for the point at which the comparator of the N-th stage switches. This expression can be written as

$$v_{IN,N} = \tfrac{1}{2} \cdot D_{N-1} \cdot V_{REF} + \tfrac{1}{4} \cdot D_{N-2} \cdot V_{REF} + \tfrac{1}{8} \cdot D_{N-3} \cdot V_{REF} + \ldots\ldots + \tfrac{1}{2^{N-1}} \cdot D_1 \cdot V_{REF} + \tfrac{1}{2^N} \cdot V_{REF} \tag{29.66}$$

Notice that the preceding equation does not include D_0. This is because D_0 is the output of the N-th stage comparator.

Now that we have derived the switching points for the ideal case, the nonideal case can be considered. Only the major sources of error will be included in the analysis so as not to overwhelm the reader in the analysis. These include the comparator offset voltage, $V_{COS,x}$, and the sample-and-hold offset voltage, $V_{SOS,x}$. The variable, x, represents the number of the stage for which each of the errors is associated, and the "prime" notation will be used to distinguish between the ideal and nonideal case. The reader should also be aware that the offset voltages can be of either polarity. It will be assumed that all of the residue amplifiers will have the same gain, denoted as A.

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The positive input to the first nonideal comparator, v'_{p1}, will include the offset from the first sample-and-hold, such that

$$v'_{p1} = v_{IN} + V_{SOS,1} \tag{29.67}$$

Now the first comparator will not switch until the voltage on the positive input overcomes the comparator offset as well. This occurs when

$$v'_{p1} = \tfrac{1}{2}V_{REF} + V_{COS,1} \tag{29.68}$$

Thus, equating Eqs. (29.67) and (29.68) and solving for the value of the input voltage when the switching occurs for the first comparator yields

$$v'_{IN,1} = \tfrac{1}{2}V_{REF} + V_{COS,1} - V_{SOS,1} \tag{29.69}$$

The input to the second comparator, v'_{p2}, can be written as

$$v'_{p2} = [v_{IN} + V_{SOS,1} - \tfrac{1}{2} \cdot D_{N-1} \cdot V_{REF}] \cdot A + V_{SOS,2} \tag{29.70}$$

and the value of input voltage at the point which the second comparator switches occurs when

$$v'_{IN,2} = \frac{1}{2} \cdot D_{N-1} \cdot V_{REF} + \frac{1}{2}\frac{V_{REF}}{A} - V_{SOS,1} - \frac{1}{A}(V_{SOS,2} - V_{COS,2}) \tag{29.71}$$

Continuing in the same manner, we can write the value of the input voltage that causes the third comparator to switch as

$$v'_{IN,3} = \tfrac{1}{2} \cdot D_{N-1} \cdot V_{REF} + \tfrac{1}{2} \cdot D_{N-2} \cdot \tfrac{V_{REF}}{A} - V_{SOS,1} - \tfrac{1}{A}V_{SOS,2} - \tfrac{1}{A^2}V_{SOS,3} - \tfrac{1}{A^2}\left[V_{COS,3} - \tfrac{1}{2}V_{REF}\right] \tag{29.72}$$

which can be generalized to the N-th switching point as

$$v'_{IN,N} = \tfrac{1}{2} \cdot D_{N-1} \cdot V_{REF} + \tfrac{1}{2} \cdot D_{N-2} \cdot \tfrac{V_{REF}}{A} + \ldots + \tfrac{1}{2} \cdot D_1 \cdot \tfrac{V_{REF}}{A^{N-2}} + \tfrac{1}{2} \cdot \tfrac{V_{REF}}{A^{N-1}} + \tfrac{V_{COS,N}}{A^{N-1}} - \sum_{k=1}^{N} \tfrac{V_{SOS,k}}{A^{k-1}} \tag{29.73}$$

The INL can be calculated by subtracting switching point between the nonideal and ideal case. Therefore, the INL of the first stage is found by subtracting Eqs. (29.69) and (29.61).

$$INL_1 = v'_{IN,1} - v_{IN,1} = V_{COS,1} - V_{SOS,1} \tag{29.74}$$

The second stage INL is

$$INL_2 = v'_{IN,2} - v_{IN,2} = \frac{V_{REF}}{2}\left(\frac{1}{A} - \frac{1}{2}\right) - V_{SOS,1} - \frac{V_{SOS,2}}{A} + \frac{V_{COS,2}}{A} \tag{29.75}$$

and the INL for the N-th stage is

$$INL_N = \frac{1}{2} \cdot D_{N-2} \cdot V_{REF} \cdot \left(\frac{1}{A} - \frac{1}{2}\right) + \frac{1}{2} \cdot D_{N-3} \cdot V_{REF} \cdot \left(\frac{1}{A^2} - \frac{1}{4}\right) + \ldots$$

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$$+\frac{1}{2}\cdot D_1\cdot V_{REF}\cdot\left(\frac{1}{A^{N-2}}-\frac{1}{2^{N-2}}\right)+\frac{1}{2}\cdot V_{REF}\cdot\left(\frac{1}{A^{N-1}}-\frac{1}{2^{N-1}}\right)+\frac{V_{COS,N}}{A^{N-1}}-\sum_{k=1}^{N}\frac{V_{SOS,K}}{A^{k-1}} \tag{29.76}$$

Equations (29.74) - (29.76) are very important to an understanding of the limitations of the pipeline ADC. Notice the importance of the comparator and summer offsets in Eq. (29.74). The worst-case addition of the offsets must be less than ½ LSB to keep the ADC N-bit accurate. The second stage is more dependent on the gain of the residue amplifier as seen in Eq. (29.75). The gain error discussed in the previous section plays an important role in determining the overall accuracy of the converter. Now examine the effects of the offsets on the INL of the N-th stage. In Eq. (29.76), both the comparator and summer offsets of the N-th stage (when $k = N$) are divided by a large gain. Therefore, the latter stages in a pipeline ADC are not as critical to the accuracy as the first stages, and die area and power can be reduced by using less accurate designs for the least significant stages. The summation term in Eq. (29.76) also reveals that the summer offset of the first stage ($k = 1$) has a large effect on the N-th stage. However, this point is inconsequential since $V_{SOS,1}$ will have to be minimized to achieve N-bit accuracy for the first stage anyway. Typically, if the INL and DNL specifications can be made N-bit accurate in the first few stages, the latter stages will not adversely affect overall accuracy.

The DNL can be found by calculating the difference between the worst-case switching points and subtracting the ideal value for an LSB. As defined earlier, the worst-case will occur at midscale when the output switches from 0111...111 to 1000...000 as v_{IN} increase. Thus, the DNL is

$$DNL_{max}=v'_{IN,1}-v'_{IN,N}-\frac{V_{REF}}{2^N} \tag{29.77}$$

where $v'_{IN,N}$ is calculated using Eq. (29.73) and assuming that D_{N-1} is a zero and all the other bits are ones. Plugging in Eqs. (29.69) and (29.73) into Eq. (29.77) yields

$$DNL_{max}=\frac{1}{2}V_{REF}\left(1-\sum_{k=1}^{N-1}\frac{1}{A^k}\right)+V_{COS,1}-\frac{V_{COS,N}}{A^{N-1}}+\sum_{k=2}^{N}\frac{V_{SOS,K}}{A^{k-1}}-\frac{V_{REF}}{2^N} \tag{29.78}$$

Again, the term that dominates this expression is the comparator offset associated with the first stage and the summer offset of the second stage. The entire expression in Eq. (29.78) must be less than ½ LSB for the ADC to have N-bit resolution.

29.2.4 Integrating ADCs

Another type of ADC performs the conversion by integrating the input signal and correlating the integration time with a digital counter. Known as single- and dual-slope ADCs, these types of converters are used in high-resolution applications but have relatively slow conversions. However, they are very inexpensive to produce and are commonly found in slow-speed, cost-conscious applications.

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Single-Slope Architecture

Figure 29.32 illustrates the single-slope converter in block level form. A counter determines the number of clock pulses that are required before the integrated value of a reference voltage is equal to the sampled input signal. The number of clock pulses is proportional to the actual value of the input, and the output of the counter is the actual digital representation of the analog voltage.

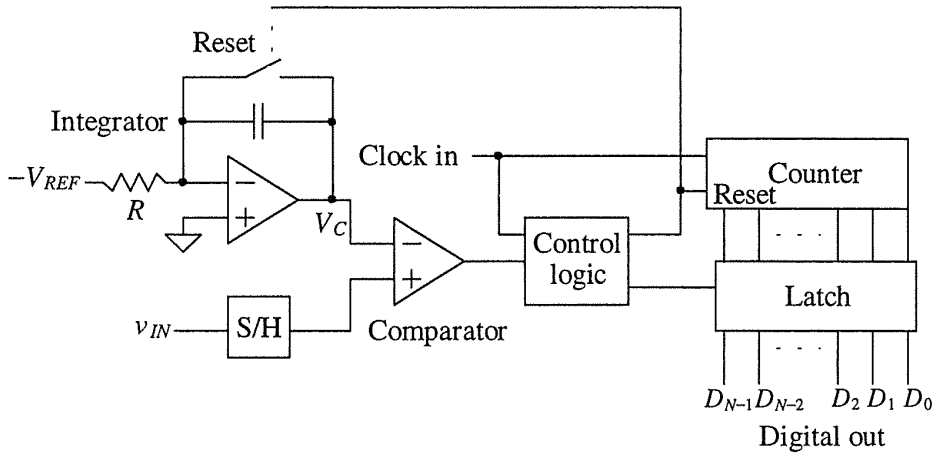


Figure 29.32 Block diagram of a single-slope ADC.

Since the reference is a DC voltage, the output of the integrator should start at zero and linearly increase with a slope that is dependent on the gain of the integrator. Notice that the reference voltage is defined as negative so that the output of the inverting integrator is positive. At the time when the output of the integrator surpasses the value of the S/H output, the comparator switches states, thus triggering the control logic to latch the value of the counter. The control logic also resets the system for the next sample. Figure 29.33 illustrates the behavior of the integrator output and the clock.

Note that if the input voltage is very small, the conversion time is very short, since the counter has to increment only a few times before the comparator latches the data. However, if the input voltage is at its full-scale value, the counter must increment to its maximum value of 2^N clock cycles. Thus, the clock frequency must be many times faster than the bandwidth of the input signal. The conversion time, t_c, is dependent on the value of the input signal and can be described as

$$t_c = \frac{v_{IN}}{V_{REF}} \cdot 2^N \cdot T_{CLK} \tag{29.79}$$

where T_{CLK} is the period of the clock. The sampling rate is inversely proportional to the conversion time and can be written as

$$f_{Sample} = \frac{V_{REF}}{V_{IN} \cdot 2^N} \cdot f_{CLK} \tag{29.80}$$

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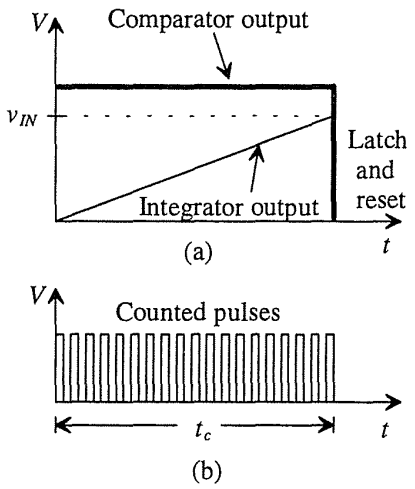


Figure 29.33 Single-slope ADC timing diagrams for (a) the comparator inputs and outputs and (b) the resulting counted pulses.

Example 29.14

Determine the clock frequency needed to form an 8-bit single-slope converter, if the analog signal bandwidth is 20 kHz.

Since the sampling rate required is 40 kHz, then the worst-case situation would occur for a full-scale input, in which event the integrator output would have to climb to its maximum value and the counter would increment 2^N times during the corresponding 25 μs period between samples. Therefore, the clock frequency would need to be 2^N times faster than the sampling rate or 10.24 MHz. ■

Accuracy Issues Related to the Single-Slope ADC

Obviously, many potential error sources abound in this architecture. At the end of the conversion, the voltage across the integrating capacitor, V_C , (assuming no initial condition), will be

$$V_C = \frac{1}{C}\int_0^{t_c} \frac{V_{REF}}{R} dt = \frac{V_{REF} \cdot t_c}{RC} \tag{29.81}$$

where t_c is the conversion time. Plugging Eq. (29.79) into Eq. (29.81) yields

$$V_C = \frac{2^N \cdot T_{CLK} \cdot v_{IN}}{RC} = \frac{2^N \cdot v_{IN}}{f_{CLK} \cdot RC} \tag{29.82}$$

Equation (29.82) is a revealing one in that the final voltage on the integrator output is dependent not only on the value of the input voltage, which is to be expected, but also on the value of R, C, and f_{CLK}. Therefore, any nonideal effects affecting these values will have an influence on the accuracy of the integrator output from sample to sample. For example, if an integrated diffused-resistor is used, then the voltage coefficient of the

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resistor could limit the accuracy, since the resistor will be effectively nonlinear. Similiarly, the capacitor may have charge leakage or aging effects associated with it. Also, any jitter in the clock will affect the overall accuracy. The integrator must have a linear slope to within the accuracy of the converter, which is dependent on the specifications of the op-amp (open-loop gain, settling time, offset, etc.) and must be considered accordingly.

Offset voltages on the comparator, the S/H, or the integrator will result in additional or fewer clock pulses, depending on the polarity of the offset. A delay also exists from the time that the inputs to the comparator are equal and the time that the output of the counter is actually latched. The reference voltage must also stay constant to within the accuracy of the converter.

Dual-Slope Architecture

A slightly more sophisticated design known as the dual-slope integrating ADC (Fig. 29.34) eliminates most of the problems encountered when using the single-slope converter. Here, two integrations are performed, one on the input signal and one on V_{REF}. The input voltage in this case is assumed to be negative, so that the output of the inverting integrator results in a positive slope during the first integration. Figure 29.35 illustrates the behavior for two separate samples. The first integration is of fixed length, dictated by the counter, in which the sample-and-held signal is integrated, resulting in the first slope. After the counter overflows and is reset, the reference voltage is connected to the input of the integrator. Since v_{IN} was negative and the reference voltage is positive, the inverting integrator output will begin discharging back down to zero at a constant slope. A counter again measures the amount of time for the integrator to discharge, thus generating the digital output.

For this figure, a 3-bit ADC is being used. Thus, the first integration period continues until the beginning of the eighth (2^3) clock pulse, which corresponds to the counter's overflow bit. Note that the integrator's output corresponding to V_B is twice the value of the output corresponding to V_A. Thus, it requires twice as many clock pulses for the integrator to discharge back to zero from V_B than from V_A. The output of the counter at t_A is three or 011, while the counter output at t_B is twice that value or six (110) and the quantization is complete.

Notice that the first slope varies according to the value of the input signal, while the second slope, dependent only on V_{REF}, is constant. Similiarly, the time required to generate the first slope is constant, since it is limited by the size of the counter. However, the discharging period is variable and results in the digital representation of the input voltage.

Accuracy Issues Related to the Dual-Slope ADC

One may wonder how the dual-slope converter is an improvement over the single-slope architecture, since a significantly longer conversion time is required. The first integration period requires a full 2^N clock cycle and cannot be decreased, because the

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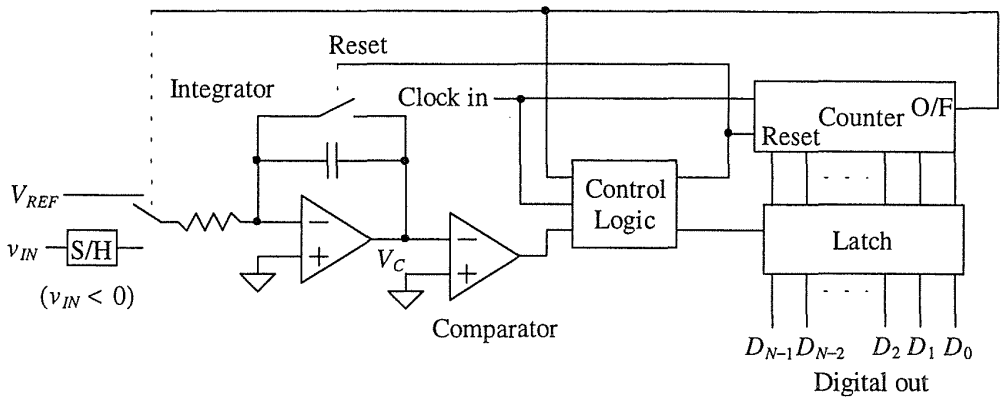


Figure 29.34 Block diagram of a dual-slope ADC.

second integration might require the full 2^N clock cycles to discharge if the maximum value of v_{IN} is being converted. However, the dual slope is the preferred architecture because the same integrator and clock are used to produce both slopes. Therefore, any nonidealities will essentially be canceled. For example, assuming that the S/H is ideal, the gain of the integrator at the end of the first integration period, T_1, becomes

$$V_C = -\frac{1}{C}\int_0^{T_1} \frac{v_{IN}}{R} dt = \frac{|v_{IN}| \cdot T_1}{RC} \tag{29.83}$$

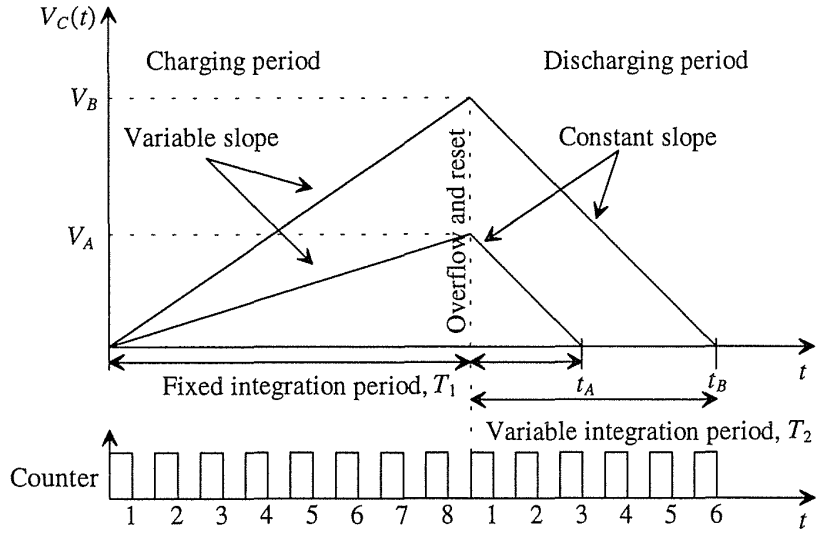


Figure 29.35 Integration periods and counter output for two separate samples of a 3-bit dual-slope ADC.

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The output at the end of T_1 is positive since the input voltage is considered to be negative and the integrator is inverting. After the clock has been reset, the discharging commences, with the initial condition defined by the value of the integrator output at the end of the charging period, or

$$V_C = \frac{|v_{IN}| \cdot T_1}{RC} - \frac{1}{C}\int_0^{T_2} \frac{V_{REF}}{R} dt \tag{29.84}$$

Once the value of the integrator output, V_C, reaches zero volts, Eq. (29.84) becomes

$$V_C = \frac{|v_{IN}| \cdot T_1}{RC} - \frac{V_{REF} \cdot T_2}{RC} = 0 \tag{29.85}$$

or,

$$|v_{IN}| \cdot T_1 = V_{REF} \cdot T_2 \tag{29.86}$$

At the end of the conversion, the dependencies on R and C have canceled out. Since we also know that the counter increments 2^N times at time, T_1, and the counter increments D times at time, T_2, Eq. (29.86) can be rewritten as

$$\frac{D}{2^N} = \frac{|v_{IN}|}{V_{REF}} \tag{29.87}$$

where D is the counter output that is actually the digital representation of the input voltage. Thus, it can be written that the ratio of the input voltage and the reference voltage is proportional to the ratio of the binary value of the digital word, D, and 2^N. Therefore, since the same clock pulse is responsible for the charging and discharging times, any irregularities will also cancel out.

29.2.5 The Successive Approximation ADC

The successive approximation converter basically performs a binary search through all possible quantization levels before converging on the final digital answer. The block diagram is seen in Fig. 29.36. An N-bit register controls the timing of the conversion where N is the resolution of the ADC. V_{IN} is sampled and compared to the output of the DAC. The comparator output controls the direction of the binary search, and the output of the successive approximation register (SAR) is the actual digital conversion. The successive approximation algorithm is as follows.

1. A 1 is applied to the input to the shift register. For each bit converted, the 1 is shifted to the right 1-bit position. $B_{N-1} = 1$ and B_{N-2} through $B_0 = 0$.
2. The MSB of the SAR, D_{N-1}, is initially set to 1, while the remaining bits, D_{N-2} through D_0, are set to 0.
3. Since the SAR output controls the DAC and the SAR output is 100...0, the DAC output will be set to $\frac{V_{REF}}{2}$.

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4. Next, v_{IN} is compared to $\frac{V_{REF}}{2}$. If $\frac{V_{REF}}{2}$ is greater than v_{IN}, then the comparator output is a 1 and the comparator resets D_{N-1} to 0. If $\frac{V_{REF}}{2}$ is less than v_{IN}, then the comparator output is a 0 and the D_{N-1} remains a 1. D_{N-1} is the actual MSB of the final digital output code.
5. The 1 applied to the shift register is then shifted by one position so that $B_{N-2} = 1$, while the remaining bits are all 0.
6. D_{N-2} is set to a 1, D_{N-3} through D_0 remain 0, while D_{N-1} remains the value from the MSB conversion. The output of the DAC will now either equal $\frac{V_{REF}}{4}$ (if $D_{N-1} = 0$) or $\frac{3V_{REF}}{4}$ (if $D_{N-1} = 1$).
7. Next, v_{IN} is compared to the output of the DAC. If the DAC output is greater than v_{IN}, the comparator the D_{N-2} is reset to 0. If v_{IN} is less than the DAC output, D_{N-2} remains a 1.
8. The process repeats until the output of the DAC converges to the value of v_{IN} within the resolution of the converter.

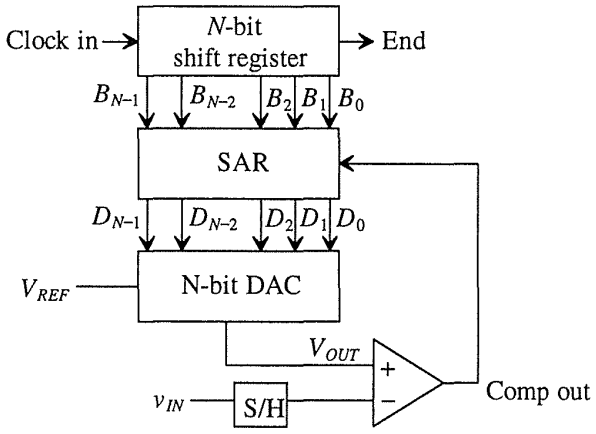


Figure 29.36 Block diagram of the successive approximation ADC.

Figure 29.37 shows an example of the binary search nature of the converter. The bolded line shows the path of the conversion for 101, corresponding to $\frac{5}{8}V_{REF}$. All possible quantization levels are represented in the binary tree. With each bit decided, the search space decreases by one-half until the correct answer is converged upon.

Example 29.15

Perform the operation of a 3-bit successive approximation ADC similar to Fig. 29.36 with $V_{REF} = 8$. Make a table that consists of $D_2D_1D_0$, $B_2B_1B_0$, V_{OUT} (the output from the DAC) and the comparator output, which shows the binary search algorithm of the converter for $v_{IN} = 5.5$ V and 2.5 V.

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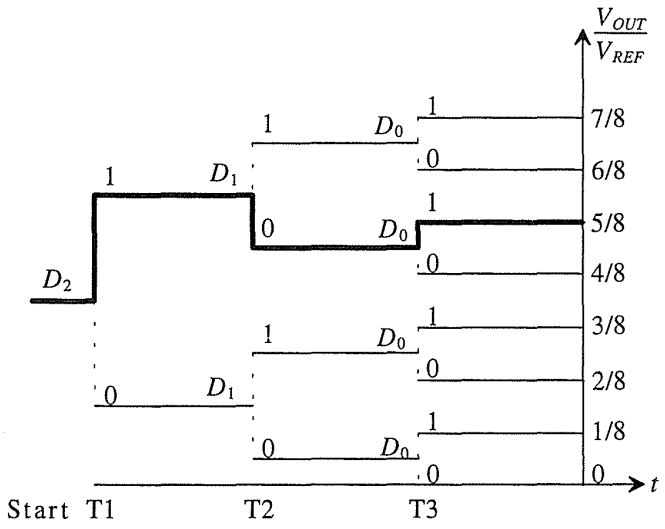


Figure 29.37 Binary search performed by a 3-bit successive approximation ADC for D=101.

We will designate $D_2'D_1'D_0'$ as the initial output of the SAR before the comparator makes its decision. The final value is designated as $D_2D_1D_0$. Notice that if the comparator is a 1, $D_2'D_1'D_0'$ differs from $D_2D_1D_0$, but if the comparator outputs a 0, then $D_2'D_1'D_0' = D_2D_1D_0$. The output of the shift register is designated as $B_2B_1B_0$.

Following the algorithm discussed previously, initially v_{IN} = 5.5 V and is compared with 4 V. Since the comparator output is 0, the MSB remains a 1. The next bit is examined, and the output of the DAC is now 6 V. Since $V_{OUT} > v_{IN}$, the comparator output is 1, which resets the current SAR bit, D_1, to a 0 at the end of period T2. Lastly, the LSB is examined, and v_{IN} is compared with 5 V. Since $v_{IN} > V_{OUT}$, The comparator output is a 0, and the current SAR bit, D_0, remains a 1. The results can be examined in Fig. 29.38a. The final value for $D_2D_1D_0$ is 101, which is what is expected considering that 101 in binary is equivalent to 5_{10}. Figure 29.38b shows the data for the ADC using v_{IN} = 2.5 V. The final value for v_{IN} = 2.5 is 010, which again is what is expected for 3-bit resolution. ■

The successive approximation ADC is one of the most popular architectures used today. The simplicity of the design allows for both high speed and high resolution while maintaining relatively small area. The limit to the ADC's accuracy is dependent mainly on the accuracy of the DAC. If the DAC does not produce the correct analog voltage with which to compare the input voltage, the entire converter output will contain an error. Referring again to Fig. 29.37, we can see that if a wrong decision is made early, a massive error will result as the converter attempts to search for the correct quantization level in the wrong half of the binary tree.

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Step	v_{IN}	$B_2B_1B_0$	$D_2'D_1'D_0'$	V_{OUT}	Comp Out	$D_2D_1D_0$
T1	5.5	100	100	$1/2\ V_{REF} = 4$ V	0	100
T2	5.5	010	110	$(1/2+1/4)V_{REF} = 6$ V	1	100
T3	5.5	001	101	$(1/2+1/8)V_{REF} = 5$ V	0	101

(a)

Step	v_{IN}	$B_2B_1B_0$	$D'_2D'_1D'_0$	V_{OUT}	Comp Out	$D_2D_1D_0$
T1	2.5	100	100	$1/2\ V_{REF} = 4$ V	1	000
T2	2.5	010	010	$1/4\ V_{REF} = 2$ V	0	010
T3	2.5	001	011	$(1/4+1/8)V_{REF} = 3$ V	1	010

(b)

Figure 29.38 Results from the 3-bit successive approximation ADC using (a) $v_{IN} = 5.5$ and (b) 2.5 V.

The Charge-Redistribution Successive Approximation ADC

One of the most popular types of successive approximation architectures uses the binary-weighted capacitor array (analyzed in Sec. 29.1.5) as its DAC. Called a charge redistribution successive approximation ADC [2,16,17], this converter samples the input signal and then performs the binary search based on the amount of charge on each of the DAC capacitors. Figure 29.39 shows an N-bit architecture. A comparator has replaced the unity gain buffer used in the DAC architecture. The binary-weighted capacitor array also samples the input voltage, so no external sample-and-hold is needed.

The conversion process begins by discharging capacitor array, via the reset switch. Although this may appear to be an insignificant action, the converter is also performing automatic offset cancellation. Once the reset switch is closed, the comparator acts as a unity gain buffer. Thus, the capacitor array charges to the offset

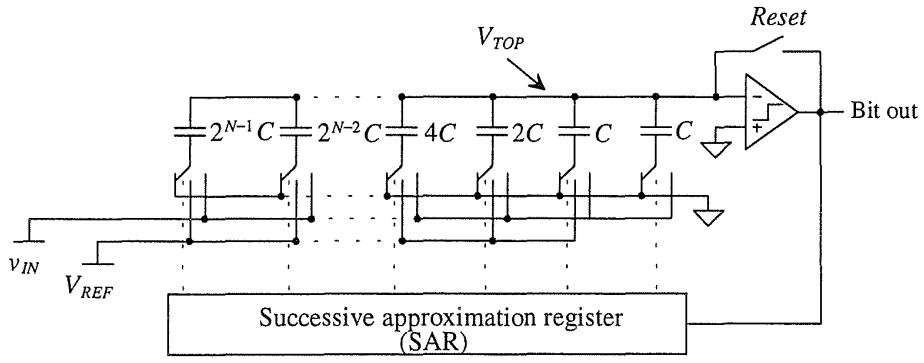


Figure 29.39 A charge redistribution ADC using a binary-weighted capacitor array DAC.

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voltage of the comparator. This requires that the comparator be designed so as to be unity gain stable, which means that internal compensation may have to be switched in during the reset period. Next, the input voltage, v_{IN}, is sampled onto the capacitor array. The reset switch is still closed, for the top plate of the capacitor array needs to be connected to virtual ground of the unity gain buffer. The equivalent circuit is seen in Fig. 29.40a.

The reset switch is then opened, and the bottom plates of each capacitor in the array are switched to ground, so that the voltage appearing at the top plate of the array is now $V_{OS} - v_{IN}$ (Fig. 29.40b). The conversion process begins by switching the bottom plate of the MSB capacitor to V_{REF} (Fig. 29.40c). If the output of the comparator is high, the bottom plate of the MSB capacitor remains connected to V_{REF}. If the comparator output is low, the bottom plate of the MSB is connected back to ground. The output of the comparator is D_{N-1}. The voltage at the top of the capacitor array, V_{TOP}, is now

$$V_{TOP} = -v_{IN} + V_{OS} + D_{N-1} \cdot \frac{V_{REF}}{2} \tag{29.88}$$

The next largest capacitor is tested in the same manner as seen in Fig. 29.40d. The voltage at the top plate of the capacitor after the second capacitor is tested becomes

$$V_{TOP} = -v_{IN} + V_{OS} + D_{N-1} \cdot \frac{V_{REF}}{2} + D_{N-2} \cdot \frac{V_{REF}}{4} \tag{29.89}$$

The conversion process continues on with the remaining capacitors so that the voltage on the top plate of the array, V_{TOP}, converges to the value of the offset voltage, V_{OS} (within the resolution of the converter), or

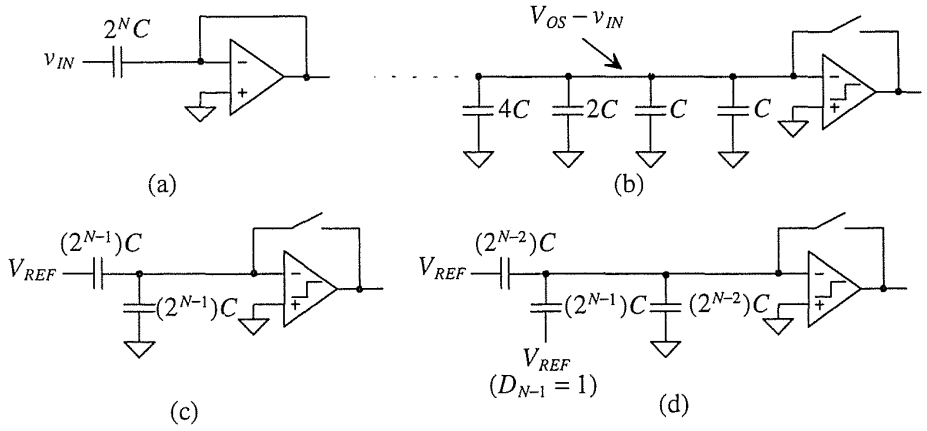


Figure 29.40 The charge redistribution process: (a) Sampling the input while autozeroing the offset, (b) the voltage at the top plate after sampling, (c) the equivalent circuit while converting the MSB, and (d) the equivalent circuit while converting the next largest capacitor with the MSB result equal to one.

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$$V_{TOP} = -v_{IN} + V_{OS} + D_{N-1} \cdot \frac{V_{REF}}{2} + D_{N-2} \cdot \frac{V_{REF}}{4} + ... + D_1 \cdot \frac{V_{REF}}{2^{N-2}} + D_0 \cdot \frac{V_{REF}}{2^{N-1}} \approx V_{OS} \tag{29.90}$$

Note that the initial charge stored on the capacitor array is now redistributed onto only those capacitors that have their bottom plates connected to V_{REF}.

Accuracy Issues Related to the Charge Redistribution Successive Approximation ADC

Obviously, the limitation of this architecture is the capacitor matching. The mismatch is analyzed in the same manner as the binary-weighted current source array of Sec. 29.1.4. Thus, substituting the value of the unit capacitance, C, for the value of the unit current source, I, and using Eqs. (29.27) – (29.30),

$$|INL|_{max} = 2^{N-1}(C + |\Delta C|_{max,INL}) - 2^{N-1} \cdot C = 2^{N-1} \cdot |\Delta C|_{max,INL} \tag{29.91}$$

where the maximum ΔC that will result in an INL that is less than ½ LSB is

$$|\Delta C|_{max,INL} = \frac{0.5C}{2^{N-1}} = \frac{C}{2^N} \tag{29.92}$$

and DNL is defined by

$$DNL_{max} = (2^N - 1) \cdot |\Delta C|_{max,DNL} \tag{29.93}$$

with the maximum ΔC which will result in a DNL less than ½ LSB being

$$|\Delta C|_{max,DNL} = \frac{0.5C}{2^N - 1} = \frac{C}{2^{N+1} - 2} \tag{29.94}$$

29.2.6 The Oversampling ADC

ADCs can be separated into two categories depending on the rate of sampling. The first category samples the input at the Nyquist rate, or $f_N = 2F$ where F is the bandwidth of the signal and f_N is the sampling rate. The second type samples the signal at a rate much higher than the signal bandwidth. This type of converter is called an oversampling converter. Traditionally, successive approximation or dual-slope converters are used when high resolution is desired. However, trimming is required when attempting to achieve higher accuracy. Dual-slope converters require high-speed, high-accuracy integrators that are only available using a high f_T bipolar process. Having to design a high-precision sample-and-hold is another factor that limits the realization of a high-resolution ADC using these architectures.

The oversampling ADC [18-20] is able to achieve much higher resolution than the Nyquist rate converters. This is because digital signal processing techniques are used in place of complex and precise analog components. The accuracy of the converter does not depend on the component matching, precise sample-and-hold circuitry, or trimming, and only a small amount of analog circuitry is required. Switched-capacitor implementations are easily achieved, and, as a result of the high sampling rate, only simplistic anti-aliasing circuitry needs to be used. However, because of the amount of

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time required to sample the input signal, the throughput is considerably less than the Nyquist rate ADCs.

Differences in Nyquist Rate and Oversampling ADCs

The typical process used in analog-to-digital conversion is seen in Fig. 29.41a, while the block diagram for the oversampling ADC is seen in Fig. 29.41b. After filtering the signal to help minimize anti-aliasing effects, the signal is sampled, quantized, and encoded or decoded using simple digital logic to provide the digital data in the proper format. When using oversampling ADCs, little if any, anti-alias filtering is needed, no dedicated S/H is required, the quantization is performed with a modulator, and the encoding usually takes the form of a digital filter.

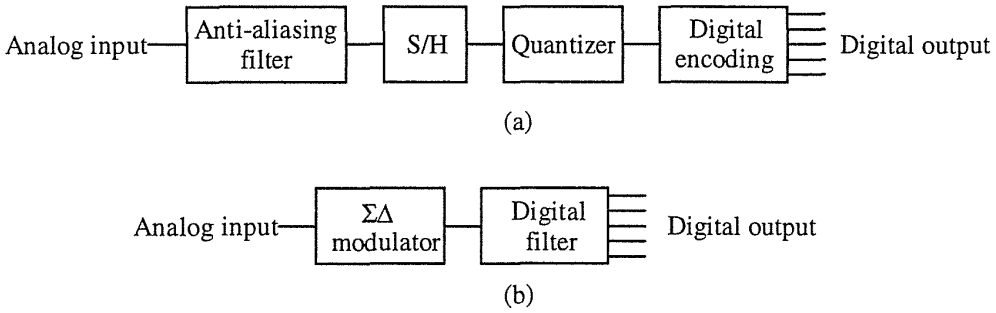


Figure 29.41 Typical block diagram for (a) Nyquist rate converters and (b) oversampling ADCs.

Since the oversampling converter samples at many times the signal bandwidth, aliasing is not a serious problem. A discussion of the frequency characteristics of aliasing was presented in Ch. 28. Figure 29.42a shows that when using Nyquist rate converters, a sampled signal in the frequency domain appears as a series of band-limited signals at multiples of the sampling frequency (see Fig. 28.26 for more details). As the sampling frequency decreases, the frequency spectra begin to overlap, and aliasing (Fig. 29.42b) occurs. Complex, "brickwall" filters are needed to correct the problem.

For oversampled ADCs, aliasing becomes much less of a factor. Since the sampling rate is much greater than the bandwidth of the signal, the frequency domain representation shows that the spectra are widely spaced, as seen in Fig. 29.42c. Therefore, overlapping of the spectra, and thus aliasing, will not occur, and only simple, first-order filters are required.

Oversampling converters typically employ switched-capacitor circuits and therefore do not need sample-and-hold circuits. The output of the modulator is a pulse-density modulated signal that represents the average of the input signal. The modulator is able to construct these pulses in real time, and so it is not necessary to hold the input value and perform the conversion.

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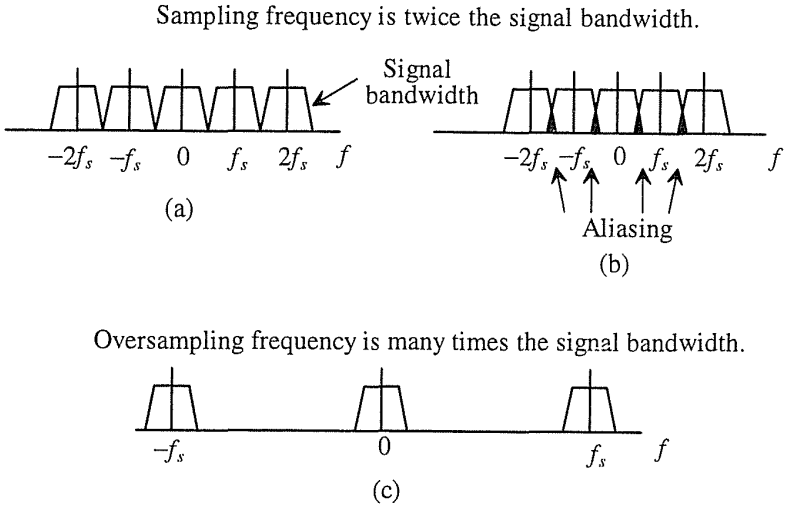


Figure 29.42 Frequency domain for (a) Nyquist rate converters (b) the aliasing that occurs; and (c) an oversampling converter.

As stated previously, the modulator actually provides the quantization in the form of a pulse-density modulated signal. Referred to as sigma-delta ($\Sigma\Delta$) or delta-sigma ($\Delta\Sigma$) modulation, the density of the pulses represents the average value of the signal over a specific period. Figure 29.43 illustrates the output of the modulator for the positive half of a sine wave input. Note that for the peak of the sine wave, most of the pulses are high. As the sine wave decreases in value, the pulses become distributed between high and low according to the sine wave value.

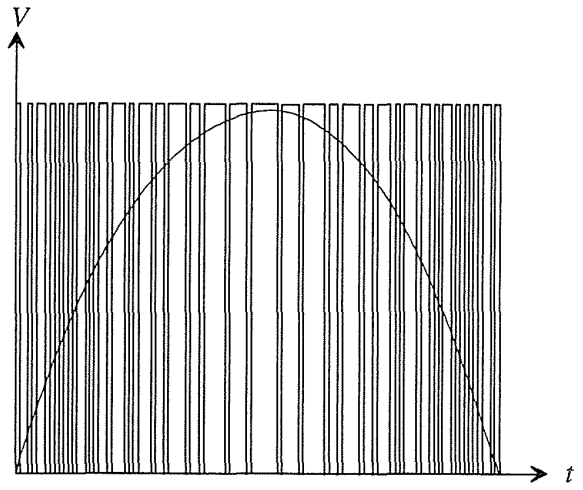


Figure 29.43 Pulse-density output from a sigma-delta modulator for a sine wave input.

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If the frequency of the sine wave represented the highest frequency component of the input signal, a Nyquist rate converter would take only two samples. The oversampling converter, however, may take hundreds of samples over the same period to produce this pulse-density signal.

Digital signal processing is then utilized, which has two purposes: to filter any out-of-band quantization noise and to attenuate any spurious out-of-band signals. The output of the filter is then downsampled to the Nyquist rate so that the resulting output of the ADC is the digital data, which represents the average value of the analog voltage over the oversampling period. The effective resolution of oversampling converters is determined by the values of signal-to-noise ratio and dynamic range obtained.

The First-Order ΣΔ Modulator

Now that the basic function of the ΣΔ modulator has been described, it would be useful to examine its inner workings and determine why ΣΔ modulation is so beneficial for generating high-resolution data. A basic first-order ΣΔ modulator can be seen in Fig. 29.44. Here, an integrator and a 1-bit ADC are in the forward path, and a 1-bit DAC is in the feedback path of a single-feedback loop system. The variables labeled are in terms of time, T, which is the inverse of the sampling frequency and k, which is an integer. The 1-bit ADC is simply a comparator that converts an analog signal into either a high or a low. The 1-bit DAC uses the comparator output to determine if $+V_{REF}$ or $-V_{REF}$ is summed with the input.

While the benefits of ΣΔ modulation are not obvious, a simple derivation of the output, $y(kT)$, will illuminate its distinct advantages. The output of the integrator, $u(kT)$, can be described as

$$u(kT) = x(kT - T) - q(kT - T) + u(kT - T) \tag{29.95}$$

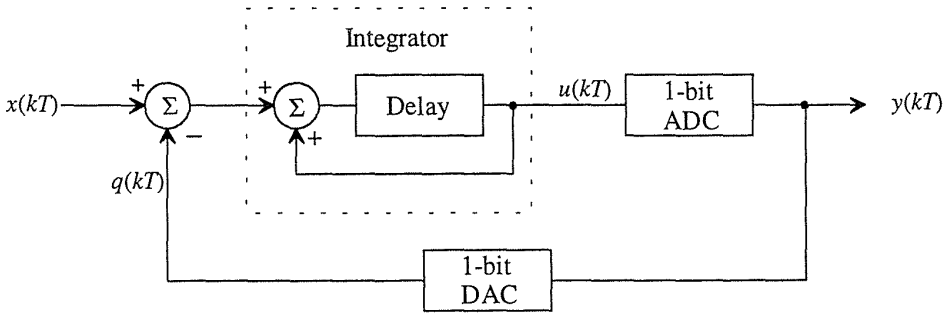


Figure 29.44 A first-order sigma-delta modulator.

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where, $x(kT-T) - q(kT-T)$ is equal to the integrator's previous input, and $u(kT-T)$ is its previous output. The quantization error for the 1-bit ADC, as discussed in Ch. 28, is again defined as the difference between its output and input such that

$$Q_e(kT) = y(kT) - u(kT) \tag{29.96}$$

Plugging Eq. (29.95) into Eq. (29.96), the output response, $y(kT)$ is

$$y(kT) = Q_e(kT) + x(kT-T) - q(kT-T) + u(kT-T) \tag{29.97}$$

An ideal 1-bit DAC has the following characteristic; if the input, $y(kT) = 0$, the output, $q(kT) = -V_{REF}$, and if $y(kT) = 1$, then $q(kT) = V_{REF}$. In reality, a 1-bit DAC consists of a couple of switches connecting V_{REF} or $-V_{REF}$ to a common node, so it is not difficult to assume that the DAC is ideal. Therefore,

$$y(kT) = q(kT) \tag{29.98}$$

Utilizing Eq. (29.96) and Eq. (29.97), we find that Eq. (29.98) becomes

$$y(kT) = x(kT-T) + Q_e(kT) - Q_e(kT-T) \tag{29.99}$$

Therefore, the output of the modulator consists of a quantized value of the input signal delayed by one sample period, plus a differencing of the quantization error between the present and previous values. Thus, the real power of ΣΔ modulation is that the quantization noise, Q_e, cancels itself out to the first order.

A frequency domain example will further illuminate this important fact. Suppose that the first-order modulator can be modeled in the s domain as seen in Fig. 29.45, with an ideal integrator represented with transfer function of $\frac{1}{s}$, the 1-bit ADC is modeled as a simple error source, $Q_e(s)$, and again the DAC is considered to be ideal, such that $y(s)$ is equal to $q(s)$. It is also assumed that the bandwidth of the input signal is much less than the bandwidth of the modulator. Therefore, using simple feedback theory, $v_{OUT}(s)$ becomes

$$v_{OUT}(s) = Q_e(s) + \frac{1}{s} \cdot [v_{IN}(s) - v_{OUT}(s)] \tag{29.100}$$

and solving for v_{OUT} yields,

$$v_{OUT}(s) = Q_e(s) \cdot \frac{s}{s+1} + v_{IN}(s)\frac{1}{s+1} \tag{29.101}$$

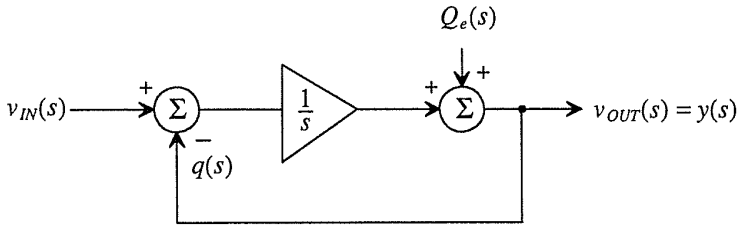


Figure 29.45 A frequency domain model for the first-order sigma-delta modulator.

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Note that the transfer function from v_{IN} to v_{OUT} follows that of a low-pass filter and that the transfer function of the quantization noise follows that of a high-pass filter. Plotted together in Fig. 29.46, it is seen that in the region where the signal is of interest, the noise has a small value while the signal has a high gain, and that at higher frequencies, beyond the bandwidth of the signal, the noise increases. The modulator has essentially pushed the power of the noise out of the bandwidth of the signal. This high-pass characteristic is known as *noise shaping* and is a powerful concept used within oversampling ADCs. Low-pass filtering will then be performed by the digital filter in order to remove all of the out-of-band quantization noise, which then permits the signal to be downsampled to yield the final high-resolution output.

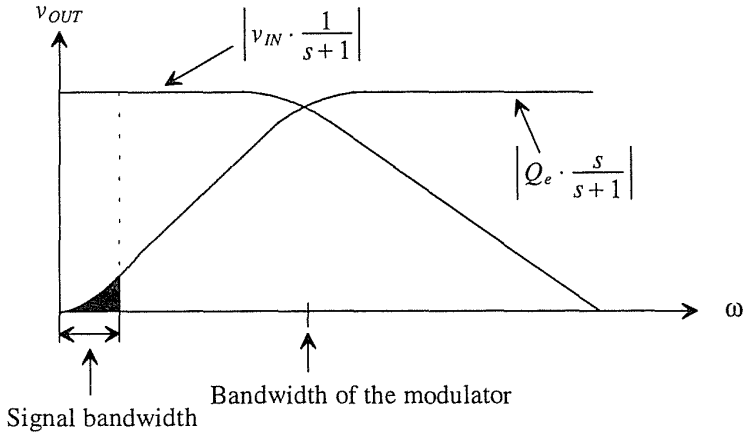


Figure 29.46 Frequency response of the first-order sigma-delta modulator.

As the ΣΔ modulator is generating the pulse-density modulated output, it is interesting to examine the mechanics occurring in the loop, which result in an average of the input. An actual ΣΔ modulator might resemble Fig. 29.47. A switched-capacitor integrator (see Sec. 27.2) provides the summing as well as the delay needed. The 1-bit ADC is a simple comparator, and 1-bit DAC is simply two voltage-controlled switches that select either $½V_{REF}$ or $-½V_{REF}$ to be summed with the input. A latched comparator is used to provide the necessary loop delay. Notice that the variables used are voltage representations of the variables used in Fig. 29.44. Remember that the function of the integrator is to accumulate differences between the input signal and the output of the DAC. If it is assumed that the input, $v_x(kT)$, is a positive DC voltage, then the output of the integrator should increase. However, the feedback mechanism is such that the 1-bit ADC (the comparator) has a low output if the integrator output, $v_u(kT)$, is positive. Thus, $½V_{REF}$ appears at the output of the DAC and is subtracted from the input, and the integrator output is driven back toward zero. The opposite occurs when $v_u(kT)$ is negative such that the integrator output is always driven toward zero by the feedback mechanism. An example will illustrate the operation of the modulator in more detail.

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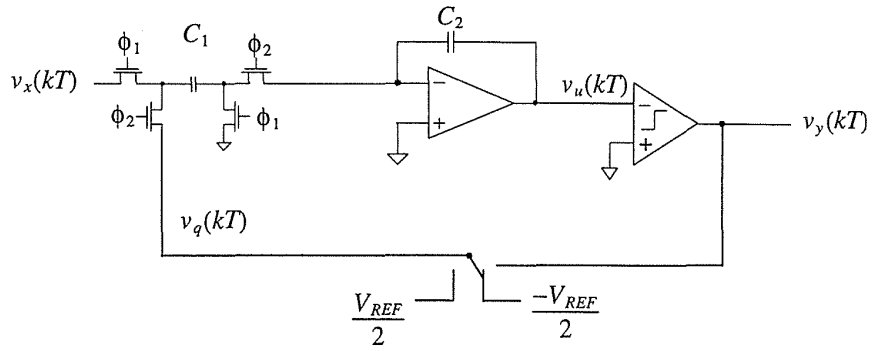


Figure 29.47 Implementation of a first-order sigma-delta modulator using a switched capacitor integrator.

Example 29.16

Using a general first-order ΣΔ modulator, assume that the input to the modulator, $v_x(kT)$ is a positive DC voltage of 0.4 V. Show the values of each variable around the ΣΔ modulator loop and prove that the overall average output of the DAC approaches 0.4 V after 10 cycles. Assume that the DAC output is ±1 V, and that the integrator output has a unity gain with an initial output voltage of 0.1 V, and that the comparator output is either ±1 V.

The present integrator output will be equal to the sum of the previous integrator output and the previous integrator input. Therefore, Eq. (29.95) becomes

$$v_u(kT) = v_u(kT - T) + v_a(kT - T) \tag{29.102}$$

where

$$v_a(kT) = v_x(kT) - v_q(kT) \tag{29.103}$$

and the quantizing error, $Q_e(kT)$, is defined by Eqs. (29.96) and (29.98) as

$$Q_e(kT) = v_q(kT) - v_u(kT) \tag{29.104}$$

The initial conditions define the values of the variable for $k = 0$. The output of the integrator is given to be 0.1 V. Thus, the ADC output is low, the DAC output is V_{REF}, and the output of the summer, $v_a(0)$, is $0.4 - V_{REF} = -0.6$ V.

The output for $k = 1$ begins again with the integrator output. Using Eq. (29.102), $v_u(kT)$ becomes

$$v_u(T) = 0.1 + (-0.6) = -0.5 \text{ V}$$

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Since the output of the integrator is negative, the output of the comparator is positive and $-V_{REF}$ is subtracted from 0.4 to arrive at the value for $v_a(T)$.

Continuing in the same manner and using the above equations, we note the voltages for each cycle in Fig. 29.48. After 10 cycles through the modulator, the average value of $v_q(kT)$ becomes,

$$\overline{v_q(kT)} = \frac{7-3}{10} = 0.4\ V$$

Notice that the behavior of $\overline{v_q(kT)}$ swings around the desired value 0.4 V. If we were to continue computing values, as k increases, the amount that $\overline{v_q(kT)}$ differs from 0.4 V would decrease. Ideally, we could make the deviation of $\overline{v_q(kT)}$ as small as desired by allowing the modulator to take as many samples as necessary to meet that accuracy. ■

k	$v_a(kT)$	$v_u(kT)$	$v_q(kT)= v_y(kT)$	$Q_e(kT)$	$\overline{v_q(kT)}$
0	–0.6	0.1	1.0	0.9	1.0
1	1.4	–0.5	–1.0	–0.5	0
2	–0.6	0.9	1.0	0.1	0.333
3	–0.6	0.3	1.0	0.7	0.50
4	1.4	–0.3	–1.0	–0.7	0.20
5	–0.6	1.1	1.0	–0.1	0.333
6	–0.6	0.5	1.0	0.5	0.429
7	1.4	–0.1	–1.0	–0.9	0.25
8	–0.6	1.3	1.0	–0.3	0.333
9	–0.6	0.7	1.0	0.3	0.40

Figure 29.48 Data from the first-order ΣΔ modulator.

One interesting note is to examine the effects of using a nonideal comparator. Suppose the integrator's output was smaller than the offset voltage of the comparator. A wrong decision would be made, causing $v_y(kT)$ to be the opposite of the desired value. However, as k increases, this error is averaged out, and the modulator still converges on the correct answer. Therefore, the comparator does not have to be very accurate in its ability to distinguish between two voltages, in contrast to Nyquist rate comparators.

An interesting application of the first-order ΣΔ modulator was reported in [20]. First-order ΣΔ modulators were used to perform pixel-level A/D conversion within a CMOS image sensor. In most digital imaging systems, ADCs are used to convert the analog signal representing the light intensity gathered by a charge-coupled device (CCD). Either a single high-speed ADC is used to convert the entire signal off of the CCD, or a parallel array of lower performance ADCs is used with one ADC assigned to

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each column of the sensor. Both of these configurations suffer performance loss because of the analog communication required between the sensor and the converter.

It would be optimum to provide an ADC for each pixel in the sensor. However, the size of the ADC becomes critical as the number of converters increases. By using 1-bit, first-order ΣΔ modulators, the author was able to minimize the area required for each pixel (including the first-order ΣΔ) to 30 μm by 30 μm and designed a first-order ΣΔ using only 19 transistors, as seen in Fig. 29.49.

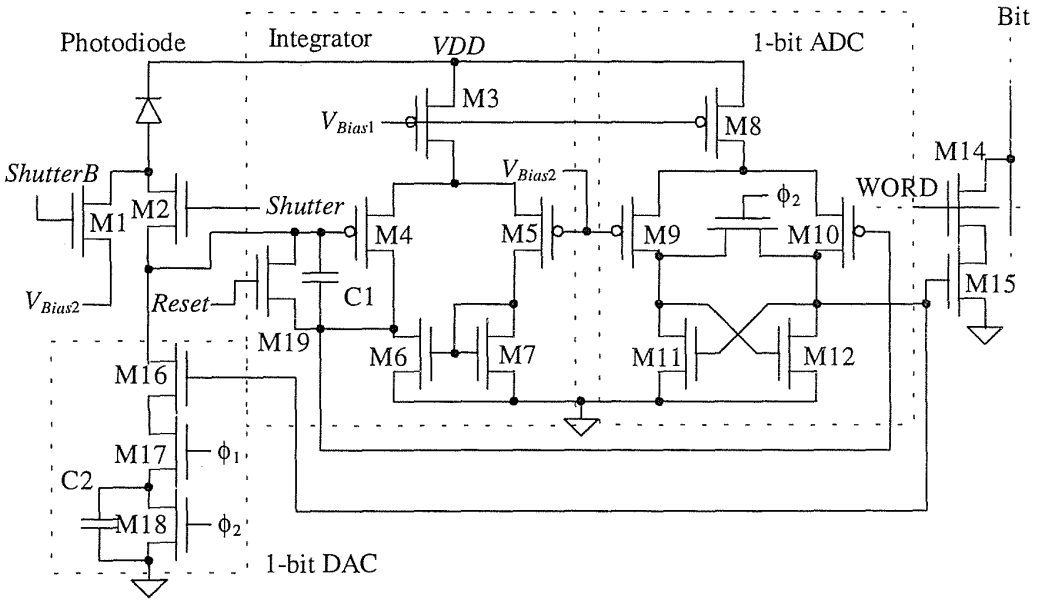


Figure 29.49 A pixel block using a first-order sigma-delta modulator [20].

Photocurrent from the photodiode is integrated on C1, using one side of a simple differential amplifier for the gain. The output of the integrator is passed on to a clocked comparator (via M10), which is a crude version of the first clocked comparator presented in Sec. 16.1.3. The comparator performs a 1-bit analog-to-digital conversion and passes the decision on to transistors, M16, M17, and M18, which actually form a 1-bit switched-capacitor DAC. This cleverly designed DAC does not convert the output of the comparator to an analog voltage, but instead uses C2 to remove charge from C1, thus resulting in an increase in output voltage of the integrator. The capacitor, C2, is discharged when ϕ2 is high. However, when the output of the comparator is high, ϕ1 is high, and ϕ2 is low, the capacitor C2 is connected directly to the input of the integrator, thus transferring charge off of C1. If the comparator output is low, no charge is transferred from C1. The author was able to achieve a SNR of 52 dB and a dynamic range of 85 dB using a 0.8 μm process.

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The Higher Order ΣΔ Modulators

Higher order ΣΔ modulators exist which provide a greater amount of noise shaping. A second-order ΣΔ modulator can be seen in Fig. 29.50. A derivation of the second-order transfer function would reveal that the output contained a delayed version of the input plus a second-order differencing of the quantization noise, Q_e (see Problem 29.38). A third-order modulator would contain third-order differencing of the quantization and can be constructed by adding another integrator similar to integrator A into the system.

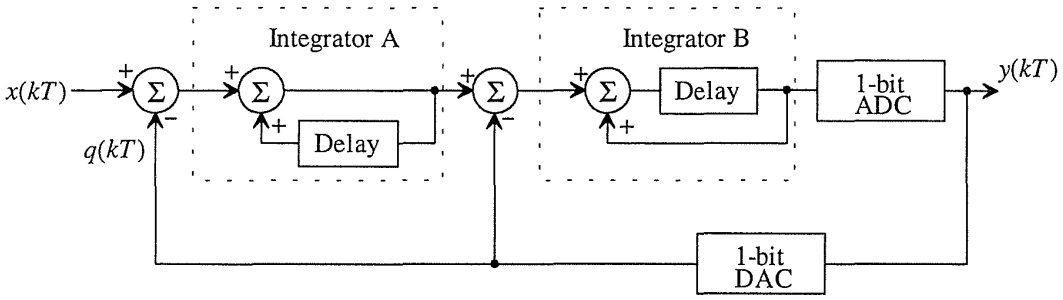


Figure 29.50 A second-order sigma-delta modulator.

Figure 29.51 shows the noise-shaping functions of a first-, second-, and third-order modulator. The cross-hatched area under each of the curves represents the noise that remains in the signal bandwidth and is a magnified version of the blackened area of Fig. 29.46. As the order increases, notice that more of the noise is pushed out into the higher frequencies, thus decreasing the noise in the signal bandwidth. It should be reiterated that ΣΔ modulators do not attenuate noise at all. In fact, they add quantization noise that is very large at high frequencies. But because almost all of the

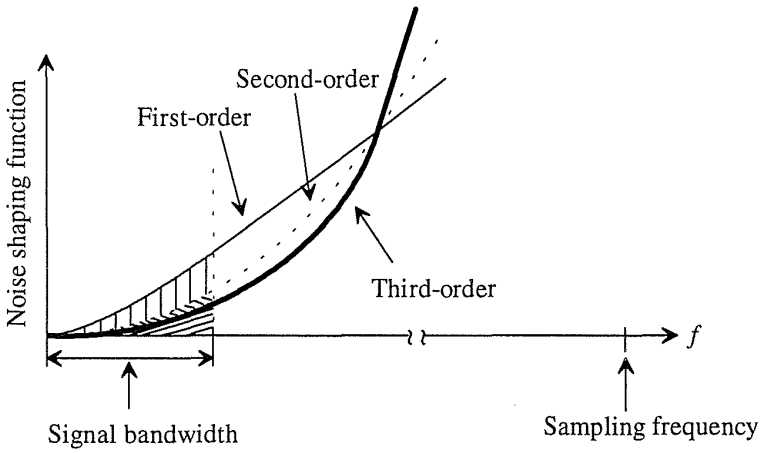


Figure 29.51 Noise shaping comparison of a first-, second-, and third-order modulator.

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noise is out of the signal bandwidth, it can be easily filtered, leaving only a small portion within the signal bandwidth. This point is important because the ΣΔ modulator should not be construed as a filtering circuit.

The resolution also increases as the order of the ΣΔ modulator and the oversampling ratio increases, as seen in Fig. 29.52 [21]. Using a first-order modulator, one can expect an increase in dynamic range of 9 dB with every doubling of the oversampling ratio. This correlates to an approximate increase in resolution of 1.5 bits according to Eq. (28.28). The higher-order modulators have even greater gains in resolution as a 2.5-bit increase is attained with each doubling of the oversampling ratio using a second-order modulator, while the third-order modulator increases 3.5 bits.

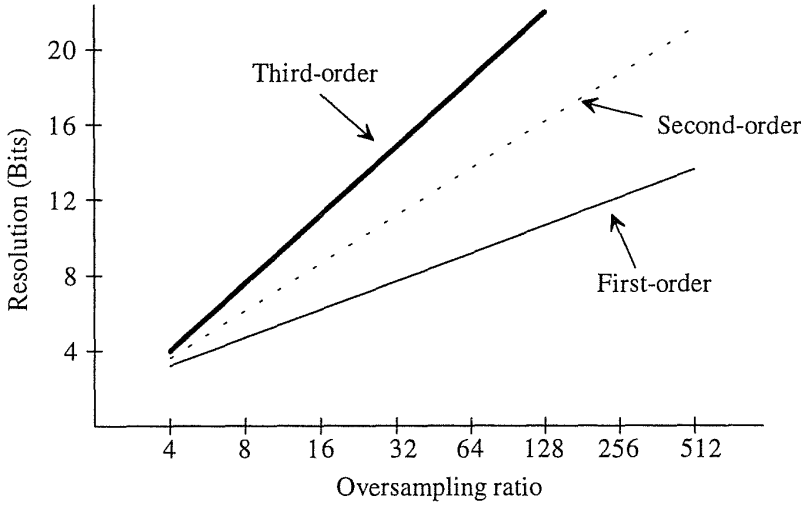


Figure 29.52 Comparison of first-, second-, and third-order modulators versus oversampling ratio and resolution.

One could essentially construct a high-order ΣΔ modulator with many integrators. However, as with any system employing feedback, stability becomes a critical issue. The same holds true for the high-order ΣΔ modulators. Several other topologies have been developed which can implement modulators in a cascaded fashion and are guaranteed to be stable [22, 23]. However, considerable matching requirements need to be overcome.

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[23] K. Uchimura et al, "Oversampling A-to-D and D-to-A Converters with Multistage Noise Shaping Modulators," *IEEE Transactions on Acoustics, Speech and Signal Processing*, pp. 1899-1905, December 1988.

PROBLEMS

29.1 A 3-bit resistor string DAC similiar to the one shown in Fig. 29.2a was designed with a desired resistor of 500 Ω. After fabrication, mismatch caused the actual value of the resistors to be

$R_1 = 500, R_2 = 480, R_3 = 470, R_4 = 520, R_5 = 510, R_6 = 490, R_7 = 530, R_8 = 500$

Determine the maximum INL and DNL for the DAC assuming V_{REF} = 5 V.

29.2 An 8-bit resistor string DAC similiar to the one shown in Fig. 29.2b was fabricated with a nominal resistor value of 1 kΩ. If the process was able to

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provide matching of resistors to within 1 percent, find the effective resolution of the converter. What is the maximum INL and DNL of the converter? Assume that V_{REF} = 5 V.

29.3 Compare the digital input codes necessary to generate all eight output values for a 3-bit resistor string DAC similiar to those shown in Fig. 29.2a and b. Design a digital circuit that will allow a 3-bit binary digital input code to be used for the DAC in Fig. 29.2a. Discuss the advantages and disadvantages of both architectures.

29.4 Plot the transfer curve of a 3-bit *R*-2*R* DAC if all *R*s = 1.1 kΩ and 2*R*s = 2 kΩ. What is the maximum INL and DNL for the converter? Assume all of the switches to be ideal and V_{REF} = 5 V.

29.5 Suppose that a 3-bit *R*-2*R* DAC contained resistors that were perfectly matched and that R = 1 kΩ and V_{REF} = 5 V. Determine the maximum switch resistance that can be tolerated for which the converter will still have 3-bit resolution. What are the values of INL and DNL?

29.6 The circuit illustrated in Fig. 29.5 is known as a current-mode *R*-2*R* DAC, since the output voltage is defined by the current through R_F. Shown in Fig. P29.6 is an *N*-bit voltage-mode *R*-2*R* DAC. Design a 3-bit voltage mode DAC and determine the output voltage for each of the eight input codes. Label each node voltage for each input. Assume that R = 1 kΩ and that $R_2 = R_1$ = 10 kΩ and V_{REF} = 5 V.

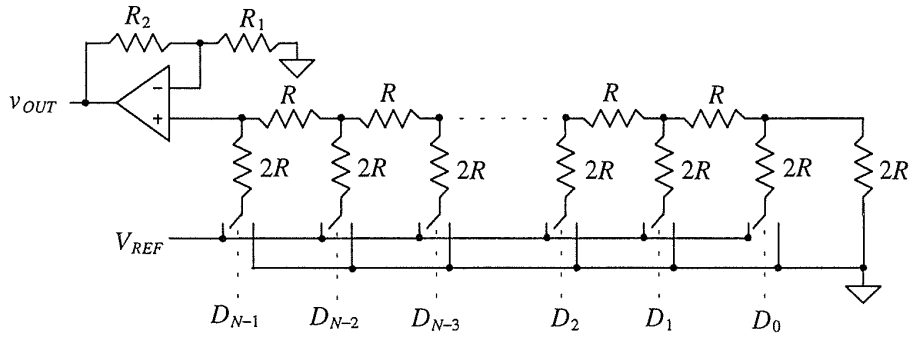


Figure P29.6

29.7 Design a 3-bit current steering DAC using the generic current steering DAC shown in Fig. 29.9. Assume that each current source, I, is 5 mA, and find the total output current for each input code.

29.8 A certain process is able to fabricate matched current sources to within 0.05 percent. Determine the maximum resolution that a current steering (nonbinary weighted) DAC can attain using this process.

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29.9 Design an 8-bit current steering DAC using binary-weighted current sources. Assume that the smallest current source will have a value of 1 μA. What is the range of values that the current source corresponding to the MSB can have while maintaining an INL of ½ LSB? Repeat for a DNL less than or equal to ½ LSB.

29.10 Prove that the 3-bit charge scaling DAC used in Ex. 29.6 has the same output voltage increments as the *R*-2*R* DAC in Ex. 29.3 for V_{REF} = 5 V and C = 0.5 pF.

29.11 Determine the output of the 6-bit charge scaling DAC used in Ex. 29.7 for each of the following inputs: D = 000010, 000100, 001000, and 010000.

29.12 Design a 4-bit charge scaling DAC using a split array. Assume that V_{REF} = 5 V and that C = 0.5 pF. Draw the equivalent circuit for each of the following input words and determine the value of the output voltage: D = 0001, 0010, 0100, 1000. Assuming the capacitor associated with the MSB had a mismatch of 4 percent, calculate the INL and DNL.

29.13 For the cyclic converter shown in Fig. 29.17, determine the gain error for a 3-bit conversion if the feedback amplifier had a gain of 0.45 V/V. Assume that V_{REF} = 5 V.

29.14 Repeat Problem 29.13 assuming that the output of the summer was always 0.2 V greater than the ideal and that the amplifier in the feedback path had a perfect gain of 0.5 V/V.

29.15 Repeat Problem 29.13 assuming that the output of the summer was always 0.2 V greater than ideal and that the amplifier in the feedback path had a gain of 0.45 V/V.

29.16 Design a 3-bit pipeline DAC using V_{REF} = 5 V. (a) Determine the maximum and minimum gain values for the first-stage amplifier for the DAC to have less than ±½ LSBs of DNL assuming the rest of the circuit is ideal. (b) Repeat for the second-stage amplifier. (c) Repeat for the last-stage amplifier.

29.17 Using the same DAC designed in Problem 29.16, (a) determine the overall error (offset, DNL, and INL) for the DAC designed in Problem 29.16 if the S/H amplifier in the first stage produces an offset at its output of 0.25 V. Assume that all the remaining components are ideal. (b) Repeat for the second-stage S/H. (c) Repeat for the last-stage S/H.

29.18 Design a 3-bit Flash ADC with its quantization error centered about zero LSBs. Determine the worst-case DNL and INL if resistor matching is known to be 5 percent. Assume that V_{REF} = 5 V.

29.19 Using the ADC designed in Problem 29.18, determine maximum offset which can be tolerated if all the comparators had the same magnitude of offset, but with different polarities, to attain a DNL of less than or equal to ±½ LSB.

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29.20 A 4-bit Flash ADC converter has a resistor string with mismatch as shown in Table P29.20. Determine the DNL and INL of the converter. How many bits of resolution does this converter possess? $V_{REF} = 5$ V.

Resistor	Mismatch (%)
1	2
2	1.5
3	0
4	–1
5	–0.5
6	1
7	1.5
8	2
9	2.5
10	1
11	–0.5
12	–1.5
13	–2
14	0
15	1
16	1

Table P29.20

29.21 Determine the open-loop gain required for the residue amplifier of a two step ADC necessary to keep the converter to within ½ LSB of accuracy with resolutions of (a) 4 bits, (b) 8 bits, and (c) 10 bits.

29.22 Assume that a 4-bit, two-step Flash ADC uses two separate Flash converters for the MSB and LSB ADCs. Assuming that all other components are ideal, show that the first Flash converter needs to be more accurate than the second converter. Assume that $V_{REF} = 5$ V.

29.23 Repeat Ex. 29.12 for $V_{IN} = 3, 5, 7.5, 14.75$ V.

29.24 Repeat Ex. 29.13 for $V_{IN} = 1, 4, 6, 7$ V and $V_{REF} = 8$ V.

29.25 Assume that an 8-bit pipeline ADC was fabricated and that all the amplifiers had a gain of 2.1 V/V instead of 2 V/V. If $V_{IN} = 3$ V and $V_{REF} = 5$ V, what would be the resulting digital output if the remaining components were considered to be ideal? What are the DNL and INL for this converter?

29.26 Show that the first-stage accuracy is the most critical for a 3-bit, 1-bit per stage pipeline ADC by generating a transfer curve and determining DNL and INL for the ADC for three cases: (1) The gain of the first-stage residue amplifier set

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equal to 2.2 V/V, (2) the second-stage residue amplifier set equal to 2.2 V/V, and (3) the third-stage residue amplifier set equal to 2.2 V/V. For each case, assume that the remaining components are ideal. Assume that $V_{REF} = 5$ V.

29.27 An 8-bit single-slope ADC with a 5 V reference is used to convert a slow-moving analog signal. What is the maximum conversion time assuming that the clock frequency is 1 MHz? What is the maximum frequency of the analog signal? What is the maximum value of the analog signal which can be converted?

29.28 An 8-bit single slope ADC with a 5 V reference uses a clock frequency of 1 MHz. Assuming all other components to be ideal, what is the limitation on the value of RC? What is the tolerance of the clock frequency which will ensure less than 0.5 LSB of INL?

29.29 An 8-bit dual slope ADC with a 5 V reference is used to convert the same analog signal in Problem 29.27. What is the maximum conversion time assuming that the clock frequency is 1 MHz? What is the mimimum conversion time that can be attained? If the analog signal is 2.5 V, what will be the total conversion time?

29.30 Discuss the advantages and disadvantages of using a dual-slope versus a single slope ADC architecture.

29.31 Repeat Ex. 29.15 for a 4-bit successive approximation ADC using $V_{REF} = 5$ V for $v_{IN} =$ 1, 3, and full-scale.

29.32 Assume that $v_{IN} = 2.49$ V for the ADC used in Problem 29.30 and that the comparator, because of its offset, makes the wrong decision for the MSB conversion. What will be the final digital output? Repeat for $v_{IN} = 0.3025$, assuming that the comparator makes the wrong decision on the LSB.

29.33 Design a 3-bit, charge redistribution ADC similiar to that shown in Fig. 29.39 and determine the voltage on the top plate of the capacitor array throughout the conversion process for $v_{IN} = 2$, 3, and 4 V, assuming that $V_{REF} = 5$ V. Assume that all components are ideal. Draw the equivalent circuit for each bit decision.

29.34 Determine the maximum INL and maximum DNL of the ADC designed in Problem 29.33 assuming that the capacitor array matching is 1 percent. Assume that the remaining components are ideal and that the unit capacitance, C, is 1 pF.

29.35 Show that the charge redistribution ADC used in Problems 29.32 and 29.33 is immune to comparator offset by assuming an initial offset voltage of 0.3 and determining the conversion for $v_{IN} = 2$ V.

29.36 Discuss the differences between Nyquist rate ADCs and oversampling ADCs.

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29.37 Write a simple computer program or use a math program to perform the analysis shown in Ex. 29.15. Run the program for $k = 200$ clock cycles and show that the average value of $v_q(kT)$ converges to the correct answer. How many clock cycles will it take to obtain an average value if $v_q(kT)$ stays within 8-bit accuracy of the ideal value of 0.4 V? 12-bit accuracy? 16-bit accuracy?

29.38 Prove that the output of the second-order ΣΔ modulator shown in Fig. 29.50 is,

$$y(kT) = x(kT - T) + Q_e(kT) - 2Q_e(kT - T) + Q_e(kT - 2T)$$

29.39 Assume that a first order ΣΔ ADC used on a satellite in low earth orbit experiences radiation in which an energetic particle causes a noise spike resulting in the comparator making the wrong decision on the 10th clock period. Using the program written in Problem 29.37, determine the number of clock cycles required before the average value of $v_q(kT)$ is within 12-bit accuracy of the ideal value of 0.4 V. How many extra clock cycles were required for this case versus the ideal conversion used in Prob. 36?

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Appendix

A

Orbit's CN20 Process

This appendix describes Orbit Semiconductor's[1] 2.0 μm double-poly, double-metal, n-well process (CN20). The process specifications, electrical and SPICE parameters, and design rules are given. The purpose is to give students the information they need to design a CMOS integrated circuit using an actual CMOS process. Commonly used symbols and physical constants are shown in Tables A.1 and A.2.

Name	Symbol	Value
terra	T	10^{12}
giga	G	10^{9}
mega	MEG	10^{6}
kilo	k	10^{3}
milli	m	10^{-3}
micro	μ	10^{-6}
nano	n	10^{-9}
pico	p	10^{-12}
femto	f	10^{-15}
atto	a	10^{-18}

Table A.1 Multiplier Symbols.

[1] Orbit Semiconductor, Inc., 1215 Bordeaux Drive, Sunnyvale, CA. 94089. Tel: (408) 744-1800.

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Name	Symbol	Value/Units
Vacuum dielectric constant	ε_0	8.85 aF/μm
Silicon dielectric constant	ε_{si}	$11.7\varepsilon_0$
SiO_2 dielectric constant	ε_{ox}	$3.97\varepsilon_0$
SiN_3 dielectric constant	ε_{Ni}	$\approx 16\varepsilon_0$
Boltzmann's constant	k	1.38×10^{-23} J/K
Electronic charge	q	1.6×10^{-19} C
Temperature	T	K
Thermal voltage	V_T	kT/q = 26 mV @ 300 K

Table A.2 Useful physical constants.

	Thickness or Separation μm	Plate Cap. aF/μm²			Fringe Cap. aF/μm		
		Min	Typ	Max	Min	Typ	Max
Poly1 gate oxide	0.040 +/– 0.003	803	863	933			
Poly2 gate oxide	0.046 +/– 0.005	677	750	842			
Poly1 to subs. (FOX)	0.600 +/– 0.050	53	58	63	85	88	92
Poly1 to poly2	0.070 +/– 0.008	443	493	557			
Poly1/2 thickness	0.400 +/– 0.030						
Metal1 thickness	0.600 +/– 0.060						
Metal2 thickness	1.150 +/– 0.120						
Metal1 to poly1/2	0.900 +/– 0.100	35	38	43	84	88	93
Metal1 to substrate	1.500 +/– 0.150	21	23	26	75	79	82
Metal1 to diffusion	0.900 +/– 0.100	35	38	43	84	88	93
Metal2 to poly1	1.900 +/– 0.200	16	18	20	83	87	91
Metal2 to substrate	2.500 +/– 0.250	13	14	15	78	81	85
Metal2 to diffusion	1.900 +/– 0.200	16	18	20	83	87	91
Metal2 to metal1	1.000 +/– 0.100	31	35	38	95	100	104

Table A.3 Process thicknesses and distances.

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A.1 Process Specifications

The physical distances, thicknesses, and capacitances for the CN20 process are shown in Table A.3. The main use of this table is in determining the parasitic capacitances in a particular layout.

A.1.1 Electrical Specifications

The following six tables describe the electrical characteristics of the p- and n-channel MOSFETs and the lateral bipolar junction transistor available in the CN20 process.

P-channel device L = 2 μm (Poly1)	**Min**	**Typ**	**Max**
Threshold voltage V_{THP}, (V)	0.6	0.8	1.1
Gamma ($V^{1/2}$)	0.45	0.55	0.65
KP = $(MUZ)(C'_{ox})$ ($\mu A/V^2$) (V_{SD} = 0.1 V with V_{SG} = 2 V to 3 V)	12	15	17
Punchthrough for minimum length channel (V)	10	14	16
Subthreshold slope^{-1} (mV/decade)	90	100	110
Delta length (DL) = $L_{drawn} - L_{eff}$ (μm)	0.7	0.4	0.1

Table A.4 Electrical parameters for the p-channel MOSFET.

N-channel device L = 2 μm (Poly1)	**Min**	**Typ**	**Max**
Threshold Voltage V_{THP}, (V)	0.6	0.8	1.1
Gamma ($V^{1/2}$)	0.15	0.25	0.35
KP = $(MUZ)(C'_{ox})$ ($\mu A/V^2$) (V_{DS} = 0.1V with V_{GS} = 2 V to 3 V)	40	46	52
Punchthrough for minimum length channel (V)	10	14	16
Subthreshold slope^{-1} (mV/decade)	90	100	110
Delta length (DL) = $L_{drawn} - L_{eff}$ (μm)	0.6	0.3	0

Table A.5 Electrical parameters for the n-channel MOSFET.

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NPN in the n-well Beta = 80-200 @ I_B = 1μA	
BV_{EBO}	10 V
BV_{CBO}	≥ 10 V
BV_{CES}	> 10 V
BV_{CBO}	≥ 60 V
P- Base Xj	0.45 to 0.5 μm
N+ emitter	= 0.3 μm
R collector	1.0 ± 0.2 kΩ/sq
P- base resistance	1.2 ± 0.2 kΩ/sq
Early voltage	>30 V

Table A.6 Electrical characteristics of the lateral NPN.

Sheet Resistance (Ω/square)	**Min**	**Typ**	**Max**
P+ active	50	70	100
N+ active	20	28	40
N-well (with field implant)	2,000	2,500	3,000
Poly1	15	21	30
Poly2	18	25	30
Metal1	0.05	0.06	0.06
Metal2	0.02	0.03	0.03
P - substrate (ohm-cm)	30	45	60

Table A.7 Sheet resistances.

Contact Resistance (Single contact 2 μm × 2 μm)	Min	Max
Metal1 to p+ active	35	75
Metal1 to n+ active	20	50
Metal1 to poly1	20	50
Metal1 to poly2	20	50
Metal1 to metal2	0.05	0.08

Table A.8 Contact resistances.

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Field Inversion and Breakdown Voltages (V)	Min	Typ	Max
n-channel poly1 field inversion	10	14	
n-channel metal1 field inversion	10	14	
p-channel poly1 field inversion		–14	–10
p-channel metal1 field inversion		–14	–10
n-diffusion to substrate junction breakdown		14	16
p-diffusion to well breakdown		15	18
n-Well to p-substrate junction breakdown		50	90

Table A.9 Field inversion and breakdown voltages.

A.1.2 N-Channel SPICE Models

This section describes the level 2 and BSIM SPICE models and shows characteristics for various-sized devices. These models are located in the file **spice.inf** in C:\LASI5\CN20.

```
.MODEL CMOSN NMOS LEVEL=2
+PHI=0.600000 TOX=4.3500E-08 XJ=0.200000U  TPG=1
+ VTO=0.8756 DELTA=8.5650E+00 LD=2.3950E-07 KP=4.5494E-05
+ UO=573.1 UEXP=1.5920E-01 UCRIT=5.9160E+04 RSH=1.0310E+01
+ GAMMA=0.4179 NSUB=3.3160E+15 NFS=8.1800E+12 VMAX=6.0280E+04
+ LAMBDA=2.9330E-02 CGDO=2.8518E-10 CGSO=2.8518E-10
+ CGBO=4.0921E-10 CJ=1.0375E-04 MJ=0.6604 CJSW=2.1694E-10
+ MJSW=0.178543 PB=0.800000

.MODEL CMOSNB NMOS LEVEL=4
+vfb=   -9.73820E-01  lvfb=    3.67458E-01   wvfb=   -4.72340E-02
+phi=   7.46556E-01   lphi=    -1.92454E-24  wphi=   8.06093E-24
+k1=    1.49134E+00   lk1=     -4.98139E-01  wk1=    2.78225E-01
+k2=    3.15199E-01   lk2=     -6.95350E-02  wk2=    -1.40057E-01
+eta=   -1.19300E-02  leta=    5.44713E-02   weta=   -2.67784E-02
+muz=   5.98328E+02   dl=      6.38067E-001  dw=     1.35520E-001
+u0=    5.27788E-02,  lu0=     4.85686E-02   wu0=    -8.55329E-02
+u1=    1.09730E-01   lu1=     7.28376E-01   wu1=    -4.22283E-01
+x2mz=7.18857E+00     lx2mz=  -2.47335E+00  wx2mz=7.12327E+01
+x2e=   -3.00000E-03  lx2e=    -7.20276E-03  wx2e=   -5.57093E-03
+x3e=   3.71969E-04   lx3e=    -3.16123E-03  wx3e=   -3.80806E-03
+x2u0=  1.30153E-03   lx2u0=   3.81838E-04   wx2u0=2.53131E-02
+x2u1=  -2.04836E-02  lx2u1=   3.48053E-02   wx2u1=4.44747E-02
+mus=   7.79064E+02   lmus=    3.62270E+02   wmus=  -2.71207E+02
+x2ms=-2.65485E+00    lx2ms=   3.68637E+01   wx2ms=1.12899E+02
+x3ms=1.18139E+01     lx3ms=   7.24951E+01   wx3ms=-5.25361E+01
+x3u1=  2.12924E-02   lx3u1=   5.85329E-02   wx3u1=-5.29634E-02
+tox=   4.35000E-002  temp=    2.70000E+01   vdd=    5.00000E+00
+cgdo=  3.79886E-010  cgso=    3.79886E-010  cgbo=   3.78415E-010
```

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```
+xpart= 1.00000E+000
+n0=    1.00000E+000  ln0=    0.00000E+000  wn0=    0.00000E+000
+nb=    0.00000E+000  lnb=    0.00000E+000  wnb=    0.00000E+000
+nd=    0.00000E+000  lnd=    0.00000E+000  wnd=    0.00000E+000
+rsh=27.9  cj=1.037500e-04  cjsw=2.169400e-10  js=1.000000e-08  pb=0.8
+pbsw=0.8  mj=0.66036  mjsw=0.178543  wdf=0  dell=0
```

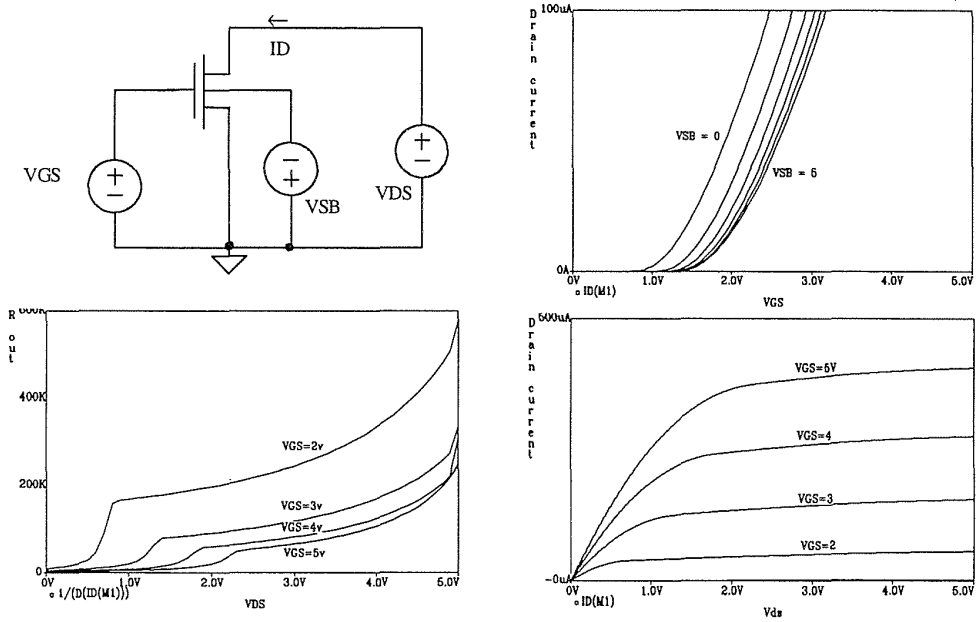


Figure A.1 Characteristics of an n-channel MOSFET with $L = 2$ μm $W = 3$ μm.

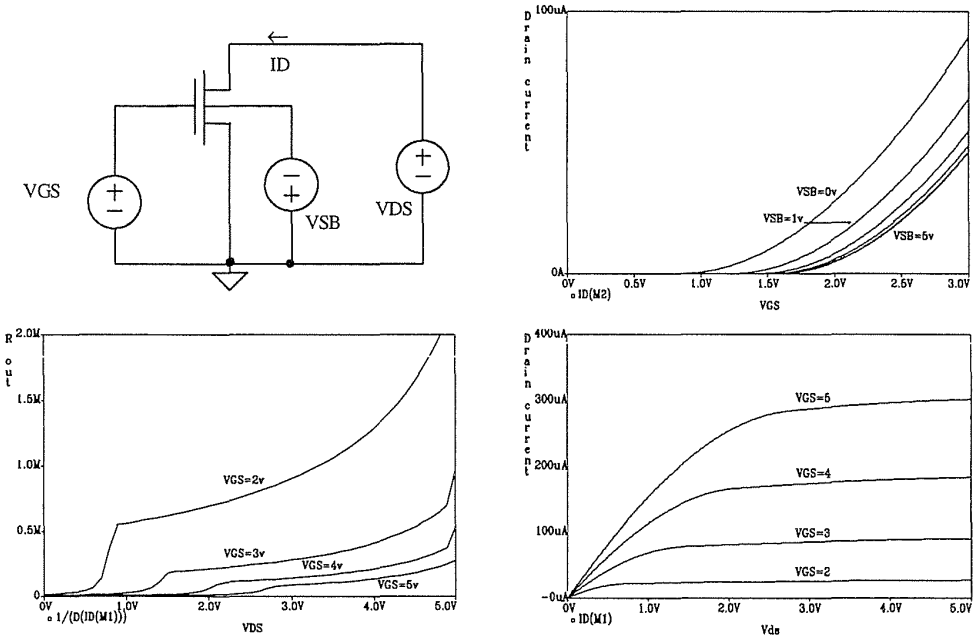


Figure A.2 Characteristics of an n-channel MOSFET with $L = 10$ μm $W = 10$ μm.

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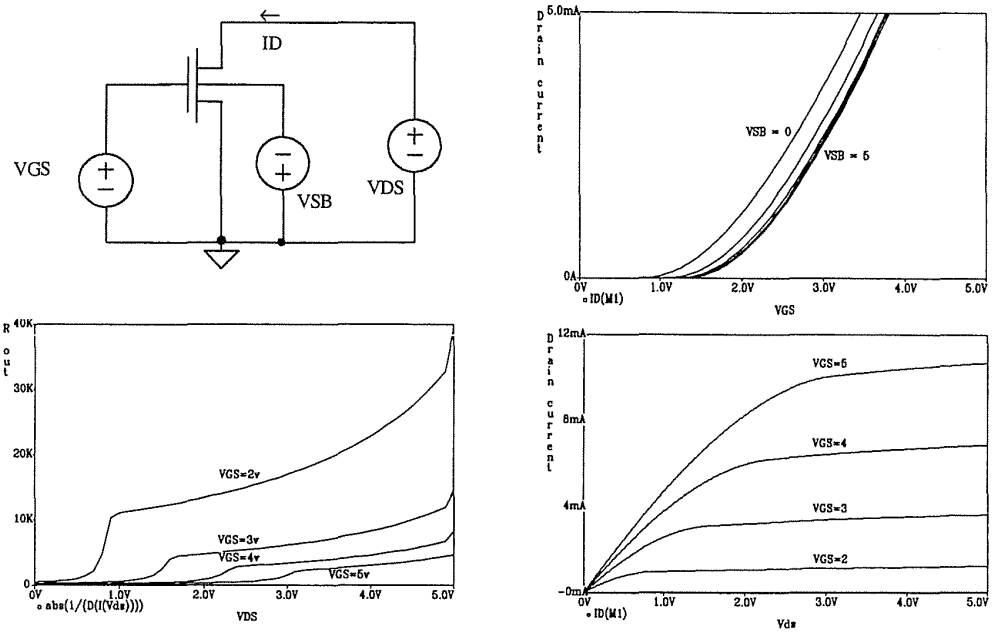


Figure A.3 Characteristics of an n-channel MOSFET with $L = 5$ μm $W = 200$ μm.

A.1.3 P-Channel SPICE Models

This section describes the level 2 and BSIM SPICE models and shows characteristics for various-sized devices. These models are located in the file **spice.inf** in C:\LASI5\CN20.

```
.MODEL CMOSP PMOS LEVEL=2
+PHI=0.600000 TOX=4.3500E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8889 DELTA=4.8720E+00 LD=2.9230E-07 KP=1.5035E-05
+ UO=189.4 UEXP=2.7910E-01 UCRIT=9.5670E+04 RSH=1.8180E+01
+ GAMMA=0.7327 NSUB=1.0190E+16 NFS=6.1500E+12 VMAX=9.9990E+05
+ LAMBDA=4.2290E-02 CGDO=3.4805E-10 CGSO=3.4805E-10
+ CGBO=4.0305E-10 CJ=3.2456E-04 MJ=0.6044 CJSW=2.5430E-10
+ MJSW=0.244194 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -3.6560E-07

.MODEL CMOSPB PMOS LEVEL=4
+vfb=   -2.65334E-01  lvfb=    6.50066E-02  wvfb=   1.48093E-01
+phi=   6.75823E-01   lphi=    -1.61406E-24  wphi=   8.03764E-24
+k1=    5.68962E-01   lk1=     3.88845E-02   wk1=    -5.33948E-02
+k2=    -5.52938E-02  lk2=     1.17906E-01   wk2=    -6.89149E-02
+eta=   -1.51784E-02  leta=    5.87976E-02   weta=   -7.51570E-04
+muz=   2.10669E+02   dl=      8.44240E-001  dw=     1.62551E-001
+u0=    1.04713E-01   lu0=     5.50950E-02   wu0=    -7.56659E-02
+u1=    1.46638E-02   lu1=     2.13581E-01   wu1=    -1.22509E-01
+x2mz=8.76354E+00     lx2mz=  -3.64793E+00  wx2mz=4.30934E+00
+x2e=   -2.13631E-03  lx2e=    -2.94140E-03  wx2e=   -2.48293E-03
```

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```
+x3e=  2.78813E-04   lx3e=   -1.60711E-03   wx3e=  -4.57237E-03
+x2u0= 3.93706E-03   lx2u0=  -5.66051E-04   wx2u0= 5.69621E-04
+x2u1= 1.07707E-04   lx2u1=  8.85125E-03    wx2u1= 1.71537E-03
+mus=  2.06464E+02   lmus=   1.39151E+02    wmus=  -4.95671E+01
+x2ms=5.86401E+00    lx2ms=  6.98887E+00,   wx2ms=5.55782E+00
+x3ms=-2.03430E-01   lx3ms=  1.16170E+01    wx3ms=-3.44342E+00
+x3u1= -1.17893E-02  lx3u1=  5.72098E-04    wx3u1= 8.29791E-03
+tox=   4.35000E-002  temp=   2.70000E+01    vdd=   5.00000E+00
+cgdo= 5.02635E-010  cgso=   5.02635E-010   cgbo=  3.85017E-010
+xpart= 1.00000E+000
+n0=    1.00000E+000  ln0=    0.00000E+000   wn0=   0.00000E+000
+nb=    0.00000E+000  lnb=    0.00000E+000   wnb=   0.00000E+000
+nd=    0.00000E+000  lnd=    0.00000E+000   wnd=   0.00000E+000
+rsh=54.7  cj=3.245600e-04  cjsw=2.543000e-10  js=1.000000e-08  pb=0.8
+pbsw=0.8  mj=0.60438  mjsw=0.244194  wdf=0  dell=0
```

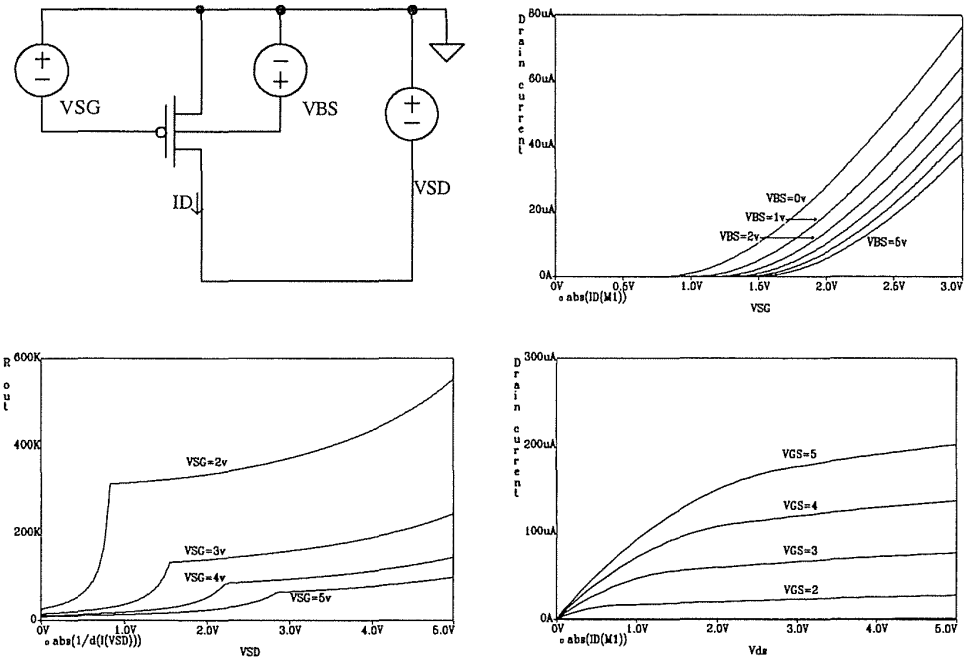


Figure A.4 Characteristics of a p-channel MOSFET with $L = 2$ μm $W = 3$ μm.

A.2 Hand Calculations

In this section we look at hand calculations using the BSIM model parameters.

A.2.1 The N-channel MOSFET Equations

DC Equations

For the n-channel MOSFET to be in the saturation region

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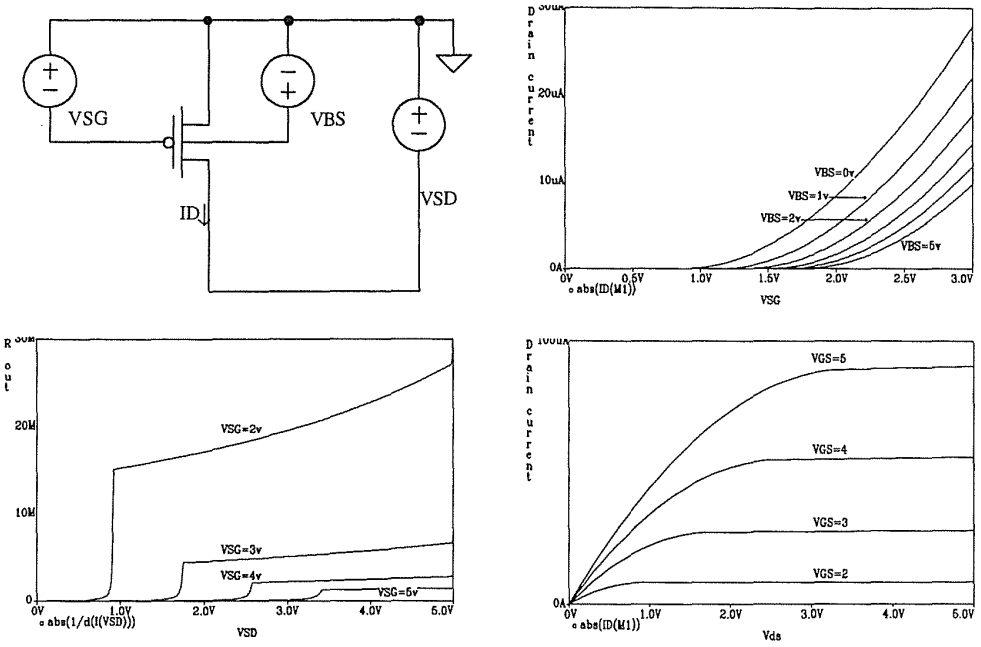


Figure A.5 Characteristics of a p-channel MOSFET with $L = 10\ \mu m$ W = 10 μm.

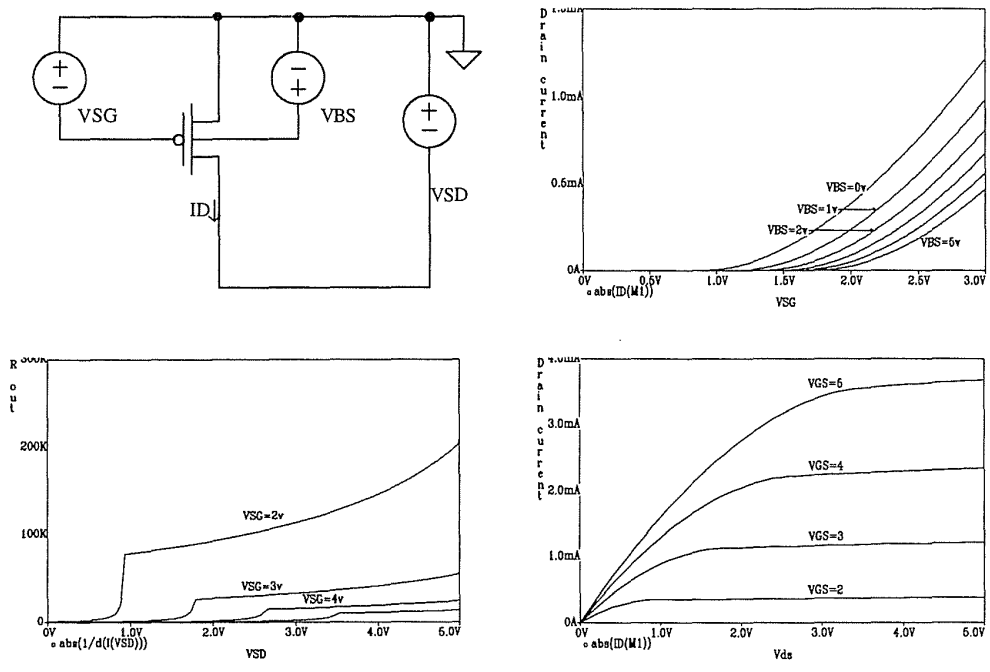


Figure A.6 Characteristics of a p-channel MOSFET with $L = 5\ \mu m$ $W = 200\ \mu m$.

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$$V_{DS} \geq V_{GS} - V_{THN} \tag{A.1}$$

The drain current, assuming $\lambda = 0$, is then given by

$$I_D = \frac{\beta}{2}(V_{GS} - V_{THN})^2 \tag{A.2}$$

where β is called the transconductance parameter and is given by

$$\beta = KP \cdot \frac{W}{L} \tag{A.3}$$

When the MOSFET is in the linear or triode region

$$V_{DS} \leq V_{GS} - V_{THN} \tag{A.4}$$

and

$$I_D = \beta\left((V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{A.5}$$

At the border between the saturation and triode regions

$$V_{DS} = V_{GS} - V_{THN} = V_{DS,sat} \tag{A.6}$$

The drain current at $V_{DS,sat}$ is called $I_{D,sat}$. The drain current of the n-channel MOSFET operating in the saturation region, including the effects of channel length modulation and mobility modulation, is given by

$$I_D = \frac{\beta}{2}(V_{GS} - V_{THN})^2[1 + (\lambda_c + \lambda_m)(V_{DS} - V_{DS,sat})] \text{ for } V_{DS} \geq V_{GS} - V_{THN} \tag{A.7}$$

Normally, the channel length and mobility modulation parameters λ_c and λ_m are combined into a single parameter, λ. This single parameter is determined empirically for a given MOSFET channel length. For the CN20 process, using device lengths in excess of 5 μm results in a λ of approximately 0.06 V^{-1}. Based on the results of Figs. A.1 through A.3, λ has a strong dependence on V_{DS}.

Calculation of V_{THN} and KP Using the BSIM Model Parameters

The threshold voltage of the n-channel MOSFET, V_{THN}, as a function of the source to substrate potential, V_{SB}, using the BSIM model parameters, is given by

$$V_{THN} = VFB + PHI + K1 \cdot \sqrt{PHI + V_{SB}} - K2 \cdot (PHI + V_{SB}) \tag{A.8}$$

or using the n-channel BSIM model parameters of the previous section and assuming that $V_{SB} = 0$ results in

$$V_{THN} \approx 0.83 \text{ V} \tag{A.9}$$

The oxide capacitance per unit area, using the oxide dielectric constant of Table A.2 and the oxide thickness from the BSIM model parameters, is given by

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$$C'_{ox} = \frac{\varepsilon_{ox}}{TOX} = \frac{35.13\ \text{aF}/\mu\text{m}}{0.0435\ \mu\text{m}} \approx 800\ \frac{\text{aF}}{\mu\text{m}^2} \tag{A.10}$$

The transconductance parameter, *KP*, for the n-channel MOSFET is then approximated by

$$KP = MUZ \cdot C'_{ox} = \frac{598\ \text{cm}^2}{\text{V} \cdot \text{s}} \cdot \frac{10^8 \mu\text{m}^2}{\text{cm}^2} \cdot \frac{800\ \text{aF}}{\mu\text{m}^2} \approx 50\ \frac{\mu\text{A}}{\text{V}^2} \tag{A.11}$$

Small-Signal Parameters

The small-signal transconductance of a MOSFET, in terms of the MOSFET's DC operating point, is given by

$$g_m = \beta(V_{GS} - V_{THN}) = \sqrt{2\beta I_D} \tag{A.12}$$

when the MOSFET is operating in the strong inversion (square law) region and

$$g_m = \frac{I_D}{V_T} \tag{A.13}$$

for a MOSFET operating in the subthreshold region. The body transconductance due to the threshold voltage changing with variations in the source to substrate voltage is given by

$$g_{mb} = g_m \cdot \eta \tag{A.14}$$

where

$$\eta = \frac{K1}{2\sqrt{PHI + V_{SB}}} - K2 \tag{A.15}$$

For large V_{SB} the small-signal parameter η can be negative. When this occurs, we will assume g_{mb} is 0. This is equivalent to saying that the threshold voltage, V_{THN}, doesn't change significantly for small AC signals varying around a large substrate-body potential. A review of Figs. A.1 to A.3 shows that indeed the threshold voltage approaches a constant with increasing V_{SB}.

The small-signal output resistance is calculated using

$$r_o = \frac{1}{\lambda I_D} \tag{A.16}$$

Normally, the value of λ is strongly dependent on the drain-source voltage of the MOSFET. (See plots of the MOSFET output resistance in Figs. A.1 to A.3.) For MOSFETs with lengths in excess of 5 μm, a λ of 0.06 V^{-1} is a good approximation.

A.2.2 The P-channel MOSFET Equations

DC Equations

Note that in this text we have assumed that the threshold voltages of both the p- and the n-channel MOSFETs are positive. Also, all voltages and currents that describe the

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operation of the p-channel MOSFET in the following discussion are positive. For the p-channel MOSFET to be in the saturation region

$$V_{SD} \geq V_{SG} - V_{THP} \tag{A.17}$$

The drain current of the p-channel MOSFET, assuming $\lambda = 0$, is given by

$$I_D = \frac{\beta}{2}(V_{SG} - V_{THP})^2 \tag{A.18}$$

with

$$\beta = KP \cdot \frac{W}{L} \tag{A.19}$$

For the p-channel MOSFET to operate in the triode region

$$V_{SD} \leq V_{SG} - V_{THP} \tag{A.20}$$

and the drain current is given by

$$I_D = \beta\left((V_{SG} - V_{THP})V_{SD} - \frac{V_{SD}^2}{2}\right) \tag{A.21}$$

Calculation of V_{THP} and KP Using the BSIM Model Parameters

The threshold voltage of the p-channel MOSFET is calculated using

$$V_{THP} = VFB + PHI + K1 \cdot \sqrt{PHI + V_{BS}} - K2 \cdot (PHI + V_{BS}) \tag{A.22}$$

Or using the BSIM model parameters of the previous section for the p-channel MOSFET with $V_{BS} = 0$ results in

$$V_{THP} \approx 0.91\text{V} \tag{A.23}$$

The transconductance parameter, *KP*, for the p-channel MOSFET is given by

$$KP = MUZ \cdot C'_{ox} \approx 17\ \frac{\mu\text{A}}{\text{V}^2} \tag{A.24}$$

Small-Signal Parameters

The small-signal transconductance of a p-channel MOSFET is given by

$$g_m = \beta(V_{SG} - V_{THP}) = \sqrt{2\beta I_D} \tag{A.25}$$

while the body transconductance is given by

$$g_{mb} = g_m \cdot \eta \tag{A.26}$$

with

$$\eta = \frac{K1}{2\sqrt{PHI + V_{BS}}} - K2 \tag{A.27}$$

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Again g_{mb} is assumed 0 when η becomes negative. The output resistance of the p-channel MOSFET is calculated using Eq. (A.16). A good approximation for λ of the p-channel MOSFET with device lengths in excess of 5 μm is also 0.06 V^{-1}.

A.3 Design Rules

The design rules presented in this appendix are a simplified, and thus more limited, version of the actual design rules specified by Orbit. The Design Rule Checker, LASIDRC, together with the check file "cn20.drc" are used to check layouts with these simplified design rules. The setups have been used successfully on student chip design and research projects at the University of Idaho for several years. The technology is specified to MOSIS as "FORESIGHT-CN20."

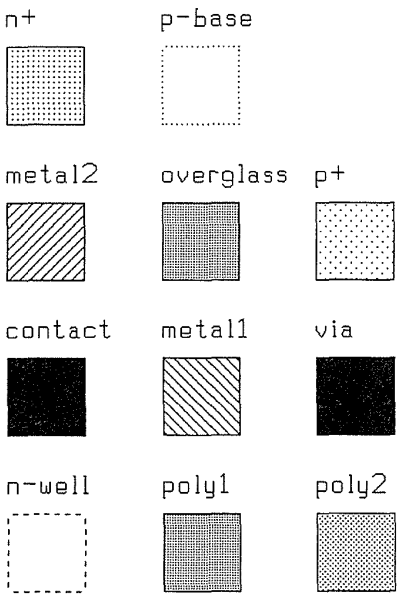
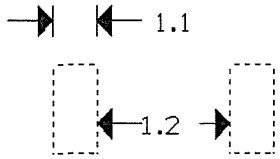


Figure A.7 Layer information, fill, and outline.

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	microns	check#
1.1 WIDTH	3.0	1
1.2 SPACE	9.0	2



1. N-WELL

Figure A.8 N-well design rules, the check number corresponding to the check number used with LASIDRC.

		microns	check #
2.1	WIDTH	3.0	3
2.2	ACTIVE TO ACTIVE	3.0	4
2.3	N+ ACTIVE TO N-WELL	7.0	5
2.4	P+ SUB. CONTACT TO N-WELL	4.0	6
2.5	N-WELL TO N+ WELL TIE DOWN	0.0	7
2.6	N-WELL OVERLAP OF P+ ACTIVE	3.0	8

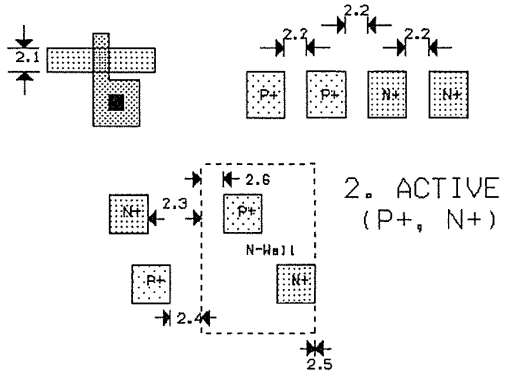
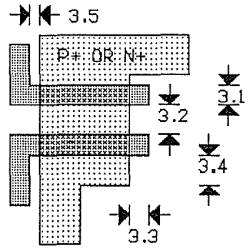


Figure A.9 Active design rules.

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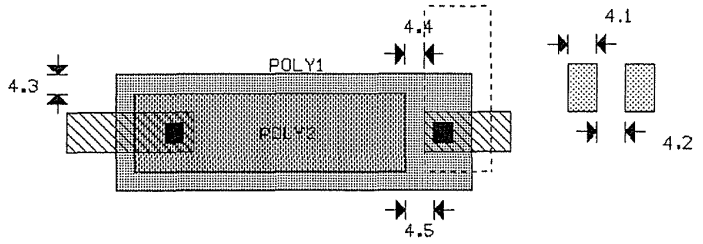
3.1	WIDTH	2.0	9
3.2	SPACE	3.0	10
3.3	GATE OVERLAP OF ACTIVE	2.0	11
3.4	ACTIVE OVERLAP OF GATE	3.0	3
3.5	FIELD POLY1 TO ACTIVE	1.0	not tested



3. POLY1

Figure A.10 Poly1 design rules.

		microns	check#
4.1	WIDTH	3.0	12
4.2	SPACE	3.0	13
4.3	POLY1 OVERLAP OF POLY2	2.0	14
4.4	SPACE TO ACTIVE OR WELL EDGE	2.0	15
4.5	SPACE TO POLY1 CONTACT	3.0	16



4. POLY2

Figure A.11 Poly2 design rules.

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		microns	check#
5.1	CONTACT SIZE (EXACTLY)	2X2	17
5.2	SPACING	2.0	18
5.3	POLY OVERLAP	2.0	19
5.4	ACTIVE OVERLAP	2.0	20
5.5	POLY CONTACT TO ACTIVE EDGE	3.0	21
5.6	ACTIVE CONTACT TO GATE	3.0	22

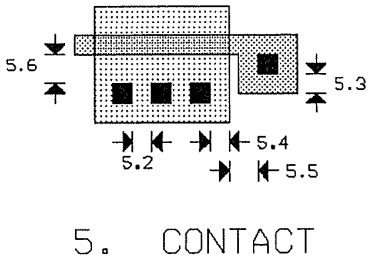


Figure A.12 Contact design rules.

		microns	check#
6.1	WIDTH	3.0	23
6.2	SPACING	3.0	24
6.3	OVERLAP OF CONTACT	1.0	25
6.4	OVERLAP OF VIA	2.0	26

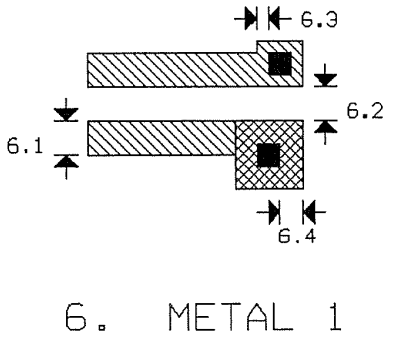
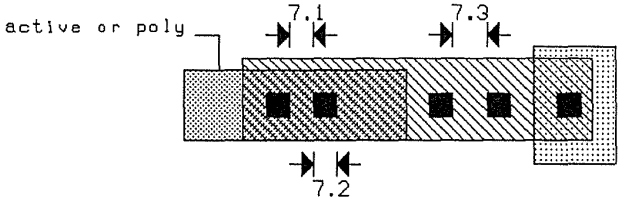


Figure A.13 Metal1 design rules.

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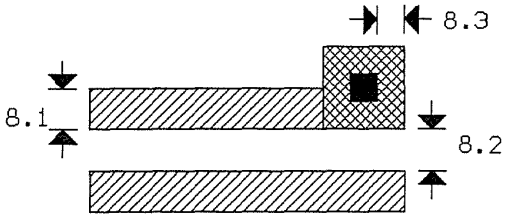
		microns	check#
7.1	SPACE TO CONTACT	2.0	27
7.2	SIZE (EXCEPT FOR PADS)	2.0x2.0	28
7.3	SPACING	3.0	29



7. VIA

Figure A.14 Via design rules.

		microns	check#
8.1	WIDTH	3.0	30
8.2	SPACE	3.0	31
8.3	METAL2 OVERLAP OF VIA	2.0	32

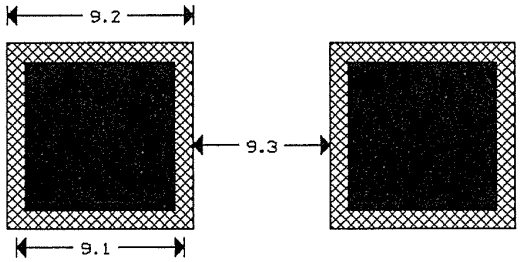


8. METAL 2

Figure A.15 Metal2 design rules.

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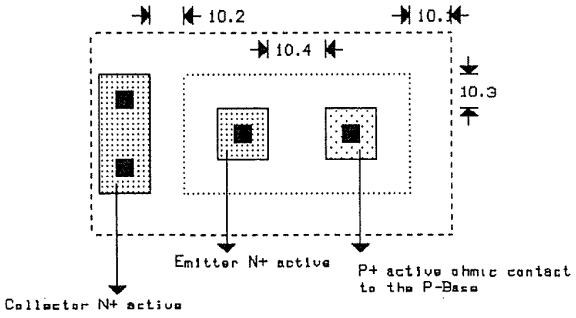
		microns	check#
9.1	MAXIMUM PAD OPENING IN A 100X100 micron METAL PAD (OVERGLASS)	90x90	not tested
9.2	METAL1 AND METAL2 PAD SIZE	100x100	not tested
9.3	MINIMUM PAD METAL TO PAD METAL SEPARATION	75	not tested



9. PAD

Figure A.16 Pad design rules.

		microns	check#
10.1	P-BASE ACTIVE TO N-WELL	5.0	33
10.2	COLLECTOR N+ ACTIVE TO P-BASE ACTIVE	4.0	34
10.3	P-BASE ACTIVE OVERLAP OF N+/P+ ACTIVE	4.0	35
10.4	P+ ACTIVE TO N+ ACTIVE	7.0	36



10. P-BASE

Figure A.17 P-base design rules.

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Appendix

B

MOSIS Scalable Design Rules

This appendix describes graphically the MOSIS Scalable CMOS Design Rules [1]. The design rule check file located in the C:\LASI5\MOSIS directory is called MOSIS.DRC. The MOSIS design rules use a generic measurement parameter λ (labeled "lam" in LASI). Whether the final project is fabricated in a 0.5 μm process or a 2 μm process is transparent to the person doing layout (except for the pads, of course) until the *.TLC files generated with LASI are changed into a *.GDS file with the LASI utility "TLC2GDS.exe" LASI (actually the setups provided with this book) uses 20 internal units to 1 lam. The GDS units per physical unit should always be 1000.

The n+ (p+) layer is drawn using the MOSIS setups with two layers: active and n-select (p-select). For example, if we want an n+ square measuring 10 λ by 10 λ, we draw a box, on the active layer, measuring 10 λ by 10 λ (this defines the openings in the FOX). Around this active box we draw another box on the n-select layer that is at least 2 λ away from the active box. That is, we draw a box on the n-select layer that is at least 14 λ by 14 λ on the same center as the 10 λ by 10 λ active box. The n-select selects the active box as n+ (actually, the n-select layer specifies an n+ implant in the areas defined by the n-select box).

Technology Specification

Reference [1] should be consulted prior to submitting a chip to MOSIS. The technology specification and lambda depend on the process that the chip will be fabricated in. For example, if we were to use the Orbit CN20 process described in Appendix A, we could specify SCNA (Scalable CMOS N-well Analog) as the technology and a lambda of 1.0.

REFERENCE

[1] J-I. Pi, "MOSIS Scalable CMOS Design Rules" *The MOSIS Service,* Information Sciences Institute, University of Southern California, 4676 Admiralty Way, Marina del Rey, CA. 90292, August 1, 1995.

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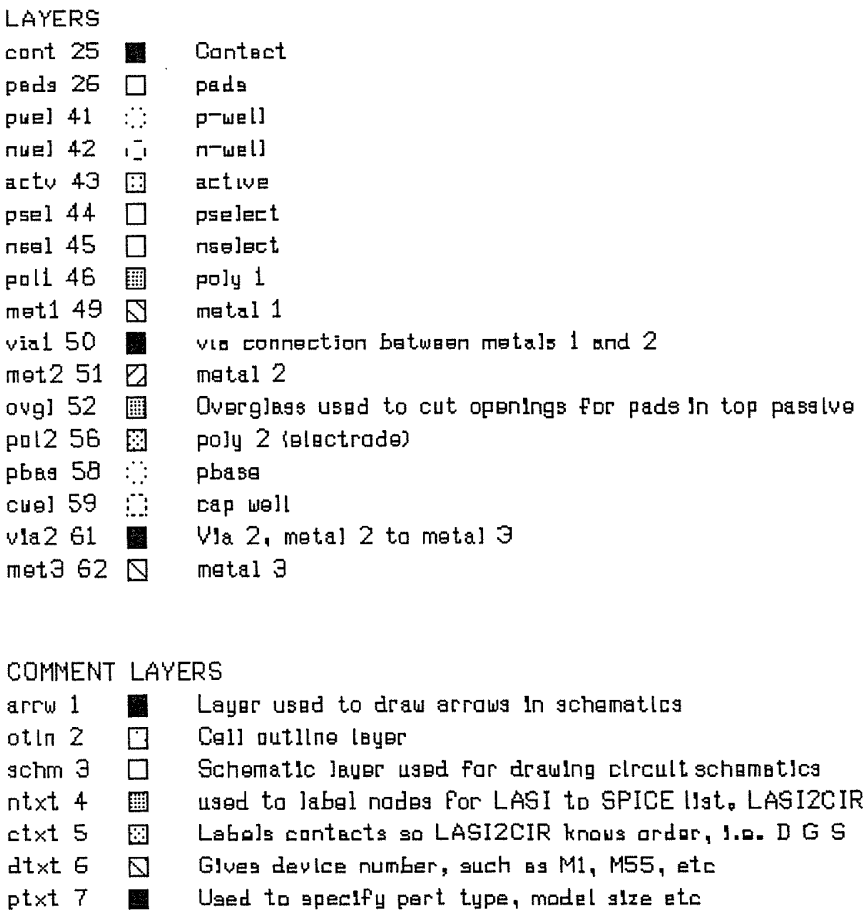


Figure B.1

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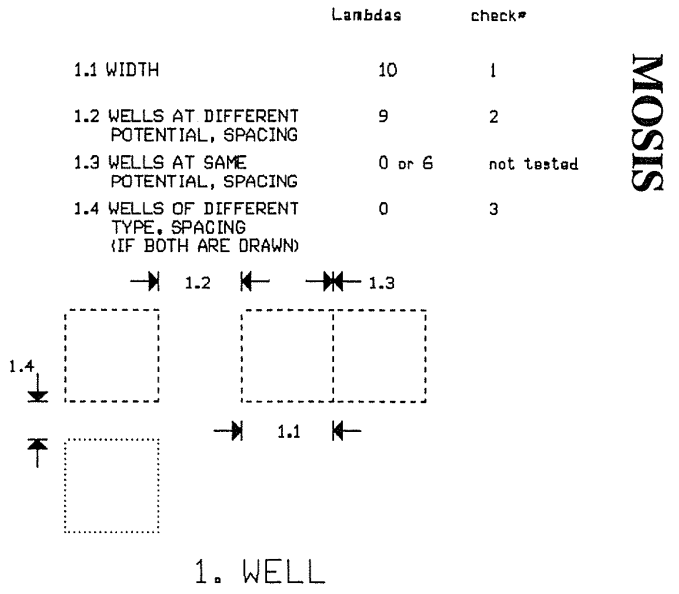


Figure B.2

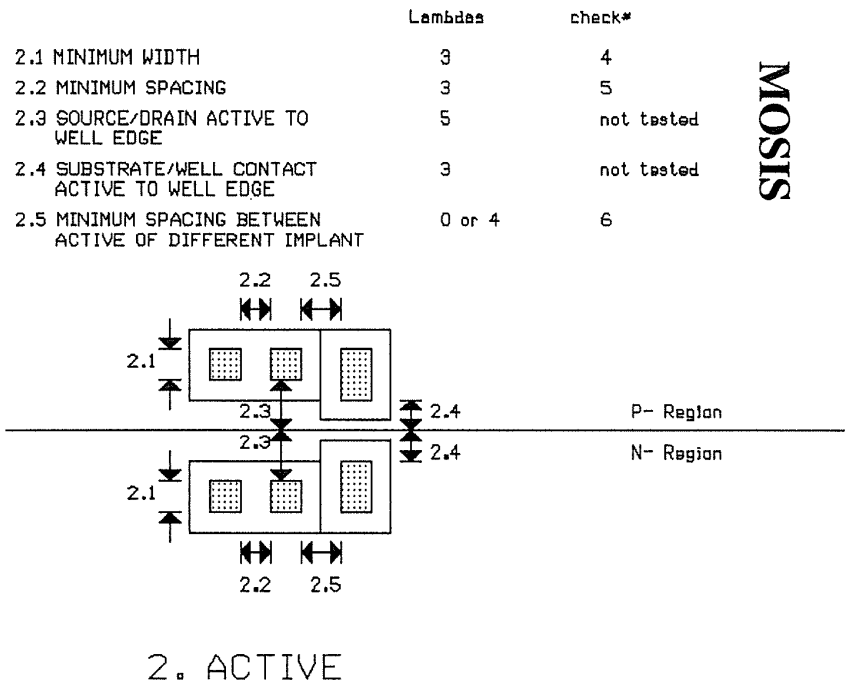


Figure B.3

	Lambdas	check#
3.1 MINIMUM WIDTH	2	7
3.2 MINIMUM SPACING	2	8
3.3 MINIMUM GATE EXTENSION OF ACTIVE	2	9
3.4 MINIMUM ACTIVE EXTENSION OF POLY1	3	4
3.5 MINIMUM FIELD POLY TO ACTIVE	1	not tested

MOSIS

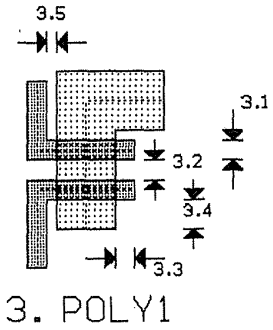


Figure B.4

	Lambdas	check#
4.1 MINIMUM SELECT SPACING TO CHANNEL OF TRANSISTOR TO ENSURE ADEQUATE SOURCE/DRAIN WIDTH	3	not tested
4.2 MINIMUM SELECT OVERLAP OF ACTIVE	2	10
4.3 MINIMUM SELECT OVERLAP OF CONTACT	1	11
4.4 MINIMUM SELECT WIDTH AND SPACING (NOTE: P-select and N-select may be coincident but must not overlap)	2	12

MOSIS

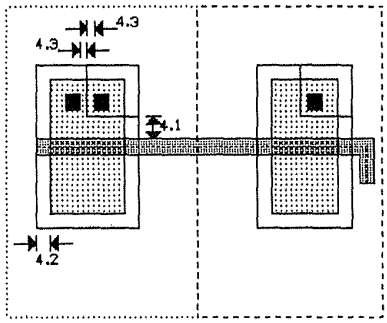
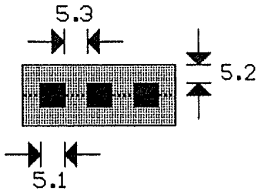


Figure B.5

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	Lambdas	check#
5.1 EXACT CONTACT SIZE	2x2	13
5.2 MINIMUM POLY1 OVERLAP	1.5	14
5.3 MINIMUM CONTACT SPACING	2	15

MOSIS

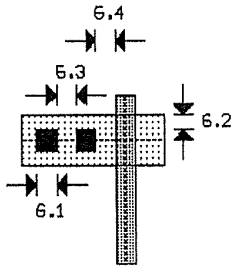


5. CONTACT TO POLY1

Figure B.6

	Lambdas	check#
6.1 EXACT CONTACT SIZE	2x2	13
6.2 MINIMUM ACTIVE OVERLAP	1.5	16
6.3 MINIMUM CONTACT SPACING	2	15
6.4 MINIMUM SPACING TO GATE OF TRANSISTOR	2	17

MOSIS



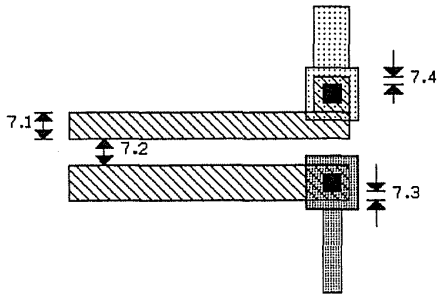
6.CONTACT TO ACTIVE

Figure B.7

Microchip Ex. 1055, p. 899
Microchip v. Aptiv
IPR2024-00228

	Lambdas	check#
7.1 MINIMUM WIDTH	3	18
7.2 MINIMUM SPACING	3	19
7.3 MINIMUM OVERLAP OF POLY CONTACT	1	20
7.4 MINIMUM OVERLAP OF ACTIVE CONTACT	1	20

MOSIS

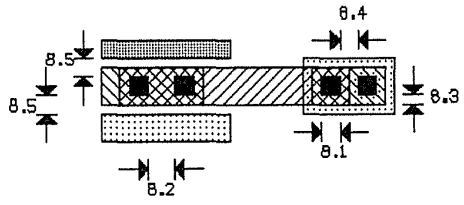


7. METAL1

Figure B.8

	Lambdas	check#
8.1 EXACT SIZE	2x2	21
8.2 MINIMUM VIA1 SPACING	3	22
8.3 MINIMUM OVERLAP BY METAL1	1	23
8.4 MINIMUM SPACING TO CONTACT	2	24
8.5 MINIMUM SPACING TO POLY OR ACTIVE EDGE	2	25

MOSIS



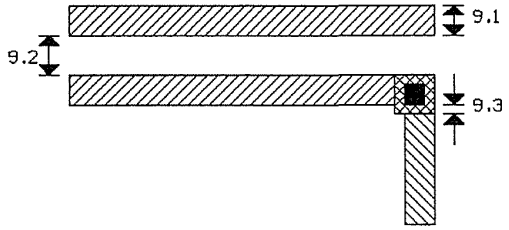
8. VIA1

Figure B.9

Microchip Ex. 1055, p. 900
Microchip v. Aptiv
IPR2024-00228

	Lambdas	check#
9.1 MINIMUM WIDTH	3	26
9.2 MINIMUM SPACING	4	27
9.3 MINIMUM OVERLAP OF VIA1	1	28

MOSIS

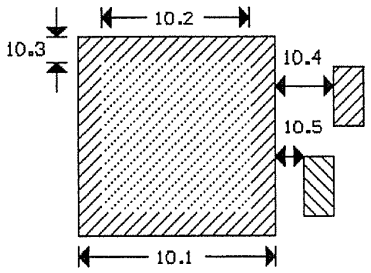


9. METAL2

Figure B.10

	um	check#
10.1 MINIMUM BONDING PAD WIDTH	100x100	not tested
10.2 MINIMUM PROBE PAD WIDTH	75x75	not tested
10.3 PAD OVERLAP OF GLASS OPENING	6	not tested
10.4 MINIMUM PAD SPACING TO UNRELATED METAL2	30	not tested
10.5 MINIMUM PAD SPACING TO UNRELATED METAL1, POLY, ELECTRODE OR ACTIVE	15	not tested

MOSIS



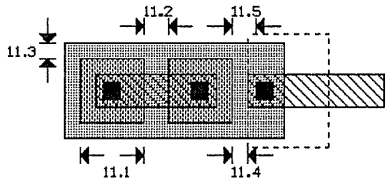
10. OVERGLASS

Figure B.11

Microchip Ex. 1055, p. 901
Microchip v. Aptiv
IPR2024-00228

	Lambdas	check*
11.1 MINIMUM WIDTH	3	not tested
11.2 MINIMUM SPACING	3	29
11.3 MINIMUM POLY1 OVERLAP	2	not tested
11.4 MINIMUM SPACING TO ACTIVE OR WELL EDGE	2	30
11.5 MINIMUM SPACING TO POLY1 CONTACT	3	31.

MOSIS

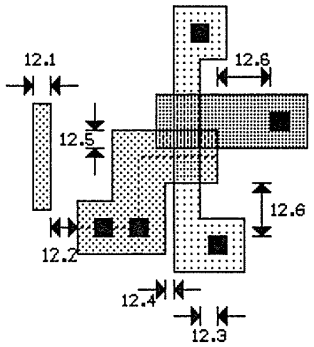


11. POLY2

Figure B.12

	Lambdas	check*
12.1 MINIMUM WIDTH	2	not tested
12.2 MINIMUM SPACING	3	29
12.3 MINIMUM POLY2 GATE OVERLAP OF ACTIVE	2	32
12.4 MINIMUM SPACING TO ACTIVE	1	not tested
12.5 MINIMUM SPACING OR OVERLAP OF POLY1	2	not tested
12.6 MINIMUM SPACING TO POLY1 OR ACTIVE CONTACT	3	31

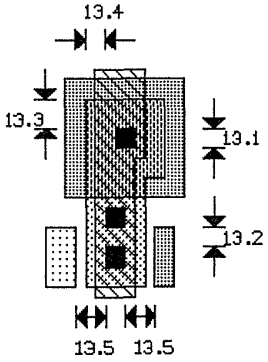
MOSIS



12. ELECTRODE FOR TRANSISTOR

Figure B.13

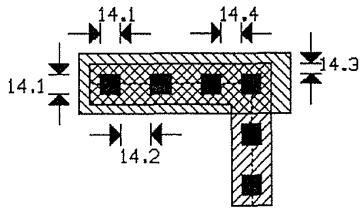
	Lambdas	check*	
13.1 EXACT CONTACT SIZE	2x2	13	
13.2 MINIMUM CONTACT SPACING	2	15	MOSIS
13.3 MINIMUM ELECTRODE OVERLAP (on capacitor)	3	33	
13.4 MINIMUM ELECTRODE OVERLAP (not on capacitor)	2	34	
13.5 MINIMUM SPACING TO POLY1 OR ACTIVE	3	not tested	



13. ELECTRODE CONTACT, ANALOG OPTION

Figure B.14

	Lambdas	check*	
14.1 EXACT SIZE	2x2	35	
14.2 MINIMUM SPACING	3	36	MOSIS
14.3 MINIMUM OVERLAP BY METAL2	1	37	
14.4 MINIMUM SPACING TO VIA1	2	38	

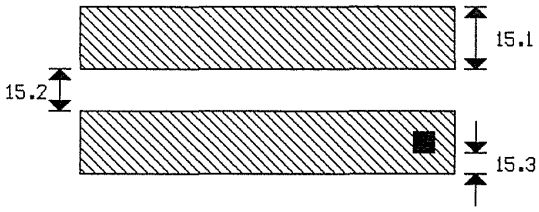


14. VIA2

Figure B.15

	Lambdas	check#
15.1 MINIMUM WIDTH	6	39
15.2 MINIMUM SPACING TO METAL3	4	40
15.3 MINIMUM OVERLAP OF VIA2	2	41

MOSIS

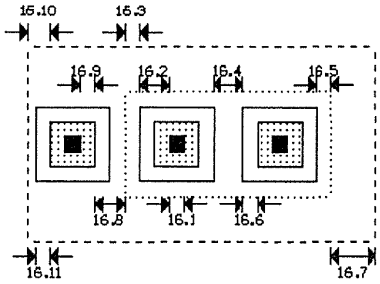


15. METAL3

Figure B.16

	Lambdas	check#
16.1 ALL ACTIVE CONTACT	2x2	13
16.2 MINIMUM SELECT OVERLAP OF EMITTER CONTACT	4	42
16.3 MINIMUM PBASE OVERLAP OF EMITTER SELECT	2	43
16.4 MINIMUM SPACING BETWEEN EMITTER SELECT AND BASE SELECT	4	44
16.5 MINIMUM PBASE OVERLAP OF BASE SELECT	2	45
16.6 MINIMUM SELECT OVERLAP OF BASE CONTACT	2	46
16.7 MINIMUM NWELL OVERLAP OF PBASE	6	47
16.8 MINIMUM SPACING BETWEEN PBASE AND COLLECTOR ACTIVE	4	48
16.9 MINIMUM ACTIVE OVERLAP OF COLLECTOR CONTACT	2	not tested
16.10 MINIMUM NWELL OVERLAP OF COLLECTOR ACTIVE	3	not tested
16.11 MINIMUM SELECT OVERLAP OF COLLECTOR ACTIVE	2	10

MOSIS



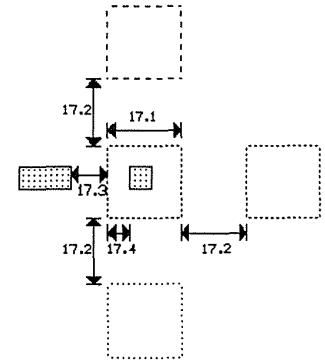
16. NPN BIPOLAR TRANSISTOR

Figure B.17

Microchip Ex. 1055, p. 904
Microchip v. Aptiv
IPR2024-00228

MOSIS

	Lambdas	check*
17.1 MINIMUM WIDTH	10	49
17.2 MINIMUM SPACING	9	50
17.3 MINIMUM SPACING TO EXTERNAL ACTIVE	5	51
17.4 MINIMUM OVERLAP OF ACTIVE	3	52



17. CAPACITOR WELL

Figure B.18

Appendix

C

HP's CMOS14TB

This appendix gives SPICE and process information for Hewlett-Packard's 0.5 μm triple-metal, n-well process (CMOS14TB) which, in addition to the CN20 process described in Appendix A, is used throughout the text. Since this is a triple-metal process, the construction of the pads is somewhat different than that described for the double-metal processes. MOSIS and HP should be contacted for complete up-to-date information (layout and electrical) on this process prior to designing or submitting a chip for fabrication. Tables C1-C4 give basic electrical information for this process.

The MOSIS Scalable Design Rules given in Appendix B can be used for layout with this process. Two different lambdas can be used, 0.3 μm and 0.35 μm. Using a lambda of 0.3 μm results in a minimum device length of 2λ or 0.6 μm, while the minimum width is 3λ or 0.9 μm. If we subtract the lateral diffusion, DL (nominally 0.1 μm), the effective channel length is 0.5 μm. Using the effective channel length when describing CMOS14TB results in a labeling of a "0.5 μm process." Some of the design rules presented in Appendix B must be changed when using a lambda of 0.3 μm. For example, the n-well width, rule 1.1, must be increased from 10 lambdas to 12 lambdas. The technology specified to MOSIS when submitting a chip in the CMOS14TB process using a lambda of 0.3 μm with the modified design rules is "SCN_SUBM" (Scalable-CMOS-N-well Sub-Micron).

To eliminate the need to modify the design rules in Appendix B, lambda can be increased to 0.35 μm. Now the drawn length of a minimum-size device is 0.7 μm. However, at MOSIS, a bias is applied to the poly mask to reduce the size to 0.6 μm. Thus, when simulating a circuit using a minimum length MOSFET, we use 0.6 μm (whether we are using 0.3 or 0.35 μm for lambda), whereas when laying the MOSFET out we use 2λ or 0.7 μm. The major benefit here is that we can use the setups given in Appendix B and on the accompanying disk without modification for laying circuits out in the 0.5 μm CMOS14TB process. The technology specification when using a lambda of 0.35 μm is "SCN."

Microchip Ex. 1055, p. 906
Microchip v. Aptiv
IPR2024-00228

N-channel device L_{drawn} = 0.6 µm	**Typ**
Threshold voltage V_{THN}, (V)	0.7
Gamma ($V^{1/2}$)	0.6
KP = $(MUZ)(C'_{ox})$ ($\mu A/V^2$)	170
DL ($L_{eff} = L_{drawn}$ – DL) (µm)	0.06
DW ($W_{eff} = W_{drawn}$ – DW) (µm)	0.35
Punchthrough voltage (V)	10
I_{drive} (µA/µm)	380

Table C.1

P-channel device L_{drawn} = 0.6 µm	**Typ**
Threshold voltage V_{THP}, (V)	0.9
Gamma ($V^{1/2}$)	0.5
KP = $(MUZ)(C'_{ox})$ ($\mu A/V^2$)	50
DL ($L_{eff} = L_{drawn}$ – DL) (µm)	0.09
DW ($W_{eff} = W_{drawn}$ – DW) (µm)	0.35
Punchthrough voltage (V)	10
I_{drive} (µA/µm)	190

Table C.2

Sheet resistance (Ω/square)	**Typ**
P+ active	2
N+ active	2
Poly1 (silicided)	2
Metal1	0.07
Metal2	0.07
Metal3	0.05

Table C.3

Microchip Ex. 1055, p. 907
Microchip v. Aptiv
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	Plate Cap. aF/μm² Typical
Poly1 to subs. (FOX)	91
Poly1 to metal1	58
Poly1 to metal2	17
Poly1 to metal3	10
Metal1 to substrate	42
Metal1 to metal2	36
Metal1 to metal3	14
Metal2 to substrate	20
Metal2 to metal3	33
Metal3 to substrate	15

Table C.4

Calculation of V_{THN} and KP_n Using the BSIM Model Parameters

The level 3 and 4 (BSIM) model parameters for the n-channel MOSFET are shown below and are located in the text file **spice.inf** in the C:\LASI5\CN20 directory.

```
* Level 3 SPICE model for CMOS14TB 0.5 um
.MODEL CMOSN5 NMOS LEVEL=3 PHI=0.700000
+ TOX=9.6000E-09 XJ=0.200000U TPG=1
+ VTO=0.7118 DELTA=2.3060E-01 LD=2.9830E-08 KP=1.8201E-04
+ UO=506.0 THETA=1.9090E-01 RSH=1.8940E+01 GAMMA=0.6051
+ NSUB=1.4270E+17 NFS=7.1500E+11 VMAX=2.4960E+05 ETA=2.5510E-02
+ KAPPA=1.8530E-01 CGDO=9.0000E-11 CGSO=9.0000E-11
+ CGBO=3.7295E-10 CJ=6.02E-04 MJ=0.805 CJSW=2.0E-11
+ MJSW=0.761 PB=0.99
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 3.5700E-07

* Level 4 (BSIM) SPICE model for CMOS14TB 0.5 um
.MODEL CMOSNB5 NMOS LEVEL=4
+ vfb=-9.65360E-01    lvfb= 4.11254E-02    wvfb=-1.21737E-01
+ phi= 9.02436E-01    lphi= 0.00000E+00    wphi= 0.00000E+00
+ k1=  9.33674E-01    lk1= -8.15872E-02    wk1=  2.03526E-01
+ k2=  7.39228E-02    lk2=  1.48295E-02    wk2=  5.89097E-02
+ eta=-2.77969E-03    leta= 1.12296E-02    weta= 1.25263E-03
+ muz= 4.71133E+02    dl=   1.57937E-001   dw=   4.09563E-001
+ u0=  1.98427E-01    lu0=  1.54850E-01    wu0= -1.05429E-01
+ u1=  3.39403E-02    lu1=  3.59469E-02    wu1= -5.00497E-03
+ x2mz=1.25728E+01    lx2mz=-1.24115E+01   wx2mz=1.77657E+01
+ x2e=-9.95217E-05    lx2e=-5.16949E-03    wx2e= 2.83253E-03
```

Microchip Ex. 1055, p. 908
Microchip v. Aptiv
IPR2024-00228

```
+ x3e=-4.27269E-04    lx3e=-1.62632E-03    wx3e=-1.60797E-03
+ x2u0=-9.02747E-04   lx2u0=-1.66946E-02   wx2u0=2.48458E-02
+ x2u1=-7.29822E-04   lx2u1=2.38803E-03    wx2u1=-9.76918E-04
+ mus=5.36631E+02     lmus=2.18647E+01     wmus=4.43373E+00
+ x2ms=5.97403E+00    lx2ms=-7.67105E+00   wx2ms=2.19614E+01
+ x3ms=7.60054E+00    lx3ms=4.73779E+00    wx3ms=2.59952E+00
+ x3u1=1.75532E-02    lx3u1=-1.21628E-03   wx3u1=-5.95548E-04
+ tox=9.60000E-003    temp=2.70000E+01     vdd=3.30000E+00
+ cgdo=4.26077E-010   cgso=4.26077E-010    cgbo=4.01709E-010
+ xpart=1.00000E+000
+ n0=1.00000E+000     ln0=0.00000E+000     wn0=0.00000E+000
+ nb=0.00000E+000     lnb=0.00000E+000     wnb=0.00000E+000
+ nd=0.00000E+000     lnd=0.00000E+000     wnd=0.00000E+000
+ rsh=2   cj=6.02e-04   cjsw=2.0e-11   js=1e-08  pb=0.99
+ pbsw=0.99   mj=0.805   mjsw=0.761   wdf=0   dell=0
```

The threshold voltage of the n-channel MOSFET, V_{THN}, as a function of the source to substrate potential, V_{SB}, using the BSIM model parameters, is given by

$$V_{THN} = VFB + PHI + K1 \cdot \sqrt{PHI + V_{SB}} - K2 \cdot (PHI + V_{SB}) \tag{C.1}$$

or using the values given in the BSIM model above

$$= -0.97 + 0.9 + 0.93 \cdot \sqrt{0.9 + V_{SB}} - 0.0074 \cdot (0.9 + V_{SB}) \tag{C.2}$$

If $V_{SB} = 0$, then

$$V_{THN} = 0.80 \text{ V} \tag{C.3}$$

The oxide capacitance per unit area using the oxide thickness from the BSIM model parameters is given by

$$C'_{ox} = \frac{\varepsilon_{ox}}{TOX} = \frac{35.13 \text{ fF/}\mu\text{m}}{0.0096 \ \mu\text{m}} \approx 3.7 \ \frac{\text{fF}}{\mu\text{m}^2} \tag{C.4}$$

The transconductance parameter, KP_n, for the n-channel MOSFET is then approximated by

$$KP_n = MUZ \cdot C'_{ox} = \frac{471 \text{ cm}^2}{\text{V} \cdot \text{s}} \cdot \frac{10^8 \mu\text{m}^2}{\text{cm}^2} \cdot \frac{3.7 \text{ fF}}{\mu\text{m}^2} \approx 174 \ \frac{\mu\text{A}}{\text{V}^2} \tag{C.5}$$

The effective-digital resistance of the n-channel MOSFET in CMOS14TB is given by

$$R_n = R'_n \cdot \frac{1}{W} = \frac{VDD}{I_{drive} \cdot W} = \frac{3.3 \text{ V} \cdot \mu\text{m}}{380 \ \mu\text{A}} \cdot \frac{1}{W} \approx \frac{9 \text{ k}\Omega \cdot \mu\text{m}}{W} \tag{C.6}$$

For a minimum-size device (i.e., 0.9/0.6), the effective resistance of the MOSFET is 10 kΩ. The process characteristic time constant for the n-channel MOSFET, using L_{drawn} is,

$$\tau_n = R_n C_{ox} = R'_n \cdot L \cdot C'_{ox} = 9 \text{ k}\Omega \cdot (0.6) \cdot (3.7 \text{ fF}) = 20 \text{ ps} \tag{C.7}$$

Microchip Ex. 1055, p. 909
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Calculation of V_{THP} and KP_p Using the BSIM Model Parameters

The level 3 and 4 (BSIM) model parameters for the n-channel MOSFET are shown below and are located in the text file **spice.inf** in the C:\LASI5\CN20 directory.

```
* Level 3 SPICE model for CMOS14TB 0.5 um
.MODEL CMOSP5 PMOS LEVEL=3 PHI=0.700000
+ TOX=9.6000E-09 XJ=0.200000U TPG=-1
+ VTO=-0.9016 DELTA=4.2020E-01 LD=4.3860E-08 KP=4.1582E-05
+ UO=115.6 THETA=3.7990E-02 RSH=9.0910E-02 GAMMA=0.4496
+ NSUB=7.8780E+16 NFS=6.4990E+11 VMAX=2.3130E+05 ETA=2.8580E-02
+ KAPPA=9.9270E+00 CGDO=9.0000E-11 CGSO=9.0000E-11
+ CGBO=3.6835E-10 CJ=9.34E-04 MJ=0.491 CJSW=2.41E-10
+ MJSW=0.222 PB=0.90
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 3.4860E-07


* Level 4 (BSIM) SPICE model for CMOS14TB 0.5 um
.MODEL CMOSPB5 PMOS LEVEL=4
+ vfb=-2.80568E-01    lvfb=5.70163E-02     wvfb=-6.17493E-02
+ phi=8.14689E-01     lphi=0.00000E+00     wphi=0.00000E+00
+ k1=4.52973E-01      lk1=-9.19899E-02     wk1=1.20834E-01
+ k2=-9.42157E-03     lk2=-2.25562E-03     wk2=3.13315E-02
+ eta=-7.03956E-03    leta=1.92833E-02     weta=5.45445E-05
+ muz=1.36047E+02     dl=1.85988E-001      dw=4.32366E-001
+ u0=1.93813E-01      lu0=6.02231E-02      wu0=-4.90734E-02
+ u1=8.52399E-03      lu1=2.60545E-02      wu1=-6.34371E-03
+ x2mz=7.96258E+00    lx2mz=-2.15761E+00   wx2mz=2.30663E+00
+ x2e=4.37912E-04     lx2e=-1.60046E-03    wx2e=-3.86750E-04
+ x3e=-3.52725E-04    lx3e=-4.09096E-04    wx3e=-2.53471E-03
+ x2u0=1.18873E-02    lx2u0=-4.81760E-03   wx2u0=8.80040E-03
+ x2u1=2.26591E-03    lx2u1=7.96828E-04    wx2u1=-4.70527E-04
+ mus=1.44421E+02     lmus=1.63665E+01     wmus=-7.31189E-01
+ x2ms=8.18970E+00    lx2ms=-1.25158E+00   wx2ms=3.62233E+00
+ x3ms=7.29640E-01    lx3ms=1.15206E+00    wx3ms=1.02833E+00
+ x3u1=-3.51521E-03   lx3u1=-3.12374E-03   wx3u1=3.48134E-03
+ tox=9.60000E-003    temp=2.70000E+01     vdd=3.30000E+00
+ cgdo=5.01753E-010   cgso=5.01753E-010    cgbo=4.14187E-010
+ xpart=1.00000E+000
+ n0=1.00000E+000     ln0=0.00000E+000     wn0=0.00000E+000
+ nb=0.00000E+000     lnb=0.00000E+000     wnb=0.00000E+000
+ nd=0.00000E+000     lnd=0.00000E+000     wnd=0.00000E+000
+ rsh=2.1   cj=9.34e-04   cjsw=2.41e-10   js=1e-08   pb=0.90
+ pbsw=0.90   mj=0.491   mjsw=0.222   wdf=0   dell=0
```

The threshold voltage of the p-channel MOSFET is calculated using

$$V_{THP} = VFB + PHI + K1 \cdot \sqrt{PHI + V_{BS}} - K2 \cdot (PHI + V_{BS}) \qquad \text{(C.8)}$$

or using the p-channel MOSFET BSIM model parameters of the previous section

$$= -0.28 + 0.81 + 0.45 \cdot \sqrt{0.81 + V_{BS}} - (-0.0094) \cdot (0.81 + V_{BS}) \qquad \text{(C.9)}$$

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If $V_{BS} = 0$, then

$$V_{THP} \approx 0.94 \text{ V} \tag{C.10}$$

The transconductance parameter, KP_p, for the p-channel MOSFET is given by

$$KP_p = MUZ \cdot C'_{ox} = \frac{136 \text{ cm}^2}{\text{V} \cdot \text{s}} \cdot \frac{10^8 \mu\text{m}^2}{\text{cm}^2} \cdot \frac{3.7 \text{ fF}}{\mu\text{m}^2} \approx 50 \frac{\mu\text{A}}{\text{V}^2} \tag{C.11}$$

The effective digital resistance of the p-channel MOSFET in CMOS14TB is given by

$$R_p = R'_p \cdot \frac{1}{W} = \frac{VDD}{I_{drive} \cdot W} = \frac{3.3 \text{ V} \cdot \mu\text{m}}{190 \mu\text{A}} \cdot \frac{1}{W} \approx \frac{18 \text{ k}\Omega \cdot \mu\text{m}}{W} \tag{C.12}$$

The process characteristic time constant for the p-channel MOSFET is,

$$\tau_p = R_p \cdot C_{ox} = R'_p \cdot L \cdot C'_{ox} = 18 \text{ k}\Omega \cdot (0.6) \cdot (3.7 \text{ fF}) = 40 \text{ ps} . \tag{C.13}$$

SPICE Simulation Results

Figure C.1 shows a plot, for a minimum-size n-channel MOSFET 0.9/0.6, of the drain current versus MOSFET V_{DS} using the BSIM (level 4) and level 3 models. Note how the level 3 model shows the drain current changing as the square of the gate-source voltage, while the BSIM model shows the drain current changing linearly with V_{GS}. This difference is due to the short-channel effects as was discussed in Ch. 6. The drive current of the n-channel MOSFET can be estimated using the data in this plot by

$$I_{drive} = \frac{I_D(@ \ VDD)}{W_{eff}} = \frac{200 \mu\text{A}}{0.9 - 0.4} = 400 \frac{\mu\text{A}}{\mu\text{m}} \tag{C.14}$$

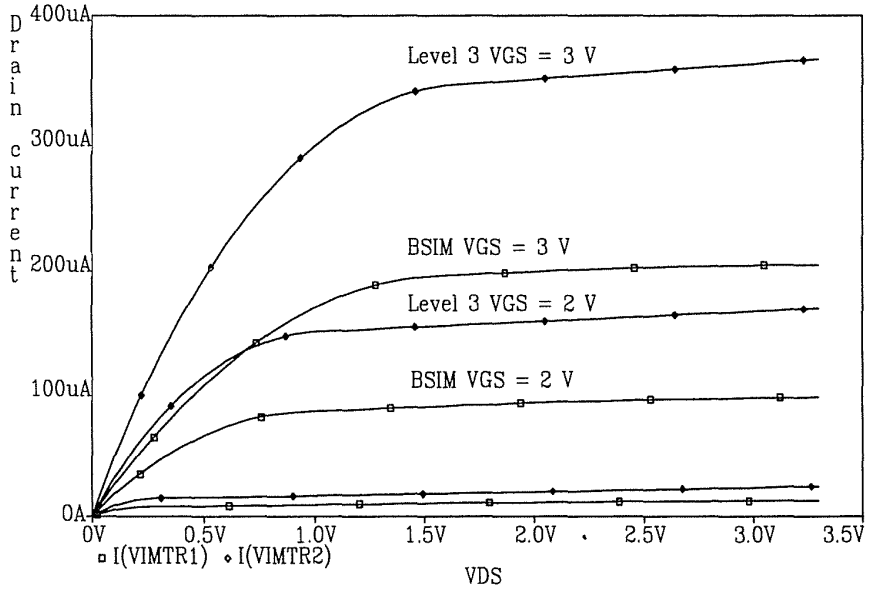


Figure C.1 Curves for a 0.9/0.6 n-channel MOSFET fabricated in CMOS14TB.

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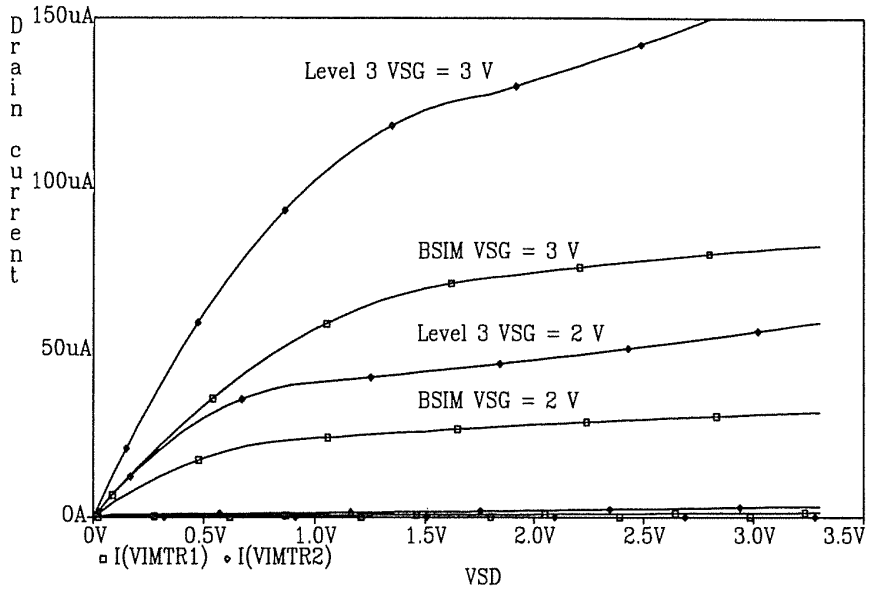


Figure C.2 Curves for a 0.9/0.6 p-channel MOSFET fabricated in CMOS14TB.

Figure C.2 shows the IV characteristics of a minimum-size p-channel MOSFET. The drive current can be estimated using these results as

$$I_{drive} = \frac{I_D(@\ VDD)}{W_{eff}} = \frac{80\ \mu A}{0.9 - 0.43} = 170\frac{\mu A}{\mu m} \tag{C.15}$$

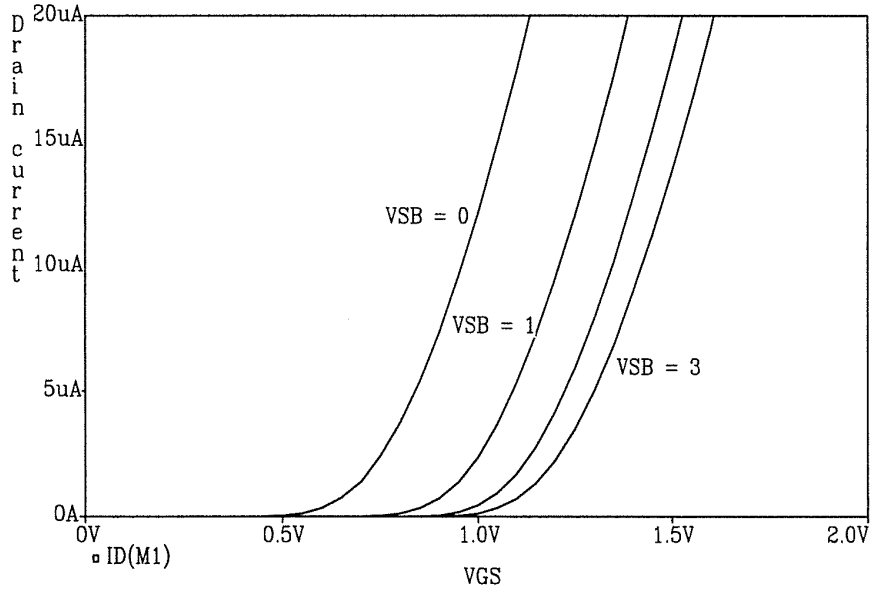


Figure C.3 Curves for a 0.9/0.6 n-channel MOSFET fabricated in the CMOS14TB process.

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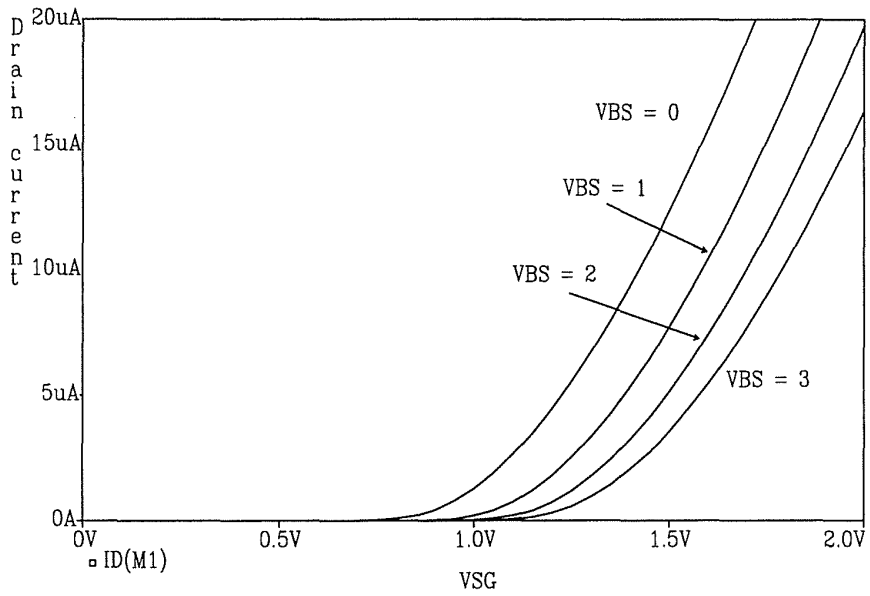


Figure C.4 Curves for a 0.9/0.6 p-channel MOSFET fabricated in the CMOS14TB process.

Figures C.3 and C.4 show how the body effect changes the threshold voltage of the MOSFETs in the CMOS14TB process with substrate(well)/source nonzero voltage.

Planarization

Another important characteristic of the modern Deep-Submicron MOSFET[1] is that planarization can be used to "flatten and level" the tops of the differing insulating layers in the CMOS process. Chemical/mechanical polishing (CMP) is used for planarization. The result is less variation between insulating layers and higher reliability. To help with the planarization process, contacts and vias can be filled with metal (Fig. C.5). This increases the reliability of the connections and reduces contact resistance.

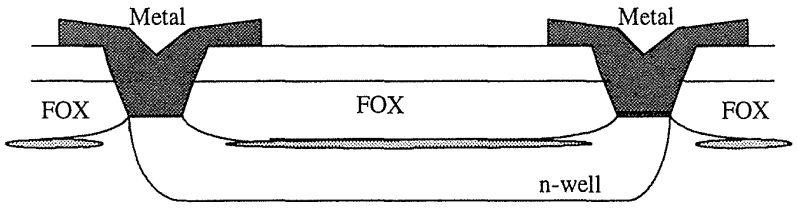


Figure C.5 Fig. 2.10 redrawn with filled contacts.

[1] "Deep" refers to the use of a deep ultra-violet light source with a wavelength, λ, less than 0.3 μm in conjunction with patterning (see Fig. 2.3).

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LASI Software

If a floppy disk is not included with this text, the LASI software can be downloaded from the Internet at:

http://www.mrc.uidaho.edu/vlsi/cad_free.html

Hardware Requirements

LASI software will run in some configuration on almost any IBM compatible computer with a 386 or higher. You need 4 Mbytes of memory, a hard disk drive, VGA video, and a mouse. For small to medium layouts, a 386 or 486 CPU will be adequate. For larger layouts, a Pentium with PCI bus is recommended.

Software Contents and Installation

Whether downloaded from the Internet, or on floppy disk, you should have the following files:

- 2INSTALL.EXE: Installation program.
- LASI52?.ZIP: Main LASI system files. ("?" indicates revision number)
- CN20.ZIP: Setups for Orbit's CN20 process using the Foresight design rules. Information is given in Appendix A.
- MOSIS.ZIP: Setups using the MOSIS Scalable Design Rules in terms of λ. Information is given in Appendix B.
- 2UCHIP.ZIP: An example of chip design (layouts and schematics) using the MOSIS Scalable Design Rules with $\lambda = 1$ μm.

If not on a floppy disk already, copy the above files to a 1.44MB floppy disk. At the DOS command prompt C:\>, type: "a:2install". Assuming LASI is to be installed on the C: drive, specify the hard drive as "C" and answer "Y" to all questions. The LASI tutorial will run when the installation is complete. If the tutorial runs, LASI is probably installed correctly. Reboot after you quit the tutorial. To run LASI on any of the sample layouts, go to Chapter 1 of the text and follow the instructions in Section 1.2 "Using the LASI Program." This will give you the fundamentals of how to work with LASI.

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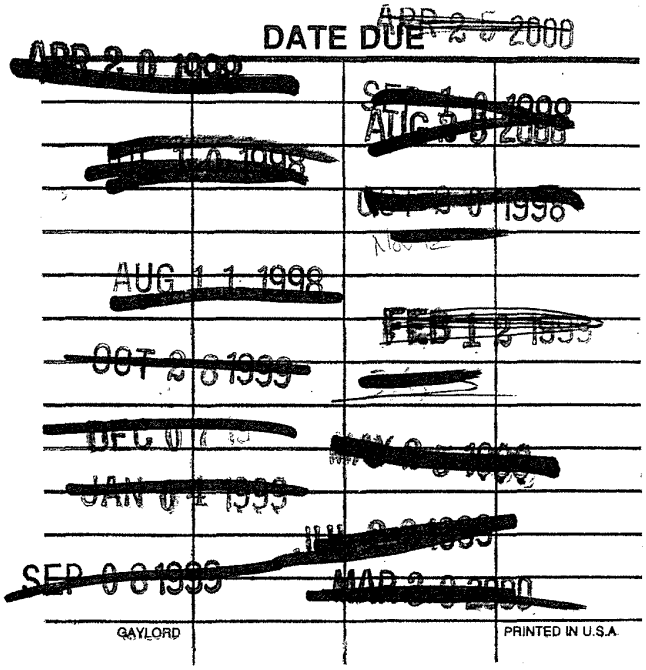
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About the Authors

R. Jacob Baker is Assistant Professor of Electrical Engineering and Assistant Director of the Microelectronics Research Center at the University of Idaho. He teaches several courses on CMOS analog and digital circuit design and has consulted internationally in these areas. With eight years of industry experience at E. G. & G. Energy Measurements, Lawrence Livermore National Laboratory, and Micron Semiconductor, Dr. Baker brings an industrial perspective into the classroom and was selected as the College of Engineering's Outstanding Young Faculty in 1997.

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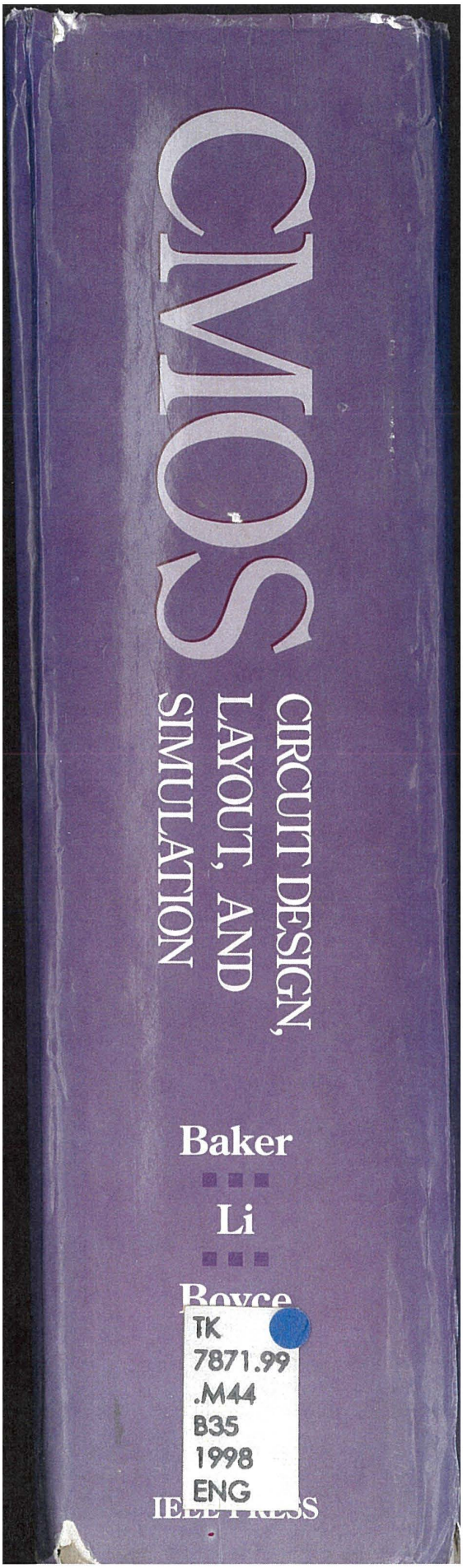
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