USB4916

USB 2.0 Hi-Speed Multi-Host Endpoint Reflector

Highlights

- USB 2.0 Hi-Speed hub
  - 1 upstream port for USB Host connection
  - 4 downstream ports with dual role (host/device) physical interfaces
  - 1 non-removable port for cascading hubs or attaching card reader devices
- Patented Multi-Host Endpoint Reflector
- Device features to enable smart phone automotive sessions with head unit display
- USB Battery Charging, revision 1.2, support on downstream ports (DCP, CDP, SDP)
- Battery charging support for China and Apple® profiles
- USB to SMBus, I^2S™, SPI, UART, and GPIO
  - Apple authentication support
  - I^2S for audio support; Asynchronous In, Adaptive Out, 48KHz, two channels, 16-bits/channel
  - Flexible I^2S capabilities with firmware update

Target Applications

- Media hubs
- Infotainment head units
- Automotive breakout boxes
- Aftermarket automotive products
  - GPS systems
  - Infotainment systems
  - Advanced instrumentations and controls
- Multi-function USB peripherals
- Embedded automotive systems
- Host to Host applications via Ethernet / NCM communication

Product Features

- **MultiTRAK™**
  - Dedicated Transaction Translator per port
- **PortMap**
  - Configurable port mapping and disable sequencing
- **PortSwap**
  - Configurable differential intra-pair signal swapping
- **PHYBoost**
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense™**
  - Programmable USB receiver sensitivity
- USB Link Power Management (LPM) support
- Vendor Specific Messaging (VSM) support
- Architected for USB Power Delivery (PD) 3.0 support
  - 32-bit embedded microcontroller in the hub executes PD stack and system policy manager
  - Interfaces to Microchip UPD350 Power Delivery Interface device
  - Power delivery stack runs from external SPI Flash
  - SPI Flash provides flexibility for specification revisions and evolving system needs
- Enhanced OEM configuration options available through external straps, OTP configuration or SMBus Slave port
- 3.3 V supply voltage
- AEC-Q100 compliance
  - Microchip parts are tested to meet or exceed the requirements of the AEC-Q100 automotive qualification standards
- Packaging
  - 64-pin VQFN (9 x 9 mm)
  - 64-pin Wettable Flanks VQFN (9 x 9 mm)
- Environmental
  - Grade 3 automotive temperature range (-40°C to +85°C)

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
ADC	Analog-to-Digital Converter
Byte	8 bits
CDC	Communication Device Class
EOP	End of Packet
EP	Endpoint
FIFO	First In First Out buffer
FS	Full-Speed
GPIO	General Purpose I/O
HS	Hi-Speed
Hub Feature Controller	The Hub Feature Controller, sometimes called a Hub Controller for short is the internal processor used to enable the unique features of the USB Controller Hub. This is not to be confused with the USB Hub Controller that is used to communicate the hub status back to the Host during a USB session.
I^2C	Inter-Integrated Circuit
LS	Low-Speed
lsb	Least Significant Bit
LSB	Least Significant Byte
msb	Most Significant Bit
MSB	Most Significant Byte
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase Lock Loop
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SDK	Software Development Kit
SMBus	System Management Bus
UUID	Universally Unique IDentifier
WORD	16 bits

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1.2 Buffer Types

TABLE 1-2: BUFFER TYPE DESCRIPTIONS

Buffer	Description
I	Input.
IS	Input with Schmitt trigger.
O4	Output buffer with 4mA sink and 4mA source.
O12	Output buffer with 12mA sink and 12mA source.
OD12	Open-drain output with 12mA sink.
PU	Internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	Internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
ICLK	Crystal oscillator input pin.
OCLK	Crystal oscillator output pin.
I/O-U	Analog input/output defined in USB specification.
I-R	RBIAS.
A	Analog.
P	Power pin.

1.3 Pin Reset States

The pin reset state definitions are detailed in Table 1-3. Refer to Section 3.0, "Pin Descriptions and Configuration" for details on individual pin reset states.

TABLE 1-3: PIN RESET STATE LEGEND

Symbol	Description
A/P	Analog/Power Input
Z	Hardware disables output driver (high impedance)
PD-15k	Hardware enables internal 15kΩ pull-down
PD-67k	Hardware enables internal 67kΩ pull-down
PU-67k	Hardware enables internal 67kΩ pull-up
USB	USB line

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1.4 Reference Documents

1. *Universal Serial Bus Revision 2.0 Specification*, http://www.usb.org
2. AN2374 - USB491x Multi-Host Endpoint Reflector Operation, http://www.microchip.com
3. *AN2439 - Configuration of the USB491x/USB492x/USB4715*, http://www.microchip.com
4. *USB4916 Atlantis Design Tutorial*, http://www.microchip.com
5. *AN2437 - USB to GPIO Bridging with USB4715 and USB49xx*, http://www.microchip.com
6. *AN2438 - USB to I^2C Bridging with USB4715 and USB49xx*, http://www.microchip.com
7. *AN2430 - USB to SPI Bridging with USB4715 and USB49xx*, http://www.microchip.com
8. *AN2426 - USB to UART Bridging with Microchip USB4715, USB4916, and USB4927*, http://www.microchip.com
9. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
10. *I^2C-Bus Specification*, Version 1.1, http://www.nxp.com/documents/user_manual/UM10204.pdf
11. *I^2S-Bus Specification*, http://www.nxp.com/acrobat_download/various/I2SBUS.pdf
12. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

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2.0 INTRODUCTION

2.1 General Description

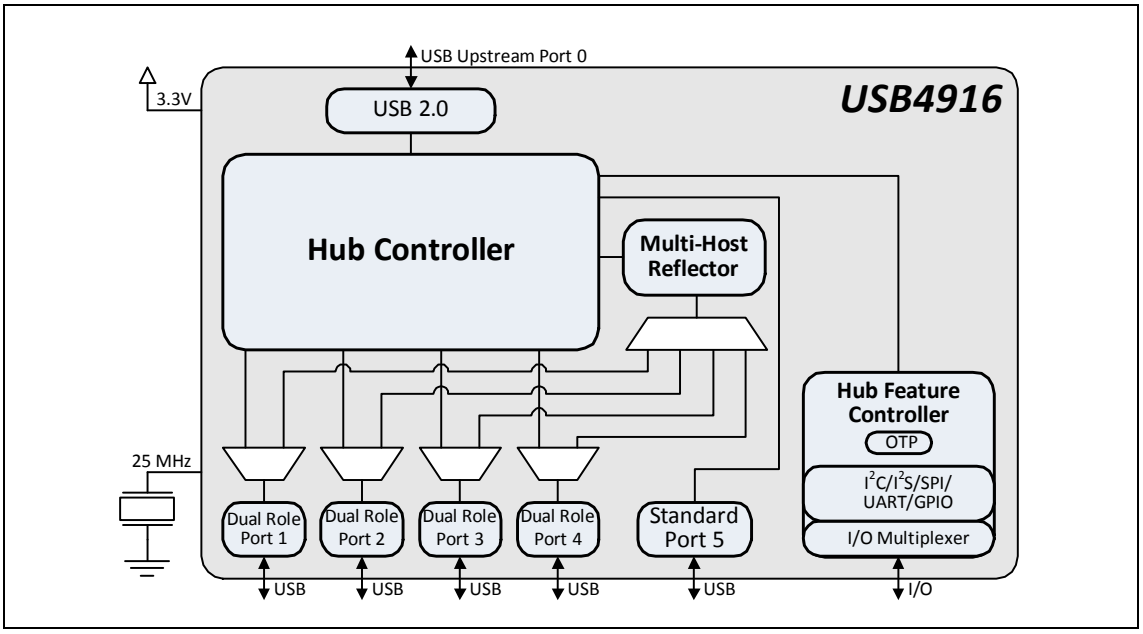
The Microchip USB4916 Multi-Host Endpoint Reflector is an automotive grade, single-chip device targeted for media hub (e.g., break-out-boxes) applications in the car. Primary functions of the device include: multiple downstream USB ports supporting USB 2.0 Low Speed/Full Speed/Hi-Speed, single USB 2.0 Hi-Speed upstream connection to a USB host, battery charging support for BC1.2, Apple and China charging profiles, USB I/O bridging, and an on-chip micro-controller.

The device employs unique USB functionality, whereby USB data can be “mirrored” between two USB hosts (Multi-Host) in order to perform a single USB transaction. This capability is fully covered by Microchip intellectual property (U.S. Pat. Nos. 7,523,243 and 7,627,708) and is instrumental in enabling Apple CarPlay functionality, where the Apple iPhone® becomes a USB Host.

For overall functionality, standard USB drivers are targeted in conjunction with CDC/NCM class drivers. The Multi-Host Endpoint Reflector is considered a USB hub controller that is integrated in conjunction with an embedded USB 2.0 Hi-Speed Hub and USB 2.0 dual role function physical interfaces.

An internal block diagram of the USB4916 is shown in Figure 2-1.

FIGURE 2-1: INTERNAL BLOCK DIAGRAM



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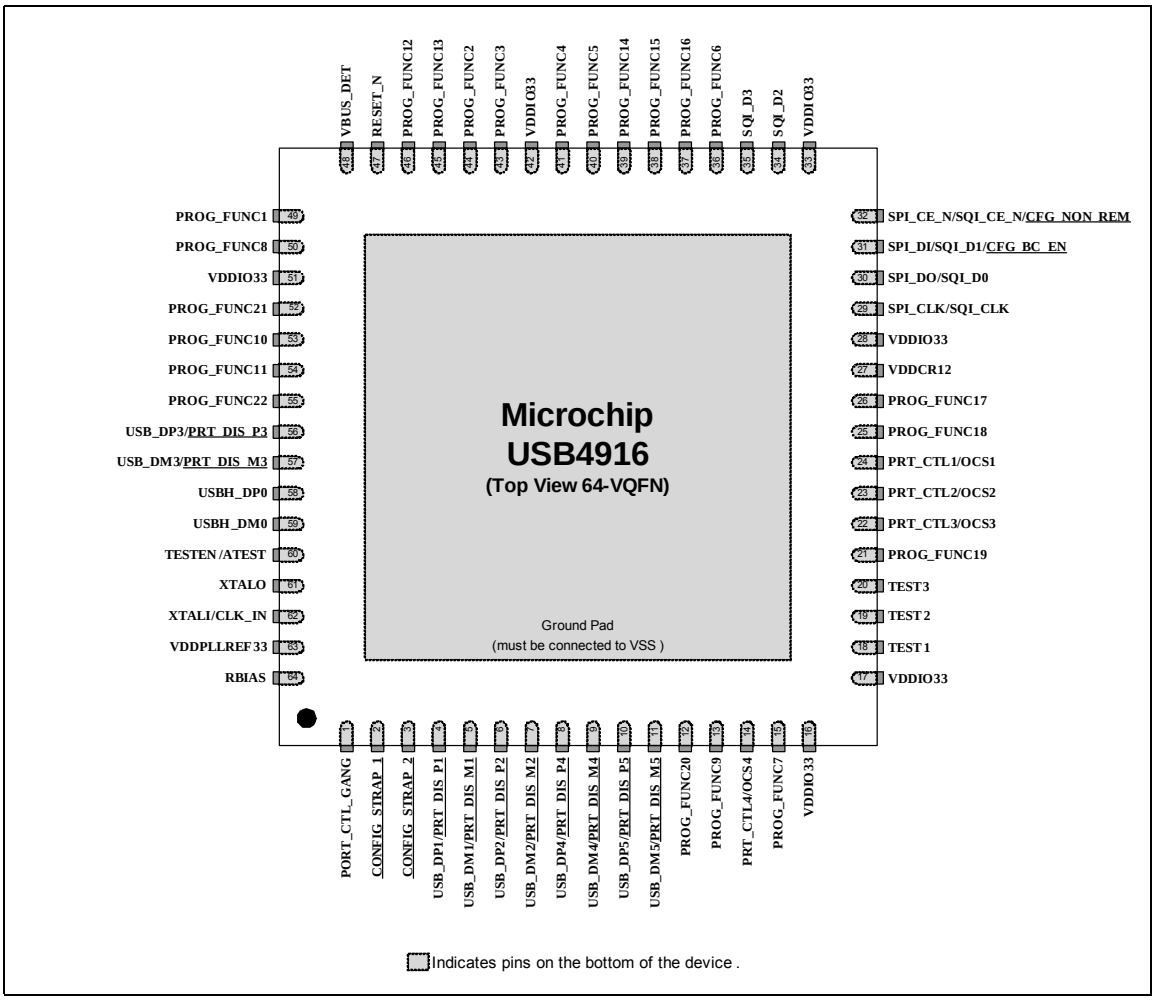
3.0 PIN DESCRIPTIONS AND CONFIGURATION

The pin assignments for the USB4916 are detailed in Section 3.1, "USB4916 Pin Assignments". Pin descriptions are provided in Section 3.2, "Pin Descriptions".

3.1 USB4916 Pin Assignments

The device pin diagram for the USB4916 can be seen in Figure 3-1. Table 3-1 provides a USB4916 pin assignments table. Pin descriptions are provided in Section 3.2, "Pin Descriptions".

FIGURE 3-1: USB4916 PIN ASSIGNMENTS



Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

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TABLE 3-1: USB4916 PIN ASSIGNMENTS

Pin	Pin Name	Reset	Pin	Pin Name	Reset
1	PORT_CTL_GANG	Z	33	VDDIO33	A/P
2	CONFIG_STRAP_1	Z	34	SQI_D2	Z
3	CONFIG_STRAP_2	Z	35	SQI_D3	Z
4	USB_DP1/PRT_DIS_P1	PD-15k	36	PROG_FUNC6	Z
5	USB_DM1/PRT_DIS_M1	PD-15k	37	PROG_FUNC16	Z
6	USB_DP2/PRT_DIS_P2	PD-15k	38	PROG_FUNC15	Z
7	USB_DM2/PRT_DIS_M2	PD-15k	39	PROG_FUNC14	Z
8	USB_DP4/PRT_DIS_P4	PD-15k	40	PROG_FUNC5	Z
9	USB_DM4/PRT_DIS_M4	PD-15k	41	PROG_FUNC4	Z
10	USB_DP5/PRT_DIS_P5	PD-15k	42	VDDIO33	A/P
11	USB_DM5/PRT_DIS_M5	PD-15k	43	PROG_FUNC3	Z
12	PROG_FUNC20	Z	44	PROG_FUNC2	Z
13	PROG_FUNC9	Z	45	PROG_FUNC13	Z
14	PRT_CTL4/OCS4	PD-67k	46	PROG_FUNC12	Z
15	PROG_FUNC7	PD-67k	47	RESET_N	PD-67k
16	VDDIO33	A/P	48	VBUS_DET	Z
17	VDDIO33	A/P	49	PROG_FUNC1	Z
18	TEST1	Z	50	PROG_FUNC8	Z
19	TEST2	Z	51	VDDIO33	A/P
20	TEST3	Z	52	PROG_FUNC21	Z
21	PROG_FUNC19	Z	53	PROG_FUNC10	Z
22	PRT_CTL3/OCS3	PD-67k	54	PROG_FUNC11	Z
23	PRT_CTL2/OCS2	PD-67k	55	PROG_FUNC22	Z
24	PRT_CTL1/OCS1	PD-67k	56	USB_DP3/PRT_DIS_P3	PD-15k
25	PROG_FUNC18	Z	57	USB_DM3/PRT_DIS_M3	PD-15k
26	PROG_FUNC17	Z	58	USBH_DP0	USB
27	VDDCR12	A/P	59	USBH_DM0	USB
28	VDDIO33	A/P	60	TESTEN/ATEST	A/P
29	SPI_CLK/SQI_CLK	Z	61	XTALO	A/P
30	SPI_DO/SQI_D0	PD-67k	62	XTALI/CLK_IN	A/P
31	SPI_DI/SQI_D1/CFG_BC_EN	Z	63	VDDPLLREF33	A/P
32	SPI_CE_N/SQI_CE_N/ CFG_NON_REM	PU-67k	64	RBIAS	A/P
Exposed Pad (VSS) must be connected to ground.					

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3.2 Pin Descriptions

TABLE 3-2: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
USB Interface			
USB Upstream D+	**USBH_DP0**	I/O-U	Upstream USB 2.0 Data Plus (D+)
USB Upstream D-	**USBH_DM0**	I/O-U	Upstream USB 2.0 Data Minus (D-)
USB Downstream Ports 5-1 D+	**USB_DP[5:1]**	I/O-U	Downstream USB 2.0 Ports 5-1 Data Plus (D+)
USB Downstream Ports 5-1 D-	**USB_DM[5:1]**	I/O-U	Downstream USB 2.0 Ports 5-1 Data Minus (D-)
USB Port Control Pins			
USB Ports 4-1 Power Enable	**PRT_CTL[4:1]**	I/O12	When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port . This pin will change to an output and be driven low when the port is disabled by configuration or by the host control.
USB Ports 4-1 Overcurrent Sense	**OCS[4:1]**	I/O12	Overcurrent sense for ports 4-1.
Gang Power	**PRT_CTL_GANG**	I/O12	This pin becomes the port control pin for all downstream ports when the hub is configured for ganged port power control mode. All port power controllers are controlled from this pin when the hub is configured for ganged port power mode.
SPI Interface Pins			
SPI Clock	**SPI_CLK**	I/O4	SPI clock.
SPI Data Out	**SPI_DO**	I/O4	SPI output data. If the SPI interface is enabled, this signal is the data out for the SPI port.
SPI Data In	**SPI_DI**	I/O4	SPI input data. If the SPI interface is enabled, this signal must have a weak pull-down applied at all times to prevent floating. **Note:** If SPI interface is not utilized, this pin cannot be left floating. It must be connected per the CFG_BC_EN pin description.

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TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
SPI Chip Enable	**SPI_CE_EN**	I/O4	Active low SPI chip enable input. If the SPI interface is enabled, this pin must be driven high in powerdown states. **Note:** If SPI interface is not utilized, this pin cannot be left floating. It must be connected per the CFG_NON_REM pin description.
SQI Interface Pins			
SQI Clock	**SQI_CLK**	I/O4	SQI clock.
SQI Data 0-3	**SQI_D[0:3]**	I/O4	SQI Data 0-3. If the SQI interface is enabled, these signals function as Data 0 through 3.
SQI Chip Enable	**SQI_CE_EN**	I/O4	Active low SQI chip enable input. If the SQI interface is enabled, this pin requires an external pull-up resistor. **Note:** If SQI interface is not utilized, this pin cannot be left floating. It must be connected per the CFG_NON_REM pin description.
Miscellaneous			
Programmable Functions 22-1	**PROG_FUNC[22:1]**	I/O12	These selectable function pins can be assigned a role via the **CONFIG_STRAP_[2:1]** pins, OTP configuration, or SMBus configuration. Refer to Section 3.3.4, "PROG_FUNC[22:1] Configuration (CONFIG_STRAP_[2:1])" for additional information.
VBUS Detection	**VBUS_DET**	I	This signal detects the state of the upstream bus power. When designing a detachable hub, this pin must be connected to the VBUS power pin of the upstream USB port through a resistor divider (50 kΩ by 100 kΩ) to provide 3.3 V. For self-powered applications with a permanently attached host, this pin must be connected to either 3.3 V or 5.0 V through a resistor divider to provide 3.3 V. In embedded applications, **VBUS_DET** may be controlled (toggled) when the host desires to renegotiate a connection without requiring a full reset of the device.
Reset Input	**RESET_N**	I	This active low signal is used by the system to reset the device. The active low pulse should be at least 1 µs wide.

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TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Bias Resistor	**RBIAS**	I-R	A 12.0 kΩ ±1.0% resistor is attached from ground to this pin to set the transceiver's internal bias settings. Place the resistor as close to the device as possible with a dedicated, low impedance connection to the GND plane.
External 25 MHz Crystal Input	**XTALI**	ICLK	External 25 MHz crystal input.
External 25 MHz Reference Clock Input	**CLK_IN**	ICLK	External reference clock input. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, **XTALO** should be left unconnected.
External 25 MHz Crystal Output	**XTALO**	OCLK	External 25 MHz crystal output.
Test	**TESTEN**	A	Test pin. This signal is used for test purposes and must always be connected to ground.
Analog Test	**ATEST**	A	Analog test pin. This signal is used for test purposes and must always be connected to ground.
Test 1	**TEST1**	A	Test 1 pin. This signal is used for test purposes and must always be pulled-up to 3.3V via a 4.7 kΩ resistor.
Test 2	**TEST2**	A	Test 2 pin. This signal is used for test purposes and must always be pulled-down to ground via a 4.7 kΩ resistor.
Test 3	**TEST3**	A	Test 3 pin. This signal is used for test purposes and must always be pulled-down to ground via a 4.7 kΩ resistor.
Configuration Straps			
Device Mode Configuration Straps 2-1	**CONFIG_STRAP_[2:1]**	I	Device mode configuration straps 2-1. These configuration straps are used to select the device's mode of operation. See Note 3-1. Refer to Section 3.3.4, "PROG_FUNC[22:1] Configuration (CONFIG_STRAP_[2:1])" for additional information.

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TABLE 3-2: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Port 5-1 D+ Disable Configuration Strap	**PRT_DIS_P[5:1]**	I	Port 5-1 D+ Disable configuration strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_M[5:1]** straps to disable the related port (5-1). See Note 3-1. Both USB data pins for the corresponding port must be tied to 3.3V to disable the associated downstream port.
Port 5-1 D- Disable Configuration Strap	**PRT_DIS_M[5:1]**	I	Port 5-1 D- Disable configuration strap. These configuration straps are used in conjunction with the corresponding **PRT_DIS_P[5:1]** straps to disable the related port (5-1). See Note 3-1. Both USB data pins for the corresponding port must be tied to 3.3V to disable the associated downstream port.
Non-Removable Ports Configuration Strap	**CFG_NON_REM**	I	Non-Removable Ports Configuration Strap. This configuration strap controls the number of reported non-removable ports. See Note 3-1.
Battery Charging Configuration Strap	**CFG_BC_EN**	I	Battery Charging Configuration Strap. This configuration strap controls the number of BC 1.2 enabled downstream ports. See Note 3-1.

Power/Ground			
+3.3V I/O Power Supply Input	**VDDIO33**	P	+3.3V I/O power supply input.
+3.3V Analog Power Supply Input	**VDDPLLREF33**	P	+3.3V master bias / PLL regulator supply input.
+1.2V Core Power Supply Output	**VDDCR12**	P	+1.2V digital core power supply output. **Note:** This signal requires connection of a 1uF low-ESR capacitor to ground.
Ground	**VSS**	P	Ground pins.

Note 3-1 Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a

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load. For additional information, refer to Section 3.3, "Configuration Straps and Programmable Functions".

3.3 Configuration Straps and Programmable Functions

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (**RESET_N**) to determine the default configuration of a particular feature. The state of the signal is latched following de-assertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated programmable pin functions.

Note: The system designer must guarantee that configuration straps meet the timing requirements specified in Section 9.6.2, "Power-On and Configuration Strap Timing" and Section 9.6.3, "Reset and Configuration Strap Timing". If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

3.3.1 PORT DISABLE CONFIGURATION (PRT_DIS_P[5:1] / PRT_DIS_M[5:1])

The **PRT_DIS_P[5:1]** / **PRT_DIS_M[5:1]** configuration straps are used in conjunction to disable the related port (5-1).

For **PRT_DIS_P*x*** (where *x* is the corresponding port 5-1):

0 = Port *x* D+ Enabled

1 = Port *x* D+ Disabled

For **PRT_DIS_M*x*** (where *x* is the corresponding port 5-1):

0 = Port *x* D- Enabled

1 = Port *x* D- Disabled

Note: Both **PRT_DIS_P*x*** and **PRT_DIS_M*x*** (where *x* is the corresponding port) must be tied to 3.3 V to disable the associated downstream port.

3.3.2 NON-REMOVABLE PORT CONFIGURATION (CFG_NON_REM)

The **CFG_NON_REM** configuration strap is used to configure the non-removable port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the **CFG_NON_REM** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, and 10 Ω pull-down, as shown in Table 3-3.

TABLE 3-3: CFG_NON_REM RESISTOR ENCODING

CFG_NON_REM Resistor Value	Setting
200 kΩ Pull-Down	Port 1-4 removable (Note 3-2)
200 kΩ Pull-Up	Port 1 non-removable
10 kΩ Pull-Down	Port 1, 2 non-removable
10 kΩ Pull-Up	Port 1, 2, 3 non-removable
10 Ω Pull-Down	Port 1, 2, 3, 4 non-removable

Note 3-2 The standard port will always be non-removable (Port 5). Battery charging and OCS are not supported for standard ports.

3.3.3 BATTERY CHARGING CONFIGURATION (CFG_BC_EN)

The **CFG_BC_EN** configuration strap is used to configure the battery charging port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the **CFG_BC_EN** pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, and 10 Ω pull-down, as shown in Table 3-4.

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TABLE 3-4: CFG_BC_EN RESISTOR ENCODING

CFG_NON_REM Resistor Value	Setting
200 kΩ Pull-Down	No battery charging
200 kΩ Pull-Up	Port 1 battery charging
10 kΩ Pull-Down	Port 1, 2 battery charging
10 kΩ Pull-Up	Port 1, 2, 3 battery charging
10 Ω Pull-Down	Port 1, 2, 3, 4 battery charging

Note: The standard port does not support battery charging and OCS (Port 5).

3.3.4 PROG_FUNC[22:1] CONFIGURATION (CONFIG_STRAP_[2:1])

The USB4916 provides 22 programmable function pins (**PROG_FUNC[22:1]**). These pins can be configured to 6 pre-defined configurations via the **CONFIG_STRAP_[2:1]** pins. These configurations are selected via external resistors on the **CONFIG_STRAP_[2:1]** pins, as detailed in Table 3-5. Resistor values and combinations not detailed in Table 3-5 are reserved and should not be used.

TABLE 3-5: CONFIG_STRAP_[2:1] RESISTOR ENCODING

Mode	CONFIG_STRAP_2 Resistor Value	CONFIG_STRAP_1 Resistor Value
Configuration 1	200 kΩ Pull-Down	200 kΩ Pull-Down
Configuration 2	200 kΩ Pull-Down	200 kΩ Pull-Up
Configuration 3	200 kΩ Pull-Down	10 kΩ Pull-Down
Configuration 4	200 kΩ Pull-Down	10 kΩ Pull-Up
Configuration 5	200 kΩ Pull-Down	10 Ω Pull-Down
Configuration 6	200 kΩ Pull-Down	10 Ω Pull-Up

A summary of the configuration pin assignments for each of the 6 configurations is provided in Table 3-6. For details on behavior of each programmable function, refer to Table 3-7.

TABLE 3-6: PROG_FUNC[22:1] FUNCTION ASSIGNMENT

Pin	Configuration 1	Configuration 2	Configuration 3	Configuration 4	Configuration 5	Configuration 6
PROG_FUNC_1	GPIO1	GPIO1	UART_nDTR	GPIO1	UART_nDTR	GPIO1
PROG_FUNC_2	GPIO2 (BC_LED3)	GPIO2 (BC_LED3)	UART_TX	GPIO2 (BC_LED3)	UART_TX	GPIO2 (BC_LED3)
PROG_FUNC_3	GPIO3 (BC_LED4)	GPIO3 (BC_LED4)	UART_RX	GPIO3 (BC_LED4)	UART_RX	GPIO3 (BC_LED4)
PROG_FUNC_4	I2S_LRCK	GPIO6	GPIO6	I2S_LRCK	I2S_LRCK	I2S_LRCK
PROG_FUNC_5	I2S_SDOUT	GPIO8	GPIO8 (BC_LED1)	I2S_SDOUT	I2S_SDOUT	I2S_SDOUT
PROG_FUNC_6	GPIO10	GPIO10	CONNECT_IND4	GPIO10	GPIO10	GPIO10
PROG_FUNC_7	SMB1_CLK	SMB1_CLK	SMB1_CLK	SMB1_CLK	SMB1_CLK	SMB1_CLK
PROG_FUNC_8	GPIO64	GPIO64	UART_nDSR	GPIO64	UART_nDSR	GPIO64
PROG_FUNC_9	GPIO65	GPIO65	CONNECT_IND2	SMB2_DAT	GPIO65	SMB2_DAT
PROG_FUNC_10	GPIO66	GPIO66	CONNECT_IND3	SMB2_CLK	GPIO66	SMB2_CLK
PROG_FUNC_11	MIC_DET	GPIO67	GPIO67	GPIO67	GPIO67	GPIO67
PROG_FUNC_12	GPIO68 (BC_LED1)	GPIO68 (BC_LED1)	UART_nCTS	GPIO68 (BC_LED1)	UART_nCTS	GPIO68 (BC_LED1)
PROG_FUNC_13	GPIO69 (BC_LED2)	GPIO69 (BC_LED2)	UART_nRTS	GPIO69 (BC_LED2)	UART_nRTS	GPIO69 (BC_LED2)
PROG_FUNC_14	I2S_SDIN	GPIO70	GPIO70 (BC_LED2)	I2S_SDIN	I2S_SDIN	I2S_SDIN

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TABLE 3-6: PROG_FUNC[22:1] FUNCTION ASSIGNMENT (CONTINUED)

Pin	Configuration 1	Configuration 2	Configuration 3	Configuration 4	Configuration 5	Configuration 6
PROG_FUNC_15	I2S_MCLK	GPIO71	GPIO71 (BC_LED3)	I2S_MCLK	I2S_MCLK	I2S_MCLK
PROG_FUNC_16	I2S_SCK	GPIO72	GPIO72 (BC_LED4)	I2S_SCK	I2S_SCK	I2S_SCK
PROG_FUNC_17	SMB1_DAT	SMB1_DAT	SMB1_DAT	SMB1_DAT	SMB1_DAT	SMB1_DAT
PROG_FUNC_18	GPIO74	GPIO74	CONNECT_IND1	PRI_SUSPEND	GPIO74	GPIO74
PROG_FUNC_19	GPIO75	GPIO75	UART_nDCD	GPIO75	UART_nDCD	GPIO75
PROG_FUNC_20	MHDC_LINK_ STATUS	MHDC_LINK_ STATUS	MHDC_LINK_ STATUS	MHDC_LINK_ STATUS	MHDC_LINK_ STATUS	MHDC_LINK_ STATUS
PROG_FUNC_21	GPIO77	GPIO77	GPIO77	GPIO77	GPIO77	GPIO77
PROG_FUNC_22	GPIO78	GPIO78	GPIO78	GPIO78	GPIO78	GPIO78

TABLE 3-7: PROGRAMMABLE FUNCTIONS DESCRIPTIONS

Function	Buffer Type	Description
UART Interface		
UART_TX	O12	UART Transmit
UART_RX	I	UART Receive
UART_nCTS	I	UART Clear To Send
UART_nRTS	O12	UART Request To Send
UART_nDCD	I	UART Data Carrier Detect
UART_nDSR	I	UART Data Set Ready
UART_nDTR	O12	UART Data Terminal Ready
SMBus Master Interface		
SMB1_CLK	I/OD12	SMBus Master Clock

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TABLE 3-7: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Function	Buffer Type	Description
SMB1_DAT	I/OD12	SMBus Master Data
SMBus Slave Interface		
SMB2_CLK	I/OD12	SMBus Slave Clock For proper SMBus slave operation, an external 10 kΩ resistor is required on this signal.
SMB2_DAT	I/OD12	SMBus Slave Data For proper SMBus slave operation, an external 10 kΩ resistor is required on this signal.
I^2S Interface		
I2S_SCK	O12	I^2S Continuous Serial Clock
I2S_LRCK	O12	I^2S Word Select / Left-Right Clock
I2S_MCLK	O12	I^2S Master Clock
I2S_SDOUT	O12	I^2S Serial Data Out
I2S_SDIN	I	I^2S Serial Data In
MIC_DET	I	I^2S MIC Plug Detect 0 = No microphone plugged into the audio jack 1 = Microphone plugged into the audio jack
Miscellaneous		
GPIO*x*	I/O12	General Purpose Inputs/Outputs (*x* = 1-3, 6, 8, 10, 64-72, 74-75, 77-78)
BC_LED[4:1]	O12	Battery Charging Status Port 4-1 LED Tri-state = Battery charging not enabled 1 = Battery charging is enabled 0 = battery charging is in BC1.2 CDP Mode. A 0 is set on when the firmware negotiates BC1.2 in CDP Mode. In CDP mode, the bit is cleared when the attached device is removed or the port is powered off. User experience: The user of the hub sees an LED “Off” id battery charging is not enabled, and an LED “On” if battery charging is enabled. When a BC1.2 device is plugged in while the hub’s upstream is active, the user sees the LED change color, indicating a positive BC1.2 negotiation. In DCP Mode, the BC_LED*x* indicates only the BC enabled statis for the specific port.
CONNECT_IND[4:1]	O12	Downstream Port 4-1 Connect Indicator 1 = USB 2.0 or USB 1.1 connection to port 0 = Nothing connected to port

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TABLE 3-7: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Function	Buffer Type	Description
PRI_SUSPEND	O12	Primary Hub Suspend Status 1 = Primary hub is suspended 0 = Primary hub is not suspended If the HUB_RESUME_INHIBIT bit is set in the HUB_CFG_3 register, the PRI_SUSPEND pin will output the RESUME_INHIBIT status and not the suspend status of the hub. In Resume Inhibit mode, by default the PRI_SUSPEND pin will be low and will become high to wakeup the power management IC and then again will become low. This time is determined by the value in the GLOBAL_RESUME_TIME register.
MHDC_LINK_STATUS	O12	Multi-Host Link Status 1 = Link up: Both arms of the link are enumerated 0 = Link Down: One or both arms of the link are not operational

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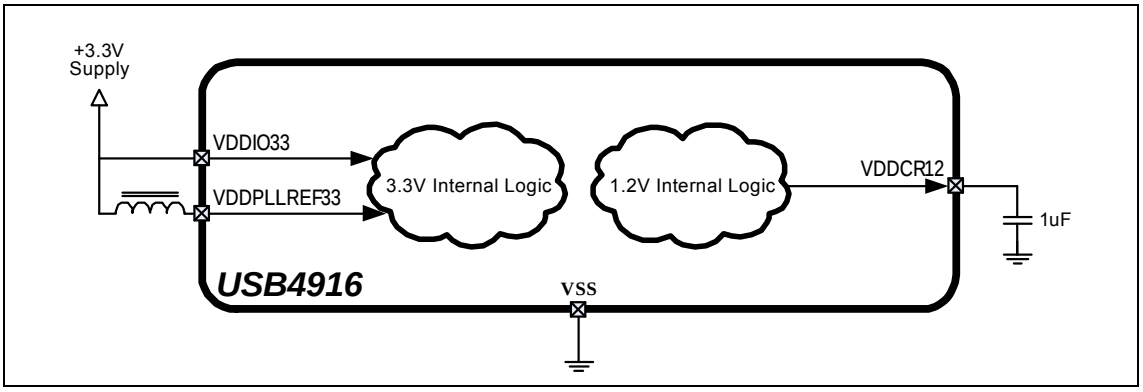
4.0 DEVICE CONNECTIONS

4.1 Power Connections

Figure 4-1 illustrates the device power connections.

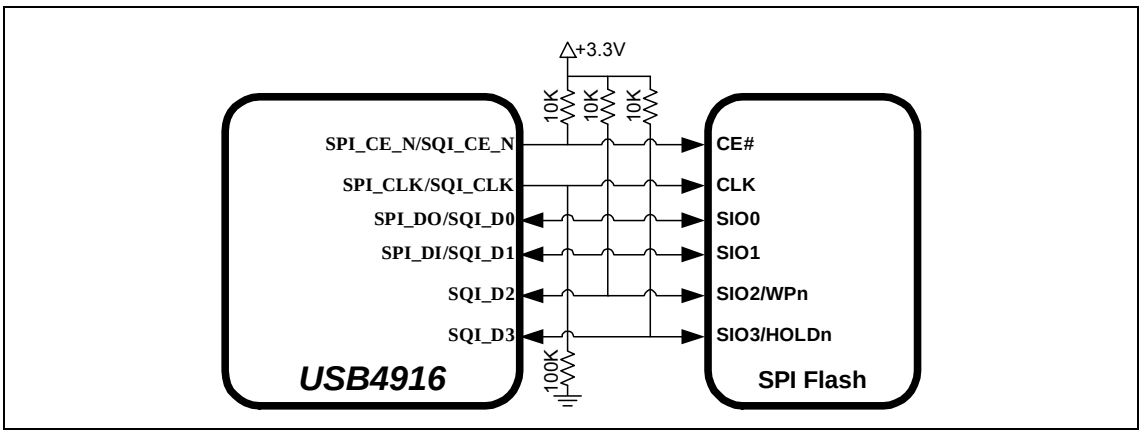
FIGURE 4-1: POWER CONNECTIONS



4.2 SPI Flash Connections

Figure 4-2 illustrates the device SPI Flash connections.

FIGURE 4-2: SPI FLASH CONNECTIONS



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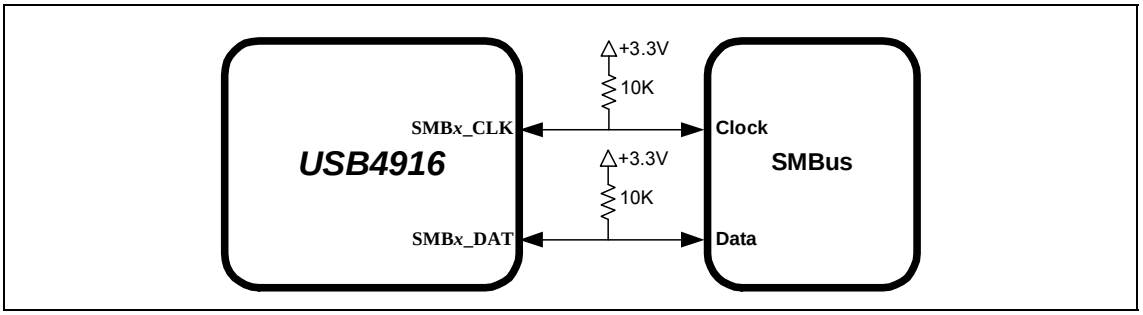
4.3 SMBus Connections

Figure 4-3 illustrates the device SMBus Connections.

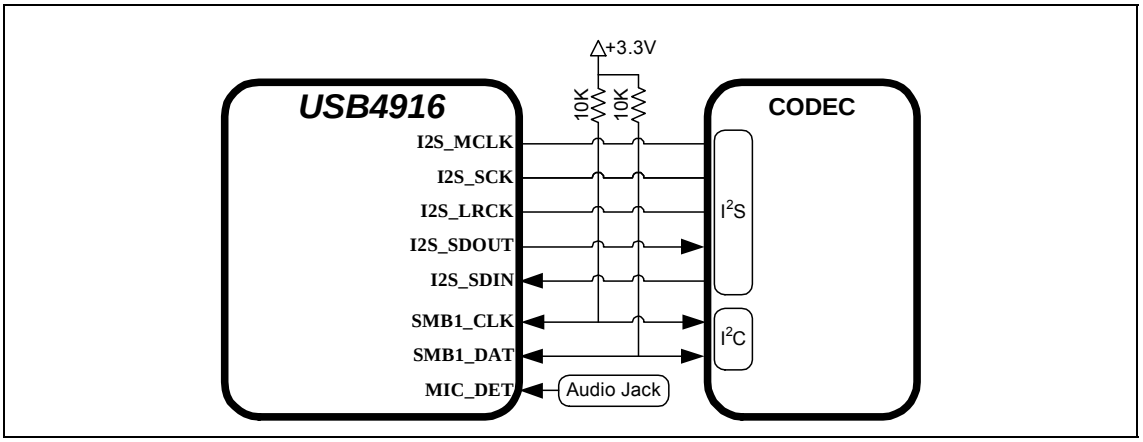
FIGURE 4-3: SMBUS CONNECTIONS



4.4 I²S Connections

Figure 4-4 illustrates the device I²S connections.

FIGURE 4-4: I²S CONNECTIONS



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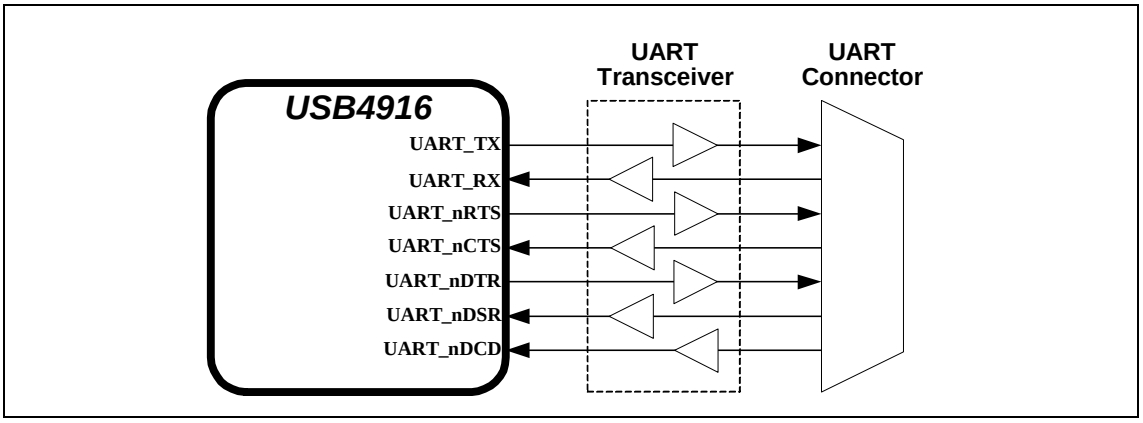
4.5 UART Connections

Figure 4-5 illustrates the device UART connections.

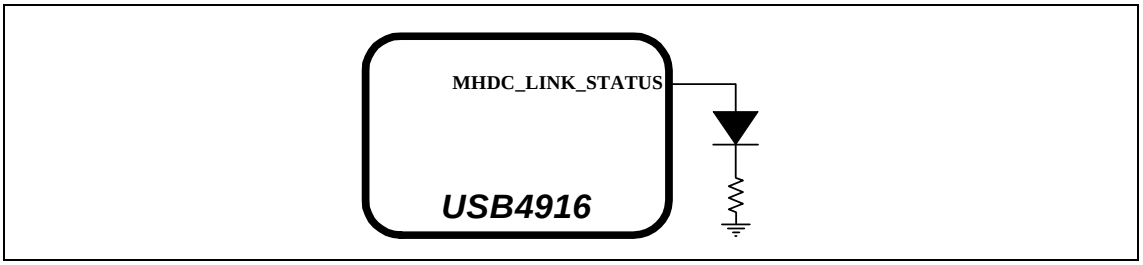
FIGURE 4-5: UART CONNECTIONS



4.6 Multi-Host Link Status Connection

Figure 4-6 illustrates the device MHDC connections.

FIGURE 4-6: MULTI-HOST LINK STATUS CONNECTION



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5.0 MODES OF OPERATION

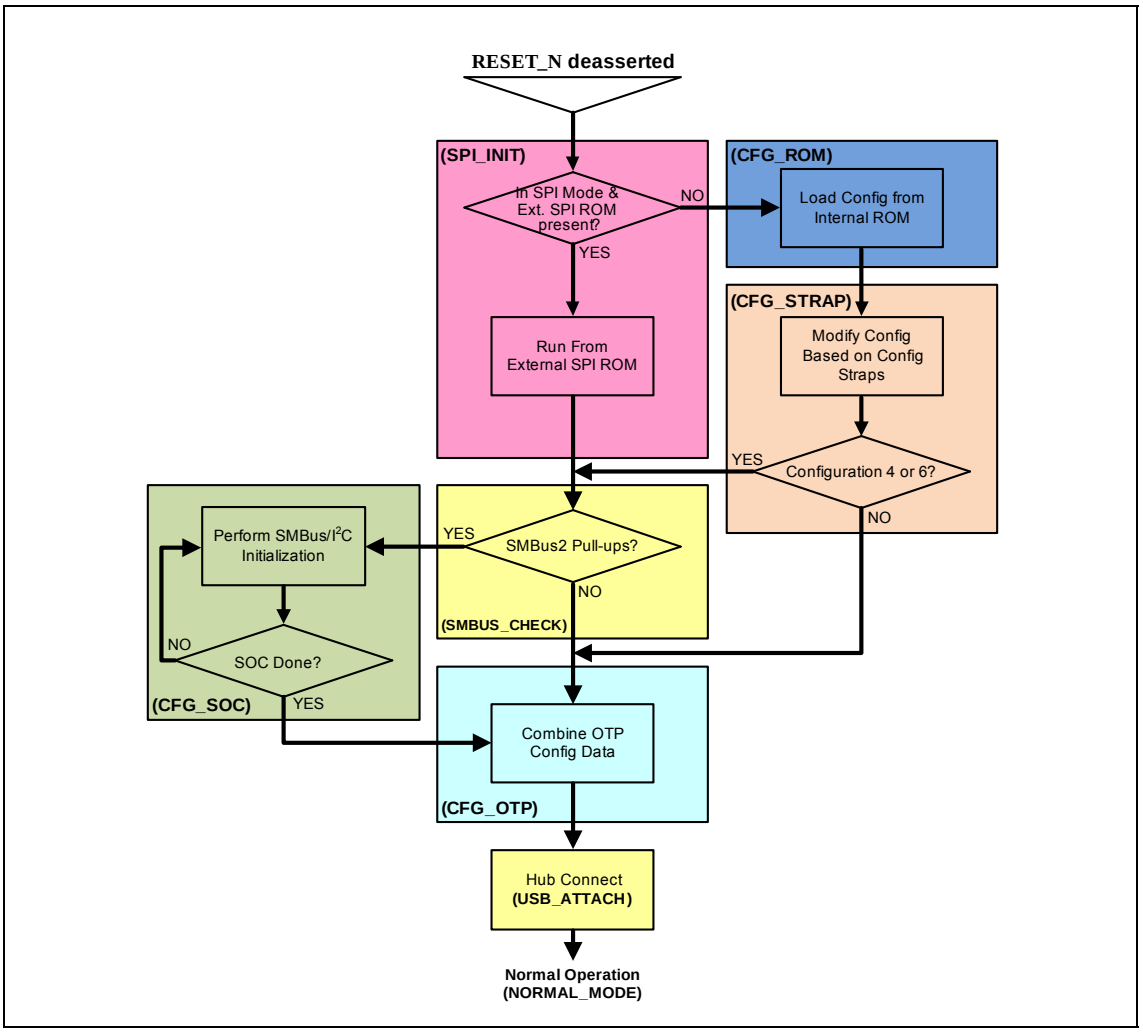
The device provides two main modes of operation: Standby Mode and Hub Mode. These modes are controlled via the **RESET_N** pin, as shown in Table 5-1.

TABLE 5-1: MODES OF OPERATION

RESET_N Input	Summary
0	**Standby Mode**: This is the lowest power mode of the device. No functions are active other than monitoring the **RESET_N** input. All port interfaces are high impedance and the PLL is halted. Refer to Section 8.9, "Resets" for additional information on **RESET_N**.
1	**Hub (Normal) Mode**: The device operates as a configurable USB hub. This mode has various sub-modes of operation, as detailed in Figure 5-1. Power consumption is based on the number of active ports, their speed, and amount of data received.

The flowchart in Figure 5-1 details the modes of operation and details how the device traverses through the Hub Mode stages (shown in bold). The remaining sub-sections provide more detail on each stage of operation.

FIGURE 5-1: HUB MODE FLOWCHART



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5.1 Boot Sequence

5.1.1 STANDBY MODE

If the **RESET_N** pin is asserted, the hub will be in Standby Mode. This mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all downstream ports are disabled, the USB data pins are held in a high-impedance state, all transactions immediately terminate (no states saved), all internal registers return to their default state, the PLL is halted, and core logic is powered down in order to minimize power consumption. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after **RESET_N** is negated high.

5.1.2 SPI INITIALIZATION STAGE (SPI_INIT)

The first stage, the initialization stage, occurs on the deassertion of **RESET_N**. In this stage, the internal logic is reset, the PLL locks if a valid clock is supplied, and the configuration registers are initialized to their default state. The internal firmware then checks for an external SPI ROM. The firmware looks for an external SPI flash device that contains a valid signature of “2DFU” (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the SPI Firmware/external SPI ROM is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM (CFG_ROM stage).

When using an external SPI ROM, a minimum of 2.2 Mbit is required, and 60 MHz or faster SPI ROM must be used. Both 1- and 2-bit SPI ROM are supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI flashes are supported.

If the system is not strapped for SPI Mode, code execution will continue from internal ROM (CFG_ROM stage).

5.1.3 CONFIGURATION FROM INTERNAL ROM STAGE (CFG_ROM)

In this stage, the internal firmware loads the default values from the internal ROM. Most of the hub configuration registers, USB descriptors, electrical settings, etc. will be initialized in this state even when running from SPI.

5.1.4 CONFIGURATION STRAP READ STAGE (CFG_STRAP)

In this stage, the firmware reads the following configuration straps to override the default values:

- **CONFIG_STRAP_[2:1]**
- **PRT_DIS_P[5:1]**
- **PRT_DIS_M[5:1]**
- **CFG_NON_REM**
- **CFG_BC_EN**

If the **CONFIG_STRAP_[2:1]** pins are set to Configuration 4 or 6, the device will move to the SMBUS_CHECK stage, otherwise it move to the CFG_OTP stage. Refer to Section 3.3, "Configuration Straps and Programmable Functions" for information on usage of the various device configuration straps.

5.1.5 SMBUS CHECK STAGE (SMBUS_CHECK)

Based on the **PROG_FUNC[22:1]** configuration selected (refer to Section 3.3.4, "PROG_FUNC[22:1] Configuration (CONFIG_STRAP_[2:1])"), the firmware will check for the presence of external pull up resistors on the SMBus slave programmable function pins. If 10K pull-ups are detected on both pins, the device will be configured as an SMBus slave, and the next state will be CFG_SOC. If a pull-up is not detected in either of the pins, the next state is CFG_OTP.

5.1.6 SOC CONFIGURATION STAGE (CFG_SOC)

In this stage, the SOC can modify any of the default configuration settings specified in the integrated ROM, such as USB device descriptors, port electrical settings, and control features such as downstream battery charging.

In this stage the firmware will wait indefinitely for the SMBus/I^2C configuration there is no time limit on this stage. The external SMBus master writes to register 0xFF, to end the configuration in legacy mode. In non-legacy mode, the SMBus command USB_ATTACH (opcode 0xAA55) or USB_ATTACH_WITH_SMBUS (opcode 0xAA56) will finish the configuration.

5.1.7 OTP CONFIGURATION STAGE (CFG_OTP)

Once the SOC has indicated that it is done with configuration, all configuration data is combined in this stage. The default data, the SOC configuration data, and the OTP data are all combined in the firmware and the device is programmed.

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Note:	Changes to hub registers made in OTP memory space are not visible via SMBus during CFG_SOC stage. Any register which is modified via SMBus during SOC_CFG and also modified in the OTP memory will exit the configuration stages with the value as programmed in the OTP memory.

5.1.8 HUB CONNECT STAGE (USB_ATTACH)

Once the hub registers are updated through default values, SMBus master, and OTP, the device firmware will enable attaching the USB host by setting the USB_ATTACH bit in the HUB_CMD_STAT register. The device will remain in the Hub Connect stage indefinitely until the VBUS function is deasserted/assertion of external RESET_N pin.

5.1.9 NORMAL MODE (NORMAL_MODE)

Lastly, the hub enters Normal Mode of operation. In this stage full USB operation is supported under control of the USB Host on the upstream port. The device will remain in the normal mode until the operating mode is changed by the USB Host.

If **RESET_N** is asserted low, then Standby Mode is entered. The device may then be placed into any of the designated hub stages. Asserting a soft disconnect on the upstream port will cause the hub to return to the Hub Connect stage until the soft disconnect is negated.

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6.0 DEVICE CONFIGURATION

The device supports a large number of features (some mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. The hub can be configured either internally or externally depending on the implemented interface.

Microchip provides a comprehensive software programming tool, MPLAB Connect (formerly ProTouch2), for OTP configuration of various USB4916 functions and registers. All configuration is to be performed via the MPLAB Connect Configurator programming tool. For additional information on this tool, refer to th MPLAB Connect Configurator programming tool product page at http://www.microchip.com/design-centers/usb/mplab-connect-configurator.

Additional information on configuring the USB4916 via SMBus is provided in the *AN2439 - Configuration of the USB491x/USB492x/USB4715*" application note, which contains details on the hub operational mode, SOC configuration stage, OTP configuration, USB configuration, and configuration register definitions. This application note, along with other USB4916 resources, can be found on the Microchip USB4916 product page at www.microchip.com/USB4916.

Note:	Device configuration straps and programmable pins are detailed in Section 3.3, "Configuration Straps and Programmable Functions," on page 13. Refer to Section 7.0, "Device Interfaces" for detailed information on each device interface.

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7.0 DEVICE INTERFACES

The USB4916 provides multiple interfaces for configuration, external memory access, etc.. This section details the various device interfaces and their usage:

- SPI/SQI Master Interface
- SMBus/I2C Master/Slave Interfaces
- I2S Interface
- UART Interface

Note: For details on how to enable each interface, refer to Section 3.3, "Configuration Straps and Programmable Functions".

For information on device connections, refer to Section 4.0, "Device Connections". For information on device configuration, refer to Section 6.0, "Device Configuration".

Microchip provides a comprehensive software programming tool, MPLAB Connect (formerly ProTouch2), for configuring the USB4916 functions, registers and OTP memory. All configuration is to be performed via the MPLAB Connect Configurator programming tool. For additional information on this tool, refer to th MPLAB Connect Configurator programming tool product page at http://www.microchip.com/design-centers/usb/mplab-connect-configurator.

7.1 SPI/SQI Master Interface

The SPI/SQI controller has two basic modes of operation: execution of an external hub firmware image, or the USB to SPI bridge. On power up, the firmware looks for an external SPI flash device that contains a valid signature of 2DFU (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM mode is enabled and the code execution begins at address 0x0000 in the external SPI device. If a valid signature is not found, then execution continues from internal ROM and the SPI interface can be used as a USB to SPI bridge.

The second mode of operation is the USB to SPI bridge operation. Additional details on this feature can be found in Section 8.5, "USB to SPI Bridging" as well as the *AN2430 - USB to SPI Bridging with USB4715 and USB49xx* application note.

Table 7-1 details how the associated pins are mapped in SPI vs. SQI mode

TABLE 7-1: SPI/SQI PIN USAGE

SPI Mode	SQI Mode	Description
SPI_CE_N	SQI_CE_N	SPI/SQI Chip Enable (Active Low)
SPI_CLK	SQI_CLK	SPI/SQI Clock
SPI_DO	SQI_D0	SPI Data Out; SQI Data I/O 0
SPI_DI	SQI_D1	SPI Data In; SQI Data I/O 1
-	SQI_D2	SQI Data I/O 2
-	SQI_D3	SQI Data I/O 3

Note: For SPI timing information, refer to Section 9.6.8, "SPI/SQI Timing".

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7.2 SMBus/I^{2}C Master/Slave Interfaces

The USB4916 provides two independent SMBus/I^{2}C controllers SMBus 1 and SMBus 2, which can be used to access internal device run time registers or program the internal OTP memory. SMBus 1 is used as the USB to SMBus/I^{2}C bridge, and SMBus 2 is used as the slave interface. The device contains two 128 byte buffers to enable simultaneous master/slave operation and to minimize firmware overhead in processed SMBus/I^{2}C packets.

The SMBus 1 and SMBus 2 interfaces are assigned to programmable pins (**PROG_FUNC_*x***) and therefore the device must be programmed into specific configurations to enable both interfaces. SMBus 1 is available in all **CONFIG_STRAP[1:2]** settings. SMBus 2 is available only with specific **CONFIG_STRAP[1:2]** settings. Refer to Section 3.3.4, "PROG_FUNC[22:1] Configuration (CONFIG_STRAP_[2:1])" for additional information.

Note:	For SMBus/I^{2}C timing information, refer to Section 9.6.5, "SMBus Timing" and Section 9.6.6, "I2C Timing".

7.3 I^{2}S Interface

The USB4916 provides an integrated I^{2}S interface to facilitate the connection of digital audio devices. The I^{2}S interface conforms to the voltage, power, and timing characteristics/specifications as set forth in the *I^{2}S-Bus Specification*, and consists of the following signals:

- **I2S_SDIN**: Serial Data Input
- **I2S_SDOUT**: Serial Data Output
- **I2S_SCK**: Serial Clock
- **I2S_LRCK**: Left/Right Clock (SS/FSYNC)
- **I2S_MCLK**: Master Clock

Each audio connection is half-duplex, so **I2S_SDOUT** exists only on the transmit side and **I2S_SDIN** exists only on the receive side of the interface. Some codecs refer to the Serial Clock (**I2S_SCK**) as Baud/Bit Clock (BCLK). Also, the Left/Right Clock is commonly referred to as LRC or LRCK. The I^{2}S and other audio protocols refer to LRC as Word Select (WS).

The following codec is supported by default:

- Analog Devices ADAU1961 (24-bit 96KHz)

Note:	For I^{2}S timing information, refer to Section 9.6.7, "I2S Timing".

7.3.1 MODES OF OPERATION

The USB audio class operates in three ways: Asynchronous, Synchronous and Adaptive. There are also multiple operating modes, such as hi-res, streaming, etc.. Typically for USB devices, inputs such as microphones are Asynchronous, and output devices such as speakers are Adaptive. The hardware is set up to handle all three modes of operation. It is recommended that the following configuration be used: Asynchronous IN; Adaptive OUT; 48Khz streaming mode; Two channels: 16 bits per channel.

7.3.1.1 Asynchronous IN 48KHz Streaming

In this mode, the codec sampling clock is set to 48Khz based on the local oscillator. This clock is never changed. The data from the codec is fed into the input FIFO. Since the sampling clock is asynchronous to the host clock, the amount of data captured in every USB frame will vary. This issue is left for the host to handle. The input FIFO has two markers, a low water mark (THRESHOLD_LOW_VAL), and a high water mark (THRESHOLD_HIGH_VAL). There are three registers to determine how much data to send back in each frame. If the amount of data in the FIFO exceeds the high water mark, then HI_PKT_SIZE worth of data is sent. If the data is between the high and low water mark, the normal MID_PKT_SIZE amount of data is sent. If the data is below the low water mark, LO_PKT_SIZE worth of data is sent.

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7.3.1.2 Adaptive OUT 48KHz Streaming

In this mode, the codec sampling clock is initially set to 48Khz based on the local oscillator. The host data is fed into the OUT FIFO. The host will send the same amount of data on every frame, i.e. 48KHz of data based on the host clock. The codec sampling clock is asynchronous to the host clock. This will cause the amount of data in the OUT FIFO to vary. If the amount of data in the FIFO exceeds the high water mark, then the sampling clock is increased. If the data is between the high and low water mark, the sampling clock does not change. If the data is below the low water mark, the sampling clock is decreased.

7.3.1.3 Synchronous Operation

For synchronous operation, the internal clock must be synchronized with the host SOF. The Frame SOF is nominally 1mS. Since there is significant jitter in the SOFs, there is circuitry provided to measure the SOFs over a long period of time to get a more accurate reading. The calculated host frequency is used to calculate the codec sampling clock.

7.4 UART Interface

The device incorporates a configurable universal asynchronous receiver/transmitter (UART) that is functionally compatible with the NS 16550AF, 16450, 16450 ACE registers and the 16C550A. The UART performs serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. Two sets of baud rates are provided: 24 Mhz and 16 MHz. When the 24 Mhz source clock is selected, standard baud rates from 50 to 115.2 K are available. When the source clock is 16 MHz, baud rates from 125 K to 1,000 K are available. The character options are programmable for the transmission of data in word lengths of from five to eight, 1 start bit; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UART contains a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UART is also capable of supporting the MIDI data rate.

7.4.1 TRANSMIT OPERATION

Transmission is initiated by writing the data to be sent to the TX Holding Register or TX FIFO (if enabled). The data is then transferred to the TX Shift Register together with a start bit and parity and stop bits as determined by settings in the Line Control Register. The bits to be transmitted are then shifted out of the TX Shift Register in the order Start bit, Data bits (LSB first), Parity bit, Stop bit, using the output from the Baud Rate Generator (divided by 16) as the clock.

If enabled, a TX Holding Register Empty interrupt will be generated when the TX Holding Register or the TX FIFO (if enabled) becomes empty.

When FIFOs are enabled (i.e. bit 0 of the FIFO Control Register is set), the UART can store up to 16 bytes of data for transmission at a time. Transmission will continue until the TX FIFO is empty. The FIFO's readiness to accept more data is indicated by interrupt.

7.4.2 RECEIVE OPERATION

Data is sampled into the RX Shift Register using the Receive clock, divided by 16. The Receive clock is provided by the Baud Rate Generator. A filter is used to remove spurious inputs that last for less than two periods of the Receive clock. When the complete word has been clocked into the receiver, the data bits are transferred to the RX Buffer Register or to the RX FIFO (if enabled) to be read by the CPU. (The first bit of the data to be received is placed in bit 0 of this register.) The receiver also checks that the parity bit and stop bits are as specified by the Line Control Register.

If enabled, an RX Data Received interrupt will be generated when the data has been transferred to the RX Buffer Register or, if FIFOs are enabled, when the RX Trigger Level has been reached. Interrupts can also be generated to signal RX FIFO Character Timeout, incorrect parity, a missing stop bit (frame error) or other Line Status errors.

When FIFOs are enabled (i.e. bit 0 of the FIFO Control Register is set), the UART can store up to 16 bytes of received data at a time. Depending on the selected RX Trigger Level, interrupt will go active to indicate that data is available when the RX FIFO contains 1, 4, 8 or 14 bytes of data.

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8.0 FUNCTIONAL DESCRIPTIONS

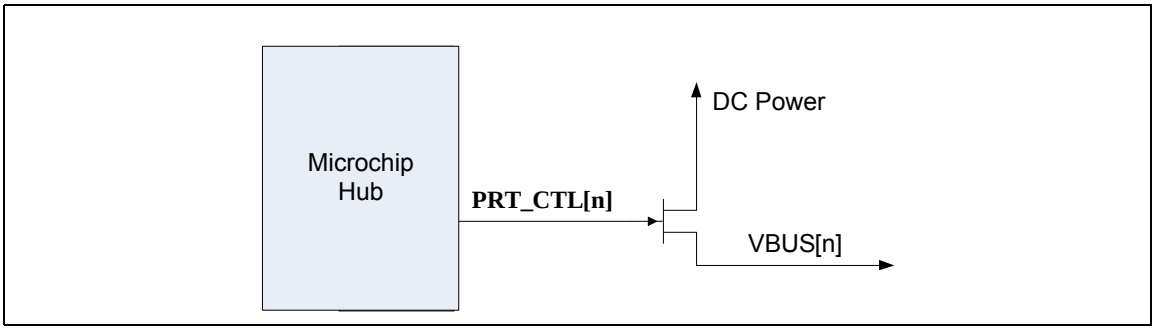
This section details various USB4916 functions, including:

- Downstream Battery Charging
- Multi-Host Endpoint Reflector
- USB to GPIO Bridging
- USB to SMBus/I2C Bridging
- USB to SPI Bridging
- USB to UART Bridging
- Link Power Management (LPM)
- Port Power Control
- Resets

8.1 Downstream Battery Charging

The device can be configured by an OEM to have any of the downstream ports support battery charging. The hub's role in battery charging is to provide acknowledgment to a device's query as to whether the hub system supports USB battery charging. The hub silicon does not provide any current or power FETs or any additional circuitry to actually charge the device. Those components must be provided externally by the OEM.

FIGURE 8-1: BATTERY CHARGING EXTERNAL POWER SUPPLY



If the OEM provides an external supply capable of supplying current per the battery charging specification, the hub can be configured to indicate the presence of such a supply from the device. This indication, via a handshake on the D+ and D- at the start of the connection with the device, is on a per port basis. For example, the OEM can configure two ports to support battery charging through high current power FETs and leave the other two ports as standard USB ports.

For detailed information on utilizing the USB4916 battery charging feature, refer to the application note "*USB Battery Charging with Microchip USB4715 and USB49xx Hubs*", which can be found on the Microchip USB4916 product page at www.microchip.com/USB4916.

8.2 Multi-Host Endpoint Reflector

The USB4916's internal Multi-Host Endpoint Reflector allows for smart-phone automotive mode sessions to be entered on the downstream ports. The USB4916 supports the Multi-Host Endpoint Reflector on four downstream ports.

The Multi-Host Endpoint Reflector uses standard Network Control Model (NCM) device protocol, which is a sub-class of Communication Device Class (CDC) group of protocols. Standard NCM USB drivers may be utilized; No custom drivers are required.

A Multi-Host Endpoint Reflector session may be entered on only 1 downstream port at a time. Entry into Multi-Host mode is initiated via a no data Control USB transfer addressed to the internal Multi-Host Endpoint Reflector device in the hub.

The USB4916 has two internal USB devices. The Multi-Host Endpoint Reflector device is a Composite WinUSB and NCM device with Product ID 0x4910. The Hub Feature Controller device which enables USB bridging function is a WinUSB device with Product ID 0x4940. The Multi-Host Endpoint Reflector is connected to port 6, while the Hub Feature Controller is connected to port 7.

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The hub ports which are connected to both the Multi-Host Endpoint Reflector and Hub Feature Controller are both configured as non-removable.

For detailed information on utilizing the USB4916 multi-host endpoint reflector feature, refer to the application note "*AN2374 - USB4916/USB4914 Multi-Host Endpoint Reflector Operation*", which can be found on the Microchip USB4916 product page at www.microchip.com/USB4916.

8.3 USB to GPIO Bridging

The USB to GPIO bridging feature of the USB4916 provides system designers expanded system control and potential BOM reduction. General Purpose Input/Outputs (GPIOs) may be used for any general 3.3V level digital control and input functions.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Set the direction of the GPIO (input or output)
- Enable a pull-up resistor
- Enable a pull-down resistor
- Read the state
- Set the state

For detailed information on utilizing the USB4916 USB to GPIO bridging feature, refer to the application note "*AN2437 - USB to GPIO Bridging with Microchip USB4715 and USB49xx Hubs*", which can be found on the Microchip USB4916 product page at www.microchip.com/USB4916.

8.4 USB to SMBus/I^{2}C Bridging

The USB to SMBus/I^{2}C bridging feature of the USB4916 provides system designers expanded system control and potential BOM reduction. The use of a separate USB to SMBus/I^{2}C device is no longer required and a downstream USB port is not lost, as occurs when a standalone USB to SMBus/I^{2}C device is implemented.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Configure SMBus/I^{2}C Pass-Through Interface
- SMBus/I^{2}C Write
- SMBus/I^{2}C Read

For detailed information on utilizing the USB4916 USB to SMBus/I^{2}C bridging feature, refer to the application note "*AN2438 - USB to I^{2}C Bridging with Microchip USB4715 and USB49xx Hubs*", which can be found on the Microchip USB4916 product page at www.microchip.com/USB4916.

8.5 USB to SPI Bridging

The USB to SPI bridging feature of the USB4916 provides system designers expanded system control and potential BOM reduction. The use of a separate USB to SPI device is no longer required and a downstream USB port is not lost, as occurs when a standalone USB to SPI device is implemented.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Enable SPI Pass-Through Interface
- SPI Write/Read
- Disable SPI Pass-Through Interface

For detailed information on utilizing the USB4916 USB to SPI bridging feature, refer to the application note "*AN2430 - USB to SPI Bridging with Microchip USB4715 and USB49xx Hubs*", which can be found on the Microchip USB4916 product page at www.microchip.com/USB4916.

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8.6 USB to UART Bridging

The USB to UART bridging feature of the USB4916 provides system designers with expanded system control and potential BOM reduction. When using Microchip's USB hubs, a separate USB to UART device is no longer required and a downstream USB port is not lost, as occurs when a standalone USB to UART device is implemented.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Enable/Disable UART Interface
- Set UART Interface Baud Rate
- UART Write
- UART Read

For detailed information on utilizing the USB4916 USB to UART bridging feature, refer to the application note "*AN2426 - USB to UART Bridging with Microchip USB4715, USB4916, and USB4927 Hubs*", which can be found on the Microchip USB4916 product page at www.microchip.com/USB4916.

8.7 Link Power Management (LPM)

The device supports the L0 (On), L1 (Sleep), and L2 (Suspend) link power management states. These supported LPM states offer low transitional latencies in the tens of microseconds versus the much longer latencies of the traditional USB suspend/resume in the tens of milliseconds. The supported LPM states are detailed in Table 8-1.

TABLE 8-1: LPM STATE DEFINITIONS

State	Description	Entry/Exit Time to L0
L2	Suspend	Entry: ~3 ms Exit: ~2 ms (from start of RESUME)
L1	Sleep	Entry: <10 us Exit: <50 us
L0	Fully Enabled (On)	-

8.8 Port Power Control

Port power and over-current sense share the same pin (**PRT_CTLx**) for each port. These functions can be controlled directly from the USB hub, or via the processor.

The device can be configured into the following port control modes:

- Ganged Mode
- Combined Mode

8.8.1 PORT CONNECTION IN GANGED MODE

In this mode, one pin (**PRT_CTL_GANG**) is used to control port power and over-current sensing.

8.8.2 PORT CONNECTION IN COMBINED MODE

8.8.2.1 Port Power Control using USB Power Switch

When operating in combined mode, the device will have one port power control and over-current sense pin for each downstream port. When disabling port power, the driver will actively drive a '0'. To avoid unnecessary power dissipation, the pull-up resistor will be disabled at that time. When port power is enabled, it will disable the output driver and enable the pull-up resistor, making it an open drain output. If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmidt trigger input will recognize that as a low. The open drain output does not interfere. The over-current sense filter handles the transient conditions such as low voltage while the device is powering up.

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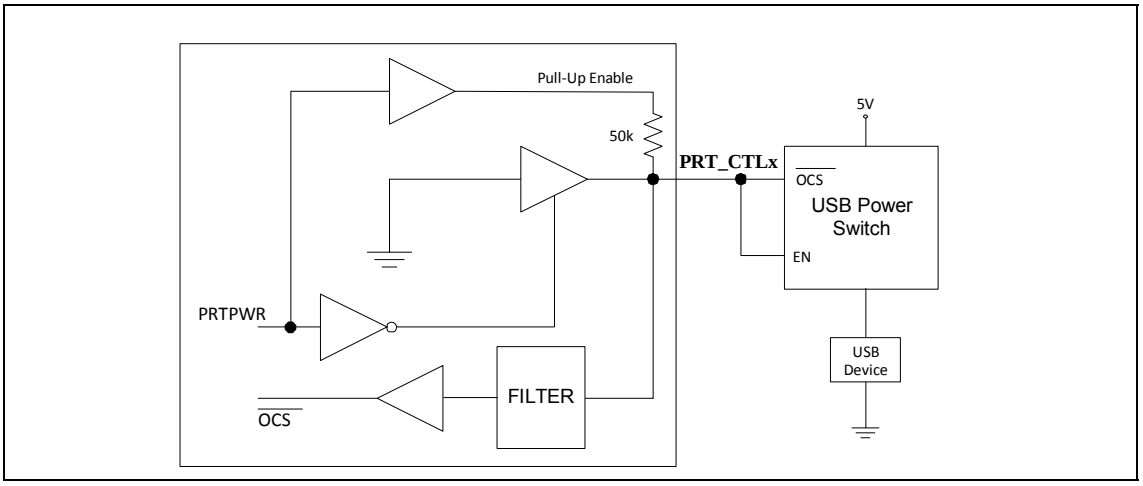
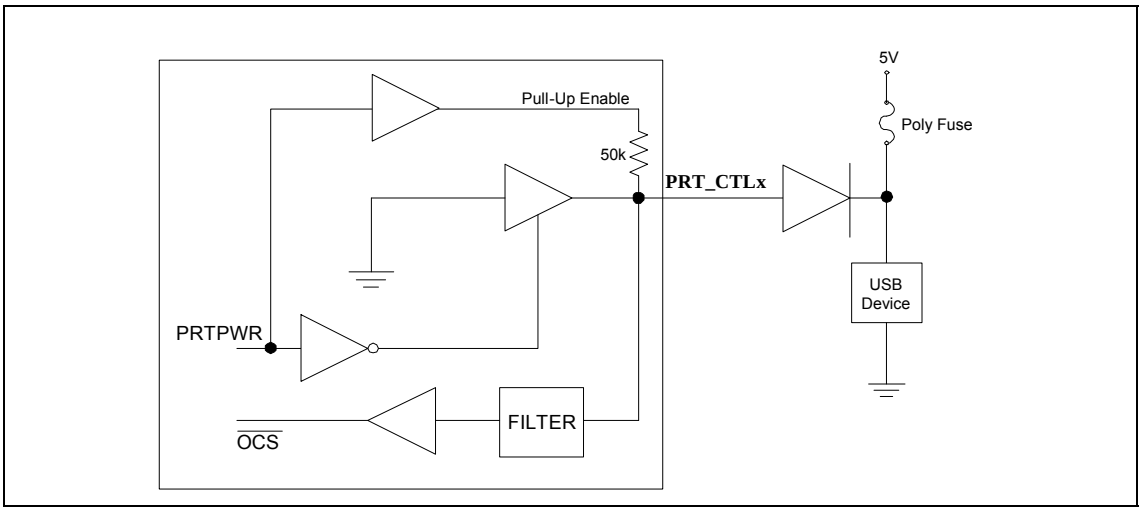
FIGURE 8-2: PORT POWER CONTROL WITH USB POWER SWITCH



8.8.2.2 Port Power Control using Poly Fuse

When using the device with a poly fuse, there is no need for an output power control. To maintain consistency, the same circuit will be used. A single port power control and over-current sense for each downstream port is still used from the Hub's perspective. When disabling port power, the driver will actively drive a '0'. This will have no effect as the external diode will isolate pin from the load. When port power is enabled, it will disable the output driver and enable the pull-up resistor. This means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to 0 volts. The anode of the diode will be at 0.7 volts, and the Schmidt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

FIGURE 8-3: PORT POWER CONTROL USING A POLY FUSE



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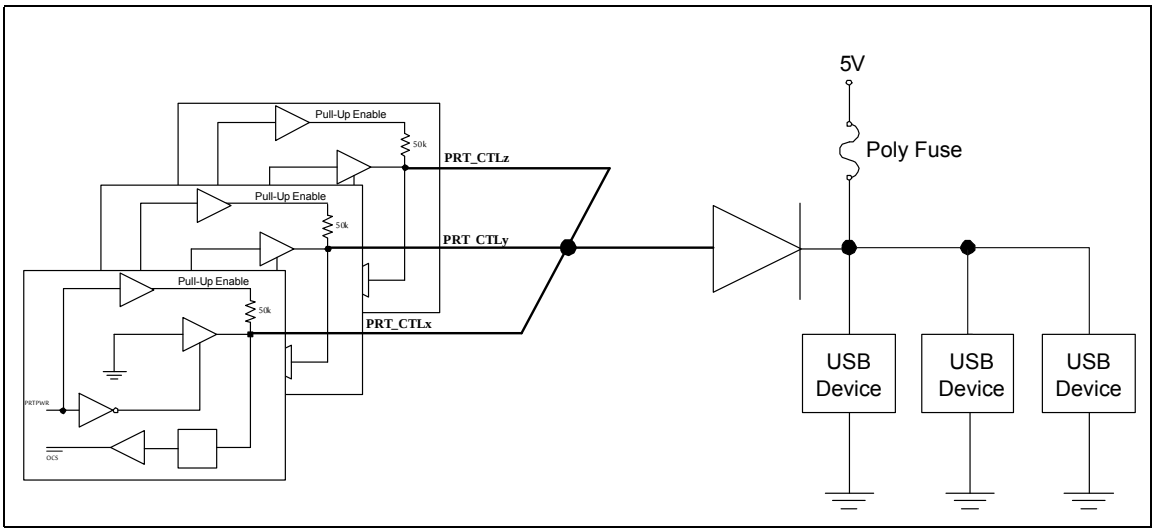
8.8.2.3 Port Power Control with Single Poly Fuse and Multiple Loads

Many customers use a single poly fuse to power all their devices. For the ganged situation, all power control pins must be tied together.

FIGURE 8-4: PORT POWER CONTROL WITH GANGED CONTROL WITH POLY FUSE



8.9 Resets

The device includes the following chip-level reset sources:

- Power-On Reset (POR)
- External Chip Reset (RESET_N)
- USB Bus Reset

8.9.1 POWER-ON RESET (POR)

A power-on reset occurs whenever power is initially supplied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset per the specifications listed in Section 9.6.2, "Power-On and Configuration Strap Timing," on page 37.

8.9.2 EXTERNAL CHIP RESET (RESET_N)

A valid hardware reset is defined as assertion of **RESET_N**, after all power supplies are within operating range, per the specifications in Section 9.6.3, "Reset and Configuration Strap Timing," on page 38. While reset is asserted, the device (and its associated external circuitry) enters Standby Mode and consumes minimal current.

Assertion of **RESET_N** causes the following:

1. The PHY is disabled and the differential pairs will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.

Note:	All power supplies must have reached the operating levels mandated in Section 9.2, "Operating Conditions**," on page 34, prior to (or coincident with) the assertion of **RESET_N**.

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8.9.3 USB BUS RESET

In response to the upstream port signaling a reset to the device, the device performs the following:

1. Sets default address to 0.
2. Sets configuration to Unconfigured.
3. Moves device from suspended to active (if suspended).
4. Complies with the USB Specification for behavior after completion of a reset sequence.

The host then configures the device in accordance with the USB Specification.

Note:	The device does not propagate the upstream USB reset to downstream devices.

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9.0 OPERATIONAL CHARACTERISTICS

9.1 Absolute Maximum Ratings*

+3.3 V Supply Voltage (**VDDIO33**, **VDDPLLREF33**) (Note 9-1) . . . . . -0.5 V to +4.6 V

Positive voltage on input signal pins, with respect to ground (Note 9-2) . . . . . +4.6 V

Negative voltage on input signal pins, with respect to ground . . . . . -0.5 V

Positive voltage on **XTALI/CLK_IN**, with respect to ground . . . . . +2.1 V

Positive voltage on USB DP/DM signal pins, with respect to ground . . . . . +6.0 V

Storage Temperature . . . . . -55°C to +150°C

Junction Temperature . . . . . +125°C

Lead Temperature Range . . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . . 5 kV

Note 9-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested to use a clamp circuit.

Note 9-2 This rating does not apply to the following pins: All USB DM/DP pins, **XTAL1/CLK_IN**, and **XTALO**

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 9.2, "Operating Conditions**", Section 9.5, "DC Specifications", or any other applicable section of this specification is not implied.

9.2 Operating Conditions**

+3.3 V Supply Voltage (**VDDIO33**, **VDDPLLREF33**) . . . . . +3.0 V to +3.6 V

Input Signal Pins Voltage (Note 9-2) . . . . . -0.3 V to +3.6 V

XTALI/CLK_IN Voltage . . . . . -0.3 V to +1.5 V

USB 2.0 DP/DM Signal Pins Voltage . . . . . -0.3 V to +5.5 V

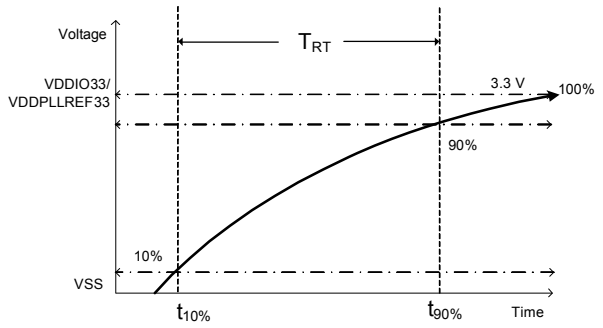
Ambient Operating Temperature in Still Air (T_A) . . . . . -40°C to +85°C

+3.3 V Supply Voltage Rise Time (T_{RT} in Figure 9-1) . . . . . 400 µs

**Proper operation of the device is guaranteed only within the ranges specified in this section.

Note: Do not drive input signals without power supplied to the device.

FIGURE 9-1: POWER SUPPLY RISE TIME MODEL



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Note: The rise time for the 3.3V supply can be extended to 100ms max if RESET_N is actively driven low, typically by another IC, until 1 µs after all supplies are within operating range.

9.3 Package Thermal Specifications

TABLE 9-1: PACKAGE THERMAL PARAMETERS

Symbol	°C/W	Velocity (Meters/s)
Θ_{JA}	25	0
	22	1
Θ_{JB}	14	0
Ψ_{JT}	0.2	0
Θ_{JC}	2.3	0

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51.

9.4 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

TABLE 9-2: DEVICE POWER CONSUMPTION

Description	Typical Current (mA)	Maximum Current (mA)
Reset Current (mA)	0.40	3.60
Suspend Current (mA)	0.40	3.60
Idle	63	77
Active Operation (5 Hi-Speed Devices)	181	198
Active Operation (1 Hi-Speed, 1 Full-Speed Device)	86	87
Active Operation (2 Hi-Speed, 2 Full-Speed Devices)	110	111
Active Operation (2 Hi-Speed, 1 Full-Speed Device)	109	110
Active Operation (4 Hi-Speed, 1 Full-Speed Device)	147	152
Active Operation (1 Full-Speed Device)	69	70
Active Operation (5 Full-Speed Devices)	75	76
Active Operation (1 Hi-Speed Device)	83	84
Active Operation (2 Hi-Speed Devices)	111	112
Active Operation (3 Hi-Speed Devices)	132	134
Active Operation (4 Hi-Speed Devices)	153	154
Active Operation (Multi-Host Endpoint Reflector enabled on 1 port, Hi-Speed data transfer on other 4 ports)	146	148

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9.5 DC Specifications

TABLE 9-3: I/O DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Units	Notes
I Type Input Buffer						
Low Input Level	V_{IL}	-0.3		Note 9-3	V	
High Input Level	V_{IH}	1.25		**VDDIO33**+0.3	V	
IS Type Input Buffer						
Low Input Level	V_{IL}	-0.3		Note 9-3	V	
High Input Level	V_{IH}	1.25		**VDDIO33**+0.3	V	
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	100	160	240	mV	
O4 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4 mA
High Output Level	V_{OH}	**VDD33**-0.4			V	I_{OH} = -4 mA
O12 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
High Output Level	V_{OH}	**VDD33**-0.4			V	I_{OH} = -12 mA
OD12 Type Output Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
ICLK Type Input Buffer (XTALI/CLK_IN Input)						Note 9-4
Low Input Level	V_{IL}	-0.2		0.35	V	
High Input Level	V_{IH}	0.9		1.2	V	
Input Capacitance	C_{IN}			2	pF	
I/O-U Type Buffer (See Note 9-5)						Note 9-5

Note 9-3 0.42V for interfaces using open drain with pull-ups to voltages up to 2.1V,
0.34V for interfaces using open drain with pull-ups to voltages greater than 2.1V

Note 9-4 **XTALI** can optionally be driven from a 25 MHz singled-ended clock oscillator.

Note 9-5 Refer to the *Universal Serial Bus Revision 2.0 Specification* for USB DC electrical characteristics.

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9.6 AC Specifications

This section details the various AC timing specifications of the device.

9.6.1 POWER SUPPLY AND RESET_N SEQUENCE TIMING

Figure 9-2 illustrates the recommended power supply sequencing and timing for the device. **RESET_N** and/or **VBUS_DET** should rise after or at the same rate as **VDDIO33/VDDPLLREF33**. **VBUS_DET** and **RESET_N** do not have any other timing dependencies.

FIGURE 9-2: POWER SUPPLY AND RESET_N SEQUENCE TIMING

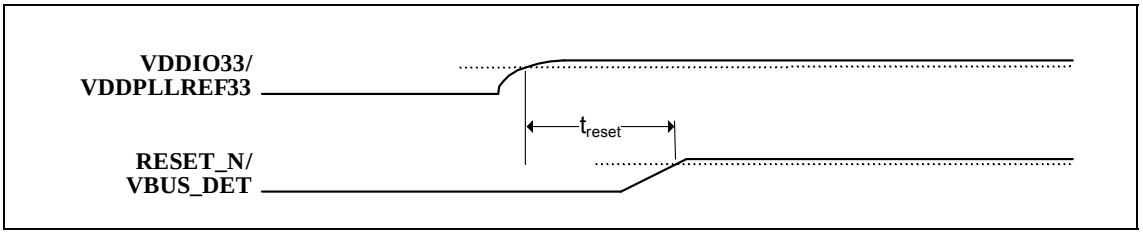

TABLE 9-4: POWER SUPPLY AND RESET_N SEQUENCE TIMING

Symbol	Description	Min	Typ	Max	Units
t_{reset}	**VDDIO33/VDDPLLREF33** to **RESET_N/VBUS_DET** rise time	0			ms

9.6.2 POWER-ON AND CONFIGURATION STRAP TIMING

Figure 9-3 illustrates the configuration strap valid timing requirements in relation to power-on, for applications where **RESET_N** is not used at power-on. In order for valid configuration strap values to be read at power-on, the following timing requirements must be met. The operational levels (V_{opp}) for the external power supplies are detailed in Section 9.2, "Operating Conditions**," on page 34.

FIGURE 9-3: POWER-ON CONFIGURATION STRAP VALID TIMING

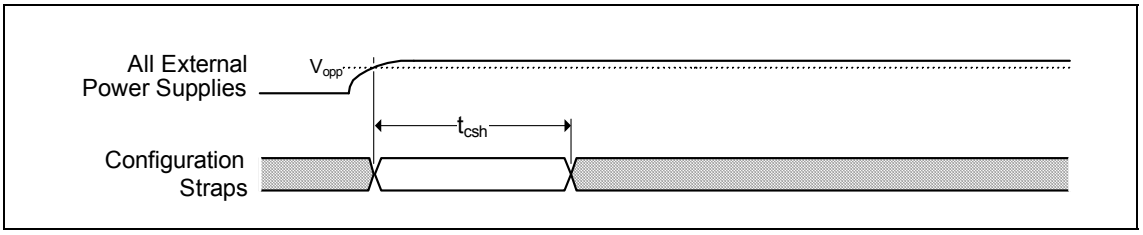

TABLE 9-5: POWER-ON CONFIGURATION STRAP LATCHING TIMING

Symbol	Description	Min	Typ	Max	Units
t_{csh}	Configuration strap hold after external power supplies at operational levels	1			ms

Device configuration straps are also latched as a result of **RESET_N** assertion. Refer to Section 9.6.3, "Reset and Configuration Strap Timing" for additional details.

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9.6.3 RESET AND CONFIGURATION STRAP TIMING

Figure 9-4 illustrates the **RESET_N** pin timing requirements and its relation to the configuration strap pins. Assertion of **RESET_N** is not a requirement. However, if used, it must be asserted for the minimum period specified. Refer to Section 8.9, "Resets" for additional information on resets. Refer to Section 3.3, "Configuration Straps and Programmable Functions" for additional information on configuration straps.

FIGURE 9-4: RESET_N CONFIGURATION STRAP TIMING

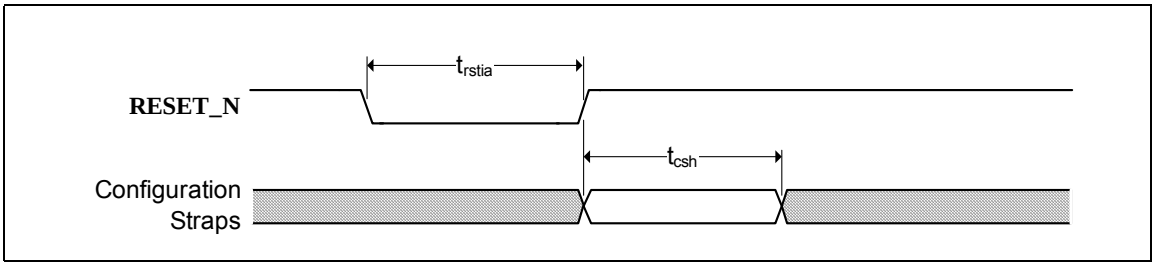

TABLE 9-6: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	**RESET_N** input assertion time	5			µs
t_{csh}	Configuration strap pins hold after **RESET_N** deassertion	1			ms

Note: The clock input must be stable prior to **RESET_N** deassertion.

Configuration strap latching and output drive timings shown assume that the Power-On reset has finished first otherwise the timings in Section 9.6.2, "Power-On and Configuration Strap Timing" apply.

9.6.4 USB TIMING

All device USB signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *Universal Serial Bus 2.0 Specification*. Please refer to the *Universal Serial Bus Revision 2.0 Specification*, available at http://www.usb.org/developers/docs/usb20_docs/.

9.6.5 SMBUS TIMING

All device SMBus signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *System Management Bus Specification.* Please refer to the *System Management Bus Specification*, Version 1.0, available at http://smbus.org/specs.

9.6.6 I^2C TIMING

All device I^2C signals conform to the 400KHz Fast Mode (Fm) voltage, power, and timing characteristics/specifications as set forth in the *I^2C-Bus Specification*. Please refer to the *I^2C-Bus Specification*, available at http://www.nxp.com/documents/user_manual/UM10204.pdf.

9.6.7 I^2S TIMING

All device I^2S signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *I^2S-Bus Specification*. Please refer to the *I^2S-Bus Specification*, available at http://www.nxp.com/acrobat_download/various/I2SBUS.pdf.

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9.6.8 SPI/SQI TIMING

This section specifies the SPI/SQI timing requirements for the device.

FIGURE 9-5: SPI/SQI TIMING

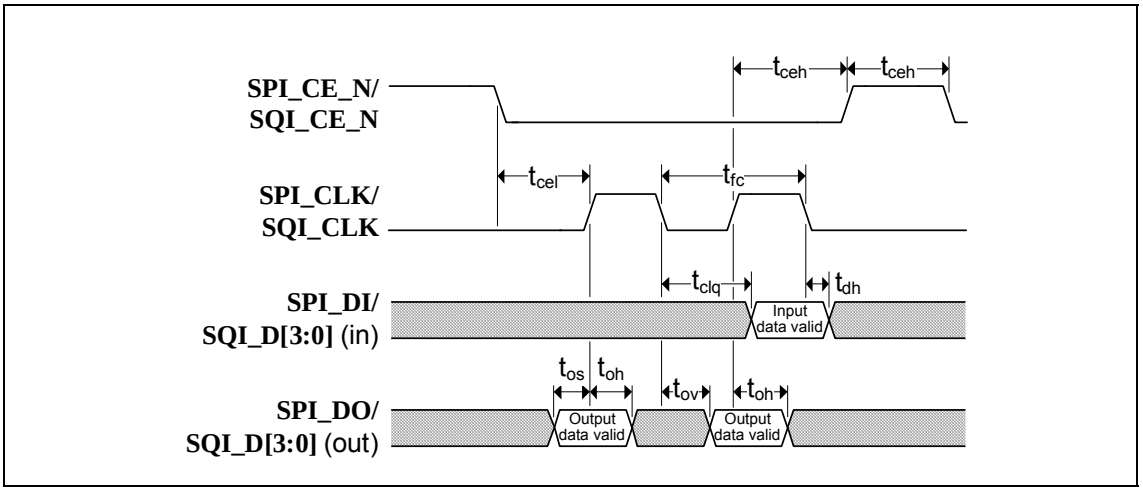

TABLE 9-7: SPI/SQI TIMING (30 MHZ OPERATION)

Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency			30	MHz
t_{ceh}	Chip enable (**SPI_CE_N/SQI_CE_N**) high time	100			ns
t_{clq}	Clock to input data			13	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	5			ns
t_{oh}	Output hold time	5			ns
t_{ov}	Clock to output valid	4			ns
t_{cel}	Chip enable (**SPI_CE_N/SQI_CE_N**) low to first clock	12			ns
t_{ceh}	Last clock to chip enable (**SPI_CE_N/SQI_CE_N**) high	12			ns

TABLE 9-8: SPI/SQI TIMING (60 MHZ OPERATION)

Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency			60	MHz
t_{ceh}	Chip enable (**SPI_CE_N/SQI_CE_N**) high time	50			ns
t_{clq}	Clock to input data			9	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	5			ns
t_{oh}	Output hold time	5			ns
t_{ov}	Clock to output valid	4			ns
t_{cel}	Chip enable (**SPI_CE_N/SQI_CE_N**) low to first clock	12			ns
t_{ceh}	Last clock to chip enable (**SPI_CE_N/SQI_CE_N**) high	12			ns

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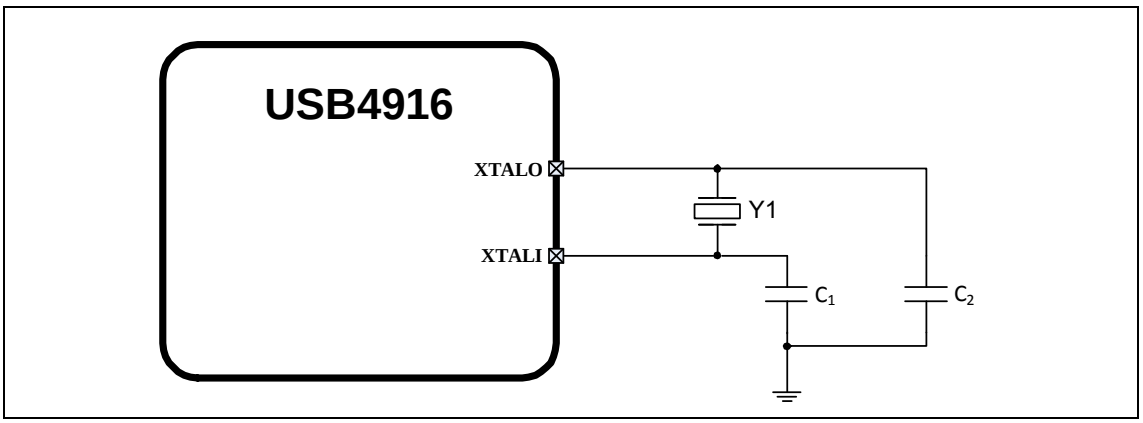
9.7 Clock Specifications

The device can accept either a 25MHz crystal or a 25MHz single-ended clock oscillator input. If the single-ended clock oscillator method is implemented, **XTALO** should be left unconnected and **XTALI/CLK_IN** should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XTALI/XTALO**). The following circuit design (Figure 9-6) and specifications (Table 9-9) are required to ensure proper operation.

FIGURE 9-6: 25MHZ CRYSTAL CIRCUIT



9.7.1 CRYSTAL SPECIFICATIONS

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XTALI/XTALO**). Refer to Table 9-9 for the recommended crystal specifications.

TABLE 9-9: CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut	AT, typ					
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	±50	PPM	
Frequency Stability Over Temp	F_{temp}	-	-	±50	PPM	
Frequency Deviation Over Time	F_{age}	-	±3 to 5	-	PPM	Note 9-6
Total Allowable PPM Budget		-	-	±100	PPM	
Shunt Capacitance	C_O	-	7 typ	-	pF	
Load Capacitance	C_L	-	20 typ	-	pF	
Drive Level	P_W	100	-	-	uW	
Equivalent Series Resistance	R_1	-	-	50	Ω	
Operating Temperature Range		-40	-	+85	°C	
XTALI/CLK_IN Pin Capacitance		-	3 typ	-	pF	Note 9-7
XTALO Pin Capacitance		-	3 typ	-	pF	Note 9-7

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Note 9-6 Frequency Deviation Over Time is also referred to as Aging.

Note 9-7 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The **XTALI/CLK_IN** pin, **XTALO** pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

9.7.2 EXTERNAL REFERENCE CLOCK (CLK_IN)

When using an external reference clock, the following input clock specifications are suggested:

- 25 MHz
- 50% duty cycle ±10%, ±100 ppm
- Jitter < 100 ps RMS

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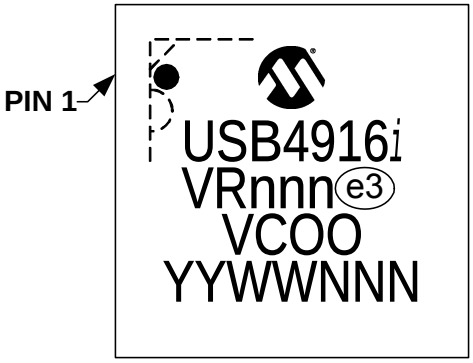
10.0 PACKAGE INFORMATION

Note: Package offerings are currently under review and are subject to change.

64-VQFN (9x9 mm)



Legend:	*i*	Temperature range designator (VAutomotive
	R	Product revision
	nnn	Internal code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	V	Plant of assembly
	COO	Country of origin
	YY	Year code (last two digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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10.1 64-VQFN

FIGURE 10-1: 64-VQFN PACKAGE (DRAWING)

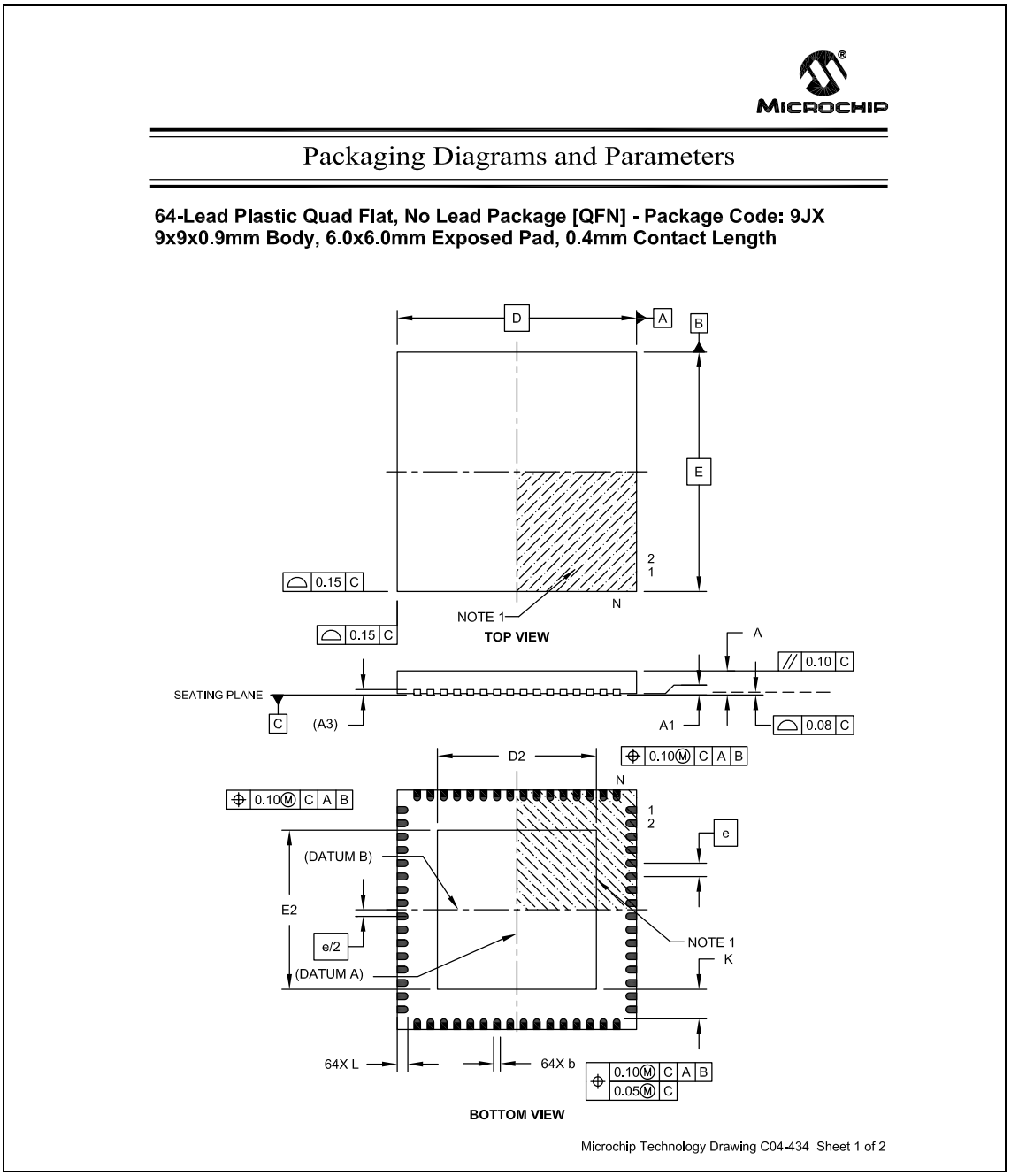

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FIGURE 10-1: 64-VQFN PACKAGE (DRAWING) (CONTINUED)

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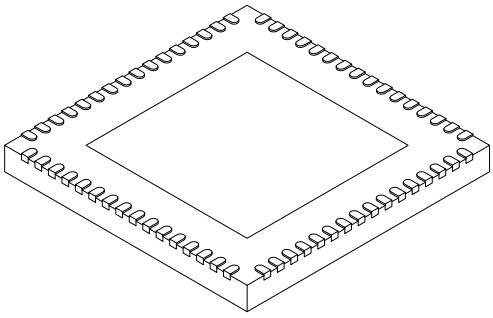
Packaging Diagrams and Parameters

64-Lead Plastic Quad Flat, No Lead Package [QFN] - Package Code: 9JX
9x9x0.9mm Body, 6.0x6.0mm Exposed Pad, 0.4mm Contact Length



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	5.90	6.00	6.10
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	5.90	6.00	6.10
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.90	1.10	-

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-434 Sheet 2 of 2

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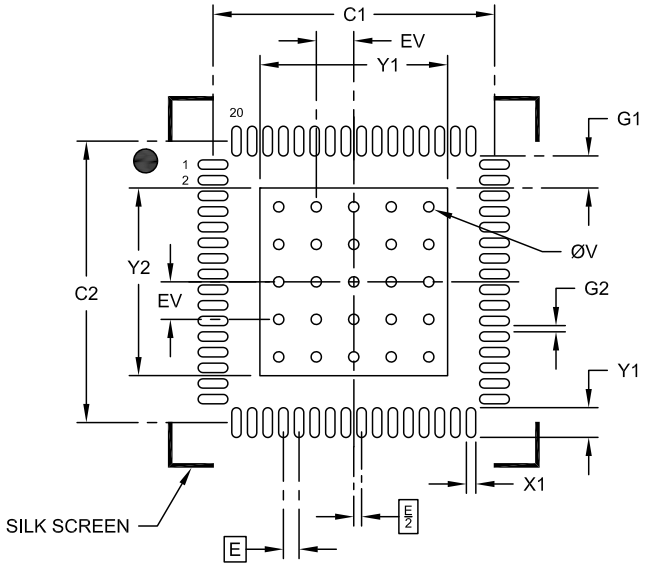
FIGURE 10-2: 64-VQFN PACKAGE (LAND PATTERN)

64-Lead Very Thin Plastic Quad Flat, No Lead Package (9JX) – 9x9x0.9 mm Body [VQFN]
With 6.0 x 6.0 Exposed Pad and 0.4mm Terminal Length [Also called QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			6.10
Optional Center Pad Length	Y2			6.10
Contact Pad Spacing	C1		9.00	
Contact Pad Spacing	C2		9.00	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.95
Contact Pad to Center Pad (X64)	G1	1.00		
Spacing Between Contact Pads (X60)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2434 [9JX]

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APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002528A (09-07-17)	All	Initial Release.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/	XXX	XXX
Device	Tape and Reel Option		Temperature Range		Package	Automotive Code

Device:	USB4916= 5 Downstream Ports, 1 Upstream Port	
Tape and Reel Option:	Blank	= Standard packaging (tray)
	T	= Tape and Reel (Note 1)
Temperature Range:	I	= -40°C to +85°C
Package:	9JX	= 64-pin VQFN
	TBD	= 64-pin VQFN (Wettable Flanks)
Automotive Code:	Vxx	= 3 character code with "V" prefix, specifying automotive product.

Examples:

a) USB4916-I/9JXVAA
Tray, -40°C to+85°C, 64-pin VQFN

b) USB4916T-I/9JXVAA
Tape & reel, -40°C to+85°C, 64-pin VQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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