

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

GREENTHREAD, LLC

Plaintiff,

vs.

**ON SEMICONDUCTOR CORPORATION;
SEMICONDUCTOR COMPONENTS
INDUSTRIES, LLC D/B/A ON
SEMICONDUCTOR LLC**

Defendants.

Civil Action No.

JURY TRIAL DEMANDED

ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Greenthread, LLC (“Greenthread” or “Plaintiff”) files this Original Complaint against Defendants ON Semiconductor Corporation, Semiconductor Components Industries, LLC d/b/a ON Semiconductor LLC (collectively “ON Semiconductor” or “Defendants”) and hereby alleges as follows:

THE NATURE OF THE ACTION

1. Greenthread owns a family of patents related to transistors and other components of integrated semiconductor devices. Greenthread’s patented inventions describe semiconductor devices that employ graded dopants and well regions for creating electric fields for aiding and/or limiting the movement of carriers to (or from) the semiconductor surface to (or from) the semiconductor substrate. These inventions improve semiconductor devices by (1) creating faster, more efficient, and more reliable processors, logic devices, and image sensors and (2) allowing manufacturers to scale down the feature size of their semiconductor products.

2. Defendants have infringed and continue to infringe two Greenthread patents:

10,510,842 (the “’842 Patent”), and 11,121,222 (the “’222 Patent) (collectively “the Greenthread Patents”), copies of which are attached hereto as Exhibits 1-2, respectively. Defendants have infringed and continue to infringe the Greenthread Patents by making, using, selling, offering for sale, and/or importing into the United States, semiconductor devices with infringing graded dopant regions and/or electronic products containing the same.

THE PARTIES

3. Plaintiff Greenthread, LLC (“Greenthread”) is a limited liability company organized and existing under the laws of Texas, having its principal place of business at 7424 Mason Dells Drive, Dallas, Texas 75230-3244.

4. Defendant ON Semiconductor Corporation is a corporation organized and existing under the laws of Delaware, having its principal place of business at 5005 East McDowell Road, Phoenix, Arizona, 85008. ON Semiconductor Corporation may be served through its registered agent the Corporation Trust Company at Corporation Trust Center 1209 Orange Street, Wilmington, Delaware 19801.

5. Defendant Semiconductor Components Industries, LLC., is a limited liability company with its principal place of business at 5005 East McDowell Road, Phoenix, Arizona, 85008. Upon information and belief, Semiconductor Components Industries, LLC., is the principal domestic operating subsidiary of ON Semiconductor Corporation and does business under the name of ON Semiconductor. Upon information and belief, Semiconductor Components Industries, LLC is a wholly-owned subsidiary of ON Semiconductor Corporation.

6. ON Semiconductor designs, manufactures, and markets a comprehensive portfolio of semiconductor products. More specifically, ON Semiconductor describes itself as a supplier of

“intelligent power and sensing technologies that solve the most challenging customer problems.”¹

ON Semiconductor further describes itself as a “leader in intelligent power and sensing” that has “pivoted our investments to align with the high-growth megatrends in automotive and industrial.”²

7. Upon information and belief, Defendants are part of the same corporate structure and distribution chain for the making, importing, designing, manufacturing, offering to sell, selling, and/or using of the ON Semiconductor Accused Products in the United States, including in the state of Delaware generally and in this judicial district in particular. Upon information and belief, Defendants and their affiliates share the same management, common ownership, advertising platforms, facilities, distribution chains and platforms, and product lines involving the ON Semiconductor Accused Products.

SUBJECT MATTER JURISDICTION

8. This action arises under the patent laws of the United States, namely 35 U.S.C. §§ 271, 281, and 284-285, among others.

9. This court has subject matter jurisdiction over the patent infringement claims asserted in this case under 28 U.S.C. §§ 1331 and 1338(a).

PERSONAL JURISDICTION AND VENUE

10. This Court has specific personal jurisdiction over Defendants because they have committed acts within this District giving rise to this action (including acts of infringement) and have established minimum contacts with this forum such that the exercise of jurisdiction over Defendants would not offend traditional notions of fair play and substantial justice. Such acts

¹ <https://investor.onsemi.com/static-files/e6394327-d8e6-48f9-81ab-2ff550c298e6>

² *Id.*

include selling ON Semiconductor Accused Products.

11. The Court has general personal jurisdiction over ON Semiconductor Corporation because it is incorporated in Delaware.

12. The Court has general personal jurisdiction over Semiconductor Components Industries, LLC, because its sole member is a Delaware corporation, ON Semiconductor Corporation.

13. Venue is proper under 28 U.S.C. §§ 1391(b) and 1400(b), because Defendants reside in this District.

14. “ON Semiconductor Accused Products” are products accused of meeting the claim limitations of a Greenthread Patent in this suit. Defendants designs and manufactures semiconductor devices containing transistors and other structures that infringe the Greenthread Patents in the United States. The infringing structures within semiconductor devices have application in many types of devices designed and manufactured by ON Semiconductor, including discrete & power modules, power management, signal conditioning & control, sensors, motor control, custom & audio/video application-specific standard products (ASSP), interfaces, wireless connectivity, and timing, logic, and memory devices.³

15. Exhibit 4 demonstrates how exemplary ON Semiconductor Accused Products meet the claim limitations of Greenthread Patents and is herein incorporated by reference.

THE GREENTHREAD PATENTS

16. On December 17, 2019, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 10,510,842 (“the ’842 Patent”), entitled “Semiconductor Devices with

³ <https://www.onsemi.com/products>

Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed on May 9, 2017. The ’842 Patent claims priority from U.S. Patent Application No. 10/934,915,⁴ filed on September 3, 2004. A true and correct copy of the ’842 Patent is attached hereto as Exhibit 1 and incorporated herein by reference.

17. On September 14, 2021, the U.S. Patent and Trademark Office duly and legally issued U.S. Patent No. 11,121,222 (“the ’222 Patent”), entitled “Semiconductor Devices with Graded Dopant Regions,” listing Dr. Mohan Rao as the inventor, from a patent application filed on July 27, 2020. The ’222 Patent claims priority from U.S. Patent Application No. 10/934,915,⁵ filed on September 3, 2004. A true and correct copy of the ’222 Patent is attached hereto as Exhibit 2 and incorporated herein by reference.

18. The ’842 and the ’222 Patents are collectively referred to as the “Greenthread Patents.”

19. Greenthread exclusively owns all rights, title, and interest in the Greenthread Patents necessary to bring this action, including the right to recover past and future damages. Certain of the Greenthread Patents were previously owned by Dr. G.R. Mohan Rao (“Dr. Rao”). On April 27, 2015, Dr. Rao assigned to Greenthread the then-issued Greenthread Patents and all related “continuations, continuations-in-part and extensions of said Applications and Patents and any pending applications or issued patents that directly claim or are amended to claim priority to any of the Applications or Patents.” Dr. Rao’s assignment was recorded with the U.S. Patent and Trademark Office on May 13, 2015, and again on July 22, 2021, and is attached hereto as Exhibit 3. Greenthread has therefore owned all rights to the Greenthread Patents necessary to bring this

⁴ Pub. No. US 2006/0049464.

⁵ Pub. No. US 2006/0049464.

action throughout the period of ON Semiconductor's infringement and still owns those rights to the Greenthread Patents.

20. Defendants are not currently licensed to practice the Greenthread Patents.

21. The Greenthread Patents are valid and enforceable.

FACTUAL BACKGROUND

22. Dr. G.R. Mohan Rao ("Dr. Rao"), the sole inventor of the Greenthread Patents, has been an innovator in the semiconductor industry since the 1960s. He is a named inventor on more than 100 Patents worldwide and authored numerous technical publications over the last 50 years.

23. In September 1968, Dr. Rao received a Ph.D. in physics with a specialization in electronics from Andhra University in Waltair, India. He then traveled to the United States to attend a graduate program in physics at the University of Cincinnati.

24. After learning of an opportunity to work with Professor William Carr of Southern Methodist University ("SMU"), Dr. Rao transferred to SMU where he earned a Ph.D. in Electrical Engineering. While there, he worked in the SMU laboratory with Jack Kilby of Texas Instruments (a pioneering electrical engineer who would later receive a Nobel Prize for his work), on metal-oxide-silicon transistors ("MOS devices"), which are used for switching and amplifying electronic signals in electronic devices. MOS devices form the basis of modern electronics and are the most widely used semiconductor devices in the world. The U.S. Patent and Trademark Office has called this device a "groundbreaking invention that transformed life and culture around the world."⁶ Dr. Rao built these devices from scratch while a graduate student at SMU.

25. Through his mentor, Jack Kilby, Dr. Rao interviewed with—and was ultimately hired by—Texas Instruments to continue his work on MOS devices in 1972. Dr. Rao worked at

⁶ <https://www.uspto.gov/about-us/news-updates/remarks-director-iancu-2019-international-lectual-property-conference>

Texas Instruments for the next twenty-two years, rising from an engineer to a Senior Fellow. At that time, Texas Instruments had only 12 Senior Fellows out of approximately 20,000 engineers. Eventually, Dr. Rao moved into a management position at Texas Instruments, ultimately becoming a Senior Vice President in 1985.

26. At Texas Instruments, Dr. Rao received his first patent while working in a process and product engineering capacity to solve a production problem with Texas Instruments' 4-kilobit RAM product. That patent was merely the beginning of Dr. Rao's long inventive career. Indeed, from the late 1970s through the mid-1980s, Dr. Rao worked on or managed projects relating to Texas Instruments' 64kb RAM, 256Kb RAM, 1Mb RAM, 4 Mb RAM, EEPROM, SRAM, and microcontrollers. For that work, Dr. Rao received numerous additional U.S. Patents.

27. The USPTO was not the only organization to recognize Dr. Rao's achievements. Some of Dr. Rao's work at Texas Instruments was so remarkable that it has been credited in multiple exhibits in the National Museum of American History at the Smithsonian Institution.⁷ For example, the Smithsonian has displayed Texas Instruments' experimental 1-megabit CMOS DRAM, produced in April 1985 under Dr. Rao's leadership, and credited Dr. Rao for the achievement.⁸

⁷ <http://smithsonianchips.si.edu/texas/wafer.htm>

⁸ http://smithsonianchips.si.edu/texas/t_360.htm



28. In 1994, Dr. Rao left Texas Instruments for Cirrus Logic. During his two-year tenure at Cirrus Logic, he received more U.S. Patents relating to his work on integrated graphics controllers and memory.

29. In 1996, Dr. Rao started a company called Silicon Aquarius. Through a relationship between Silicon Aquarius and Matsushita, Dr. Rao led a design team in working on a 256Mb DRAM chip. After Silicon Aquarius ceased operations, Dr. Rao did consulting work for a number of different consulting companies and devoted much of his free time to thinking about various challenges and problems with which the semiconductor industry had struggled for years.

30. In 2003, Dr. Rao and Philip John founded Greenthread to continue Dr. Rao's pioneering work. A focal point of Dr. Rao's research was poor refresh time and the related problem of how to deal with and control the movement of both wanted and unwanted carriers in semiconductor devices, including memory and logic devices. Dr. Rao realized that graded dopants

could be used to create a “drift layer” and other structures to facilitate the movement—in an upward or downward direction, as appropriate—of carriers from the semiconductor surfaces down into the substrate and vice versa. It was Dr. Rao’s work on this problem that culminated in the Greenthread Patents.

ON SEMICONDUCTOR’S INFRINGEMENT

31. ON Semiconductor has directly infringed, and continues to infringe, one or more claims of each of the Greenthread Patents through making, using, offering to sell, selling within the United States, and/or importing into the United States semiconductor products, including AR0820AT, that practice the claimed inventions (*i.e.*, the ON Semiconductor Accused Products). A non-exhaustive, exemplary list of the types or categories of products or devices that infringe are further identified in Exhibit 4.

32. As shown in Exhibit 4, the exemplary ON Semiconductor Accused Product, AR0820AT, meets each and every element of at least one claim of the Greenthread Patents.

33. Upon information and belief, ON Semiconductor fabricates and designs the ON Semiconductor Accused Products using similar designs according to a limited number of processes, many or all of which utilize substantially similar process steps, including process steps for creating regions with graded dopant concentrations, because the invention would have application in those categories of products, for example by improving switching time in transistors in the ON Semiconductor Accused Products. Upon information and belief, the ON Semiconductor Accused Products are in relevant part substantially similar to the exemplary AR0820AT shown in Exhibit 4, particularly with regard to the manner in which the exemplary AR0820AT includes and utilizes regions with graded dopant concentrations. Exhibit 4 is thus illustrative of the manner in which the ON Semiconductor Accused Products meet the claim limitations of the Greenthread

Patents.⁹

COUNT I: INFRINGEMENT OF U.S. PATENT NO. 10,510,842

34. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

35. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the ON Semiconductor Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the ON Semiconductor Accused Products that it obtains during discovery.

36. As alleged above and in Exhibit 4, the products analyzed in Exhibit 4 meet each and every one of the claim limitations of at least one claim of the '842 Patent.

37. As alleged above, the products analyzed in Exhibit 4 are exemplary of the ON

⁹ Multiple courts have upheld Greenthread's construction of the Greenthread Patents in related matters. In *Greenthread, LLC v. Samsung Electronics Co., Ltd. et al.*, Case No. 2:19-cv-00147-JRG (E.D. Tex.), the Eastern District of Texas Court adopted Greenthread's claim construction. See Dkt. 67. In *Greenthread, LLC v. Intel Corp., et al.*, Case No. 6:22-cv-00105-ADA (W.D. Tex), the Western District of Texas similarly issued a preliminary claim construction order adopting Greenthread's construction. See Dkt. 36-21 in *Greenthread, LLC v. Intel Corp.*, Case No. 3:22-cv-02001-JR (attaching as an exhibit the Western District of Texas's preliminary claim construction order in a status update before the District of Oregon). The claims in this matter against Intel were ultimately severed and transferred to Oregon, and the District of Oregon adopted the Western District of Texas' preliminary claim construction. See Dkt. 44 ("The Court also finds that the WDTX's preliminary constructions and summary judgment rulings are neither legally incorrect nor factually distinguishable. As a result, the Court adopts the WDTX's preliminary constructions and summary judgment rulings as its own. . ."). The Western District of Texas also denied Defendants' motions to dismiss and for summary judgment on similar grounds. See Dkt. 36-22 in *Greenthread, LLC v. Intel Corp.*, Case no. 3:22-cv-02001-JR (attaching as an exhibit the Western District of Texas' denial of Defendants' motion for summary judgment); Dkt. 110 in *Greenthread LLC v. Intel Corp.*, Case No. 6:22-cv-00105-ADA (W.D. Tex). The District of Oregon similarly adopted these rulings. See Dkt. 44 in *Greenthread, LLC v. Intel Corp.*, Case no. 3:22-cv-02001-JR.

Semiconductor Accused Products.

38. As alleged above, Defendants have infringed and continue to infringe at least one claim of the '842 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States ON Semiconductor Accused Products.

39. Defendants' infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

COUNT II: INFRINGEMENT OF U.S. PATENT NO. 11,121,222

40. Greenthread incorporates by reference and re-alleges all of the foregoing paragraphs of this Complaint and exhibits attached hereto as if fully set forth herein.

41. The following allegations are based on publicly available information and a reasonable investigation of the structure and operation of the ON Semiconductor Accused Products. Greenthread reserves the right to modify this description, including, for example, on the basis of information about the ON Semiconductor Accused Products that it obtains during discovery.

42. As alleged above and in Exhibit 4, the products analyzed in Exhibit 4 meet each and every one of the claim limitations of at least one claim of the '222 Patent.

43. As alleged above, the products analyzed in Exhibit 4 are exemplary of the ON Semiconductor Accused Products.

44. As alleged above, Defendants have infringed and continue to infringe at least one claim of the '222 Patent by making, using, offering to sell, selling within the United States, and/or importing into the United States ON Semiconductor Accused Products.

45. Defendants' infringement has damaged and continues to damage Greenthread in an amount yet to be determined, of at least a reasonable royalty.

DAMAGES

46. As a result of Defendants' acts of infringement, Greenthread has suffered and continues to suffer actual and consequential damages. However, Greenthread does not yet know the full extent of the infringement and the amount of damages cannot be ascertained except through discovery and special accounting. To the fullest extent permitted by law, Greenthread seeks recovery of damages at least for reasonable royalties, unjust enrichment, and benefits received by Defendant as a result of using the patented technology. Greenthread further seeks any other damages to which Greenthread is entitled under law or in equity.

DEMAND FOR JURY TRIAL

47. Greenthread hereby demands a jury trial for all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, Greenthread respectfully requests that this Court enter judgment in its favor as follows:

- A. That Judgment be entered that Defendants have infringed one or more claims of the Greenthread Patents, literally and under the doctrine of equivalents;
- B. That, in accordance with 35 U.S.C. § 283, Defendants and all their affiliates, employees, agents, officers, directors, attorneys, successors, and assigns and all those acting on behalf of or in active concert or participation with any of them, be preliminarily and permanently enjoined from (1) infringing the Greenthread Patents and (2) making, using, selling, and offering for sale, or importing into the United States, the ON Semiconductor Accused Products;
- C. An award of damages sufficient to compensate Greenthread for Defendants' infringement under 35 U.S.C. § 284;

- D. That the case be found exceptional under 35 U.S.C. § 285 and that Greenthread be awarded its reasonable attorneys' fees;
- E. Costs and expenses in this action;
- F. Damages for pre-issuance infringement under 35 U.S.C. § 154(d);
- G. An award of prejudgment and post-judgment interest; and
- H. Such other and further relief as the Court may deem just and proper.

Dated: April 21, 2023

Respectfully submitted,

FARNAN LLP

/s/ Brian E. Farnan

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EXHIBIT 1



US010510842B2

(12) **United States Patent**
Rao

(10) **Patent No.:** **US 10,510,842 B2**

(45) **Date of Patent:** **Dec. 17, 2019**

(54) **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

H01L 29/7395 (2013.01); *H01L 27/0214* (2013.01); *H01L 27/10844* (2013.01)

(71) Applicant: **GREENTHREAD, LLC**, Dallas, TX (US)

(58) **Field of Classification Search**

CPC *H01L 29/1095*

USPC 257/655

See application file for complete search history.

(72) Inventor: **G.R. Mohan Rao**, Allen, TX (US)

(73) Assignee: **GREENTHREAD, LLC**, Dallas, TX (US)

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/590,282**

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(65) **Prior Publication Data**

US 2017/0243876 A1 Aug. 24, 2017

(Continued)

Related U.S. Application Data

(60) Continuation of application No. 14/931,636, filed on Nov. 3, 2015, now Pat. No. 9,647,070, which is a continuation of application No. 14/515,584, filed on Oct. 16, 2014, now Pat. No. 9,190,502, which is a continuation of application No. 13/854,319, filed on (Continued)

Primary Examiner — Ajay Arora

(74) *Attorney, Agent, or Firm* — Bill R. Naifeh; Timothy F. Bliss

(51) **Int. Cl.**

H01L 21/02 (2006.01)

H01L 29/10 (2006.01)

H01L 27/11524 (2017.01)

H01L 27/146 (2006.01)

H01L 27/11521 (2017.01)

H01L 29/739 (2006.01)

H01L 29/36 (2006.01)

(Continued)

(57)

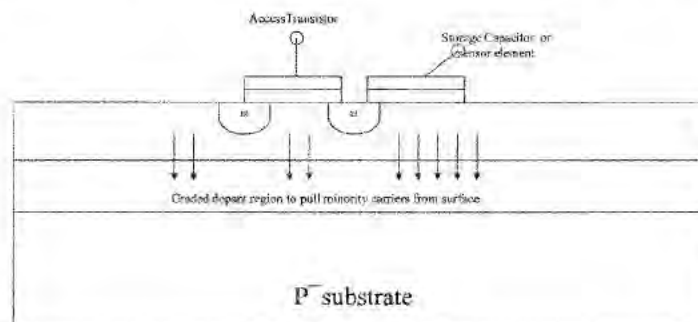
ABSTRACT

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFETs, and a host of other applications.

18 Claims, 10 Drawing Sheets

(52) **U.S. Cl.**

CPC *H01L 29/1095* (2013.01); *H01L 27/11521* (2013.01); *H01L 27/11524* (2013.01); *H01L 27/14643* (2013.01); *H01L 29/36* (2013.01);



Related U.S. Application Data

Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(51) **Int. Cl.**

H01L 27/02 (2006.01)
H01L 27/108 (2006.01)

(56)

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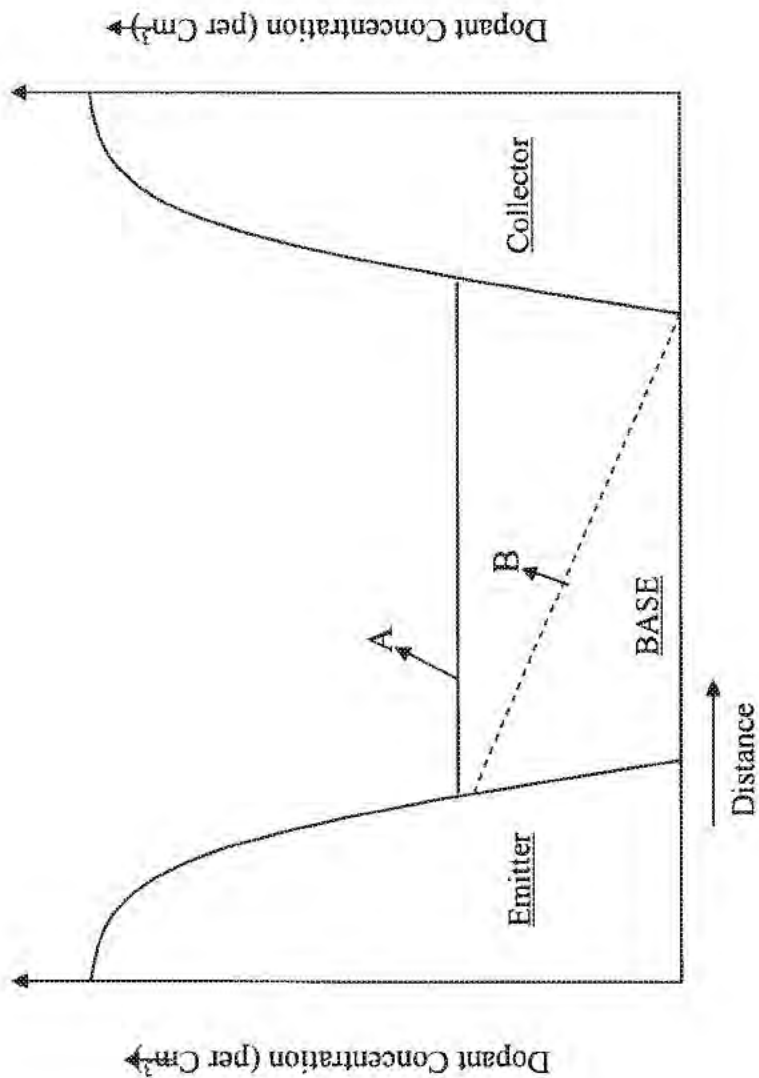


Figure 1 Prior Art

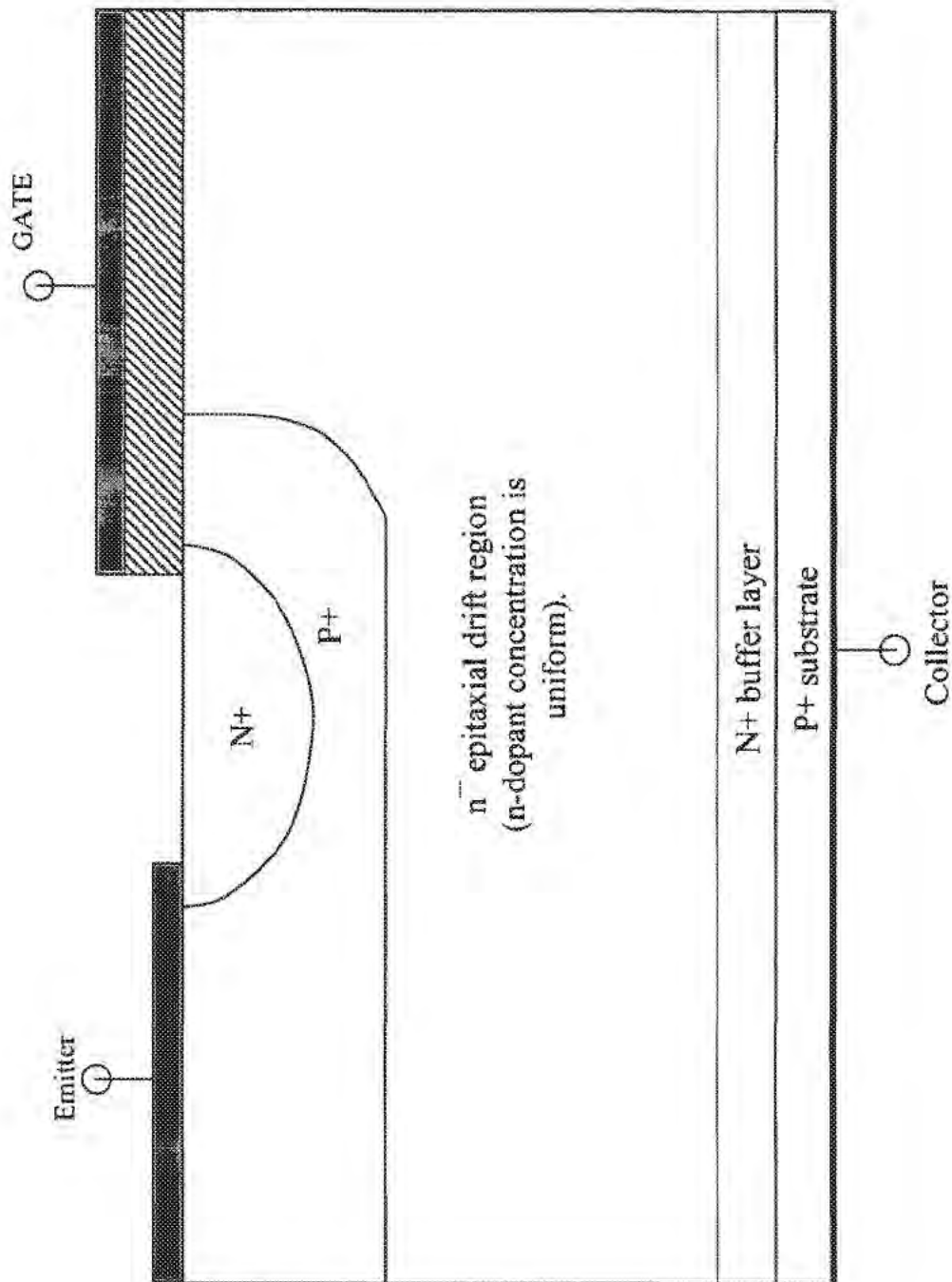


FIGURE 2 Prior art

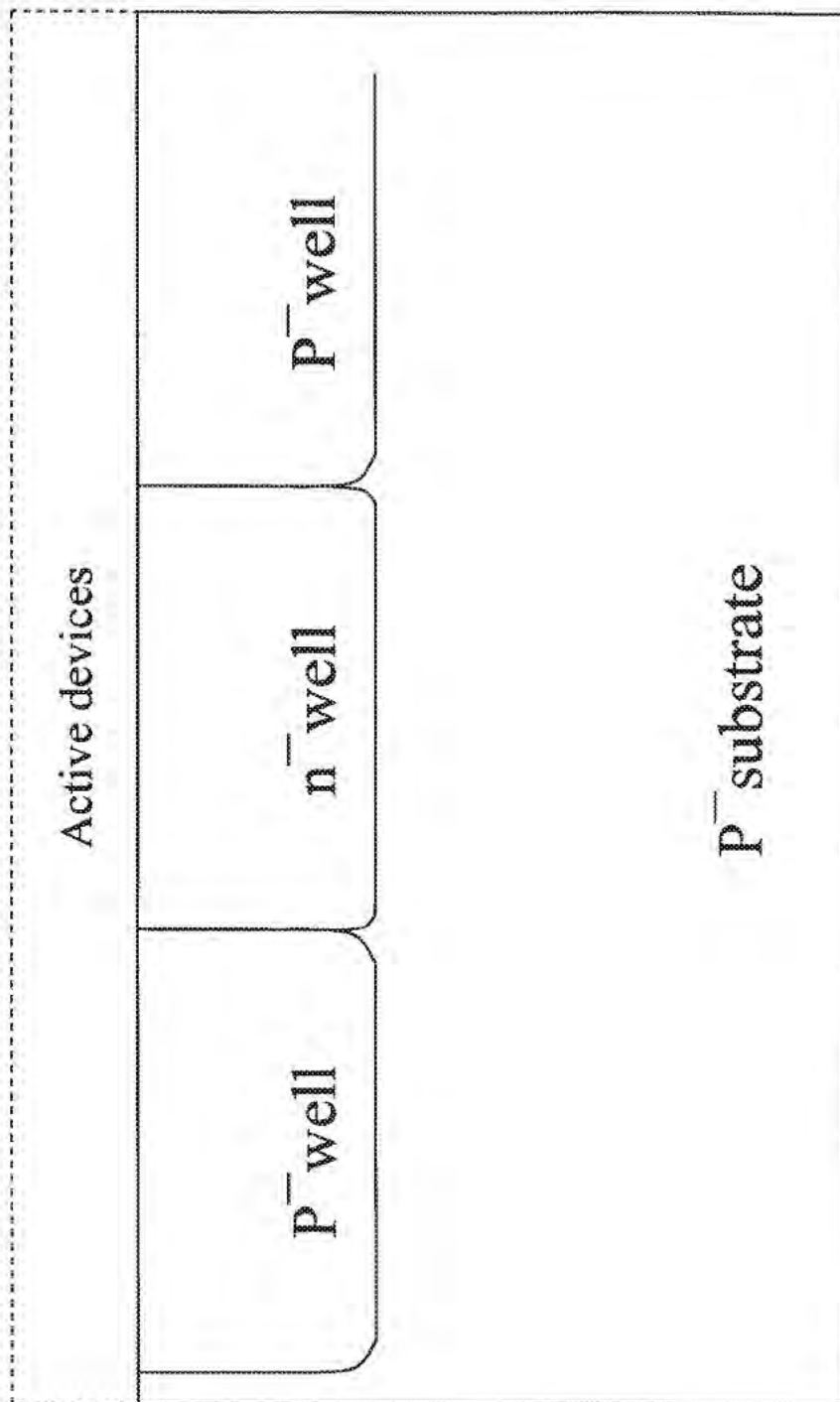


FIGURE 3A Prior art (Twin well CMOS) for a CMOS integrated circuit

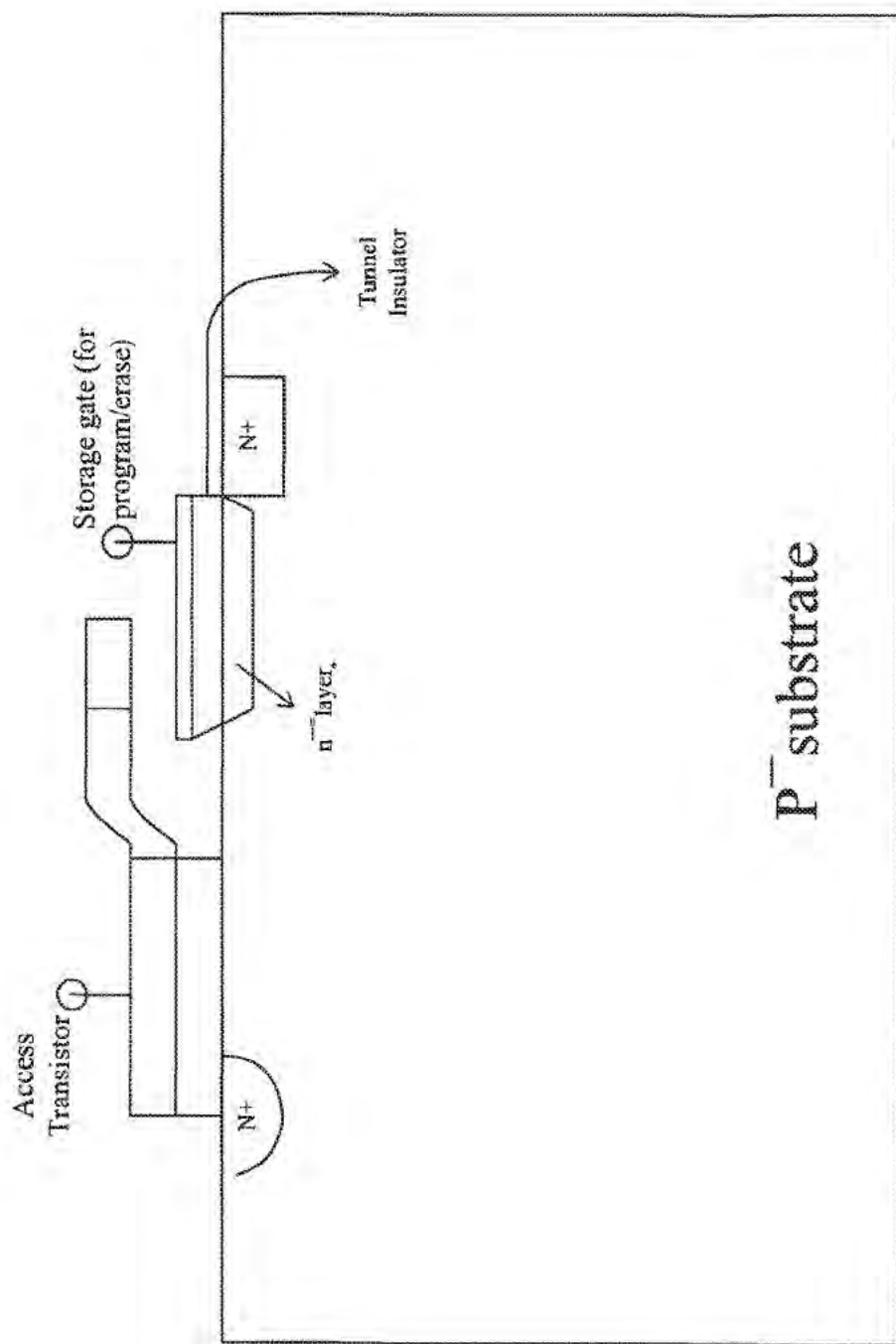


FIGURE 3B Prior art for a two-device EEPROM memory cell

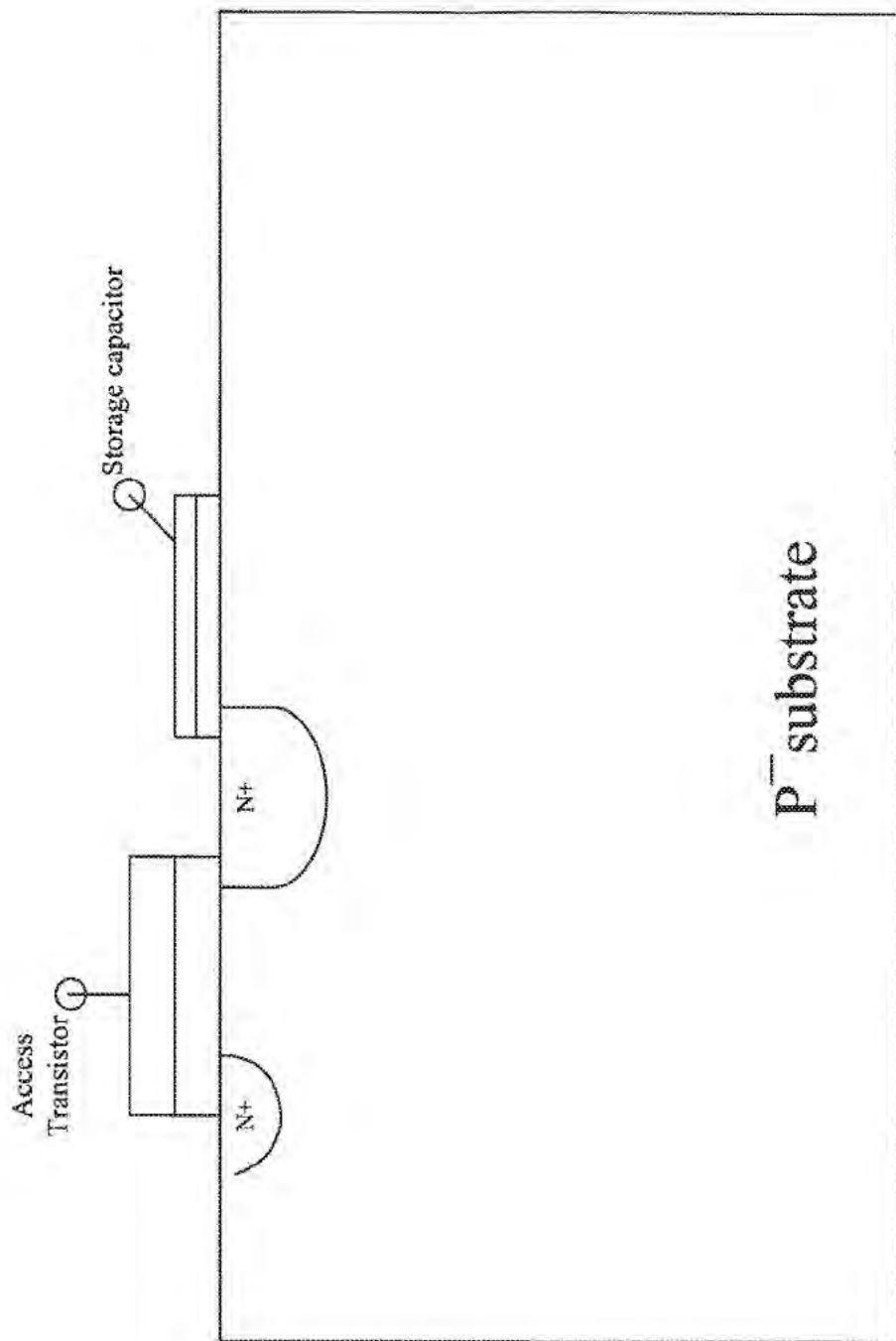


FIGURE 3C Prior art for a 1T-1C DRAM memory cell

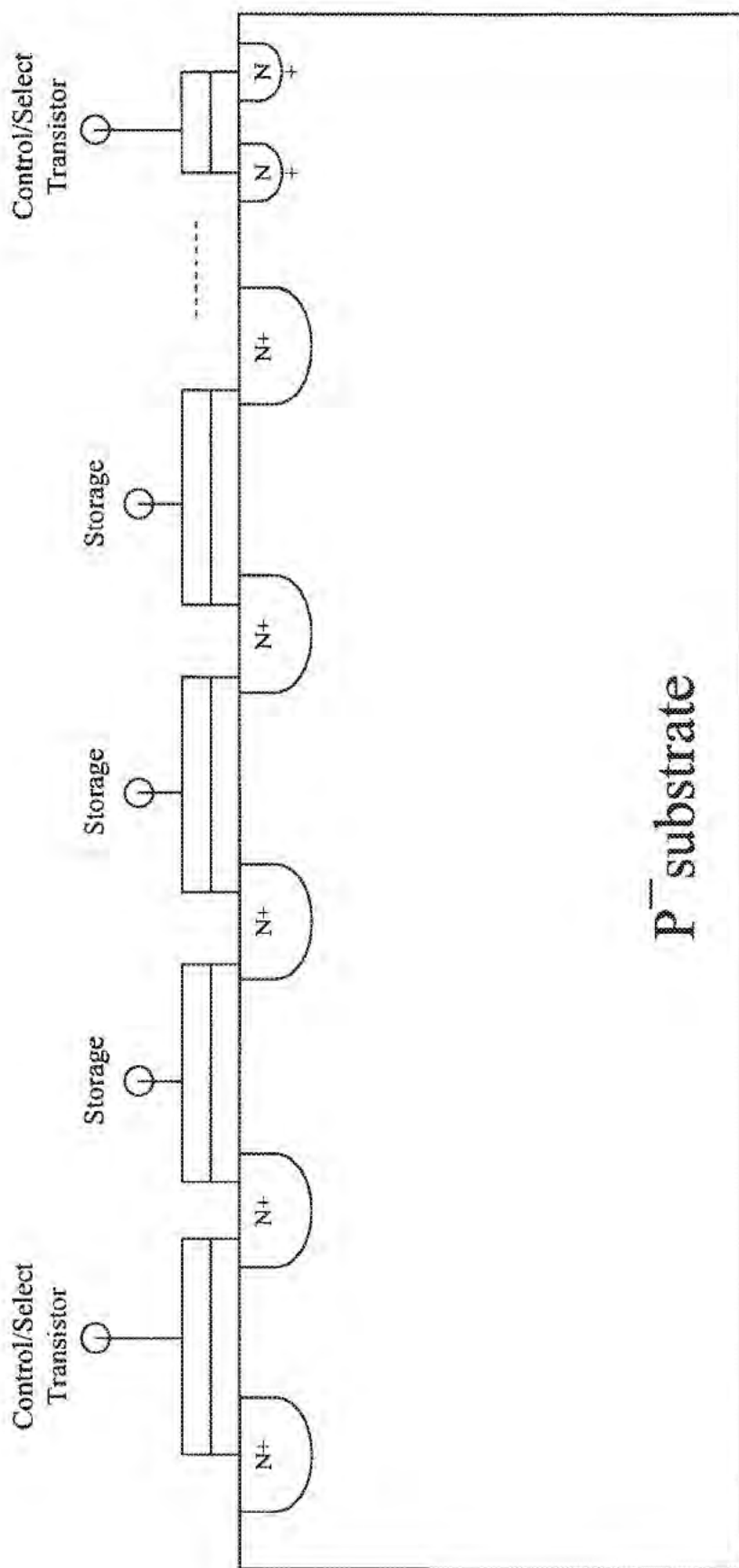


FIGURE 3D Prior art for a NAND flash memory cell

Note: Control/ Select transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

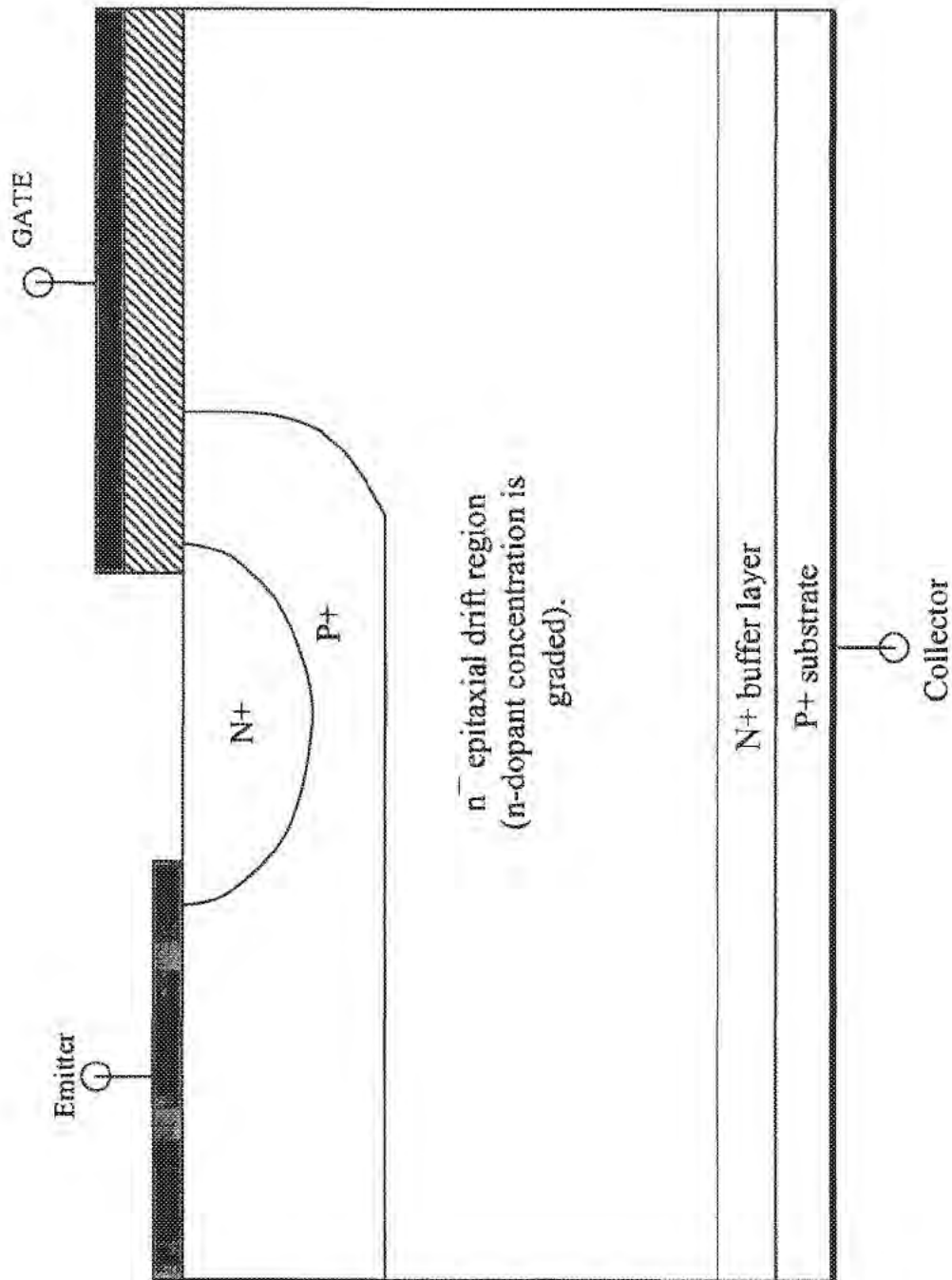


FIGURE 4 A dopant - concentration graded drift region in a IGBT

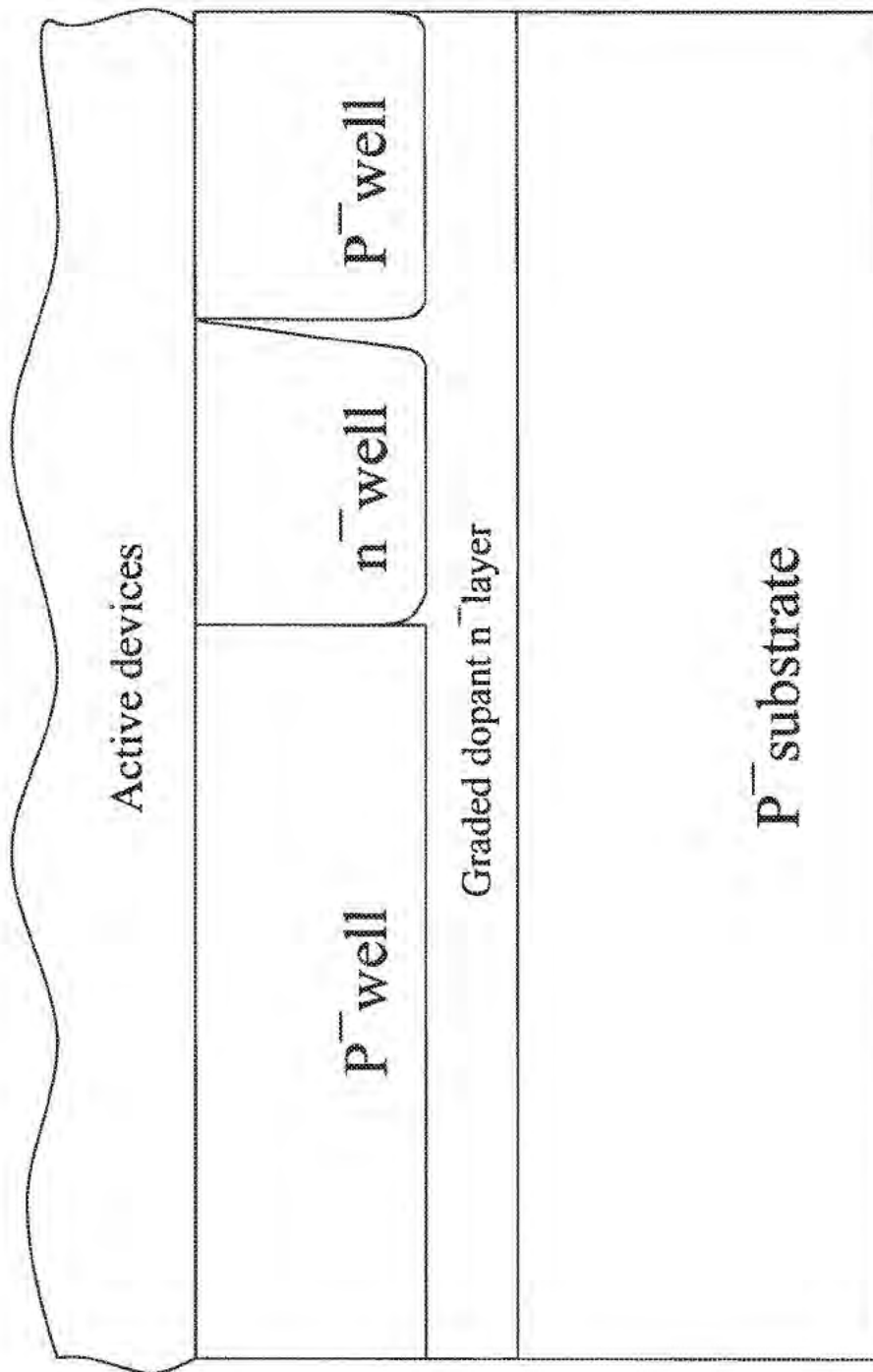


FIGURE 5A A CMOS Substrate for digital, mixed, signal, and sensors IC's

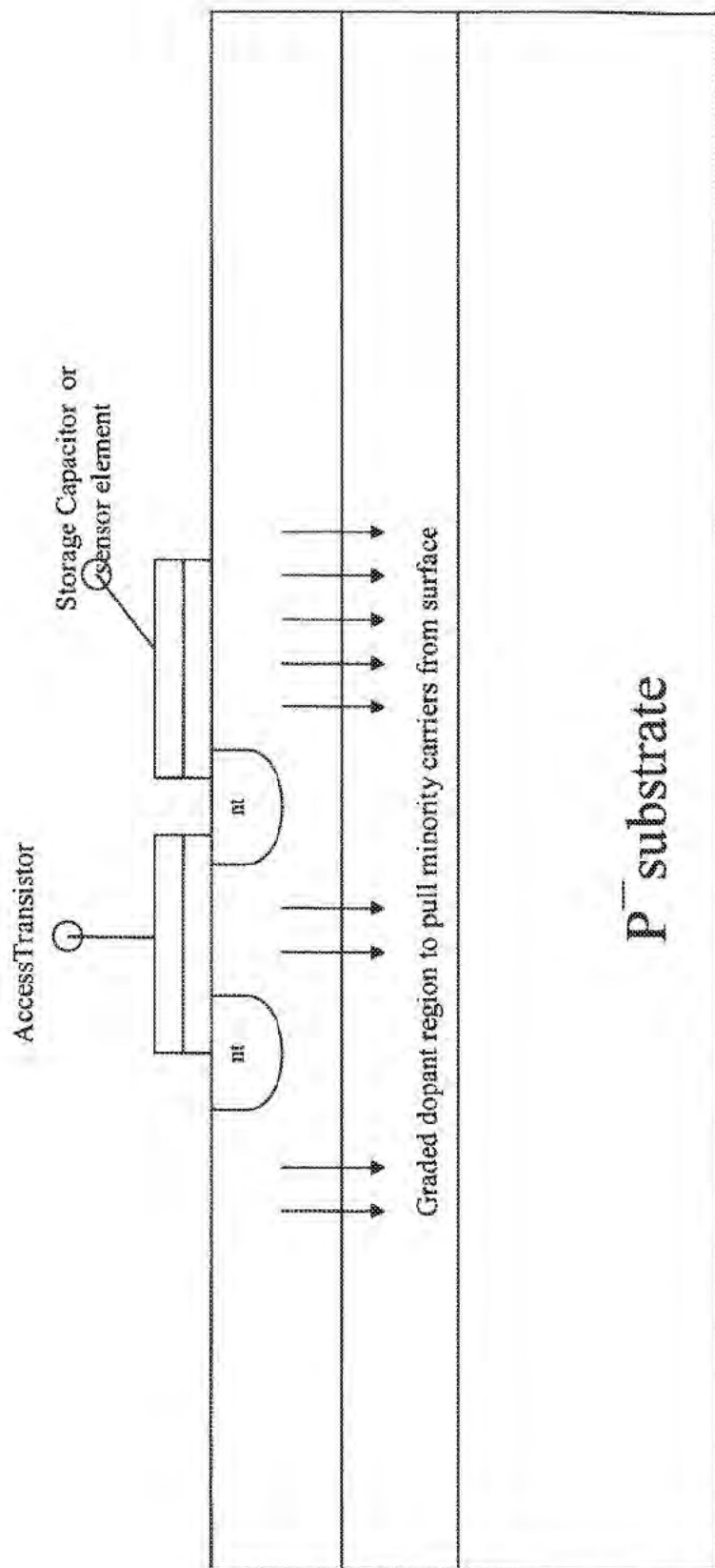


FIGURE 5B CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

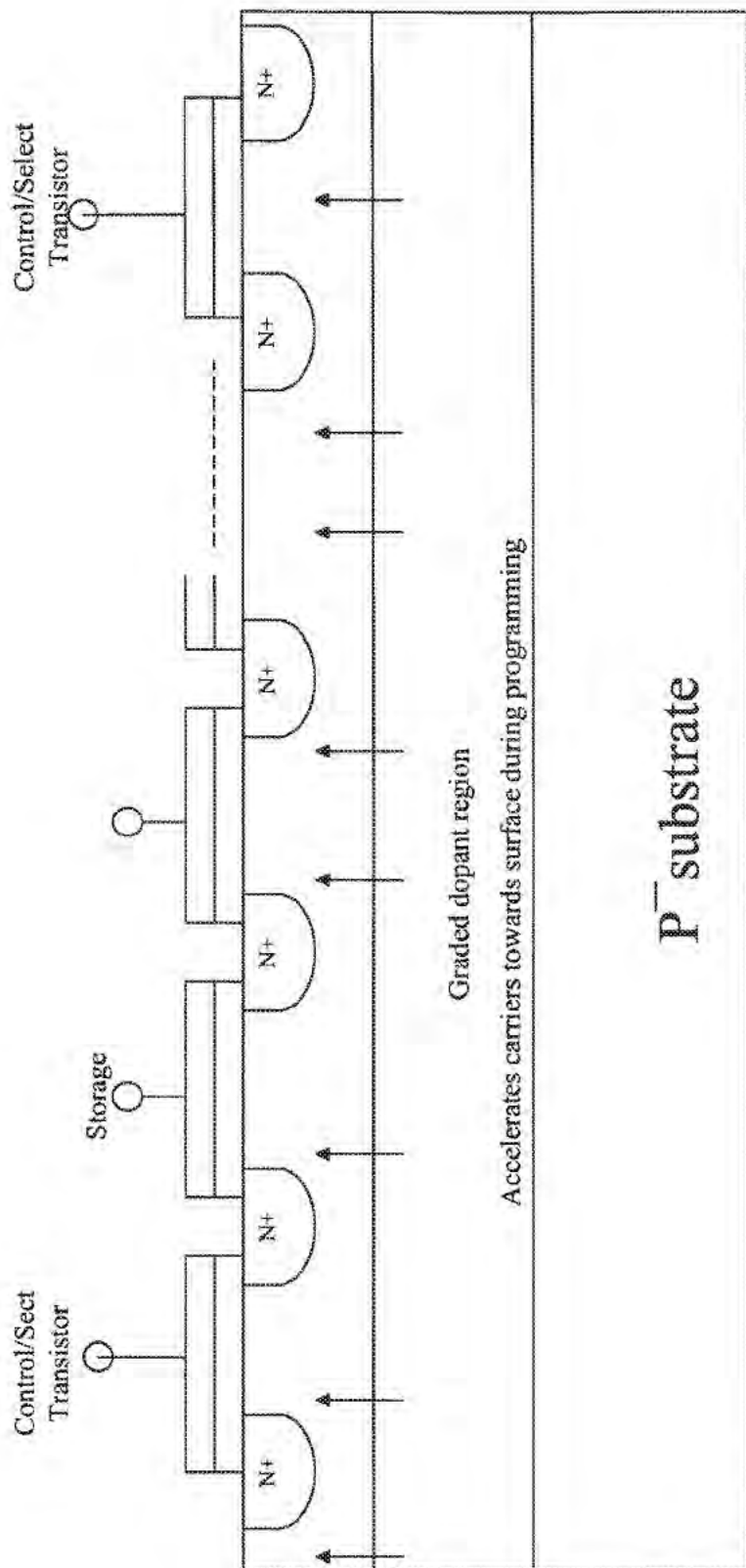


FIGURE 5C CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of U.S. patent application Ser. No. 14/931,636, filed Nov. 3, 2015, published on Jun. 16, 2016 as U.S. Publication No. 2016-0172447, now U.S. Pat. No. 9,647,070, issued on May 9, 2017. Application Ser. No. 14/931,636 is a continuation of U.S. patent application Ser. No. 14/515,584, filed Oct. 16, 2014, published on Feb. 5, 2015, as U.S. Publication No. 2015-0035004, now U.S. Pat. No. 9,190,502, issued on Nov. 17, 2015. Application Ser. No. 14/515,584 is a Continuation of U.S. patent application Ser. No. 13/854,319 filed Apr. 1, 2013, published on Aug. 29, 2013, as U.S. Publication No. 2013-0221488. Application Ser. No. 13/854,319 is a Continuation of Ser. No. 11/622,496, filed Jan. 12, 2007, published on Jul. 12, 2007, as Publication No. 2007-0158790, now U.S. Pat. No. 8,421,195, issued on Apr. 16, 2013. Application Ser. No. 11/622,496, is a Division of U.S. patent application Ser. No. 10/934,915, filed Sep. 3, 2004, published on Mar. 9, 2006, as U.S. Publication No. 2006-0049464. U.S. Pat. Nos. 9,647,070, 9,190,502, and 8,421,195, and Patent Application Publication Nos. 2016-0172447, 2015-0035004, 2013-0221488, 2007-0158790, and 2006-0049464, are incorporated herein by reference in their entirety.

TECHNICAL FIELD

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the

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sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n-well in which p-channel transistors are subsequently fabricated and one p-well in which n-channel transistors are subsequently fabricated); FIG. 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, whereas the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100x at the emitter-base junction, relative to the base-collector junction.

(1×). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or, frequency at unity gain, f_T) can be as large as 2×-5×. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region— n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The “average” base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} , holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n^- epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The “reverse recovery time” for an IGBT is significantly improved due to the optimized graded dopant in the so called “drift region” as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held “actively held high” nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating “subterranean” recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible. In a preferred embodiment, the subterranean n^- layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer

bonding or similar “transfer” mechanisms. This n^- layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^- well and p^- wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the “channel pinch-off” is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A semiconductor device, comprising:

- a substrate of a first doping type at a first doping level having first and second surfaces;
- a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
- a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
- transistors formed in at least one of the first active region or second active region; and
- at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

2. The semiconductor device of claim 1, wherein the substrate is a p-type substrate.

3. The semiconductor device of claim 1, wherein the substrate is an n-type substrate.

4. The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

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5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.

6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.

7. The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

8. The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.

9. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level having first and second surfaces;

a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.

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10. The semiconductor device of claim 9, wherein the substrate is a p-type substrate.

11. The semiconductor device of claim 9, wherein the substrate is an n-type substrate.

12. The semiconductor device of claim 9, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.

14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.

15. The semiconductor device of claim 9, wherein the first active region and second active region are each separated by at least one isolation region.

16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.

17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.

18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a source, a drain, a gate and a channel region.

* * * * *

EXHIBIT 2



US011121222B2

(12) **United States Patent**
Rao

(10) **Patent No.:** **US 11,121,222 B2**
(45) **Date of Patent:** **Sep. 14, 2021**

(54) **SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS**

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(72) Inventor: **G.R. Mohan Rao**, Allen, TX (US)

(73) Assignee: **GREENTHREAD, LLC**, Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(65) **Prior Publication Data**

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Related U.S. Application Data

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(51) **Int. Cl.**
H01L 29/10 (2006.01)
H01L 27/11524 (2017.01)
(Continued)

(52) **U.S. Cl.**
CPC **H01L 29/1095** (2013.01); **H01L 27/11521** (2013.01); **H01L 27/11524** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC **H01L 29/1095**
(Continued)

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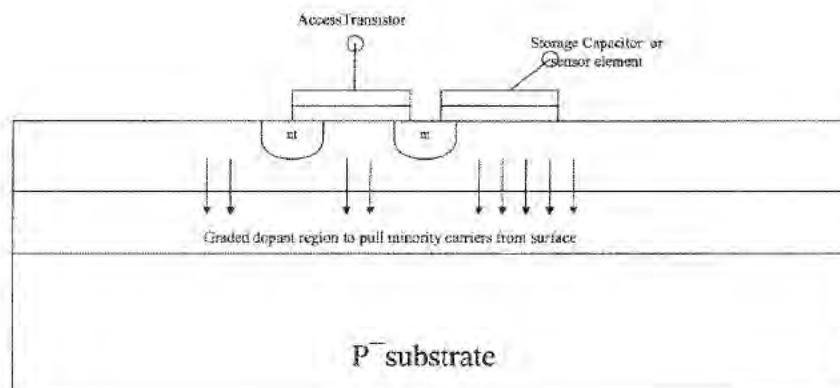
Primary Examiner — Ajay Arora

(74) *Attorney, Agent, or Firm* — Gregory M. Howison

(57) **ABSTRACT**

Most semiconductor devices manufactured today, have uniform dopant concentration, either in the lateral or vertical device active (and isolation) regions. By grading the dopant concentration, the performance in various semiconductor devices can be significantly improved. Performance improvements can be obtained in application specific areas like increase in frequency of operation for digital logic, various power MOSFET and IGBT ICs, improvement in refresh time for DRAMs, decrease in programming time for nonvolatile memory, better visual quality including pixel resolution and color sensitivity for imaging ICs, better sensitivity for varactors in tunable filters, higher drive capabilities for JFETs, and a host of other applications.

44 Claims, 10 Drawing Sheets



Related U.S. Application Data

continuation of application No. 15/590,282, filed on May 9, 2017, now Pat. No. 10,510,842, which is a continuation of application No. 14/931,636, filed on Nov. 3, 2015, now Pat. No. 9,647,070, which is a continuation of application No. 14/515,584, filed on Oct. 16, 2014, now Pat. No. 9,190,502, which is a continuation of application No. 13/854,319, filed on Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now Pat. No. 8,421,195, which is a division of application No. 10/934,915, filed on Sep. 3, 2004, now abandoned.

(51) **Int. Cl.**

H01L 27/146 (2006.01)
H01L 27/1521 (2017.01)
H01L 29/739 (2006.01)
H01L 29/36 (2006.01)
H01L 27/02 (2006.01)
H01L 27/108 (2006.01)

(52) **U.S. Cl.**

CPC **H01L 27/14643** (2013.01); **H01L 29/36** (2013.01); **H01L 29/7395** (2013.01); **H01L 27/0214** (2013.01); **H01L 27/10844** (2013.01)

(58) **Field of Classification Search**

USPC 257/25
 See application file for complete search history.

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 IPR2020-00289—Patent Owner Pre Resp.
 IPR2020-00289—Patent Owner Sur reply.
 IPR2020-00289—Petition.
 IPR2020-00290—Exhibit 1003—Declaration of Dr. Bruce Smith.
 IPR2020-00290—Exhibit 1013—Tango, *Mega bit Memory Technology*.
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 IPR2020-00290—Petition.
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 IPR2020-00291—Exhibit 1003—Declaration of Dr. Bruce Smith.
 IPR2020-00291—Exhibit 1011—The Insulated Gate Bipolar Transistor: IGBT Theory and Design, Vinod Kumar Khanna, IEEE Press and Wiley-Interscience, 2003.
 IPR2020-00291—Exhibit 1020—S. M. Sze, *Physics of Semiconductor Devices*, Wiley-Interscience, 2nd Ed., 1981 (“Sze 81”).
 IPR2020-00291—Exhibit 1021—S. M. Sze, *Semiconductor Devices: Physics and Technology*, John Wiley & Sons, 2nd Ed., 2002 (“Sze ’02”).
 IPR2020-00291—Exhibit 2001—Exhibit 2 to Appendix B of Samsung Electronics Co., Ltd.'s Invalidity Contentions (Invalidity Contention based on U.S Patent Application Publication No. 2002/0195656 (“Hattori”).
 IPR2020-00291—Exhibit 2013—Declaration of Dr. Alexander D. Glew.
 IPR2020-00291—Patent Owner Preliminary Resp.
 IPR2020-00291—Patent Owner Sur Reply.
 IPR2020-00291—Petition.
 IPR2020-00291—Petitioners Reply.
 IPR2020-00292—Exhibit 1003—Declaration of Dr. Bruce Smith.
 IPR2020-00292—Exhibit 2001—Excerpt from Exhibit 1 to Appendix B of Samsung Electronics Co., Ltd.'s Invalidity Contentions (Invalidity Contention based on “Insulated Gate Bipolar Transistor IGBT Theory and Design” by Vinod Kumar Khanna.
 IPR2020-00292—Exhibit 2012—Excerpt from Exhibit A to Joint Claim Construction Chart Pursuant to Patent Rule 4-5, *Greenthread, LLC v. Samsung Electronics Co., Ltd., et al.*, Case No. 2:19-CV-147-JRG, Dkt. 53-1 (Mar. 18, 2020).
 IPR2020-00292—Patent Owner Preliminary Response.

* cited by examiner

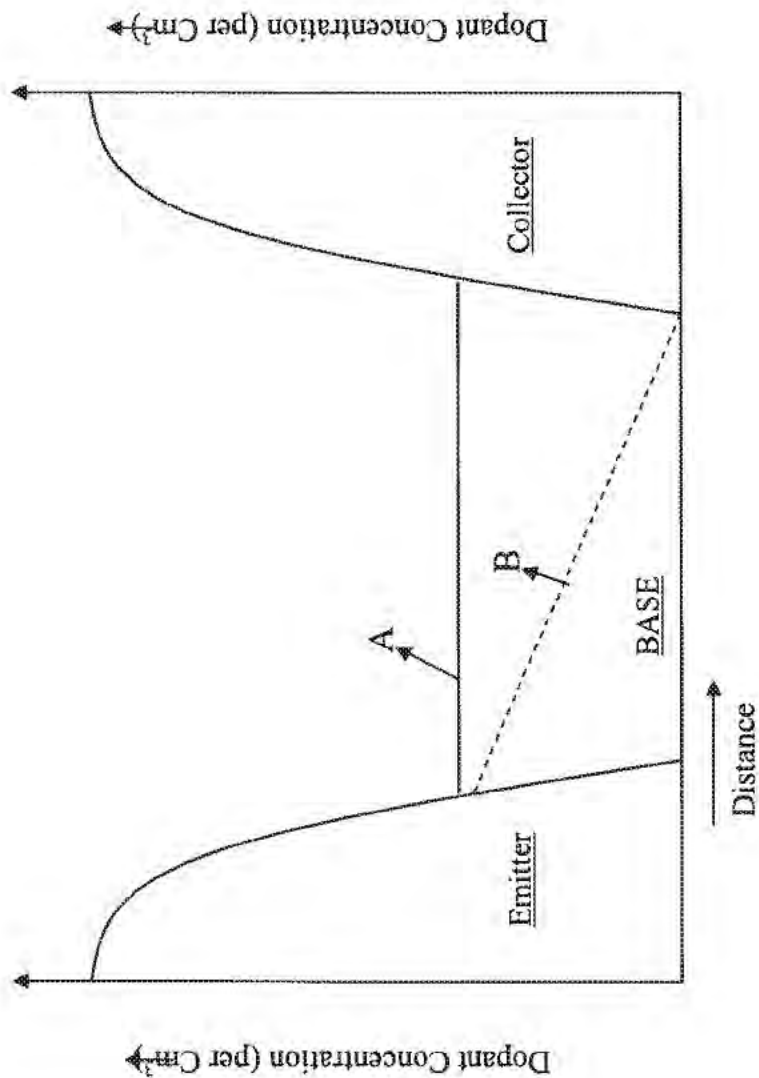


Figure 1 Prior Art

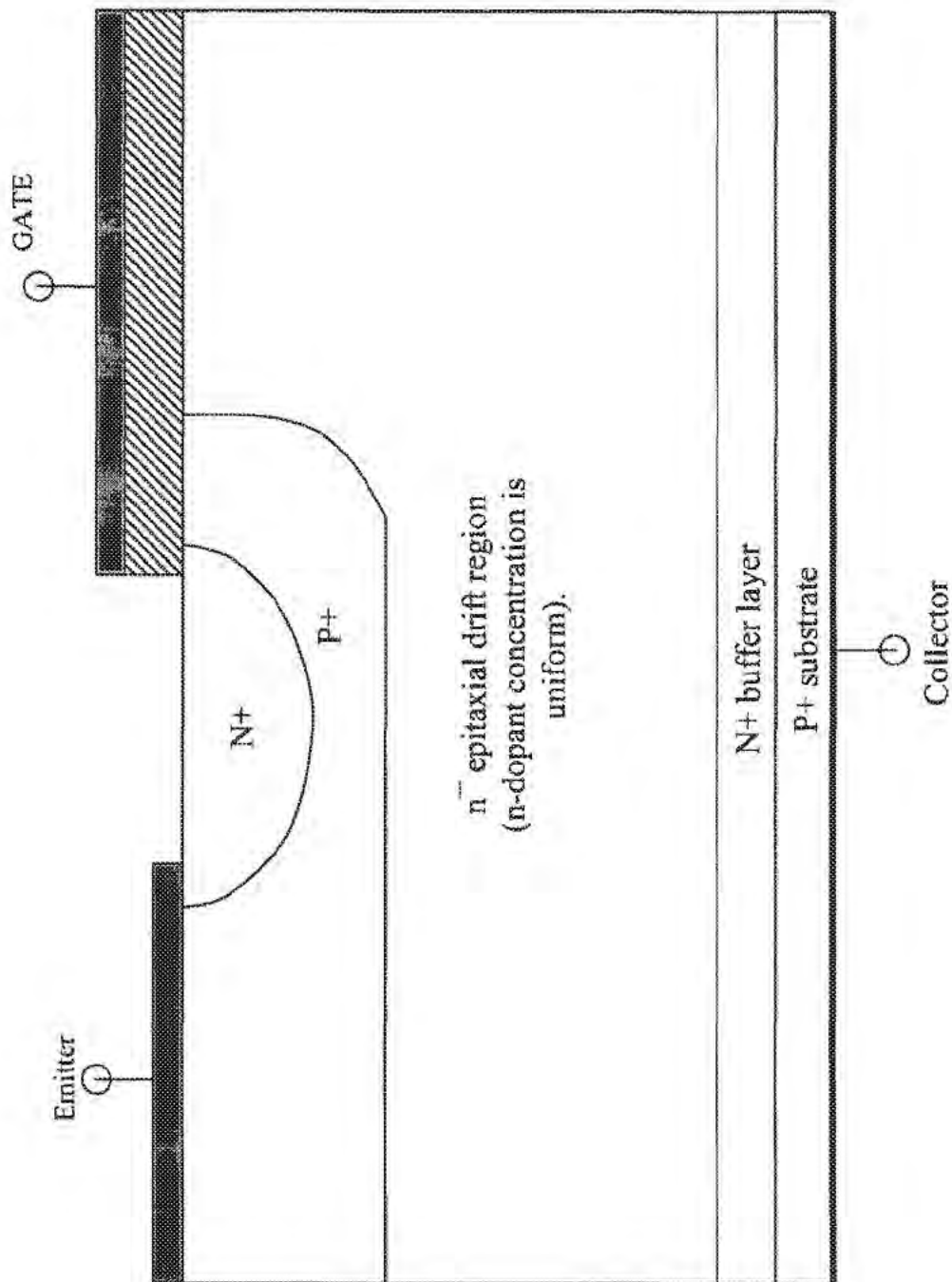


FIGURE 2 Prior art

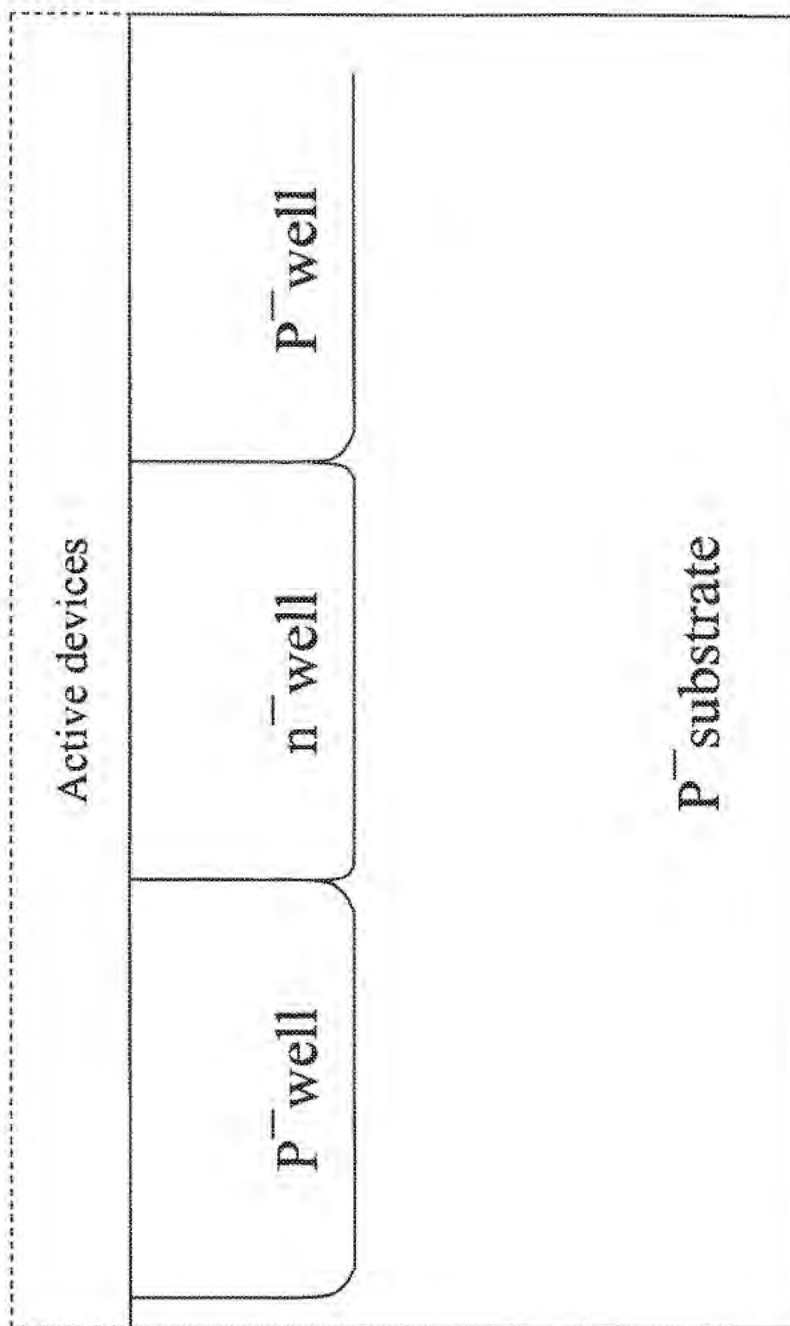


FIGURE 3A Prior art (Twin well CMOS) for a CMOS integrated circuit

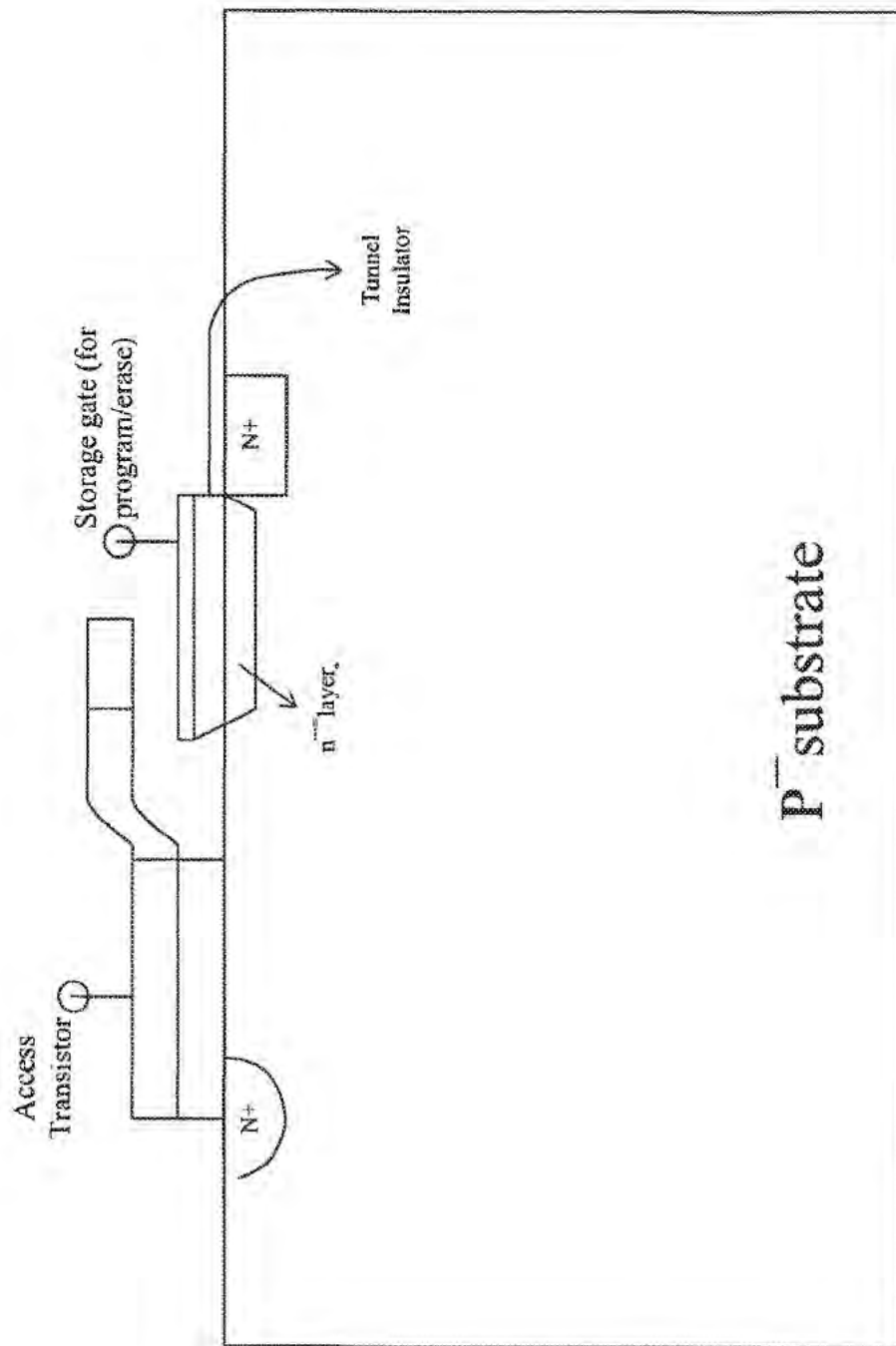


FIGURE 3B Prior art for a two-device EEPROM memory cell

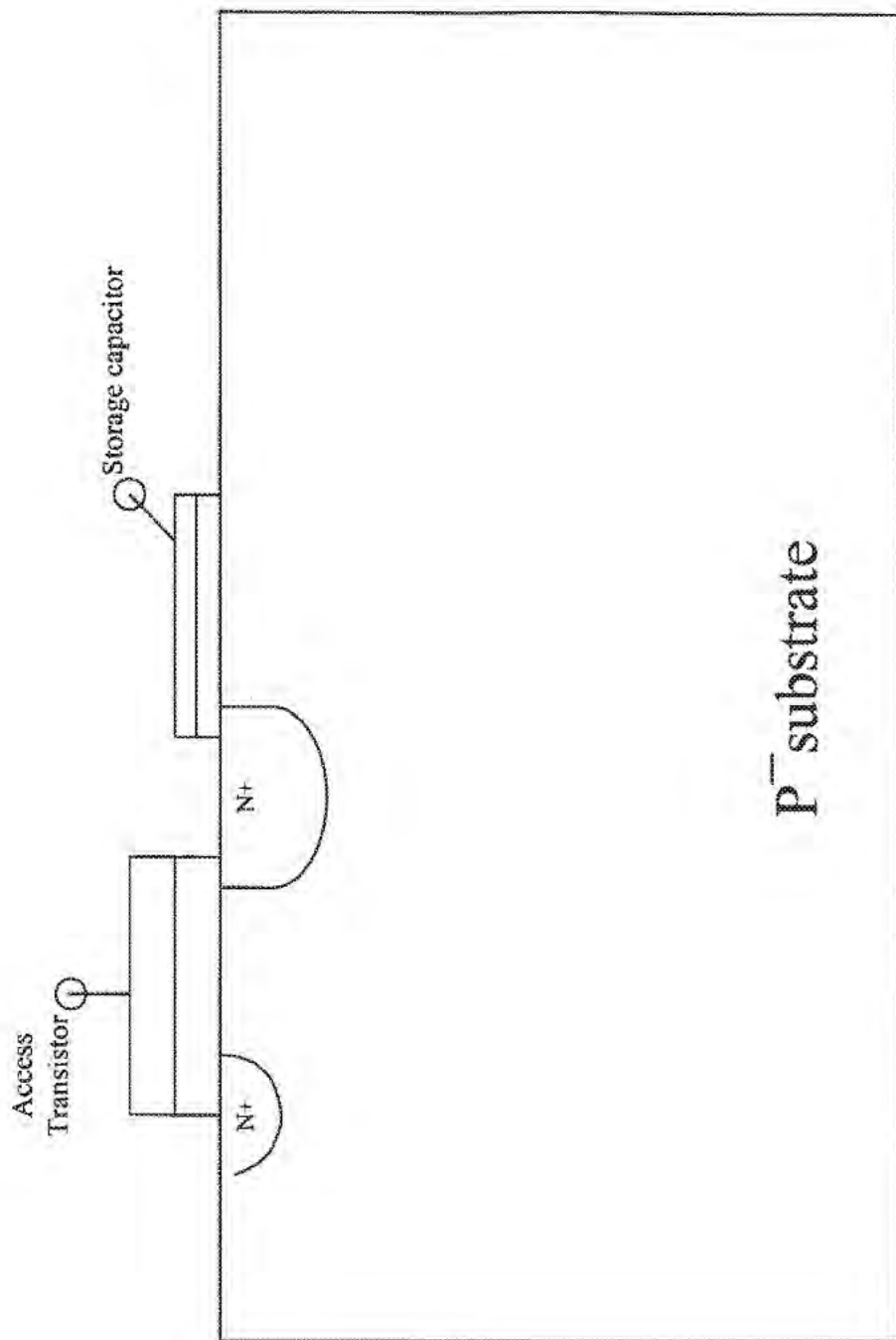


FIGURE 3C Prior art for a 1T-1C DRAM memory cell

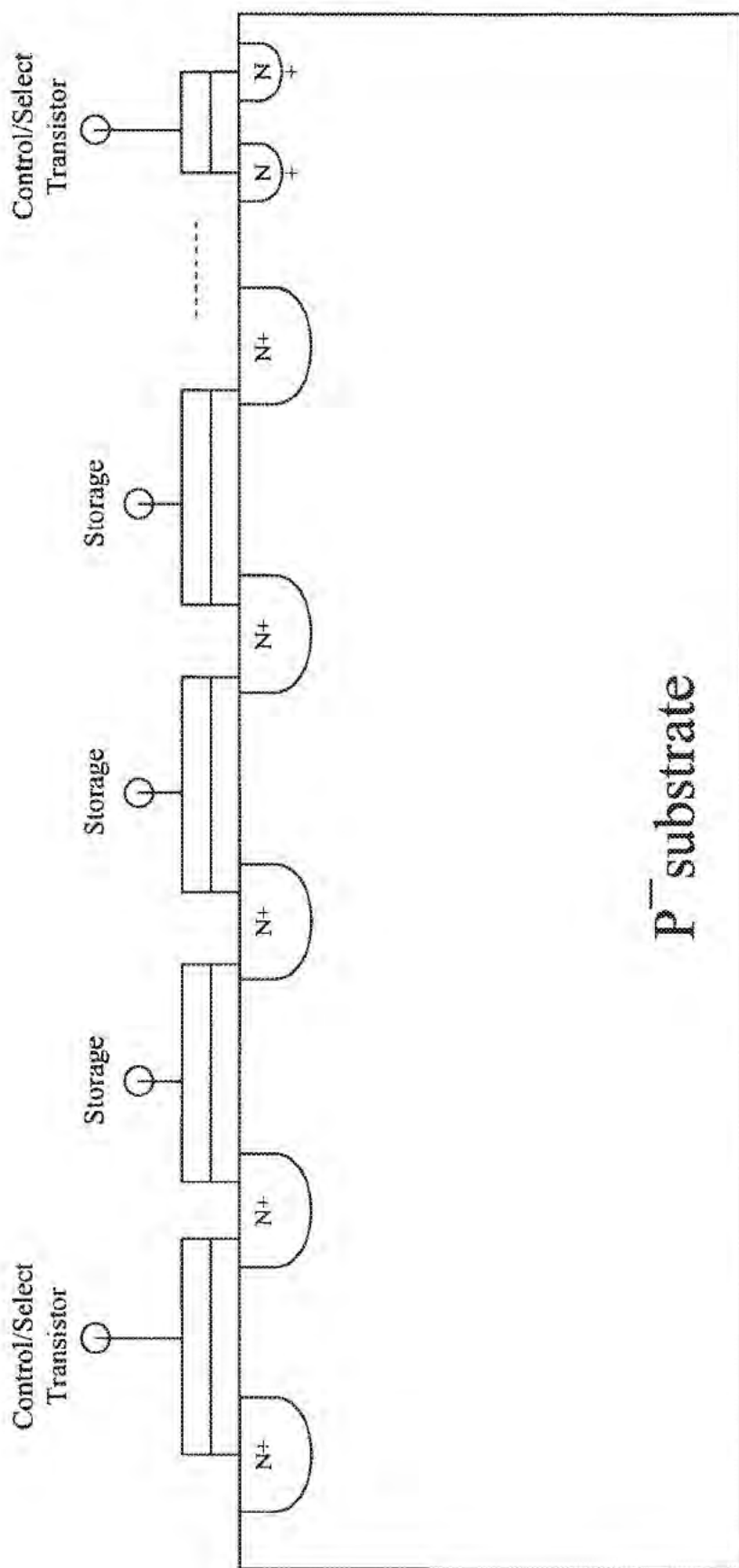


FIGURE 3D Prior art for a NAND flash memory cell

Note: Control/ Select transistors have a single insulator - traditional MOS transistor.

Storage nodes have a stacked gate structure, typically with a floating gate and control gate comprising the stack.

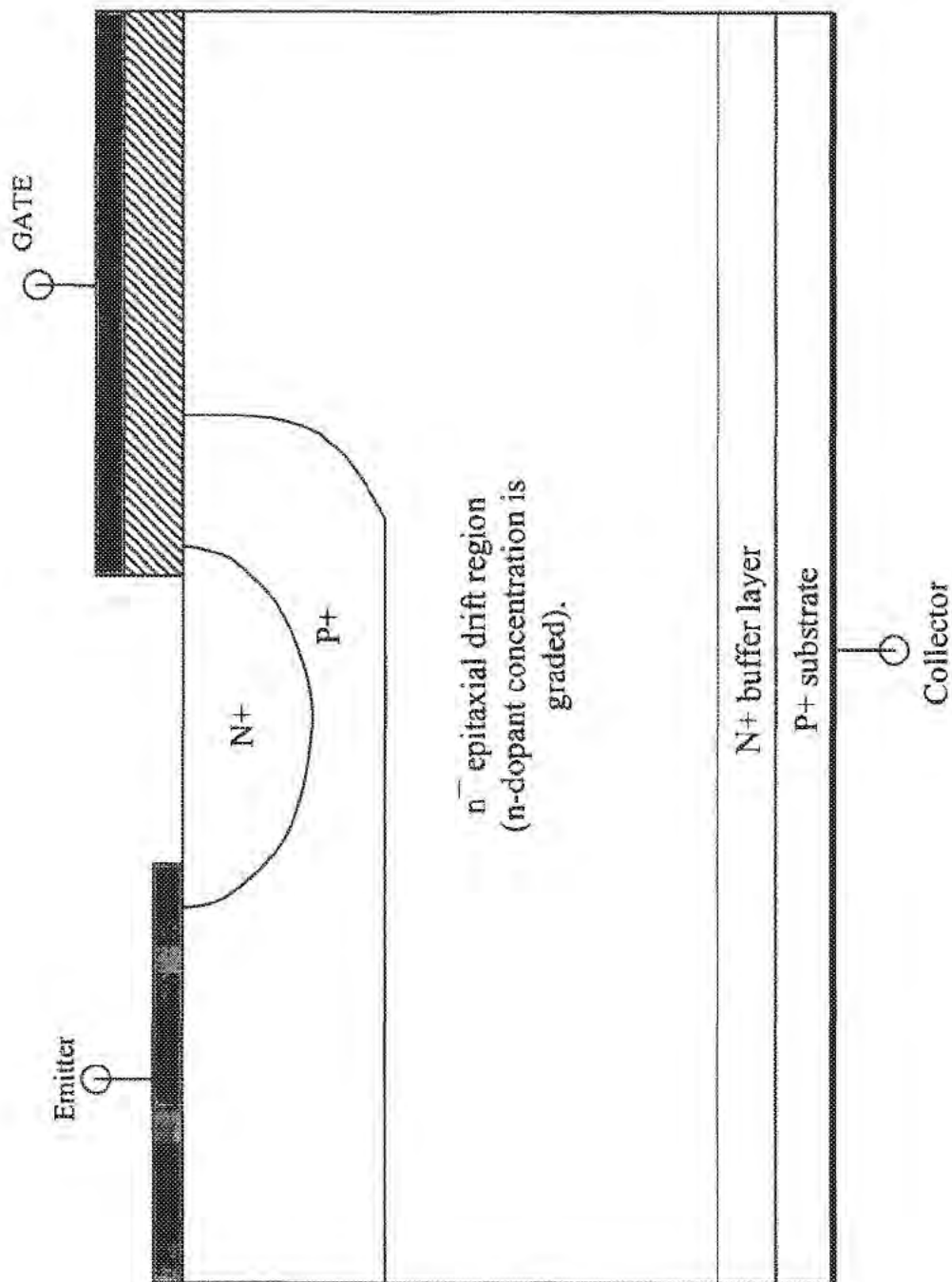


FIGURE 4 A dopant - concentration graded drift region in a IGBT

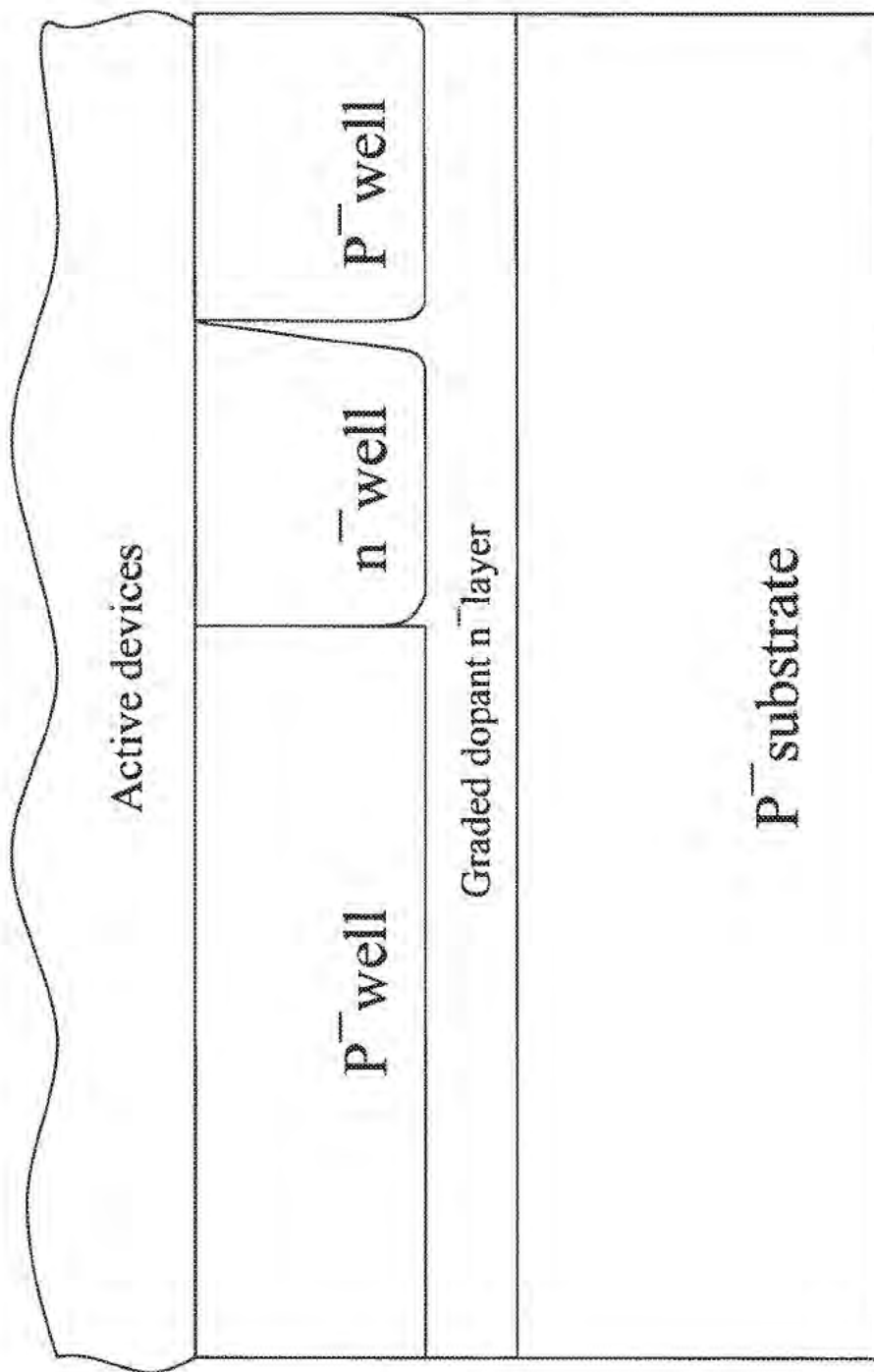


FIGURE 5A A CMOS Substrate for digital, mixed, signal, and sensors IC's

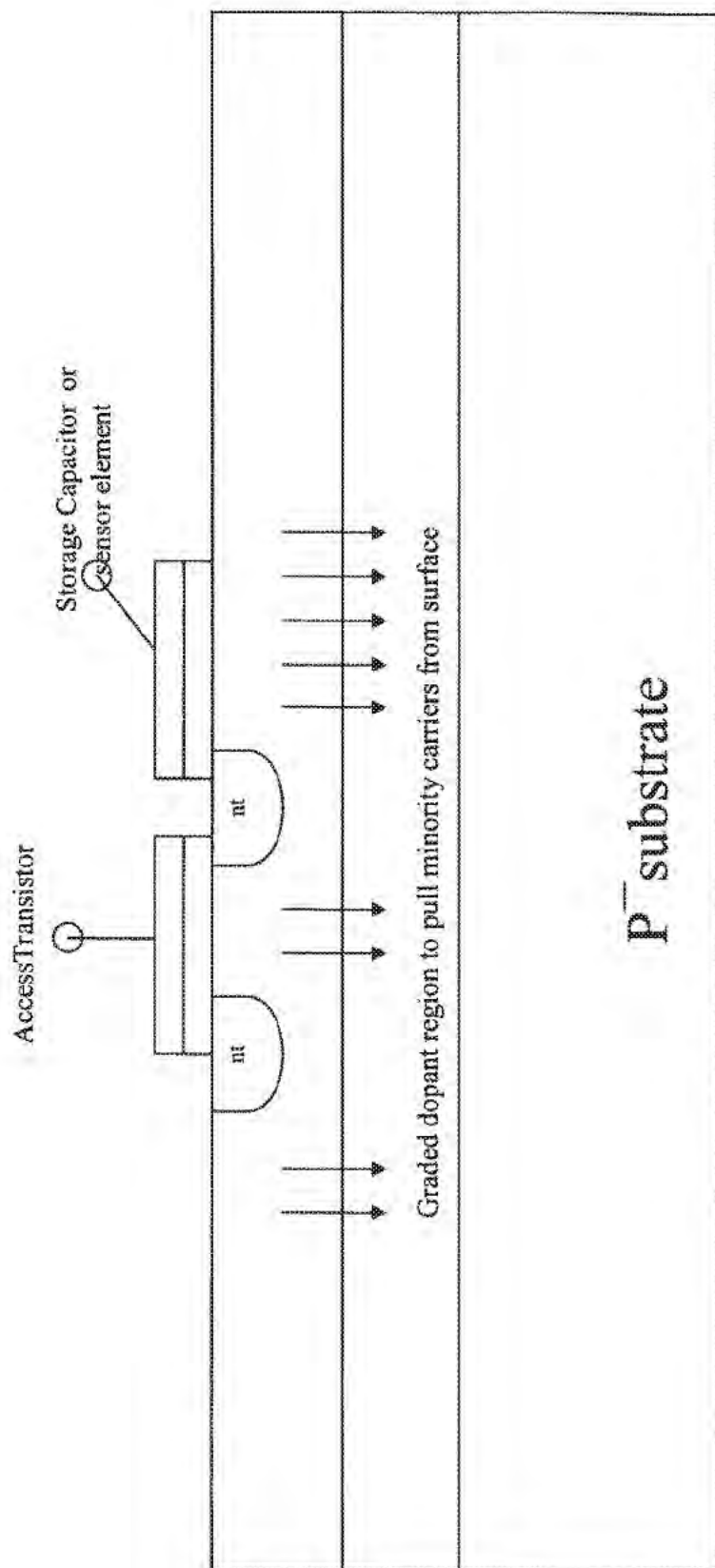


FIGURE 5B CMOS Substrate for a DRAM or image sensor, with one embodiment of the invention

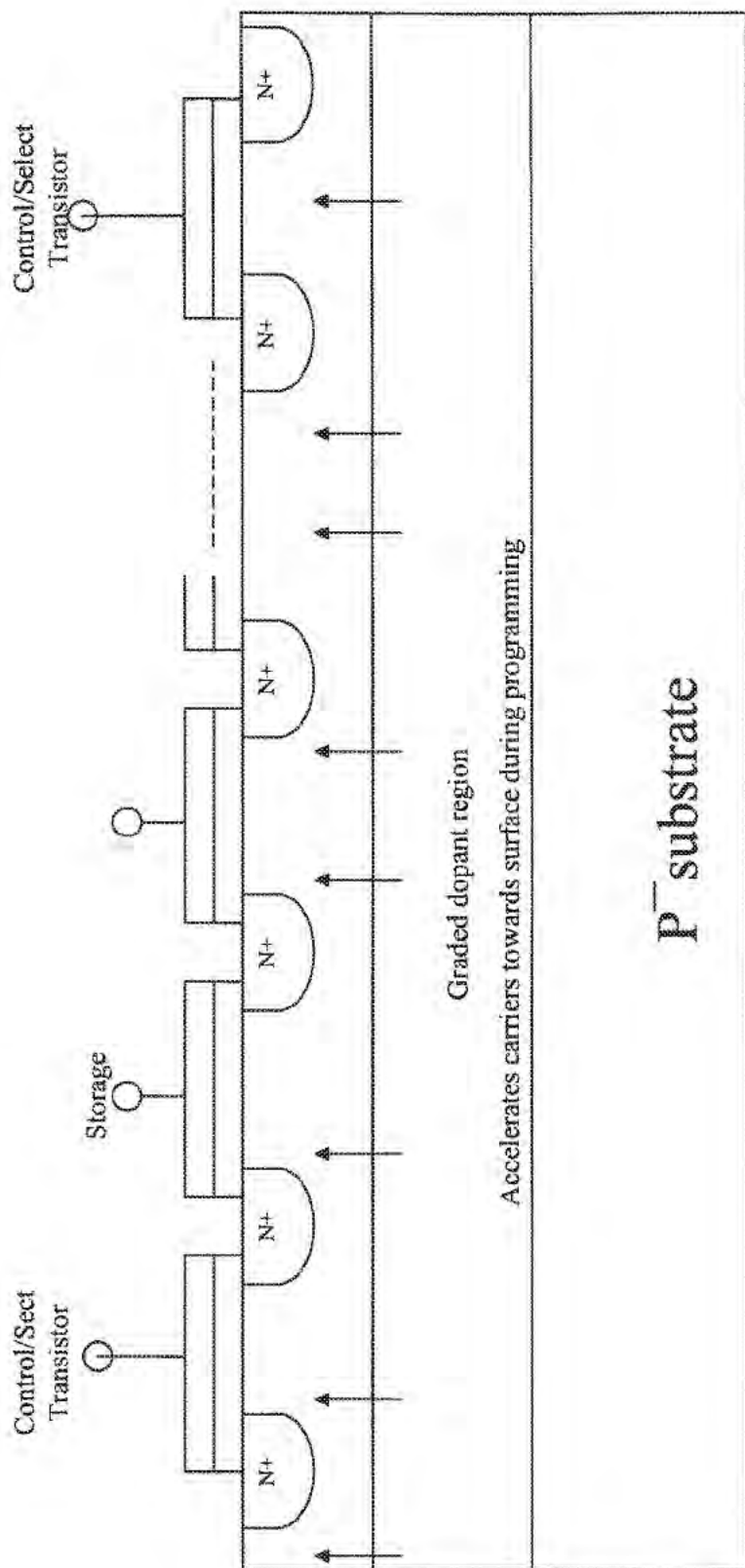


FIGURE 5C CMOS Substrate for a NAND flash device to improve programming times

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SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of U.S. patent application Ser. No. 16/717,950, filed Dec. 17, 2019, which is a Continuation of U.S. patent application Ser. No. 15/590,282, filed May 9, 2017, which is a Continuation of U.S. patent application Ser. No. 14/931,636, filed Nov. 3, 2015, which is a Continuation of U.S. patent application Ser. No. 14/515,584, filed Oct. 16, 2014, which is a Continuation of U.S. patent application Ser. No. 13/854,319 filed Apr. 1, 2013, which is a Continuation of Ser. No. 11/622,496, filed Jan. 12, 2007, which is a Divisional of U.S. patent application Ser. No. 10/934,915, filed Sep. 3, 2004. The disclosures of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

This present invention relates to all semiconductor devices and systems. Particularly it applies to diffused diodes, avalanche diodes, Schottky devices, power MOS transistors, JFET's, RF bipolar transistors, IGBTs (Insulated Gate Bipolar Transistors), varactors, digital VLSI, mixed signal circuits and sensor devices including camera ICs employing CCD (Charge Coupled Device) as well as CMOS technologies.

BACKGROUND

Bipolar Junction Transistors (BJT) are classified as minority carrier devices because minority carriers are the principle device conduction mechanism. However, majority carriers also play a small but finite role in modulating the conductivity in BJTs. Consequently, both carriers (electrons and holes) play a role in the switching performance of BJTs. The maximum frequency of operation in BJTs is limited by the base transit time as well as the quick recombination of the majority carriers when the device is switched off (prior to beginning the next cycle). The dominant carrier mechanism in BJTs is carrier diffusion. The carrier drift current component is fairly small, especially in uniformly doped base BJTs. Efforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector. However, most semiconductor devices, including various power MOSFETs (traditional, DMOS, lateral, vertical and a host of other configurations), IGBT's (Insulated Gated Base Transistors), still use a uniformly doped 'drift epitaxial' region in the base. FIG. 1 shows the relative doping concentration versus distance in a BJT. FIG. 2 shows the uniformly doped epi region in an IGBT. In contrast to BJTs, MOS devices are majority carrier devices for conduction. The conduction is channel dominated. The channel can be a surface in one plane in planar devices. The surface can also be on the sidewalls in a vertical device. Other device architectures to combine planar and vertical conduction are also possible. The maximum frequency of operation is dictated primarily by source-drain separation distance. Most MOS devices use a uniformly doped substrate (or a well region). When a MOSFET is optimally integrated with a BJT in a monolithic fashion, an IGBT results. The IGBT inherits the advantages of both MOSFET and BJT. It also brings new challenges because the required characteristics (electron transit and

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hole recombination as fast as possible in n-channel IGBT) necessitate different dopant gradients either in the same layer at different positions, or at the interfaces of similar or dissimilar layers.

Retrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits. FIG. 3A shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated. FIGS. 3B, 3C, and 3D illustrate device cross sections, as practiced today. Retrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs. Most of these techniques either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B");

FIG. 2 illustrates the cross section of a commercial IGBT with a uniform epitaxial drift region (base);

FIGS. 3A, 3B, 3C, and 3D illustrate cross sections of commonly used prior art CMOS silicon substrates; FIG. 3A showing a typical prior art IC with two wells (one n⁺ well in which p-channel transistors are subsequently fabricated and one p⁺ well in which n-channel transistors are subsequently fabricated); FIG. 3B showing a prior art EEPROM (Electrically Erasable Programmable Read-Only Memory) memory cell having a tunnel insulator; FIG. 3C showing a prior art DRAM memory cell; and FIG. 3D showing a prior art NAND flash memory cell;

FIG. 4 illustrates the cross section of an IGBT, using one embodiment of the invention described here, where the dopant is optimally graded in the epitaxial drift region; and

FIGS. 5A, 5B, and 5C illustrate the cross sections of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application—VLSI logic, DRAM/image IC, nonvolatile memory IC.

DETAILED DESCRIPTION

The relative doping concentrations of emitter and collector regions varies from 10^{18} to $10^{20}/\text{cm}^3$, whereas the base region is 10^{14} to $10^{16}/\text{cm}^3$ depending on the desired characteristics of the BJT. In graded base p-n-p transistors, the donor dopant concentration may be 10 to 100x at the emitter-base junction, relative to the base-collector junction (1x). The gradient can be linear, quasi linear, exponential or complimentary error function. The relative slope of the donor concentration throughout the base creates a suitable aiding drift electric field, to help the holes (p-n-p transistor) transverse from emitter to collector. Since the aiding drift electric field helps hole conduction, the current gain at a given frequency is enhanced, relative to a uniformly-doped (base) BJT. The improvement in cut-off frequency (or

frequency at unity gain, f_T) can be as large as $2\times-5\times$. Similar performance improvements are also applicable to n-p-n transistors.

As illustrated in FIG. 4, in one embodiment according to the invention, a donor gradient is established from the emitter-drift epitaxial base region junction of the punch-through IGBT, to the drift epitaxial base region— n^+ buffer layer boundary (electrons in this case are accelerated in their transit from emitter to collector). The “average” base resistance is optimized so that conductivity modulation and lifetime (for minority carriers) in the base region are not compromised. By sweeping the carriers towards the n^+ buffer region a number of advantages are obtained. First, the frequency of operation (combination of t_{on} and t_{off} as is known in the IGBT commercial nomenclature) can be enhanced. Second, and maybe more importantly, during t_{off} , holes can be recombined much quicker at the n^+ buffer layer, compared to the uniformly doped n^- epitaxial drift region by establishing a different dopant gradient near the n^+ buffer layer. It should be noted that the drift region can also be a non-epitaxial silicon substrate. Although epitaxy enhances lifetime, it is not mandatory. Different layers of dopant regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication. The “reverse recovery time” for an IGBT is significantly improved due to the optimized graded dopant in the so called “drift region” as well as at the interfaces of the drift region. Graded dopants can also be implemented in the n^+ buffer layer as well as other regions adjacent to the respective layers. Two important performance enhancements are the result of dopant gradients. For example, in an n-channel IGBT, electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n^+ buffer layer. This can improve t_{on} and t_{off} in the same device.

As illustrated in FIGS. 5A, 5B, and 5C, donor gradient is also of benefit to very large scale integrated circuits (VLSI)—VLSI logic, DRAM, nonvolatile memory like NAND flash. Spurious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs. These unwanted carriers can discharge dynamically-held “actively held high” nodes. In most cases, statically-held nodes (with V_{cc}) cannot be affected. Degradation of refresh time in DRAMs is one of the results, because the capacitor holds charge dynamically. Similarly, degradation of CMOS digital images in digital imaging ICs is another result of the havoc caused by minority carriers. Pixel and color resolution can be significantly enhanced in imaging ICs with the embodiments described herein. Creating “subterranean” recombination centers underneath the wells (gold doping, platinum doping) as is done in some high-voltage diodes is not practical for VLSI circuits. Hence, a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible. In a preferred embodiment, the subterranean n^- layer has a graded donor concentration to sweep the minority carriers deep into the substrate. One or more of such layers can also be implemented through wafer to wafer bonding or similar “transfer” mechanisms. This n^- layer can be a deeply-implanted layer. It can also be an epitaxial layer. As desired, the n^- well and p^- wells can also be graded or retrograded in dopants to sweep those carriers away from the surface as well. The graded dopant can also be implemented in surface channel MOS devices to accelerate majority carriers towards the drain. To decrease programming time in nonvolatile memory devices, carriers should be accelerated

towards the surface when programming of memory cells is executed. The graded dopant can also be used to fabricate superior Junction Field-Effect transistors where the “channel pinch-off” is controlled by a graded channel instead of a uniformly doped channel (as practiced in the prior art).

One of ordinary skill and familiarity in the art will recognize that the concepts taught herein can be customized and tailored to a particular application in many advantageous ways. For instance, minority carriers can be channeled to the surface to aid programming in nonvolatile memory devices (NOR, NAND, multivalued-cell). Moreover, single-well, and triple-well CMOS fabrication techniques can also be optimized to incorporate these embodiments individually and collectively. Any modifications of such embodiments (described here) fall within the spirit and scope of the invention. Hence, they fall within the scope of the claims described below.

Although the invention has been described with reference to specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

What is claimed is:

1. A VLSI semiconductor device, comprising:

- a substrate of a first doping type at a first doping level having a surface;
- a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
- a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
- transistors formed in at least one of the first active region or second active region;
- at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and
- at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

2. The VLSI semiconductor device of claim 1, wherein the substrate is a p-type substrate.

3. The VLSI semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

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4. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain digital logic formed by one of either p-channel and n-channel devices.

5. The VLSI semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

6. The VLSI semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

7. The VLSI semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.

8. The VLSI semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.

9. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

10. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

11. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

12. The VLSI semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

13. The VLSI semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS digital logic transistors requiring at least a source, a drain, a gate and a channel.

14. The VLSI semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).

15. The VLSI semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.

16. The VLSI semiconductor device of claim 1, wherein the device is a flash memory.

17. The VLSI semiconductor device of claim 1, wherein the device comprises digital logic and capacitors.

18. The VLSI semiconductor device of claim 1, wherein the device is central processing unit.

19. The VLSI semiconductor device of claim 1, wherein the device is an image sensor.

20. The VLSI semiconductor device of claim 1, wherein each of the first and second active regions are in the lateral or vertical direction.

21. A VLSI semiconductor device, comprising:

a substrate of a first doping type at a first doping level having a surface;

a first active region disposed adjacent the surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof; transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to an area of the substrate where there are no active regions; and

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at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface to the area of the substrate where there are no active regions, and wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.

22. The VLSI semiconductor device of claim 21, wherein the substrate is an n-type substrate.

23. The VLSI semiconductor device of claim 21, wherein the substrate is a p-type substrate.

24. The VLSI semiconductor device of claim 21, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

25. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.

26. The VLSI semiconductor device of claim 21, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.

27. The VLSI semiconductor device of claim 21, wherein the first active region and second active region are each separated by at least one isolation region.

28. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.

29. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the first active region are both p-type and n-type.

30. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant concentration in the second active region are both p-type and n-type.

31. The VLSI semiconductor device of claim 21, wherein dopants of the graded dopant region in the well region are both p-type and n-type.

32. The VLSI semiconductor device of claim 21, wherein the graded dopant is fabricated with an ion implantation process.

33. The VLSI semiconductor device of claim 21, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.

34. The VLSI semiconductor device of claim 21, wherein the device is a flash memory.

35. The VLSI semiconductor device of claim 21, wherein the device is a logic device with capacitors in at least some of the first or second active regions.

36. The VLSI semiconductor device of claim 21, wherein the device is central processing unit.

37. The VLSI semiconductor device of claim 21, wherein the device is an image sensor.

38. The VLSI semiconductor device of claim 21, wherein each of the first and second active regions are in the lateral or vertical direction.

39. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;

a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

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at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

40. The semiconductor device of claim 39 further comprising at least one well region adjacent to the first or second active region and containing at least one graded dopant region, the graded dopant region to aid carrier movement from any region in the well to the substrate area where there is no well.

41. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;
a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

42. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;
a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded donor dopant

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concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

43. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level;
a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region; and

at least a portion of at least one of the first and second active regions having at least one graded acceptor dopant concentration and one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.

44. A CMOS Semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of the surface layer;

a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and

at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

* * * * *

EXHIBIT 3

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT3351825

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
	Name	Execution Date
	G.R. MOHAN RAO	04/27/2015
RECEIVING PARTY DATA		
Name:	GREENTHREAD, LLC	
Street Address:	4544 HARRYS LANE	
City:	DALLAS	
State/Country:	TEXAS	
Postal Code:	75229-5400	
PROPERTY NUMBERS Total: 9		
Property Type	Number	
Application Number:	10934915	
Patent Number:	8421195	
Patent Number:	8106481	
Application Number:	13854319	
Application Number:	14515584	
Application Number:	60982175	
Application Number:	14335160	
Application Number:	61509257	
Application Number:	14525411	
CORRESPONDENCE DATA		
Fax Number:	(972)479-0464	
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>		
Phone:	9724790462	
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ATTORNEY DOCKET NUMBER:	GRTD-32569	
NAME OF SUBMITTER:	GREGORY M. HOWISON	

Greenthread Ex. 2020, p. 50
 Separable from v. Greenthread

PATENT

SIGNATURE:	/Gregory M. Howison, Reg. #30646/
DATE SIGNED:	05/13/2015
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ASSIGNMENT

WHEREAS, G.R. MOHAN RAO, an individual, residing at 1611 Willingham Drive, Allen, Texas 75013 ("Assignor"), has invented certain new and useful inventions set forth on the attached Exhibit A (collectively, the "Inventions"), for which certain applications for United States and foreign patents were filed as set forth on Exhibit A (collectively, the "Applications"), and from which certain United States patents have issued as set forth on Exhibit A (collectively, the "Patents"); and

WHEREAS, GREENTHREAD, LLC, a Texas Limited Liability Company, having a business address at 4544 Harry's Lane, Dallas, Texas 75229-5400 ("Assignee"), is desirous of acquiring the entire right, title, and interest in and to the Applications and Patents and any and all foreign counterparts, divisions, continuations, continuation-in-parts, improvements, reexaminations, reissues, extensions, renewals, substitutes, provisional applications, certificates, all rights under the International Convention for the Protection of Industrial Property and prolongations of the Applications and Patents.

Now, THEREFORE, for other good and valuable consideration, Assignor, by these presents does hereby irrevocably sell, assign, and transfer unto Assignee, its successors, assigns, and legal representatives the full and exclusive right in and to:

- (a) the Applications and Patents in the United States and the entire right, title, and interest in and to any and all issued patents or patent applications which may be granted therefor and/or therefrom in the United States, to all divisions, reissues, substitutions, continuations, continuations-in-part, and extensions of said Applications and Patents and any pending applications or issued patents that directly claim or are amended to claim priority to any of the Applications or Patents;
- (b) all causes of action (whether known or unknown or whether currently pending, filed or otherwise) and other enforcement rights under or on account of the Applications and Patents, including without limitation all causes of action and other enforcement rights for damages, injunctive relief, and any other remedies of any kind for past, current and future infringement; and
- (c) all rights to collect royalties or other payments under or on account of the Applications and Patents and the foregoing subcategory (b).

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue all patents for the Applications, or patents resulting therefrom, insofar as Assignor's interests are concerned, to Assignee, of the entire right, title, and interest in and to the same, for its sole use and benefit; and for the use and benefit of its legal representatives, to the full end of the term for which said patents may be granted, as fully and entirely as the same would have been held by the Assignor had this assignment not been made.

Assignor also sells and assigns to Assignee, its successors, assigns and legal representatives the full and exclusive right, title, and interest in and to the Inventions disclosed in

said Applications throughout the world, including the right to file applications and obtain patents, utility models, industrial models, and designs for the inventions in the Assignee's own name throughout the world, including all rights of priority, all rights to publish cautionary notices reserving ownership of the inventions and all rights to register the inventions in appropriate registries, all foreign rights arising from pre-grant publication of the Applications; and Assignor further agrees to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such right, title and interest in Assignee, its successors, assigns and legal representatives.

Assignor further agrees to communicate to Assignee, its successors, assigns and/or legal representatives, any known facts respecting any improvements, and, at the expense of Assignee, to testify in any legal proceedings, sign all lawful papers, execute all divisional, continuation, continuation-in-part, reissue and substitute applications, make all lawful oaths, and generally do everything possible to vest title in Assignee and to aid Assignee, its successors, assigns and legal representatives to obtain and enforce proper protection for the Inventions in all countries.

[Signature Page to Follow]

G.R. Mohan Rao
G.R. Mohan Rao

April 27, 2015
Date

STATE OF: Texas §

COUNTY OF: Dallas §

BEFORE ME, a Notary Public, on this 27th day of April, 2015, personally appeared G.R. MOHAN RAO, known to me to be the person whose name is subscribed to the foregoing instrument and acknowledged to me that he/she executed same of his/her own free will for the purposes and consideration therein expressed.

[SEAL]

Kristy Lea Kyles
Notary Public
Commission Expires: 9-9-17

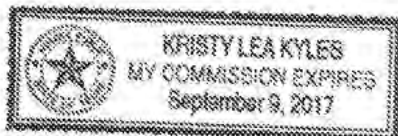


EXHIBIT A

	Atty. Ref.	Country	Serial No.	Patent No.	Title
1.	32625	US	10/934,915		Semiconductor Devices with Graded Dopant Regions
2.	32611	US	11/622,496	8,421,195	Semiconductor Devices with Graded Dopant Regions
3.	32612	US	12/549,283	8,106,481	Semiconductor Devices with Graded Dopant Regions
4.	32626	US	13/854,319		Semiconductor Devices with Graded Dopant Regions
5.	32613	US	14/515,584		Semiconductor Devices with Graded Dopant Regions
6.	32623	US	60/982,175		Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
7.	32614	US	12/256,362	7,855,916	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
8.	32615	US	12/915,177	8,194,452	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
9.	32616	US	13/458,173	8,531,880	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
10.	32617	US	13/967,649	8,817,537	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
11.	32618	US	14/335,160		Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
12.	32624	US	61/509,257		Lifetime Mixed Level Non-Volatile Memory System
13.	32619	US	13/455,267	8,891,298	Lifetime Mixed Level Non-Volatile Memory System
14.	32620	US	14/525,411		Lifetime Mixed Level Non-Volatile Memory System



United States Patent and Trademark Office

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Your assignment has been received by the USPTO.
The coversheet of the assignment is displayed below:

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1

Stylesheet Version v1.2

SUBMISSION TYPE:	NEW ASSIGNMENT										
NATURE OF CONVEYANCE:	CONFIRMATORY ASSIGNMENT										
CONVEYING PARTY DATA											
<table border="1"><thead><tr><th>Name</th><th>Execution Date</th></tr></thead><tbody><tr><td>VERVAIN, LLC</td><td>03/07/2022</td></tr></tbody></table>	Name	Execution Date	VERVAIN, LLC	03/07/2022							
Name	Execution Date										
VERVAIN, LLC	03/07/2022										
RECEIVING PARTY DATA											
<table border="1"><tr><td>Name:</td><td>GREENTHREAD, LLC</td></tr><tr><td>Street Address:</td><td>4544 HARRYS LANE</td></tr><tr><td>City:</td><td>DALLAS</td></tr><tr><td>State/Country:</td><td>TEXAS</td></tr><tr><td>Postal Code:</td><td>75229-5400</td></tr></table>	Name:	GREENTHREAD, LLC	Street Address:	4544 HARRYS LANE	City:	DALLAS	State/Country:	TEXAS	Postal Code:	75229-5400	
Name:	GREENTHREAD, LLC										
Street Address:	4544 HARRYS LANE										
City:	DALLAS										
State/Country:	TEXAS										
Postal Code:	75229-5400										
PROPERTY NUMBERS Total: 1											
<table border="1"><thead><tr><th>Property Type</th><th>Number</th></tr></thead><tbody><tr><td>Application Number:</td><td>17371839</td></tr></tbody></table>	Property Type	Number	Application Number:	17371839							
Property Type	Number										
Application Number:	17371839										
CORRESPONDENCE DATA											
Fax Number:	(972)628-3616										
Phone:	9726283600										

Greenthread Ex. 2020, p. 56
Semiconductor v. Greenthread

Email: admin@dalpat.com <i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i> Correspondent Name: GREGORY M. HOWISON Address Line 1: P.O. DRAWER 800889 Address Line 4: DALLAS, TEXAS 75380	
ATTORNEY DOCKET NUMBER:	GRTD60-35314
NAME OF SUBMITTER:	GREGORY M. HOWISON
Signature:	/Gregory M. Howison, Reg. #30646/
Date:	03/07/2022
Total Attachments: 2 source=GRT35314 Confirmatory Assignment exe#page1.tif source=GRT35314 Confirmatory Assignment exe#page2.tif	
RECEIPT INFORMATION EPAS ID: PAT7210634 Receipt Date: 03/07/2022	

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PATENT ASSIGNMENT COVER SHEET

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 Stylesheet Version v1.2

EPAS ID: PAT6827716

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
	Name	Execution Date
	MR G.R. MOHAN RAO	09/09/2017
RECEIVING PARTY DATA		
Name:	GREENTHREAD, LLC	
Street Address:	4544 HARRYS LANE	
City:	DALLAS	
State/Country:	TEXAS	
Postal Code:	75229	
PROPERTY NUMBERS Total: 1		
Property Type	Number	
Application Number:	17371839	
CORRESPONDENCE DATA		
Fax Number:	(972)628-3616	
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>		
Phone:	9726283624	
Email:	ipdocketing@munckwilson.com	
Correspondent Name:	GREGORY M HOWISON	
Address Line 1:	12770 COIT RD STE 600 STE 660	
Address Line 2:	STE 660	
Address Line 4:	DALLAS, TEXAS 75251	
NAME OF SUBMITTER:	GREGORY HOWISON	
SIGNATURE:	/Gregory Howison - Reg# 30646/	
DATE SIGNED:	07/22/2021	
Total Attachments: 4		
source=GRT34138RaotoGreenthreadASSMTEXE#page1.tif		
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source=GRT34138RaotoGreenthreadASSMTEXE#page4.tif		

ASSIGNMENT

WHEREAS, G.R. MOHAN RAO, an individual, residing at 1611 Willingham Drive, Allen, Texas 75013 ("Assignor"), has invented certain new and useful inventions set forth on the attached Exhibit A (collectively, the "Inventions"), for which certain applications for United States and foreign patents were filed as set forth on Exhibit A (collectively, the "Applications"), and from which certain United States patents have issued as set forth on Exhibit A (collectively, the "Patents"); and

WHEREAS, GREENTHREAD, LLC, a Texas Limited Liability Company, having a business address at 4544 Harry's Lane, Dallas, Texas 75229-5400 ("Assignee"), is desirous of acquiring the entire right, title, and interest in and to the Applications and Patents and any and all foreign counterparts, divisions, continuations, continuation-in-parts, improvements, reexaminations, reissues, extensions, renewals, substitutes, provisional applications, certificates, all rights under the International Convention for the Protection of Industrial Property and prolongations of the Applications and Patents.

Now, THEREFORE, for other good and valuable consideration, Assignor, by these presents does hereby irrevocably sell, assign, and transfer unto Assignee, its successors, assigns, and legal representatives the full and exclusive right in and to:

- (a) the Applications and Patents in the United States and the entire right, title, and interest in and to any and all issued patents or patent applications which may be granted therefor and/or therefrom in the United States, to all divisions, reissues, substitutions, continuations, continuations-in-part, and extensions of said Applications and Patents and any pending applications or issued patents that directly claim or are amended to claim priority to any of the Applications or Patents;
- (b) all causes of action (whether known or unknown or whether currently pending, filed or otherwise) and other enforcement rights under or on account of the Applications and Patents, including without limitation all causes of action and other enforcement rights for damages, injunctive relief, and any other remedies of any kind for past, current and future infringement; and
- (c) all rights to collect royalties or other payments under or on account of the Applications and Patents and the foregoing subcategory (b).

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue all patents for the Applications, or patents resulting therefrom, insofar as Assignor's interests are concerned, to Assignee, of the entire right, title, and interest in and to the same, for its sole use and benefit; and for the use and benefit of its legal representatives, to the full end of the term for which said patents may be granted, as fully and entirely as the same would have been held by the Assignor had this assignment not been made.

Assignor also sells and assigns to Assignee, its successors, assigns and legal representatives the full and exclusive right, title, and interest in and to the Inventions disclosed in

said Applications throughout the world, including the right to file applications and obtain patents, utility models, industrial models, and designs for the inventions in the Assignee's own name throughout the world, including all rights of priority, all rights to publish cautionary notices reserving ownership of the inventions and all rights to register the inventions in appropriate registries, all foreign rights arising from pre-grant publication of the Applications; and Assignor further agrees to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such right, title and interest in Assignee, its successors, assigns and legal representatives.

Assignor further agrees to communicate to Assignee, its successors, assigns and/or legal representatives, any known facts respecting any improvements, and, at the expense of Assignee, to testify in any legal proceedings, sign all lawful papers, execute all divisional, continuation, continuation-in-part, reissue and substitute applications, make all lawful oaths, and generally do everything possible to vest title in Assignee and to aid Assignee, its successors, assigns and legal representatives to obtain and enforce proper protection for the Inventions in all countries.

[Signature Page to Follow]

G.R. Mohan Rao
G.R. Mohan Rao

April 27, 2015
Date

STATE OF: Texas §

COUNTY OF: Dallas §

BEFORE ME, a Notary Public, on this 27th day of April, 2015, personally appeared G.R. MOHAN RAO, known to me to be the person whose name is subscribed to the foregoing instrument and acknowledged to me that he/she executed same of his/her own free will for the purposes and consideration therein expressed.

[SEAL]

Kristyle Kyles
Notary Public
Commission Expires: 9-9-17

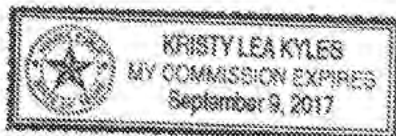


EXHIBIT A

	Atty. Ref.	Country	Serial No.	Patent No.	Title
1.	32625	US	10/934,915		Semiconductor Devices with Graded Dopant Regions
2.	32611	US	11/622,496	8,421,195	Semiconductor Devices with Graded Dopant Regions
3.	32612	US	12/549,283	8,106,481	Semiconductor Devices with Graded Dopant Regions
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7.	32614	US	12/256,362	7,855,916	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
8.	32615	US	12/915,177	8,194,452	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
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10.	32617	US	13/967,649	8,817,537	Nonvolatile Memory Systems with Embedded Fast Read and Write Memories
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14.	32620	US	14/525,411		Lifetime Mixed Level Non-Volatile Memory System

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT6827495

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
	Name	Execution Date
	GREENTHREAD, LLC	08/19/2019
RECEIVING PARTY DATA		
Name:	VERVAIN, LLC	
Street Address:	724 MASON DELLS DRIVE	
City:	DALLAS	
State/Country:	TEXAS	
Postal Code:	75230	
PROPERTY NUMBERS Total: 1		
Property Type	Number	
Application Number:	17371839	
CORRESPONDENCE DATA		
Fax Number:	(972)628-3616	
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>		
Phone:	972-628-3624	
Email:	ipdocketing@munckwilson.com	
Correspondent Name:	GREGORY HOWISON	
Address Line 1:	12770 COIT ROAD SUITE 660	
Address Line 2:	SUITE 660	
Address Line 4:	DALLAS, TEXAS 75251	
NAME OF SUBMITTER:	GREGORY HOWISON	
SIGNATURE:	/Gregory Howison - Reg# 30646/	
DATE SIGNED:	07/22/2021	
Total Attachments: 2		
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ASSIGNOR Greenthread, LLC Philip W. John, Jr. Manager 6307 Bandera Ave, Apt B Dallas, Texas 75225-3617 Email: john@greenthreadllc.com	ASSIGNEE Vervain, LLC Philip W. John, Jr., Member 7424 Mason Dells Drive Dallas, Texas 75230-3244 Email: john@vervainllc.com
--	---

ASSIGNMENT AGREEMENT

This Assignment Agreement ("Assignment") is entered into by and between Vervain, LLC, a Texas limited liability company, hereinafter referred to as "Assignee," and Greenthread, LLC, a Texas limited liability company, hereinafter referred to as "Assignor," and shall become effective upon being duly signed by the authorized representative of Assignor ("Effective Date").

RECITALS:

Assignor and Assignee are entering into a Patent Assignment Agreement (the "Agreement").

Pursuant to the Agreement, Assignor hereby desires to assign to Assignee all of its rights, title and interest in and to the following United States patents and pending application:

1. U.S. Provisional Application Number ~~61/509,256~~ ^{61/509,257}, entitled, "Lifetime Mixed Level Nand Flash System," filed on July 19, 2011;
2. U.S. Patent Number 8,891,298, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on April 25, 2012, and issued on November 18, 2014;
3. U.S. Patent Number 9,196,385, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on October 28, 2014, and issued on November 24, 2015;
4. U.S. Patent Number 9,997,240, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on November 24, 2015, and issued on June 12, 2018, and
5. U.S. Patent Application Number 16/006,299, entitled, "Lifetime Mixed Level Non-Volatile Memory System," filed on June 12, 2018, and is pending (collectively referred to hereinafter referred to as the "Patent").

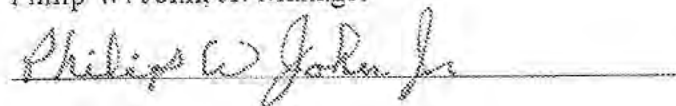
For good and valuable consideration, Assignor and Assignee hereby agree as follows:

ASSIGNMENT:

1. Assignor hereby assigns to Assignee its entire worldwide right, title and interest in and to Assignor's Patent, including the entire worldwide right, title and interest in and to any reexamination or reissue of the Patent. This includes, without limitation, Assignor's right to prosecute, and receive, all damages, royalties, awards and compensation for past, present and/or future infringement.
2. Assignor agrees to do the following without further consideration, in order to carry out the intent of this Assignment:
 - i. Execute all oaths, assignments, applications, and other papers necessary or desirable to fully secure to Assignee the rights, titles and interests herein conveyed; and
 - ii. Generally do all lawful acts for vesting in Assignee the rights, titles, and interests herein conveyed.
3. Assignor has not made and will not hereafter make any assignment, grant, mortgage, license, or other agreement affecting the rights, titles, and interests herein conveyed to Assignee.
4. Assignor hereby represents and warrants that Assignor has the authority to assign the applicable Patent pursuant to this Assignment.

The undersigned having read this Assignment and fully understanding the provisions of this Assignment, hereby executes this Assignment as of the Effective Date,

Greenthread, LLC (Assignor)
Philip W. John, Jr. Manager



Signature:

Printed Name: Philip W. John, Jr.

Date: August 9, 2019

CONFIRMATORY ASSIGNMENT

Whereas, **VERVAIN, LLC**, a Texas limited liability company, located at 724 Mason Dells Drive, Dallas, Texas 75230 ("Assignor"), hereby confirms that it has zero right, title and interest in and to the currently pending application entitled, SEMICONDUCTOR DEVICES WITH GRADED DOPANT REGIONS (the "Invention"), for which United States Patent Application was filed on July 9, 2021 (Serial No. 17/371,839) (the "Application"), and confirms the Assignment previously Assigned and recorded at reel/frame 056950/0048 on July 22, 2021 from inventor G.R. Mohan RAO to Greenthread, LLC is the only valid Assignment and the Assignment recorded on July 22, 2021 from Greenthread, LLC to Vervain, LLC at reel/frame 056949/0013 was in error as it did not list the Application; and

Whereas, **GREENTHREAD, LLC**, a Texas Limited Liability Company, located at 4544 Harrys Lane, Dallas, Texas 75229-5400 ("Assignee"), is desirous of confirming that the entire right, title, and interest in the Application is fully vested in Assignee, and desires confirmation that Assignee has never assigned any interest in and to the Application to Assignor and that Assignor has no rights to this Application, as no rights have ever been conveyed to Assignor.

Now, Therefore, for other good and valuable consideration, Assignor, by these presents does hereby sell, assign, and transfer unto Assignee, its successors, assigns, and legal representatives the full and exclusive right to the Application in the United States and the entire right, title, and interest in and to any and all Patents which may be granted therefore and/or therefrom in the United States, to all divisions, reissues, substitutions, continuations, continuations-in-part, and extensions of said application. Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks to issue all patents for the Invention, or patents resulting therefrom, insofar as Assignor's interests are concerned, to Assignee, of the entire right, title, and interest in and to the same, for his sole use and benefit; and for the use and benefit of his legal representatives, to the full end of the term for which said Patent(s) may be granted, as fully and entirely as the same would have been held by the Assignor had this assignment not been made.

Assignor also sells and assigns to Assignee, its successors, assigns and legal representatives the full and exclusive right, title, and interest to the Invention disclosed in said Application throughout the world, including the right to file applications and obtain patents, utility models, industrial models, and designs for the Invention in the Assignee's own name throughout the world, including all rights of priority, all rights to publish cautionary notices reserving ownership of the Invention and all rights to register the Invention in appropriate registries, all foreign rights arising from pre-grant publication of the Application; and Assignor further agrees to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such right, title and interest in Assignee, its successors, assigns and legal representatives.

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Assignor further authorizes and directs Assignee's attorneys to insert the serial number and filing date of said application now identified by the attorney docket number and title set forth above as soon as the same shall have been made known to them by the United States Patent and Trademark Office.

VERVAIN, LLC

By: Philip W. Sohn Jr
Name: Philip W. Sohn Jr
Title: MANAGER
Date: 3/7/2022

EXHIBIT 4

ON Semiconductor Accused Products

The following list of Accused Products is exemplary, non-exhaustive, and non-limiting. Greenthread identifies the following list to illustrate each category or type of product that constitutes an ON Semiconductor Accused Product, and this listing is therefore exemplary, non-exhaustive, and non-limiting. Greenthread further asserts claims against all product variations and part numbers of the ON Semiconductor Accused Products. All of the below product categories were identified by ON Semiconductor's website at <https://www.onsemi.com/products>

ON Semiconductor Accused Product Categories/Types	
1.	Discrete & Power Modules
2.	Power Management
3.	Signal Conditioning & Control
4.	Sensors
5.	Motor Control
6.	Custom & ASSP
7.	Interfaces
8.	Wireless Connectivity
9.	Timing, Logic & Memory

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

U.S. Patent No. 10,510,842	Accused Products ON Semiconductor AR0820AT CMOS Image Sensor
[Claim 1, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the ON Semiconductor Accused Products include a semiconductor device. This chart includes exemplary information regarding a representative example of the ON Semiconductor Accused Products, the ON Semiconductor AR0820AT, 1/2" Format, 8.3 MP, 2.1 micrometer Pixel Pitch, Stacked Back-illuminated CMOS Image Sensor with DR-Pix Technology ("AR0820AT"). The AR0820AT was analyzed in the below-referenced report from Tech Insights. The complete report is hereby incorporated by reference into each and every claim and claim element discussed. "ON Semiconductor AR0820AT, 1/2" Format, 8.3 MP, 2.1 micrometer Pixel Pitch, Stacked Back-illuminated CMOS Image Sensor with DR-Pix Technology for Automotive Applications Device Essentials Plus Summary," available at https://library.techinsights.com/search/device-details?tab=reports&id=DEP-2004-801&genealogyCode=ONS-LI-AR0820-GMSL2_Front-Cam ("AR0820AT Report"). Selected pages are reproduced herein to aid in understanding.  techinsights.com  Device Essentials Plus Summary AR0820AT Report at Cover.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

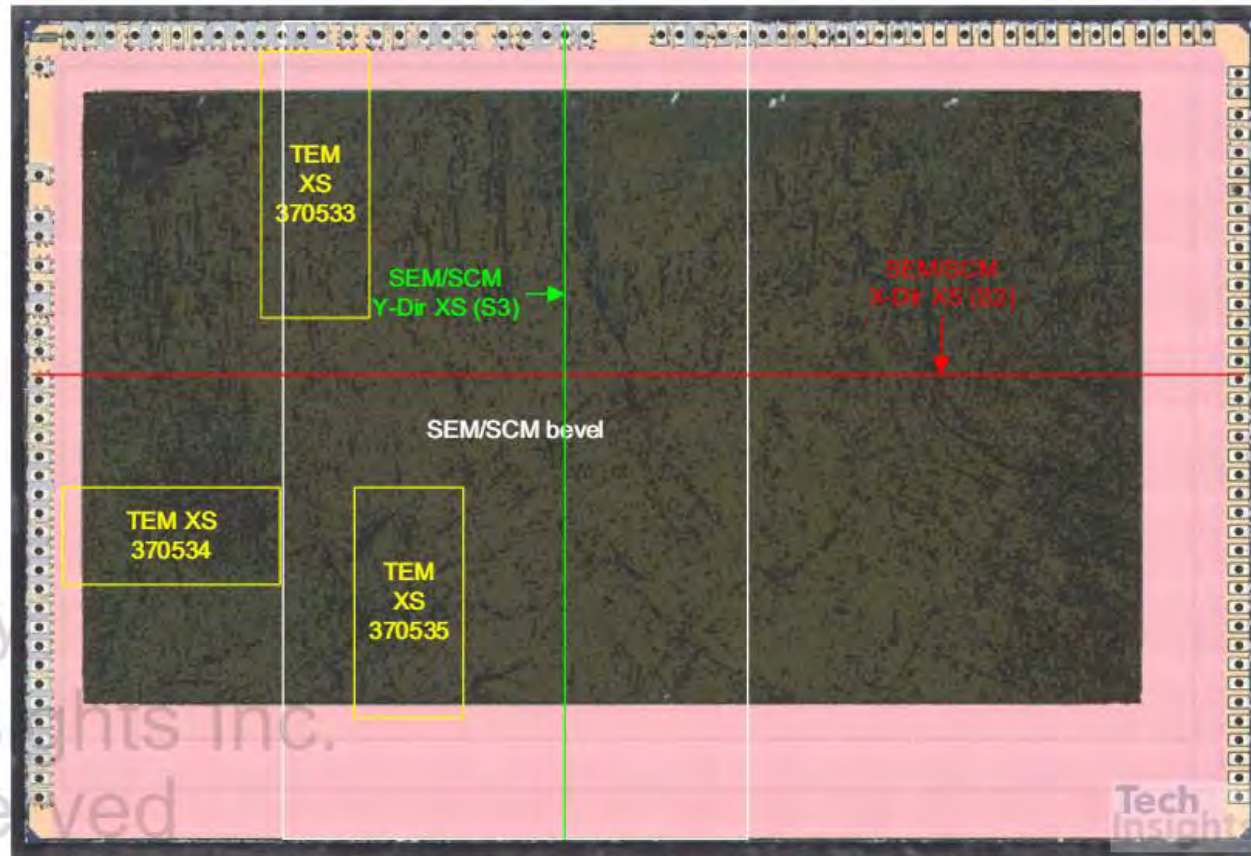
The ON Semiconductor AR0820AT is representative of the ON Semiconductor Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other ON Semiconductor Accused Products would have similarly been advantageously designed to move carriers (e.g., towards the substrate) and achieve the performance enhancements described and claimed in the '842 patent (and the other asserted patents). For example, the other ON Semiconductor Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the '842 patent (and the other asserted patents). The claimed invention would have application in numerous types of ON Semiconductor products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other ON Semiconductor Accused Products contain similar features as the ON Semiconductor AR0820AT transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other ON Semiconductor Accused Products contain similar features as the ON Semiconductor AR0820AT, and function in a similar way with respect to the features claimed in the asserted claims.

This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery. The ON Semiconductor Accused Products, of which ON Semiconductor AR0820AT is one example, are semiconductor devices.

Device Summary – CIS

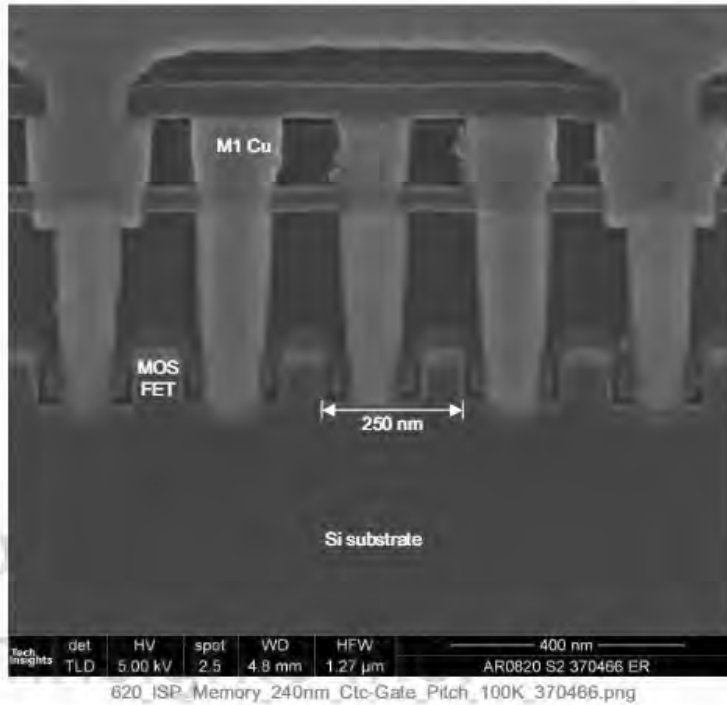
Manufacturer	ON Semiconductor
Foundry	TSMC
Part number	AR0820AT
Type	Stacked BI CIS
Active Si thickness	2.9 μm
Die size, measured from the die edge	9.76 mm $\times$ 6.53 mm (63.7 mm ²)
Die size, measured from the die seal	9.70 mm $\times$ 6.47 mm (62.8 mm ²)
Process type	Stacked BI CMOS imager
Number of metal layers (CIS)	4 Cu pixel interconnect + 1 Cu hybrid bond pad + back W shield/grid + back Al bond pad
Number of poly layers (CIS)	1
Contacted logic gate pitch (CIS)	–
Minimum metal pitch logic (CIS)	–
Minimum metal pitch pixel array (CIS)	250 nm
Process generation (CIS)	90 nm
Features measured to determine process generation	Minimum metal pitch

Sample Locations – SEM, SCM, and TEM Analyses



LI-AR0820-GMSL2_060H_Front-Cam_AR0820_2018_CIS_371697_Oriented_ann.png

ISP Minimum Contacted Gate Pitch

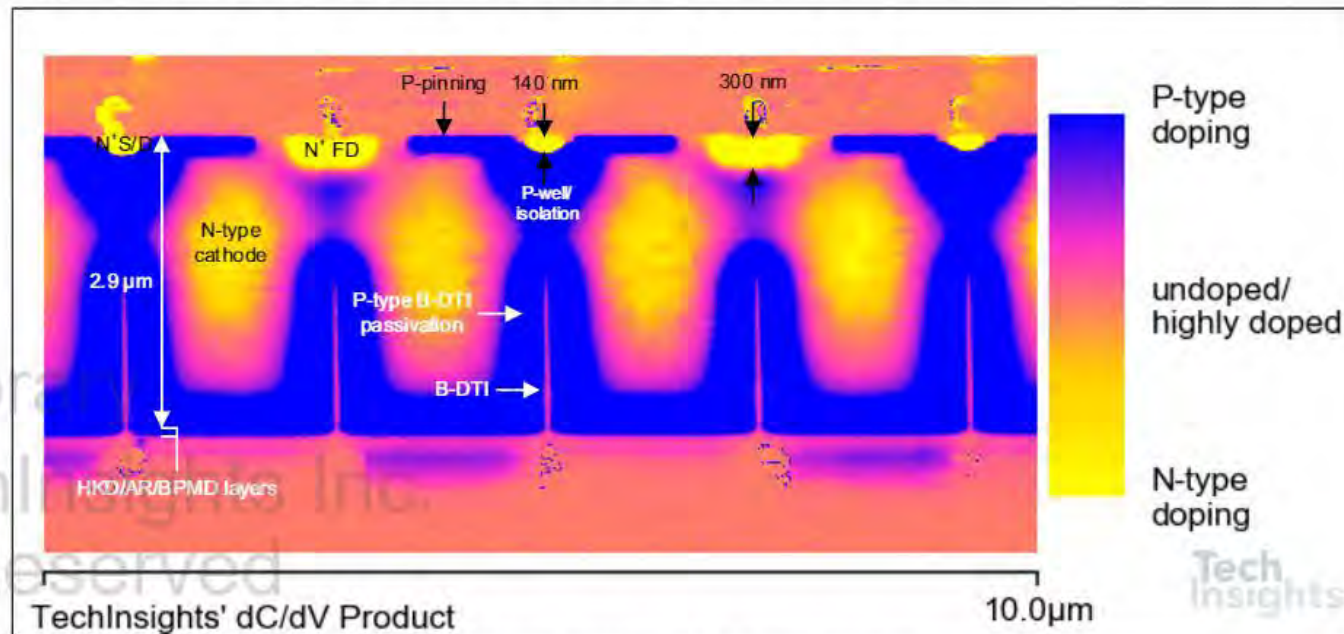


- The minimum contacted gate pitch of 250 nm was observed in the 6T SRAM.
- The minimum contacted gate pitch observed in the logic region was 260 nm.
- The ISP is manufactured by TSMC using a 65 nm CMOS process generation

SRAM Contacted Gate Pitch

CIS Active Si and Wells – SCM Pixel Array

- Pages 51 and 52 show SCM and sMIM-C cross section images, respectively, through N⁺ FD and N⁺ S/D regions.
- The N⁺ FD and region is 300 nm deep and the N⁺ S/D is 140 nm deep.
- The P-well/isolation region is 0.68 μm deep.
- Note: The P-type region at the back of the active Si looks thicker than it is; this is likely due to the smearing of the P-type doping onto the HKD/AR and BPDM layers during the sample preparation.

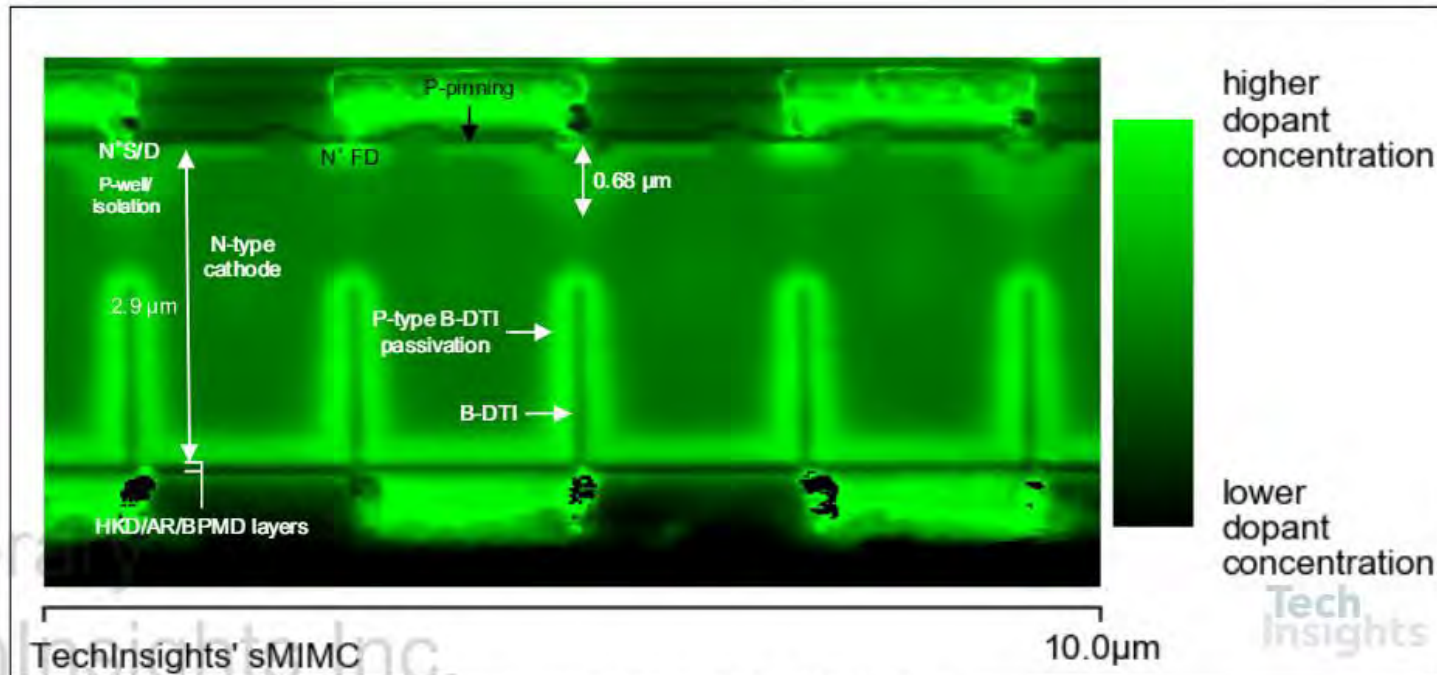


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AR0820AT Report at 51.

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CIS Active Si and Wells – SCM Pixel Array



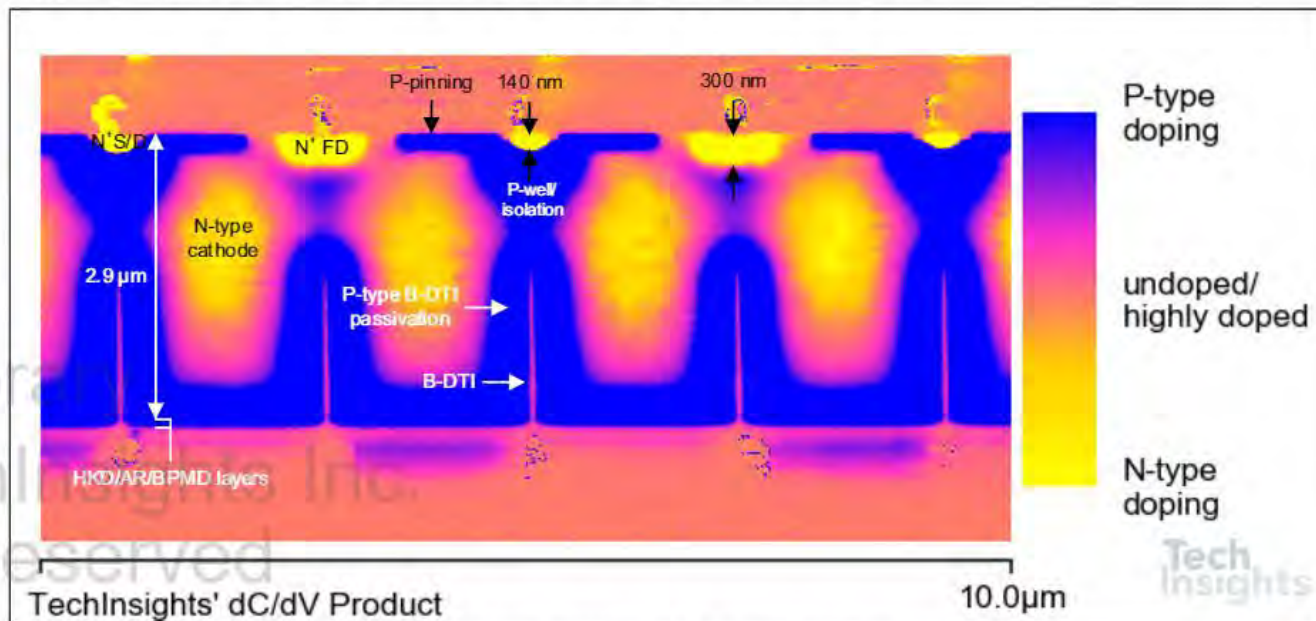
[Claim 1, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;

The ON Semiconductor Accused Products include/comprise a semiconductor device comprising a substrate of a first doping type at a first doping level having first and second surfaces. For example, analysis of an exemplary ON Semiconductor Accused Product (the ON Semiconductor AR0820AT discussed above) reveals the presence of such a substrate.

For example, the ON Semiconductor AR0820AT discussed above for Claim 1, Preamble, was imaged using scanning electron microscopy (SEM) scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. The SCM image of the pixel array shows a silicon (Si) substrate having a first doping type (n-type) at a first doping level, the substrate having a first and second surface.

CIS Active Si and Wells – SCM Pixel Array

- Pages 51 and 52 show SCM and sMIM-C cross section images, respectively, through N⁺ FD and N⁺ S/D regions.
- The N⁺ FD and region is 300 nm deep and the N⁺ S/D is 140 nm deep.
- The P-well/isolation region is 0.68 μm deep.
- Note: The P-type region at the back of the active Si looks thicker than it is; this is likely due to the smearing of the P-type doping onto the HKD/AR and BPDM layers during the sample preparation.



0711201032_PRODUCT_FRW_10.0u_512p_370466.png

N⁺ FD and N⁺ S/D Regions – SCM

51

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AR0820AT Report at 51.

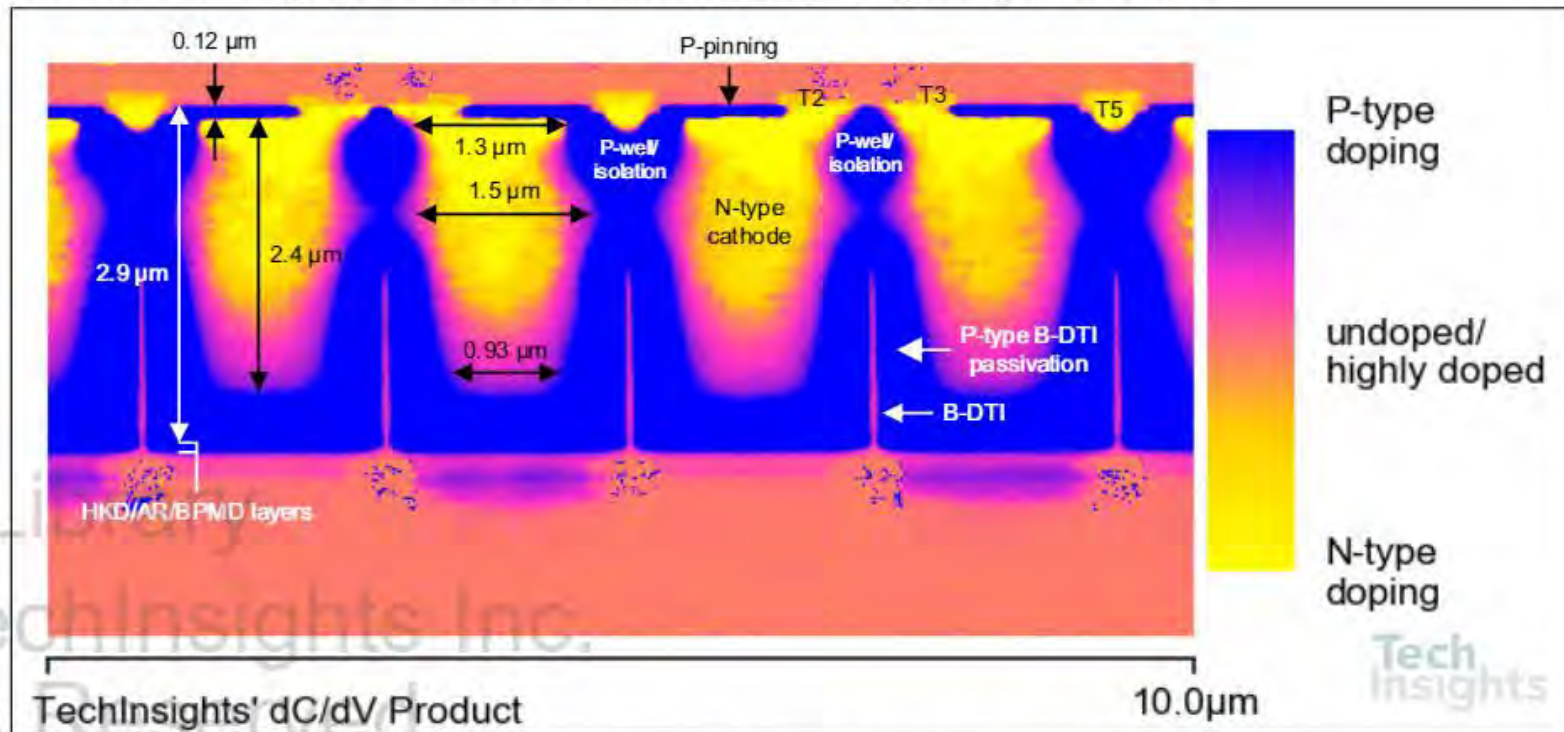
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Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

[Claim 1, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The ON Semiconductor Accused Products, and products incorporating them, include/comprise a semiconductor device comprising a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed. For example, as shown in imagery from the Tech Insights Report, the exemplary ON Semiconductor AR0820AT scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis includes a first active region disposed adjacent the first surface of the substrate. See below showing a transistor within “P-wells” where P-wells are formed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed (see, for example, T2, T3, T5 labeled below in the SCM image where transistors is formed). Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.
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Pixel Cross Section Analysis – X-Direction

- SCM cross section image through section line G (T2 and T3 XFER gates).
- The N-type photocathode is 2.4 μm thick. As shown in the sMIM-C image on the next page, the top region of the photocathode has a higher doping concentration.
- The width of the N-type photocathode varies from 0.93-1.5 μm , depending on the location.

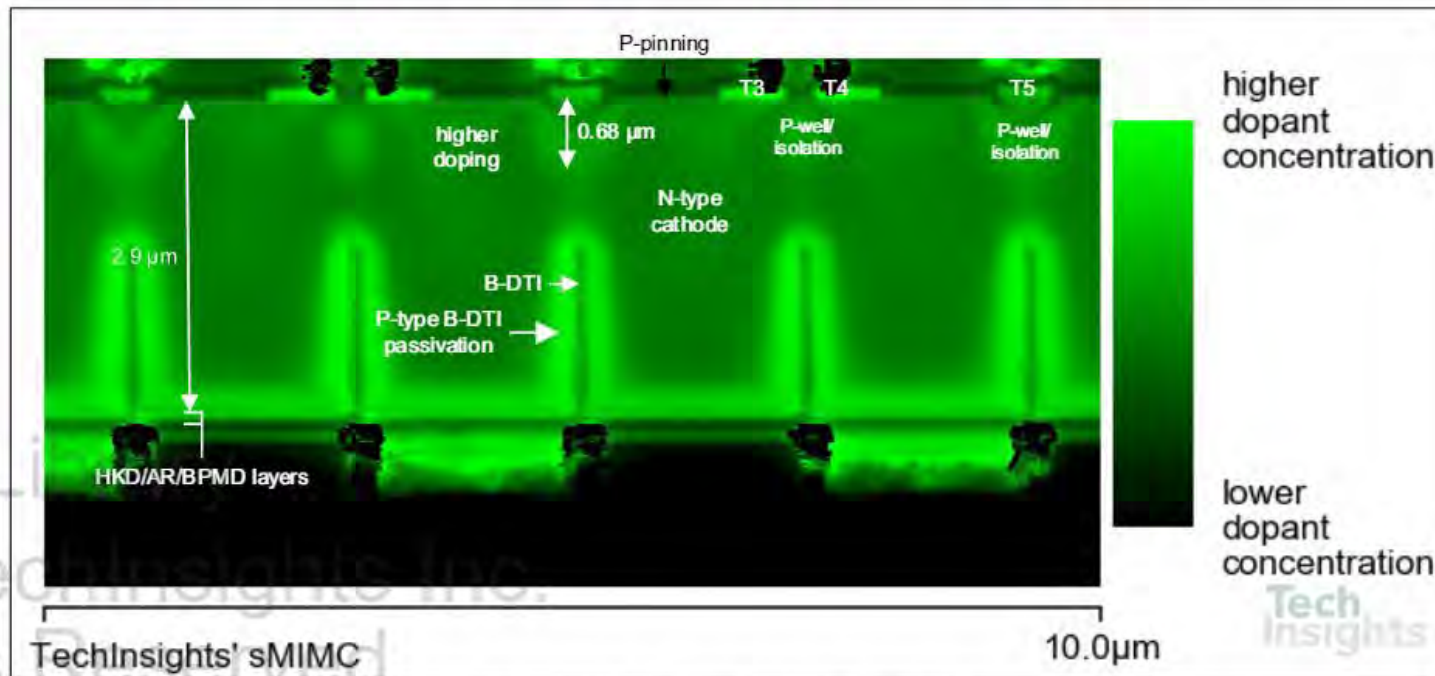


0711201114_PRODUCT_FRW_10.0u_512p_370466.png

T2 and T3 (XFER) Gates and Photocathode (Section Line G) – SCM

Pixel Cross Section Analysis – X-Direction

- sMIM-C cross section overview image through section line G (T2 and T3 XFER gates)
- The P-well/isolation region is 0.68 μm thick.
- The sMIM-C image shows that the upper and center regions of the photocathode have a higher doping concentration.



0711201114_SMIMC_FRW_10.0u_512p_370466.png

T2 and T3 (XFER) Gates and Photocathode (Section Line G) – sMIM-C

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Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

[Claim 1, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The ON Semiconductor Accused Products include a semiconductor device comprising a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed. For example, the images reproduced at Claim 1, Element 2 show an active region within which transistors can be formed. Details regarding formation of transistors are in the possession of Defendants and are expected to be obtained through discovery.
[Claim 1, Element 4] transistors formed in at least one of the first active region or second active region; and	The ON Semiconductor Accused Products include a semiconductor device comprising transistors formed in at least one of the first active region or second active region. See above images reproduced at Claim 1, Element 2, showing where the transistors are formed (T2, T3, T5).
[Claim 1, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.	The ON Semiconductor Accused Products meet this limitation. See images reproduced above at Claim 1, Element 2 showing the active regions of the transistors having graded dopants. For example, this is shown by the scanning capacitance/microwave impedance microscopy (SCM/sMIM) analysis. SCM/sMIM electrically characterizes the tested device and generates maps which provide graphical representation of the dopant types and concentrations by measuring carrier movement as they are attracted to or repulsed by the probe. The SCM/sMIM maps taken from ON Semiconductor Accused Products shown herein demonstrate differences in carrier concentration as a function of depth, which generate electric fields within the accused products. The contrast in the SMIM image is proportional to the capacitance of the sample under inspection, so that brighter green corresponds to higher dopant concentration, and darker green/black corresponds to lower dopant concentration. Likewise, the SCM images above show doping concentration and doping type as indicated in the legends to the right.

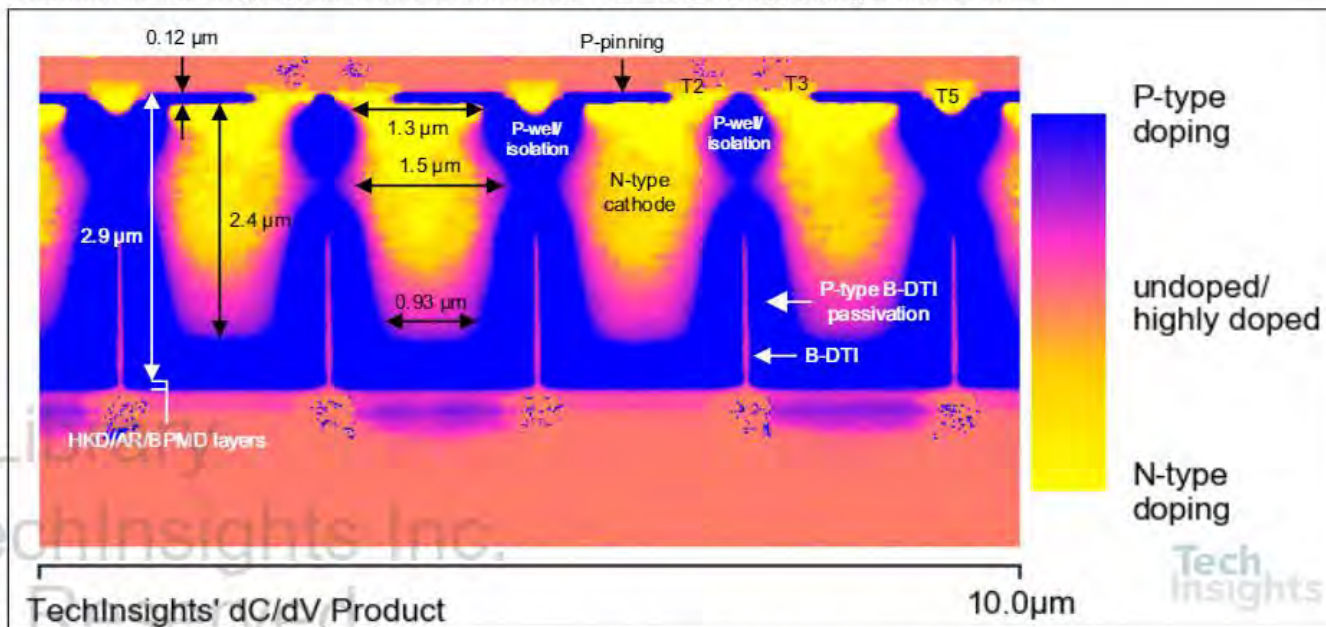
Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

5. The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.	The ON Semiconductor Accused Products meet this limitation. As shown above, the first and second active regions contains n-channel devices. See Tech Insights Report images reproduced above at Claim 1, Element 1.
6. The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The ON Semiconductor Accused Products meet this limitation. As shown above, P-wells are used in this device, and the wells include graded dopants. The first and second active regions accordingly contain n-channel devices. See Tech Insights Report images reproduced at Claim 1, Element 2.
7. The semiconductor device of claim 1, wherein the first active region and second active region are	The ON Semiconductor Accused Products meet this limitation. The substrate of the ON Semiconductor Accused Products have isolation regions that separate the first and second active region, as shown in the SCM cross-section below (labeled "P-well/isolation").

each separated by at least one isolation region.

Pixel Cross Section Analysis – X-Direction

- SCM cross section image through section line G (T2 and T3 XFER gates).
- The N-type photocathode is 2.4 μm thick. As shown in the sMIM-C image on the next page, the top region of the photocathode has a higher doping concentration.
- The width of the N-type photocathode varies from 0.93-1.5 μm , depending on the location.



0711201114_PRODUCT_FRW_10.0u_512p_370466.png

T2 and T3 (XFER) Gates and Photocathode (Section Line G) – SCM

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AR0820AT Report at 152.

8. The semiconductor device of claim 1, wherein the

Upon information and belief, the graded dopant is fabricated with an ion implantation process. For example, ion implantation is the prevalent process for implementing doping in semiconductor devices, and is believed to be used for the ON Semiconductor Accused Products. Because it is well known in the art, ON Semiconductor Accused Products likely meet this limitation. Information about the fabrication process for the ON Semiconductor Accused Products, including usage of an ion implantation process, is in the possession of Defendants and is expected to be obtained through discovery.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

graded dopant is fabricated with an ion implantation process.	
[Claim 9, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the ON Semiconductor Accused Products include a semiconductor device. <i>See above at Claim 1, Preamble.</i>
[Claim 9, Element 1] a substrate of a first doping type at a first doping level having first and second surfaces;	The ON Semiconductor Accused Products meet this limitation. <i>See above at Claim 1, Element 1.</i>
[Claim 9, Element 2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;	The ON Semiconductor Accused Products meet this limitation. <i>See above at Claim 1, Element 2.</i>

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

[Claim 9, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;	The ON Semiconductor Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 3.
[Claim 9, Element 4] transistors formed in at least one of the first active region or second active region; and	The ON Semiconductor Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 4.
[Claim 9, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate.	The ON Semiconductor Accused Products meet this limitation. <i>See</i> above at Claim 1, Element 5.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

13. The semiconductor device of claim 9, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.	The ON Semiconductor Accused Products meet this limitation. <i>See above at Claim 5.</i>
14. The semiconductor device of claim 9, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has a graded dopant.	The ON Semiconductor Accused Products meet this limitation. <i>See above at Claim 6.</i>
15. The semiconductor device of claim 9, wherein the first active region and second active	Upon information and belief, the ON Semiconductor Accused Products meet this limitation. <i>See above at Claim 7.</i>

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

region are each separated by at least one isolation region.	
16. The semiconductor device of claim 9, wherein the graded dopant is fabricated with an ion implantation process.	Upon information and belief, the ON Semiconductor Accused Products meet this limitation. <i>See</i> above at Claim 8.
17. The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.	The ON Semiconductor Accused Products meet this limitation. <i>See</i> above at Claim 1, Elements 2-3.
18. The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring a	The ON Semiconductor Accused Products meet this limitation. As discussed above for Claim 1, the ON Semiconductor Accused Products include first and second active regions. Upon information and belief, CMOS transistors formed in the first and second active regions, the CMOS transistors requiring a source, a drain, a gate, and a channel region. Details regarding transistors used are in the possession of Defendants and are expected to be obtained through discovery.

Exhibit A-1 to Greenthread's Complaint (U.S. Patent No. 10,510,842)

source, a drain, a gate and a channel region.	
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U.S. Patent No. 11,121,222	Accused Products
[Claim 39, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the ON Semiconductor Accused Products include a semiconductor device. The AR0820AT, ½” Format, 8.3 MP, 2.1 micrometer Pixel Pitch, Stacked Back-illuminated CMOS Image Sensor with DR-Pix Technology (“AR0820AT”) discussed for claim 1 of Exhibit A-1 is a semiconductor device (<i>see</i> Exhibit A-1, Claim 1, Preamble). This chart includes exemplary information regarding a representative example of the ON Semiconductor Accused Products, the ON Semiconductor AR0820AT. The ON Semiconductor AR0820AT is representative of the ON Semiconductor Accused Products for purposes of this claim chart and the other infringement contention claim charts because upon information and belief, the other ON Semiconductor Accused Products would have similarly been advantageously designed to move carriers and achieve the performance enhancements described and claimed in the ’222 patent (and the other asserted patents). For example, the other ON Semiconductor Accused Products would similarly have been designed with a dopant gradient in order to improve performance characteristics such as on and off switching times and other performance enhancements described in the Abstract of the ’222 patent (and the other asserted patents). The claimed invention would have application in numerous types of ON Semiconductor products, including, but not limited to, amplifiers, audio processors, digital-to-analog converters, analog-to-digital converters, digital clocks, interface ICs, isolation ICS, microcontrollers and processors, digital signal processors, digital light processors, motor drivers, power management, switches & multiplexers, radio frequency and microwave ICs, wireless connectivity ICs, logic & voltage translation, sensors, and other ICs, because such products would benefit from, among other things, improved switching time for transistors in the device. Therefore, upon information and belief the other ON Semiconductor Accused Products contain similar features as the ON Semiconductor AR0820AT transistors depicted here, and function in a similar way with respect to the features claimed in the asserted claims, and the other ON Semiconductor Accused Products contain similar features as the ON Semiconductor AR0820AT, and function in a similar way with respect to the features claimed in the asserted claims. This claim chart is based on publicly available information, and additional information regarding these and other accused products is expected to be obtained through discovery.
[Claim 39, Element 1] a substrate of a first doping type at a first doping level;	The ON Semiconductor Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 39, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The ON Semiconductor Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 2.
[Claim 39, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The ON Semiconductor Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 3.

U.S. Patent No. 11,121,222	Accused Products
[Claim 39, Element 4] transistors formed in at least one of the first active region or second active region; and	The ON Semiconductor Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.
[Claim 39, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The ON Semiconductor Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 5. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 41, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the ON Semiconductor Accused Products include a semiconductor device. <i>See</i> above at Claim 39, Preamble.
[Claim 41, Element 1] a substrate of a first doping type at a first doping level;	The ON Semiconductor Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 41, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The ON Semiconductor Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 2.
[Claim 41, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The ON Semiconductor Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 3.
[Claim 41, Element 4] transistors formed in at least one	The ON Semiconductor Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.

U.S. Patent No. 11,121,222	Accused Products
of the first active region or second active region; and	
[Claim 41, Element 5] at least a portion of at least one of the first and second active regions having at least one graded dopant acceptor concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The ON Semiconductor Accused Products meet this limitation. <i>See</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.
[Claim 42, Preamble] A semiconductor device, comprising:	To the extent the preamble is a limitation, the ON Semiconductor Accused Products include a semiconductor device. <i>See</i> above at Claim 39, Preamble.
[Claim 42, Element 1] a substrate of a first doping type at a first doping level;	The ON Semiconductor Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 1.
[Claim 42, Element 2] a first active region disposed adjacent to a surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;	The ON Semiconductor Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 2.
[Claim 42, Element 3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;	The ON Semiconductor Accused Products meet this limitation. <i>See</i> above at Claim 39, Element 3.
[Claim 42, Element 4] transistors formed in at least one of the first active region or second active region; and	The ON Semiconductor Accused Products meet this limitation. <i>See</i> Exhibit A-1, Claim 1, Element 4.

U.S. Patent No. 11,121,222	Accused Products
[Claim 42, Element 5] at least a portion of at least one of the first and second active regions having at least one graded donor dopant concentration to aid carrier movement from the first or second active region to at least one substrate area where there is no active region.	The ON Semiconductor Accused Products meet this limitation. SCM/sMIM analysis (<i>see</i> Exhibit A-1, Claim 1, Element 5) reveals at least one graded dopant acceptor concentration (e.g., concentration in n-well) as claimed. <i>See also</i> SCM/sMIM analysis reproduced at Exhibit A-1, Claim 1, Element 5 electrically characterizing the accused product and showing carrier movement and electric fields. SCM/sMIM analysis generally is discussed at Exhibit A-1, Claim 1, Element 5.

**ON Semiconductor
AR0820AT, 1/2" Format, 8.3 MP,
2.1 μm Pixel Pitch, Stacked Back-Illuminated
CMOS Image Sensor with DR-Pix™ Technology
for Automotive Applications**

Device Essentials Plus Summary

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DEP-2004-801

105521OOWM

Published: August 4, 2020

DEP Content

- This is a Device Essentials Plus (DEP) summary document, provided as a companion deliverable for a Device Essentials Plus project. The DEP deliverable builds on the content generated in a Device Essentials (DEF) project.
- The DEF deliverable includes an analysis summary document and a pixel schematic, and is supported by unannotated image folders including:
 - Downstream product teardown images, package photographs and X-rays, die photograph, non-invasive optical photographs of die features, scanning electron microscopy (SEM) bevel images of the pixel array showing the metal, transistor, and diffusion levels, and exploratory cross-sectional SEM images of the general pixel array and peripheral structures
- The purpose of the DEP is to extend coverage of chip analysis beyond the SEM-based imaging used for DEF projects, and to expand the analyst commentary. A DEP contains interpreted results from transmission electron microscopy (TEM), TEM-based energy dispersive X-ray spectroscopy (TEM-EDS), TEM-based electron energy loss spectroscopy (TEM-EELS), secondary ion mass spectroscopy (SIMS) and scanning capacitance microscopy (SCM) analyses (the DEP scope is target device dependent).
- This DEP report includes a summary of salient features of the device and is supported with the following image folders:
 - TEM images of pre-metal dielectrics (PMD), deep trench isolation (DTI), back layers, microlenses, and microlens coating
 - TEM-EDS spectra of dielectrics, metals, DTI, back dielectrics, color filters, microlenses, and microlens coating
 - Scanning microwave impedance microscopy (SMIM) of the pixel photocathode (along horizontal and vertical cross section planes) and periphery
 - SIMS analysis of the CMOS image sensor (CIS) die pixel array and periphery

Overview

- The ON Semiconductor AR0820AT is a color, 8.3 MP, stacked, back-illuminated (BI) CIS, with on-sensor 140 dB high dynamic range (HDR) capability, for use in automotive applications [1].
- The AR0820AT is a 2.1 μm pixel size CIS fabricated using stacked-die architecture and a red/clear/clear/blue (RCCB) pattern color filter array (CFA). Other CFA options such as RGB and RCCC are also available [1].
- The HDR is achieved using DR-Pix™ technology. A capacitor connected to the floating diffusion (FD) node enables dual conversion gain (DCG), providing good image quality in high and low light conditions.
- The AR0820AT also offers 2 x 2 in-pixel binning mode and color binning mode [1].
- The AR0820AT CIS die is stacked on the image signal processor (ISP) die and uses hybrid bonding (direct bond interconnect (DBI)) to electrically connect the CIS die to the ISP die.
- The AR0820AT CIS die uses a composite material grid (CMG) pixel aperture/light shield comprising an oxide layer over the tungsten (W) grid to increase the thickness of the grid.

Note: In this report, the descriptions “horizontal” and vertical are used to mean a direction parallel to row select lines and to column out lines, respectively.

Device Summary

Device Summary – CIS

Manufacturer	ON Semiconductor
Foundry	TSMC
Part number	AR0820AT
Type	Stacked BI CIS
Active Si thickness	2.9 μm
Die size, measured from the die edge	9.76 mm $\times$ 6.53 mm (63.7 mm ²)
Die size, measured from the die seal	9.70 mm $\times$ 6.47 mm (62.8 mm ²)
Process type	Stacked BI CMOS imager
Number of metal layers (CIS)	4 Cu pixel interconnect + 1 Cu hybrid bond pad + back W shield/grid + back Al bond pad
Number of poly layers (CIS)	1
Contacted logic gate pitch (CIS)	–
Minimum metal pitch logic (CIS)	–
Minimum metal pitch pixel array (CIS)	250 nm
Process generation (CIS)	90 nm
Features measured to determine process generation	Minimum metal pitch

Device Summary – ISP

Foundry	TSMC
Number, type of metals	5 Cu + 1 Cu hybrid bond pad
Number of poly layers	1
Contacted logic gate pitch	260 nm
Minimum metal pitch logic	200 nm
Process generation	65 nm
Features measured to determine process generation	Logic contacted gate pitch and minimum metal pitch

Salient Features

General ISP

- Manufactured by TSMC in a 65 nm CMOS process
- The logic gate length is 68 nm
 - Contacted gate pitch of 260 nm
 - 92 nm thick polysilicon gate
 - Polysilicon gate and source/drain (S/D) regions use nickel platinum (NiPt) silicide
 - The gate dielectric comprises a 2.8 nm nitrided oxide
- Minimum metal pitch of 200 nm
- Five Cu interconnect layers, plus one Cu hybrid bond metal

Salient Features

General CIS

- Manufactured by TSMC in a 90 nm CMOS imager process
- 2.1 μm pixel pitch with gapless on-chip microlens array with silicon oxide (SiO) coating
 - Microlens radius of curvature is 1.8 μm
 - RCCB patterned CFA
 - CMG structure with embedded (buried) CFA
- 2.9 μm thick active Si
- 1.9 μm thick optical stack
- The periphery region uses four Cu metal interconnect layers, non-silicided contacts, one Cu DBI layer, one back CMG/shield, and shallow trench isolation (STI).
- The periphery PMD comprises seven layers, including oxide (SiO), nitride (SiN), phosphosilicate glass (PSG/SiOP), and carbon-doped oxide (SiOC) layers.
- The pixel array uses four Cu metal interconnect layers, one back CMG, non-silicided transistors, partial back DTI (B-DTI) for pixel isolation, and STI for transistor isolation
 - Metal 1 through metal 4 are Cu damascene with tantalum (Ta) based liners
- The active pixel array and shielded pixel array PMD comprises nine layers, including oxide (SiO), nitride (SiN), SiOP, and SiOC layers, and two more layers than the periphery, an oxide pad 2, and contact etch stop layer (CESL) 2 SiN.
- Interlayer dielectric (ILD) 1 and ILD 2 have a similar structures, comprising SiCN, oxide, and SiOC layers. ILD 3 comprises SiCN, oxide, and nitride.
- The passivation comprises nitride and oxide layers.

Salient Features

General CIS

- Active hybrid bonding (DBI) arrays are used along the bottom and right of the pixel array.
 - Cu-Cu hybrid bonding is made between CIS metal 5 and ISP metal 6. The DBI has a circular shape with a diameter of 1.8 μm .
 - An active column out hybrid bonding array is used along the bottom of the die. The column DBI array comprises 18 rows and has a horizontal and vertical DBI pitch of 4.2 μm .
 - An active row select hybrid bonding array is used along the right side of the pixel array. The row DBI arrays likely comprise 28 columns and have a DBI pitch of 4.2 μm in the horizontal direction (vertical DBI pitch direction not analyzed).
- No dummy DBIs were observed.
- The oxide bonding is made between the CIS wafer bonding layer (WBL) 1 SiON and the ISP WBL 1 SiON. The SiON layers are plasma treated, increasing the number of OH groups at their surfaces. After the wafers are bonded together, during the post wafer bonding anneal, the OH bonds break, forming SiO bonds, and consequently a 4.2 nm thick interface bonding layer (IBL) oxide is created [2].

Salient Features

Pixel Array

- Four-shared pixel architecture (2×2 pixel configuration), with seven transistors per four pixels and a capacitor, yielding 1.75 transistors (1.75T) effective per pixel
- Single gate dielectric process
 - T1 to T4 transfer (XFER), T5 reset (RST), T6 source follower (SF) and T7 row select (ROW) transistor gate dielectrics are 5.9 nm thick nitrided oxide
- Non-silicided pixel transistors
- N⁺ floating diffusion (FD) is 0.30 μm thick
- N⁺ S/D regions are 0.14 μm thick
- N-type photocathode is 2.7 μm thick
- P-pinning layer is approximately 0.12 nm thick
- Shielded (optical black) pixels are used at the bottom and right of the pixel array
 - Shielded pixels are separated from the active pixel array by an intermediary periphery region
 - 40 rows of shielded pixels at the bottom
 - 119 rows of shielded pixels at the right
- Edge pixels are shifted toward the array center
 - At the left, the grid and CF are shifted by 130 nm and the on-chip lenses (OCLs) are shifted by 260 nm. The center of the OCL is approximately 8° off-center of the pixel.
 - At the right, the grid and CF are shifted by 110 nm and the OCLs are shifted by 240 nm. The center of the OCL is approximately 7° off-center of the pixel.

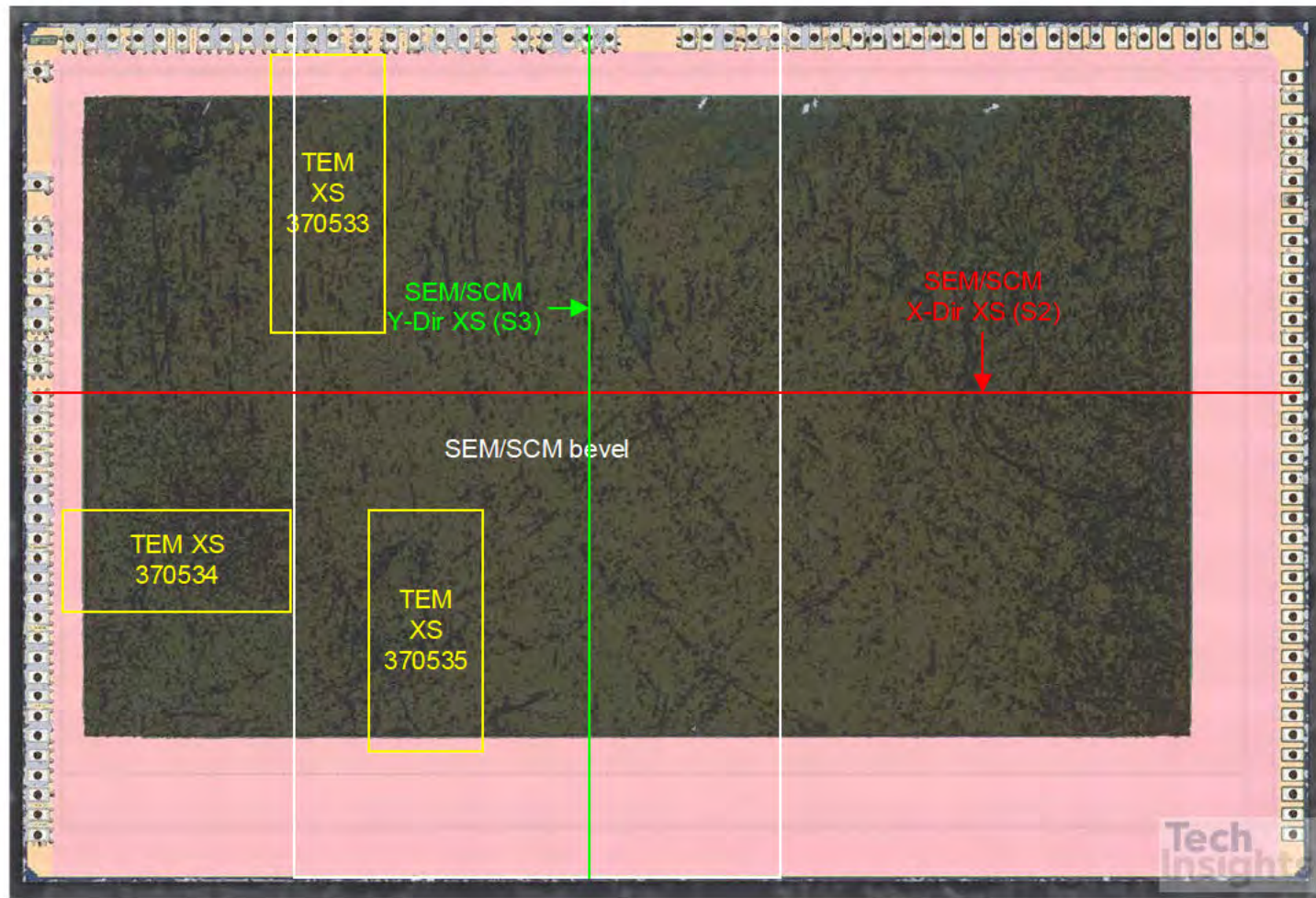
Salient Features

Pixel Array

- Edge pixels are shifted toward the array center
 - At the top, the grid and CF are shifted by 58 nm and the OCLs are shifted by 120 nm μm ; the center of the OCL is approximately 4° off-center of the pixel.
 - At the bottom, the grid and CF are shifted by 74 nm and the OCLs are shifted by 170 nm; the center of the OCL is approximately 6° off-center of the pixel.
- The back side high-k dielectrics (HKD)/antireflective (AR) layers used for surface passivation comprise three layers: a 4.7 nm thick aluminum oxide (AlO), a 4.3 nm thick hafnium oxide (HfO), and a 47 nm thick tantalum oxide (TaO).
- The CMG/light shield is 590 nm thick and comprises a 160 nm thick W layer with a 28 nm thick titanium nitride (TiN) barrier, and a 400 nm thick grid extension oxide.
- Partial depth B-DTI trenches are used for pixel-to-pixel isolation in the active pixel array and shielded pixel array.
 - The depth of the B-DTI trench varies from 1.6 μm at the grid edge intersection to 1.8 μm at the grid vertices (crossing points).
 - The B-DTI average width is about 0.18 μm , yielding an aspect ratio of 8.9 (1.6 μm /0.18 μm).
 - The B-DTI trench is lined with the HKD/AR layers (AlO/HfO/TaO) and filled with oxide.
 - At the center of the B-DTI, a void is formed as the oxide fill layer, as it pinches near the mouth during deposition.

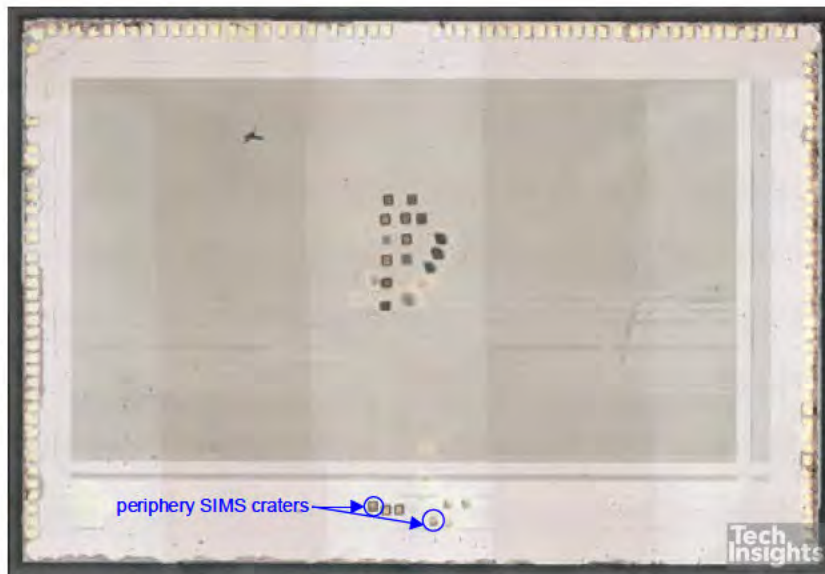
Sample Locations

Sample Locations – SEM, SCM, and TEM Analyses



.png

Sample Locations – SIMS Analyses



SIMS_Analysis_Sample_1.png



SIMS_Analysis_Sample_2.png

Locations of SIMS Craters Pixel Array

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Camera Module and CIS Die

Package Photographs



LI-AR0820_-GMSL2-060H_Front-Cam_Pkg_Top_370468.png

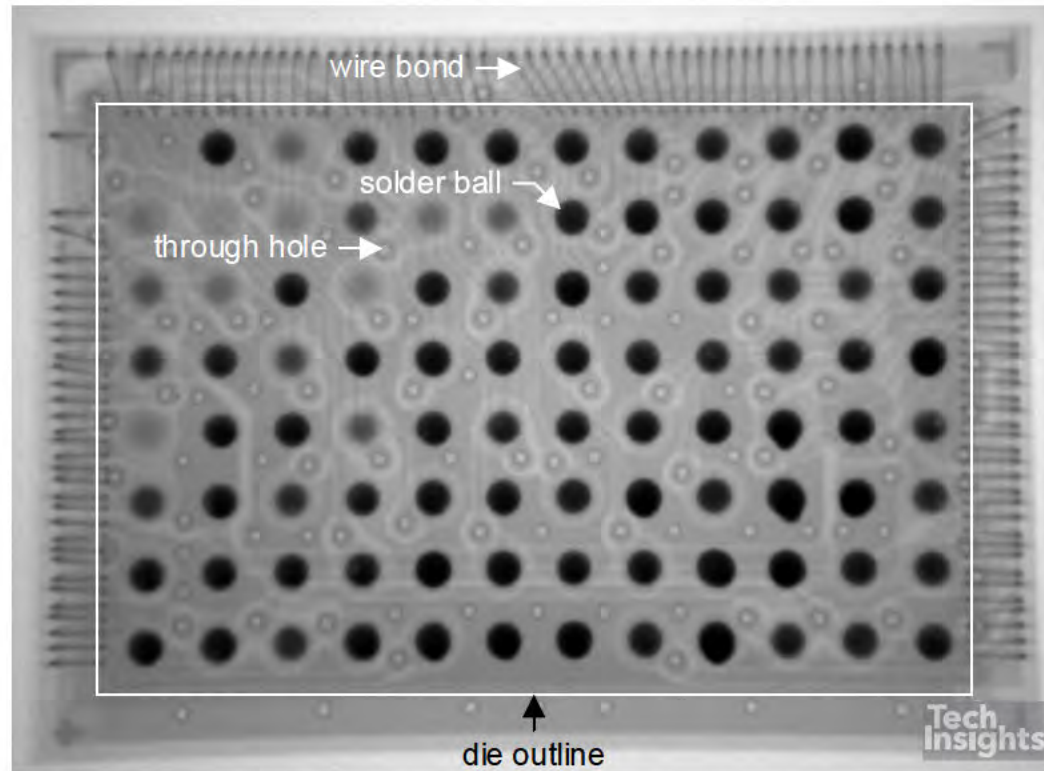
Top



LI-AR0820_-GMSL2-060H_Front-Cam_Pkg_Bot_370468.png

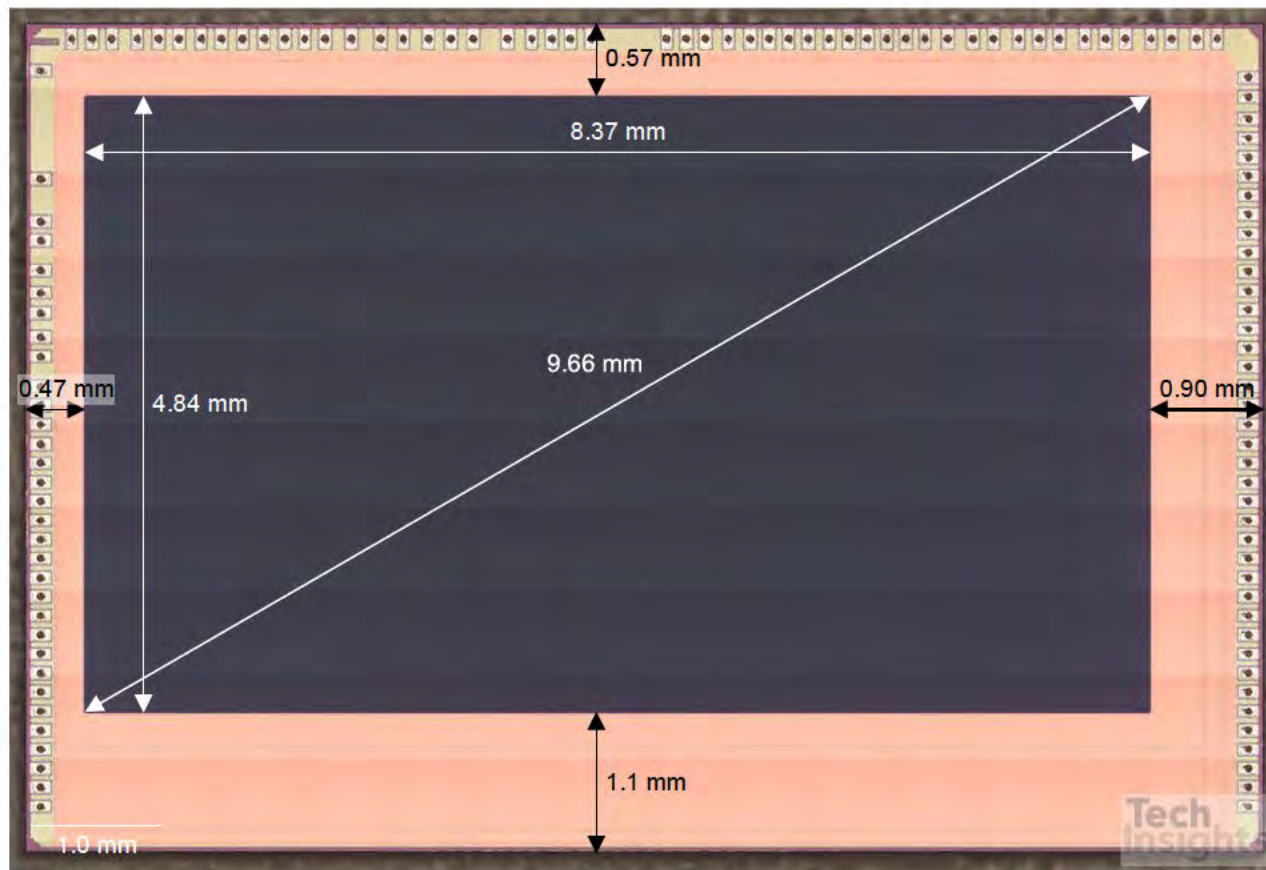
Bottom

Package X-Ray



LI-AR0820-GMSL2-060H_Front-Cam_Xray_Top_370465.png

Annotated CIS Die Photograph



LI-AR0820-GMSL2_Front-Cam_AR0820_CIS_357602_Oriented.png

CIS Die Markings

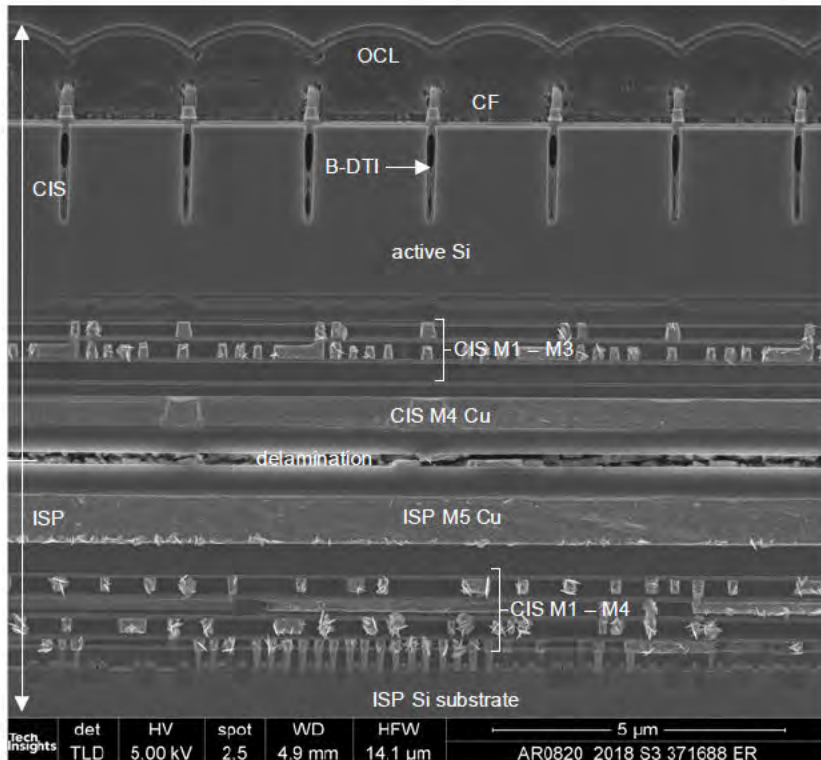


LI-AR0820-GMSL2_060H_Front-Cam_AR0820_2018_CIS_371697_DieMrk.png

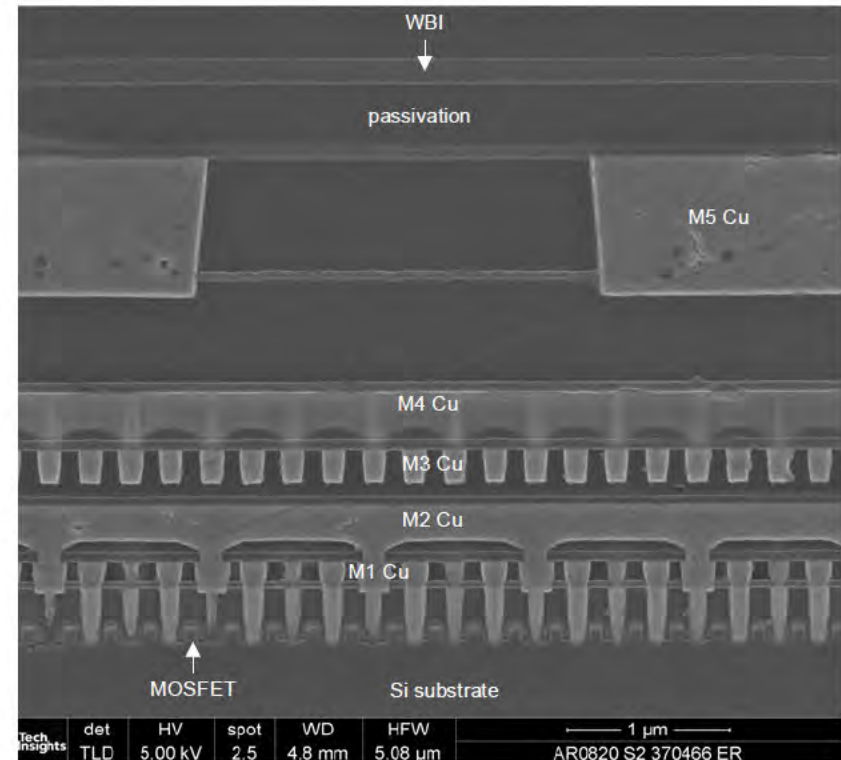
ISP General Structure

ISP General Structure

- SEM cross section images of ISP general structure
- The ISP is fabricated using five Cu metal interconnect layers and one Cu (metal 6) for hybrid bonding (DBI)

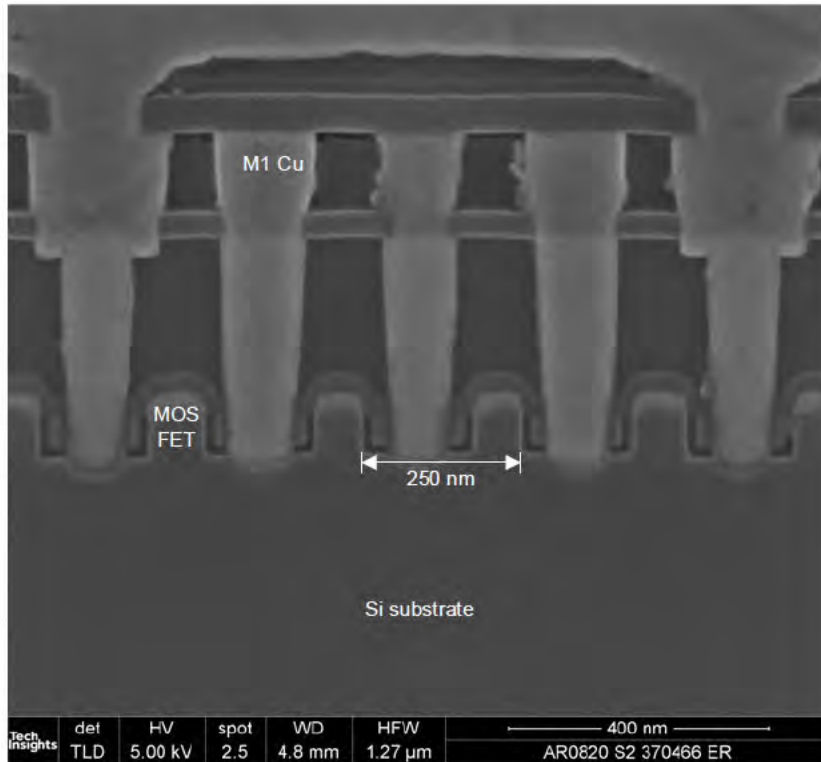


ISP/CIS Stack General Structure



ISP General Structure

ISP Minimum Contacted Gate Pitch

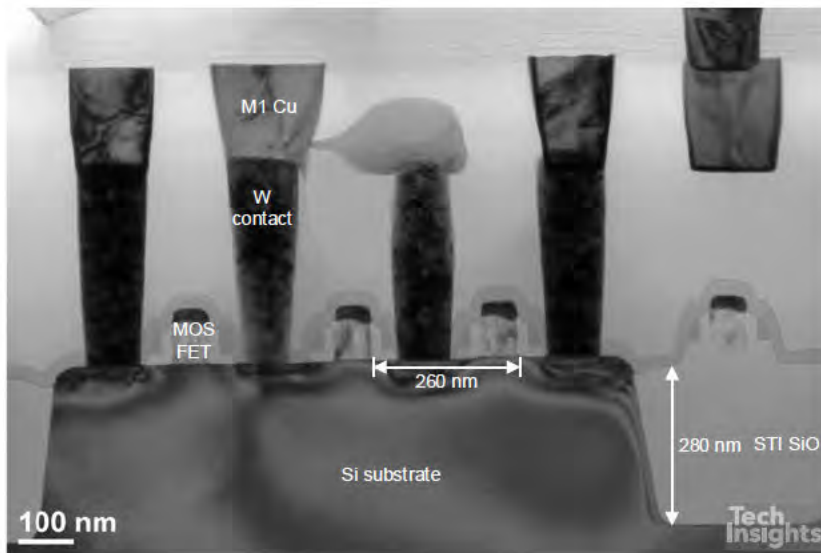


- The minimum contacted gate pitch of 250 nm was observed in the 6T SRAM.
- The minimum contacted gate pitch observed in the logic region was 260 nm.
- The ISP is manufactured by TSMC using a 65 nm CMOS process generation

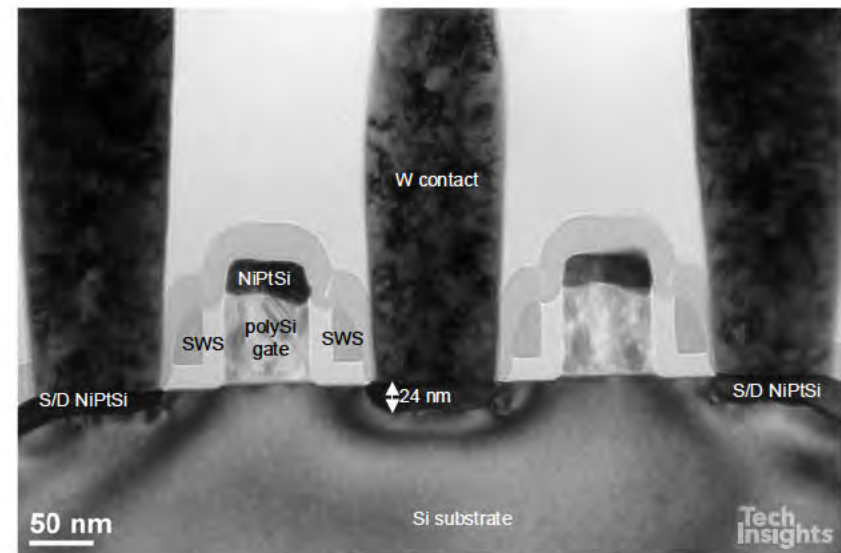
SRAM Contacted Gate Pitch

ISP Logic Transistor

- TEM cross section images of the logic transistors
- The logic transistor CGP is 260 nm.
- The S/D regions have a 24 nm NiPt silicide.



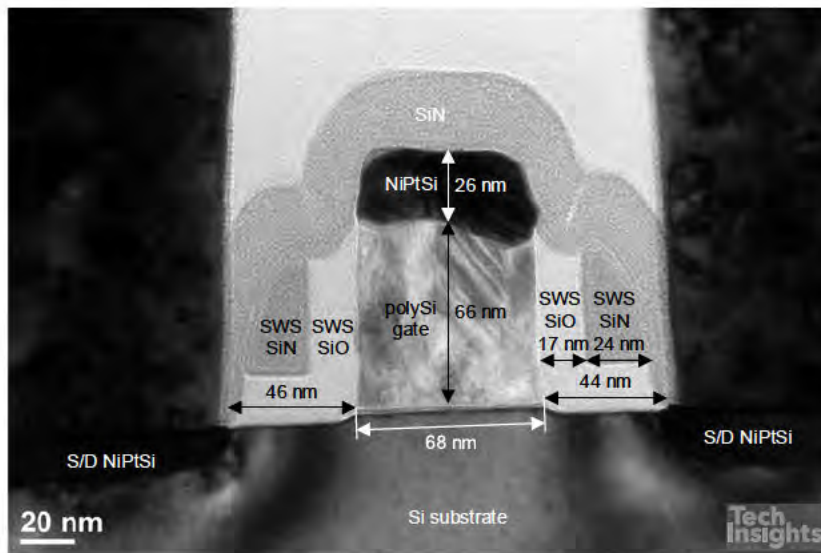
ISP Logic Transistor Overview



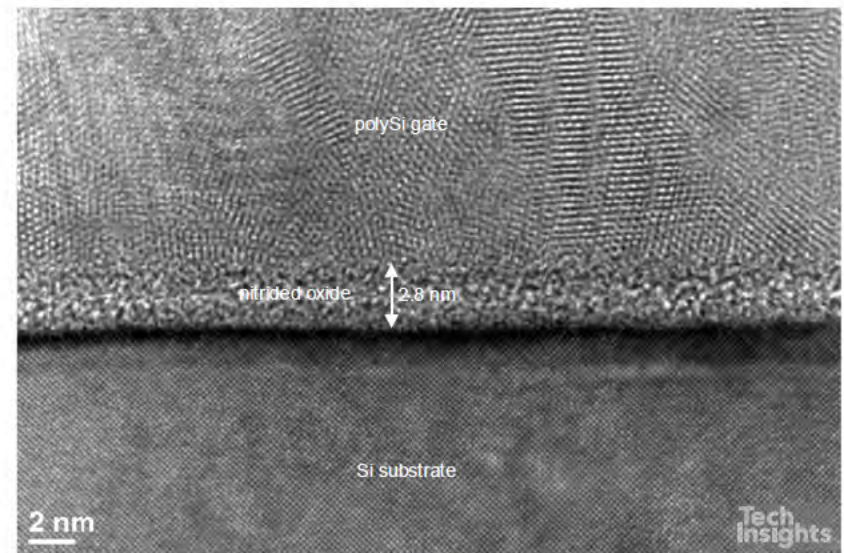
ISP Logic Transistor Detail

ISP Logic Transistor Detail

- TEM cross section detail images of the logic transistors and gate dielectric
- The length of the logic transistor is 68 nm. The gate comprises a 66 nm thick polysilicon and a 26 nm thick NiPt silicide.
- The gate dielectric comprises a 2.8 nm nitrided oxide.

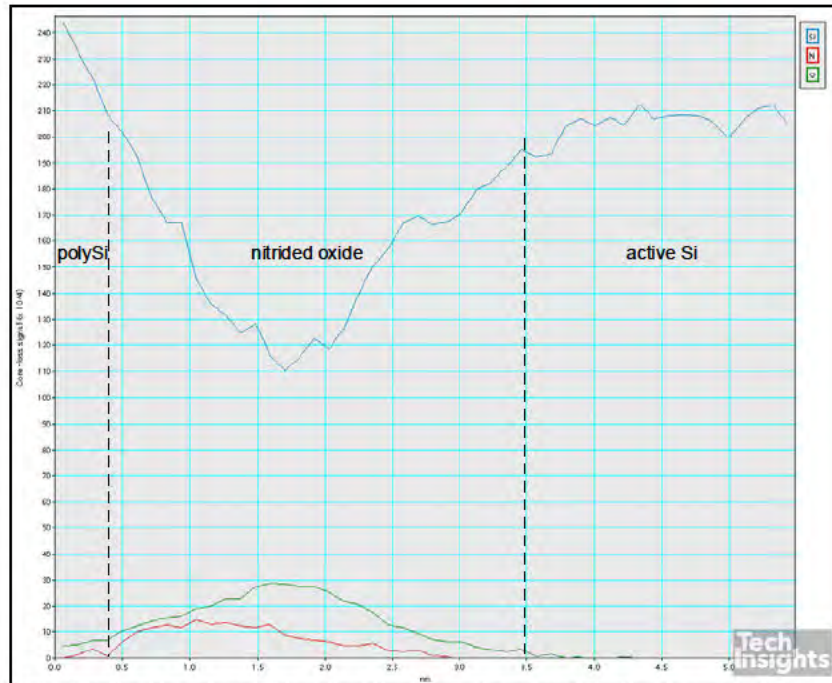


ISP Logic Transistor Detail



ISP Logic Transistor Gate Dielectric

ISP Logic Transistor Gate Dielectric



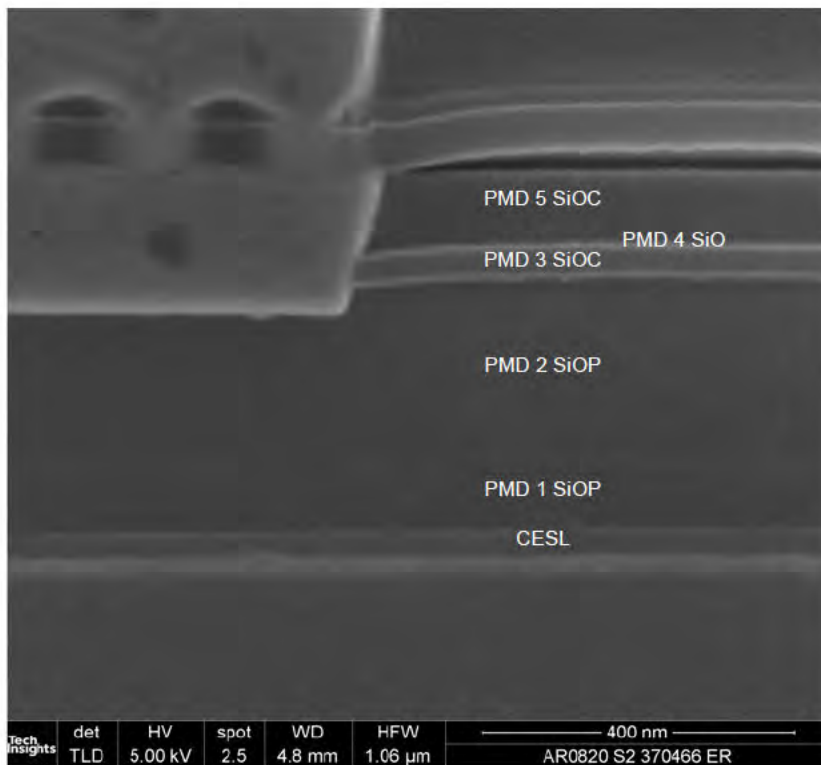
- TEM-EELS scan spectra of the ISP logic transistor gate dielectric
- The gate dielectric is a nitrided oxide.

GOX_15.25.48 Edge Profiles_370537T5_Gox_18.28.39 Edge Profiles_364918.png

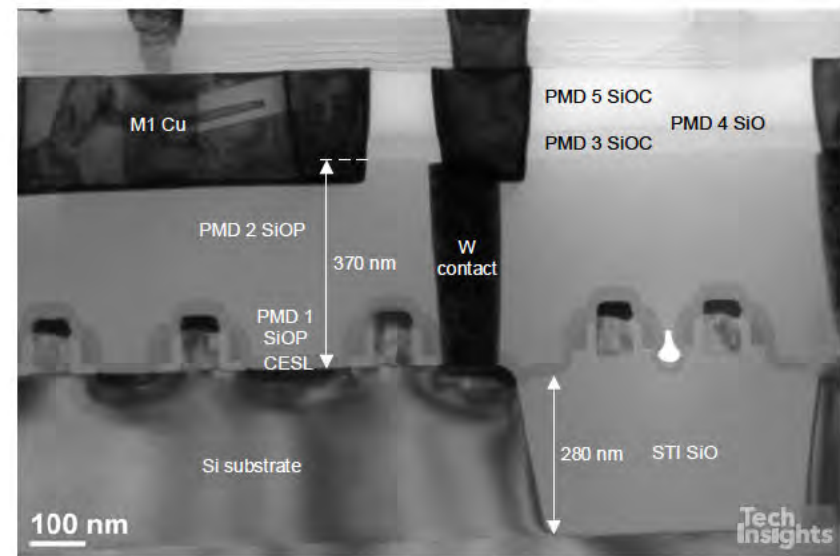
ISP Logic Transistor Gate Dielectric – TEM-EELS

ISP PMD

- The PMD comprises a CESL nitride, and a 370 nm thick PMD stack of SiOP PMD 1 and PMD 2, a SiOC PMD 3, a SiO PMD 4, and a SiOC PMD 5 layers.



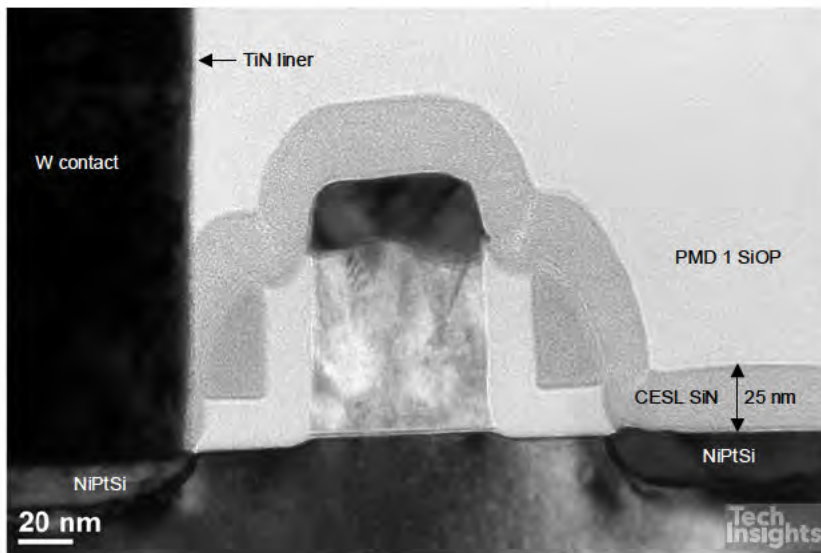
ISP PMD – SEM



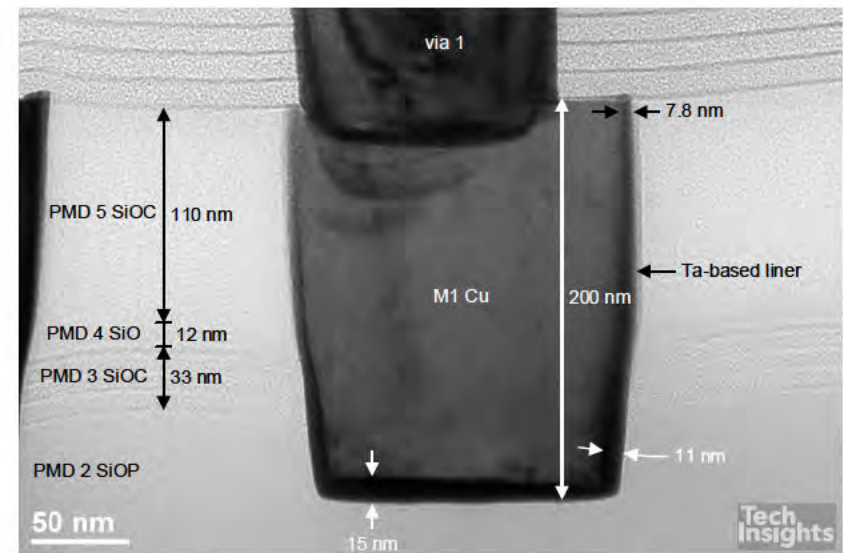
ISP Logic Transistor Gate Dielectric

ISP PMD and Metal 1

- The CESL nitride is 25 nm thick, PMD 3 is a 33 nm thick SiOC, PMD 4 is a 12 nm thick SiO, and PMD 5 is a 110 nm thick SiOC.
- Metal 1 is a 200 nm thick single damascene Cu with a Ta-based liner.
- The metal 1 Ta-based liner thickness on the sidewall varies from 7.8 nm to 11 nm, and on the bottom it is 15 nm.



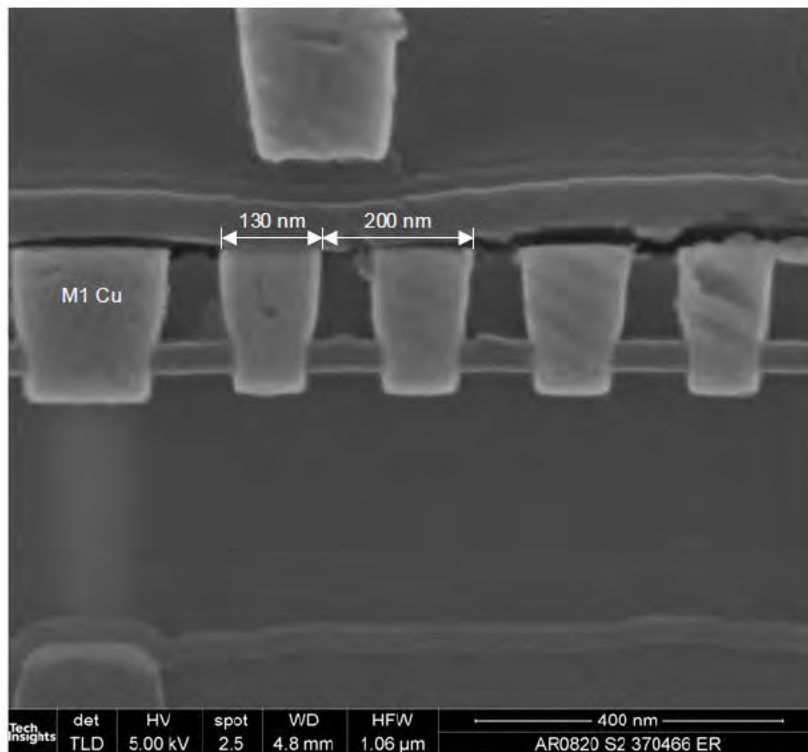
CESL – SEM



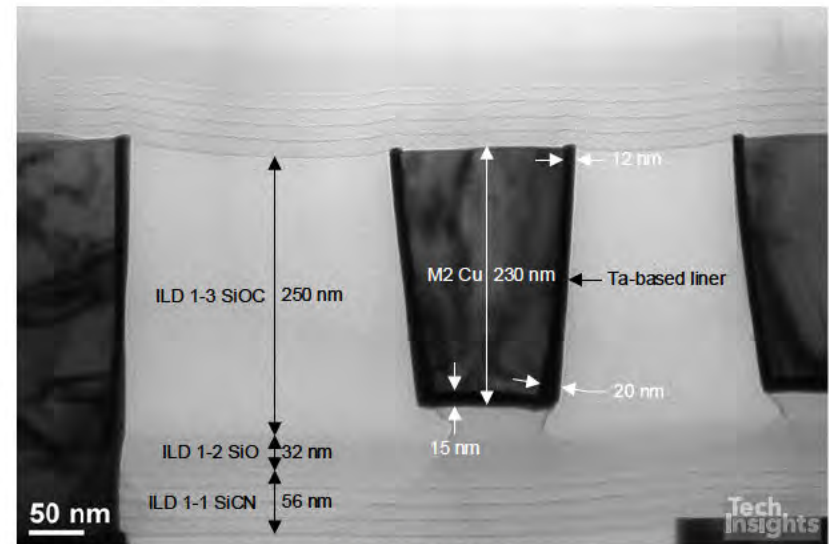
Top PMD Layers and Metal 1 – TEM

ISP Minimum Metal Pitch and ILD 1

- The minimum metal pitch observed is 200 nm.
- ILD 1 comprises a 56 nm thick ILD 1-1 SiCN, a 32 nm thick ILD 1-2 oxide, and a 250 nm thick ILD 1-3 SiOC.
- Metal 2 is 230 nm thick dual damascene Cu with Ta-based liner
- The metal 2 Ta-based liner thickness on the sidewall varies from 12 nm to 20 nm, and on the bottom it is 15 nm.



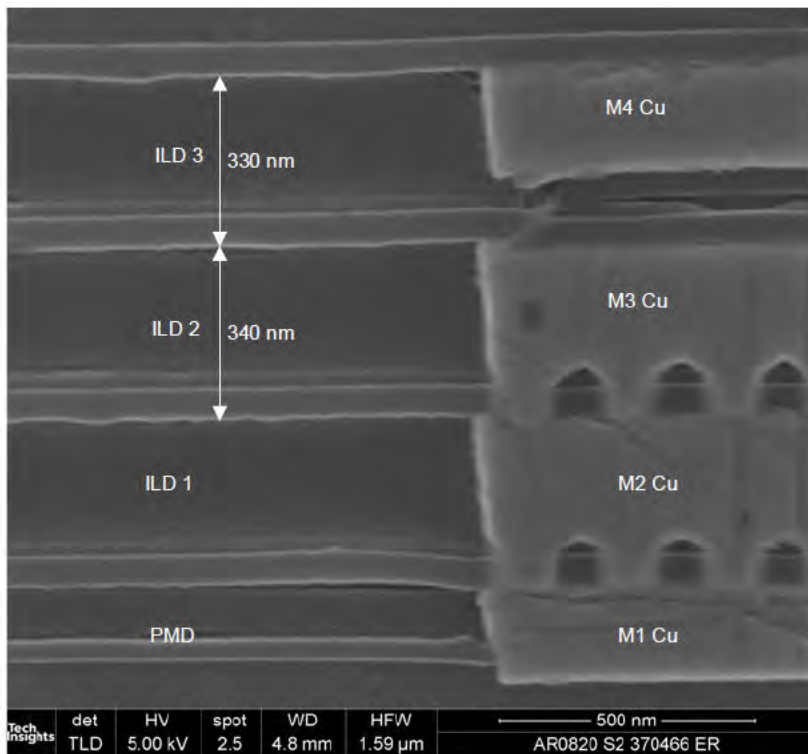
Minimum Metal Pitch – SEM



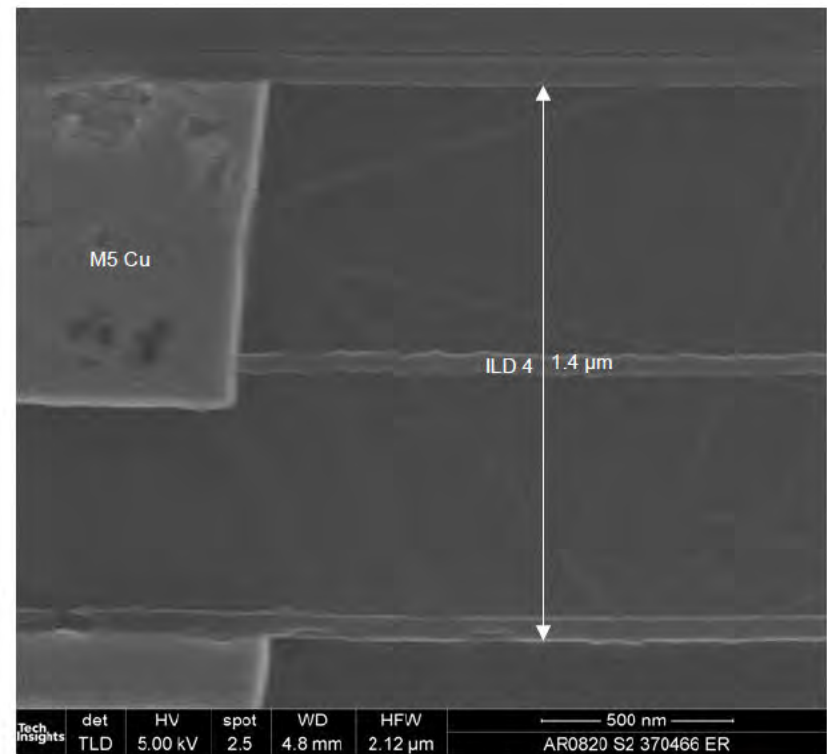
ILD 1 – TEM

ISP ILD and Metal Layers

- The ILD 2, ILD 3, and ILD 4 layers were not analyzed.
- ILD 2 and ILD 3 are 340 nm and 330 nm thick, respectively, with likely the same composition as ILD 1.
- ILD 4 is 1.4 μm thick.

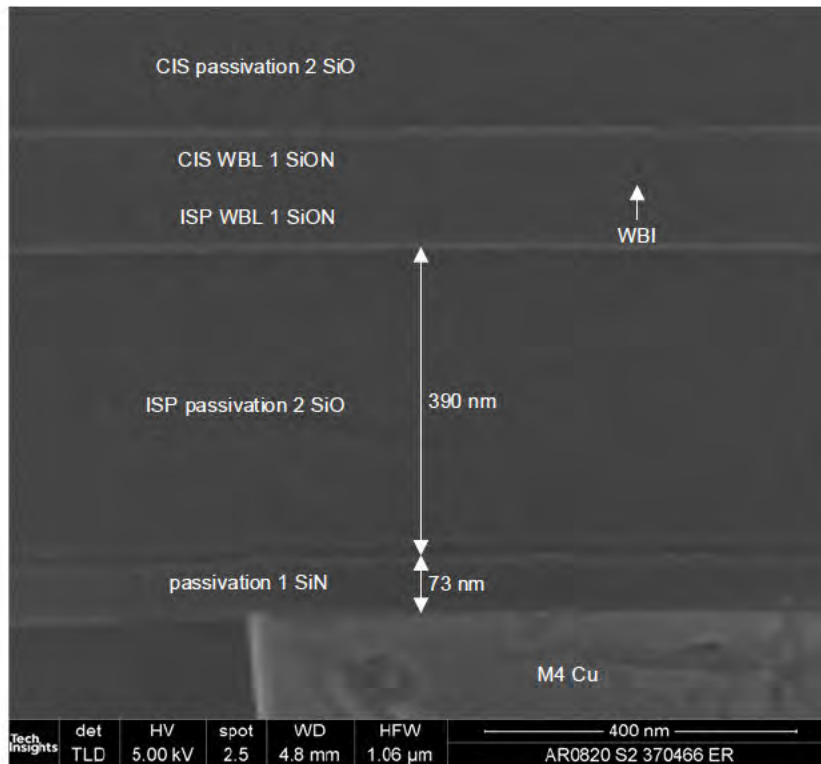


ILD 2 and ILD 3 – SEM



ILD 4 – SEM

ISP Passivation



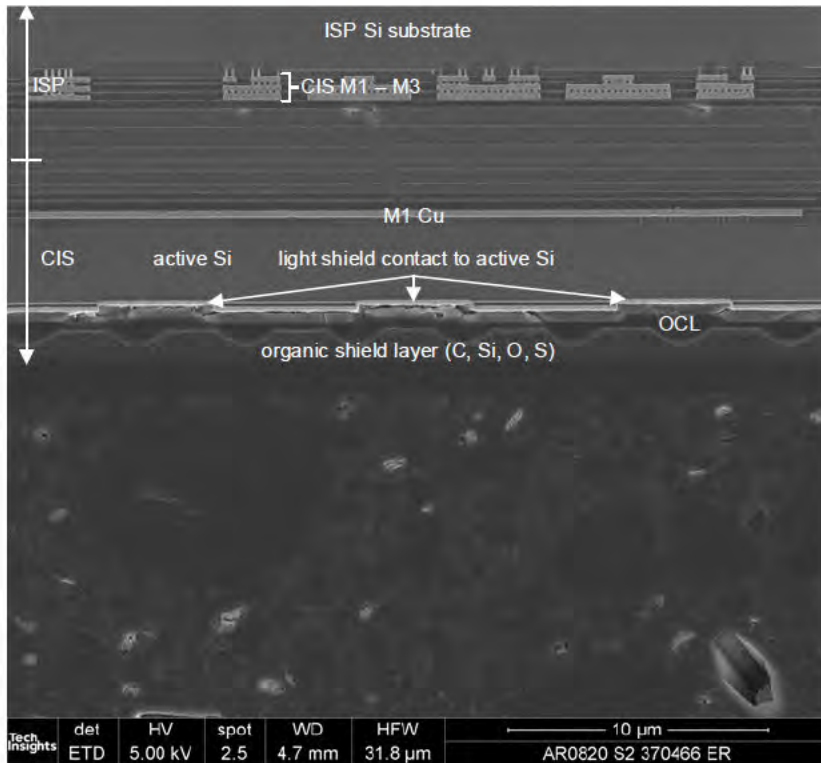
- The passivation comprises a 73 nm thick nitride and a 390 nm thick oxide.

Passivation – SEM

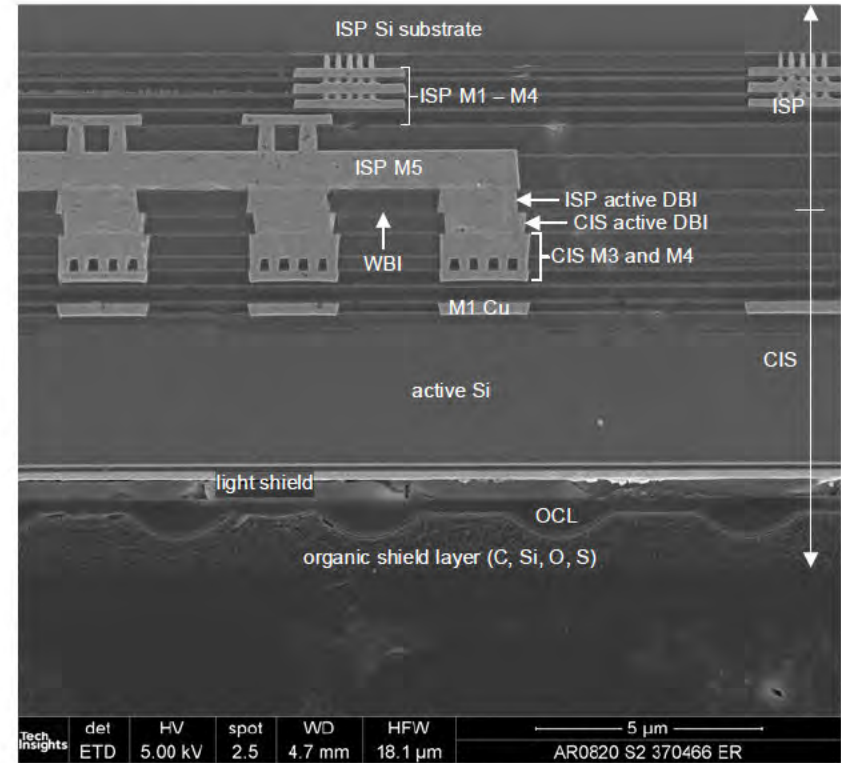
CIS General Structure

CIS General Structure – Periphery

- SEM cross section images showing the CIS general structure in the periphery region



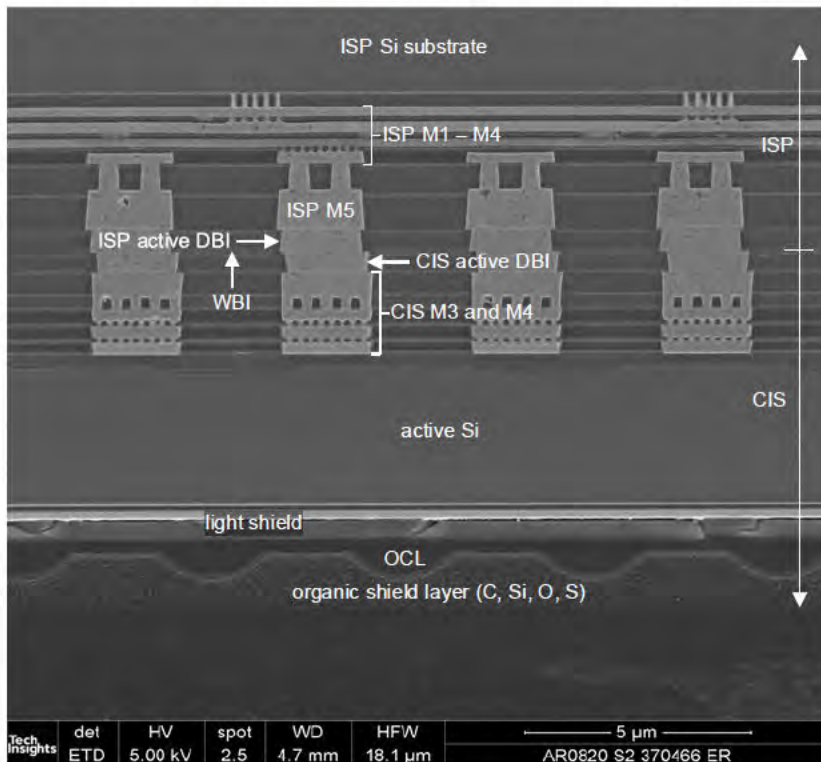
Shield Contact to Active Si



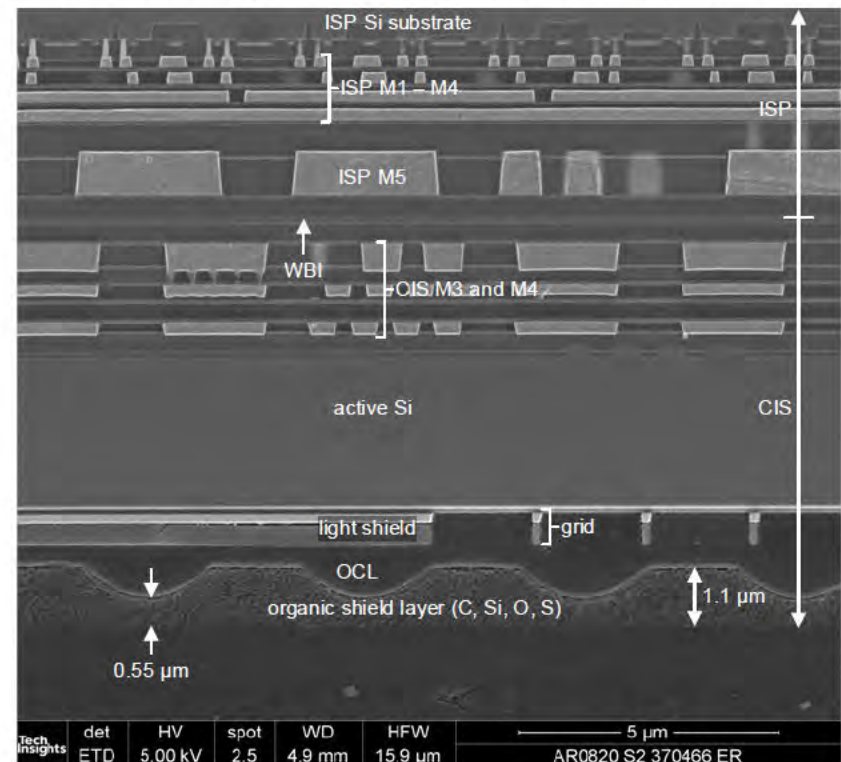
Column Out Active DBI

CIS General Structure – Periphery

- SEM cross section images showing the CIS general structure in the periphery region
- The periphery region is covered with an organic shield layer containing carbon (C), silicon (Si), oxygen (O), and sulfur (S).
- The light shield transitions to a grid in the peripheral region; usually, this happens at the start of the active pixels.



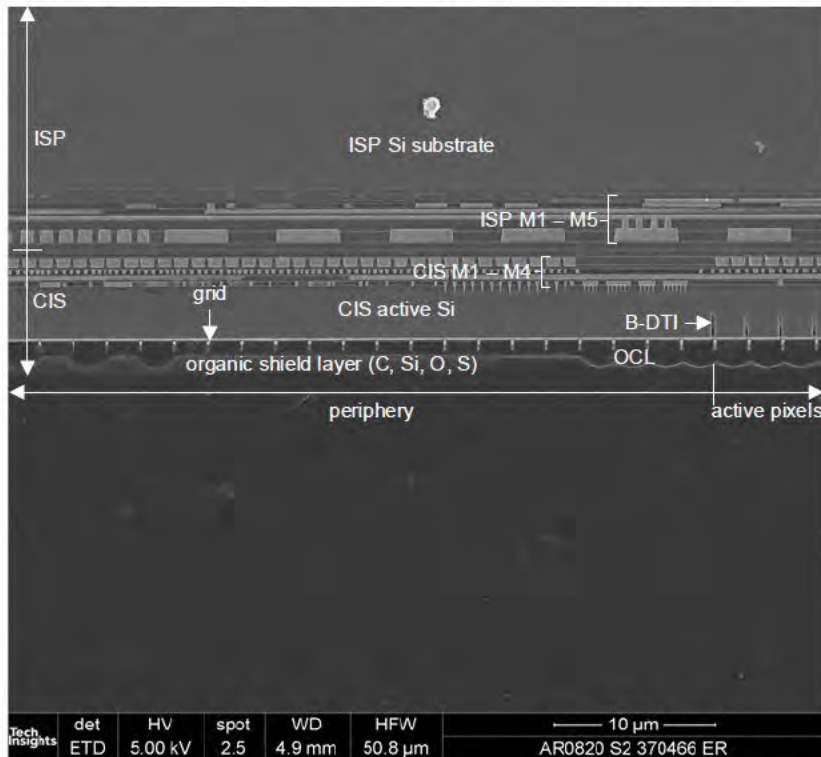
Column Out Active DBI



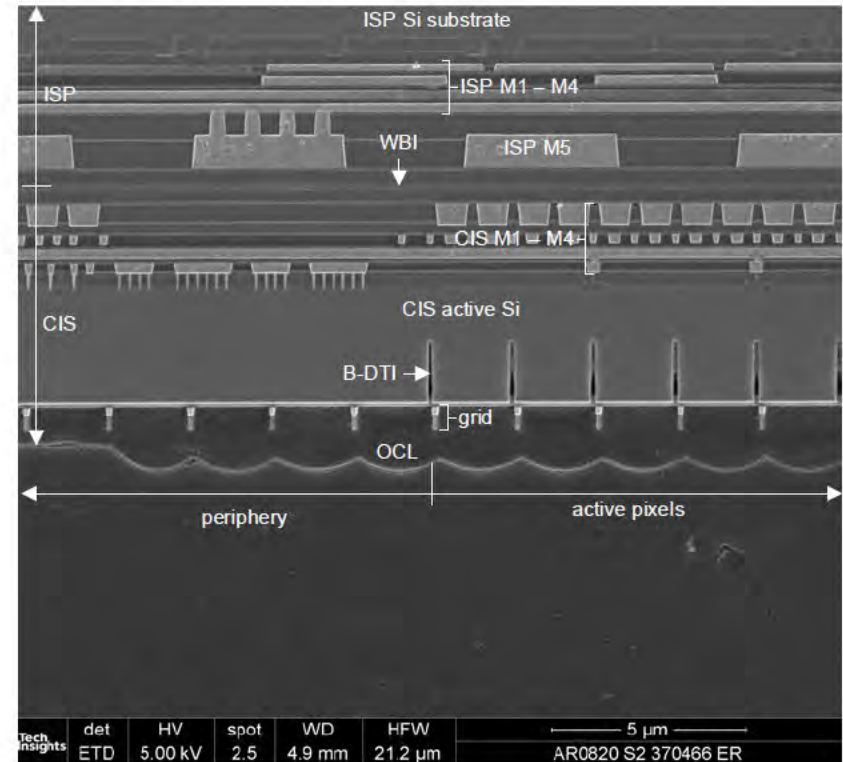
Start of the Grid

CIS General Structure – Transition from Periphery to Active Pixels

- SEM cross section overview and detail images showing the transition from periphery to active pixels at the left of the pixel array
- There are no shielded pixels at the left of the pixel array.
- The periphery has a wide region with the grid before the light shield starts.



Transition from Periphery to Active Pixels – Left

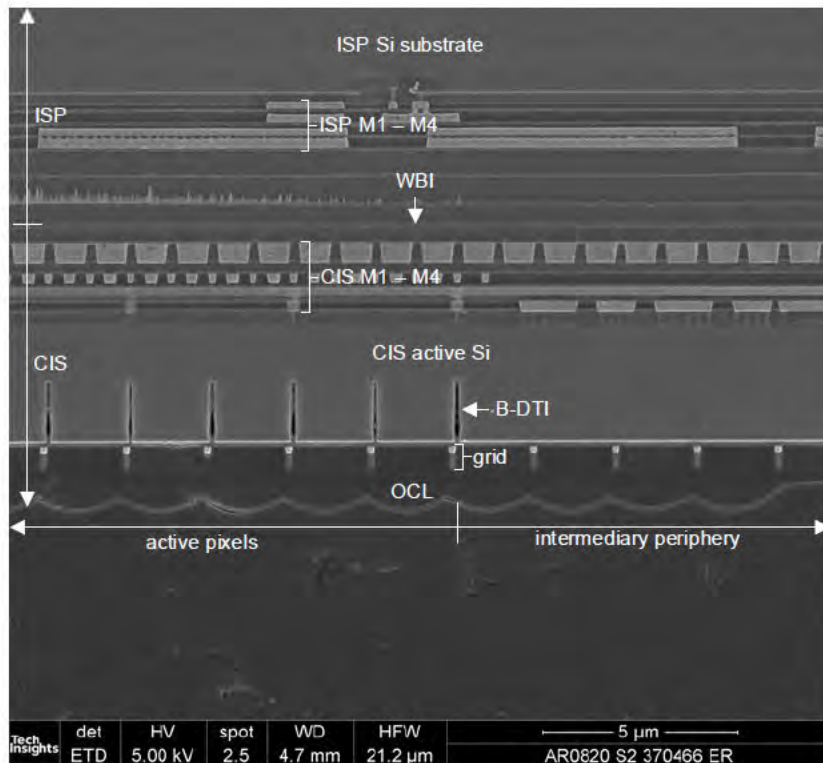


Transition from Periphery to Active Pixels – Left

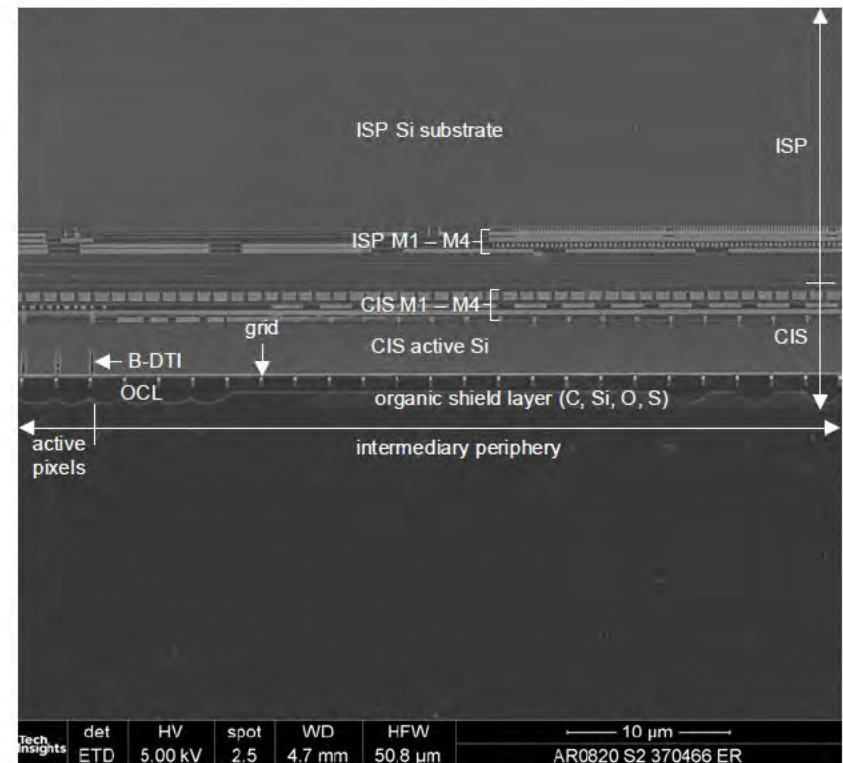
443_CIS_Periphery_PixelArray_Transition_6K_370466.png

CIS General Structure – Transition from Periphery to Active Pixels

- SEM cross section images showing the transition from the active pixel array to periphery at the right of the pixel array
- At the right of the pixel array, the active pixels transition to an intermediary periphery region.



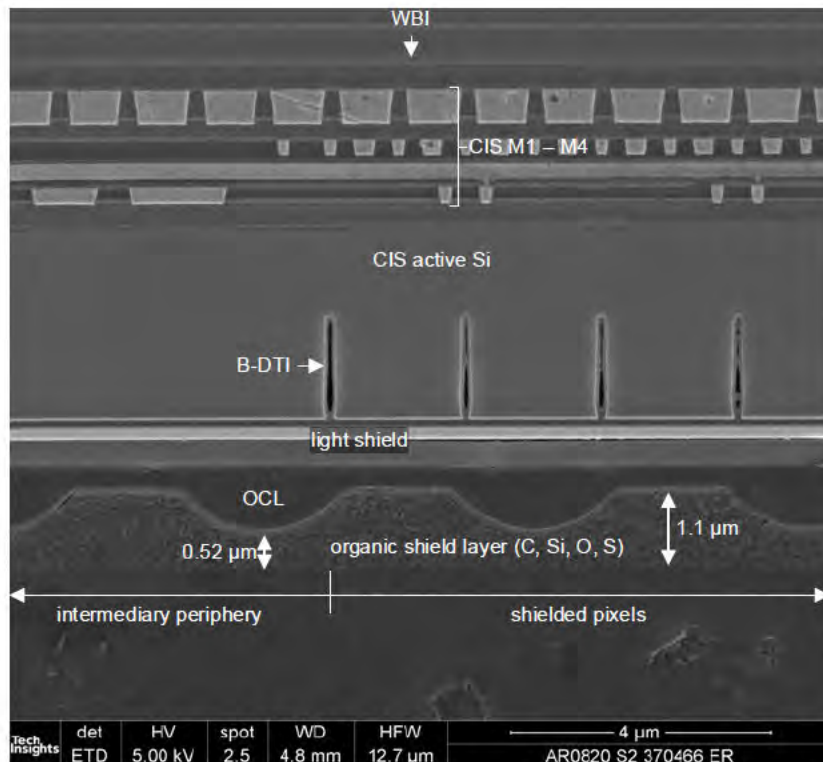
Transition from Active Pixels to Periphery – Right



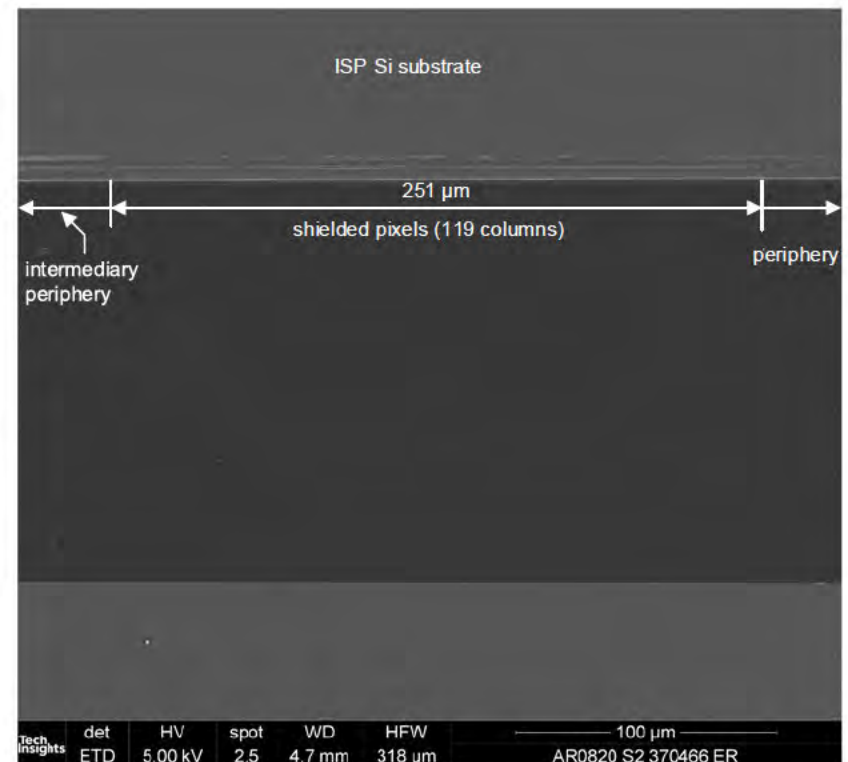
Transition from Active Pixels to Periphery – Right

CIS General Structure – Shielded Pixels

- SEM cross section images showing the transition from the intermediary periphery to shielded pixels at the right side
- The shielded pixel region at the right is 251 μm long, which is equivalent to 119 pixel columns.



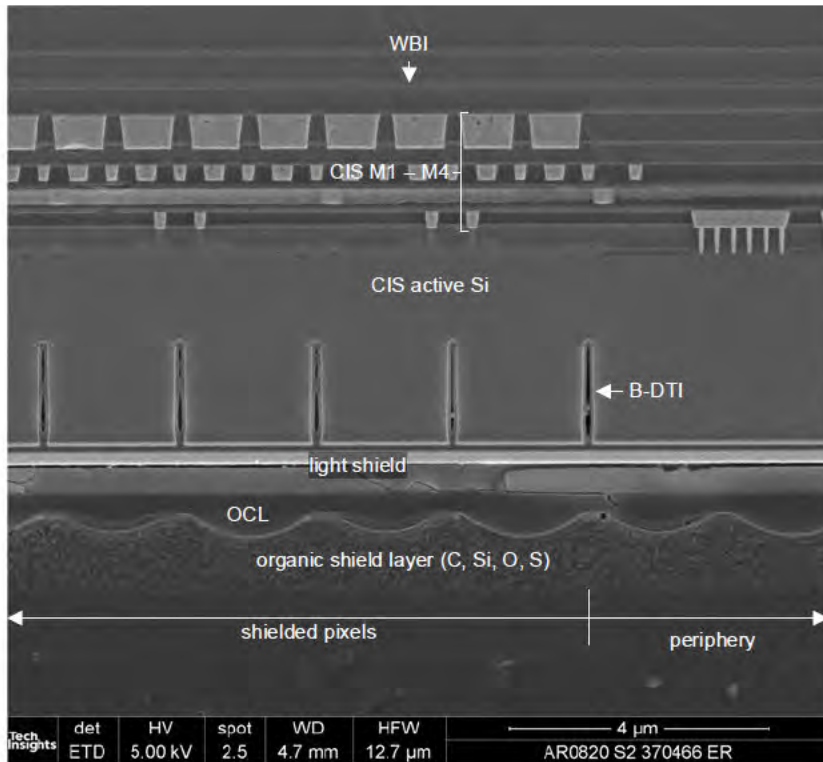
**Intermediary Periphery to Shielded Pixels
Transition – Right**



434_CIS_Periphery_Shielded_Test_Pixels_400x_370466.png

Shielded Pixels – Right

CIS General Structure – Transition from Shielded Pixels to Periphery

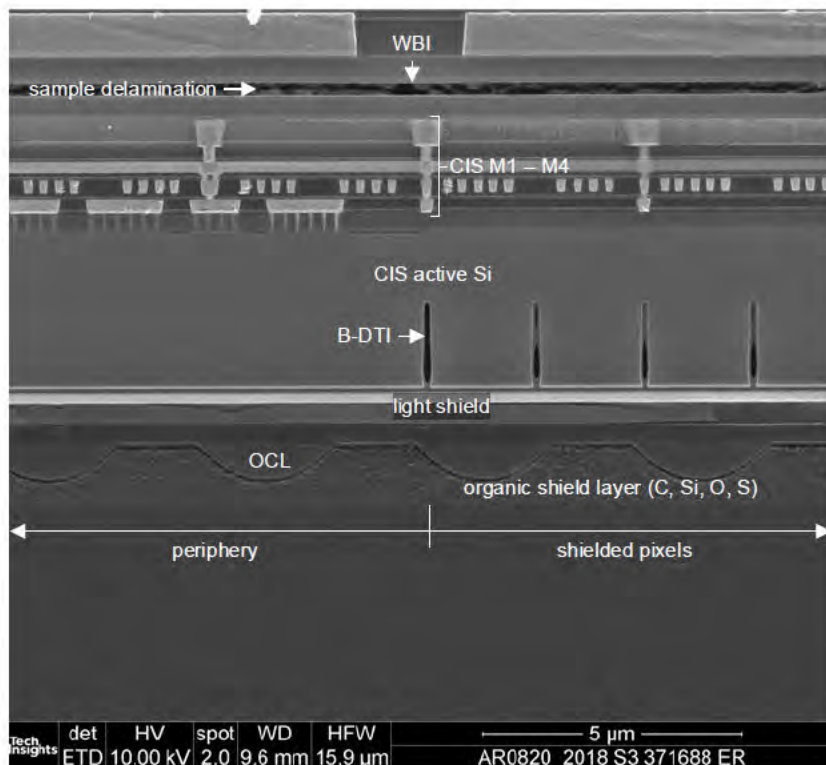


- SEM image showing the transition from shielded pixels to periphery at the right side

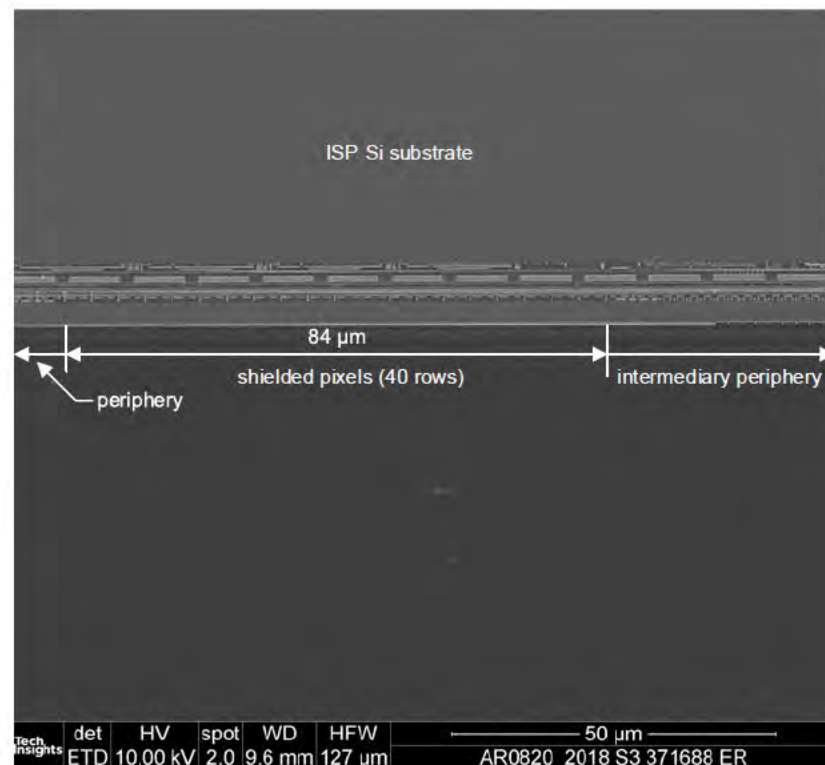
Shielded Pixels to Periphery Transition – Right

CIS General Structure – Transition from Periphery to Shielded Pixels

- SEM cross section images showing the transition from periphery to shielded pixels at the bottom of the pixel array
- The shielded pixel region at the bottom is 84 μm long, which is equivalent to 40 pixel rows.



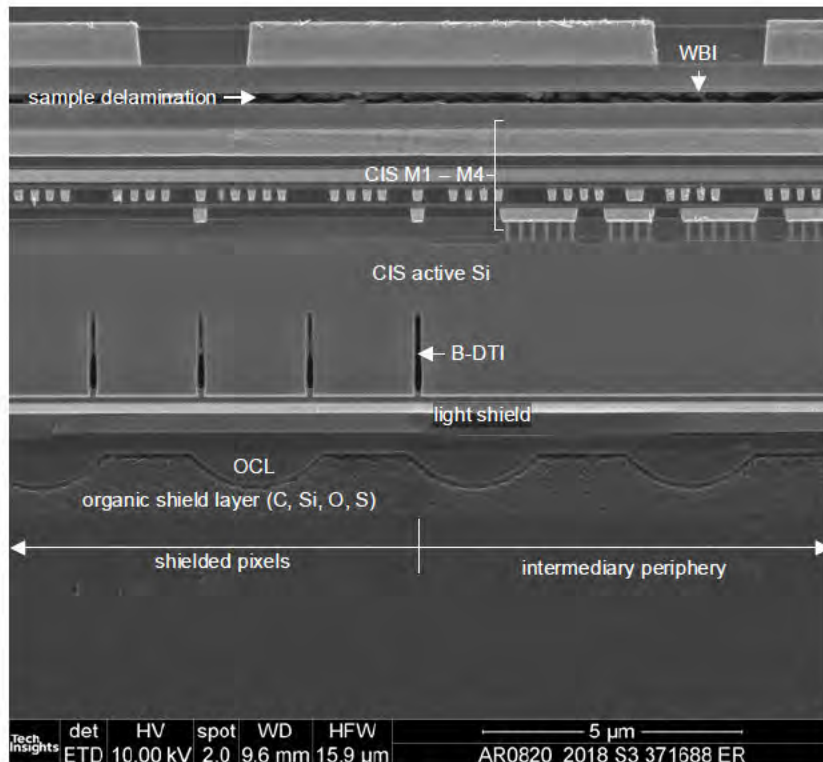
Transition from Periphery to Shielded Pixels – Bottom



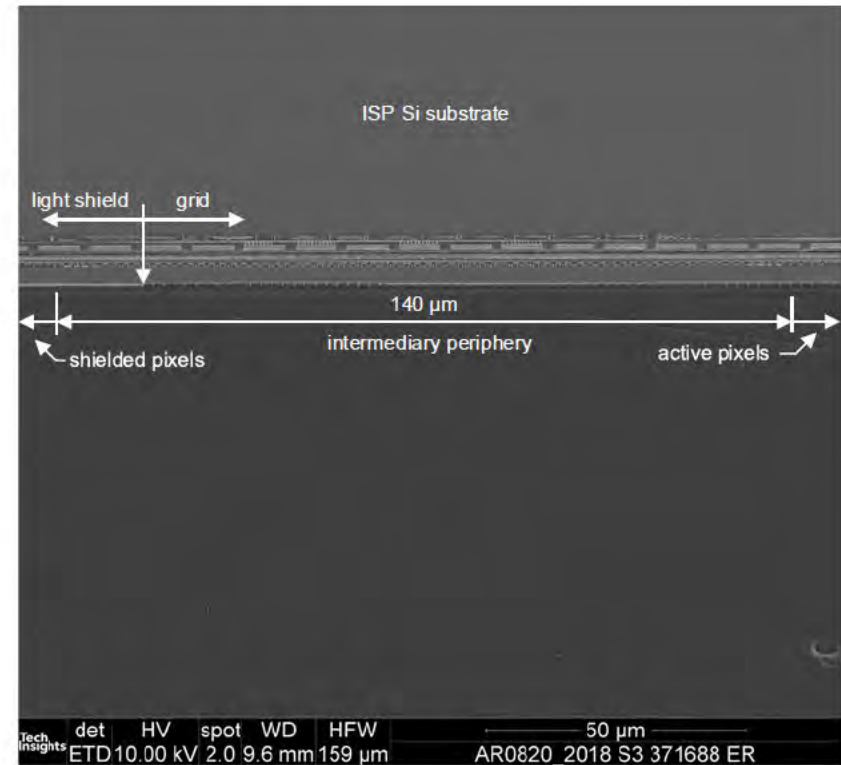
Shielded Pixels – Bottom

CIS General Structure – Intermediary Periphery Region

- SEM cross section images showing the transition from the shielded pixels to intermediary periphery at the bottom of the pixel array
- The intermediary periphery region between shielded pixels and active pixels is 140 μm long.



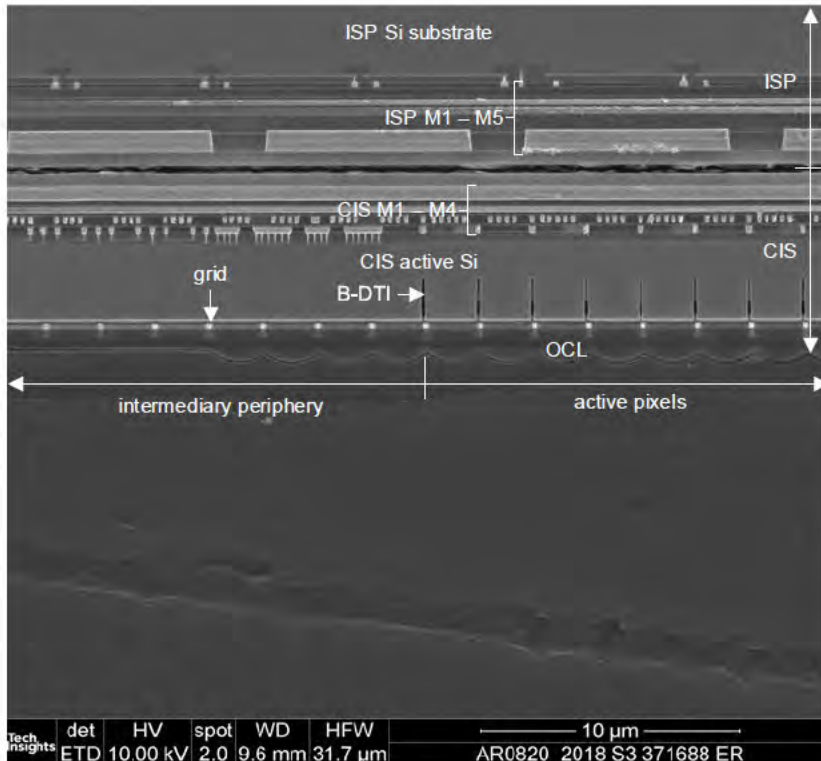
Transition from Shielded Pixels to Intermediary Periphery – Bottom



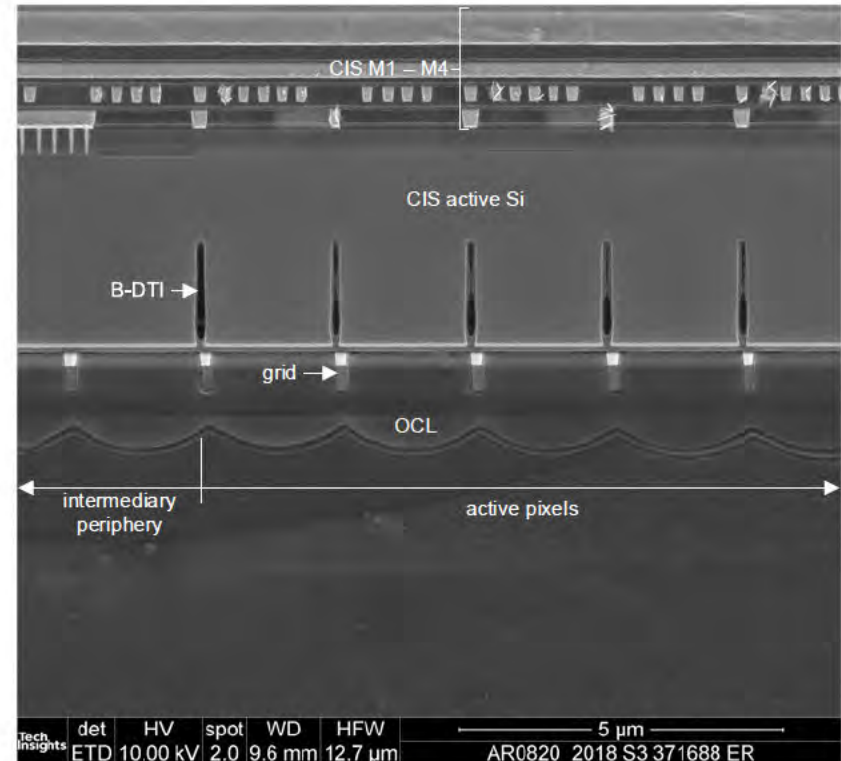
Intermediary Periphery – Bottom

CIS General Structure – Transition from Intermediary Periphery to Active Pixels

- SEM cross section overview and detail images showing the transition from the intermediary periphery to active pixels at the bottom



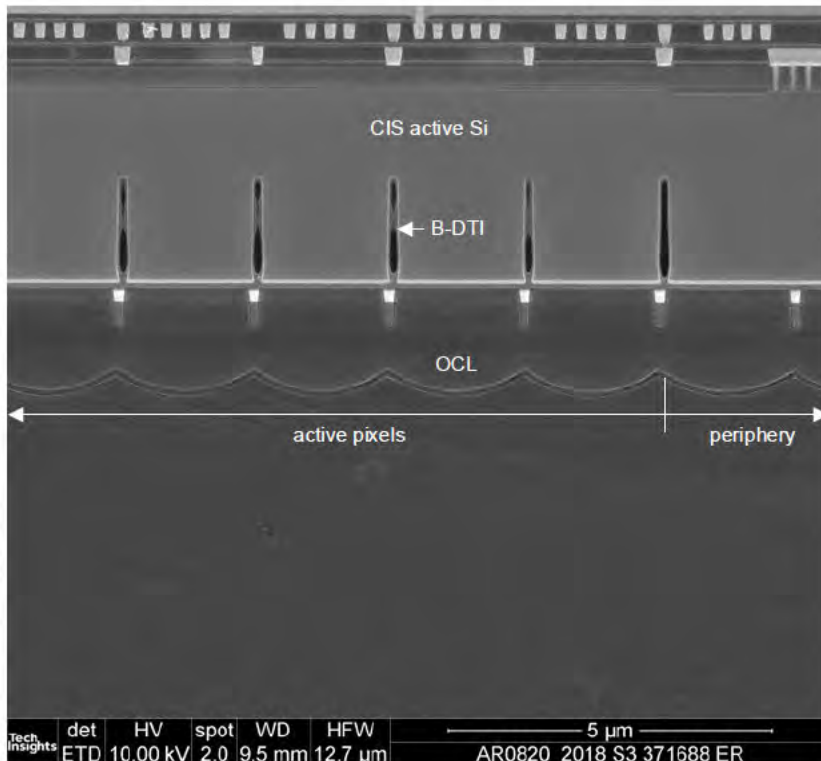
Intermediary Periphery to Active Pixels Transition Overview – Bottom



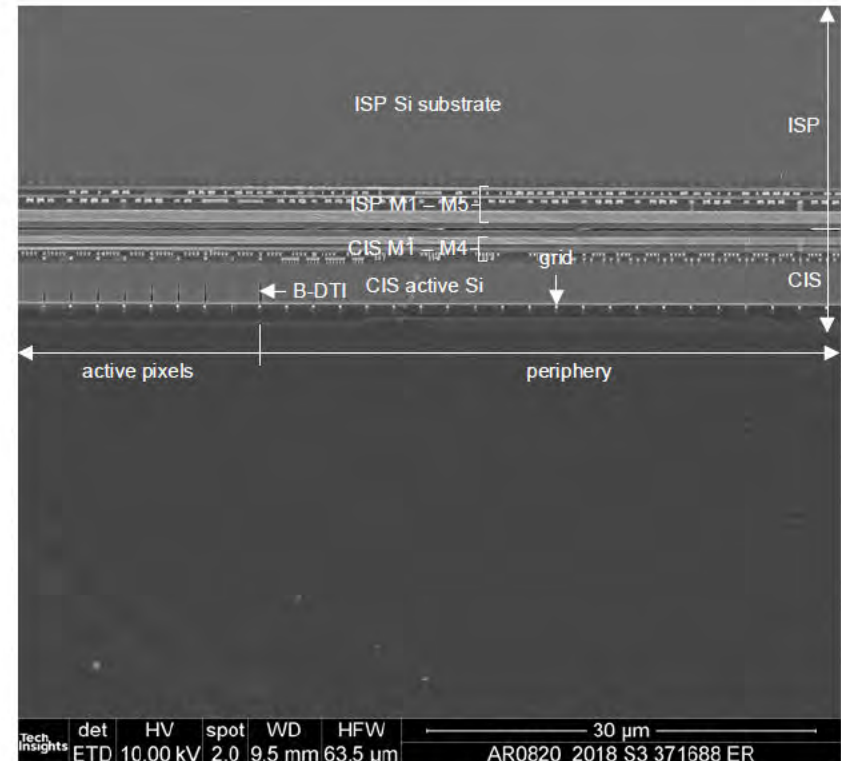
Intermediary Periphery to Active Pixels Transition Detail – Bottom

CIS General Structure – Transition from Periphery to Active Pixels

- SEM cross section overview and detail images showing the transition from the active pixel array to periphery at the top of the pixel array



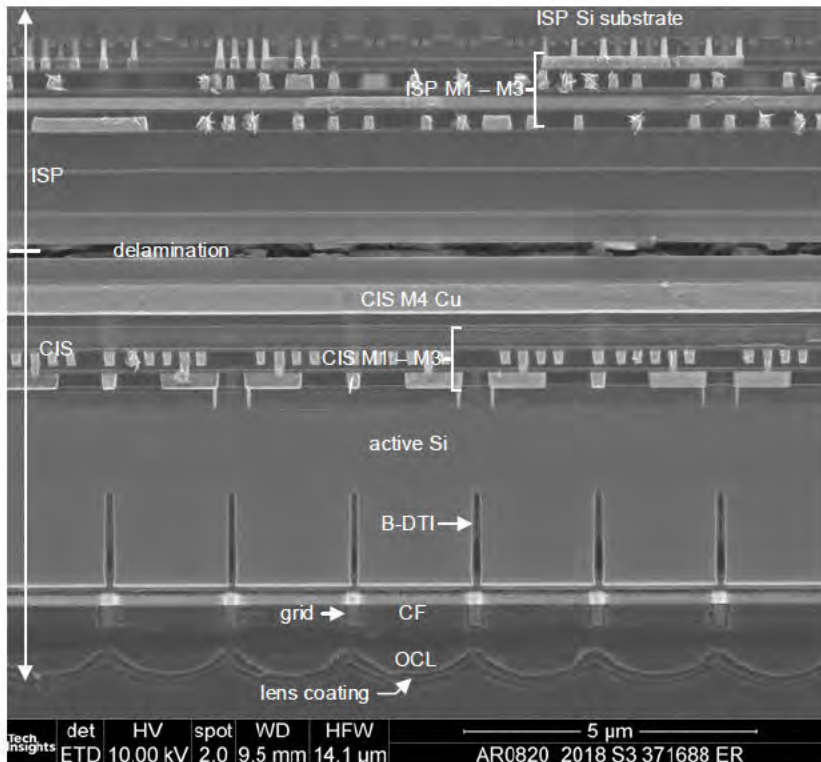
Active Pixels to Periphery Transition Detail – Top



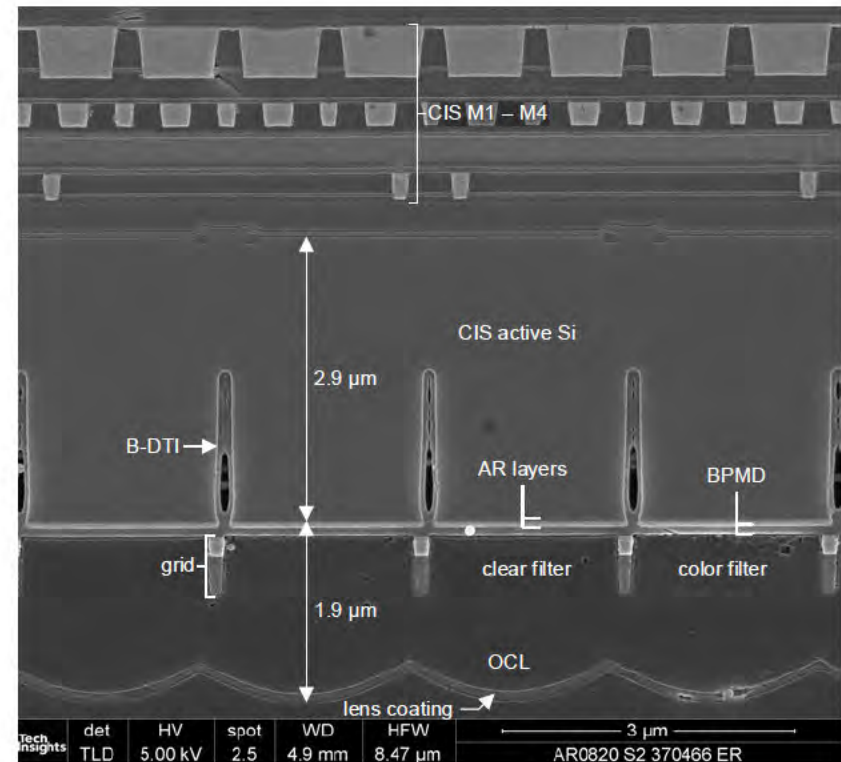
Active Pixels to Periphery Transition Overview – Top

CIS General Structure – Pixel Array

- SEM cross section overview images of the active pixels in the X- and Y-directions
- The CIS active Si is 2.9 μm thick and the optical stack is 1.9 μm thick. The 2017 version has a 2.2 μm thick optical stack.



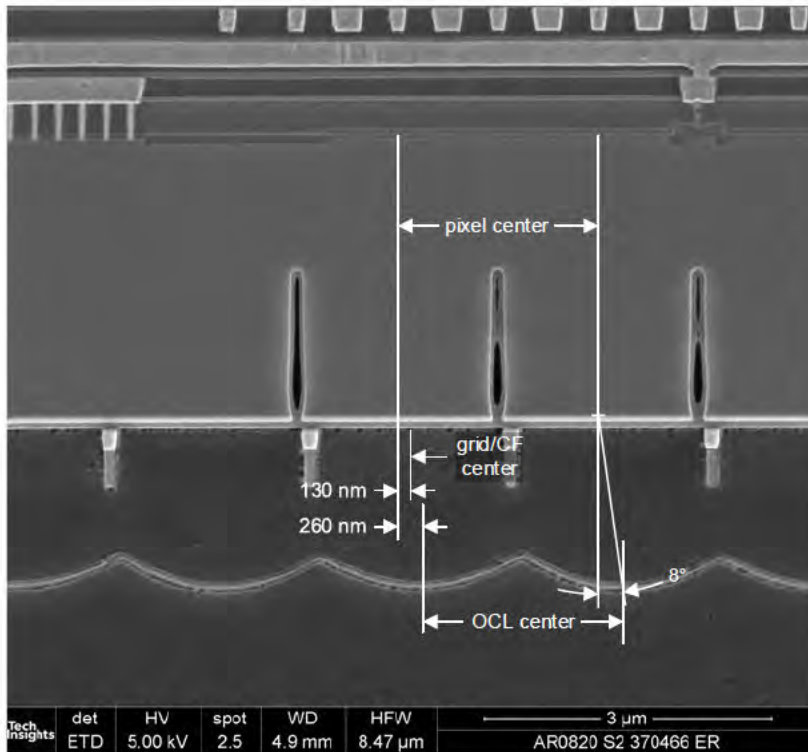
Active Pixels Overview – Y-Direction



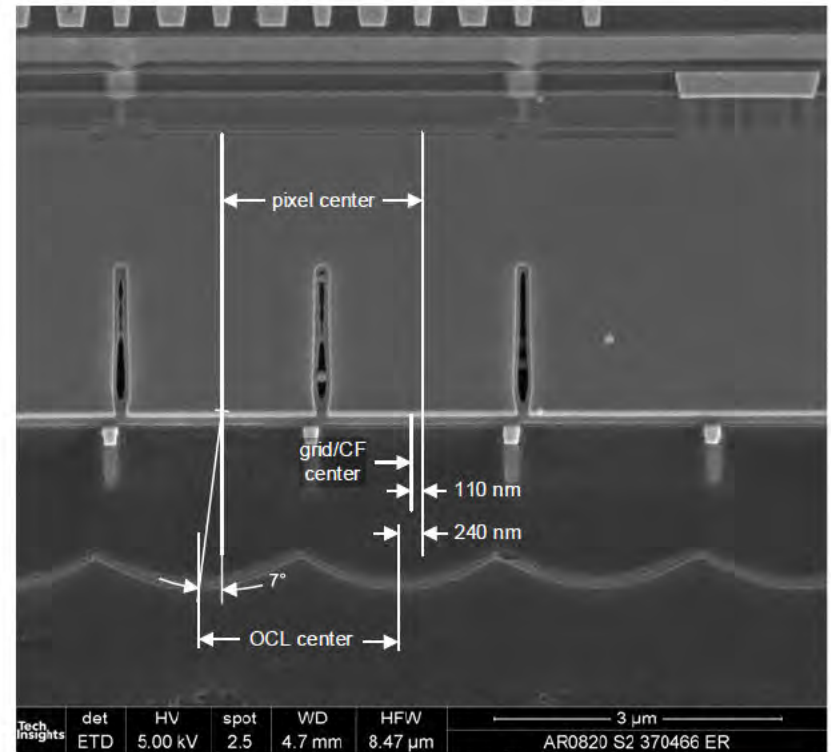
Active Pixels Overview – X-Direction

CIS General Structure – Edge Pixels Shift

- The edge pixels, OCL, CF, and grid are gradually shifted toward the array center.
 - At the left, the grid and CF are shifted by 130 nm and the OCLs are shifted by 260 nm. The center of the OCL is approximately 8° off-center of the pixel.
 - At the right, the grid and CF are shifted by 110 nm and the OCLs are shifted by 240 nm. The center of the OCL is approximately 7° off-center of the pixel.



Edge Microlens, Color Filters, and Grid Shift – Left

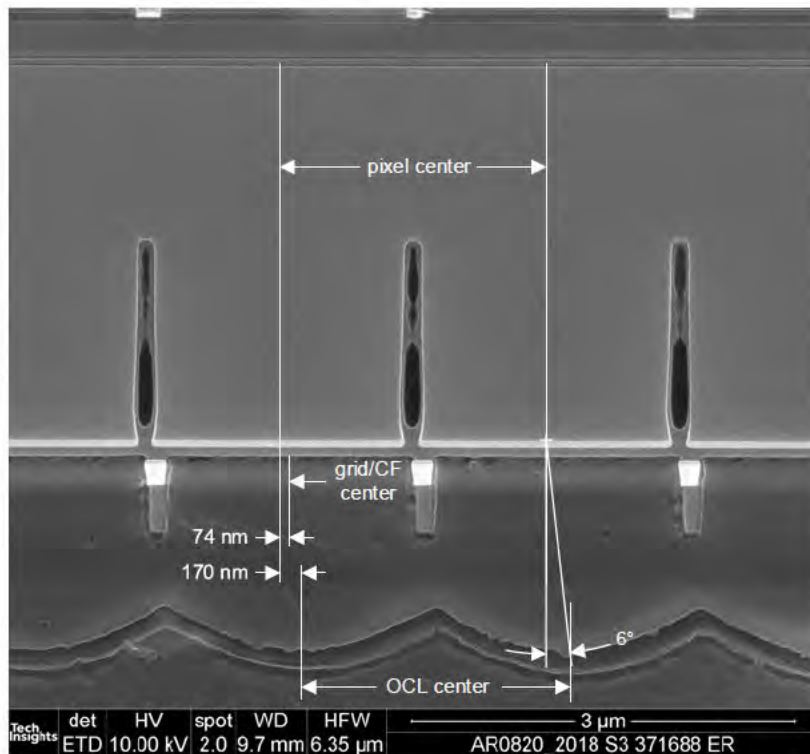


Edge Microlens, Color Filters, and Grid Shift – Right

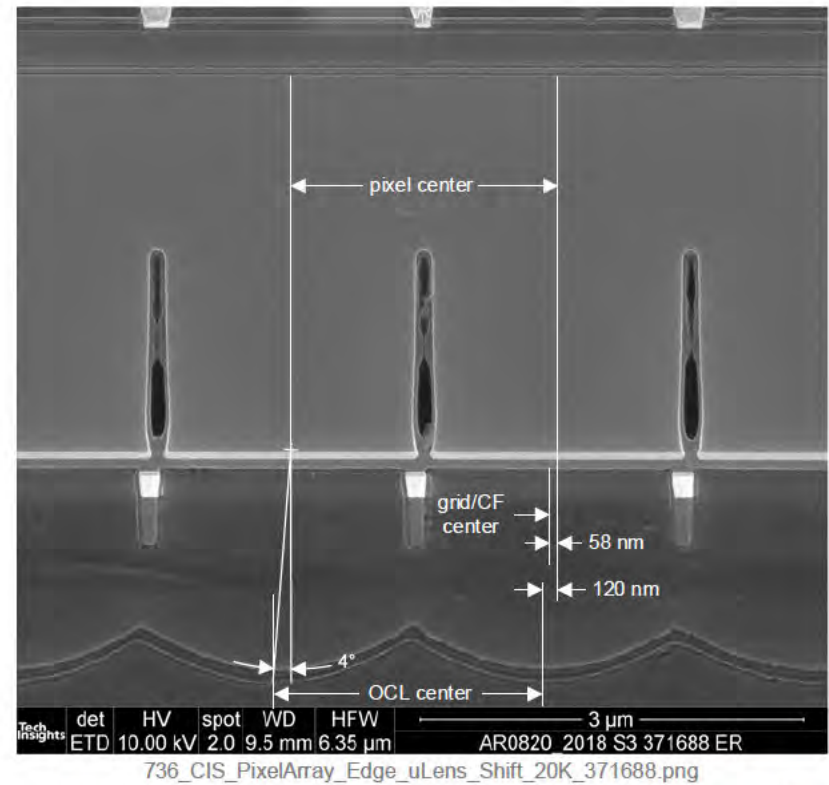
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CIS General Structure – Edge Pixels Shift

- The edge pixels, OCL, CF, and grid are gradually shifted toward the array center.
 - At the bottom, the grid and CF are shifted by 74 nm and the OCLs are shifted by 170 nm; the center of the OCL is approximately 6° off-center of the pixel.
 - At the top, the grid and CF are shifted by 58 nm and the OCLs are shifted by 120 nm; the center of the OCL is approximately 4° off-center of the pixel.



Edge Microlens, Color Filters, and Grid Shift – Bottom



Edge Microlens, Color Filters, and Grid Shift – Top

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CIS Die Active Si and Wells

CIS Active Si and Wells – Vertical Dimensions

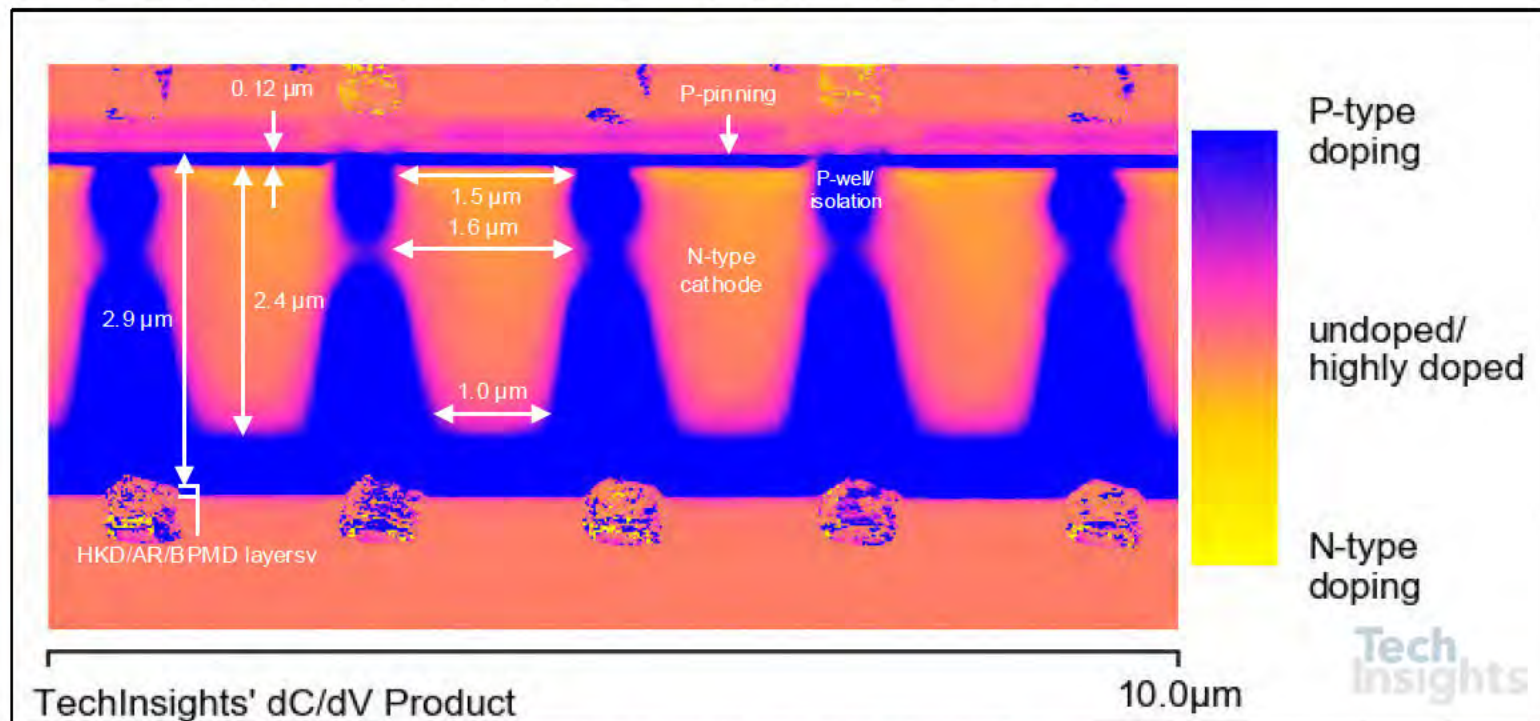
Feature	Dimension (μm)
CIS active Si thickness	2.9 ^a
N-photocathode thickness	2.4 ^b
P-pinning	0.12 ^b
Pixel array transistors N ⁺ S/D depth	0.14 ^b
Pixel array floating diffusion N ⁺ depth	0.30 ^b
Pixel array P-well	0.68 ^b
Peripheral deep N-well depth	2.4 ^b

CIS Active Si and Wells – Doping Levels

Feature	Doping (cm ⁻³)
N-type photocathode (75As) (upper region)	1.2×10^{18}
N-type photocathode (75As) (lower region)	$1 \times 10^{15} - 6 \times 10^{16}$
P-pinning (11B)	1×10^{22}
Pixel array N ⁺ S/D, N ⁺ FD (31P)	2×10^{21}
Pixel array P-well, P-type pixel isolation (11B)	$4 \times 10^{16} - 1 \times 10^{22}$
Pixel array V _{SS} contact (11B)	1×10^{22}
Pixel array active Si (11B)	1×10^{16}
Pixel array P-type B-DTI passivation (10B/11B)	$1 \times 10^{15} - 4 \times 10^{16}$
Periphery active Si (11B)	2×10^{16}
Periphery N-well	—

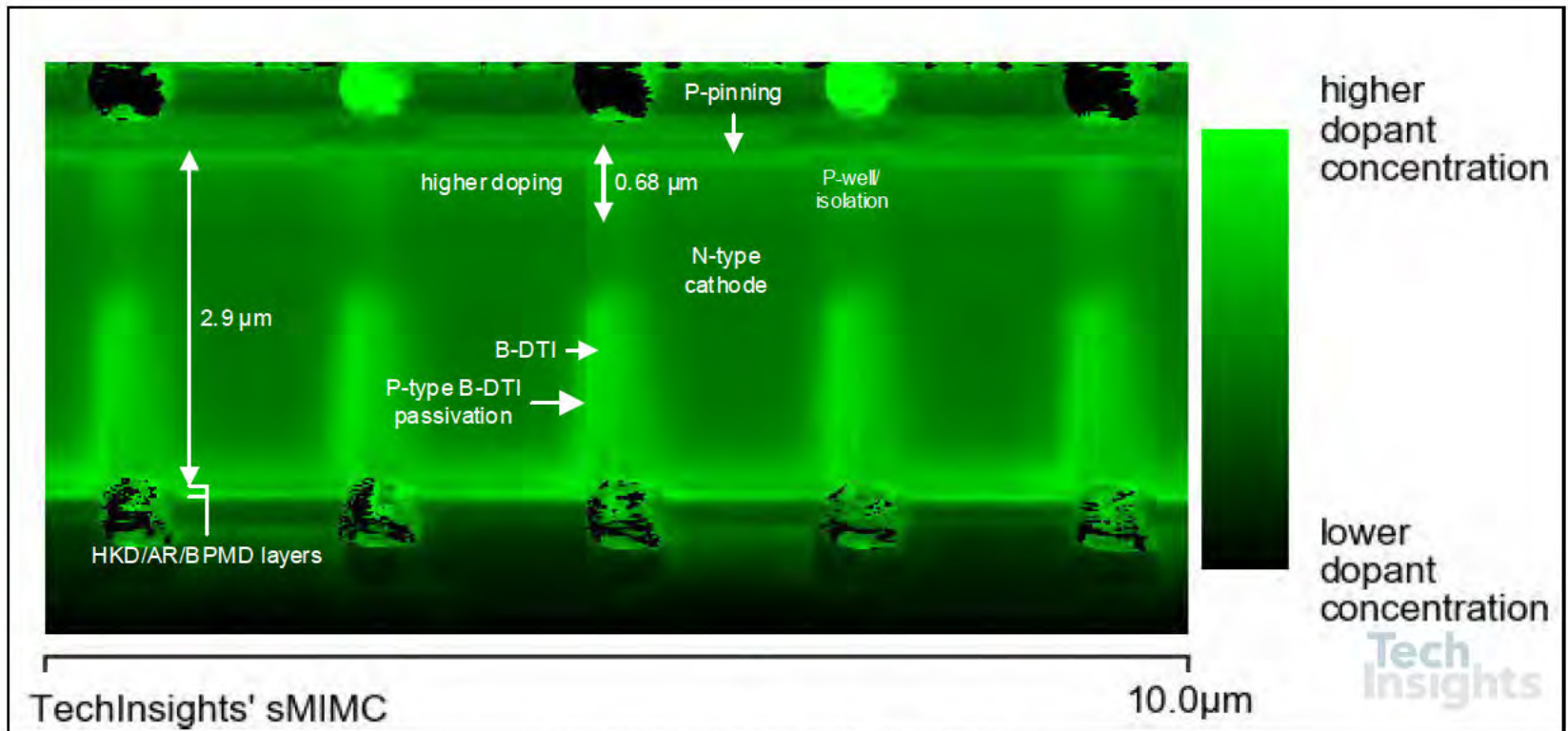
CIS Active Si and Wells – SCM Pixel Array

- Pages 49 and 50 show SCM and sMIM-C cross section images through the pixel center in the X-direction.
- The N-type cathode is 2.4 μm thick and 1.0-1.6 μm wide. The upper region of the photocathode has a higher doping concentration.
- The P-pinning layer is 0.12 μm deep, and the P-well/isolation regions are 0.68 μm deep.
- Note: The P-type region at the back of the active Si looks thicker than it is; this is likely due to the smearing of the P-type doping onto the HKD/AR and BPDM layers during the sample preparation.



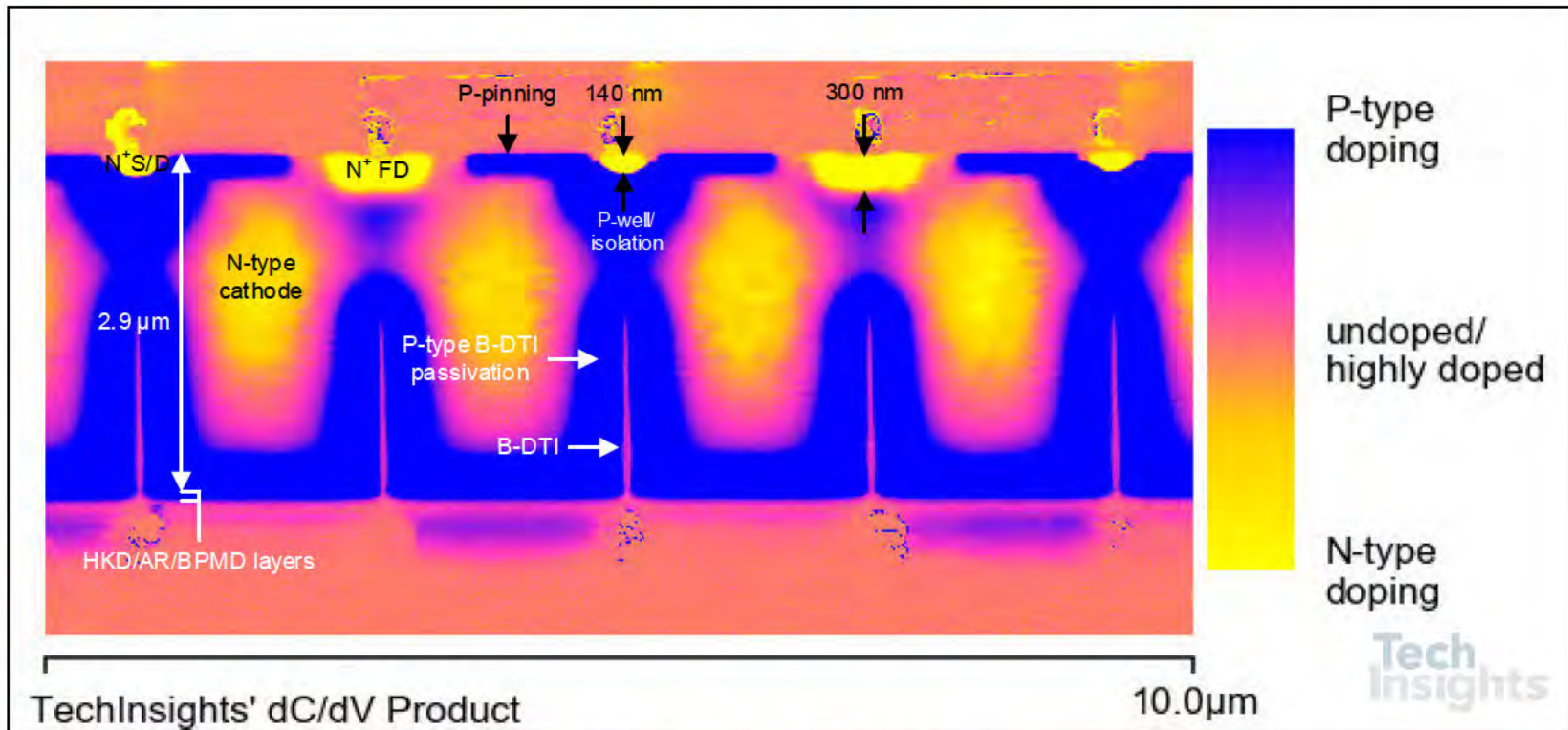
0720200854_PRODUCT_FRW_10.0u_512p_371688.png

CIS Active Si and Wells – SCM Pixel Array



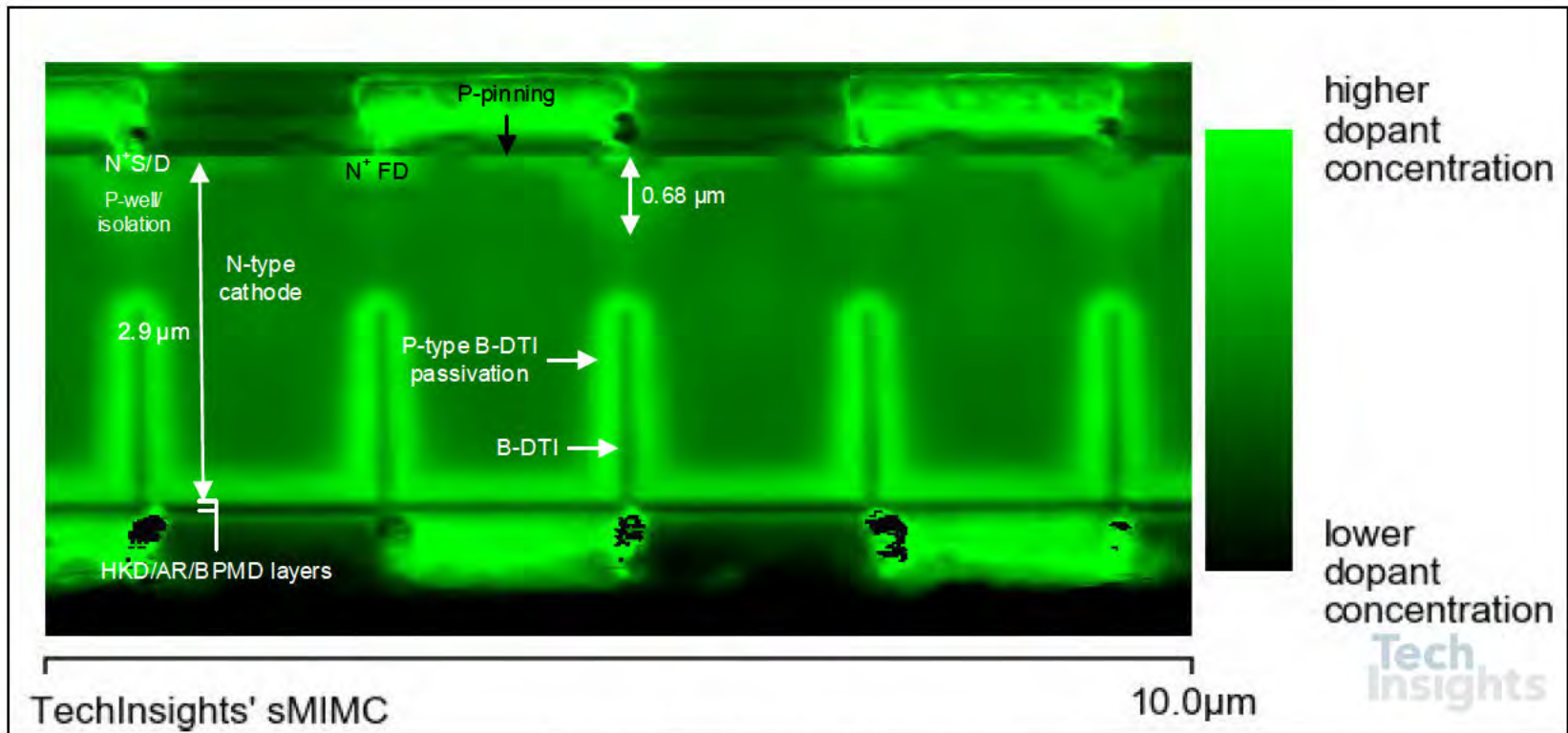
CIS Active Si and Wells – SCM Pixel Array

- Pages 51 and 52 show SCM and sMIM-C cross section images, respectively, through N^+ FD and N^+ S/D regions.
- The N^+ FD and region is 300 nm deep and the N^+ S/D is 140 nm deep.
- The P-well/isolation region is 0.68 μm deep.
- Note: The P-type region at the back of the active Si looks thicker than it is; this is likely due to the smearing of the P-type doping onto the HKD/AR and BPDM layers during the sample preparation.



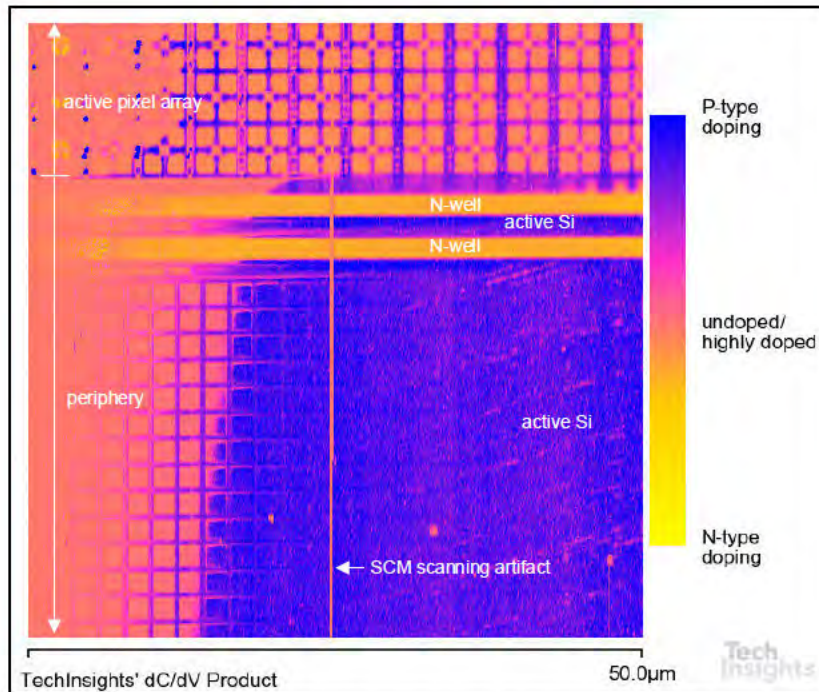
0711201032_PRODUCT_FRW_10.0u_512p_370466.png

CIS Active Si and Wells – SCM Pixel Array



0711201032_SMIMC_FRW_10.0u_512p_370466.png

CIS Active Si and Wells – SCM Periphery

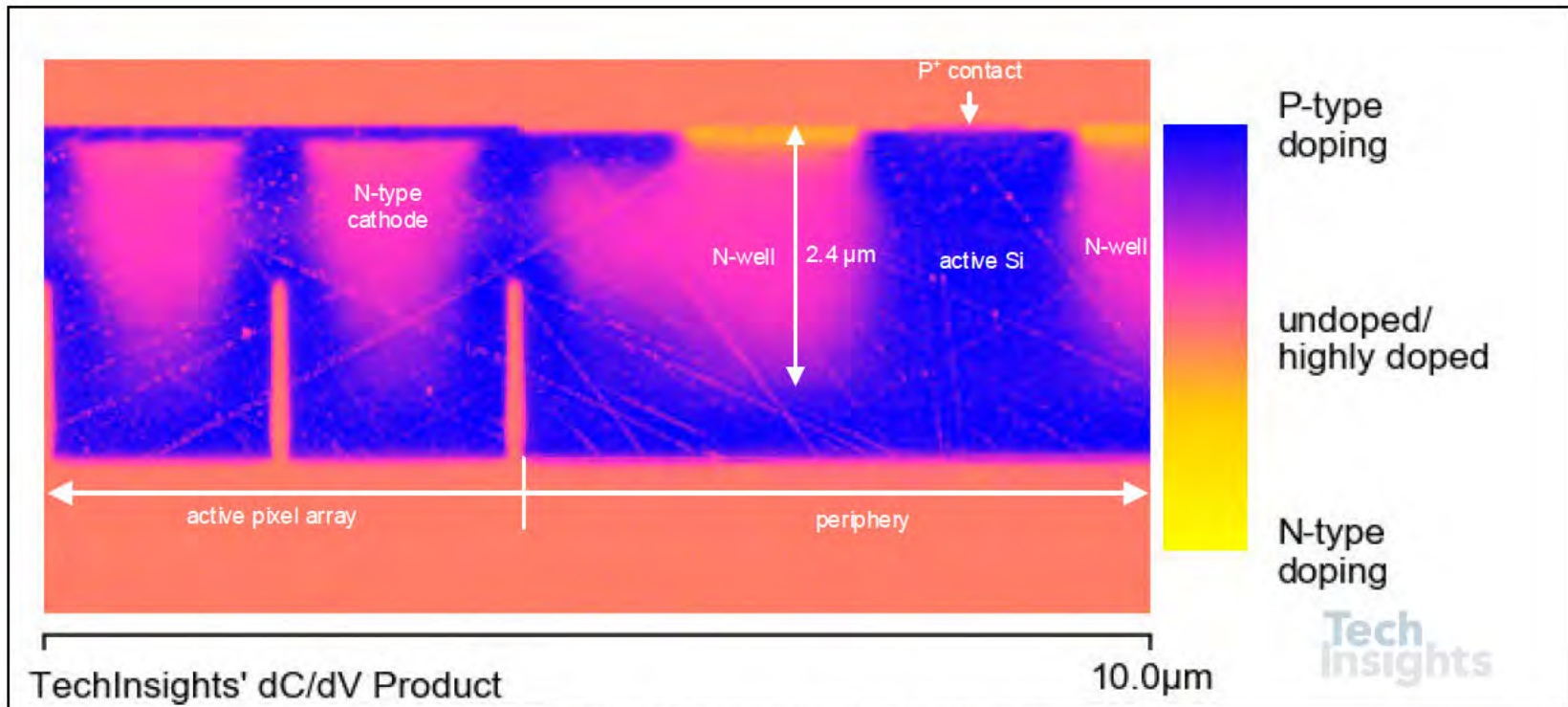


0718201124_PRODUCT_FRW_50.0u_512p_371773.png

- SCM plan-view image at the transition from the pixel array to the periphery
- Two deep N-wells were observed at the transition from the pixel array to the periphery at the bottom of the pixel array.

CIS Active Si and Wells – SCM Periphery

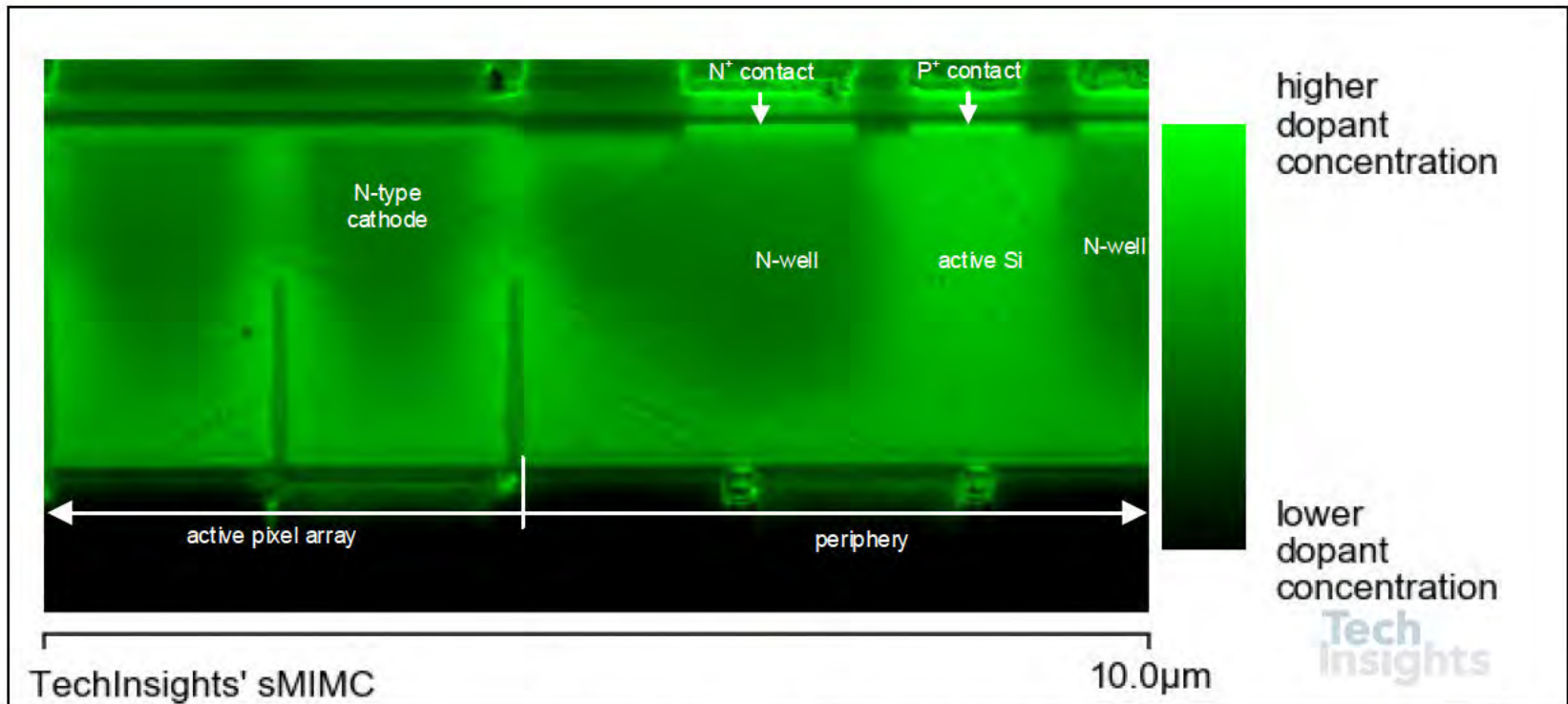
- SCM cross section image at the transition from active pixels to the peripheral region
- Two 2.4 μm deep N-wells were observed at the transition from the pixel array to the peripheral region.



0721200937_PRODUCT_FRW_10.0u_512p_371688.png

CIS Active Si and Wells – SCM Periphery

- SCM cross section image at the transition from active pixels to the periphery region, showing the two deep N-wells and the N⁺ N-well contact region and P⁺ active Si contact region.



0721200937_SMIMC_FRW_10.0u_512p_371688.png

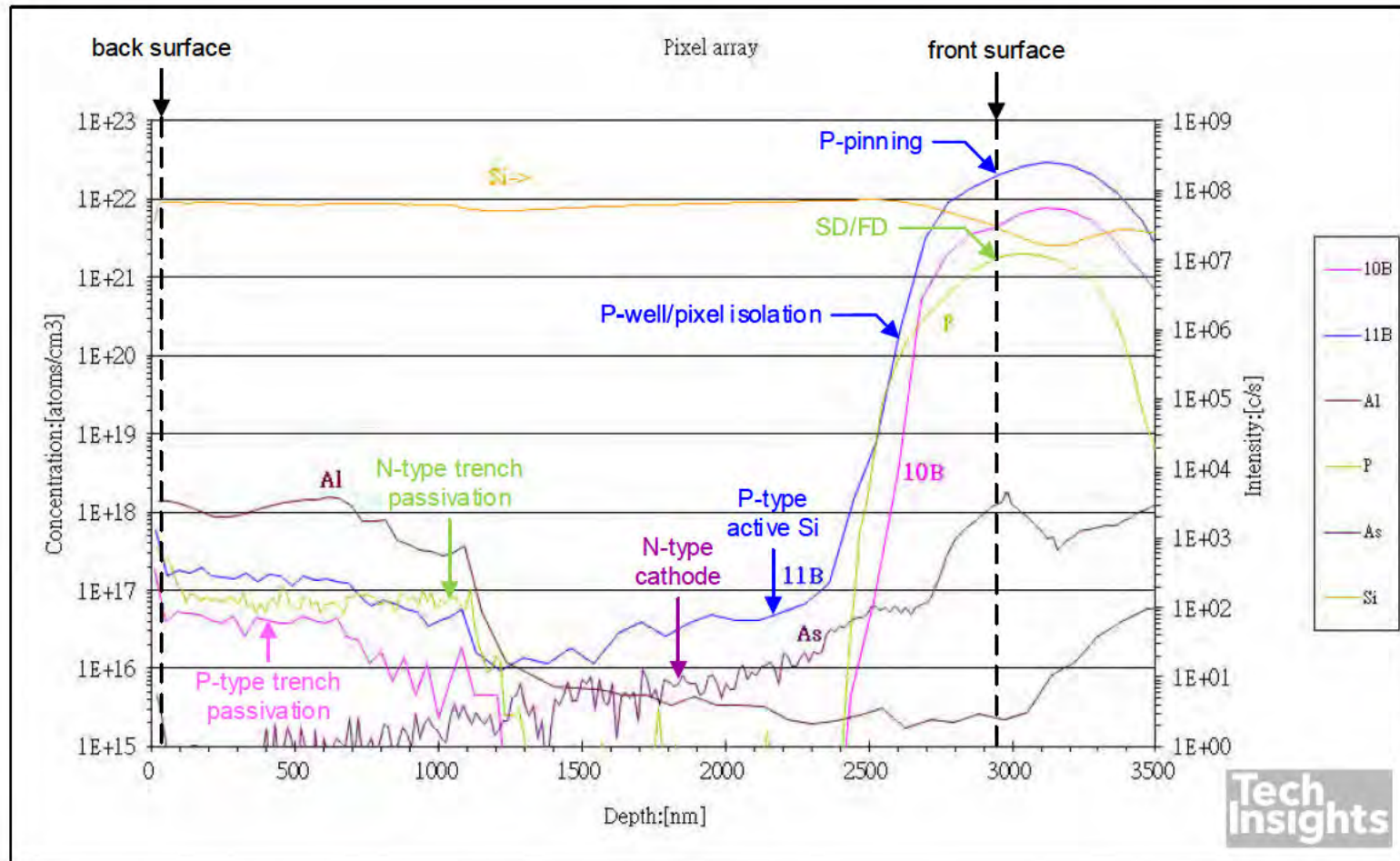
CIS Active Si and Wells – SIMS Analysis

CIS Active Si and Wells – Pixel Array SIMS Doping Profile

for the passivation of the B-DTI trench to reduce dark current.

of $8 \times 10^{16} \text{ cm}^{-3}$ at a depth of $1.8 \text{ }\mu\text{m}$ up to the back of the active Si. The increasing 31P doping concentration seems to be associated with the presence of B-DTI and could be one of a few steps used to neutralize the interface states at the B-DTI Si/SiO interface.

CIS Active Si and Wells – Pixel Array SIMS Doping Profile

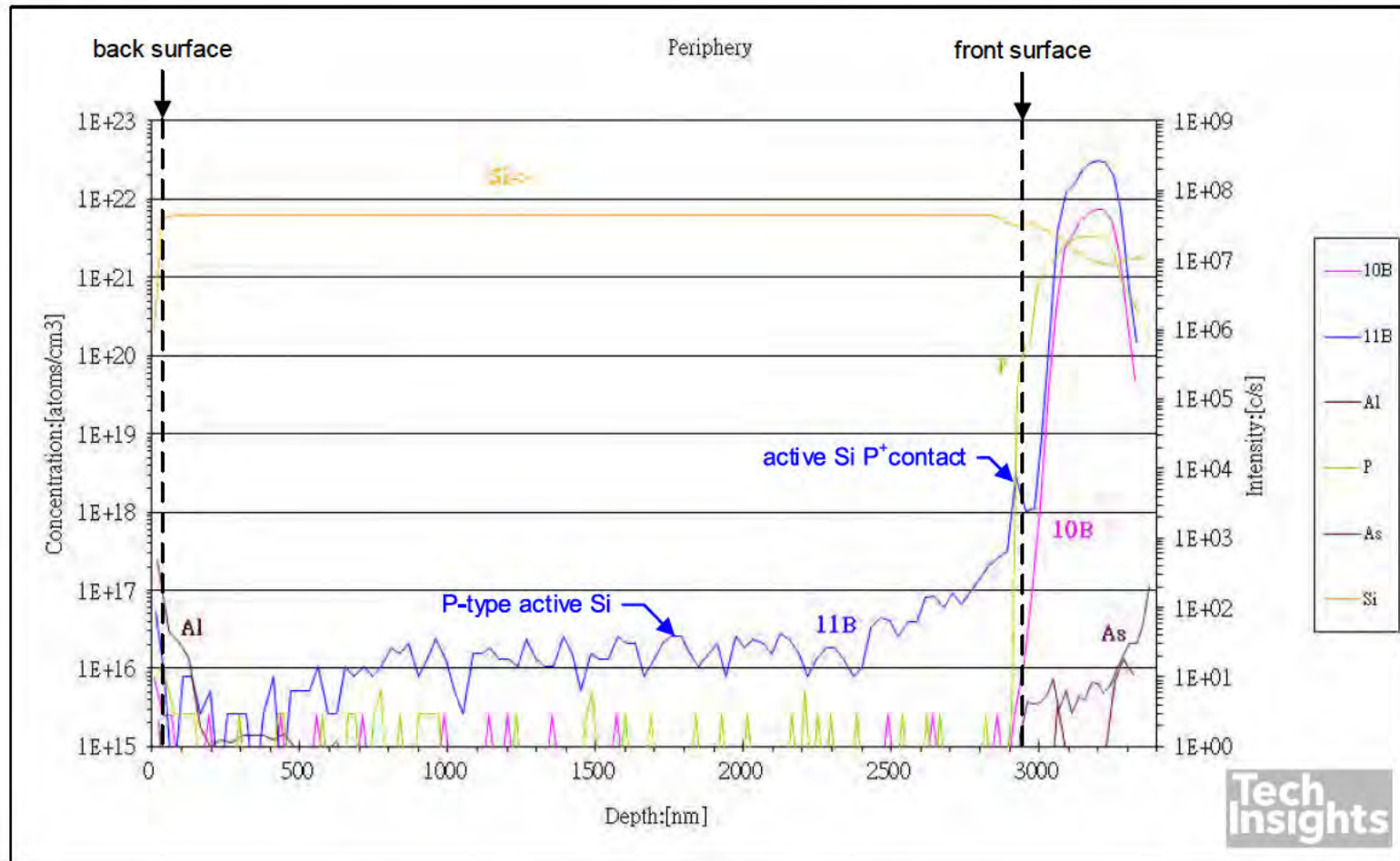


Pixel Array Doping Profile – SIMS

CIS Active Si and Wells – Periphery SIMS Doping Profile

$1 \times 10^{15} \text{ cm}^{-3}$ at this SIMS analysis location.

CIS Active Si and Wells – Periphery SIMS Doping Profile



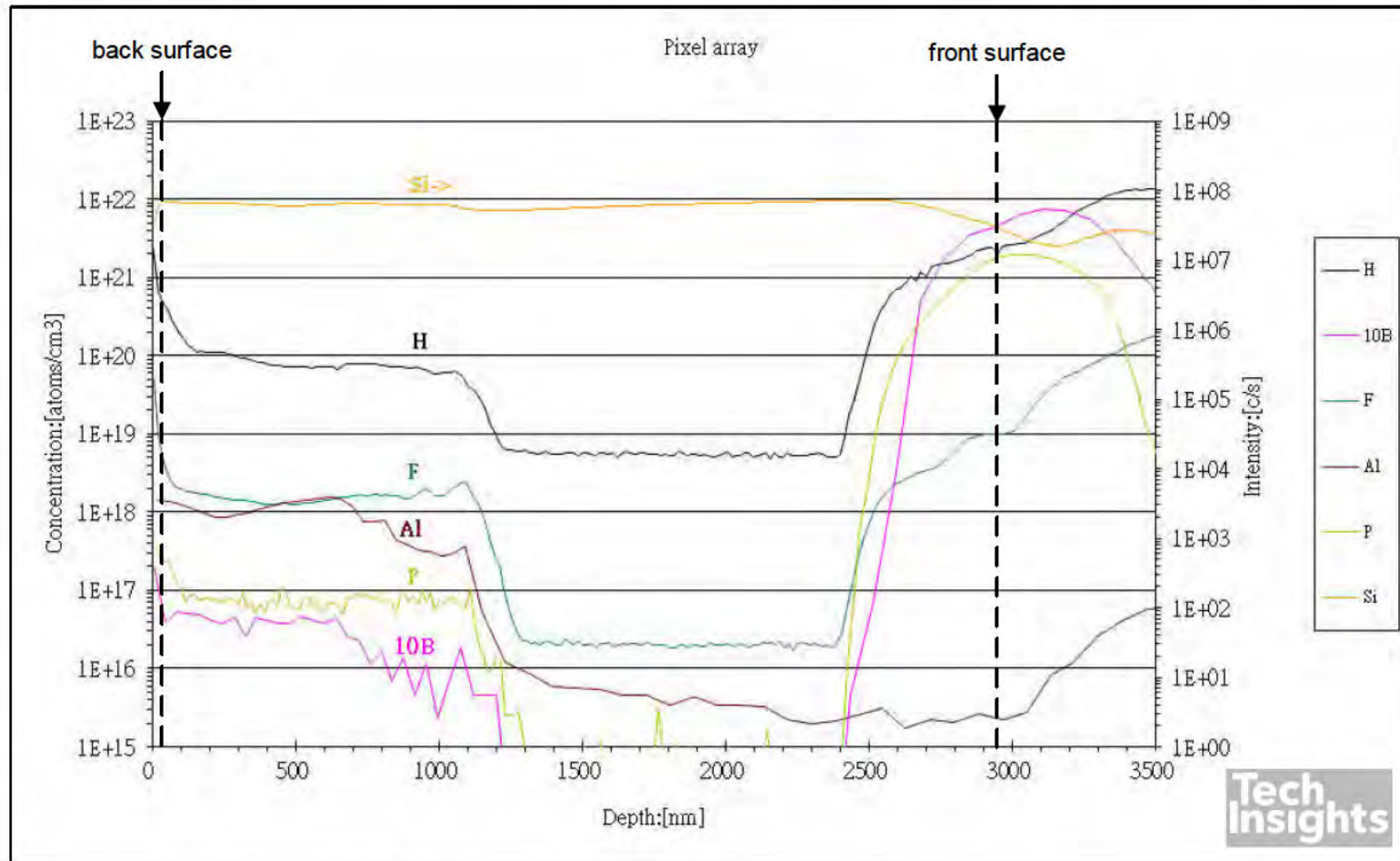
Periphery Doping Profile – SIMS

CIS Active Si and Wells – Trench Passivation SIMS Doping Profile

$7 \times 10^{16} \text{ cm}^{-3}$. The increasing P doping concentration is associated with the presence of B-DTI and could be one of a few steps used to neutralize the interface states at the B-DTI Si/SiO interface.

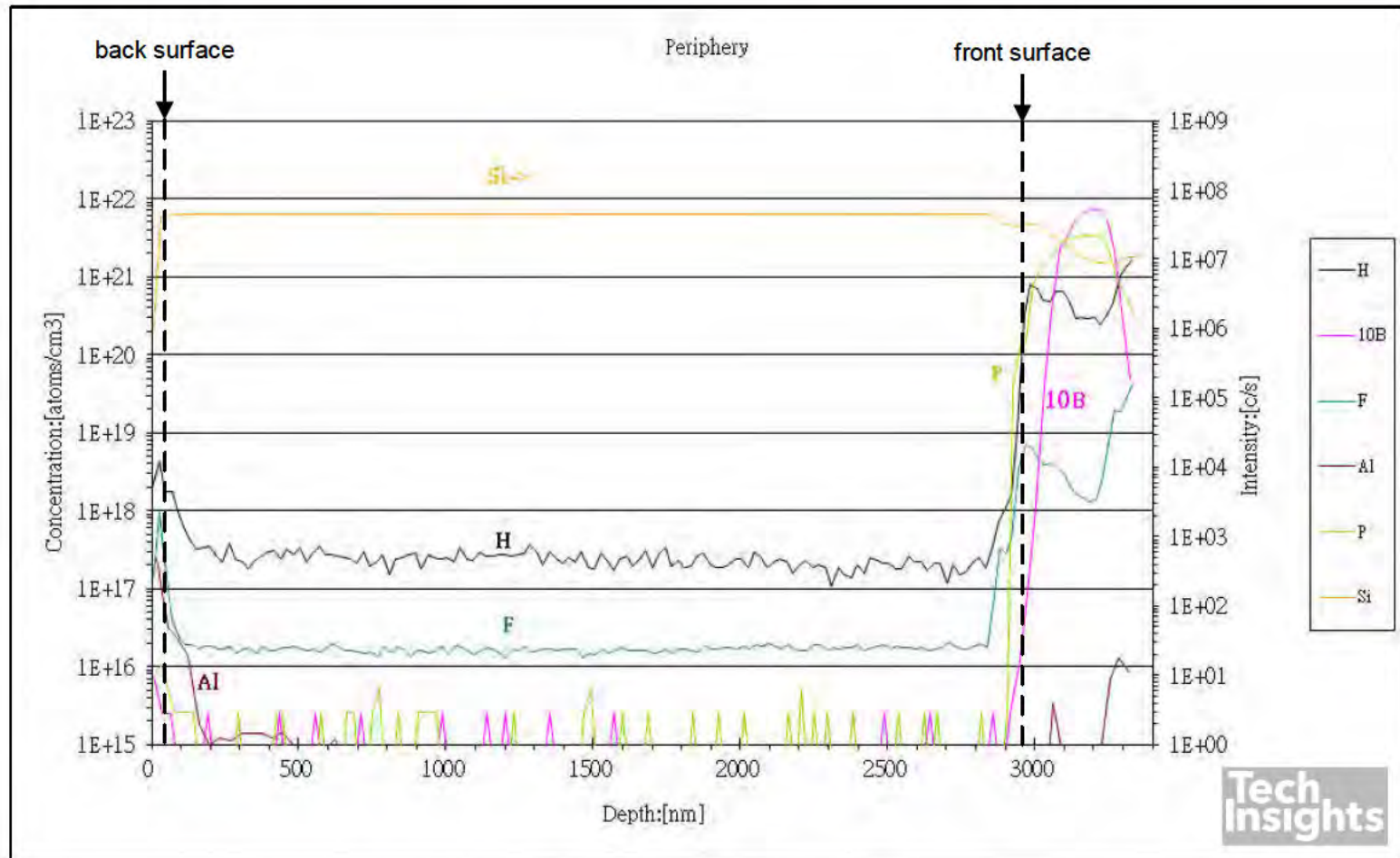
for the passivation of the B-DTI trench [\[4\]](#) [\[5\]](#).

CIS Active Si and Wells – Trench Passivation SIMS Doping Profile



Pixel Array F, H, P, and 10B Doping Profile – SIMS

CIS Active Si and Wells – SIMS Trench Passivation

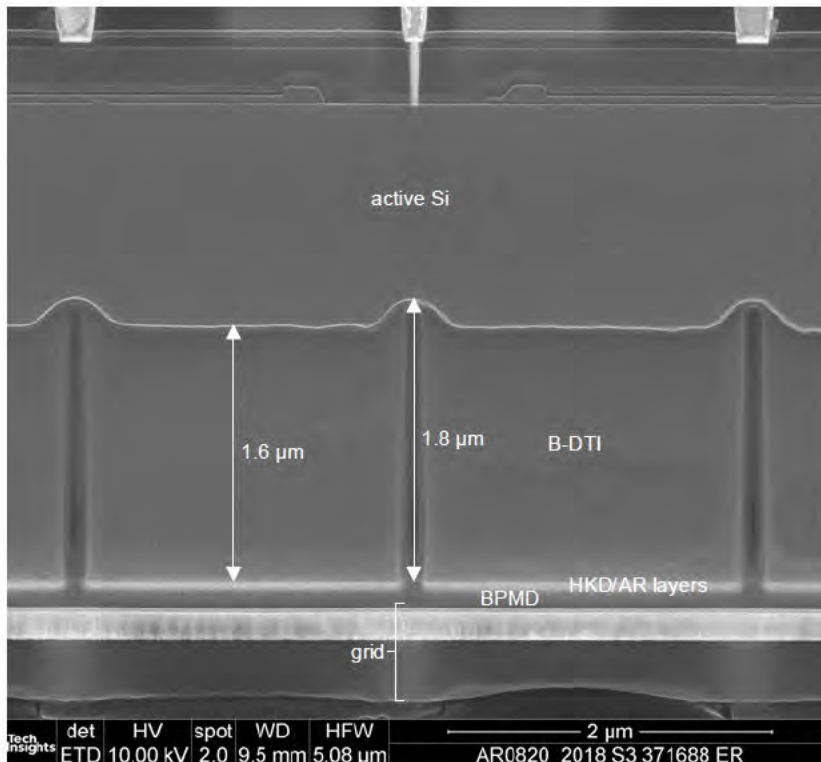


Periphery F, H, P, and 10B Doping Profile – SIMS

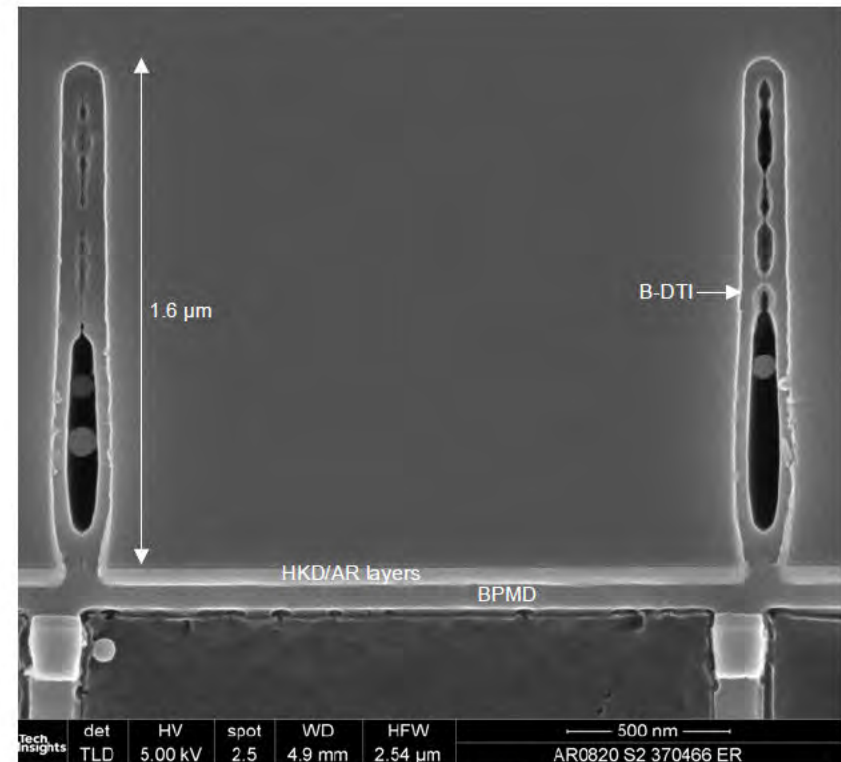
CIS Isolation Structures

CIS Pixel Isolation – B-DTI

- The pixel isolation is realized using partial depth B-DTI and P-type doping.
- The depth of the B-DTI trench varies from 1.6 μm at the grid edge intersection to 1.8 μm at the grid vertices.



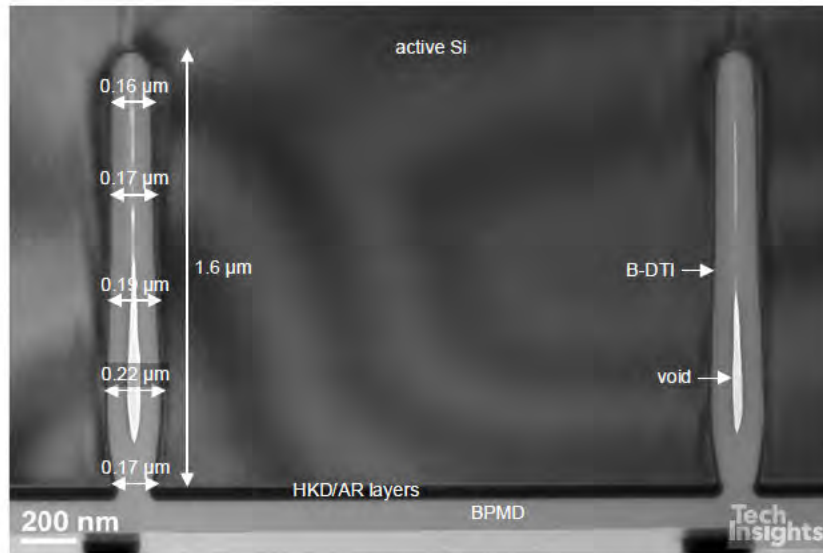
751_CIS_PixelArray_B-DTI_Between_Pixels_25K_371688.png



476_CIS_PixelArray_B-DTI_50K_370466.png

B-DTI at Grid Edge Intersection – TEM

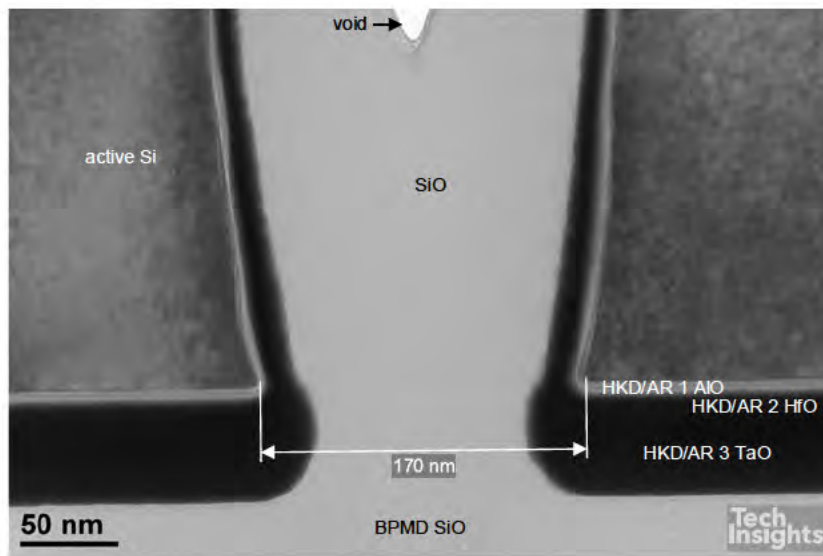
CIS Pixel Isolation – B-DTI



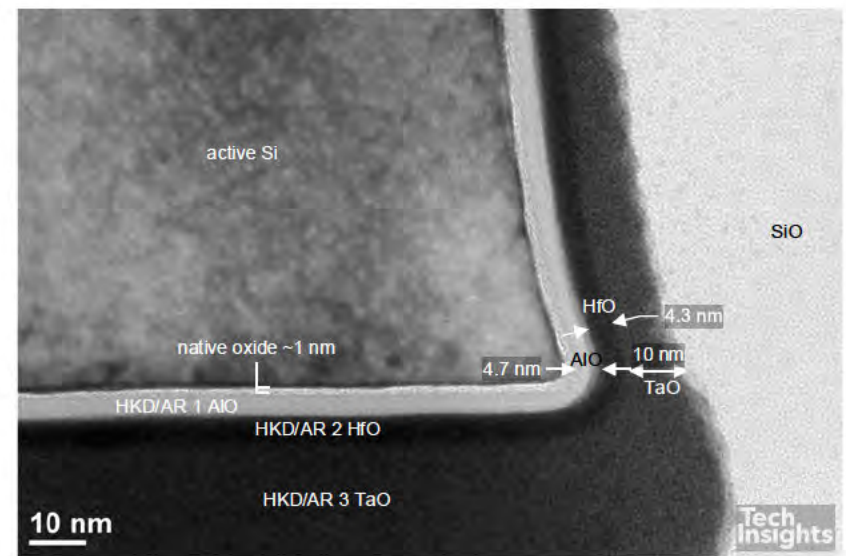
- TEM cross section overview image of the B-DTI at the grid edge intersection
- The depth of the B-DTI trench is $1.6\text{ }\mu\text{m}$ at the grid edge intersection and the average width is about $0.18\text{ }\mu\text{m}$. The B-DTI aspect ratio is approximately 8.9 ($1.6\text{ }\mu\text{m}/0.18\text{ }\mu\text{m}$).
- The oxide fill layer pinches near the B-DTI trench top (mouth) during the deposition step, creating a void.

CIS Pixel Isolation – B-DTI

- The B-DTI is etched from the back of the CIS active Si after the CIS wafer thinning.
- The B-DTI trench is lined with the HKD/AR layers (AlO/HfO/TaO) and filled with the oxide.
- Near the top (mouth), the B-DTI trench is 170 nm wide, and the HKD/AR 1 AlO is 4.7 nm thick, HKD/AR 2 HfO is 4.3 nm thick, and HKD/AR 3 TaO is 10 nm thick.



BDTI_bot_64kx_370534.png

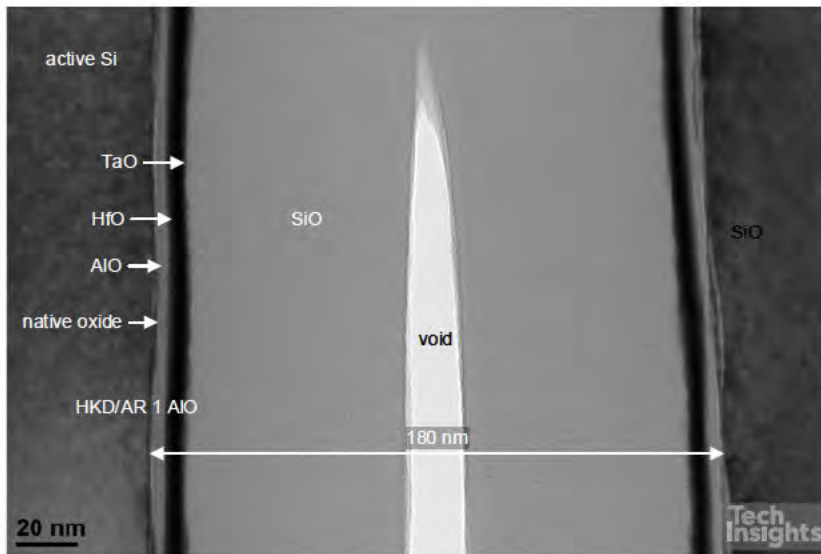


BDTI_bot_180kx_370534.png

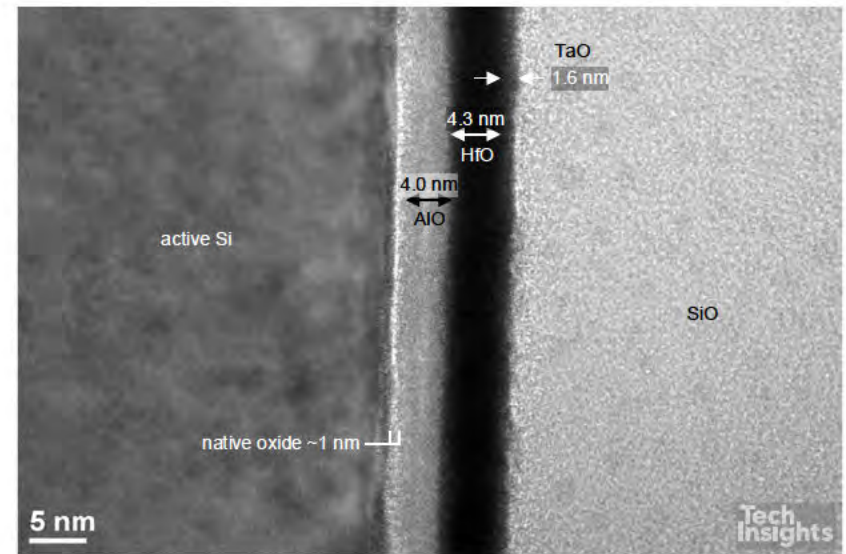
B-DTI Top Detail – TEM

CIS Pixel Isolation – B-DTI

- Near the center, the HKD/AR 1 AlO is 4.0 nm thick, HKD/AR 2 HfO is 4.3 nm thick, and HKD/AR 3 TaO is 1.6 nm thick.



BDTI_mid_88kx_370535.png

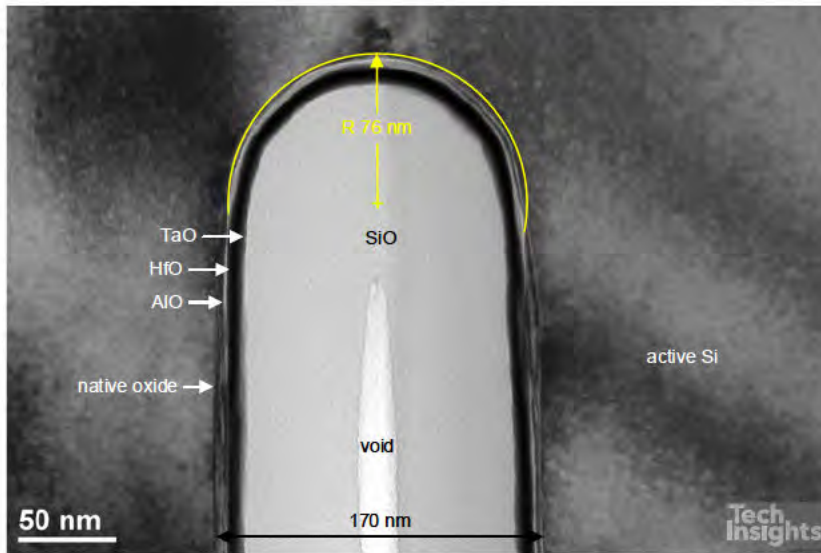


BDTI_mid_360kx_370534.png

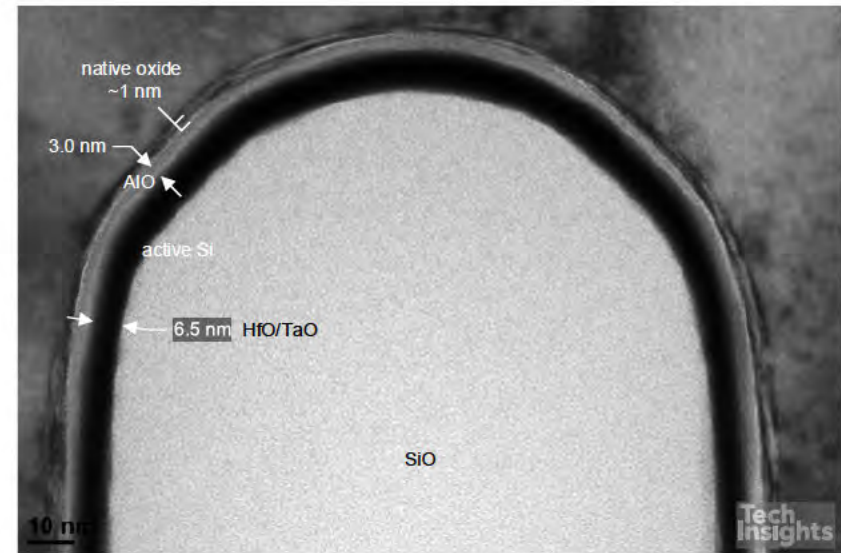
B-DTI Center Detail – TEM

CIS Pixel Isolation – B-DTI

- The B-DTI near the bottom is 170 nm wide, and the radius of curvature is approximately 76 nm.
- The HKD/AR 1 AIO is 3.0 nm thick, and the HKD/AR 2/3 HfO/TaO is 6.5 nm thick.



BDTI_top_64kx_370534.png

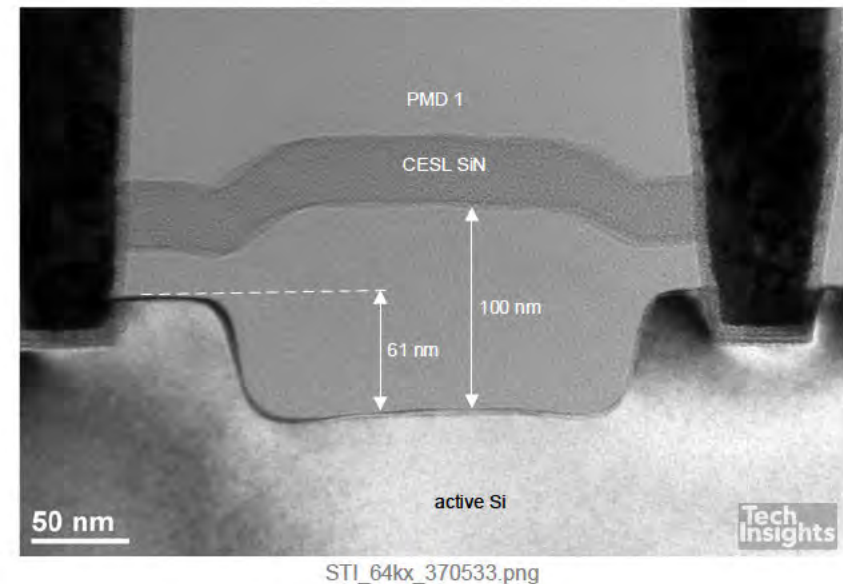
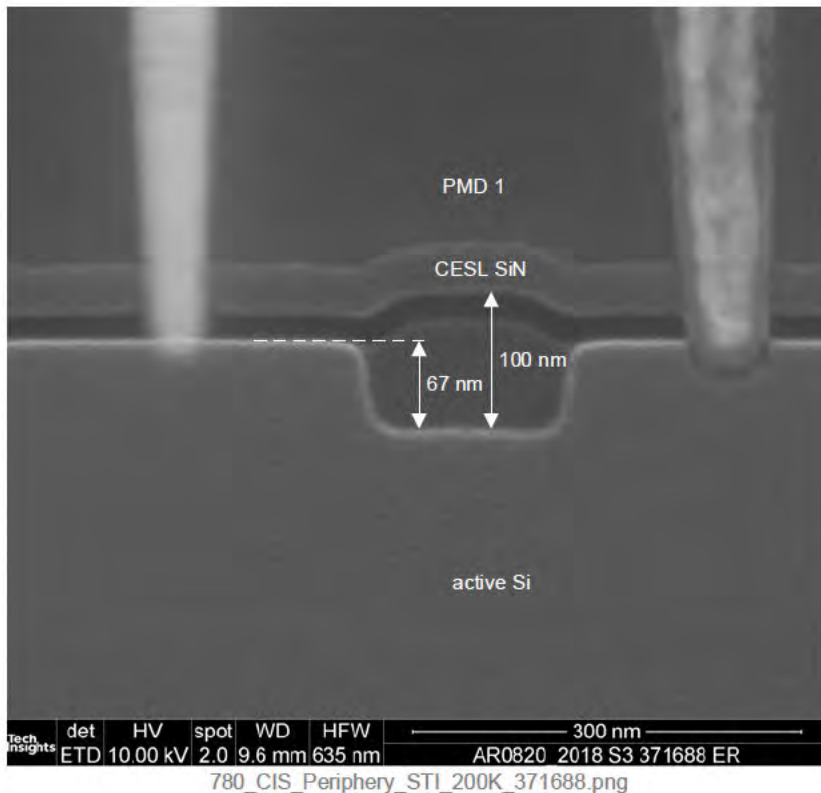


BDTI_top_130kx_370535.png

B-DTI Bottom Detail – TEM

CIS Pixel Transistors Isolation – STI

- SEM and TEM cross section images of the STI in the periphery and pixel array, respectively
- The STI thickness below the active Si in the periphery and pixel array are 67 nm and 61 nm, respectively.



STI Pixel Array – TEM

CIS Front Dielectrics and Metal Interconnect

CIS Front Dielectrics Summary – Pixel Array

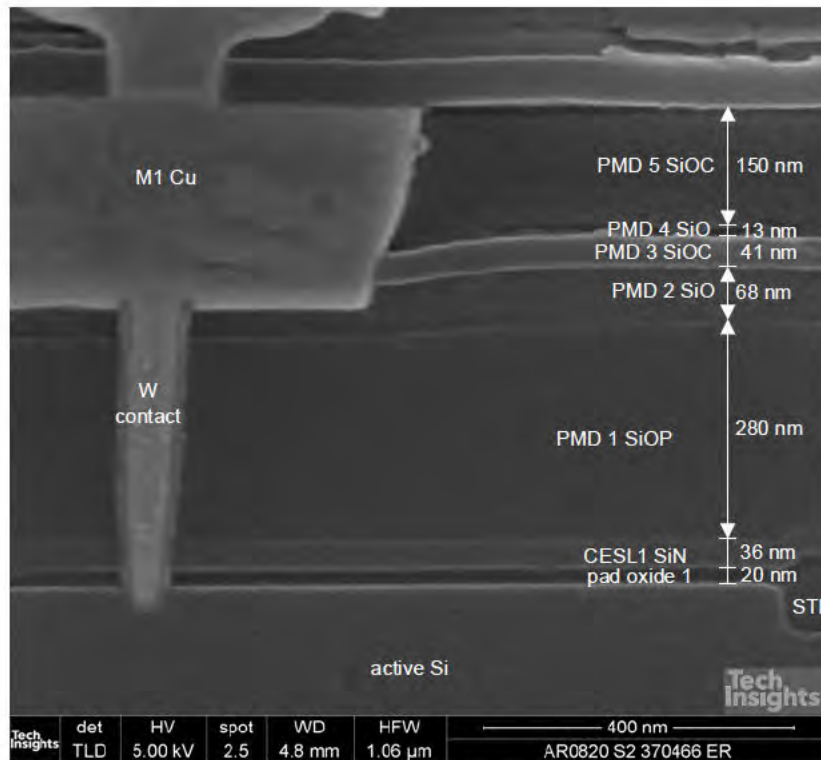
Layer (Pixel Array Region)	Composition (Based on TEM-EDS)	Thickness (nm)
Pad oxide 1/2	SiO/SiO	20/20
CESL 1/CESL 2	SiN/SiN	36/36
PMD 1/PMD 2/PMD 3/PMD 4/PMD 5	SiOP/SiO/SiOC/SiO/SiOC	260/67/31/13/180
ILD 1-1/ILD 1-2/ILD 1-3	SiCN/SiO/SiOC	57/29/260
ILD 2-1/ILD 2-2/ILD 2-3	SiCN/SiO/SiOC	57/25/260
ILD 3-1/ILD 3-2/ILD 3-3/ILD 3-4	SiNO/SiO/SiON/SiO	60/260/52/370
Passivation 1/passivation 2	SiN/SiO	70/330
CIS WBL 1	SiON	73
ISP WBL 1	SiON	79
Interface bonding layer (IBL)	SiO	4.2

CIS Front Metals Summary

Layer	Composition (Based on TEM-EDS)	Thickness (nm)
Metal 1/liner	Cu/Ta-based	280
Metal 2/liner	Cu/Ta-based	250
Metal 3/liner	Cu/Ta-based ¹	230
Metal 4/liner	Cu/Ta-based	510
CIS metal 5 (DBI)/liner	Cu/Ta-based	470
ISP metal 7 (DBI)/liner	Cu/Ta-based	500

¹ The metal 3 layer was not analyzed; a likely composition is shown, based on the similarity to the metal 2 layer.

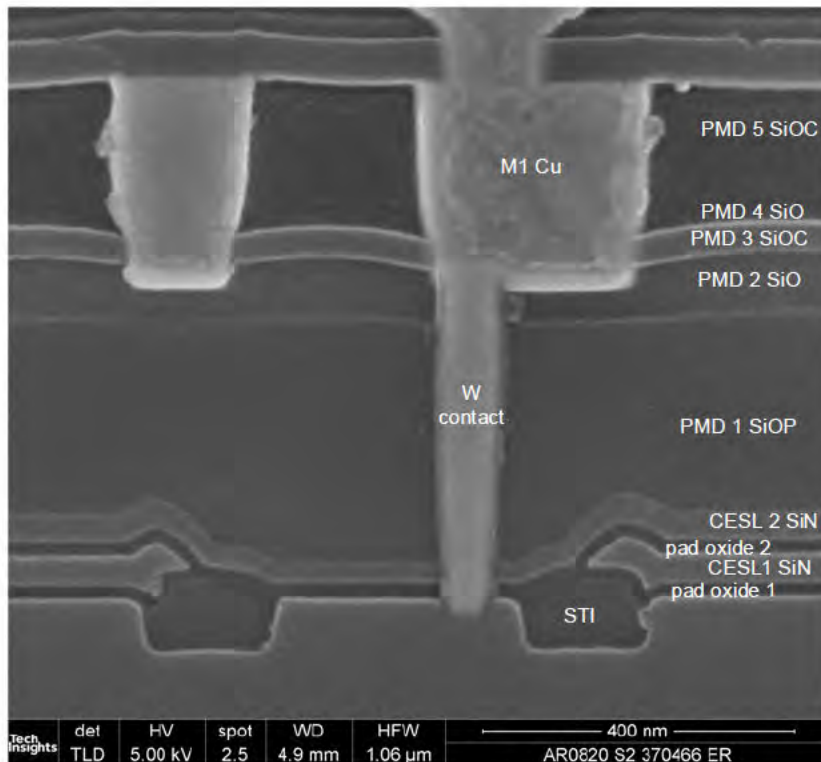
CIS Front Dielectrics and Metals



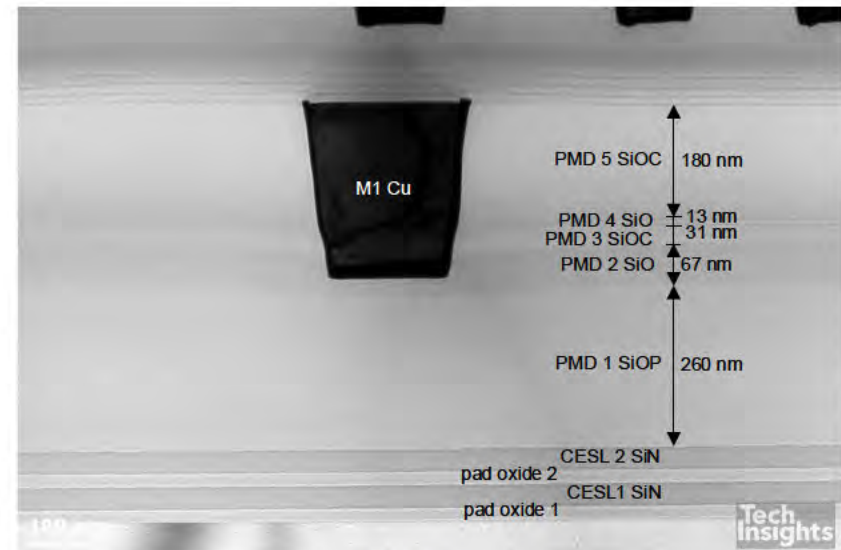
- The PMD in the periphery comprises a 20 nm thick pad oxide, a 36 nm thick CESL 1 nitride, a 280 nm thick PMD 1 SiOP, a 68 nm thick PMD 2 oxide, a 41 nm thick PMD 3 SiOC, a 13 nm thick PMD 4 oxide, and a 150 nm thick PMD 5 SiOC.

CIS Front Dielectrics and Metals

- The PMD in the pixel array comprises the same seven layers as the periphery, with additional pad oxide 2 and CESL 2 layers. The PMD in the pixel array includes a 20 nm thick pad oxide 1, a 36 nm thick CESL 1 nitride, a 20 nm thick pad oxide 2, a 36 nm thick CESL 2 nitride, a 260 nm thick PMD 1 SiOP, a 67 nm thick PMD 2 oxide, a 31 nm thick PMD 3 SiOC, a 13 nm thick PMD 4 oxide, and a 180 nm thick PMD 5 SiOC.



485_CIS_PixelArray_Vpix_120K_370466.png

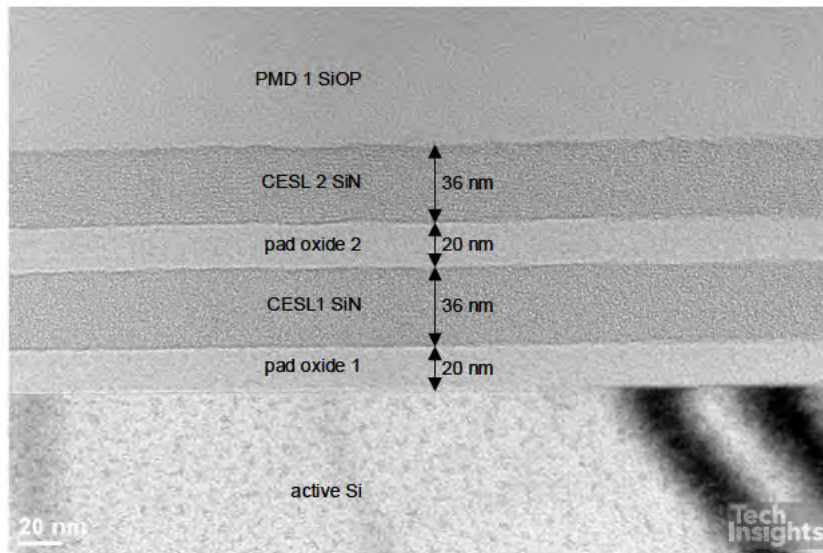


PMD_17.5kx_1_370533.png

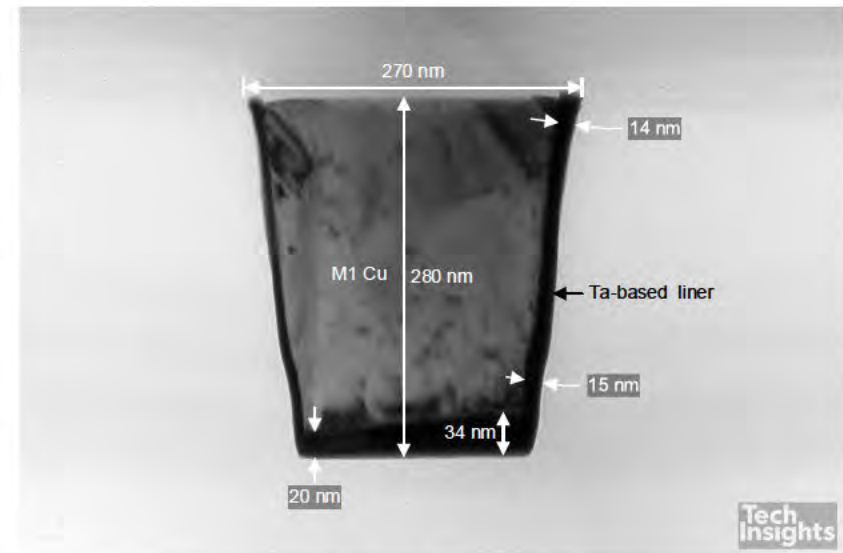
Pixel Array PMD – TEM

CIS Front Dielectrics and Metals

- The pixel array PMD lower layers comprise 20 nm thick pad oxide 1, a 36 nm thick CESL 1 nitride, a 20 nm thick pad oxide 2, and a 36 nm thick CESL 2 nitride.
- Metal 1 is 280 nm thick and 270 nm wide single Cu damascene with a Ta-based liner.



PMD_Lower_layers_64kx_370533.png

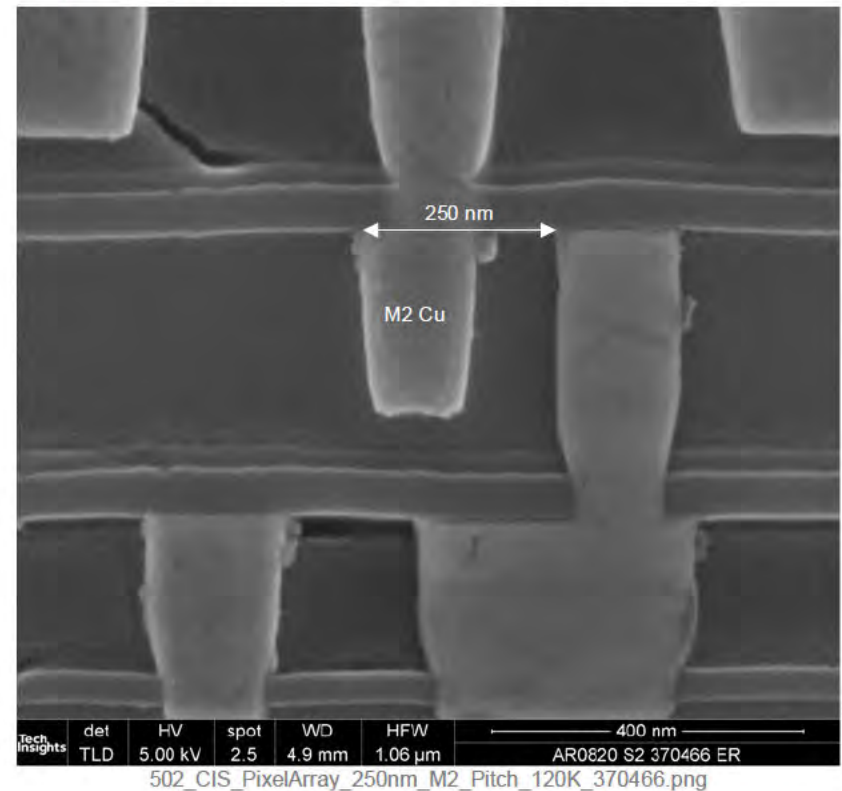
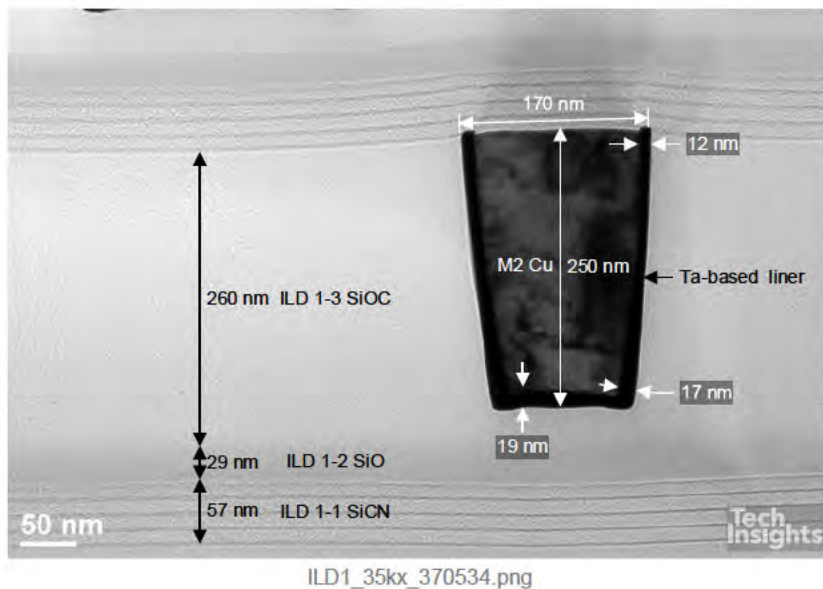


M1_35kx_370533.png

Metal 1 – TEM

CIS Front Dielectrics and Metals

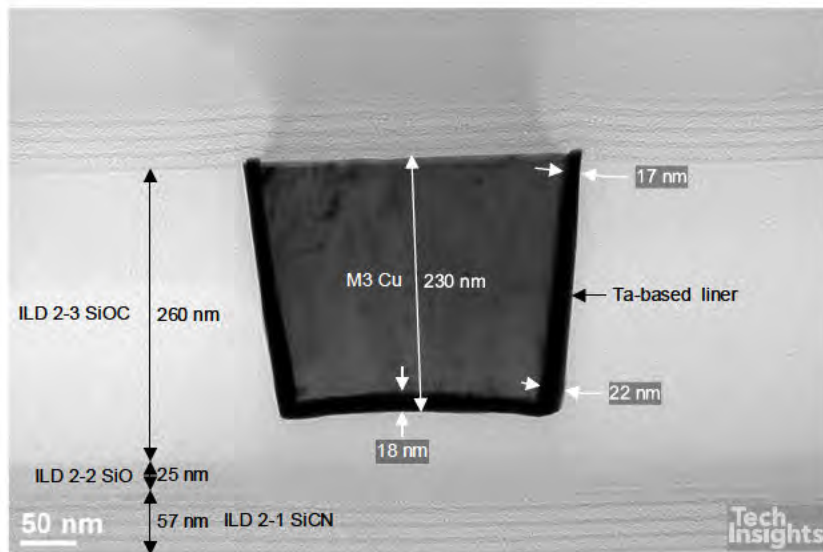
- Metal 2 through metal 4 are dual Cu damascene with single Ta-based liners.
- ILD 1 through ILD 3 have the same structure and composition. ILD 1 comprises a 57 nm thick ILD 1-1 SiCN, a 29 nm thick ILD 1-2 oxide, and a 260 nm thick ILD 1-3 SiOC.
- Metal 2 is 250 nm thick and 170 nm wide. The minimum metal pitch of 250 nm was observed in metal 2.



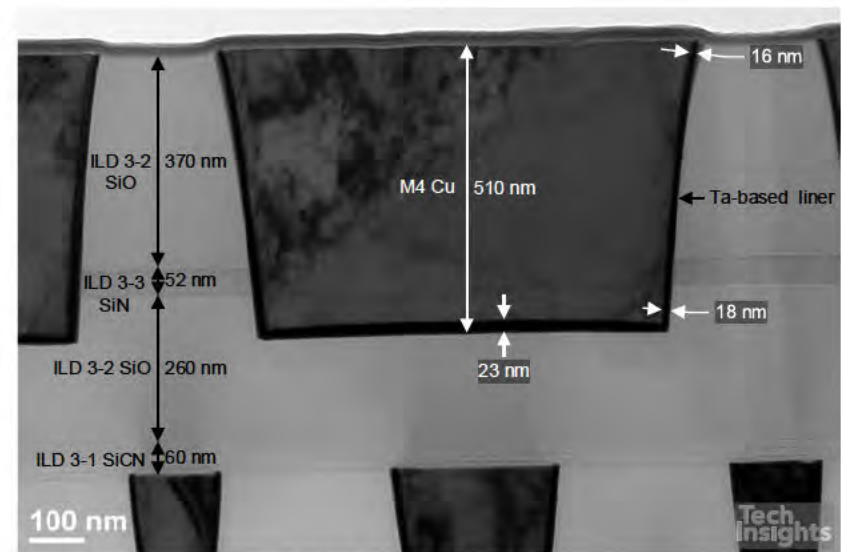
Metal 2 Minimum Pitch – SEM

CIS Front Dielectrics and Metals

- Metal 3 is 230 nm thick. ILD 2 comprises a 57 nm thick ILD 2-1 SiCN, a 25 nm thick ILD 2-2 oxide, and a 260 nm thick ILD 2-3 SiOC.
- Metal 4 is 510 nm thick. ILD 3 comprises a 60 nm thick ILD 3-1 SiCN, a 260 nm thick ILD 3-2 oxide, a 52 nm thick ILD 3-3 SiN, and a 370 nm thick ILD 3-4 oxide.



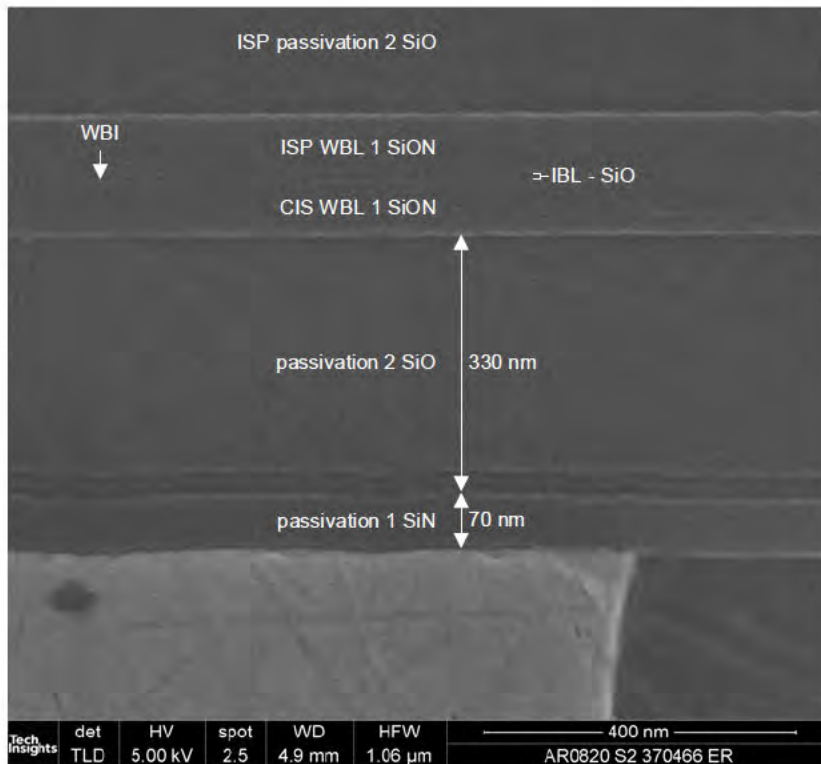
ILD2_35kx_370534.png



ILD3_17.5kx_370534.png

ILD 3 and Metal 4 – TEM

CIS Front Dielectrics and Metals



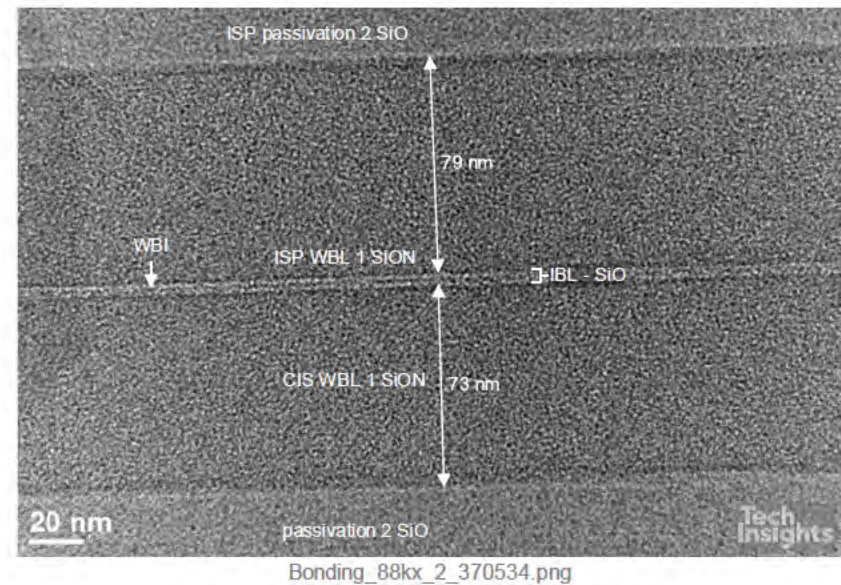
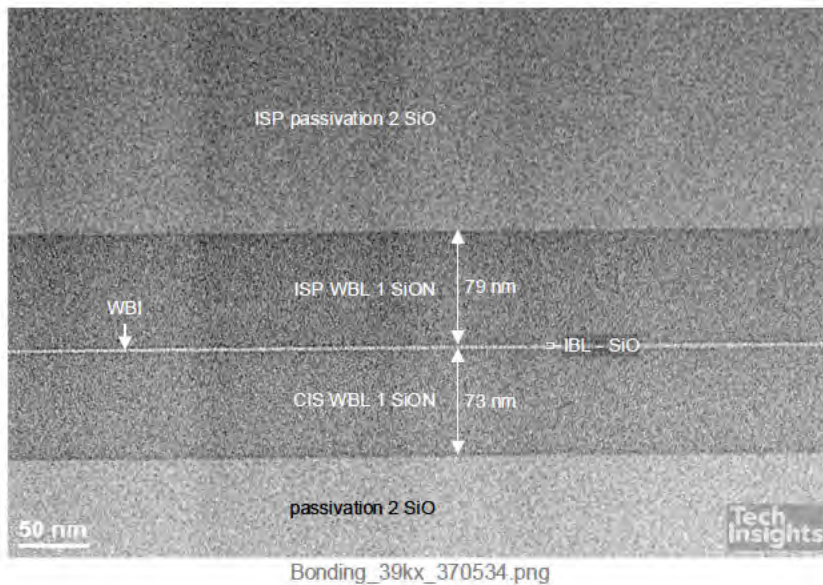
- The passivation comprises a 70 nm thick passivation 1 SiN and a 330 nm thick passivation 2 oxide.

465_CIS_Periphery_Passivation_120K_370466.png

CIS/ISP Hybrid Bonding (DBI)

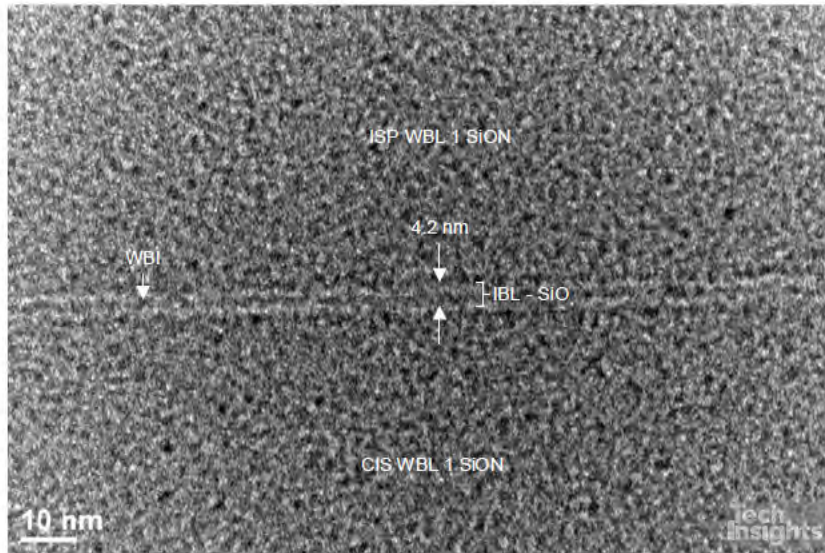
CIS/ISP Hybrid Bonding – Oxide Bonding

- TEM images showing the oxide bonding
- The 73 nm thick CIS WBL 1 SiON and 79 nm thick ISP WBL 1 SiON layers are plasma treated, which causes an increase the number of OH groups at the surface of the SiON layers. After the wafers are bonded together, during the post wafer bonding anneal, the OH bonds break, forming SiO bonds, and consequently a 4.2 nm thick IBL oxide is formed [2].



Oxide Bonding Detailed – TEM

CIS/ISP Hybrid Bonding – Oxide Bonding

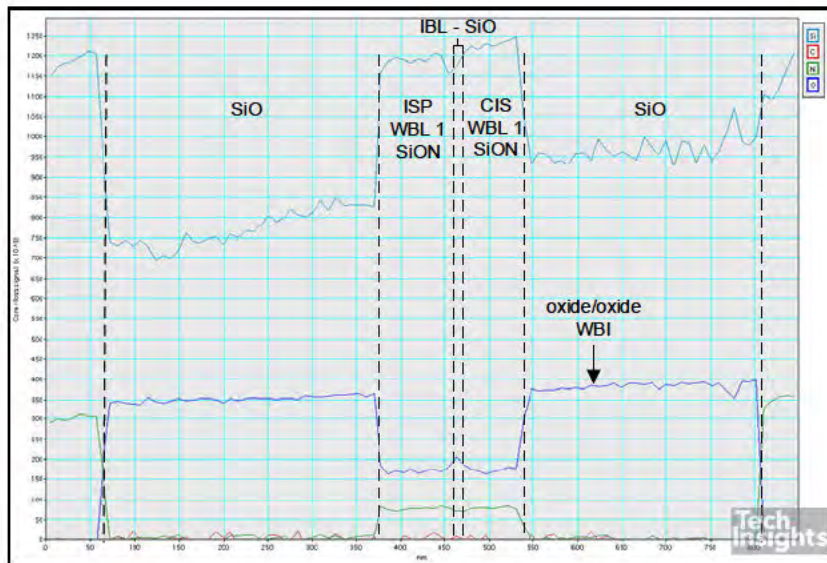


Bonding_180kx_370534.png

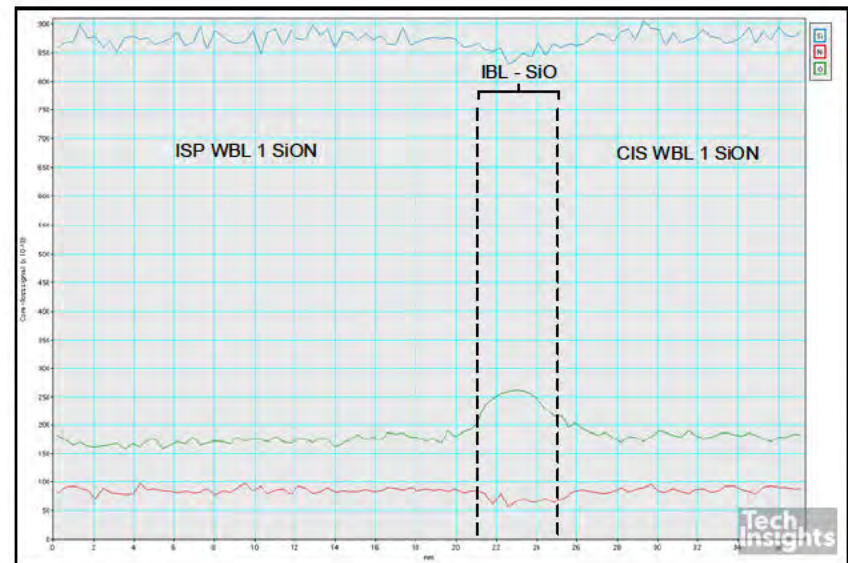
- TEM high-magnification detail image showing the oxide bonding
- The IBL oxide is 4.2 nm thick.

CIS/ISP Hybrid Bonding – Oxide Bonding

- TEM-EELS profiles showing the oxide-oxide bonding
- The overview profile at the wafer bonding interface shows an increase in oxygen and a decrease in silicon, and almost no noticeable drop in nitrogen. However, the detail profile shows an increase in oxygen and a slight decrease in nitrogen; because of the size of the beam and the small thickness of the oxide layer, the nitride does not drop to zero.



Bonding_14.45.04 Edge Profiles_370534.png

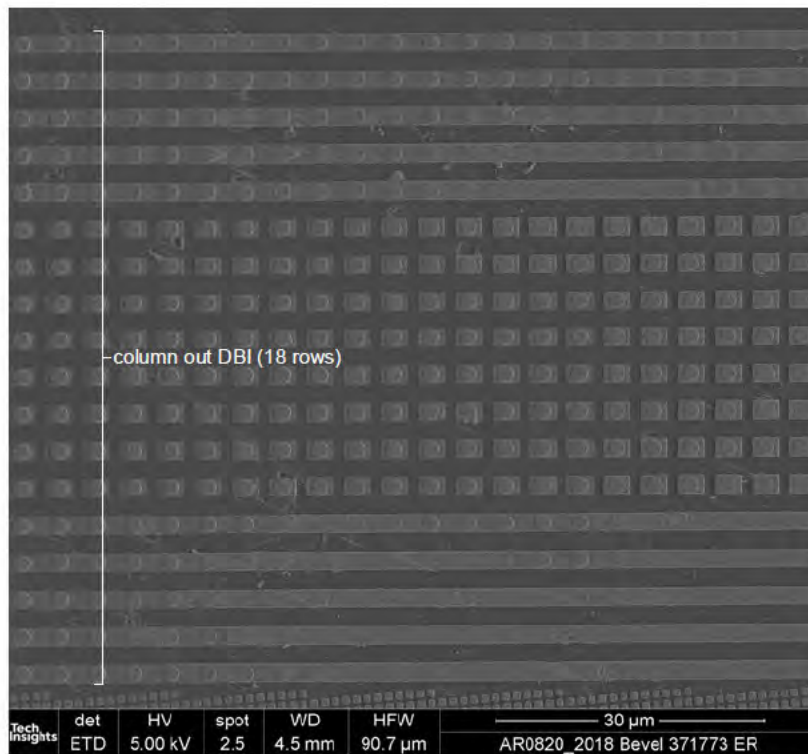


Bonding_14.42.12 Edge Profiles_370534.png

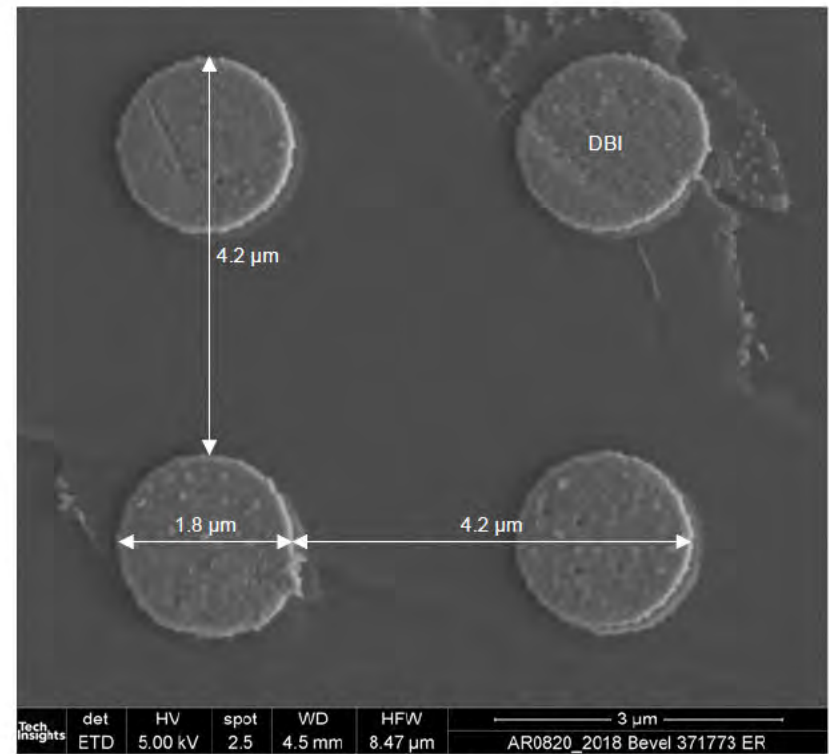
Oxide Bonding Detail – TEM-EELS

CIS/ISP Wafer Hybrid Bonding – Column Out DBI

- SEM plan-view images showing the column out DBI array at the bottom of the pixel array
- There are 18 rows of active column out DBIs.
- The active DBI is circular with a diameter of $1.8\text{ }\mu\text{m}$.
 - Active column out DBIs have horizontal and vertical minimum pitches of $4.2\text{ }\mu\text{m}$.



535_CIS_DBI_Connection_1p4K_371773.png



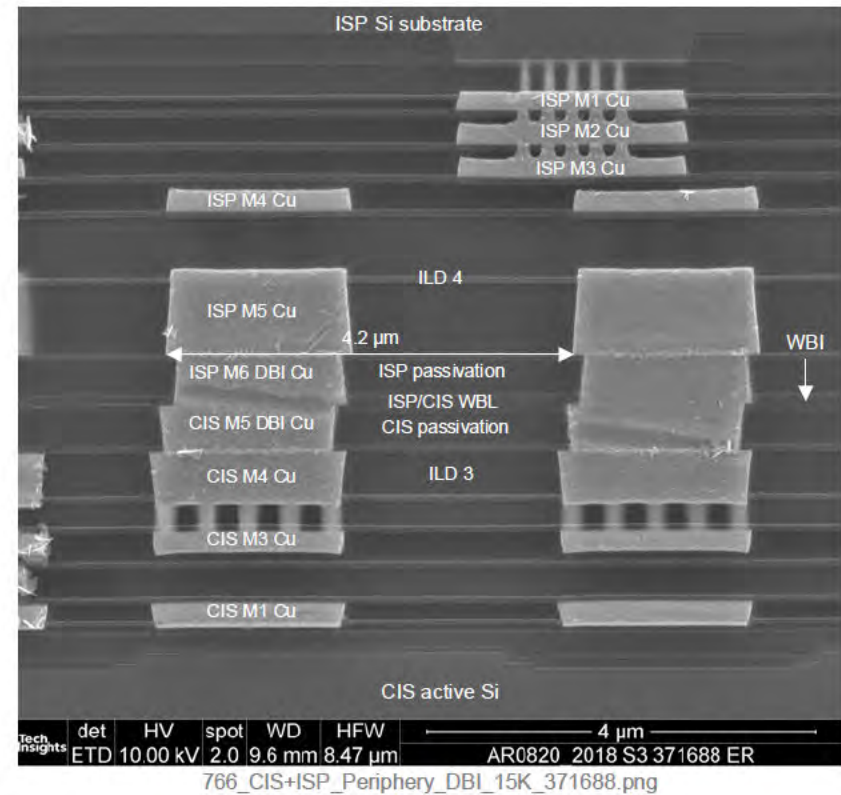
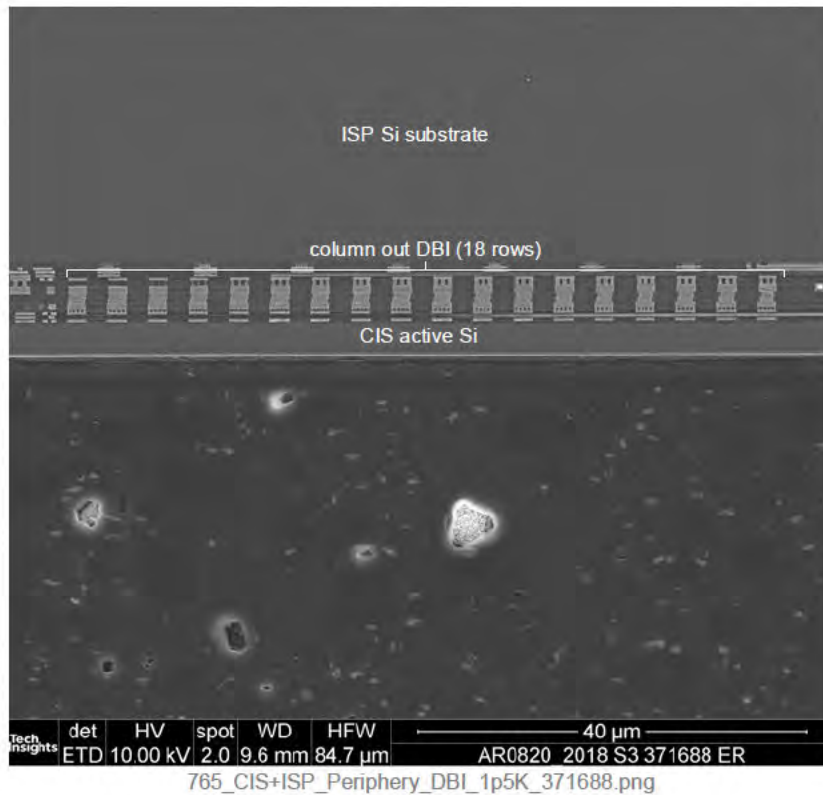
537_CIS+ISP_DBI_Connection_15K_371773.png

Active Column Out DBI Detail – SEM

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Semiconductor v. Greenthread

CIS/ISP Wafer Hybrid Bonding – Column Out DBI

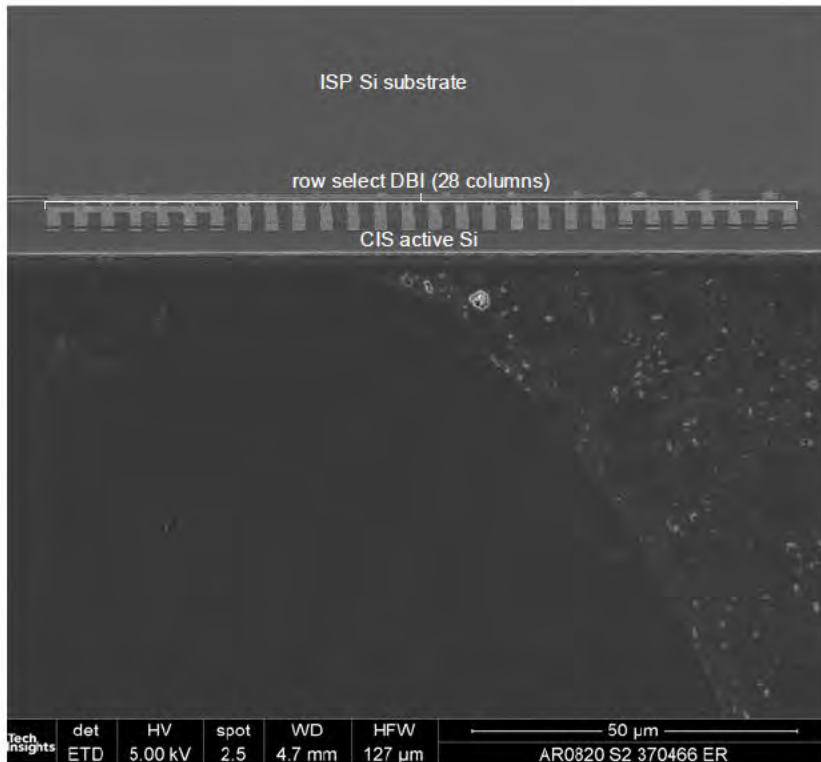
- SEM cross section overview images of the active column and row DBIs
- The active column out DBI array comprises 18 rows.



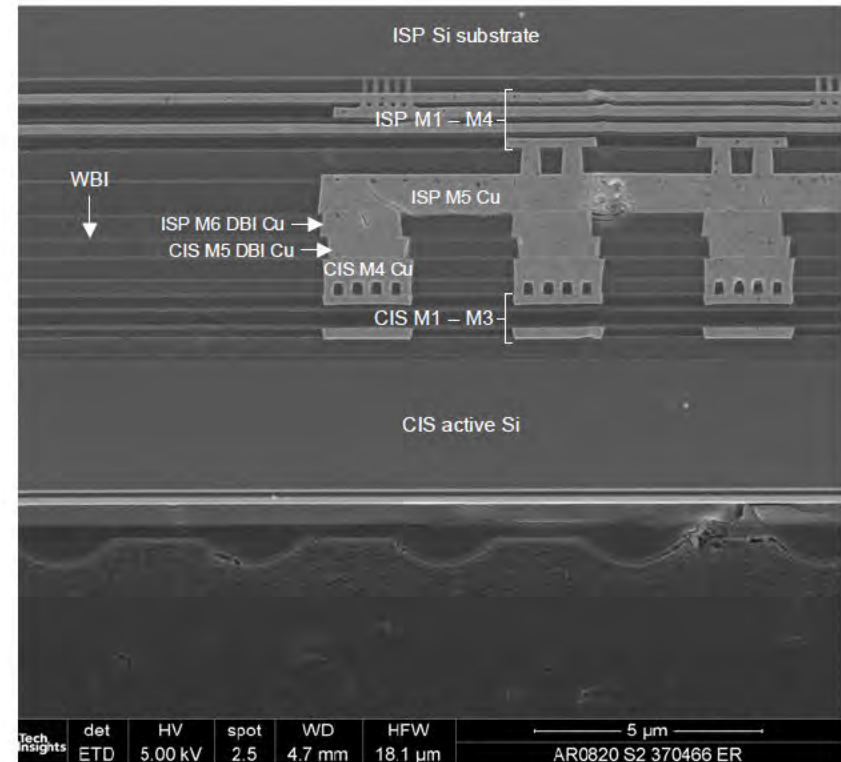
Active Column Out DBI Detail – SEM

CIS/ISP Wafer Hybrid Bonding – Row Select DBI

- SEM cross section overview and detail images of the active row select DBIs
- The active row select DBI array comprises 28 columns.
- The seven columns on each side of the array are connected together.



426_CIS+ISP_Periphery_DBI_Array_1K_370466.png

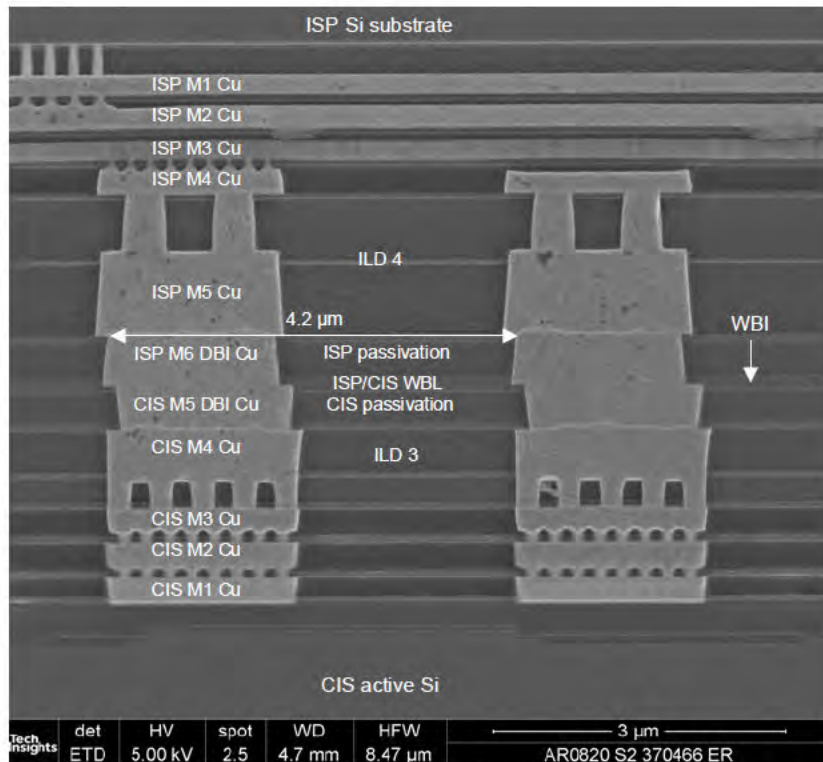


432_CIS+ISP_Periphery_DBI_Array_Edge_7K_370466.png

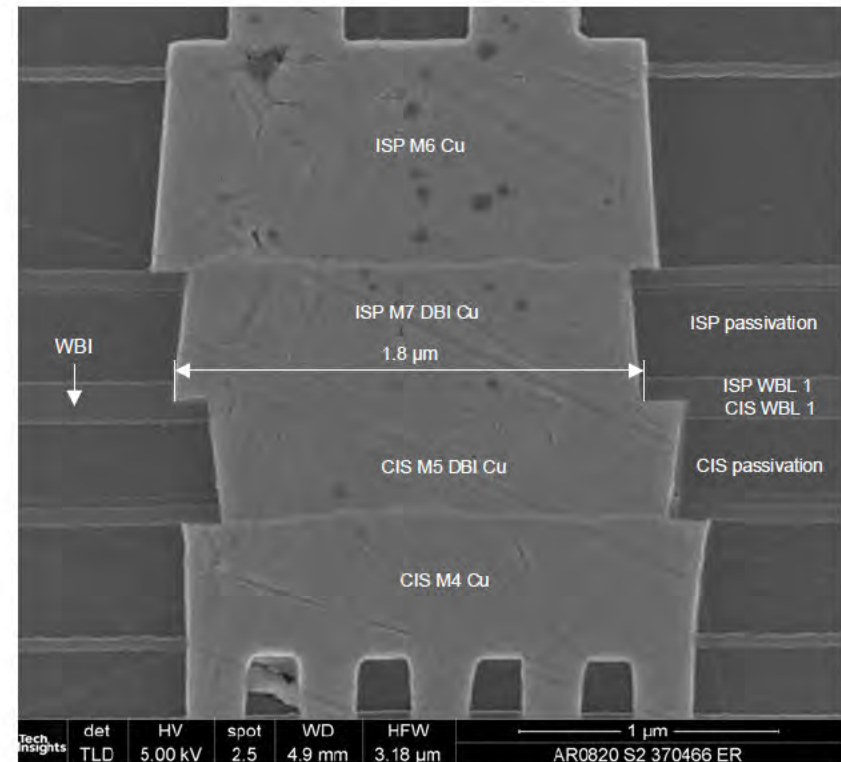
Active Row Select DBI Detail – SEM

CIS/ISP Hybrid Bonding – Row Select DBI

- The hybrid bonding (DBI) electrically connects the CIS and ISP dies. The hybrid bonding is made between the CIS Cu metal 5 and the ISP Cu metal 6, and between the plasma treated CIS WBL 1 SiCN and the ISP WBL 1 SiCN.
- The active row select has a horizontal pitch of 4.2 μm (vertical pitch not measured).



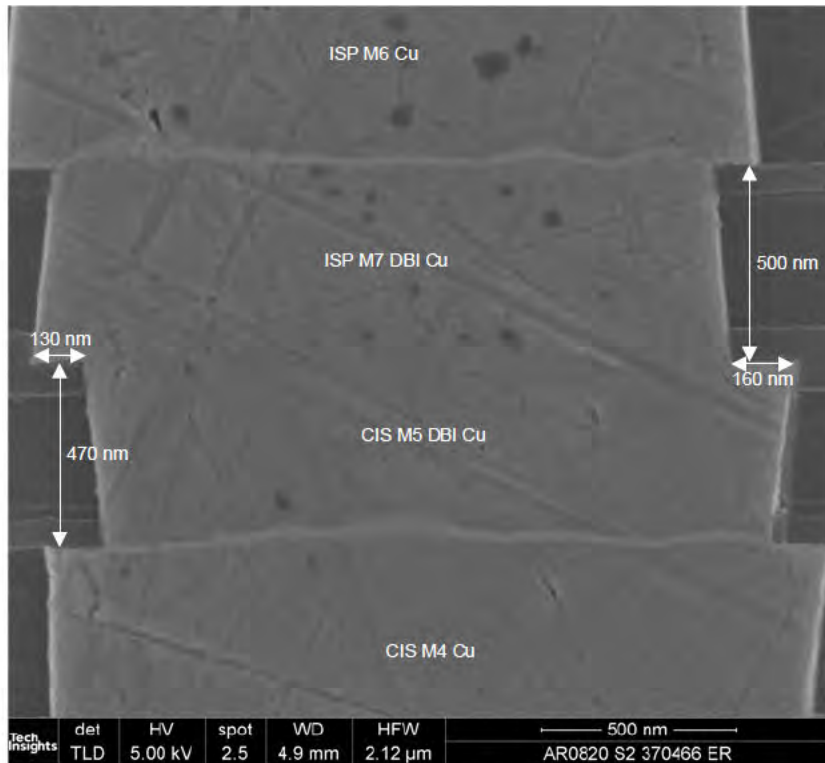
430_CIS+ISP_Periphery_DBI_Array_Middle_15K_370466.png



459_CIS+ISP_Periphery_DBI_40K_370466.png

Active Row Select DBI Detail – SEM

CIS/ISP Hybrid Bonding – Row Select DBI

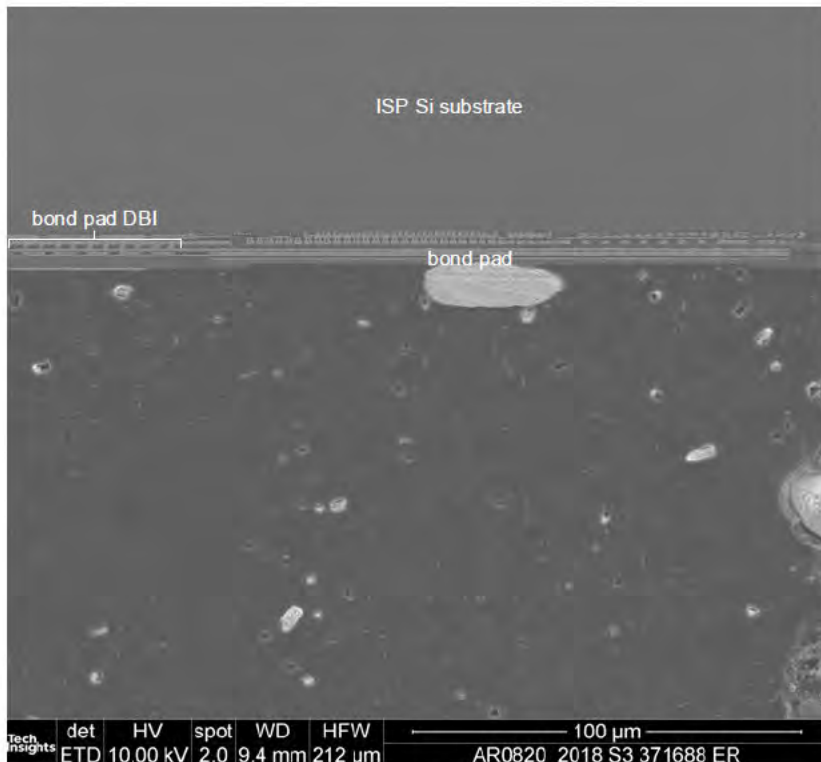


460_CIS+ISP_Periphery_DBI_60K_370466.png

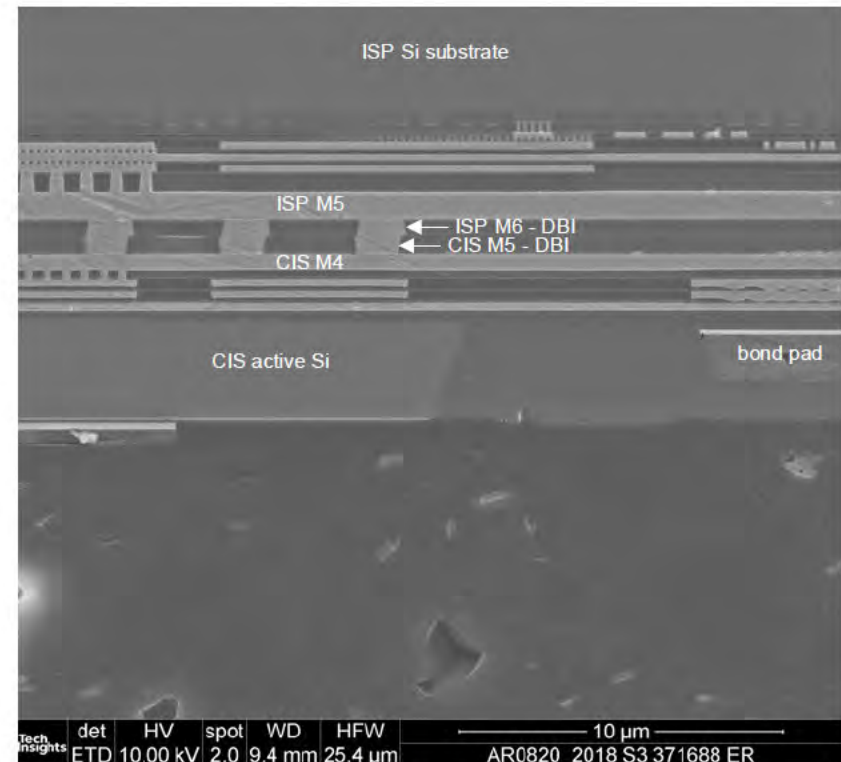
- The ISP metal 6 DBI is 500 nm thick and the CIS Cu metal 5 DBI is 470 nm thick. There is a 130-160 nm misalignment between the two DBIs.

CIS/ISP Hybrid Bonding – Bond Pad DBI

- The CIS bond pad metal stack is connected to the active hybrid bonding (DBI).



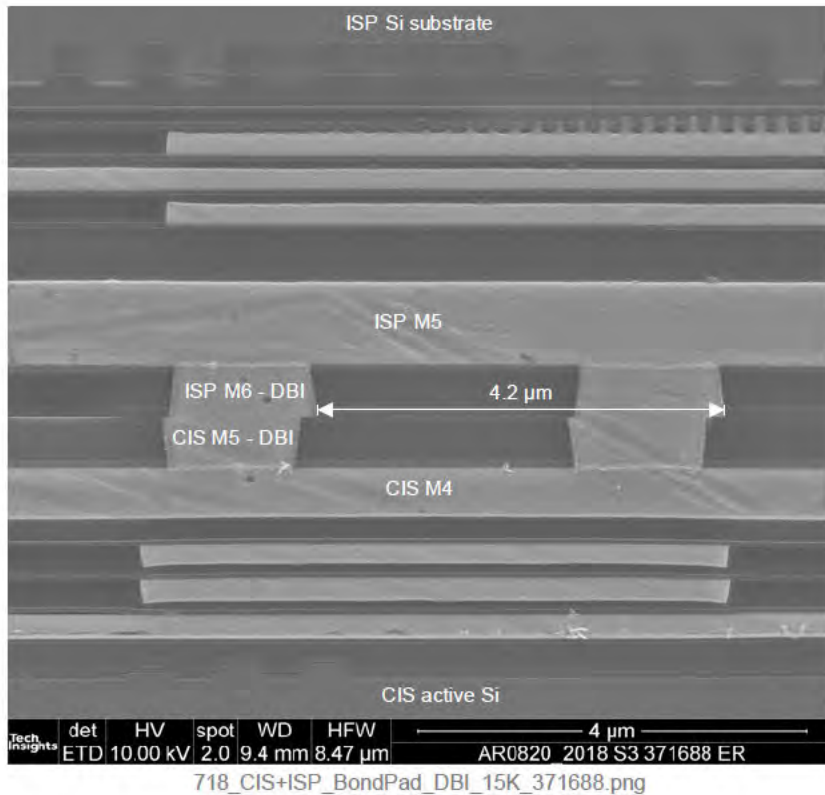
709_CIS+ISP_BondPad_600x_371688.png



713_CIS+ISP_BondPad_Edge_5K_371688.png

Bond Pad DBI Detail – SEM

CIS/ISP Hybrid Bonding – Bond Pad DBI



- The bond pad DBI has a vertical pitch of 4.2 μm .

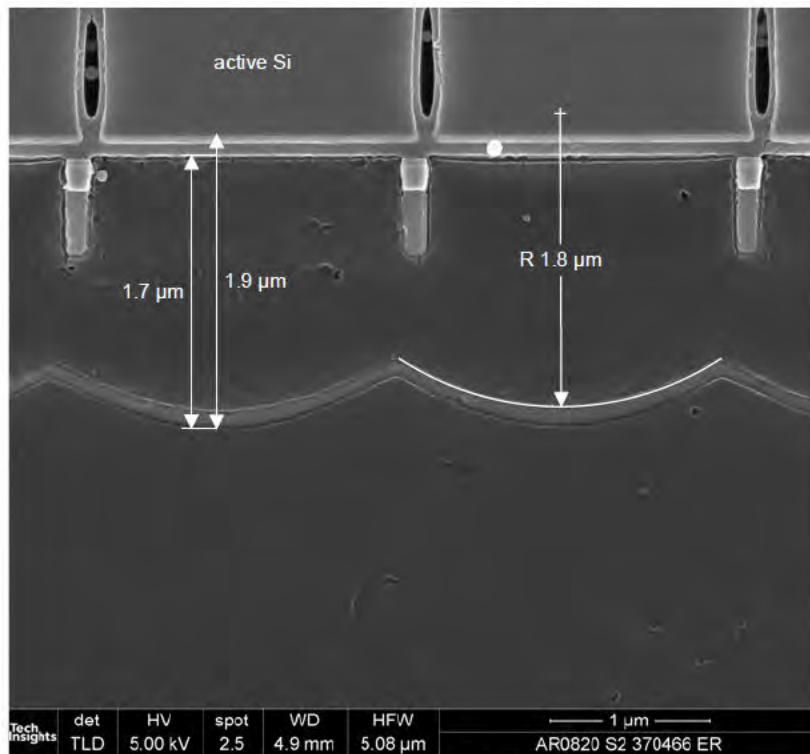
CIS Back Layers

CIS Back Layers Summary

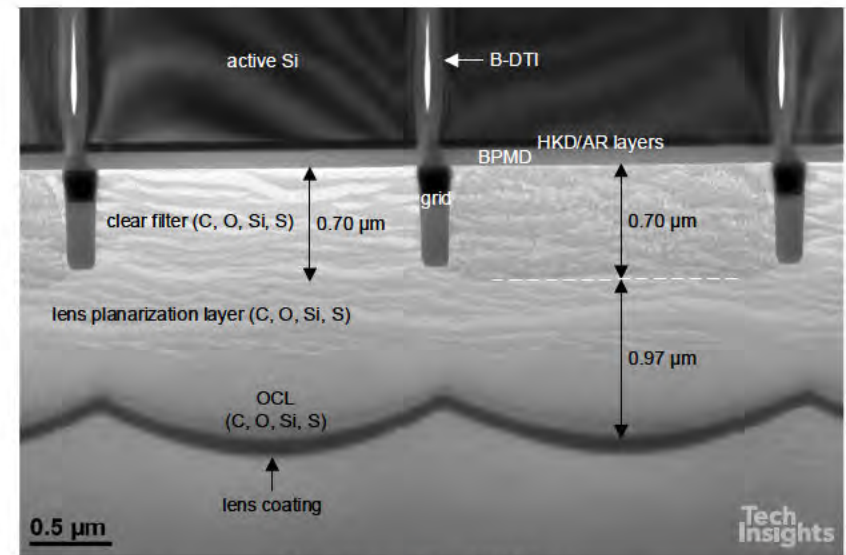
Layer	Composition (Based on TEM-EDS)	Thickness (nm)
High-k dielectric/AR 1	AlO	4.7
High-k dielectric/AR 2	HfO	4.3
High-k dielectric/AR 3	TaO	47
BPMD	SiO	110
CMG/light shield (barrier/metal/dielectric)	TiN/W/SiO	28/160/400
Clear filter	C, O, Si, S	0.70 μm
Other filter	C, O, Si, N, Cl	0.71 μm
Lens buffer	C, O, Si, S	0.24 μm
OCL (including lens planarization layer)	C, O, Si, S	0.96-0.97 μm
Lens coating	SiO	61-87
Organic shield layer	C, Si, O, S	1.1 μm
Microlens radius of curvature	—	0.59 μm
Optical stack	—	1.7 μm

CIS Back Layers – CF and OCL

- SEM and TEM overview images of CIS back layers
- The CFs are embedded (buried) in the grid. The clear filter is $0.70\ \mu\text{m}$ thick and contains C, O, Si, and S. One of the other filters is also $0.70\ \mu\text{m}$ thick.
- The OCL contains C, O, Si, and S, and has an approximate thickness of $0.97\ \mu\text{m}$, including the lens planarization layer. The OCL radius of curvature is $1.8\ \mu\text{m}$.



475_CIS_PixelArray_Color_Filter_Pair_25K_370466.png

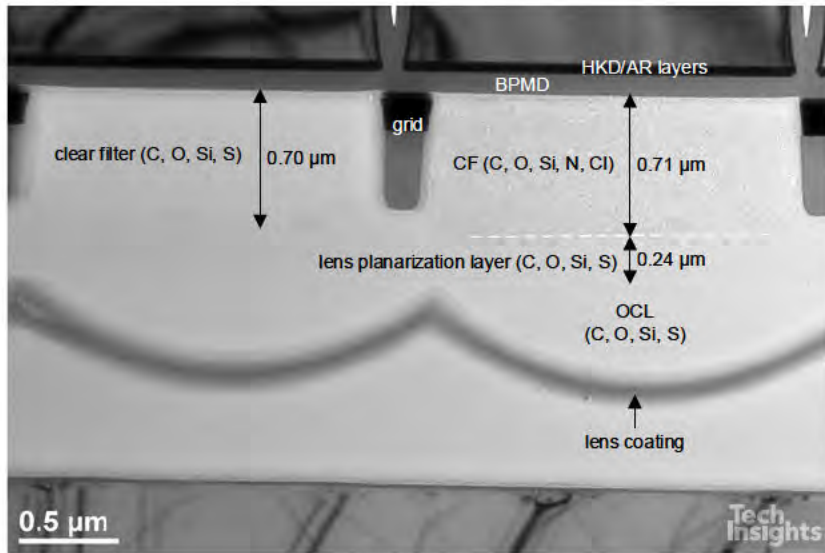


Color_filters_4.5kx_370535.png

Back Layers Overview – TEM

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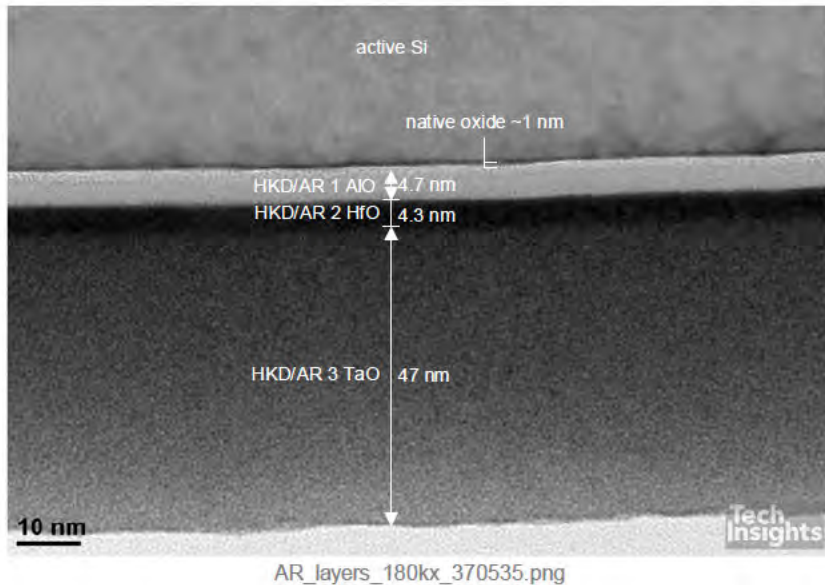
CIS Back Layers – CF and OCL



Lenses_6.3kx_1_370534.png

- TEM overview images of CIS back layers
- One of the other filters is 0.71 μm thick and contains C, O, Si, N, and Cl.
- The OCL is 0.96 μm to 0.97 μm thick, and comprises a 0.24 μm lens planarization layer and the remainder of the thickness is the lens layer.

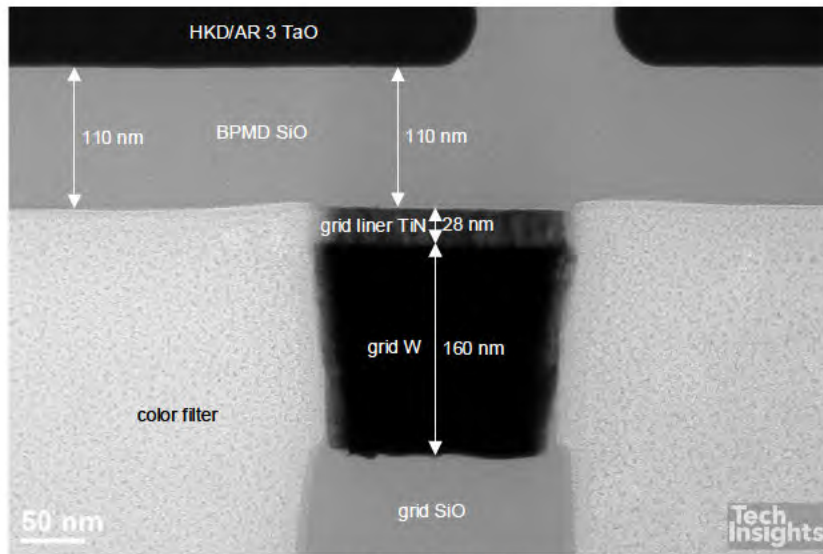
CIS Back Layers – HKD/AR Layers



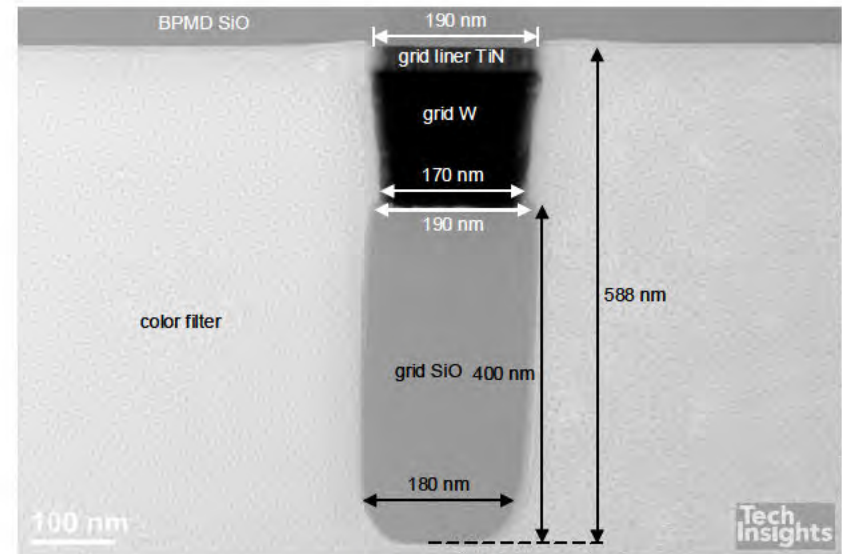
- TEM image showing the HKD/AR layers used to passivate the back of the active Si and B-DTI sidewalls, as well as the BPMD, and grid.
- A HKD/AR layer is deposited on the back of the active Si. It comprises a 4.7 nm thick HKD/AR 1 AlO, a 4.3 nm thick HKD/AR 2 HfO, and a 47 nm thick HKD/AR 3 TaO.

CIS Back Layers – BPMD and CMG

- TEM images showing the BPMD and CMG
- The BPMD is a 110 nm thick oxide.
- The CMG is 588 nm thick and comprises a 28 nm TiN liner, a 160 nm W layer, and a 400 nm thick oxide.



grid_39kx_370534.png

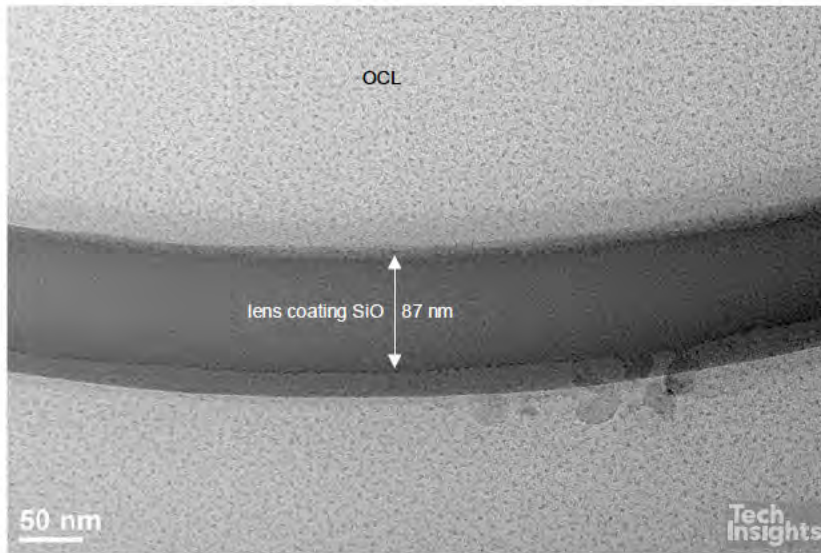


grid_26.5kx_370534.png

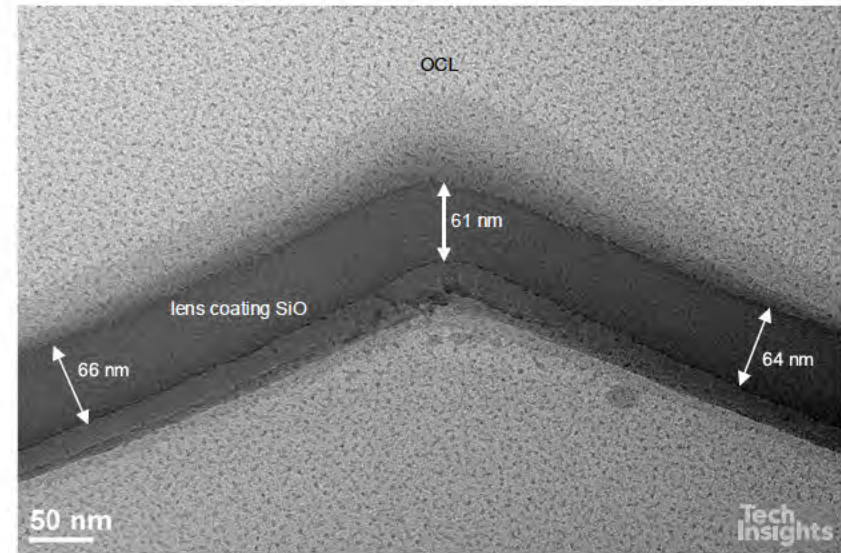
CMG – TEM

CIS Back Layers – Lens Coating

- The OCL coating is a 61 nm to 87 nm thick oxide.

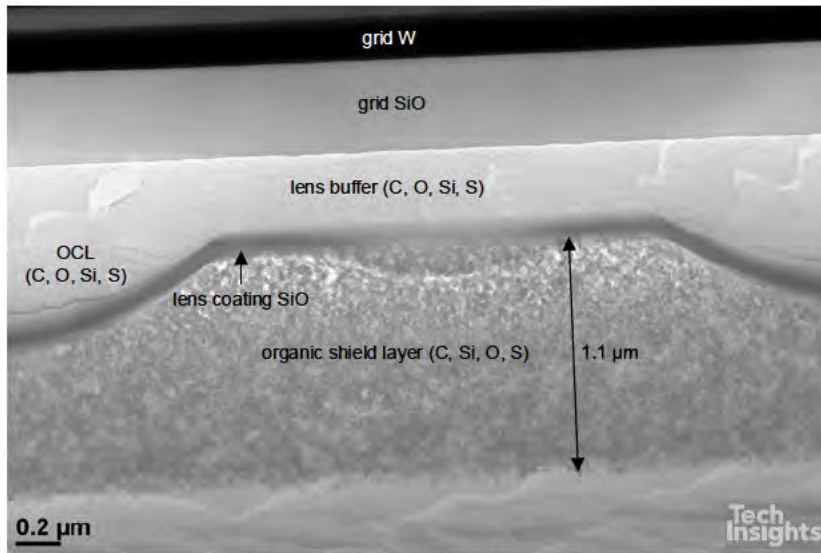


Lens_39kx_370534.png



Lens_39kx_1_370534.png

CIS Back Layers – Organic Shield Layer



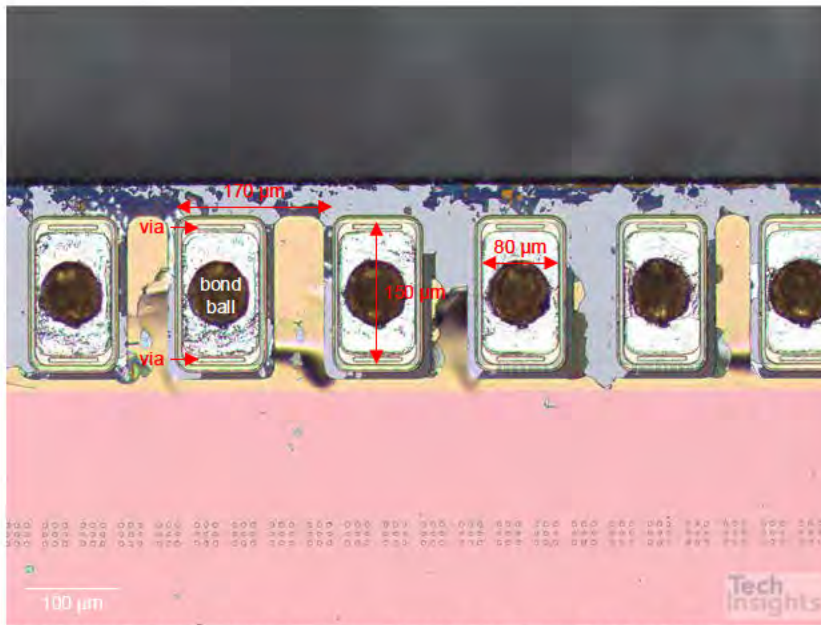
Lens_periphery_6.3kx_370535.png

- The periphery region is covered with a 1.1 μm thick organic shield layer containing C, Si, O, and S.

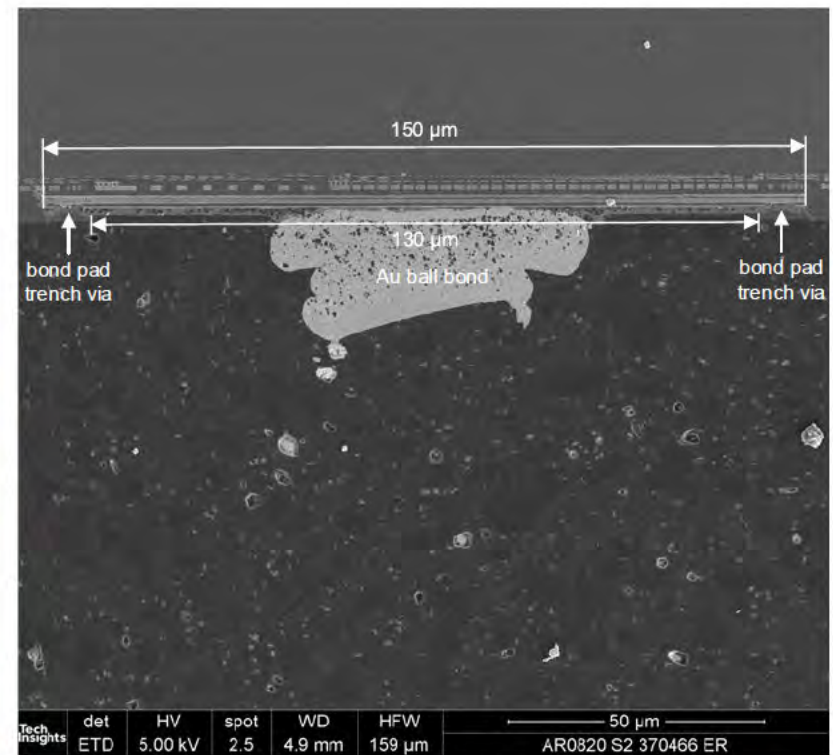
CIS Bond Pad

Bond Pad

- The bond pad has a pitch of 170 μm and is formed in a 150 μm long x 80 μm wide window, which penetrates the CIS active Si and pad oxide.
- The bond pad opening (exposed Al) is 130 μm long, and it is isolated from the CIS active Si by a dielectric layer.



LI-AR0820-GMSL2_060H_Front-Cam_AR0820_2018_CIS_371697_BondPads.png



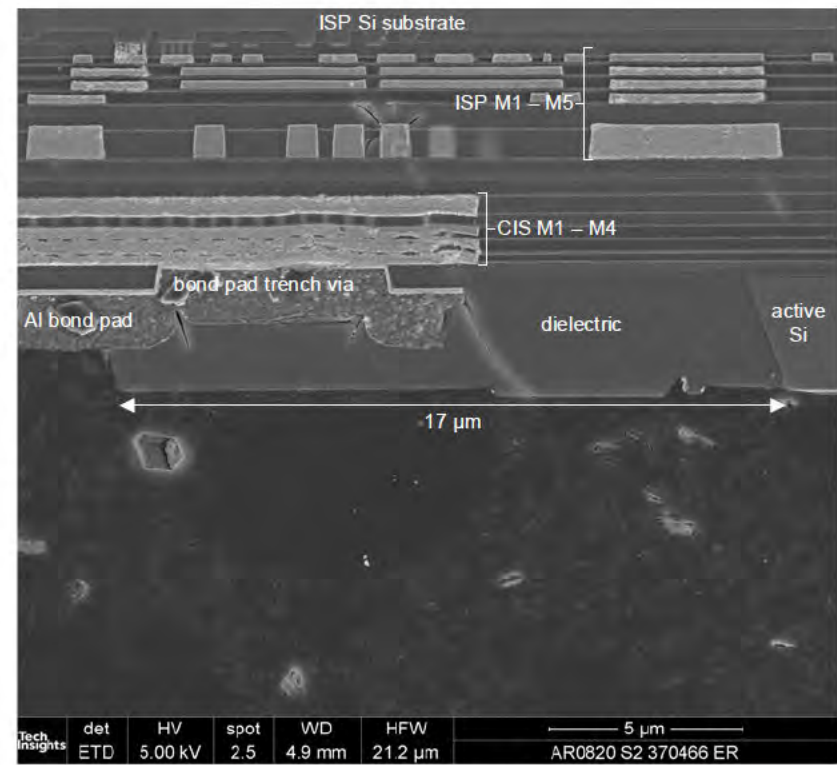
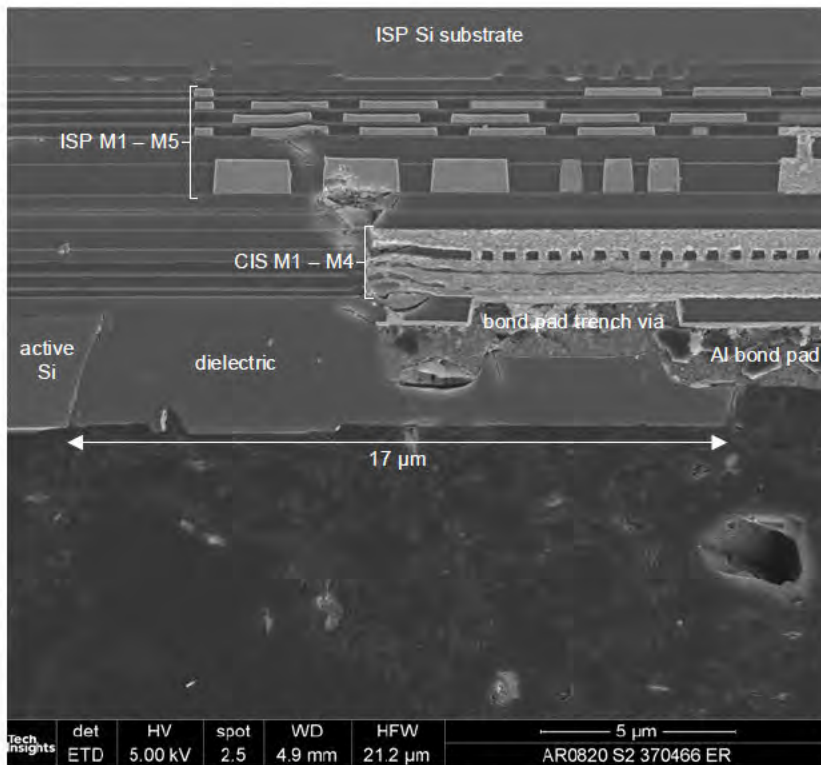
449_CIS+ISP_BondPad_800x_370466.png

Bond Pad Overview – SEM Cross Section

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Bond Pad

- The bond pad comprises an Al layer with top and bottom barrier layers and two trench vias.
- The trench vias connect the bond pad to CIS metal 1 to metal 4 stack
- Dielectric layers isolate the bond pad from the active Si



Bond Pad Overview – SEM Cross Section

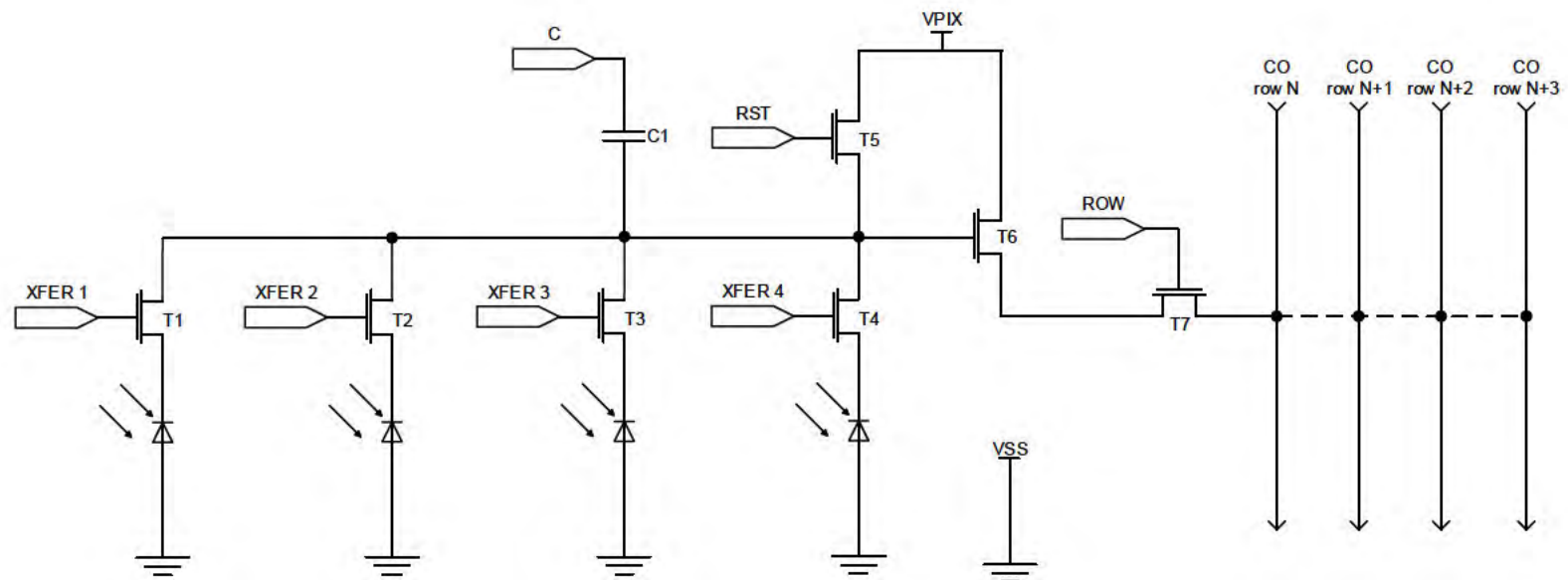
Greenthread Ex 2020, p. 193
Semiconductor v. Greenthread

CIS Pixel Analysis

Pixel Schematic

our-shared pixel architecture (2×2 pixel configuration) with seven transistors per four pixels, yielding 1.75T effective per pixel, plus an in-pixel poly MOS capacitor, giving a shared-pixel footprint of two rows and two columns.

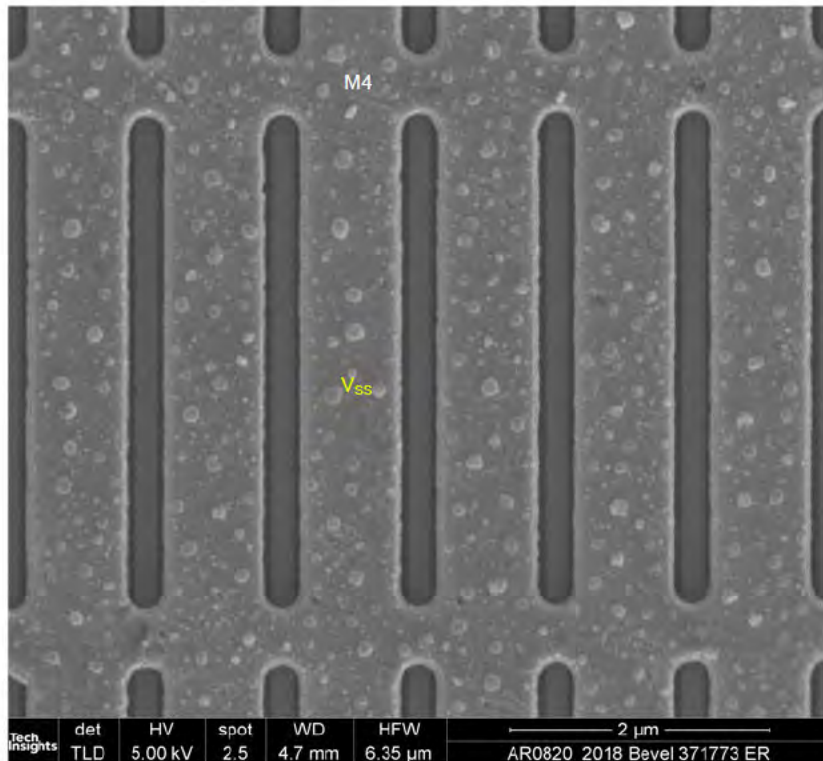
Pixel Schematic



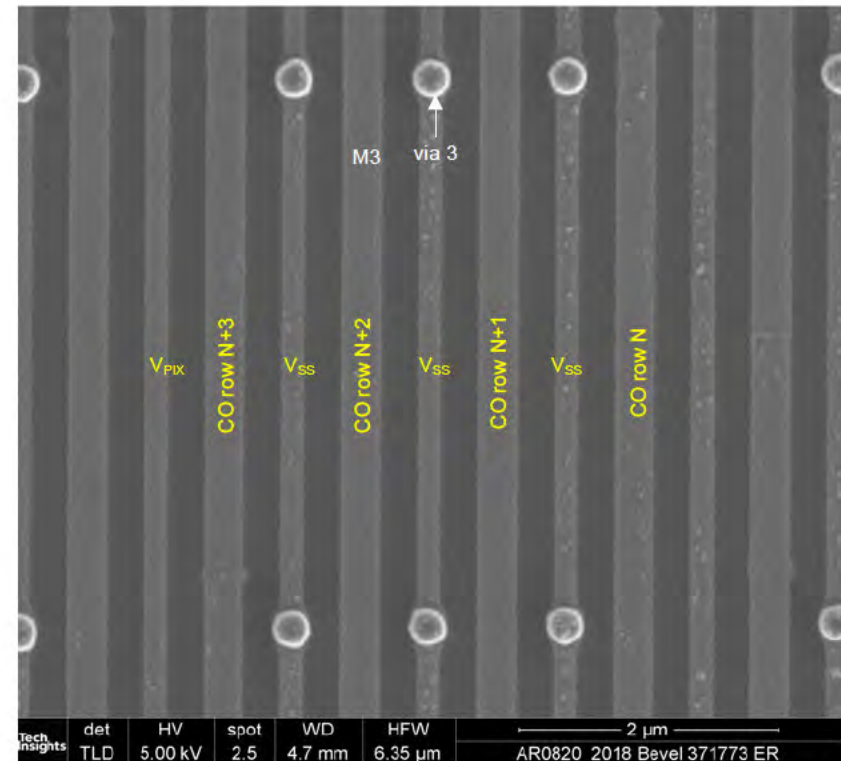
CIS Plan-View Analysis

Pixel Planar Analysis

- Metal 4 forms a grid connected to V_{SS} over the pixel array.
- Metal 3 comprises metal lines running vertically over the pixel array. Metal 3 is used for the CO, V_{PIX} , and V_{SS} lines.



550_CIS_PixelArray_M4_20K_371773.png

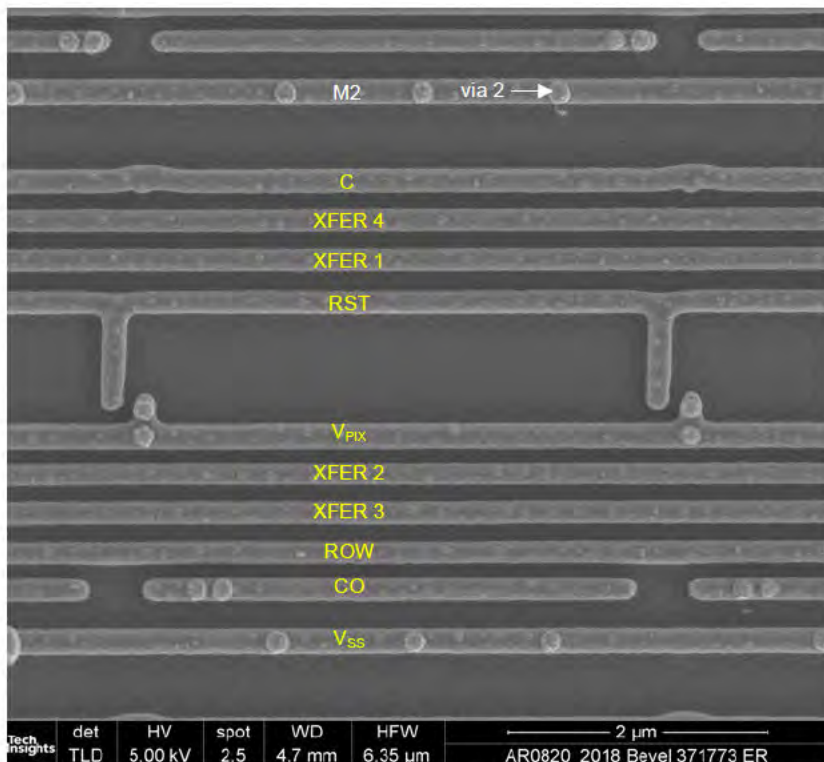


549_CIS_PixelArray_M3_Via3_20K_371773.png

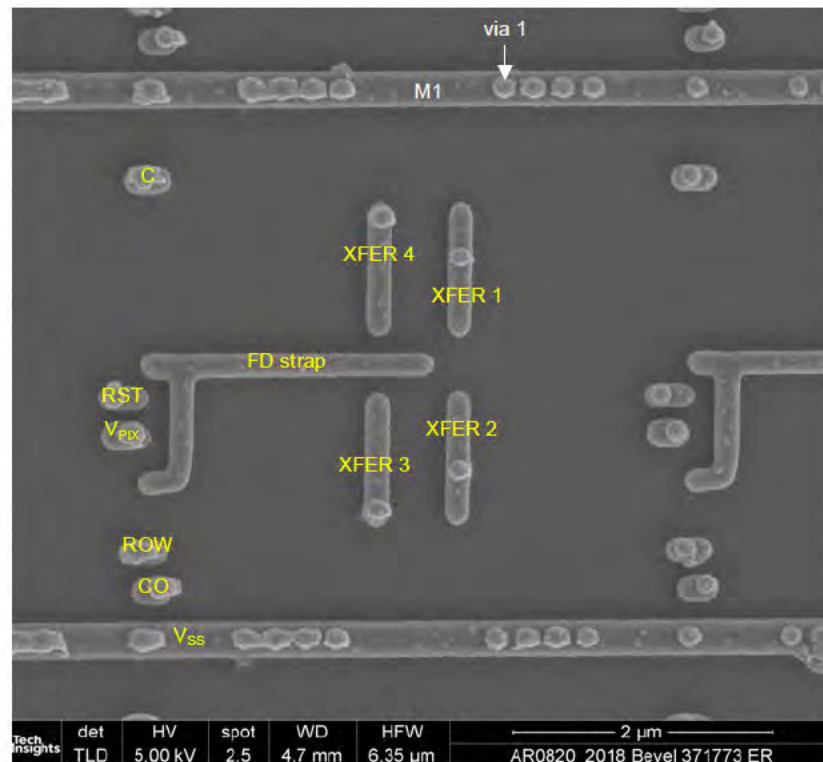
Pixel at Metal 3 – SEM

Pixel Planar Analysis

- Single and multiple via 2s and single via 1s are used for pixel interconnect.
- Metal 2 is used for XFER 1, XFER 2, XFER 3, XFER 4, V_{SS} , V_{PIX} , RST, ROW, and C lines, as well as for CO lands.
- Metal 1 is used for XFER 1, XFER 2, XFER 3, XFER 4, V_{PIX} , RST, ROW and CO lands, and FD strap and V_{SS} lines.



547_CIS_PixelArray_M2_Via2_20K_371773.png

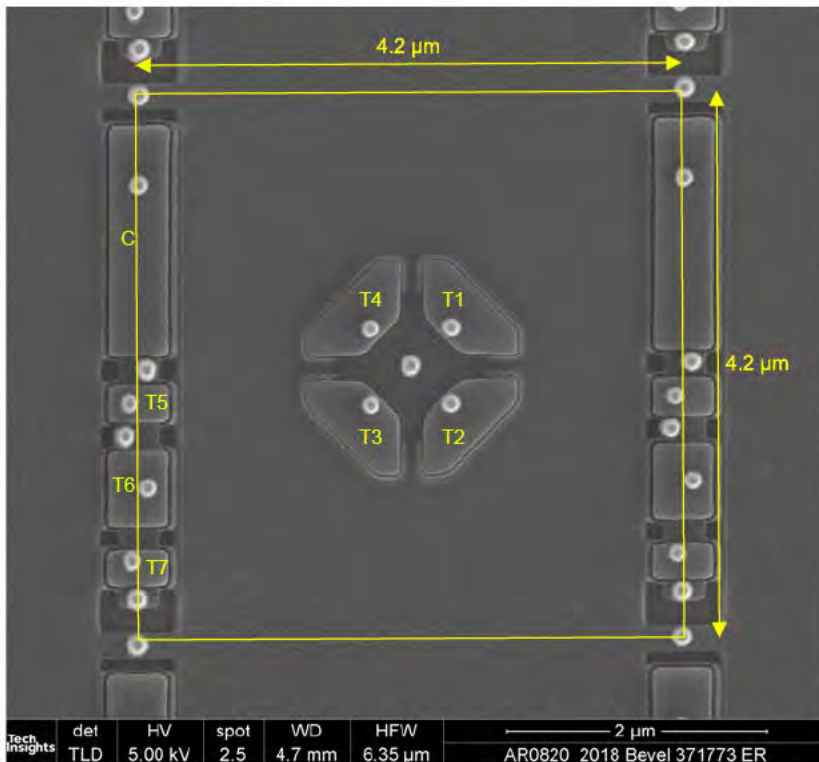


545_CIS_PixelArray_M1_Via1_20K_371773.png

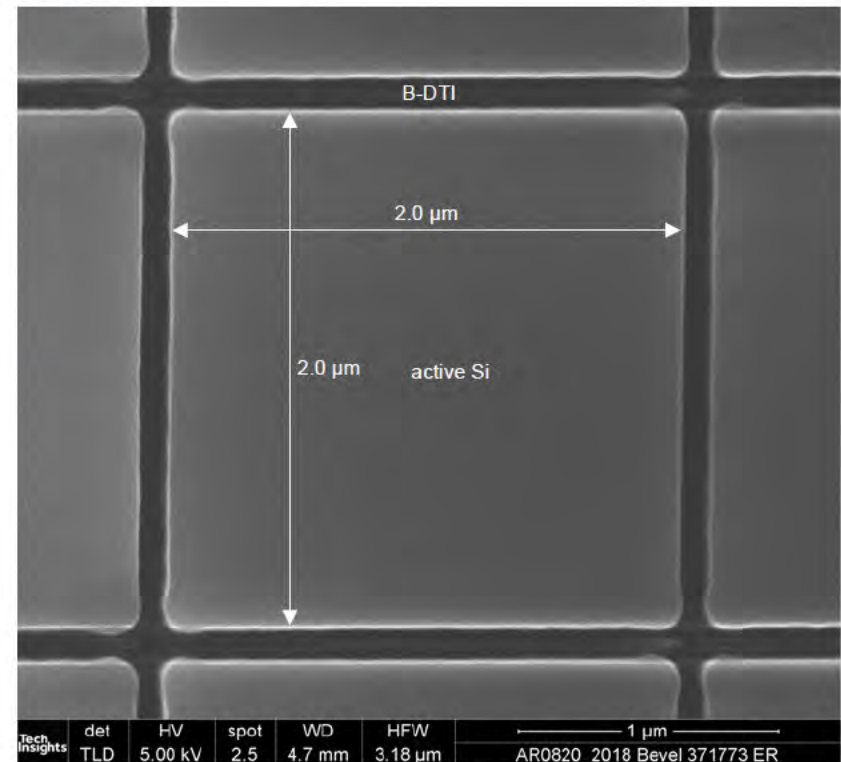
Pixel at Metal 1 and Via 1 – SEM

Pixel Planar Analysis

- The pixel at poly and contact shows single contacts to all pixel transistors.
- The pixel size is $2.1\text{ }\mu\text{m} \times 2.1\text{ }\mu\text{m}$. The four-shared pixel has a footprint of $4.2\text{ }\mu\text{m} \times 4.2\text{ }\mu\text{m}$. The yellow rectangle shows the four-shared pixel boundary.
- The pixel active Si inside the B-DTI grid is about $2.0\text{ }\mu\text{m} \times 2.0\text{ }\mu\text{m}$.



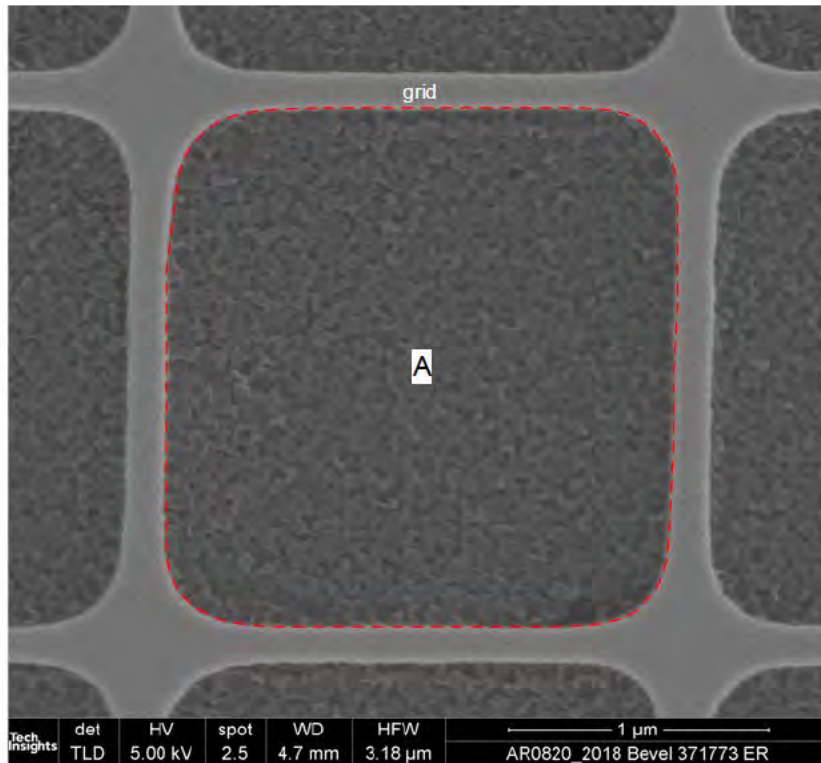
543_CIS_PixelArray_Poly_20K_371773.png



566_CIS_PixelArray_Substrate_B-DTI_40K_371773.png

B-DTI Grid – SEM Plan View

Pixel Planar Analysis

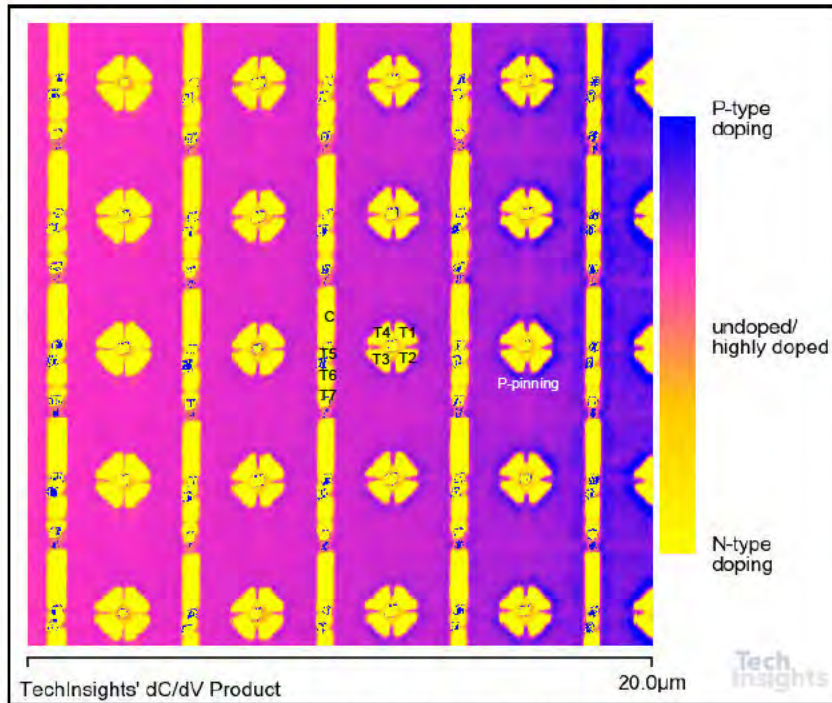


569_CIS_PixelArray_Grid_40K_371773.png

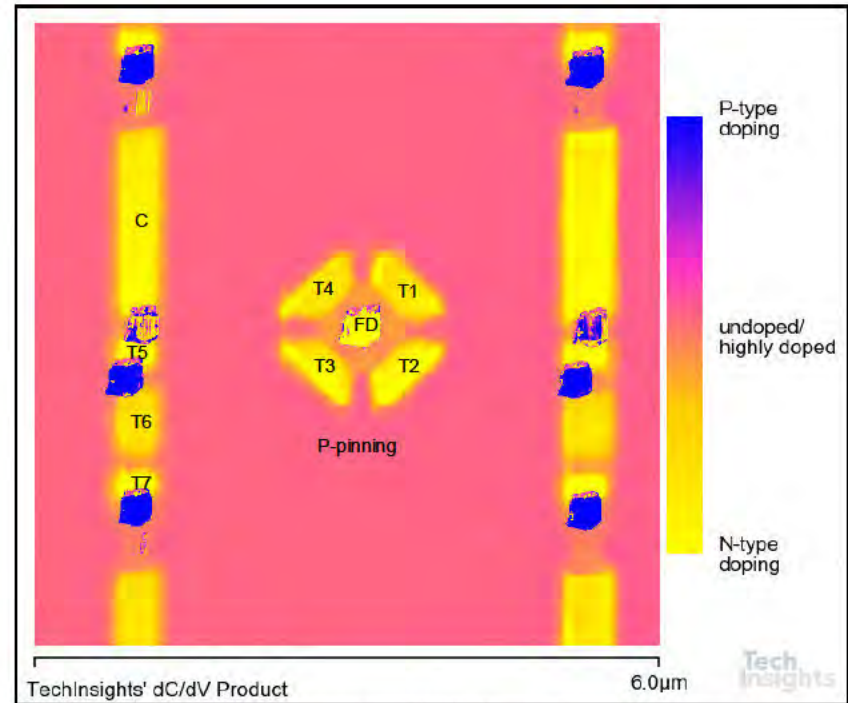
- The grid aperture has an approximate area (A, red dashed line) of $3.794 \mu\text{m}^2$, corresponding to a fill factor of ~86% ($3.794/[2.1]^2$).

Pixel Planar Analysis

- SCM overview and detail images of the pixel near the active Si surface, showing the transistor gates and P-pinning layer



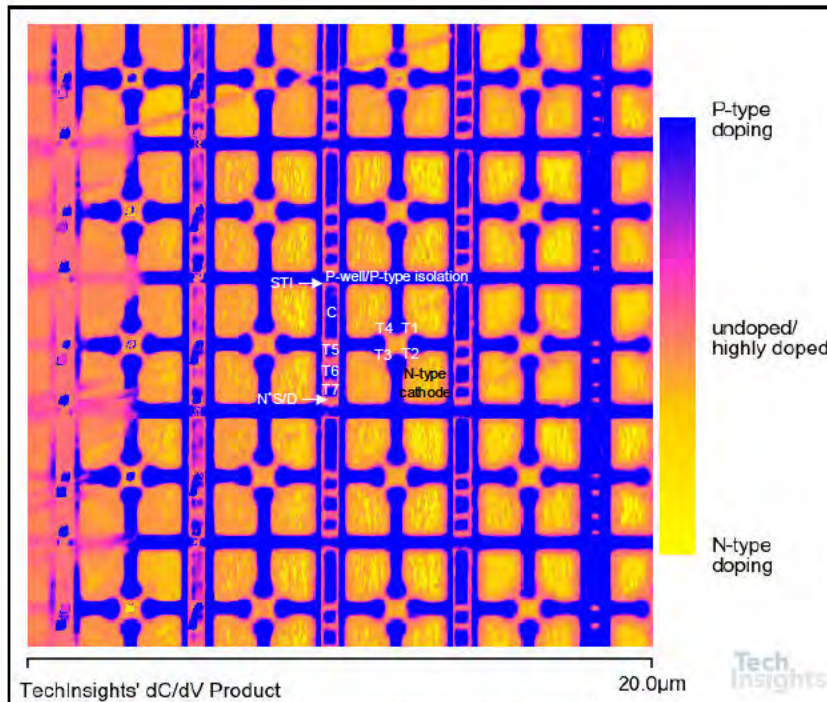
Pixel at the Active Si Surface Overview – Planar SCM



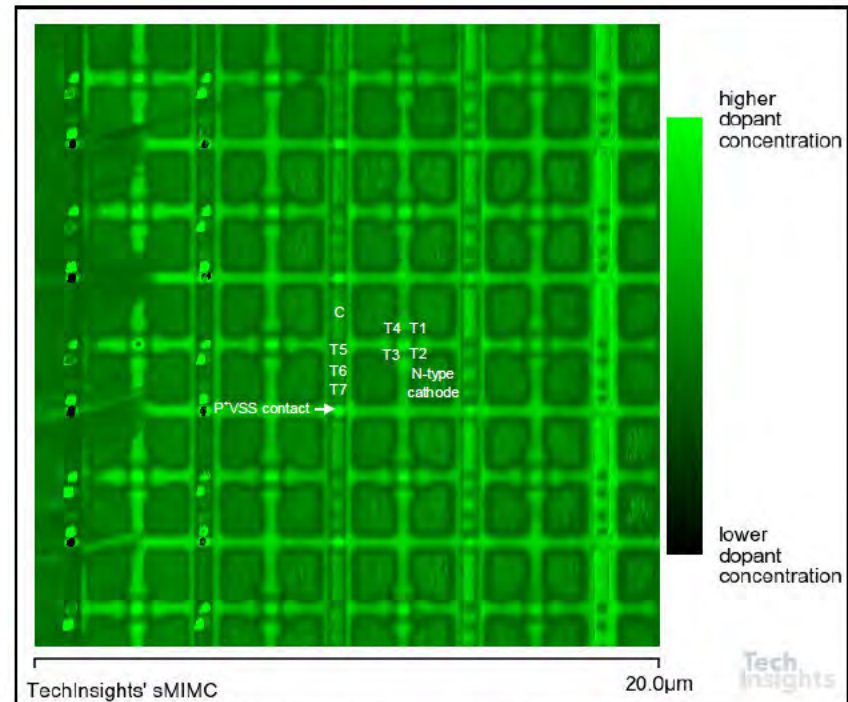
Pixel at the Active Si Surface Detail – Planar SCM

Pixel Planar Analysis

- The SCM and sMIM-C images show the pixel below the active Si surface. The N-type photocathodes, STI, and P-type pixel isolation regions are visible.



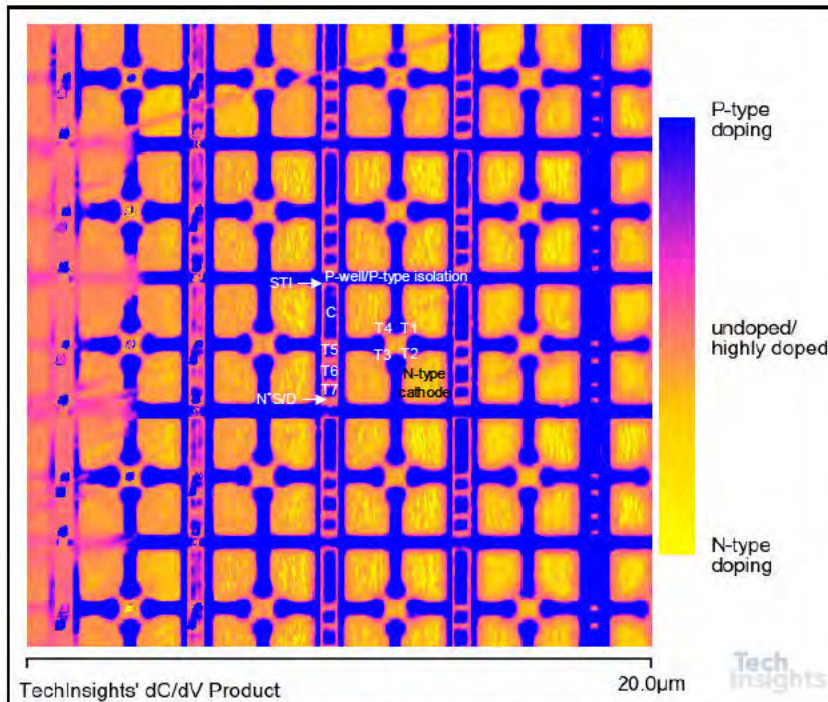
Pixel Below S/D Regions – Planar SCM



Pixel Below S/D Regions – Planar sMIM-C

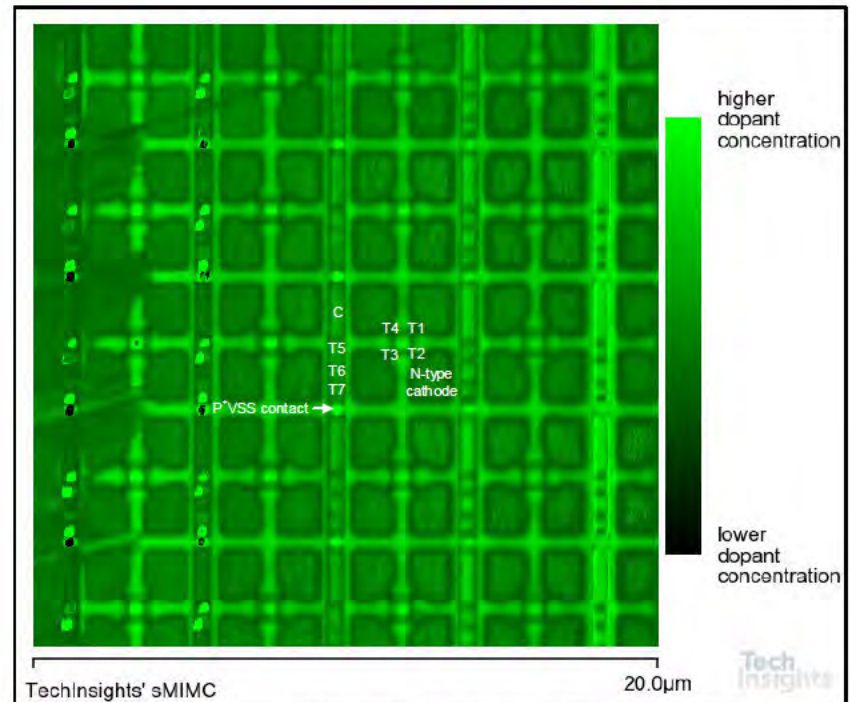
Pixel Planar Analysis

- The SCM and sMIM-C images show the pixel at the S/D regions. The N-type photocathodes, STI, and P-type pixel isolation regions are visible.



0715201204_PRODUCT_FRW_20.0u_512p_371773.png

Pixel at the S/D Regions Overview – Planar SCM

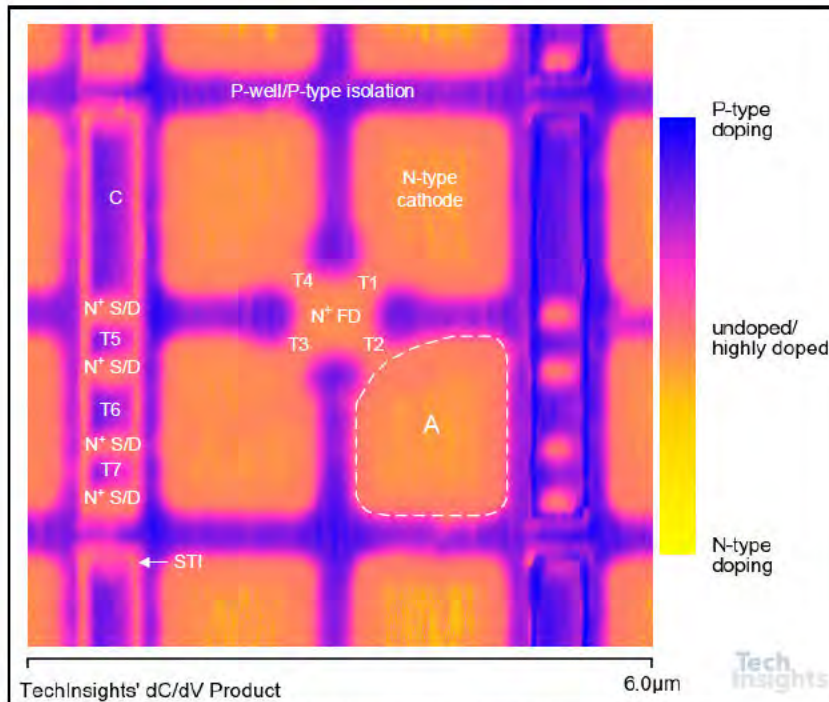


0715201204_SMIMC_FRW_20.0u_512p_371773.png

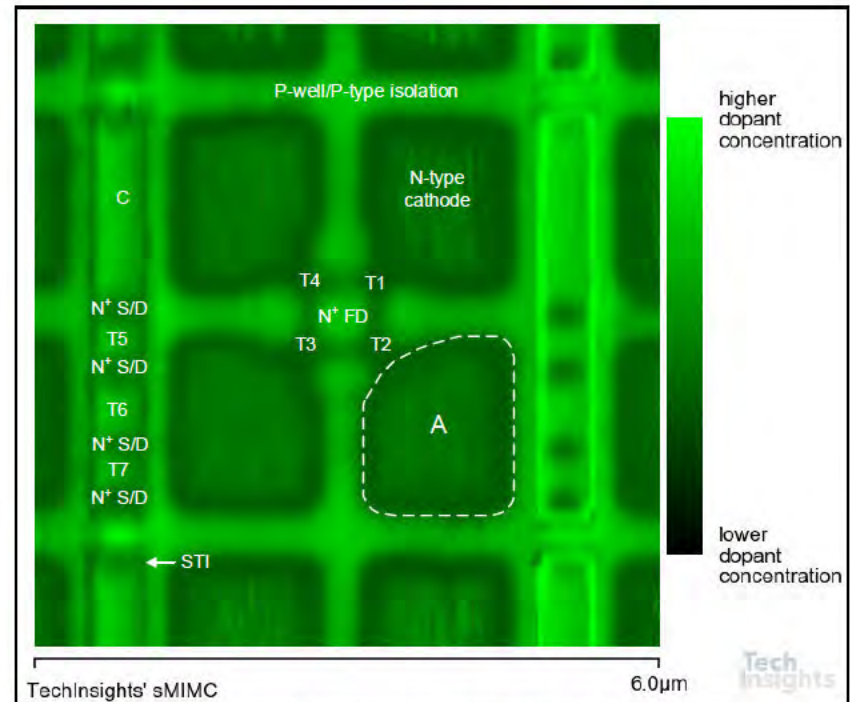
Pixel at the S/D Regions Overview – Planar sMIM-C

Pixel Planar Analysis

- The SCM and sMIM-C images show the pixel at the S/D regions. The N-type photocathodes, STI, and P-type pixel isolation regions are visible.
- The area of the N-type cathode is approximately $2.38 \mu\text{m}^2$.



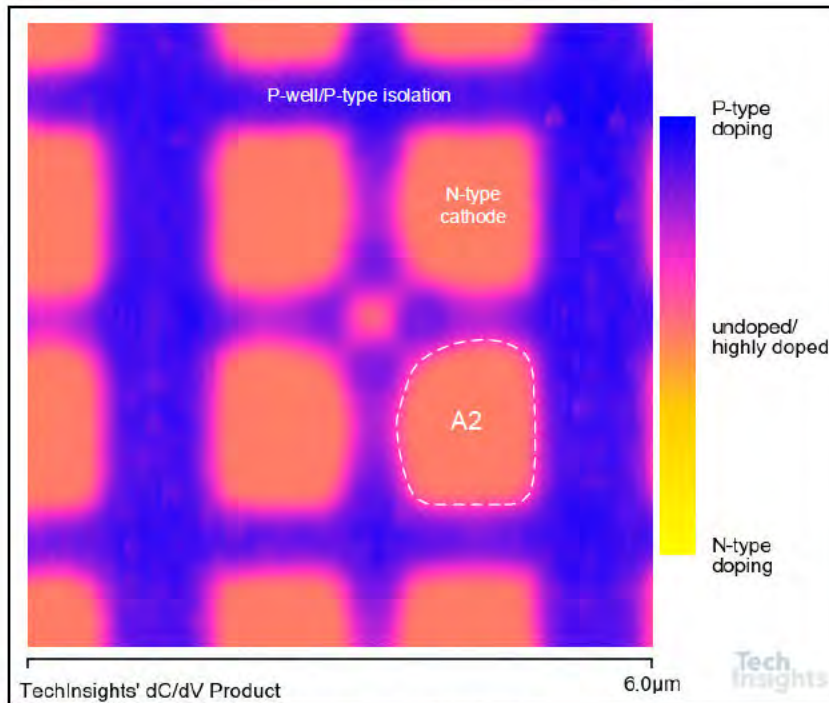
Pixel at the S/D Regions Detail – Planar SCM



Pixel at the S/D Regions Detail – Planar sMIM-C

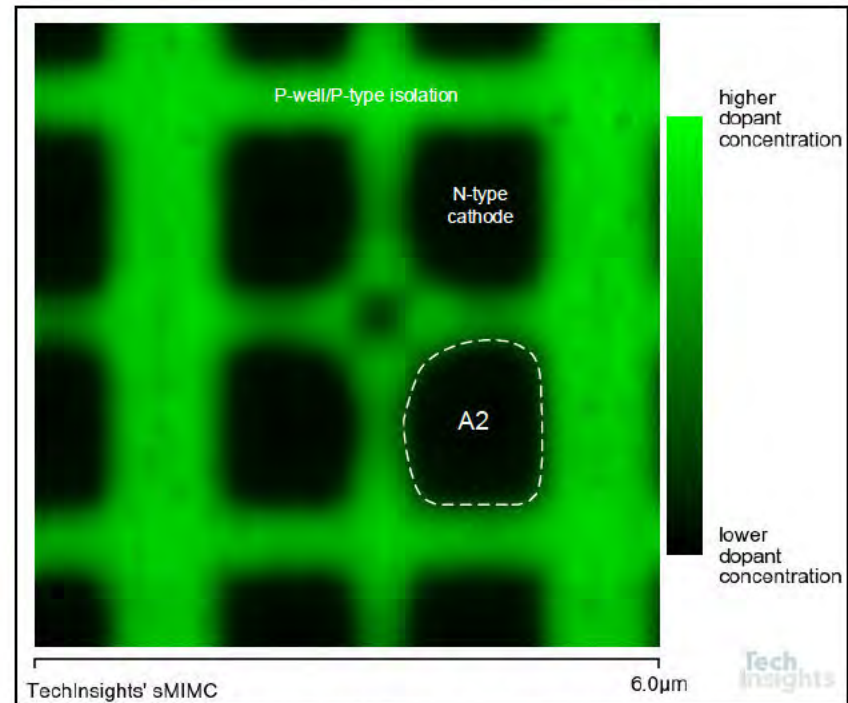
Pixel Planar Analysis

- SCM and sMIM-C images of the photocathodes before the start of the B-DTI
- The N-type photocathode has an approximate area of $1.94 \mu\text{m}^2$.



0716201217_PRODUCT_FRW_6.0u_512p_371773.png

Pixel Before the Start of B-DTI – Planar SCM

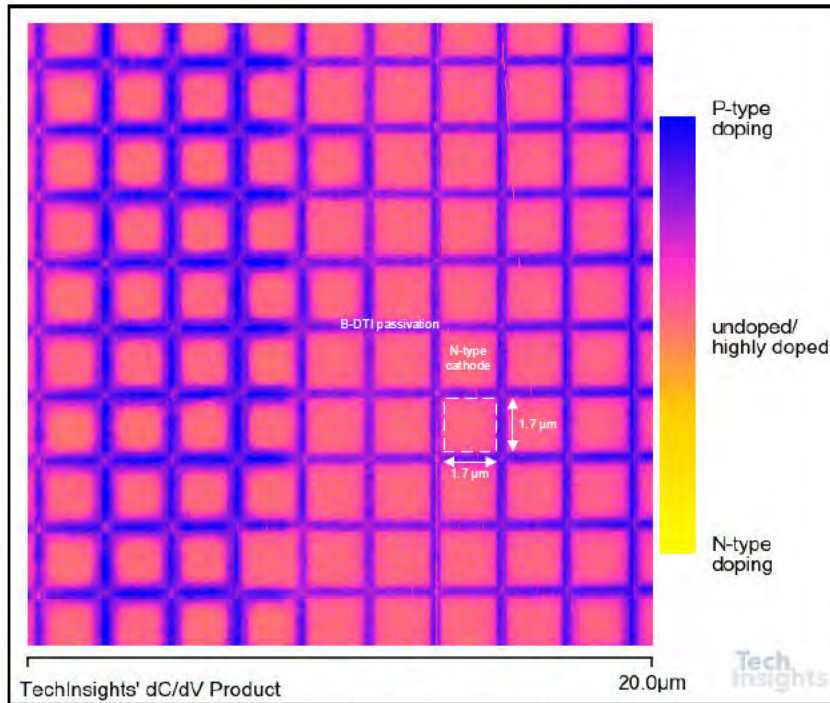


0716201217_SMIMC_FRW_6.0u_512p_371773.png

Pixel Before the Start of B-DTI – Planar sMIM-C

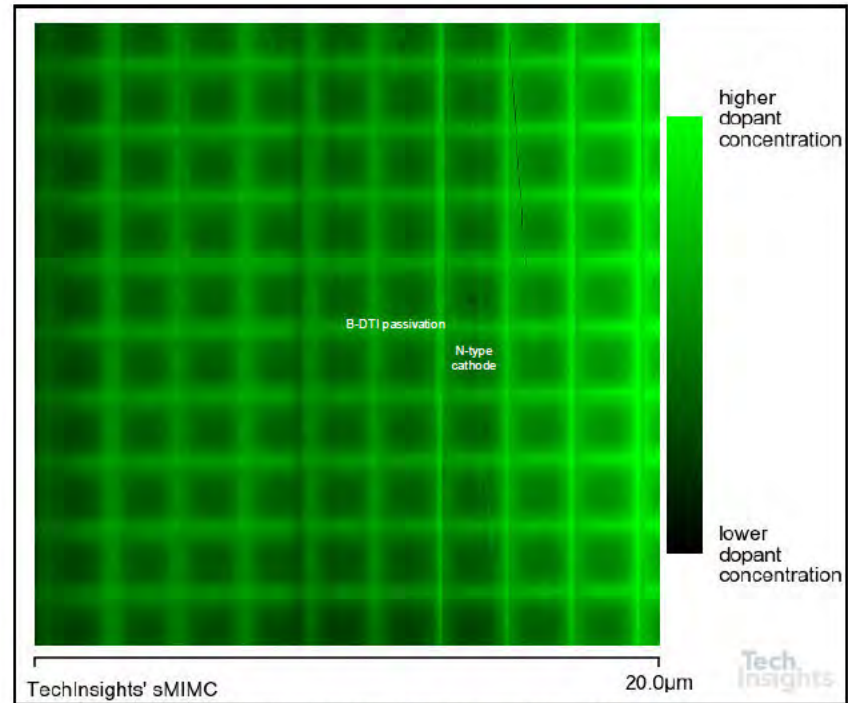
Pixel Planar Analysis

- SCM and sMIM-C images of the photocathodes at the B-DTI region
- The N-type photocathode has an approximate area of $2.89 \mu\text{m}^2$.



0717200822_PRODUCT_FRW_20.0u_512p_371773.png

Pixel at the Start of B-DTI Region – Planar SCM

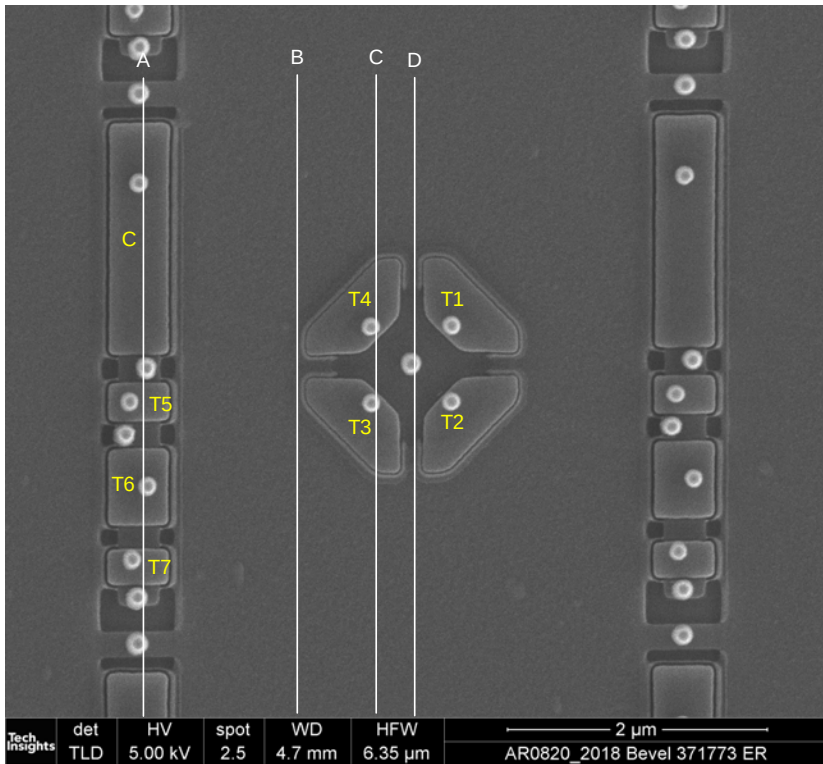


0717200822_SMIMC_FRW_20.0u_512p_371773.png

Pixel at the Start of B-DTI Region – Planar sMIM-C

CIS Cross Section Analysis – Y-Direction

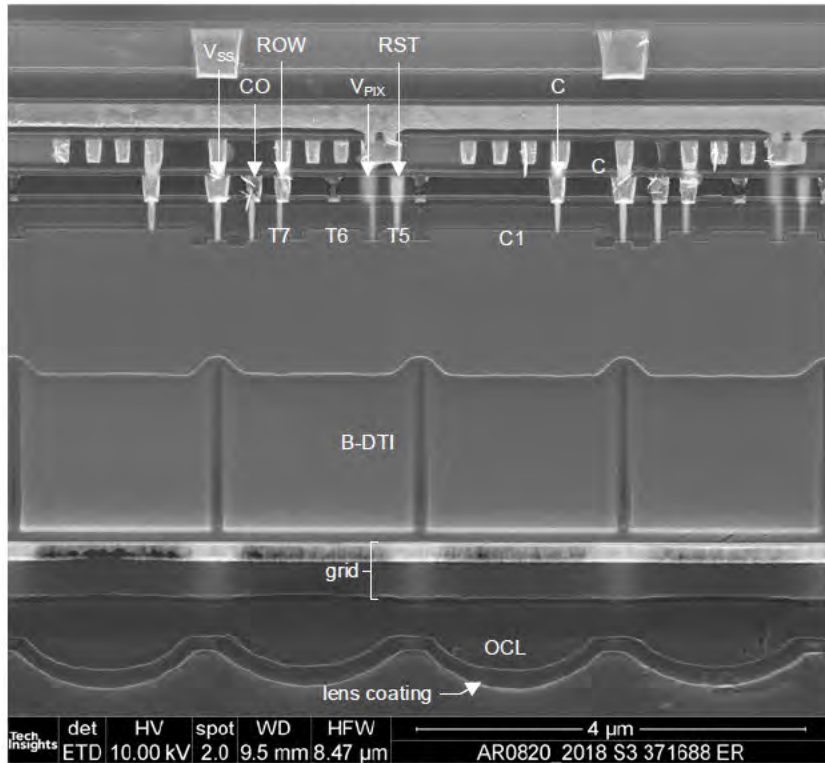
Pixel Cross Section Analysis – Y-Direction



543_CIS_PixelArray_Poly_20K_371773_1.png

- SEM bevel image at the polysilicon level showing the locations of the pixel cross section planes in the Y-direction (parallel to column out lines) and X-direction (parallel to the row select lines)

Pixel Cross Section Analysis – Y-Direction



- SEM cross section overview through section line A (T5, T6, T7, and C1)

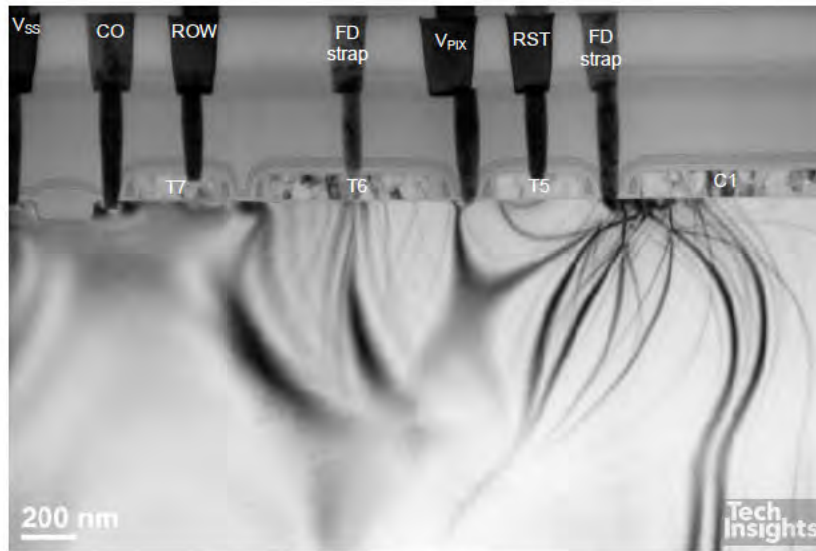
758_CIS_PixelArray_T7-RS_T6-SF_T5-RST_C1_15K_371688.png

Pixel Transistor Summary

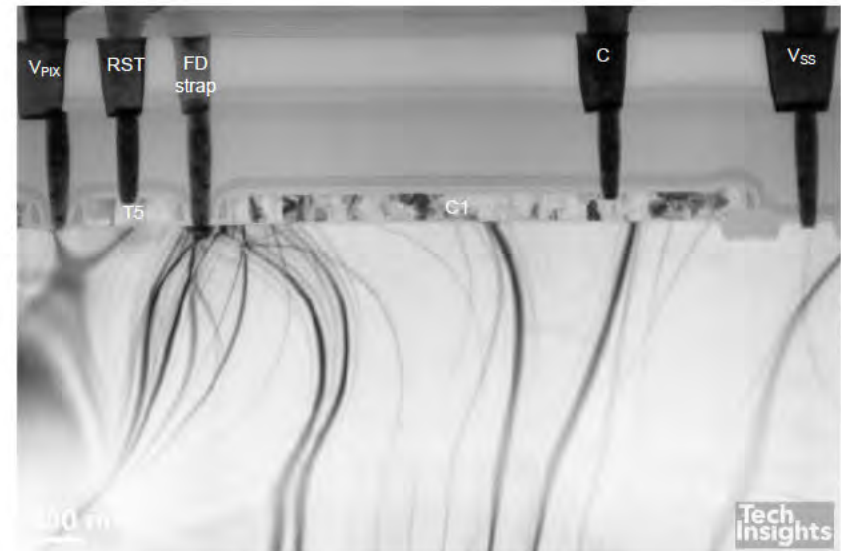
Transistor	Length (nm)	Gate Dielectric	Gate Dielectric Thickness (nm)
Transfer gate (T1-T4)	440	Nitrided oxide	5.9
RST (T5)	300	Nitrided oxide	5.9
SF (T6)	600	Nitrided oxide	5.9
ROW (T7)	280	Nitrided oxide	5.9
Capacitor (C1)	1.7 μm	Nitrided oxide	5.9

Pixel Cross Section Analysis – Y-Direction

- TEM cross section overview images through section line A (T5, T6, T7, and C1)



T5-7_C1_8.9kx_370533.png

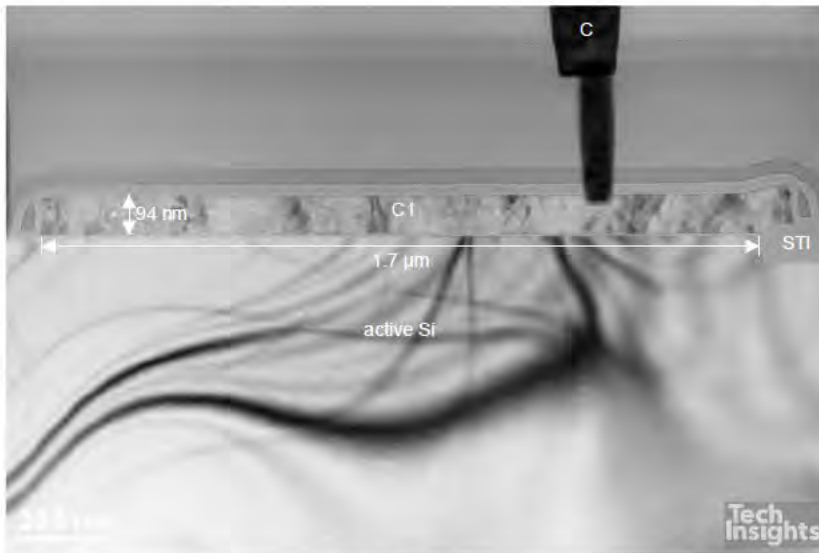


T5_C1_8.9kx_370533.png

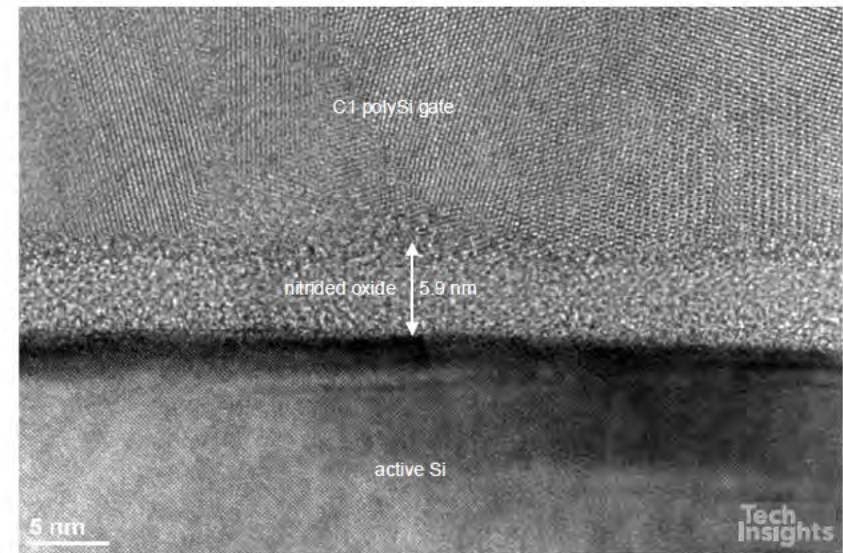
T5 and C1 Overview (Section Line A) – TEM

Pixel Cross Section Analysis – Y-Direction

- TEM cross section across C1 MOS capacitor
- The capacitor C1 polysilicon gate is 1.7 μm long .
- The C1 gate dielectric comprises a 5.9 nm thick nitrided oxide.



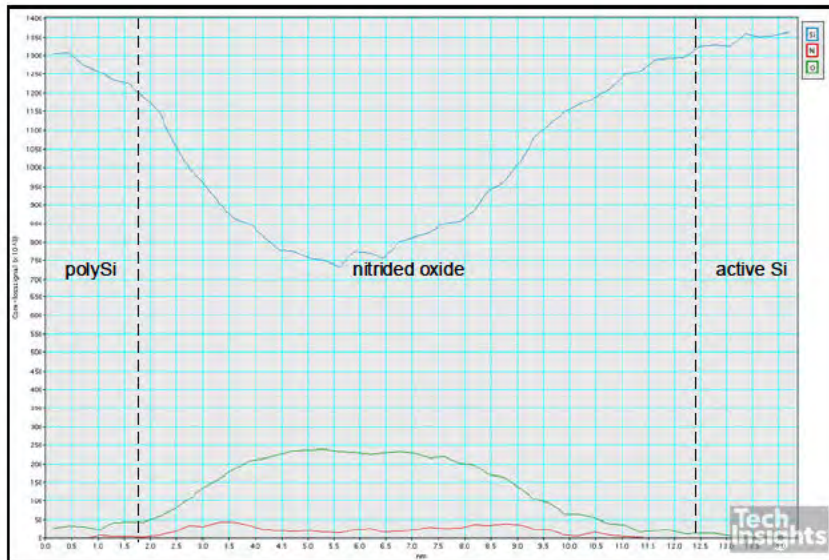
C1_13.5kx_370533.png



C1_Gox_440kx_3r_370533.png

C1 Gate Dielectric – TEM

Pixel Cross Section Analysis – Y-Direction



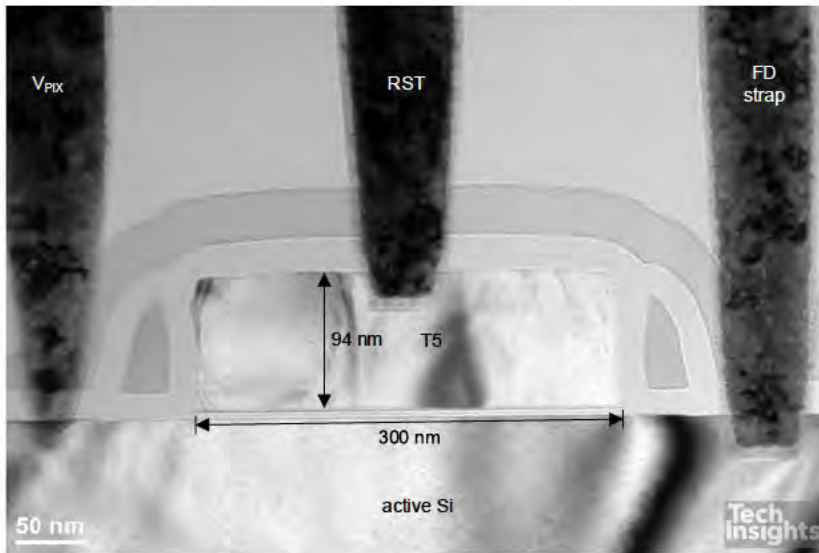
C1_Gox_20.17.39 Edge Profiles_370533.png

C1 Gate Dielectric – TEM-EELS

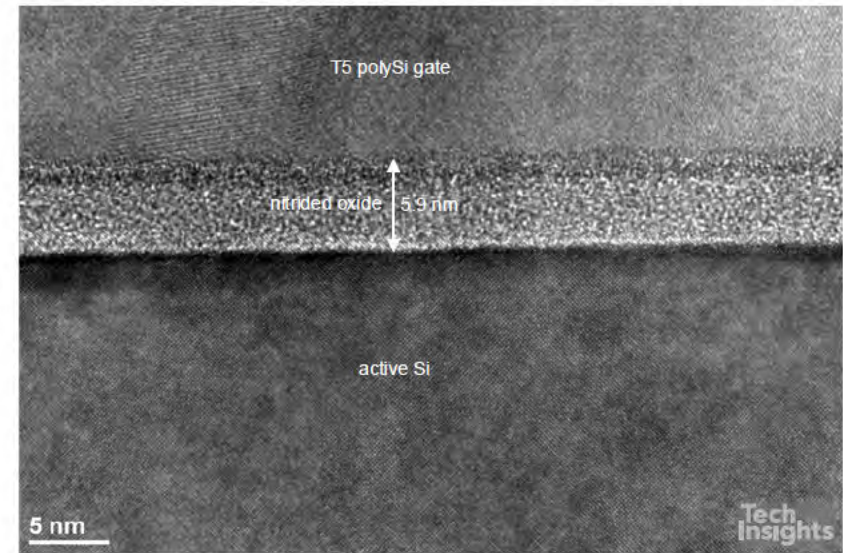
- TEM-EELS scan spectra of C1 gate dielectric
- The gate dielectric is a nitrided oxide.

Pixel Cross Section Analysis – Y-Direction

- TEM cross section across T5 (RST)
- The T5 (RST) is 300 nm long.
- T5 (RST) gate dielectric comprises a 5.9 nm thick nitrided oxide.



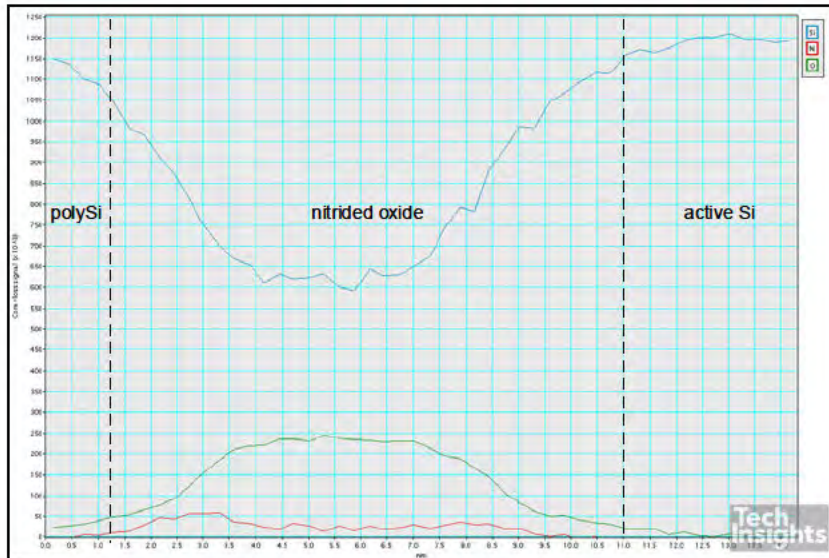
T5_39kx_1r_370533.png



T5_Gox_440kx_1r_370533.png

T5 (RST) Gate Dielectric – TEM

Pixel Cross Section Analysis – Y-Direction

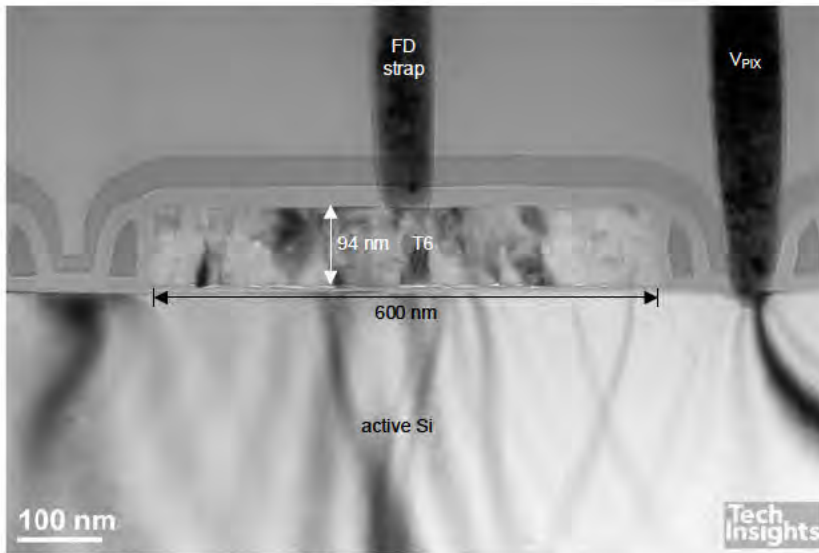


- TEM-EELS scan spectra of T5 (RST) gate dielectric
- The gate dielectric is a nitrated oxide.

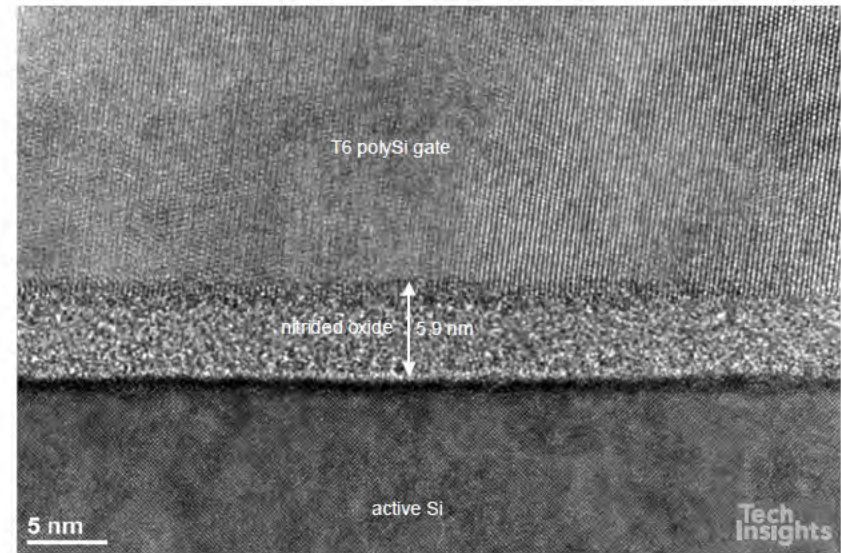
T5_Gox_20.50.08 Edge Profiles_370533.png

Pixel Cross Section Analysis – Y-Direction

- TEM cross section across T6 (SF)
- The T6 (SF) is 600 nm long.
- T6 (SF) gate dielectric comprises a 5.9 nm thick nitrided oxide.



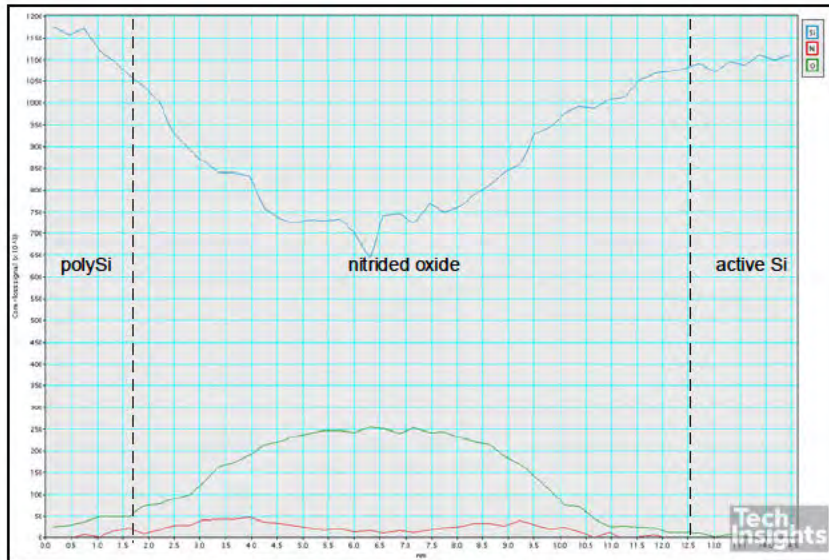
T6_26.5kx_370533.png



T6_Gox_440kx_1r_370533.png

T6 (SF) Gate Dielectric – TEM

Pixel Cross Section Analysis – Y-Direction



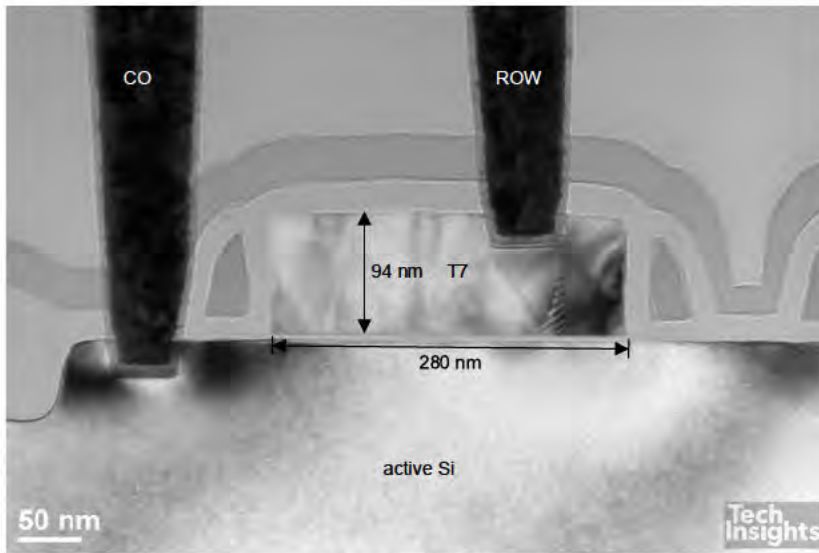
T6_Gox_20.39.43 Edge Profiles_370533.png

T6 (SF) Gate Dielectric – TEM-EELS

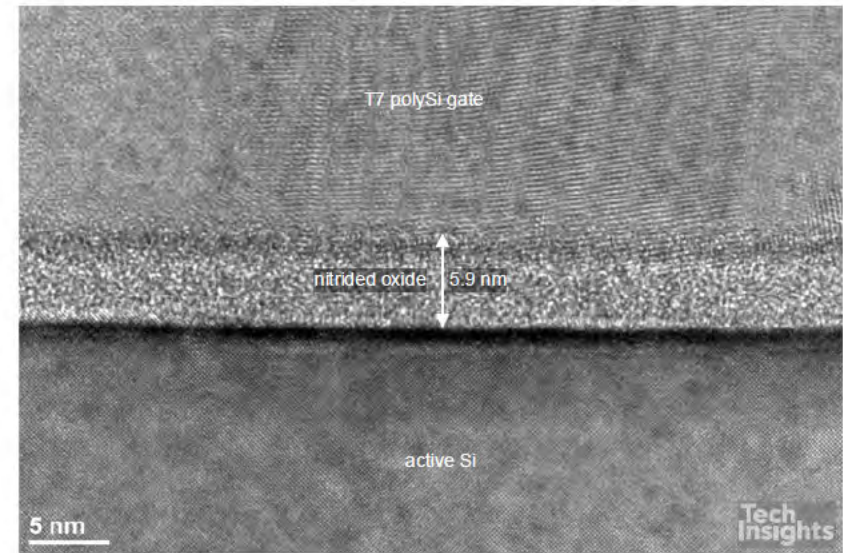
- TEM-EELS scan spectra of T6 (SF) gate dielectric
- The gate dielectric is a nitrided oxide.

Pixel Cross Section Analysis – Y-Direction

- TEM cross sections across T7 (ROW)
- The T7 (ROW) is 280 nm long.
- T7 (ROW) gate dielectric comprises a 5.9 nm thick nitrided oxide.



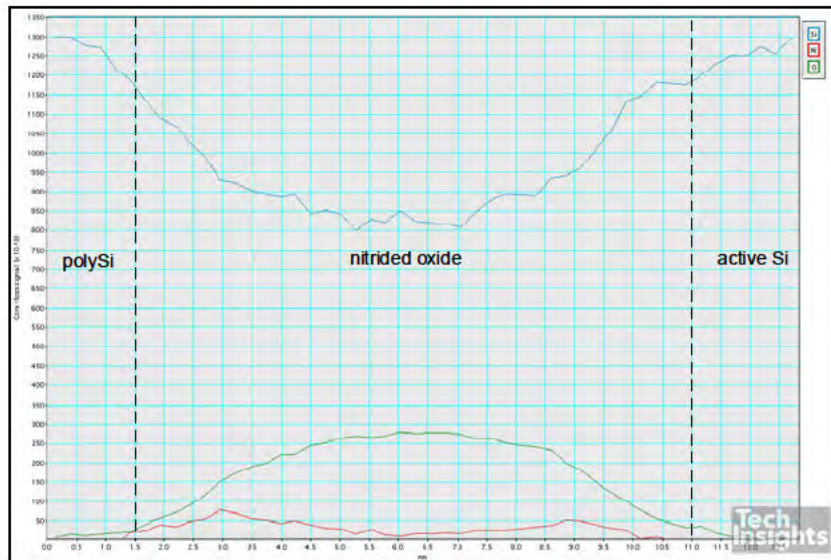
T7_39kx_370533.png



T7_Gox_440kx_1r_370533.png

T7 (ROW) Gate Dielectric – TEM

Pixel Cross Section Analysis – Y-Direction



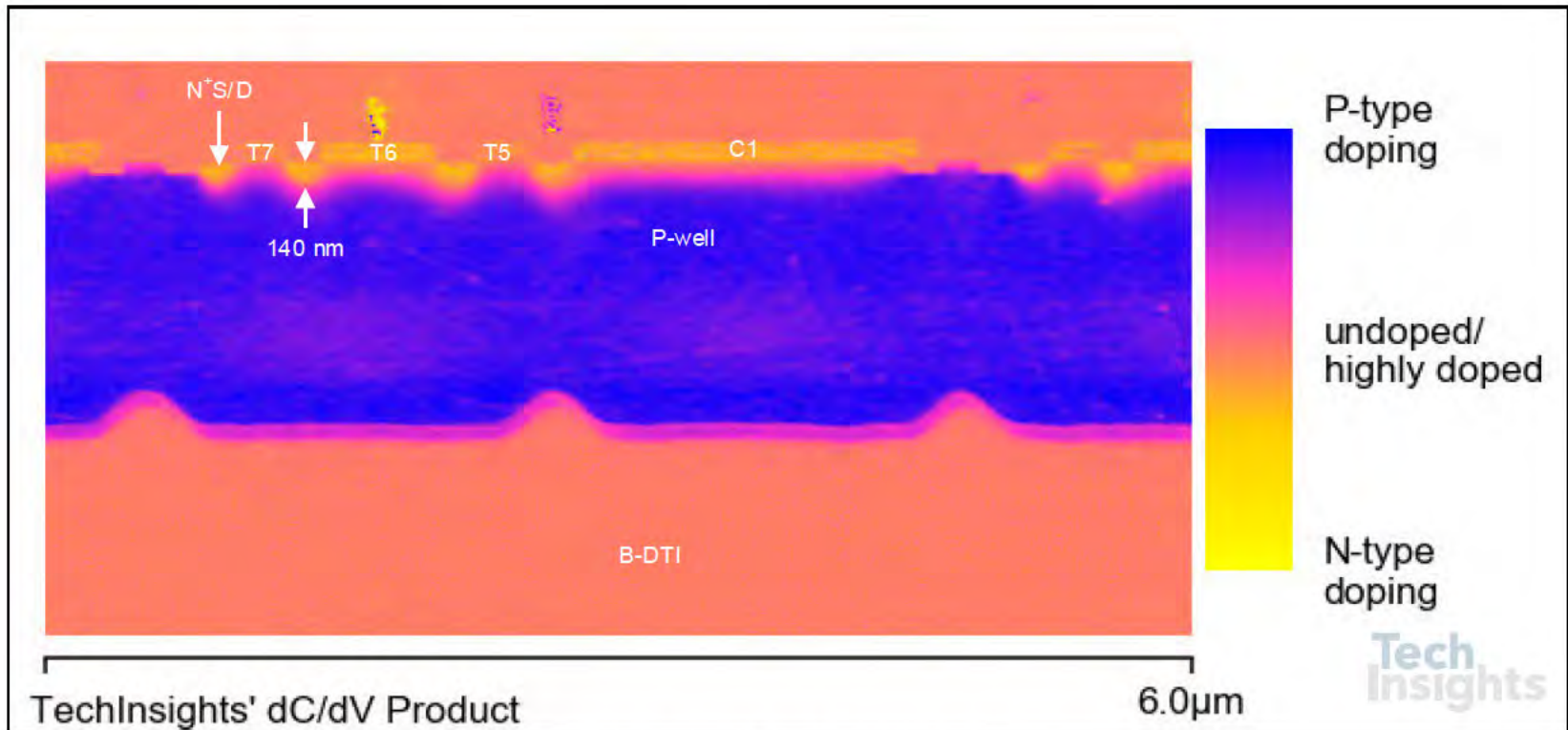
T7_Gox_20.28.16 Edge Profiles_370533.png

T7 (ROW) Gate Dielectric – TEM-EELS

- TEM-EELS scan spectra of T7 (ROW) gate dielectric
- The gate dielectric is a nitrided oxide.

Pixel Cross Section Analysis – Y-Direction

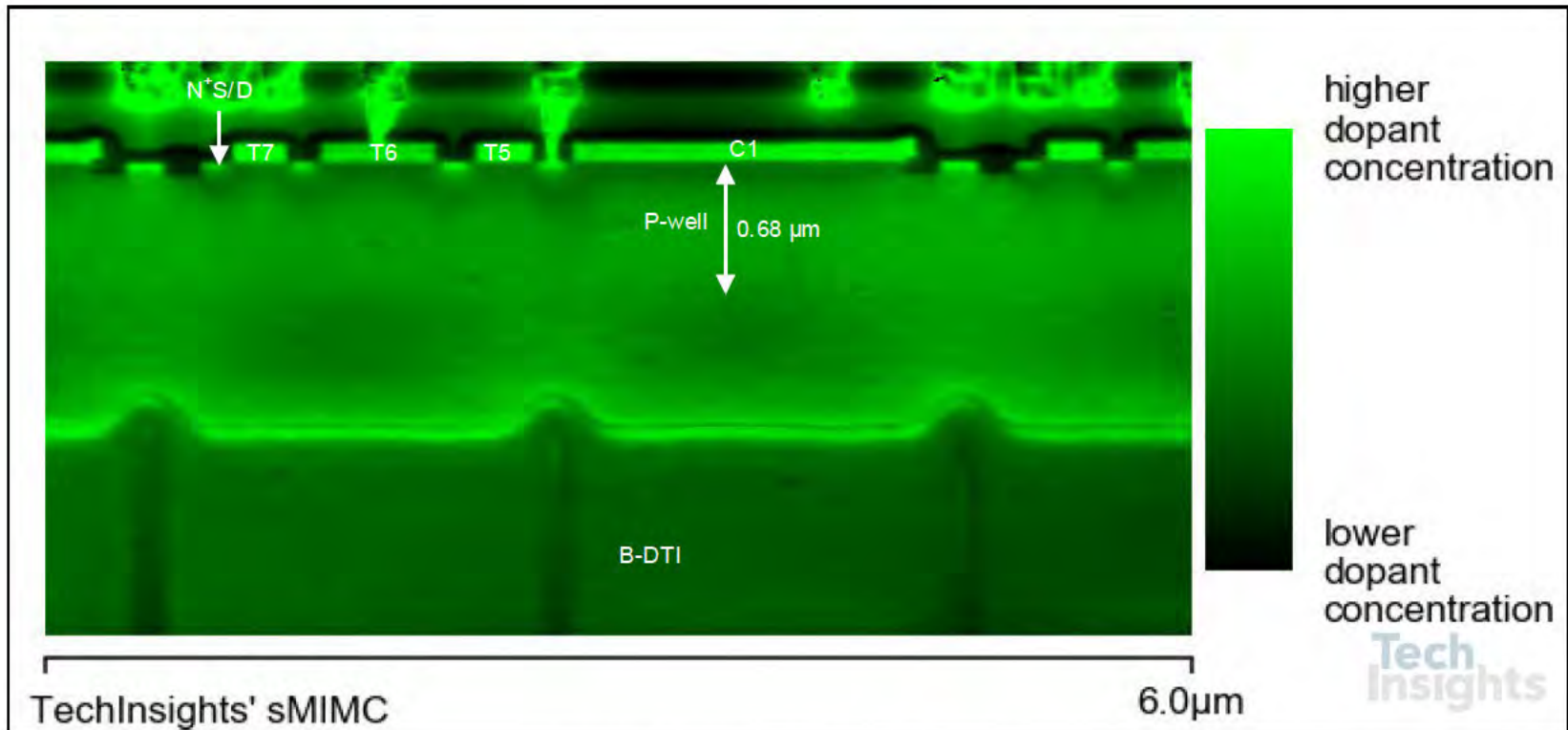
- SCM cross section image through section line A (T5, T6, T7, and C1)
- The N⁺ S/D region is 140 nm thick.



0721200829_PRODUCT_FRW_6.0u_512p_371688.png

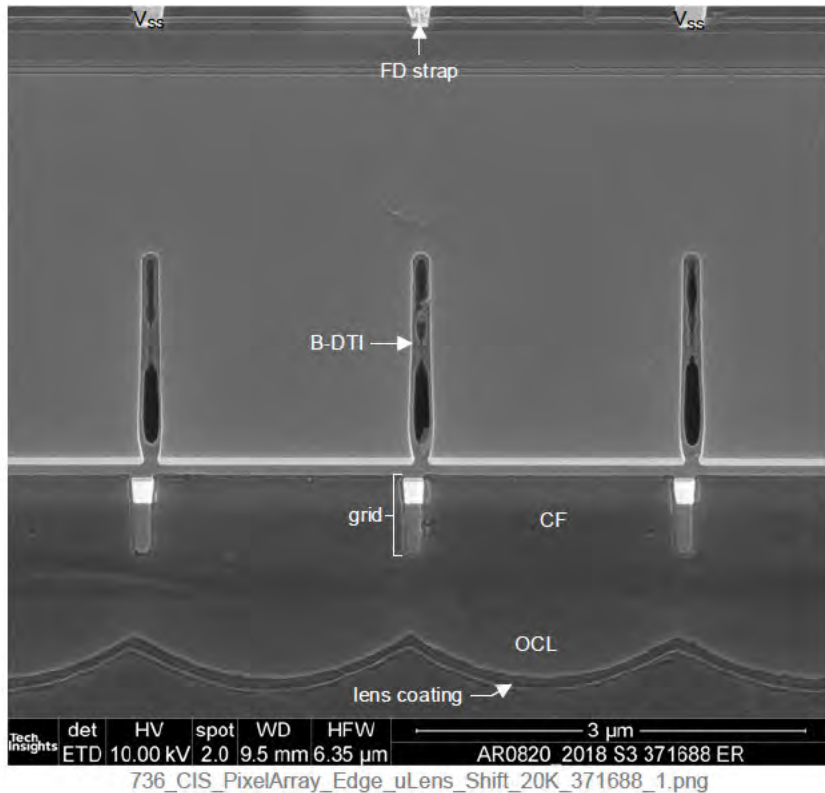
Pixel Cross Section Analysis – Y-Direction

- sMIM-C cross section image through section line A (T5, T6, T7, and C1)
- The P-well is about 0.68 μm thick.



0721200829_SMIMC_FRW_6.0u_512p_371688.png

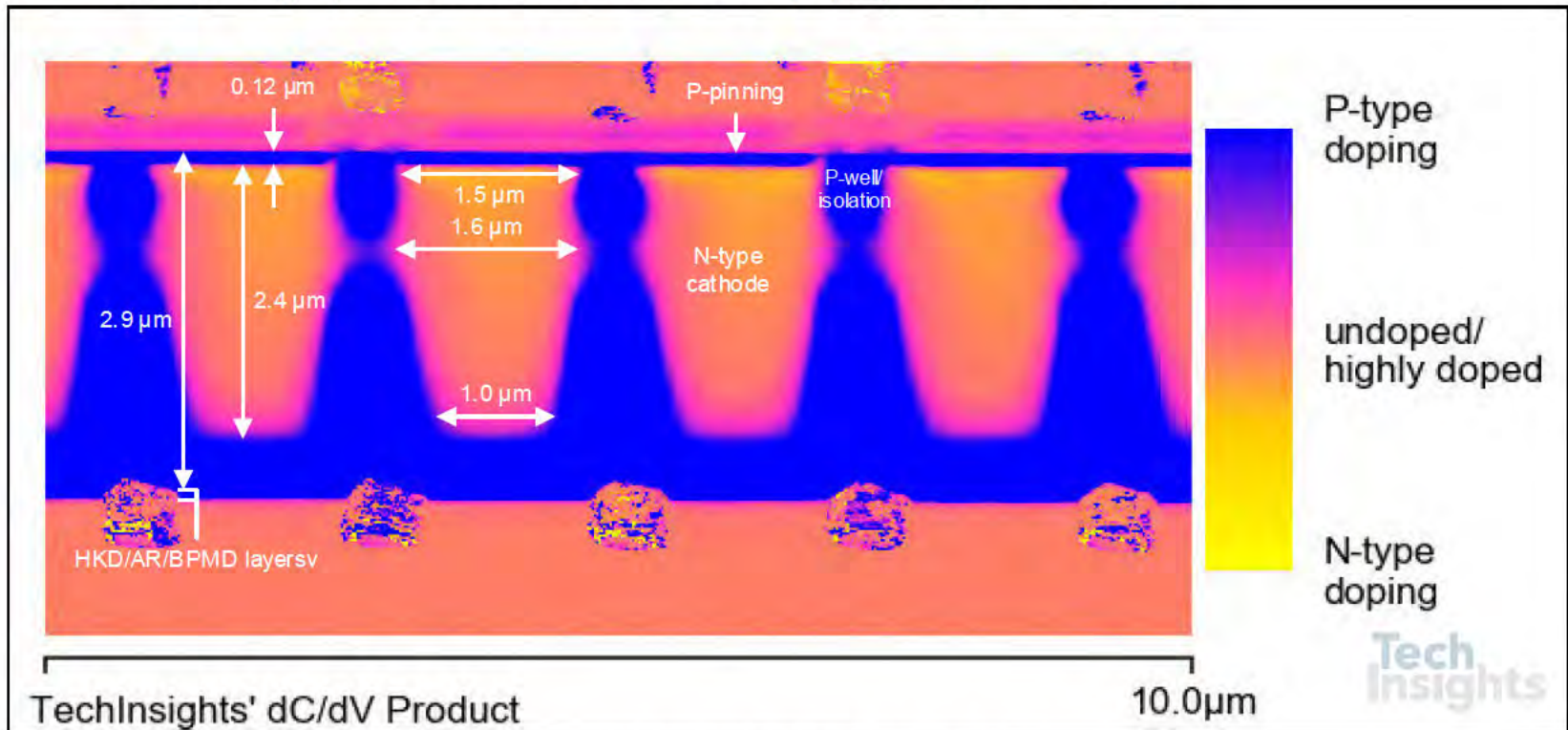
Pixel Cross Section Analysis – Y-Direction



- SEM cross section overview image through section line B (pixel center)

Pixel Cross Section Analysis – Y-Direction

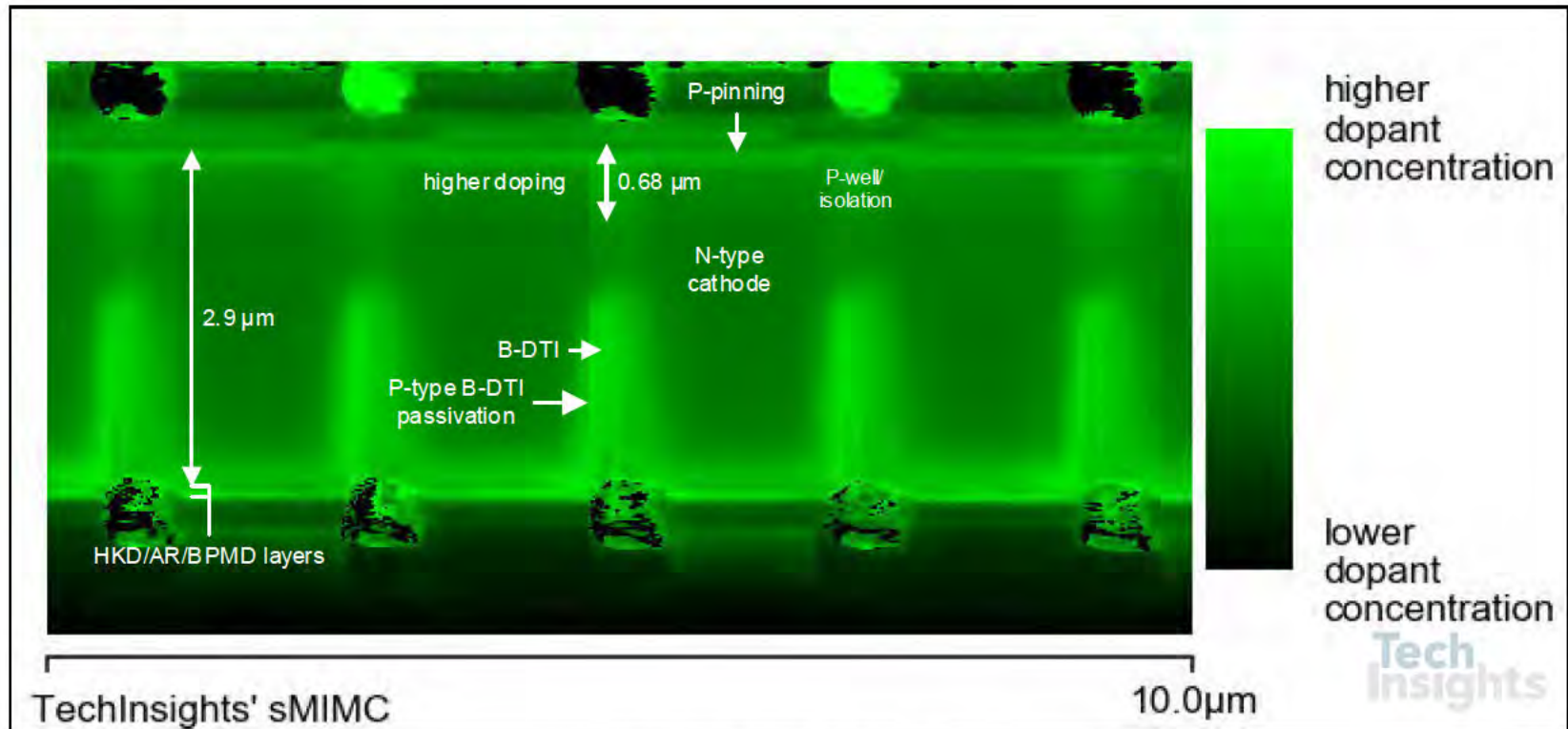
- SCM cross section overview image through section line B (pixel center)
- The N-type photocathode is 2.4 μm thick. As shown in the sMIM-C image on the next page, the top region of the photocathode has a higher doping concentration.
- The width of the N-type photocathode varies from 1.0-1.6 μm , depending on the location.



0720200854_PRODUCT_FRW_10.0u_512p_371688.png

Pixel Cross Section Analysis – Y-Direction

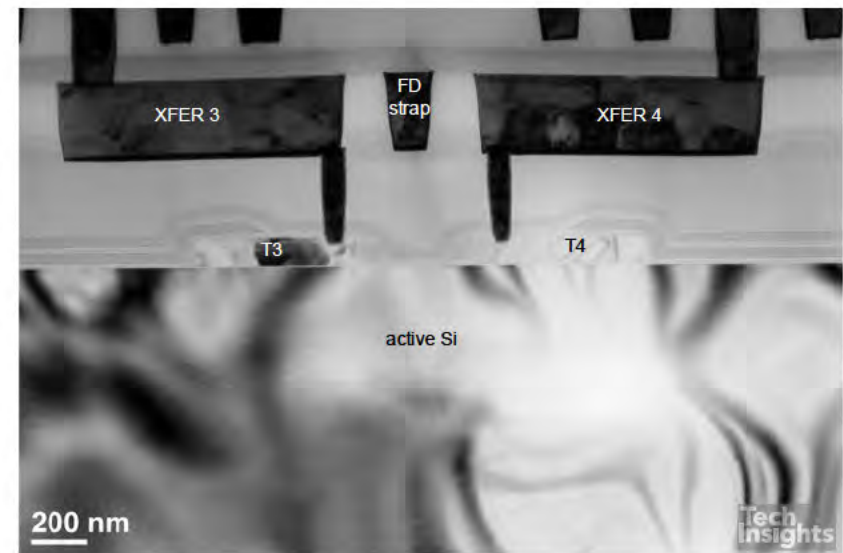
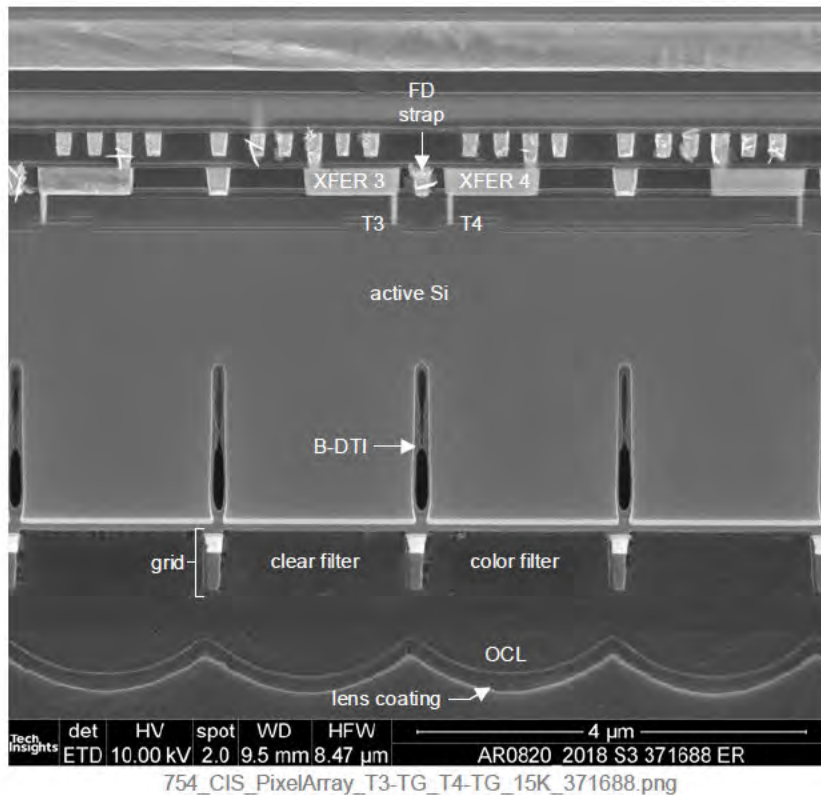
- sMIM-C cross section overview image through section line B (pixel center)
- The P-well/isolation region is $0.68\text{ }\mu\text{m}$ thick.
- The sMIM-C image shows that the upper region of the photocathode has a higher doping concentration.



0720200854_SMIMC_FRW_10.0u_512p_371688.png

Pixel Cross Section Analysis – Y-Direction

- SEM cross section overview and TEM detail images through section line C (T3/T4 transfer gates)

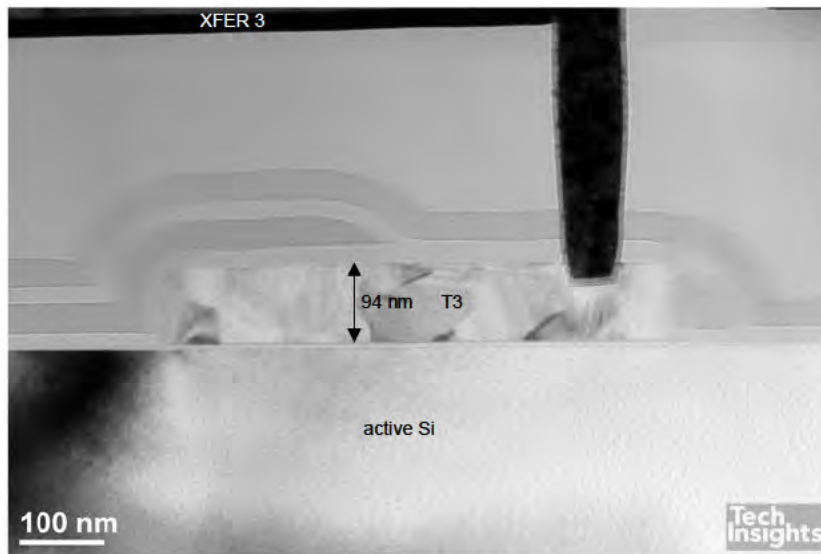


**T3 and T4 Transfer Gates Detail
(Section Line C) – TEM**

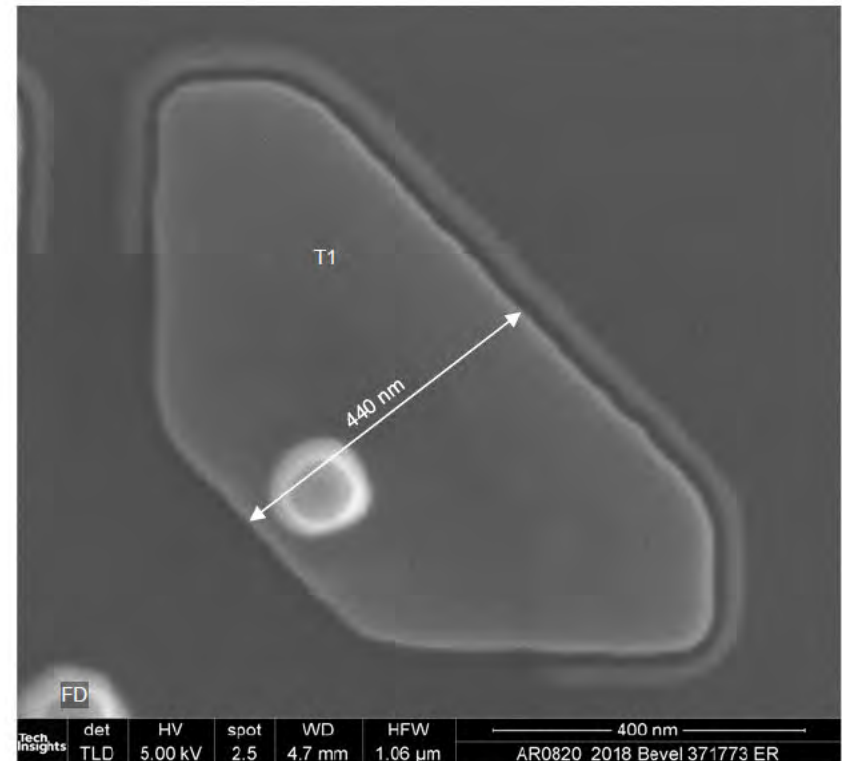
Greenthread Ex 2020, p. 226
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Pixel Cross Section Analysis – Y-Direction

- TEM cross section image of T3 and SEM cross plan view image of T1
- The transfer gates have a length of 440 nm.



T1-4_26.5kx_370533.png

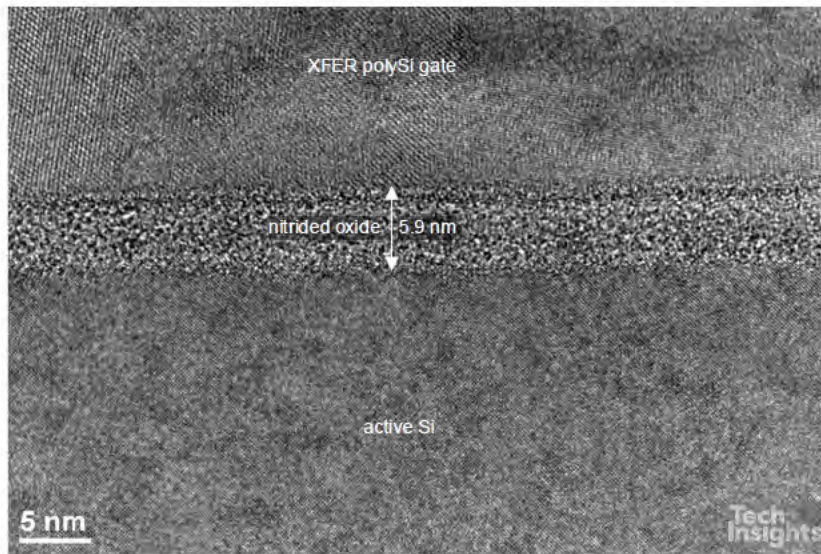


552_CIS_PixelArray_T1-TG_120K_371773.png

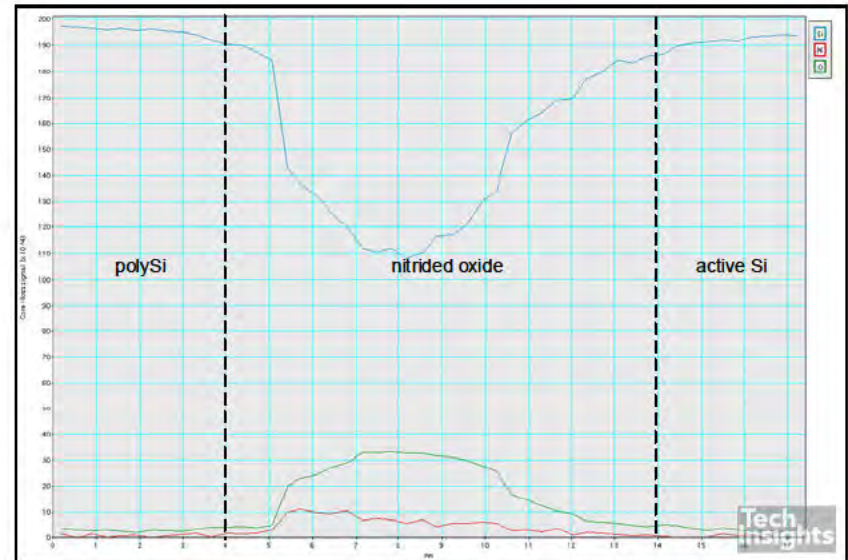
T1 Transfer Gate Detail – SEM Plan View

Pixel Cross Section Analysis – Y-Direction

- The transfer transistor gate dielectric comprises a 5.9 nm thick nitrided oxide.



T1-4_Gox_440kx_1_370533.png

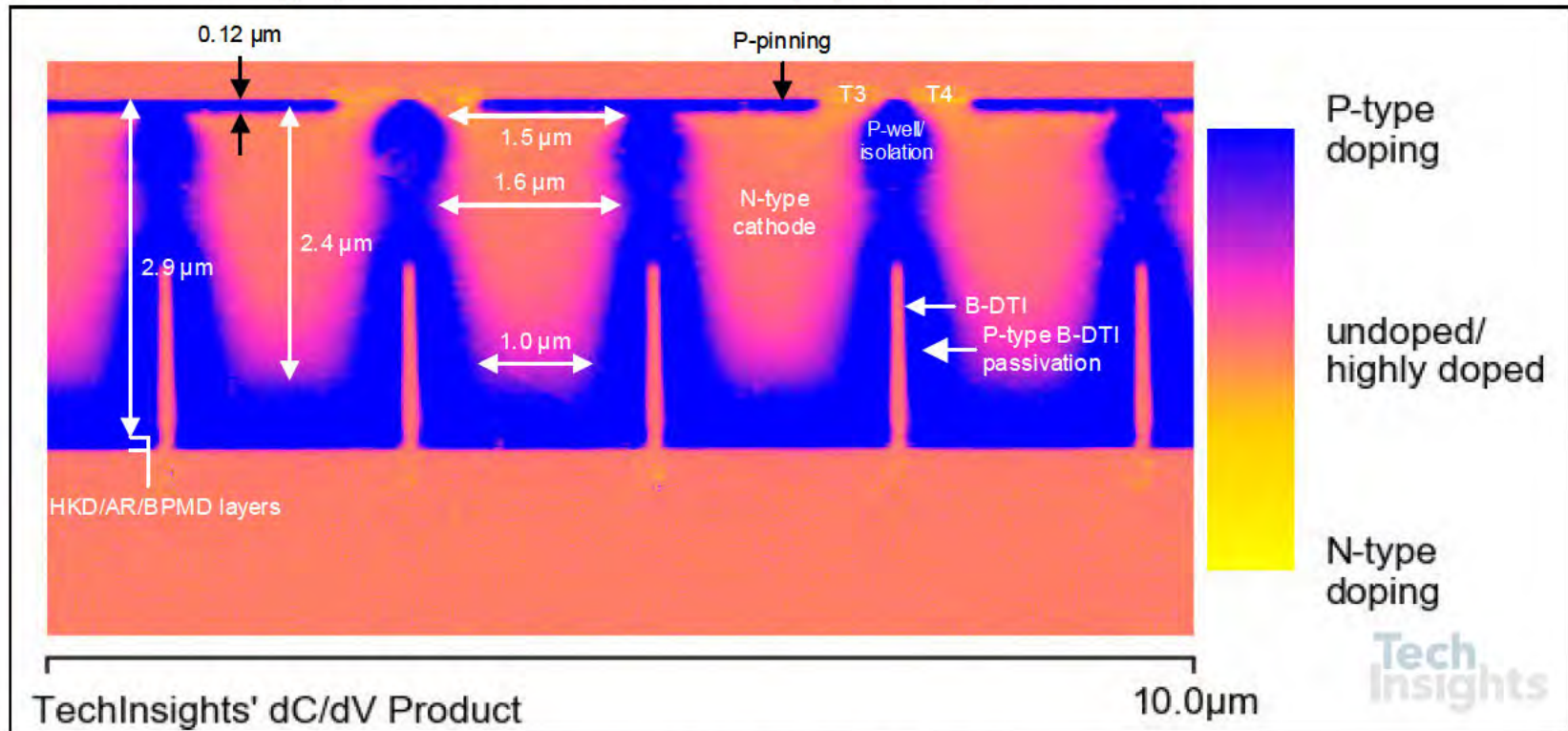


T1-4_Gox_16.08.42 Edge Profiles_370533.png

XFER Gate Dielectric – TEM-EELS

Pixel Cross Section Analysis – Y-Direction

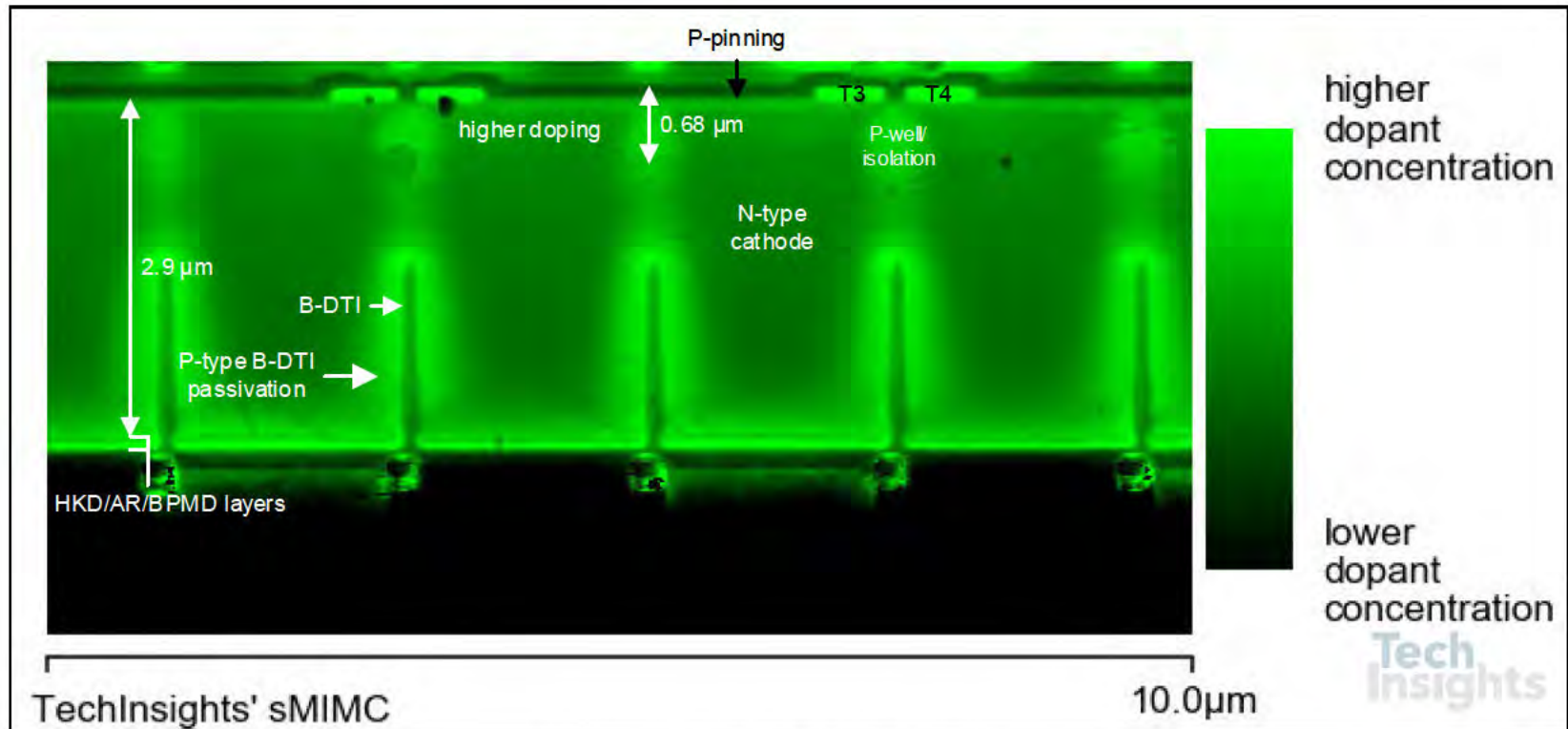
- SCM cross section image through section line C (T3 and T4 and photocathode)
- The N-type photocathode is 2.4 μm thick. As shown in the sMIM-C image on the next page, the top region of the photocathode has a higher doping concentration.
- The width of the N-type photocathode varies from 1.0-1.6 μm , depending on the location.



0721201156_PRODUCT_FRW_10.0u_512p_371688.png

Pixel Cross Section Analysis – Y-Direction

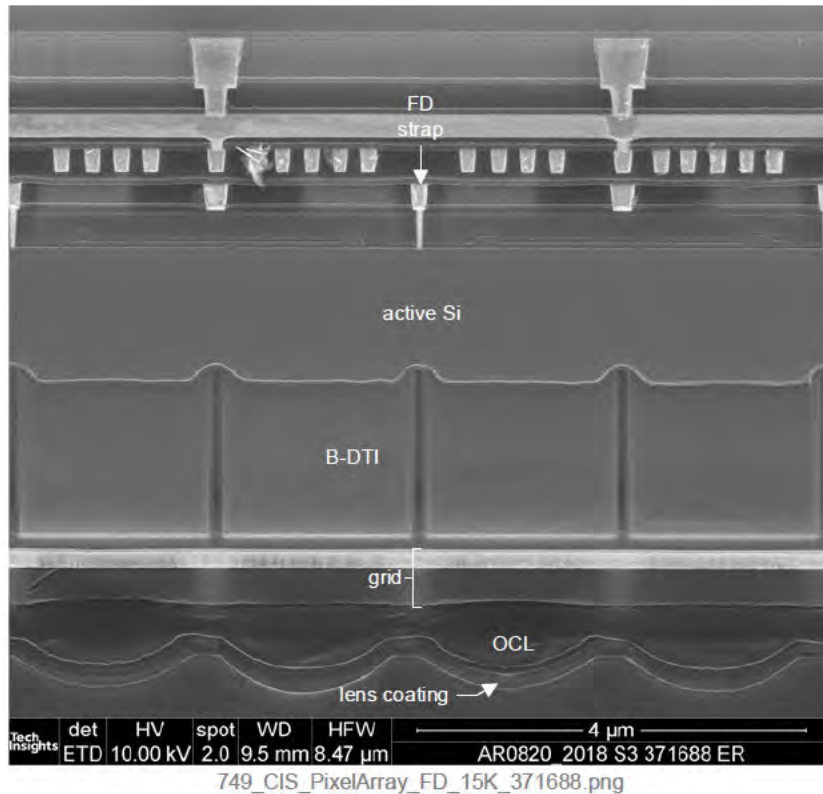
- sMIM-C cross section overview image through section line C (XFER gates and photocathode)
- The P-well/isolation region is $0.68\ \mu\text{m}$ thick.
- The sMIM-C image shows that the upper region of the photocathode has a higher doping concentration.



0721201156_SMIMC_FRW_10.0u_512p_371688.png

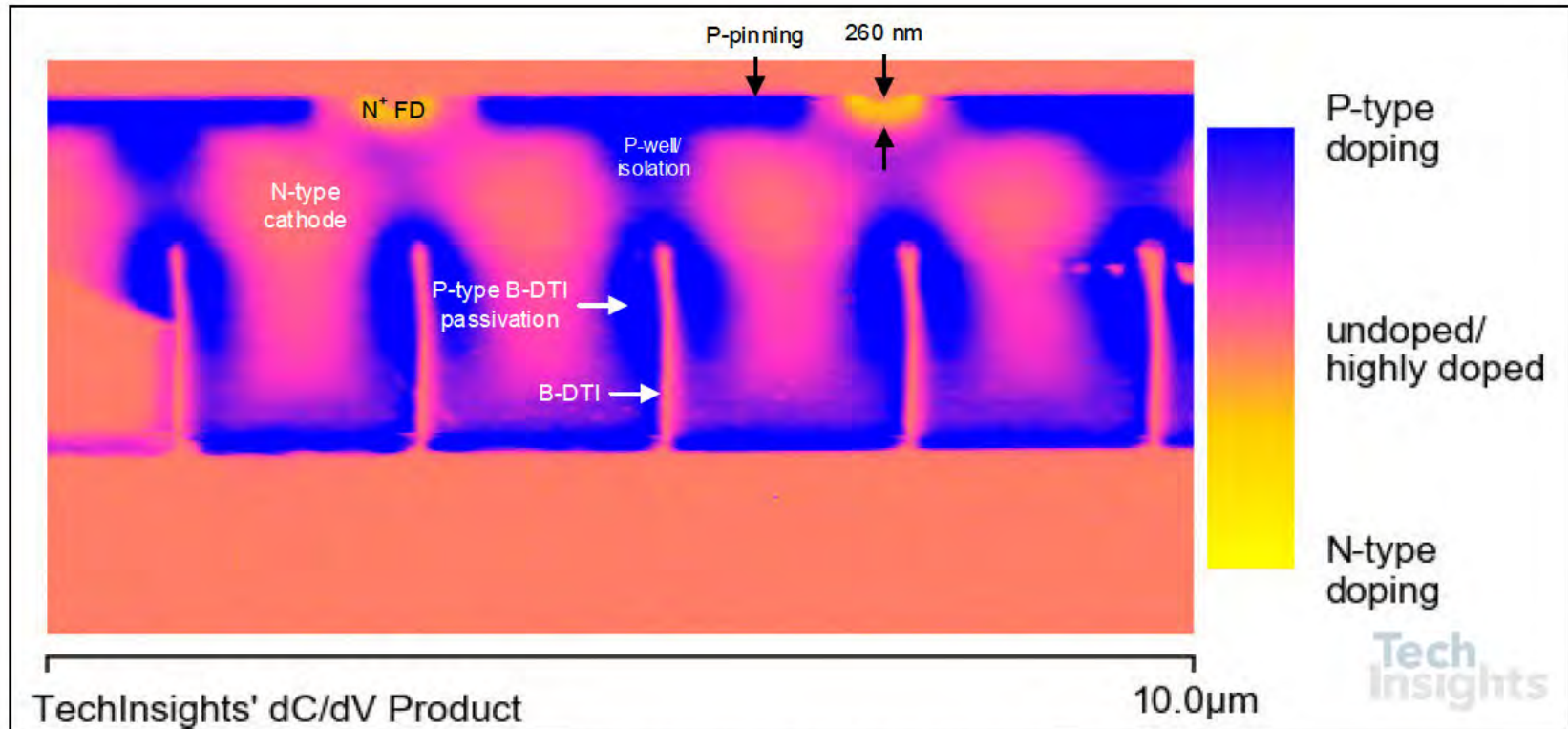
Pixel Cross Section Analysis – Y-Direction

- SEM cross section overview image through section line D (FD)



Pixel Cross Section Analysis – Y-Direction

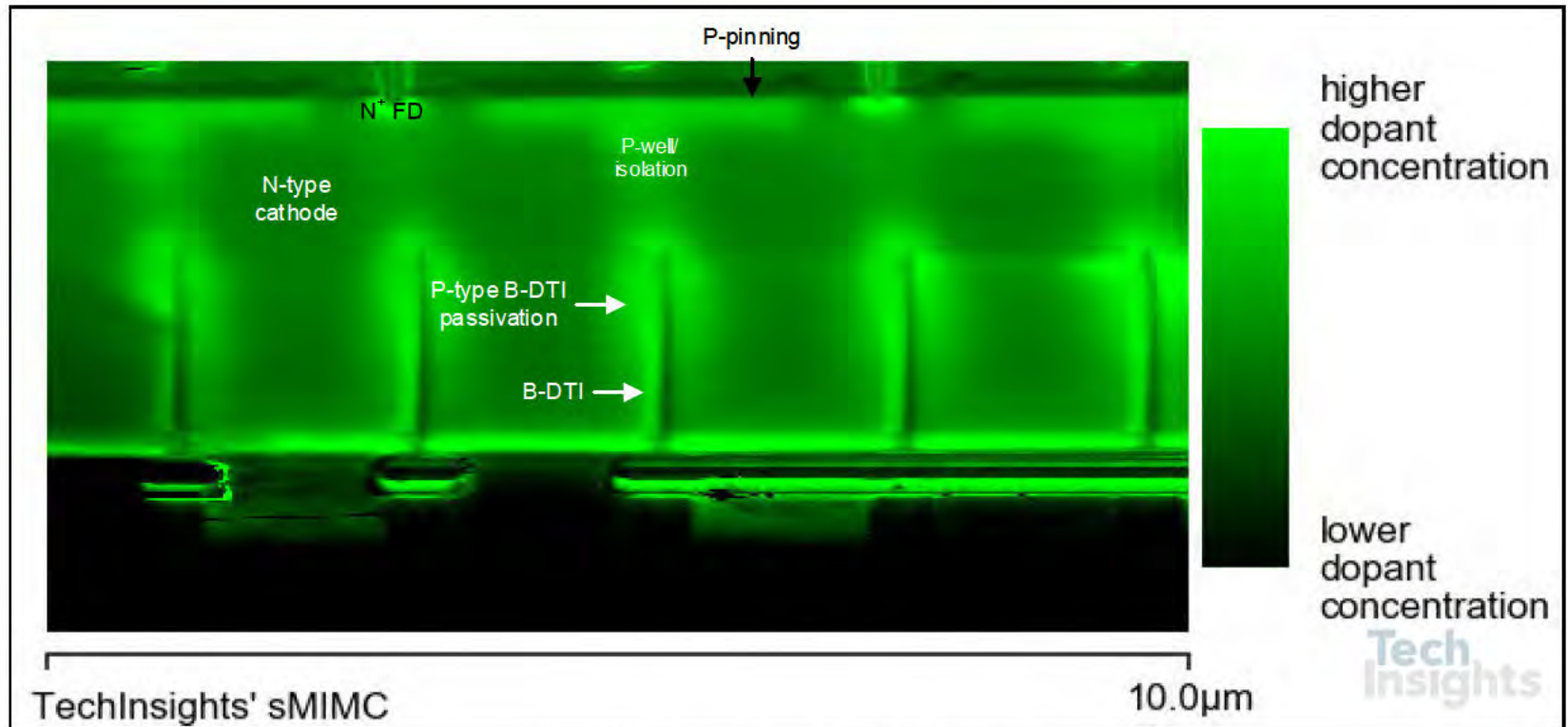
- SCM cross section overview image through section line D (FD)
- The N⁺ FD region is 260 nm deep.
- Note: The apparent distortion of the B-DTI is an artifact of the SCM scan.



0721200655_PRODUCT_FRW_10.0u_512p_371688.png

Pixel Cross Section Analysis – Y-Direction

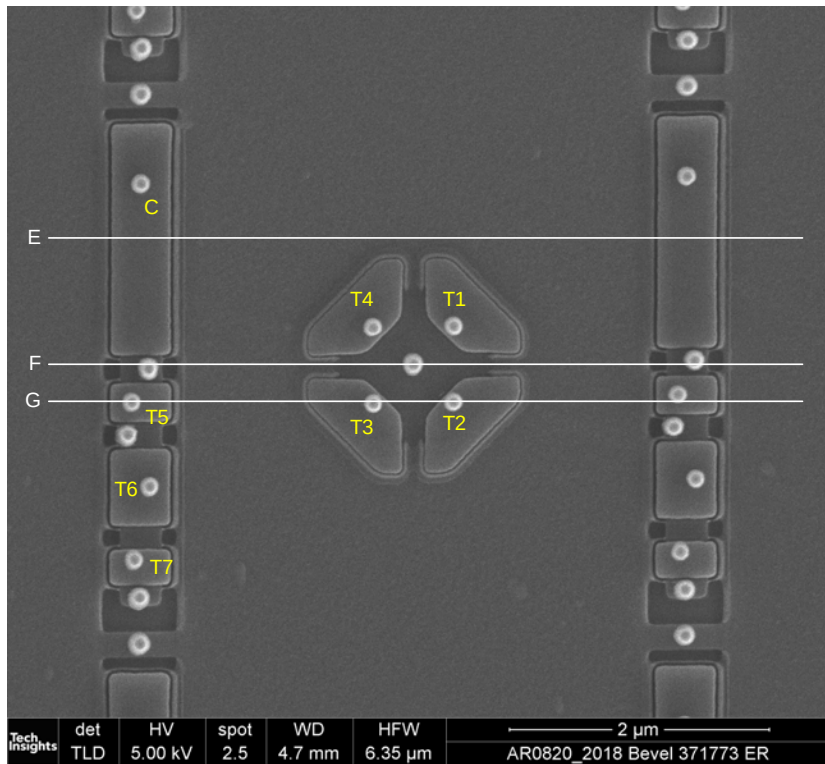
- sMIM-C cross section overview image through section line D (FD)
- Note: The apparent distortion of the B-DTI is an artifact of the SCM scan.



0721200655_SMIMC_FRW_10.0u_512p_371688.png

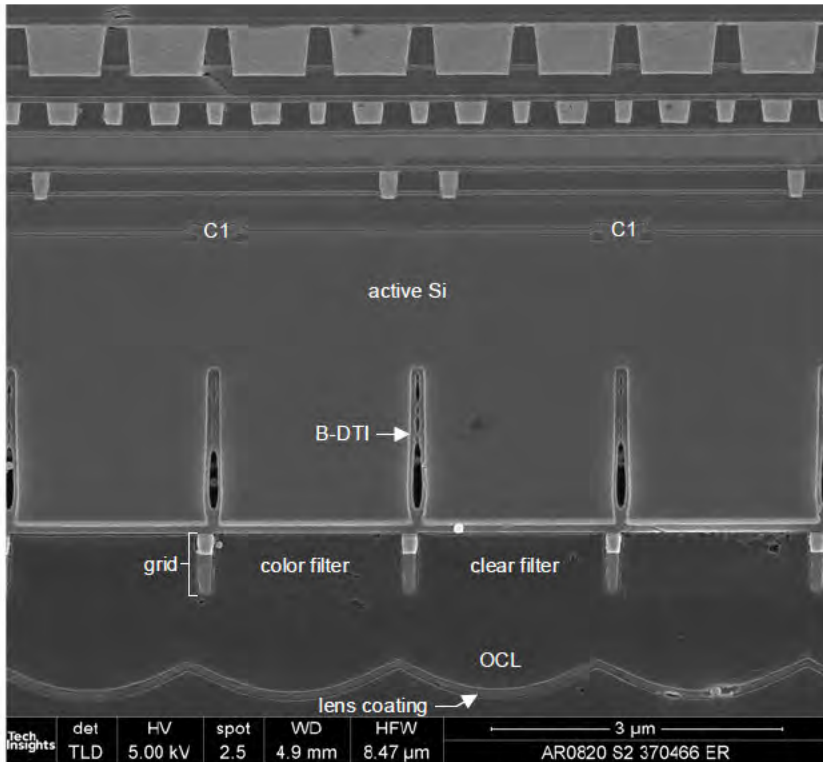
CIS Cross Section Analysis – X-Direction

Pixel Cross Section Analysis – X-Direction



- SEM bevel image at the polysilicon level showing the locations of the pixel cross section planes in the Y-direction (parallel to column out lines) and X-direction (parallel to the row select lines)

Pixel Cross Section Analysis – X-Direction

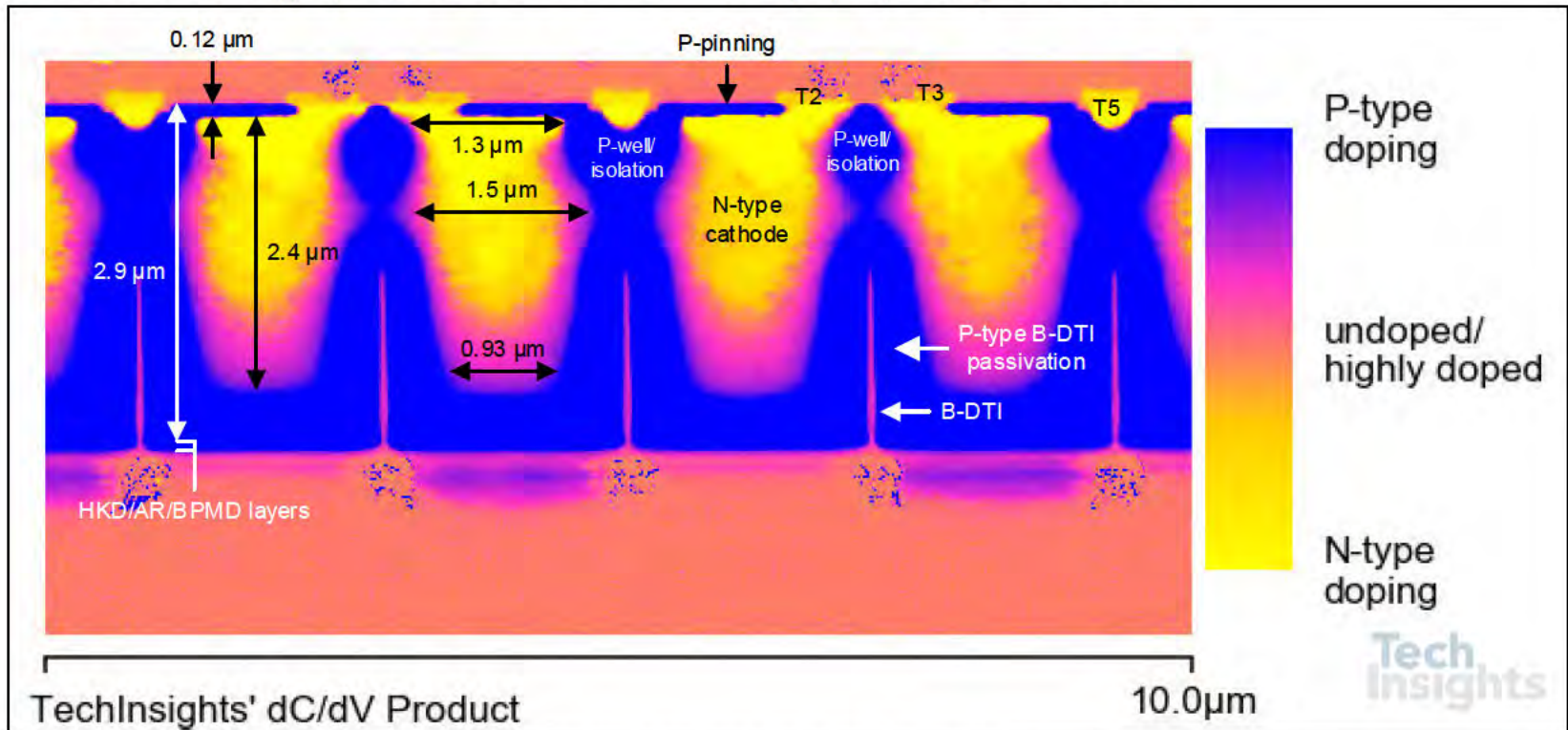


471_CIS_PixelArray_Center+15K_370466_1.png

- SEM cross section image through section line E (pixel center)

Pixel Cross Section Analysis – X-Direction

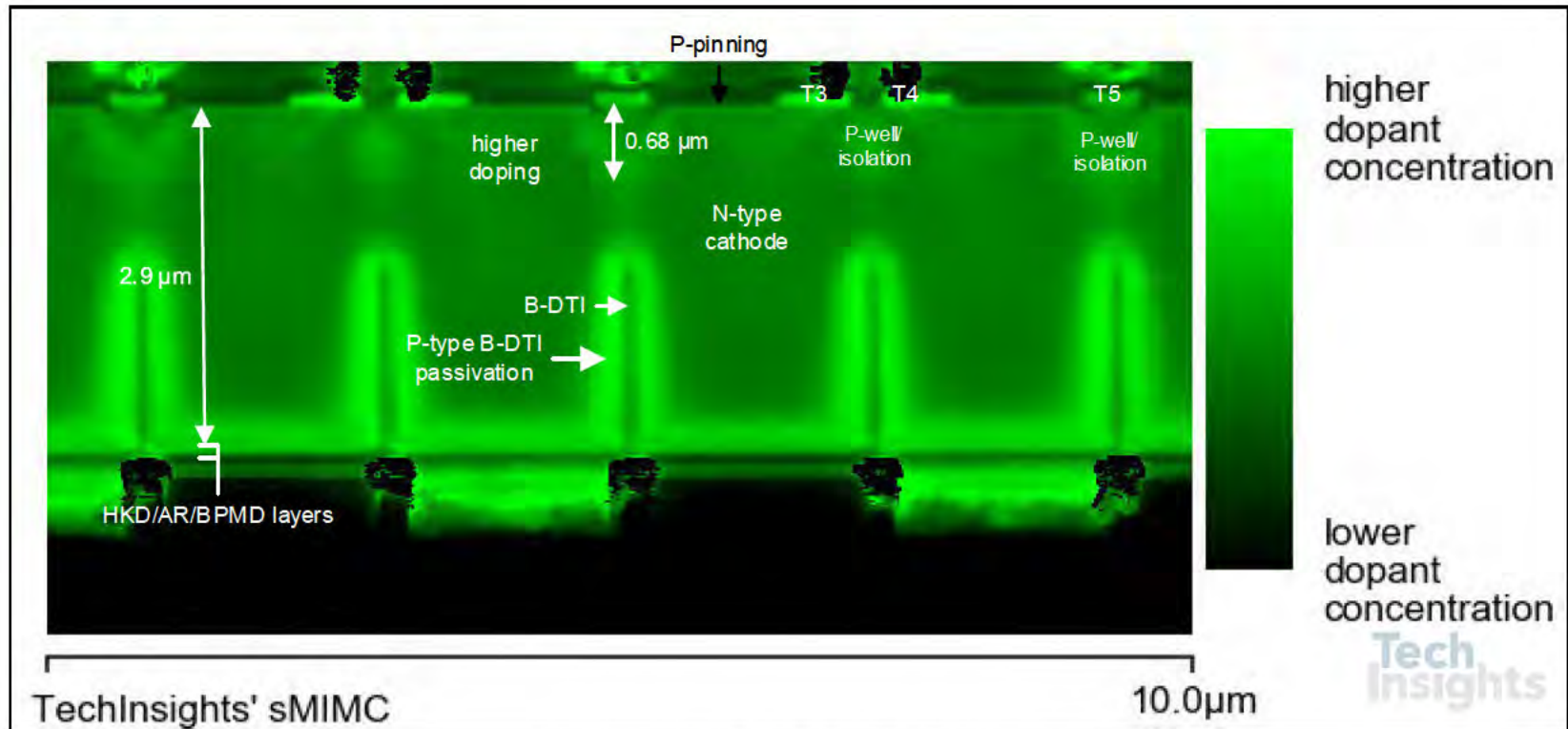
- SCM cross section overview image through section line E (pixel center)
- The N-type photocathode is 2.4 μm thick. As shown in the sMIM-C image on the next page, the top region of the photocathode has a higher doping concentration.
- The width of the N-type photocathode varies from 1.1-1.6 μm , depending on the location.



0708201114_PRODUCT_FRW_10.0u_512p_370466.png

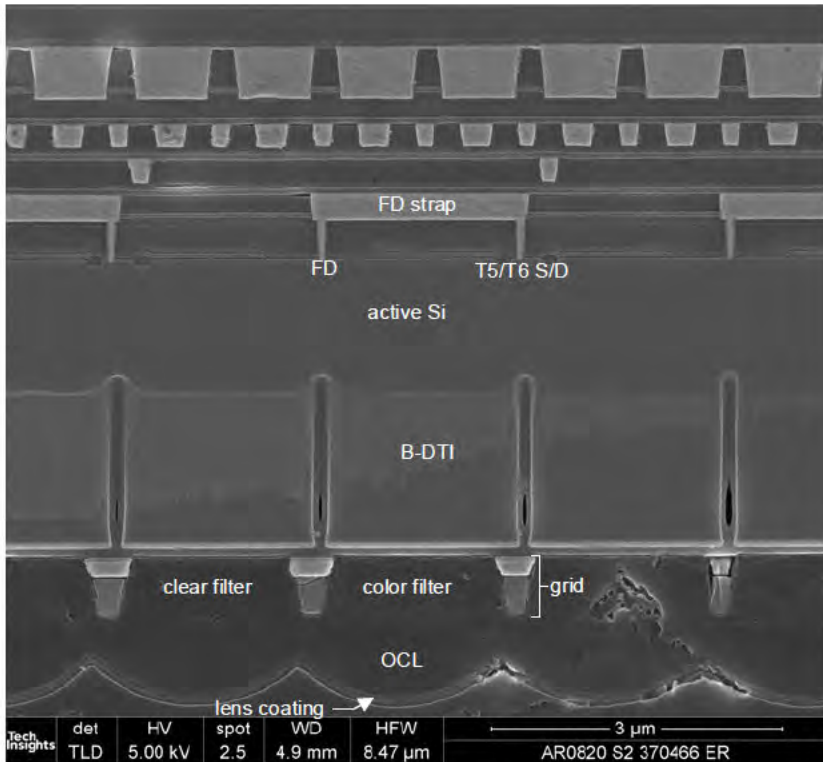
Pixel Cross Section Analysis – X-Direction

- sMIM-C cross section overview image through section line E (pixel center)
- The P-well/isolation region is $0.68\text{ }\mu\text{m}$ thick.
- The sMIM-C image shows that the upper region of the photocathode has a higher doping concentration.



0708201114_SMIMC_FRW_10.0u_512p_370466.png

Pixel Cross Section Analysis – X-Direction

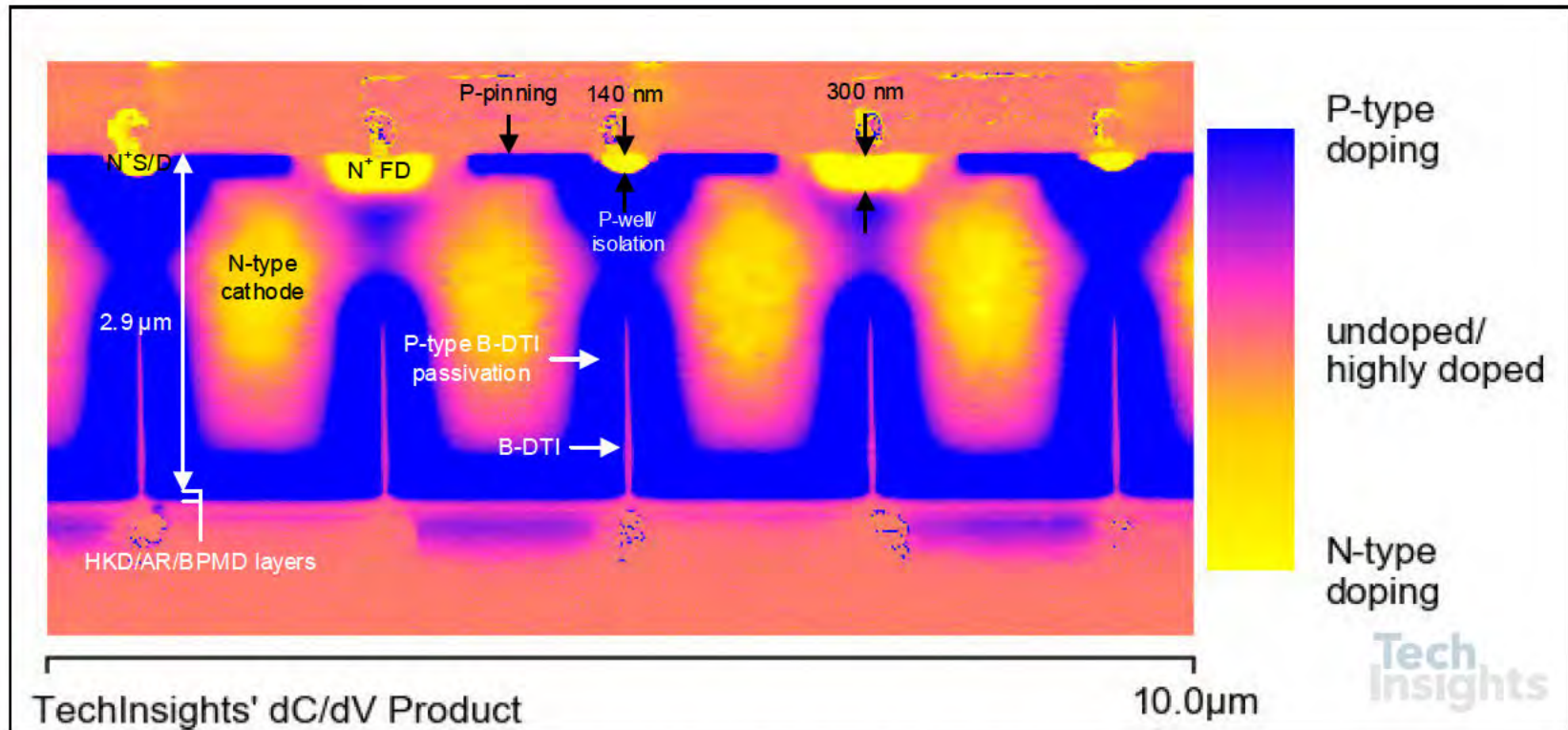


- SEM cross section overview image through section line F (FD)

470_CIS_PixelArray_FD_Strap_15K_370466.png

Pixel Cross Section Analysis – X-Direction

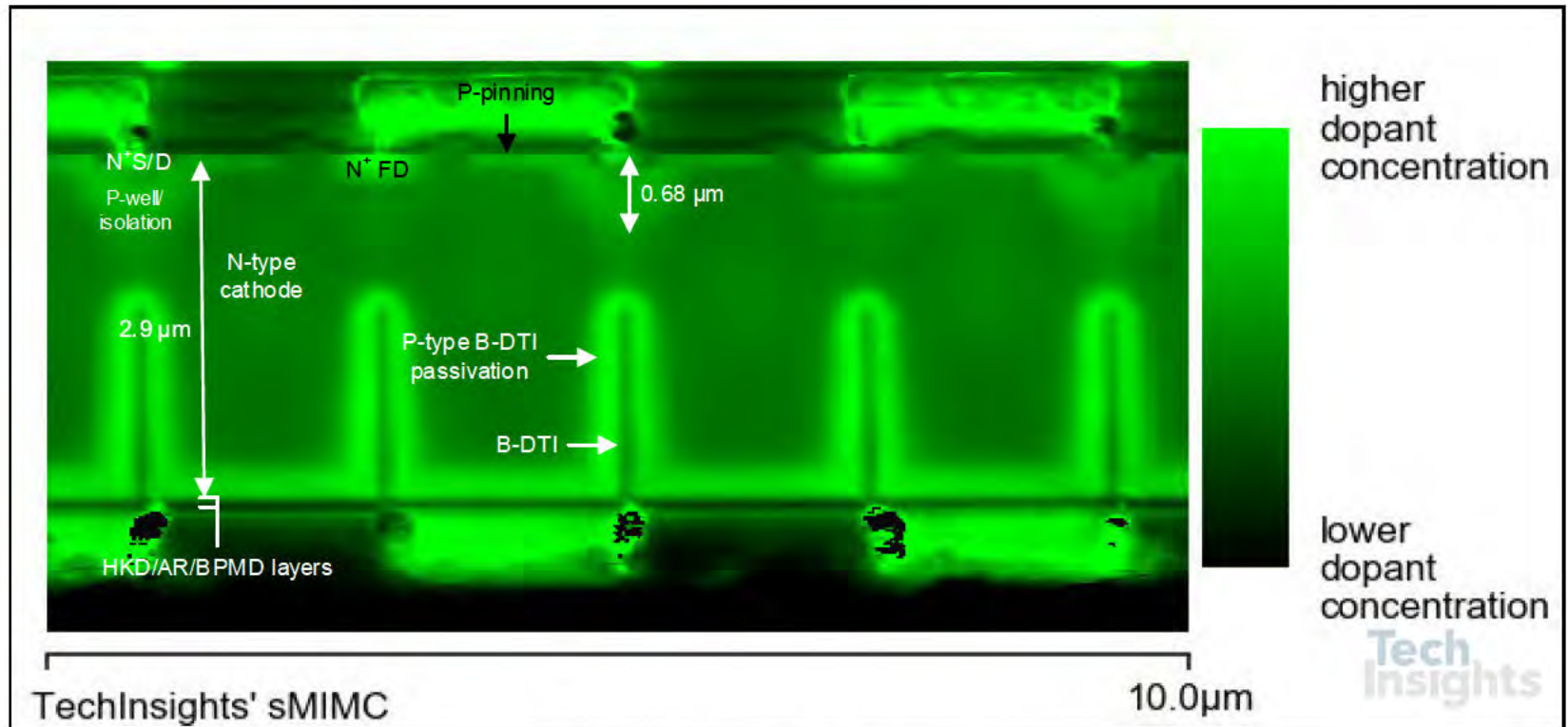
- SCM cross section image through section line F (FD)
- The N⁺ FD region is 300 nm deep, and the N⁺ S/D regions are 140 nm deep.



0711201032_PRODUCT_FRW_10.0u_512p_370466.png

Pixel Cross Section Analysis – X-Direction

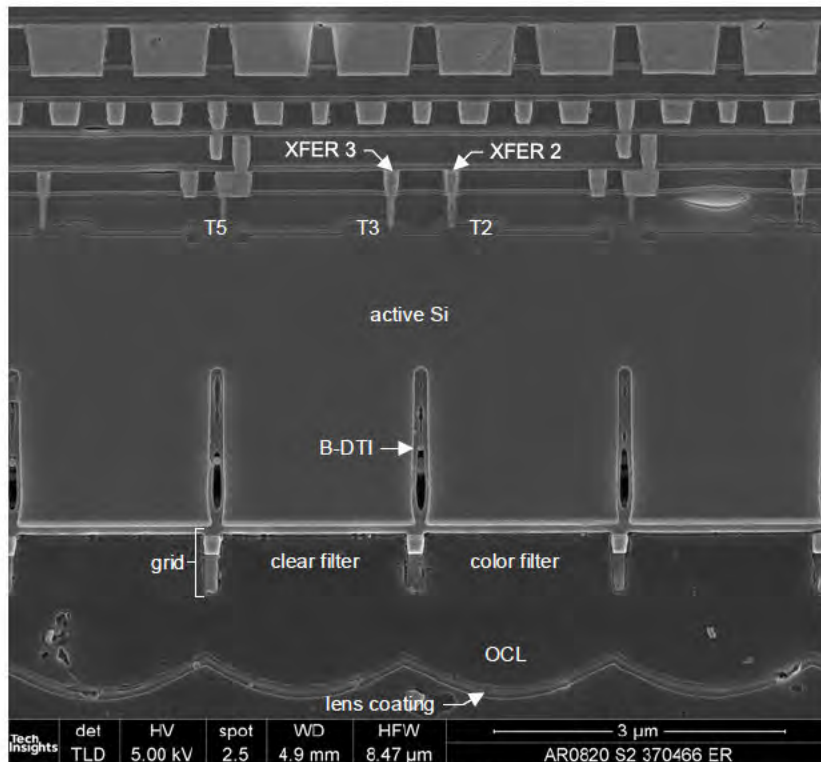
- sMIM-C cross section overview image through section line F (FD)
- The P-well/isolation region is $0.68\text{ }\mu\text{m}$ thick.



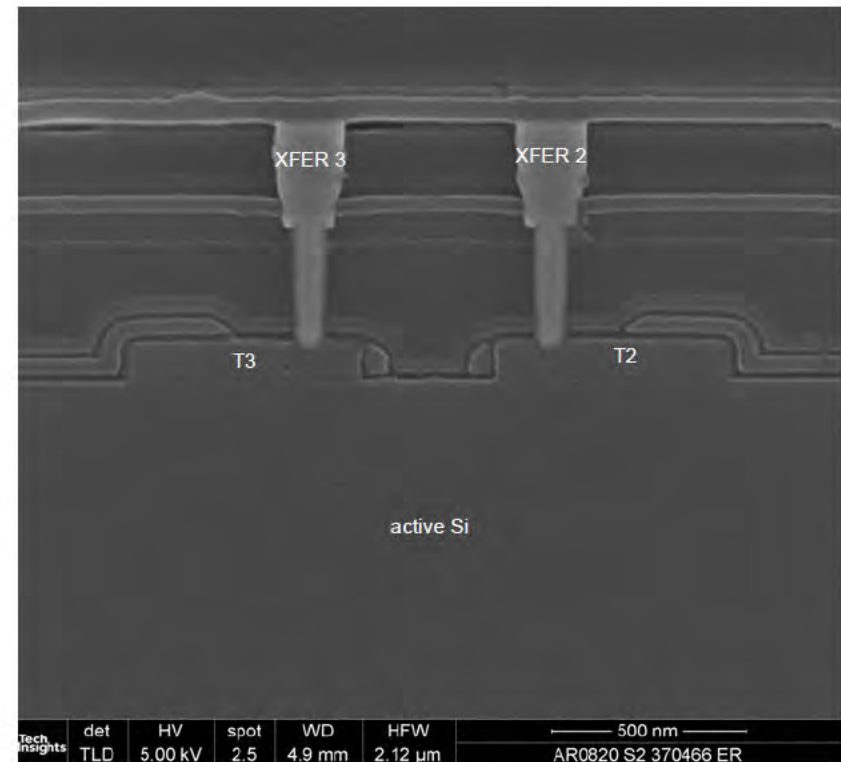
0711201032_SMIMC_FRW_10.0u_512p_370466.png

Pixel Cross Section Analysis – X-Direction

- SEM cross section overview and TEM detail images through section line G (T2 and T3 XFER gates)



486_CIS_PixelArray_T3-TG_T2-TG_15K_370466.png

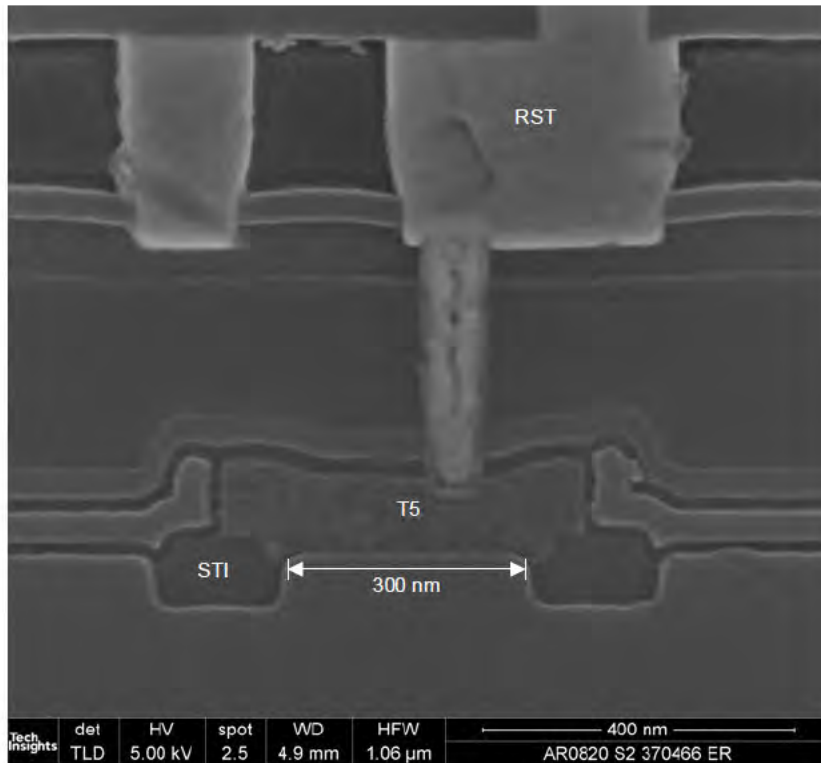


498_CIS_PixelArray_T4-TG_T1-TG_60K_370466.png

T2 and T3 XFER Gates Detail (Section Line G) – SEM

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Pixel Cross Section Analysis – X-Direction

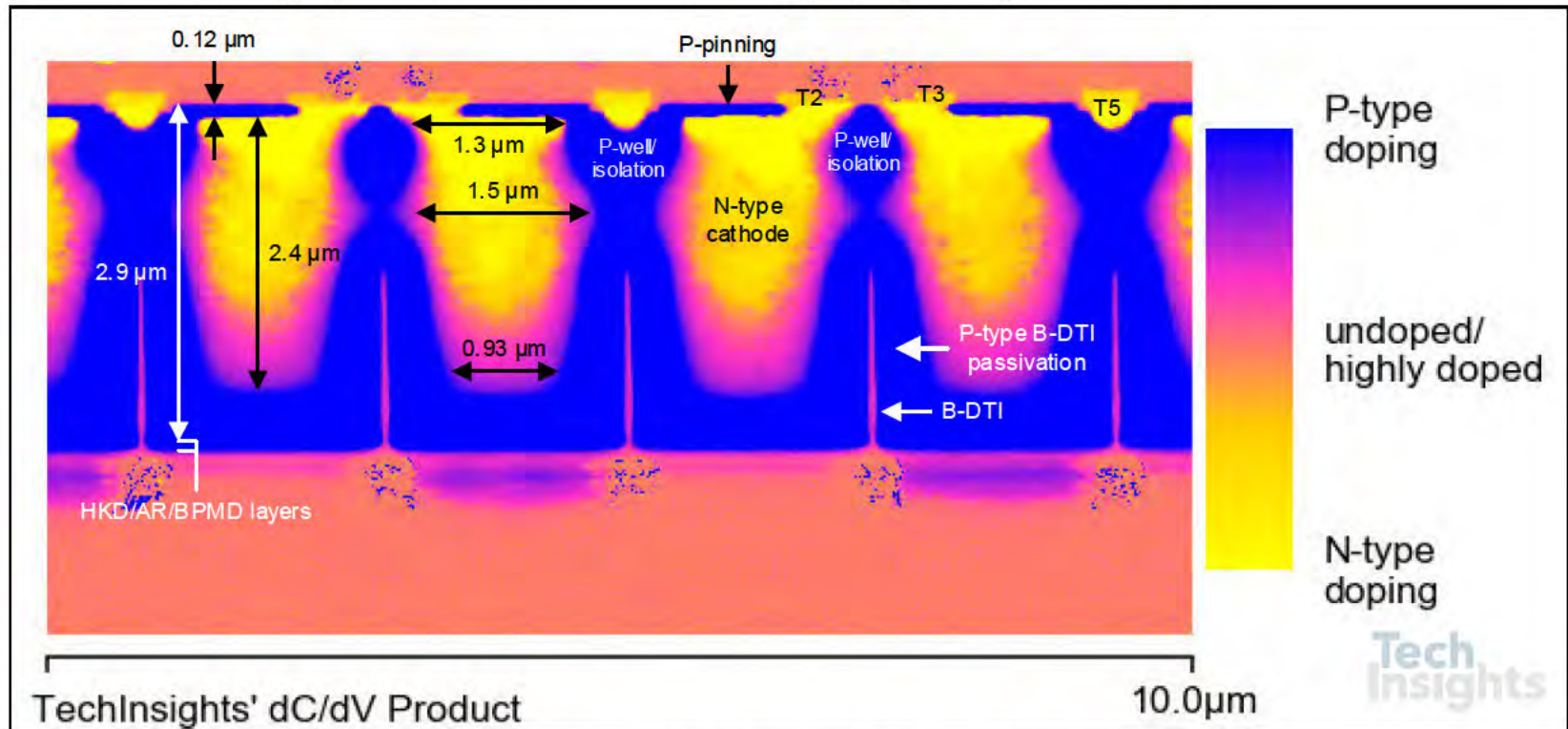


- SEM cross section overview image through section line G (T5 RST)
- T5 (RST) is 300 nm wide. It is the same width for T6, T7, and C1.

501_CIS_PixelArray_T5-RST_120K_370466

Pixel Cross Section Analysis – X-Direction

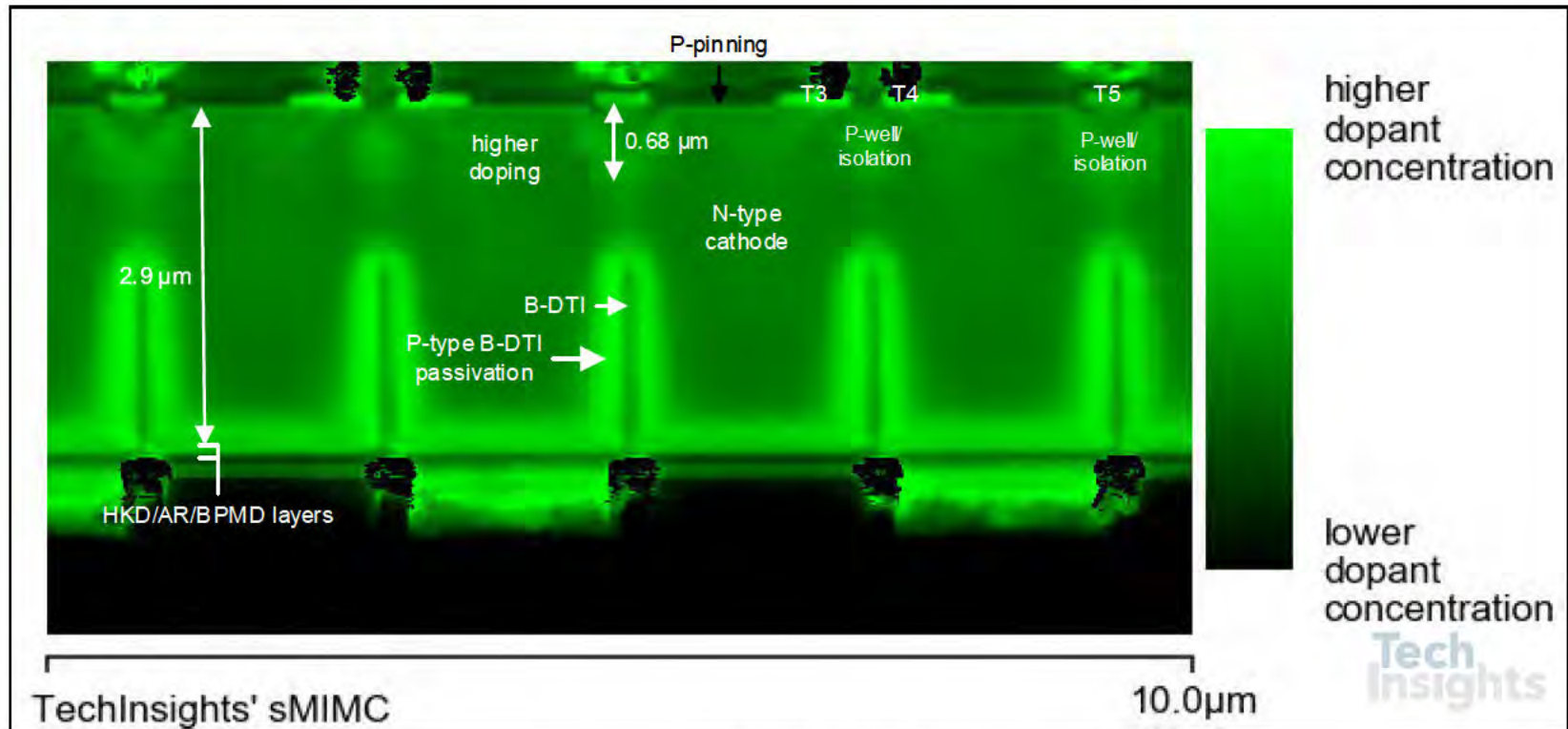
- SCM cross section image through section line G (T2 and T3 XFER gates).
- The N-type photocathode is 2.4 μm thick. As shown in the sMIM-C image on the next page, the top region of the photocathode has a higher doping concentration.
- The width of the N-type photocathode varies from 0.93-1.5 μm , depending on the location.



0711201114_PRODUCT_FRW_10.0u_512p_370466.png

Pixel Cross Section Analysis – X-Direction

- sMIM-C cross section overview image through section line G (T2 and T3 XFER gates)
- The P-well/isolation region is $0.68\ \mu\text{m}$ thick.
- The sMIM-C image shows that the upper and center regions of the photocathode have a higher doping concentration.



0711201114_SMIMC_FRW_10.0u_512p_370466.png

References

<https://www.onsemi.com/products/sensors/image-sensors-processors/image-sensors/ar0820at> (accessed July 15, 2020)

IISW 2011

Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

TechInsights calibrates length measurements on its scanning electron microscope (SEM), transmission electron microscope (TEM), and optical microscopes using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm ($\pm 1.4\%$) pitch, as certified by the NPL. TechInsights verifies every six months that its SEM and TEM are calibrated to within $\pm 2\%$ of this standard, over the full magnification ranges used.

TechInsights' optical microscopes are calibrated using a stage micrometer calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010). This standard has an expanded uncertainty of $0.3 \mu\text{m}$ (0.3%) for the stage micrometer's $100 \mu\text{m}$ pitch lines.

Random measurement errors, introduced during measurements of features on the calibrated images, yield an additional expanded uncertainty, which together with calibration uncertainty, is approximately $\pm 5\%$ or better for features larger than about 20% of the image width.

TechInsights camera systems, used for package photographs and teardown photographs, and TechInsights X-ray instruments are not calibrated. Package dimensions are measured physically with calipers.

The materials analysis reported in TechInsights reports is normally limited to approximate elemental composition, rather than stoichiometry. Quantification of energy dispersive spectroscopy (SEM-EDS and TEM-EDS) and TEM-based electron energy loss spectroscopy (TEM-EELS) materials analysis is usually not provided, unless otherwise stated. TechInsights will typically abbreviate the material composition, using only the elemental symbols (rather than full chemical formula) in approximate order of the peak heights in the spectra, but this does signify the relative concentration.

Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available. Spreading resistance profiling (SRP) data is typically calibrated. Scanning microwave impedance microscopy (sMIM) provides spatial information on the dopant type; however, it is not quantitative. The accuracy of other methods is available on request.

Statement of Scope Variation

Due to the nature of reverse engineering and the diversity of analyzed devices, there is a possibility of content variation in TechInsights technical reports.

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Complaints

[1:99-mc-09999 Plaintiff\(s\) v. Defendant\(s\)](#)

U.S. District Court

District of Delaware

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The following transaction was entered by Farnan, Brian on 4/21/2023 at 4:42 PM EDT and filed on 4/21/2023

Case Name: Plaintiff(s) v. Defendant(s)

Case Number: [1:99-mc-09999](#)

Filer:

Document Number: [364](#)

Docket Text:

COMPLAINT - Greenthread, LLC v. ON Semiconductor Corporation, Semiconductor Components Industries, LLC d/b/a ON Semiconductor LLC. Filing fee \$ 402, receipt number ADEDC-4118805. (Attachments: # (1) Exhibit 1, # (2) Exhibit 2, # (3) Exhibit 3, # (4) Exhibit 4, # (5) Civil Cover Sheet, # (6) Patent/Trademark Report, # (7) Rule 7.1 Disclosure Statement, # (8) Summons Forms - Unsigned)(Farnan, Brian)

1:99-mc-09999 Notice has been electronically mailed to:

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Original filename:n/a

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[STAMP dcecfStamp ID 1079733196 [Date 4/21/2023] [FileNumber 5197828-0] [67b08ce05c21fa6ad6b0a424ba20d4d64e795d3b375a926b50045f78186aedf74fed933de1b58141d246a6bb5f18a598263c7bed32de304b5594c17faa60d903]]

Document description:Exhibit 1

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[STAMP dcecfStamp ID 1079733196 [Date 4/21/2023] [FileNumber 5197828-1] [75db2500e3abb80fada344b48c4f8f49d6cc9c78ed011807c26b9e4bba452d7a6f0af2b04e44db602c18ce2b46a9fb9f37b16fe5863b6fc4e38f183edf38468c]]

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Original filename:n/a

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Document description:Exhibit 3

Original filename:n/a

Electronic document Stamp:

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Document description:Exhibit 4

Greenthread Ex. 2020, p. 249
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Original filename:n/a

Electronic document Stamp:

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Document description:Civil Cover Sheet

Original filename:n/a

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Document description:Patent/Trademark Report

Original filename:n/a

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Document description: Rule 7.1 Disclosure Statement

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