Trials@uspto.gov
571-272-7822

Paper 35
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PUBLIC VERSION

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,
Petitioner,

v.

GREENTHREAD LLC,
Patent Owner.

IPR2023-01242
Patent 11,121,222 B2

Before JON B. TORNQUIST, CHRISTOPHER M. KAISER, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

A. Background and Summary

Semiconductor Components Industries, LLC ("Petitioner") filed a petition for an *inter partes* review (Paper 2 ("Pet.")) challenging claims 1–9, 13–28, and 32–42 of U.S. Patent No. 11,121,222 B2 (Ex. 1001 ("the '222 patent")). In addition, Petitioner filed a paper explaining and ranking the parallel petitions challenging the '222 patent: the present Petition and the petition filed in IPR2023-01242. Paper 3. Greenthread, LLC ("Patent Owner") filed a Preliminary Response. Paper 18 ("Prelim. Resp."). With our authorization, Petitioner filed a Preliminary Reply (Paper 22, "Prelim. Reply"), and Patent Owner filed a Preliminary Sur-Reply (Paper 28, "Prelim. Sur-Reply").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted "unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons set forth below, we determine the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail with respect to at least one of the challenged claims. Accordingly, we institute an *inter partes* review on all claims and grounds challenged in the Petition.

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B. Real Parties-in-Interest

Each party identifies itself as a real party-in-interest. Pet. 1; Paper 5, 2. In addition, Petitioner identifies ON Semiconductor Corporation as a real party-in-interest. Pet. 1.

C. Related Matters

The parties identify several proceedings involving the '222 patent as related matters, including *Greenthread, LLC v. ON Semiconductor Corp.*, No. 1:23-cv-00443 (D. Del.); *Greenthread, LLC v. Western Digital Corp.*, No. 1:23-cv-00326 (D. Del.); *Greenthread, LLC v. Cirrus Logic, Inc.*, 1:23-cv-00369 (W.D. Tex.); *Greenthread, LLC v. Texas Instruments Inc.*, No. 2:23-cv-00157 (E.D. Tex.); *Greenthread, LLC v. OSRAM GmbH*, No. 2:23-cv-00179 (E.D. Tex.); *Greenthread, LLC v. OmniVision Technologies, Inc.*, No. 2:23-cv-00212 (E.D. Tex.); *Greenthread, LLC v. Monolithic Power Systems, Inc.*, No. 1:23-cv-00579 (D. Del.); *Greenthread, LLC v. Intel Corp.*, No. 6:22-cv-105 (W.D. Tex.); *Greenthread, LLC v. Intel Corp.*, No. 6:22-cv-01293 (W.D. Tex.); *Greenthread, LLC v. Micron Technology, Inc.*, No. 1:23-cv-00333 (D. Del.); *Intel Corp. v. Greenthread, LLC*, IPR2023-00420 (PTAB); *Intel Corp. v. Greenthread, LLC*, IPR2023-00552 (PTAB); *Dell Technologies Inc. v. Greenthread, LLC*, IPR2023-00509 (PTAB); and *Sony Group Corp. v. Greenthread, LLC*, IPR2023-00324 (PTAB). Pet. 1–3; Paper 5, 2–5. In addition, Petitioner challenges claim 44 of the '222 patent in IPR2023-01244, currently pending. Paper 3, 3. Further, Patent Owner identifies two additional matters involving the '222 patent: *Cirrus Logic, Inc. v. Greenthread, LLC*, IPR2024-00020 (PTAB); and *Cirrus Logic, Inc. v. Greenthread, LLC*, IPR2024-00021 (PTAB). Paper 16, 2.

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D. The '222 Patent

The '222 patent, titled "Semiconductor Devices with Graded Dopant Regions," issued on September 14, 2021. Ex. 1001, codes (45), (54). The '222 patent "relates to all semiconductor devices and systems." *Id.* at 1:23–24. According to the '222 patent, in bipolar junction transistors, "[e]fforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector" versus the standard "uniformly doped base." *Id.* at 1:34–48. This improvement has not been implemented in "most semiconductor devices, including various power MOSFETs [and] IGBT's," which "still use a uniformly doped 'drift epitaxial' region in the base." *Id.* at 1:48–53. The invention of the '222 patent implements graded dopant concentration in these devices, which causes "[t]wo important performance enhancements." *Id.* at 3:4–31. These include sweeping electrons "from source to drain rapidly" and simultaneously causing holes to "be recombined closer to the n^+ buffer layer," which "can improve t_{on} and t_{off} in the same device." *Id.* at 3:31–35.

E. Illustrative Claim

Of the challenged claims, claims 1, 21, 39, and 41–43 are independent. Claim 1 is illustrative and reproduced below.

> 1. A VLSI semiconductor device, comprising:
>
> a substrate of a first doping type at a first doping level having a surface;
>
> a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

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a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the VLSI semiconductor device.

Ex. 1001, 4:39–62.

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F. Asserted Unpatentability Challenges

Petitioner asserts that claims 1–9, 13–28, and 32–42 are unpatentable based on the following challenges:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–9, 13, 14, 16–21, 23–28, 32–42	103	Kawagoe[1]
1–9, 13, 14, 16–21, 23–28, 32–42	103	Kawagoe, Gupta[2]
1, 2, 4–9, 13–23, 25–28, 32–42	103	Wieczorek,[3] Wolf[4]
1, 2, 4–9, 13–23, 25–28, 32–42	103	Wieczorek, Wolf, Gupta
19, 37	103	Kawagoe, Silverbrook[5]
19, 37	103	Wieczorek, Wolf, Silverbrook

Petitioner relies on the declaration of Travis Blalock, Ph.D. (Ex. 1003, "Blalock Declaration").

II. ANALYSIS

A. Parallel Petitions

Petitioner filed two petitions challenging the '222 patent. Paper 3, 2. According to the Board's Patent Trial Practice Guide,[6] "one petition should

[1] US 6,043,114, issued Mar. 28, 2000 (Ex. 1007).

[2] US 6,163,877, issued Dec. 19, 2000 (Ex. 1014).

[3] US 2003/0183856 A1, published Oct. 2, 2003 (Ex. 1006).

[4] STANLEY WOLF & RICHARD N. TAUBER, SILICON PROCESSING FOR THE VLSI ERA, Vols. 1–4 (Lattice Press 2000) (Ex. 1008).

[5] US 6,614,560 B1, issued Sept. 2, 2003 (Ex. 1042).

[6] Patent Trial and Appeal Board Consolidated Trial Practice Guide (Nov. 2019), available at https://www.uspto.gov/TrialPracticeGuideConsolidated ("Trial Practice Guide").

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be sufficient to challenge the claims of a patent in most situations," but "there may be circumstances in which more than one petition may be necessary." Trial Practice Guide 59. Petitioner explains that the two petitions filed here have "material differences" including "mutually exclusive claim sets," "significant differences in claim scope between claims of the two claim sets," and "different prior art and prior art combinations to better address the difference in claim scope." Paper 3, 3. In addition, Petitioner notes that the petition in IPR2023-01242 addresses a potential claim-construction dispute, requiring that petition to be longer than it might otherwise be. *Id.* at 4. Patent Owner has not challenged Petitioner's arguments for the institution of multiple petitions, despite having an opportunity to do so. Prelim. Resp. 1–25; Trial Practice Guide 60–61.

On the present record, we agree with Petitioner that the two petitions filed to challenge the claims of the '222 patent will not substantially burden the Board or the parties. The petitions in IPR2023-01242 and IPR2023-01244 challenge different claims, and those claims appear on the present record to have different claim scope, as Petitioner argues. Paper 3, 3 (arguing that claim 44, challenged in IPR2023-01244, recites "a 'surface layer,' a 'single drift layer,' and 'at least one well region disposed in the single drift layer,' which are not" recited in the claims challenged in IPR2023-01242); Ex. 1001, 4:39–8:39. In addition, there is little overlap between the prior art asserted in the two petitions, and what overlap there is—the use of Kawagoe in both petitions—is used in different prior-art combinations in each petition. *Compare* IPR2023-01242, Paper 2, 5 (asserting Kawagoe alone and in combination with Gupta or Silverbrook), *with* IPR2023-01244, Paper 2, 5 (asserting Kawagoe in combination with

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Sakai). Further, as Petitioner notes, the oral hearing (if requested) and depositions in the two proceedings may be combined, which would further reduce the burden placed on the Board and the parties. Accordingly, we do not exercise our discretion to deny either of the petitions challenging the '222 patent for being parallel petitions.

B. Legal Standards

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). The burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A claim is unpatentable under 35 U.S.C. § 103 if "the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains." 35 U.S.C. § 103. The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when present, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To show obviousness, it is not enough to merely show that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). "Rather, obviousness requires the additional showing that

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a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and development to yield the claimed invention." *Id.* (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007)). "This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *KSR*, 550 U.S. at 418–19. On the other hand, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.* at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). Nevertheless, "[a] factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning." *KSR*, 550 U.S. at 421.

C. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art "would have had a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience." Pet. 5–6 (citing Ex. 1003 ¶ 48). According to Petitioner, "[a]dditional education might compensate for less experience, and vice-versa." *Id.* On the present record, Patent Owner does not contest Petitioner's definition of a person of ordinary skill in the art. Prelim. Resp. 1–25.

In light of the record before us, and for purposes of this Decision, we adopt Petitioner's proposal regarding the level of ordinary skill in the art.

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Based on our review of the '222 patent and the prior art of record, we determine that the definition offered by Petitioner comports with the qualifications a person would have needed to understand and implement the teachings of the '222 patent and the prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required "where the prior art itself reflects an appropriate level and a need for testimony is not shown") (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

D. Claim Construction

In an *inter partes* review, we construe claim terms according to the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2022). Under *Phillips*, claim terms are afforded "their ordinary and customary meaning." *Phillips*, 415 F.3d at 1312. "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1313. "Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Neither party proposes any claim terms for construction. Pet. 6; Prelim. Resp. 1–25. After considering the arguments and information presented in the Petition and Preliminary Response, we agree that we do not need to construe any terms expressly in order to determine whether to institute trial. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am.*

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Sci. & Eng'g, Inc., 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.")).

E. Timeliness of Petition Under 35 U.S.C. § 315(b)

Patent Owner argues that "[t]he Petition should be dismissed because it is untimely." Prelim. Resp. 1. Specifically, Patent Owner argues that Petitioner is in privity with [redacted] who Petitioner asserts are time-barred under 35 U.S.C. § 315(b). *Id.* at 1–25. [redacted] *Id.* at 1 (quoting *Taylor v. Sturgell*, 553 U.S. 880, 894 (2008)). Further, Patent Owner argues, [redacted] Therefore, Petitioner has a [redacted] giving rise to privity." *Id.* at 1–2 (quoting *Taylor*, 553 U.S. at 895; *Applications in Internet Time, LLC v. RPX Corp.*, 897 F.3d 1336, 1360 (Fed. Cir. 2018)).

1. Legal Standard

"[T]he mere existence of some relationship between a petitioner and another entity is not sufficient" to place that petitioner in privity with that entity. *Google LLC v. DDC Technology, LLC*, IPR2023-00707, Paper 27 at 37 (PTAB Oct. 25, 2023). Instead, "that relationship must be related to [an earlier] lawsuit and be sufficiently close that it can be fairly said the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit." *Id.* In other words, privity concerns "whether the petitioner

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and the prior litigant's relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit," or "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319 (Fed. Cir. 2018).

A petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1244 (Fed. Cir. 2018). In order to raise such a dispute, "a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy]." *Id.* The amount of evidence a patent owner must produce does not rise to the level of that required to overcome a burden of production. *Id.* at 1244 n.8. Instead, the "burden remains with the petitioner to establish" the timeliness of its petition. *Id.* at 1242.

2. Whether We May Consider Petitioner's Preliminary Reply

As noted above, we authorized Petitioner to file a Preliminary Reply and Patent Owner to file a Preliminary Sur-Reply, both limited to addressing the issue of the timeliness of the Petition. Patent Owner argues that consideration of Petitioner's Preliminary Reply "is not appropriate," because "Petitioner could have reasonably foreseen" the timeliness arguments raised in the Preliminary Response when Petitioner was "filing its petition." Prelim. Resp. 23 (quoting *Sandoz Inc. v. Abbvie Biotechnology Ltd.*, IPR2018-00002, Paper 11 at 3 (PTAB Mar. 6, 2018)).

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We disagree with this argument raised by Patent Owner. According to the Federal Circuit, a petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds*, 903 F.3d at 1244. Thus, there is no requirement that a petitioner preemptively address a disputed issue of privity in its petition.

We also find that Patent Owner's foreseeability argument is factually unsupported. Although Patent Owner argues [redacted] Without more information, the [redacted] would not have suggested Patent Owner's privity argument because Petitioner was not involved in either one.

Accordingly, we consider Petitioner's Preliminary Reply, as well as Patent Owner's Preliminary Sur-Reply, in determining whether Petitioner has shown its Petition is timely.

3. The Effect of the Earlier Suit [redacted] *on the Timeliness of the Present Petition*

Patent Owner alleges that [redacted] are time-barred under § 315(b). Prelim. Resp. 1. [redacted] the present record does not contain any evidence tending to show that this is the case. Section 315(b) bars institution of *inter partes* review only when "the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent." On this record, there is no evidence that [redacted] any earlier than January 23,

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2023, which is less than one year before the filing of the present petition on July 27, 2023. *Compare* Pet. 89, *with* Ex. 2019, 1. Accordingly, the service of [redacted] time-barred under § 315(b).

Patent Owner also argues that, [redacted] Prelim. Sur-Reply 10 (citing *Kofax Inc. v. Uniloc USA Inc.*, IPR2015-01207, Paper 24 at 4–5 (PTAB July 20, 2016)); *see* Prelim. Resp. 1–3 [redacted] In *Kofax*, the Board held that the real party-in-interest of a petitioner in a first *inter partes* review could be estopped under § 315(e)(1) from seeking institution of a second *inter partes* review once a final written decision had been issued in the first review. *Kofax*, IPR2015-01207, Paper 22 at 10–11. Sections 315(b) and 315(e)(1) both apply not only to the petitioner, but also the "real party in interest, or privy of the petitioner." Patent Owner implicitly argues that the ruling in *Kofax* should extend § 315(b) beyond its limits to bar [redacted] Prelim. Sur-Reply 10. We see nothing in the Board's decision in *Kofax* that would justify extending § 315(b) so far beyond its statutory text, and Patent Owner provides us with none. Thus, Patent Owner has produced no evidence that [redacted] under § 315(b).[7]

[7] In the next five subsections, [redacted]

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4. [redacted]
Preceding and Succeeding Owners of Property

Patent Owner argues that [redacted] in the form of goods that either infringe the challenged patent's claims [redacted] because [redacted] Prelim. Resp. 13–17. It is true that entities who are "preceding and succeeding owners of property" can be in privity with one another. *Taylor*, 553 U.S. at 894. But it is also true that this rule does not extend to the point where all manufacturers of allegedly infringing goods are in privity with the customers who buy those goods. *See, e.g.*, *WesternGeco*, 889 F.3d at 1319–22 (the parties "had a contractual and fairly standard customer-manufacturer relationship regarding the accused product," which "does not necessarily suggest that the relationship is sufficiently close that both" parties should be considered to be in privity); *Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1340–41 (Fed. Cir. 2018) (same); *Samsung Electronics Co. Ltd. v. Netlist Inc.*, IPR2022-00615, Paper 64, at 22–26 (PTAB June 30, 2023) (same). Thus, to the extent that Patent Owner has produced evidence that [redacted] none of that evidence tends to show [redacted] Even if a manufacturer-customer relationship with respect to accused products were evidence of privity, [redacted]

[redacted] provides additional support for our conclusion regarding Patent Owner's § 315(b) argument.

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because Patent Owner asserts unequivocally that Prelim. Resp. 10.

5.

Patent Owner argues . Prelim. Resp. 16–17 (citing *Ventex Co. v. Columbia Sportswear North America, Inc.*, IPR2017-00651, Paper 148 (PTAB Jan. 24, 2019) (precedential)). We disagree. Unlike the agreements in *Ventex*, Paper 148 at 12, Even if Petitioner were considered [8]

[8] In contract law, a third-party beneficiary is not a privy. *See, e.g., Pac. Gas & Elec. Co. v. United States*, 838 F.3d 1341, 1350–51 (Fed. Cir. 2016) ("Limited exceptions to the privity requirement have been recognized when a 'party standing outside of privity by contractual obligation stands in the shoes of a party within privity,' such as when a party can demonstrate that it was an intended third-party beneficiary under the contract."); *Prime Finish, LLC v. Cameo, LLC*, 487 F. App'x 956, 959 (6th Cir. 2012) ("Ordinarily, the obligations arising out of a contract are due only to those with whom it is made; a contract cannot be enforced by a person who is not a party to it or in privity with it, except . . . under certain circumstances, [such as] by a third-party beneficiary.").

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6. [redacted]

Patent Owner argues that the doctrine of patent exhaustion [redacted] Prelim. Resp. 17. According to Patent Owner, [redacted] *Id.* We disagree. It is true that [redacted] against any claim of infringement by Patent Owner. We do not see how such a defense [redacted]

7. [redacted]

Patent Owner argues that [redacted] Prelim. Resp. 18–19. As evidence of this alleged indemnification obligation, Patent Owner directs us to Petitioner's "Standard Terms and Conditions of Sale." *Id.* at 18 (citing Ex. 2010, 3). This evidence shows that Petitioner "agrees to defend any claim, suit or proceeding asserted against Buyer based upon a claim that any Product(s) . . . directly infringes any patent . . . effective in the USA and to pay settlements or costs and damages finally awarded in any such suit." Ex. 2010, 3. This agreement is contingent on Petitioner being "promptly notified in writing of the claim and given, at [Petitioner's] request and expense, sole control of the defense or response to such claim and all requested reasonable assistance by Buyer for defense of the same." *Id.* Moreover, Petitioner has the "sole discretion to (i) obtain for Buyer the right

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to use and sell the Product, (ii) replace or modify the Product(s) with non-infringing Product(s), or (iii) accept the return of the Product(s) and refund the purchase price less reasonable wear and tear" in lieu of defending against any infringement claim. *Id.*

An agreement by a petitioner to indemnify a third party in an earlier infringement suit can give rise to a privity relationship between the petitioner and that third party. *Intel Corp. v. U.S. Int'l Trade Comm'n*, 946 F.2d 821, 839 (Fed. Cir. 1991). But not all indemnification agreements create privity between the parties to the agreement. An indemnification agreement does not give rise to privity where the indemnitor has the option either "to pay for any litigation defense expenses or for any damages related to infringement" or, in the alternative, "to modify or replace the equipment if an infringement claim [is] made," as opposed to being required "to defend [the indemnitee] from a patent infringement lawsuit, reimburse or pay for a lawsuit, cover any damages liability for any adverse patent infringement verdict against [the indemnitee], or initiate an invalidity challenge in one or more fora." *WesternGeco*, 889 F.3d at 1321. This describes precisely the option Petitioner has under the Standard Terms and Conditions of Exhibit 2010. Accordingly, we determine that, on the present record, the indemnification agreement of Exhibit 2010 does not [redacted].

Patent Owner speculates that, as [redacted] might have "received terms [even more] generous [than] the 'Standard' conditions [Petitioner] offers to any purchaser." Prelim. Resp. 18. But Patent Owner does not direct us to any such more generous terms in the evidence presently of record. *Id.* at 18–19.

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"A mere assertion that a third party is an unnamed [privy], without any support for that assertion, is insufficient to put the issue into dispute." *Worlds*, 903 F.3d at 1244. Moreover, Patent Owner does not dispute Petitioner's assertion that [redacted] with respect to Patent Owner's lawsuit [redacted]. Prelim. Reply 6. Thus, on the present record, Patent Owner has not directed us to any evidence that an indemnification obligation creates [redacted].

8. [redacted]

Patent Owner argues that Petitioner is [redacted] Prelim. Resp. 3–4, 19–20. Patent Owner argues that, "by making accused products [redacted] Petitioner acts within the definition of an agent by acting as "[s]omeone who is authorized to act for or in place of another." *Id.* at 20 (quoting Ex. 2041, 1) (second alteration in original). We disagree for three reasons.

First, Patent Owner's agency argument is not based on the applicable legal standard. For purposes of privity under § 315(b), the relevant question is whether [redacted] in filing a petition for *inter partes* review. The applicable principle is that "preclusion is appropriate when a nonparty later brings suit as an agent for a party who is bound by a judgment." *Taylor*, 553 U.S. at 895. As the Federal Circuit explains, the rationale behind § 315(b)'s time bar is "to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation." *WesternGeco*, 889 F.3d at 1319. Therefore,

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the relevant question is "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *Id.* Here, Patent Owner does not assert that [redacted] in this proceeding. Any such assertion would be appropriate only based on evidence that [redacted] *See Taylor*, 553 U.S. at 906 (cautioning that "preclusion is appropriate only if the putative agent's conduct of the suit is subject to the control of the party who is bound by the prior adjudication"). No such evidence is in this record.

Second, the case law cited by Patent Owner does not apply.[9] In each case, the alleged privy was the party asserting a defense of res judicata or collateral estoppel, not the party against whom collateral estoppel was asserted, as is the case here.[10] The privity issue was whether the party raising a res judicata or collateral estoppel defense was in privity with a defendant in a prior lawsuit brought by the same plaintiff. In *Herrion*, for example, the plaintiff brought successive lawsuits arising out of the same incident, and the defendants in the second suit asserted a res judicata defense. 448 F. App'x at 72. Applicable res judicata law required the court

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[9] Prelim. Resp. 19–20 (citing *Herrion v. Children's Hosp. Nat. Med. Ctr.*, 786 F. Supp. 2d 359 (D.D.C.), *aff'd*, 448 F. App'x 71 (D.C. Cir. 2011); *John Street Leasehold, LLC v. Cap. Mgmt. Res., L.P.*, 283 F.3d 73 (2d Cir. 2002); *Fiumara v. Fireman's Fund Ins. Companies*, 746 F.2d 87 (1st Cir. 1984)).

[10] By asserting Petitioner is time-barred under § 315(b), Patent Owner is in effect asserting a collateral estoppel bar against Petitioner. *See WesternGeco*, 889 F.3d at 1318 ("Privity is essentially a shorthand statement that collateral estoppel is to be applied in a given case." (citing Consolidated Trial Practice Guide November 2019 at 15, available at https://www.uspto.gov/TrialPracticeGuideConsolidated)).

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to consider whether the defendants in the second lawsuit were in privity with the defendant in the first lawsuit. *Id.* at 72–73 (finding privity existed for res judicata purposes). Similarly, in *John Street*, the court held that plaintiff's second lawsuit was barred by res judicata in part because the defendants were in privity with the defendants in the prior action. 283 F.3d at 75. Likewise in *Fiumara*, the court held that "the res judicata defense is unmistakably available" to the defendants "as persons in privity with" the defendants in a prior lawsuit brought by the same plaintiff. 746 F.2d at 92. The privity issue in each of these cases was entirely different from this case, where Patent Owner asserts that Petitioner is barred because Petitioner is in privity with the defendants in the prior lawsuit.

Third, even if Patent Owner's argument were on solid legal footing, it lacks factual support in the record. An "essential element[] of agency" is "the principal's 'right to direct or control the agent's actions.'" *In re Google LLC*, 949 F.3d 1338, 1345 (Fed. Cir. 2022) (quoting *Meyer v. Holley*, 537 U.S. 280, 286 (2003)). Patent Owner does not argue in the Preliminary Response that [redacted], much less direct us to any evidence that would tend to prove the existence of such a right. Prelim. Resp. 19–20. In the Preliminary Sur-Reply, Patent Owner argues that [redacted] because [redacted] Prelim. Sur-Reply 8 (citing Ex. 2010, 5; Ex. 2053) (alterations in original). Patent Owner does not, however, present any evidence that Petitioner manufactures products [redacted] *Cf. Google*, 949 F.3d at 1346 (contracts to "[a]ssembl[e] equipment based on information and instructions provided by Google" were

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"suggestive of an agency relationship" (first alteration in original)). Patent Owner also does not allege that any particular product [redacted] *See* Ex. 2010, 5 (providing different cancelation policies for "standard Product[s]" than for "Custom Product[s]"); Ex. 2053, 1 (touting Petitioner's ability to supply "System-on-Chip (SoC), Application Specific Integrated Circuit (ASIC), and other custom solutions," but not identifying any particular such products). Thus, Patent Owner does not direct us to any evidence that Petitioner [redacted]

9. Conclusion as to Timeliness of Petition

As noted above, privity concerns "whether the petitioner and the prior litigant's relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit," or "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *WesternGeco*, 889 F.3d at 1319. A petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds*, 903 F.3d at 1244. In order to raise such a dispute, "a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy]." *Id.* Here, Patent Owner argues that it has produced such evidence in several respects, but, on the present record, none of the evidence in question tends to show [redacted]

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F. Challenges Based on Kawagoe

Petitioner contends claims 1–9, 13, 14, 16–21, and 23–28, and 32–42 would have been obvious in view of Kawagoe or in view of the combination of Kawagoe and Gupta. Pet. 5–45, 78–83. On the present record, Patent Owner does not dispute Petitioner's arguments. Prelim. Resp. 1–25.

1. Kawagoe

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device using an epitaxial wafer, i.e., a semiconductor wafer having a semiconductor single crystal epitaxial layer grown over a polished semiconductor substrate. Ex. 1007, 1:13–27, 2:31–35. According to Kawagoe, "[t]he epitaxial wafer is advantageous in that it is excellent in suppressing the soft errors and resisting to the latchup,"[11] as well as "drastically reduc[ing] the defect density of the gate insulating film" of a semiconductor integrated device. *Id.* at 1:33–40.

Kawagoe discloses various "representative" processes, including processes in which the single crystal (epitaxial) layer contains an impurity of the same type and in the same concentration as the substrate body. Ex. 1007, 2:55–3:9. According to Kawagoe, the impurity concentration of the substrate body can be made higher than that of epitaxial layer "so that

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[11] Petitioner submits Exhibit 1009 (Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Int'l Conf on VLSI Design, 429–434, IEEE 2008), which explains that "soft errors" are "random and not related to permanent hardware faults" and "[t]heir causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation)," including "alpha particles [that] are emitted when the nucleus of an unstable isotope decays to a lower energy state." Ex. 1009, Abstract, 430. Dr. Blalock characterizes "latchup" as "a 'short-circuit' failure condition in poorly designed circuits." Ex. 1003 ¶ 77.

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the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup." *Id.* at 4:1–8. Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device including a step of forming a semiconductor region (well) extending below the epitaxial layer and having an impurity concentration that decreases with increasing depth below the epitaxial layer. *Id.* at 3:10–25. According to Kawagoe, the well can be used for forming a complementary Metal-Oxide-Semiconductor.Field-Effect-Transistor ("MOS.FET") circuit. *Id.* at 3:32–38.

Kawagoe describes seven embodiments, including Embodiment 1 (Ex. 1007, 6:41–12:40, Figs. 1–8) and Embodiment 4 (*id.* at 14:46–19:64, Figs. 16–25). According to Embodiment 1, a semiconductor integrated circuit device includes semiconductor substrate body 2S, epitaxial layer 2E, and gettering layer 2G. *Id.* at 6:51–56, Fig. 1. Substrate body 2S and epitaxial layer 2E are doped with p-type impurity in equal concentrations. *Id.* at 6:60–7:3, 10:51–55, 11:12–16. Embodiment 1 includes n-channel MOS.FET ("nMOS") 4N and p-channel MOS.FET ("pMOS") 4P, the latter being formed in n-well 6, which is doped with n-type impurity and extends below the epitaxial layer. *Id.* at 8:46–52, 9:32–40, 11:18–24, 11:43–50, Figs. 1, 5, 7.

According to Embodiment 4, substrate body 2S and epitaxial layer 2E are doped with p-type impurity, and the impurity concentration of substrate body 2S is higher than that of epitaxial layer 2E "to improve the resistance to the latchup." Ex. 1007, 14:64–15:6, 15:13–17, 16:16–21, 19:59–63, Fig. 17. Embodiment 4 includes p-well 6*p* formed with nMOS 4N and n-well 6*n* formed with pMOS 4P. *Id.* at 15:26–40, 17:40–18:35, Figs. 16,

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21–23. In Embodiment 4, the impurity concentration in p-well 6*p* and n-well 6*n* decreases with increasing depth below the epitaxial layer. *Id.* at 15:62–16:15, 17:55–61, Fig. 17. Kawagoe discloses that the concentration gradient reduces soft errors by attracting carriers (electrons) to the substrate and preventing them from entering the p-well. *Id.* at 16:2–11.

Petitioner relies on Kawagoe Figures 17 and 23, which are reproduced below and illustrate Embodiment 4 and its properties.

FIG. 17

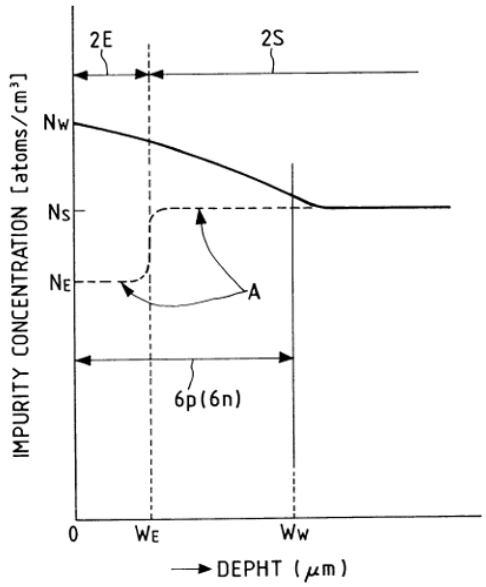

FIG. 23

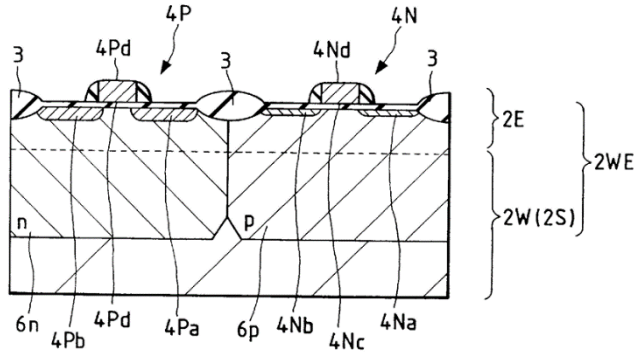

Figure 17 is a plot of impurity concentration as a function of depth in a semiconductor integrated circuit device, which shows "the p-well 6*p* and n-well 6*n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer 2E." Ex. 1007, 5:41–45, 15:62–16:40. Figure 23 shows a step in a process for manufacturing a semiconductor integrated circuit device, including p-well 6*p* formed with

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nMOS 4N and n-well 6*n* formed with pMOS 4P. *Id.* at 5:1–4, 15:26–32, 18:3–35.

2. Gupta

Gupta "relates to the field of complimentary metal oxide semiconductor (CMOS) circuits, and more particularly to automatically producing layouts for CMOS circuits." Ex. 1014, 1:7–10. According to Gupta, "[a]s semiconductor chips become ever larger, incorporating ever more devices, it becomes increasingly important to minimize semiconductor area used by a given number of devices." *Id.* at 1:28–31. Doing so "potentially [saves] millions of dollars." *Id.* at 1:31–34. To accomplish this goal, Gupta discloses abutting multiple transistors to "form transistor chains." *Id.* at 2:17–21, Fig. 4.

3. Analysis

Petitioner argues that Kawagoe or the combination of Kawagoe and Gupta would have taught or suggested the limitations of the challenged claims and that a person of ordinary skill in the art would have had reason to combine the teachings of Kawagoe and Gupta. Pet. 5–45, 78–83. On the present record, Patent Owner does not disagree. Prelim. Resp. 1–25.

a) Claim 1

The preamble of claim 1 recites "[a] VLSI semiconductor device." Ex. 1001, 4:39. Petitioner argues that Kawagoe teaches the preamble. Pet. 6–8. Patent Owner does not dispute this argument. Prelim. Resp. 1–25. Kawagoe discloses "a semiconductor integrated circuit device." Ex. 1007, 1:15–16, 14:50–51. In particular, Kawagoe discloses "4 Megabit Dynamic RAM" devices. *Id.* at 19:15–18. Dr. Blalock testifies that such devices have "millions of transistors." Ex. 1003 ¶ 68. Petitioner also directs us to

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evidence that "a VLSI semiconductor device means a device consisting of at least one million active elements," where "an active element is a semiconductor transistor." Ex. 1016, 73. Thus, Petitioner has shown sufficiently that Kawagoe teaches the preamble of claim 1.

Claim 1 recites "a substrate of a first doping type at a first doping level having a surface." Ex. 1001, 4:40–41. Relying on a combination of Kawagoe's Embodiment 1 and Embodiment 4, Petitioner argues that Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 8–13; Prelim. Resp. 1–25. Petitioner contends that "a substrate of a first doping type" is taught by Kawagoe's epitaxial substrate, including epitaxial layer 2E and substrate body 2S doped with p-type impurity, and that the recited "surface" corresponds to the top surface of the epitaxial substrate. Pet. 8–9 (citing Ex. 1007, 6:50–7:3, 14:61–15:12, 17:10–18:38, Figs. 20, 23). Petitioner contends that the recitation, "at a first doping level," is taught by Kawagoe's Embodiment 1, which has a uniformly-doped epitaxial substrate, with epitaxial layer 2E and substrate body 2S having the same impurity concentration. Pet. 10 (citing Ex. 1007, code (57), 2:57–3:9, 6:60–7:3). Petitioner contends that a POSITA would have understood that Kawagoe teaches forming a twin-well CMOS device on either a uniformly doped epitaxial substrate, as described in Embodiment 1, or a non-uniformly doped latchup-resistant epitaxial substrate, as described in Embodiment 4. Pet. 10 (citing Ex. 1003 ¶ 74). Relying on Dr. Blalock's testimony and various prior art disclosures, Petitioner contends that a POSITA would have been motivated to use a uniformly-doped epitaxial substrate to form a twin-well CMOS device and would have had a reasonable expectation of success. Pet. 10–13 (citing

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Ex. 1003 ¶¶ 75–80; Ex. 1007, 1:33–40, 2:57–65, 8:40–52, 12:8–40, 14:58–60, 15:7–40, 19:49–63, Fig. 23; Ex. 1008, 381, 387–89, 406, 419, 523, 530; Ex. 1026, 1). We find that Petitioner's contention for this limitation is sufficiently supported for purposes of institution.

Claim 1 recites "a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed." Ex. 1001, 4:42–45. Petitioner argues that Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 13–16; Prelim. Resp. 1–25. Kawagoe discloses "semiconductor regions 4Na and 4Nb . . . for forming the source-drain regions of the nMOS 4N." Ex. 1007, 8:66–67, Fig. 23. Petitioner contends that Kawagoe's semiconductor regions 4Na and 4Nb (corresponding to the "first active region") have a doping type (n-type) opposite to the doping type (p-type) of the substrate. Pet. 14. Kawagoe discloses that these regions "are doped with an n-type impurity such as phosphor[us] (P) or arsenic (As)." *Id.* at 8:67–9:3. Petitioner directs us to evidence tending to show that source-drain regions 4Na and 4Nb, as well as the channel region between those regions and below insulating film 4Nc all would have been considered part of an active region. Ex. 1008B, 299–300 ("The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions."). Thus, Petitioner has shown sufficiently that Kawagoe teaches this limitation of claim 1.

Claim 1 recites "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed." Ex. 1001, 4:46–48. Petitioner argues that Kawagoe teaches this limitation, and Patent Owner does not dispute this

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argument. Pet. 16–18; Prelim. Resp. 1–25. Kawagoe discloses "semiconductor regions 4Pa and 4Pb . . . for forming the source-drain regions of the pMOS 4P." Ex. 1007, 9:47–48, Fig. 23. These regions "are doped with a[] p-type impurity such as boron." *Id.* at 9:48–50. Petitioner directs us to evidence that source-drain regions 4Pa and 4Pb, as well as the channel region between those regions and below insulating film 4Pc all would have been considered part of an active region. Ex. 1008B, 299–300 ("The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions."). This active region is separate from and disposed adjacent to the first active region. Ex. 1007, Fig. 23. Thus, Petitioner has shown sufficiently that Kawagoe teaches this limitation of claim 1.

Claim 1 recites "transistors formed in at least one of the first active region or second active region." Ex. 1001, 4:49–50. Petitioner argues that Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 18;[12] Prelim. Resp. 1–25. Kawagoe discloses forming transistors 4N and 4P, each in an active region, as discussed above. Ex. 1007, 8:66–9:3, 9:47–50, Fig. 23. Petitioner notes that the disclosure of

[12] Petitioner's entire argument with respect to this limitation is a cross-reference to another portion of the Petition. Pet. 18. Specifically, Petitioner directs us to "§§VIII.A.1.c-d." *Id.* We note that these sections of the Petition do not exist. It is clear from context, however, that Petitioner intended to direct us to § VII.A.1.c–d of the Petition, where Petitioner discusses the formation of the nMOS 4N and pMOS 4P transistors. Accordingly, we treat Petitioner's citation as directing us to the portion of the Petition to which Petitioner intended to direct us. Similar errors occur throughout the Petition. *See, e.g.*, Pet. 29, 30, 37, 55, 64, 71, 72. For similar reasons, we treat these errors the same way.

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Kawagoe satisfies claim 1's recitation of "transistors" either under Patent Owner's district court construction of "transistors" as requiring one or more transistors or under an alternative construction requiring multiple transistors in each active region. Pet. 14 ("a POSITA would have understood that Kawagoe teaches forming multiple nMOS transistors in this [first active] region to minimize chip area, as good layout practice dictates"), 17 ("a POSITA would have understood that Kawagoe teaches forming multiple pMOS transistors in this [second active] region"), 79 (citing Ex. 1003 ¶¶ 82, 87; Ex. 1014, 1:52–54, 2:17–21, Fig. 23; Ex. 1020, 31).

Petitioner further argues that, under the alternative construction requiring the presence of multiple transistors in each active region, Kawagoe in combination with Gupta teaches this limitation. *Id.* at 79–83. Gupta discloses "[t]ransistors which are abutted in a layout [so as to] form transistor chains," noting that "[i]t is desirable to produce a layout with a maximum number of transistors chained" and that such a layout helps to "minimize semiconductor area used by a given number of devices," which "potentially . . . [saves] millions of dollars." Ex. 1014, 1:28–34, 2:17–21, Fig. 4. Petitioner also argues that a person of ordinary skill in the art would have combined the teachings of Gupta with those of Kawagoe in order to achieve Gupta's benefit of "high packing density" of transistors while still achieving "the additional benefit of improved immunity to soft errors through appropriate well doping" of Kawagoe. Pet. 81. Thus, Petitioner has shown sufficiently that either Kawagoe alone or the combination of Kawagoe and Gupta teaches or suggests the "transistors" limitation of claim 1, as well as that a person of ordinary skill in the art would have had reason to combine the teachings of Kawagoe with those of Gupta.

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Claim 1 recites "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions." Ex. 1001, 4:51–55. Petitioner argues that Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 18–23; Prelim. Resp. 1–25. Kawagoe discloses its wells "hav[ing] their impurity concentrations gradually lowered in the depthwise direction from the principal surface . . . of the epitaxial layer 2E." Ex. 1007, 15:62–16:2, Figs. 17, 23. Petitioner directs us to evidence that tends to show that these depthwise variations in impurity concentrations include the channel regions of each active region and that such variations in impurity concentrations sweep carriers down into the substrate, away from any active regions. Ex. 1003 ¶ 91; Ex. 1007, Figs. 17, 23; Ex. 1016, 289–90. Thus, Petitioner has shown sufficiently that Kawagoe teaches this limitation of claim 1.

Claim 1 recites "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions." Ex. 1001, 4:56–60. Petitioner argues that Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 23–28; Prelim. Resp. 1–25. Kawagoe discloses its wells "hav[ing] their impurity concentrations gradually lowered in the depthwise direction from the principal surface . . . of the epitaxial layer 2E." Ex. 1007, 15:62–16:2, Figs. 17, 23. Petitioner directs us to evidence that tends to show that these depthwise variations in impurity concentrations sweep carriers down into the substrate, away from any active regions.

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Ex. 1007, Figs. 17, 23; Ex. 1016, 289–90. Thus, Petitioner has shown sufficiently that Kawagoe teaches this limitation of claim 1.

Claim 1 recites "wherein at least some of the transistors form digital logic of the VLSI semiconductor device." Ex. 1001, 4:60–62. Petitioner argues that Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 28; Prelim. Resp. 1–25. Kawagoe discloses a "semiconductor integrated circuit device" that can be a "DRAM," "a flash memory," or "a logic circuit." Ex. 1003 ¶ 108; Ex. 1007, 20:1–33, 22:10–29, 24:28–31. Thus, Petitioner has shown sufficiently that Kawagoe teaches this limitation of claim 1.

b) Remaining Claims

In view of our determination that Petitioner establishes a reasonable likelihood for claim 1, and because Petitioner's arguments and evidence for remaining claims 2–9, 13, 14, 16–21, and 23–28, and 32–42 (Pet. 28–45) are similar to Petitioner's arguments and evidence for claim 1 (Pet. 6–28) and are unopposed at this stage by Patent Owner, we determine that it is unnecessary to provide an explicit analysis of Petitioner's challenges to the remaining claims in order to provide guidance to the parties for the upcoming trial. Consolidated Trial Practice Guide November 2019 ("CTPG")[13] at 64; *see* 37 C.F.R. § 42.108(a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim."); *see also SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60

[13] *Available at* https://www.uspto.gov/TrialPracticeGuideConsolidated.

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(2018) (holding that 35 U.S.C. § 314 forbids the Board's prior "partial institution" practice).

G. Challenges Based on the Combination of Wieczorek and Wolf

Petitioner contends claims 1, 2, 4–9, 13–23, 25–28, and 32–42 would have been obvious in view of the combination of Wieczorek and Wolf or in view of the combination of Wieczorek, Wolf, and Gupta. Pet. 5, 45–83. On the present record, Patent Owner does not dispute Petitioner's arguments. Prelim. Resp. 1–25.

1. Wieczorek

Wieczorek relates "to a semiconductor device, such as a field-effect transistor, having an improved retrograde dopant profile in a channel region of the transistor element." Ex. 1006 ¶ 2. The Petition relies on Wieczorek's description of the prior art, not its disclosed improvement. Pet. 11, 40.

Wieczorek explains that a retrograde channel dopant profile is one where "the concentration of dopants increases from the gate insulation layer to the areas located deeper down the channel region." Ex. 1006 ¶ 6. According to Wieczorek, a retrograde channel dopant profile is desirable, but "very difficult to obtain." *Id.* Wieczorek states that "the dopant concentration immediately after the implantation process exhibits a desired retrograde dopant profile" (*id.* ¶ 9), but during heat treatment, "the initially retrograde profile in the vicinity of the surface of the semiconductor device . . . may have become substantially uniformly distributed" due to diffusion of the dopant atoms (*id.* ¶ 11).

Petitioner relies on Figures 1b and 2b (reproduced below), which Wieczorek uses to illustrate the prior art.

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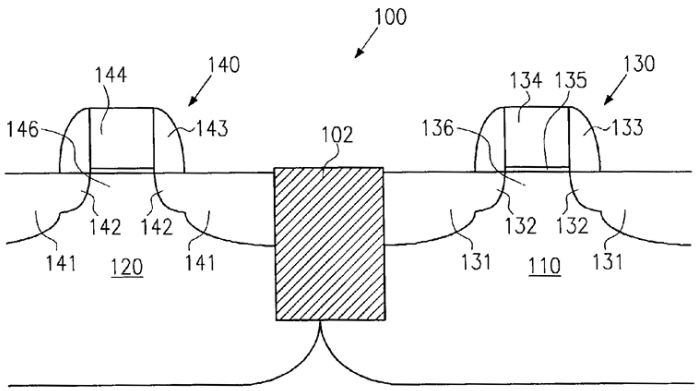

FIG.1b
(Prior Art)

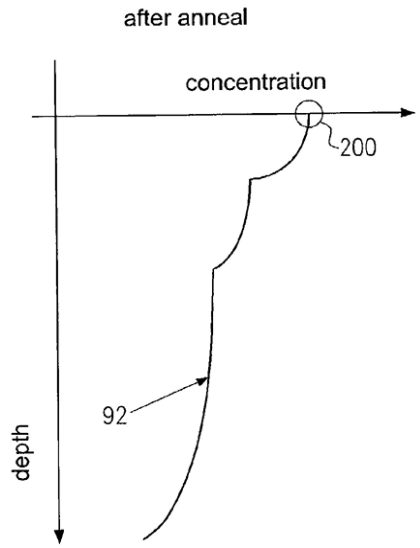

FIG.2b
(Prior Art)

Wieczorek Figure 1b shows a conventional semiconductor device at an intermediate manufacturing stage, including shallow trench isolation 102 separating N-well structure 120 from P-well structure 110. Ex. 1006 ¶¶ 7, 20. The device includes P-channel transistor 140 with source and drain regions 141 in N-well structure 120 and N-channel transistor 130 with source and drain regions 131 in P-well structure 110. *Id.* ¶ 12. Wieczorek Figure 2b is a graph of dopant concentration versus depth of N-well structure 120 and P-well structure 110 and shows "a typical dopant profile with respect to the depth of the respective well structure" after ion implantation and heat treatment. *Id.* ¶¶ 9–11, 13, 21.

2. Wolf

Wolf is a four-volume textbook titled "Silicon Processing for the VLSI Era." Ex. 1008. A portion of the textbook focuses on CMOS technology. Ex. 1008A, 807–40.

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3. *Analysis*

Petitioner argues that the combination of Wieczorek and Wolf or the combination of Wieczorek, Wolf, and Gupta would have taught or suggested the limitations of the challenged claims and that a person of ordinary skill in the art would have had reason to combine the teachings of Wieczorek and Wolf or those of Wieczorek, Wolf, and Gupta. Pet. 5, 45–83. On the present record, Patent Owner does not disagree. Prelim. Resp. 1–25.

a) Reason to Combine Wieczorek and Wolf

Petitioner argues that a person of ordinary skill in the art would have had a reason to combine the teachings of Wieczorek with those of Wolf. Pet. 45. On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 1–25. Petitioner argues specifically that Wieczorek discloses "a conventional prior-art CMOS device" and that "Wolf is a well-known textbook that teaches known fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS devices." Pet. 45. Wieczorek discloses "[a] typical process flow for forming the semiconductor device 100" which is "a complementary MOS transistor pair." Ex. 1006 ¶ 12, Fig. 1b. Petitioner directs us to evidence that a person of ordinary skill in the art would have looked to Wolf for details on how to manufacture the conventional CMOS devices of Wieczorek. Ex. 1003 ¶ 138; Ex. 1008A, 807–40. Accordingly, Petitioner has shown sufficiently, for purposes of this decision, that a person of ordinary skill in the art would have had a reason to combine the teachings of Wieczorek with those of Wolf.

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b) Claim 1

The preamble of claim 1 recites "[a] VLSI semiconductor device." Ex. 1001, 4:39. Petitioner argues that the combination of Wieczorek and Wolf teaches the preamble. Pet. 45–47. Patent Owner does not dispute this argument. Prelim. Resp. 1–25. Wieczorek discloses a "semiconductor device." Ex. 1006 ¶ 12, Fig. 1b. Wolf discloses that such devices include microprocessors, DRAM, and flash memory, each with at least one million transistors. Ex. 1008A, Fig. 1; Ex. 1008B, 596–97, 633–35. Petitioner also directs us to evidence that "a VLSI semiconductor device means a device consisting of at least one million active elements," where "an active element is a semiconductor transistor." Ex. 1016, 73. Thus, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches the preamble of claim 1.

Claim 1 recites "a substrate of a first doping type at a first doping level having a surface." Ex. 1001, 4:40–41. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation, and Patent Owner does not dispute this argument. Pet. 47–50; Prelim. Resp. 1–25. Wolf discloses that its twin-well CMOS devices "are formed . . . on a lightly doped substrate . . . of *n* or *p* material. Ex. 1008C, 530, Fig. 8-1(e). The substrates of Wieczorek and Wolf both have surfaces. Ex. 1006, Fig. 1b; Ex. 1008C, 525, Fig. 8-1(e). Relying on Dr. Blalock's testimony, Petitioner contends that "a POSITA would have found it obvious to use a uniformly doped n- or p-type substrate ('a substrate of a first doping type at a first doping level') as a suitable substrate for Wieczorek's CMOS device in Figure 1b." Pet. 48–49 (citing Ex. 1003 ¶ 143). Thus, Petitioner has shown

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sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

Claim 1 recites "a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed." Ex. 1001, 4:42–45. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation, and Patent Owner does not dispute this argument. Pet. 50–53; Prelim. Resp. 1–25. Petitioner contends that, "[b]ecause the source-drain regions of the first active region are N-doped, Wieczorek-Wolf's first active region has a second doping type (N-type) opposite in conductivity to the first doping type (P-type) of the substrate." Pet. 52 (citing Ex. 1003 ¶ 147; Ex. 1006 ¶ 12). Wieczorek discloses "N-channel transistor 130" that includes "heavily N-doped source and drain regions 131" and "channel region 136." Ex. 1006 ¶ 12; *see id.* ¶ 4 (describing "field effect transistor[s]" generally as having the same parts). Wolf discloses that the source-drain and the channel region between those regions would have been considered part of an active region. Ex. 1008B, 299–300 ("The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions."). Thus, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

Claim 1 recites "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed." Ex. 1001, 4:46–48. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation, and Patent Owner does not dispute this argument. Pet. 53–55; Prelim. Resp. 1–25. Wieczorek discloses "P-channel transistor 140" that includes "heavily P-

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doped source and drain regions 141" and "channel region 146." Ex. 1006 ¶¶ 4, 13. Wolf discloses that the source-drain and the channel region between those regions would have been considered part of an active region. Ex. 1008B, 299–300 ("The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions."). This active region is separate from and disposed adjacent to the first active region. Ex. 1006, Fig. 1b. Thus, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

Claim 1 recites "transistors formed in at least one of the first active region or second active region." Ex. 1001, 4:49–50. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation, and Patent Owner does not dispute this argument. Pet. 55; Prelim. Resp. 1–25. Wieczorek discloses forming transistors N-channel and P-channel transistors, each in an active region, as discussed above. Ex. 1006 ¶¶ 12–13, Fig. 1b. Petitioner notes that the disclosure of Wieczorek and Wolf satisfies claim 1's recitation of "transistors" either under Patent Owner's district court construction of "transistors" as requiring one or more transistors or under an alternative construction requiring multiple transistors in each active region. Pet. 52 ("a POSITA would have understood that Wieczorek teaches forming multiple nMOS transistors in the first active region to minimize chip area, as good layout practice dictates"), 55 ("a POSITA would have understood that Wieczorek teaches forming multiple pMOS transistors in the second active region"), 79 (citing Ex. 1003 ¶¶ 148, 153; Ex. 1006 ¶ 4; Ex. 1014, 1:52–54, 2:17–21; Ex. 1020, 31).

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Petitioner further argues that, under the alternative construction requiring the presence of multiple transistors in each active region, Gupta teaches this limitation. *Id.* at 79–83. Gupta discloses "[t]ransistors which are abutted in a layout [so as to] form transistor chains," noting that "[i]t is desirable to produce a layout with a maximum number of transistors chained" and that such a layout helps to "minimize semiconductor area used by a given number of devices," which "potentially . . . [saves] millions of dollars." Ex. 1014, 1:28–34, 2:17–21, Fig. 4. Petitioner also argues that a person of ordinary skill in the art would have combined the teachings of Gupta with those of Wieczorek and Wolf because doing so would have amounted to no more than the "use of a known technique . . . to improve similar devices . . . in the same way," and Petitioner directs us to evidence that this is the case. Pet. 81–82 (citing Ex. 1003 ¶ 205). Thus, Petitioner has shown sufficiently that either the combination of Wieczorek and Wolf or the combination of Wieczorek, Wolf, and Gupta teaches or suggests this limitation of claim 1, as well as that a person of ordinary skill in the art would have had reason to combine the teachings of Wieczorek and Wolf with those of Gupta.

Claim 1 recites "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions." Ex. 1001, 4:51–55. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation, and Patent Owner does not dispute this argument. Pet. 55–60; Prelim. Resp. 1–25. The channel region of Wieczorek's transistors exhibits graded dopant concentration, with the concentration decreasing with

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increasing depth away from the surface. Ex. 1006 ¶¶ 11, 13, Figs. 1b, 2b. Petitioner directs us to evidence that tends to show that these depthwise variations in impurity concentrations sweep carriers down into the substrate, away from any active regions. Ex. 1003 ¶ 159; Ex. 1010, 2:27–32, 5:14–22; Ex. 1016, 289–90. Thus, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

Claim 1 recites "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions." Ex. 1001, 4:56–60. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation, and Patent Owner does not dispute this argument. Pet. 60–62; Prelim. Resp. 1–25. Wieczorek's P-well exhibits gradually decreasing dopant concentration with increasing depth away from the surface. Ex. 1006 ¶¶ 9, 11, 13, Figs. 1b, 2b. Petitioner directs us to evidence that tends to show that these depthwise variations in impurity concentrations sweep carriers down into the substrate, away from any active regions. Ex. 1003 ¶ 165; Ex. 1010, 2:27–32, 5:14–22; Ex. 1016, 289–90. Thus, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

Claim 1 recites "wherein at least some of the transistors form digital logic of the VLSI semiconductor device." Ex. 1001, 4:60–62. Petitioner argues that the combination of Wieczorek and Wolf teaches this limitation, and Patent Owner does not dispute this argument. Pet. 62–63; Prelim. Resp. 1–25. Petitioner directs us to evidence that Wieczorek's structure "was understood by a [person of ordinary skill in the art] to form digital

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logic gates." Ex. 1003 ¶ 168; Ex. 1006 ¶¶ 7, 26; Ex. 1008A, 810–11. Thus, Petitioner has shown sufficiently that the combination of Wieczorek and Wolf teaches this limitation of claim 1.

c) Remaining Claims

In view of our determination that Petitioner establishes a reasonable likelihood for claim 1, and because Petitioner's arguments and evidence for remaining claims 2, 4–9, 13–23, 25–28, and 32–42 (Pet. 64–78) are similar to Petitioner's arguments and evidence for claim 1 (Pet. 45–63) and are unopposed at this stage by Patent Owner, we determine that it is unnecessary to provide an explicit analysis of Petitioner's challenges to the remaining claims in order to provide guidance to the parties for the upcoming trial. CTPG at 64; 37 C.F.R. § 42.108(a); *SAS*, 138 S. Ct. at 1359–60.

H. Challenges Based on Silverbrook

Petitioner contends claims 19 and 37 would have been obvious in view of the combination of Kawagoe and Silverbrook or in view of the combination of Wieczorek, Wolf, and Silverbrook. Pet. 5, 83–85. On the present record, Patent Owner does not dispute Petitioner's arguments. Prelim. Resp. 1–25.

1. Silverbrook

Silverbrook "relates substantially to the concept of a disposable camera having instant printing capabilities." Ex. 1042, 1:8–9. Part of Silverbrook's camera is an "Image Capture and Processing Chip" that performs "CMOS image sensing." *Id.* at 6:41–49. The CMOS image sensing is accomplished by "a CMOS active pixel sensor array" manufactured using a "CMOS/DRAM/APS process." *Id.* at 6:50–55.

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2. Analysis

Petitioner argues that the combination of Kawagoe and Silverbrook or the combination of Wieczorek, Wolf, and Silverbrook would have taught or suggested the limitations of the challenged claims and that a person of ordinary skill in the art would have had reason to combine the teachings of the references. Pet. 5, 83–85. On the present record, Patent Owner does not disagree. Prelim. Resp. 1–25.

Claim 19 depends from claim 1, and claim 37 depends from claim 21; each recites a limitation requiring that "the device [be] an image sensor." Petitioner argues that Silverbrook teaches this limitation, and Patent Owner does not dispute this argument. Pet. 84; Prelim. Resp. 1–25. Silverbrook discloses a "CMOS image sensor." Ex. 1042, 6:41–67. Thus, Petitioner has shown sufficiently that Silverbrook teaches this limitation.

Petitioner argues that a person of ordinary skill in the art would have had a reason to combine the teachings of Silverbrook either with those of Kawagoe or with those of Wieczorek and Wolf. Pet. 83–85. On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 1–25. Petitioner argues specifically that "Silverbrook calls for a 'CMOS' image sensor, but does not include any details about the fabrication of CMOS devices," forcing a person of ordinary skill in the art "to implement the CMOS . . . designs disclosed by Kawagoe and Wieczorek-Wolf." Pet. 84. Petitioner directs us to evidence that this is the case. Ex. 1003 ¶ 210; Ex. 1042, 7:28–30; Ex. 1044, 1, Fig. 2. Accordingly, Petitioner has shown sufficiently, for purposes of this decision, that a person of ordinary skill in the art would have had a reason to combine the teachings of Silverbrook with those of Kawagoe or with those of Wieczorek and Wolf.

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III. CONCLUSION

Upon consideration of the Petition, the Preliminary Response, the Preliminary Reply, the Preliminary Sur-Reply, and the evidence presented, we determine that Petitioner has shown a reasonable likelihood that it will prevail in showing that at least one of the challenged claims is unpatentable. In addition, we are persuaded on the present record that the Petition is not time-barred under 35 U.S.C. § 315(b). Accordingly, we institute an *inter partes* review of all challenged claims based on the grounds asserted in the Petition.

IV. ORDER

For the reasons given, it is:

ORDERED that an *inter partes* review is instituted with respect to the grounds asserted in the Petition;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision;

FURTHER ORDERED that, in view of the pending motion to seal, this Decision is being filed "Board and Parties Only"; and

FURTHER ORDERED that after conferring with Petitioner, Patent Owner shall, within one week of this Decision, submit to the Board via email to Trials@uspto.gov, a version of this Decision to be filed on the public record, with any redactions proposed by either party.

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For PETITIONER:

Roger Fulghum
Mark Speegle
BAKER BOTTS L.L.P.
Roger.Fulghum@BakerBotts.com
Mark.Speegle@BakerBotts.com

Daniel Anderson
Daniel.Anderson@andersonpatents.com

For PATENT OWNER:

Alan Whitehurst
Nicholas T. Matich
Arvind Jairam
Stuart McCommas
Archis "Neil" Ozarkar
MCKOOL SMITH, P.C.
awhitehurst@mckoolsmith.com
nmatich@mckoolsmith.com
ajairam@mckoolsmith.com
smccommas@mckoolsmith.com
nozarkar@mckoolsmith.com

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