



UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC.,
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

IPR2024-00263
Patent 11,316,014 B2

Before JON B. TORNQUIST, MONICA S. ULLAGADDI, and
JULIA HEANEY, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Semiconductor Components Industries, LLC. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–9 and 13–28 of U.S. Patent No. 11,316,014 B2 (Ex. 1001, “the ’014 patent”). Paper 1 (“Pet.”). Greenthread, LLC (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 13 (“Prelim. Resp.”). With authorization, Petitioner subsequently filed a Preliminary Reply (Paper 15, “Prelim. Reply”) and Patent Owner filed a Preliminary Sur-reply (Paper 18, “Prelim. Sur-reply”).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence set forth by Petitioner and Patent Owner, we determine that the information presented in the Petition demonstrates a reasonable likelihood that Petitioner would prevail on at least one of the challenged claims of the ’014 patent. Accordingly, we institute an *inter partes* review as to all of the challenged claims of the ’014 patent on all of the grounds of unpatentability set forth in the Petition.

II. BACKGROUND

A. *Related Matters*

The parties indicate that the ’014 patent is at issue in the following proceedings:

Greenthread, LLC v. Cirrus Logic, Inc., No. 1:23-cv-00369 (W.D. Tex. filed March 31, 2023);

Greenthread, LLC v. Texas Instruments Inc., No. 2:23-cv-00157 (E.D. Tex. filed April 6, 2023);

Greenthread, LLC v. OSRAM GmbH, No. 2:23-cv-00179 (E.D. Tex. filed April 19, 2023);

Greenthread, LLC v. OmniVision Technologies, Inc., No. 2:23-cv-00212 (E.D. Tex. filed May 10, 2023);

Greenthread, LLC v. Monolithic Power Systems, Inc., No. 1:23-cv-00579 (D. Del. filed May 26, 2023); and

Cirrus Logic v. Greenthread, LLC, IPR2024-00019, filed October 27, 2023 (instituted on May 28, 2024). Paper 4, 2–3 (Patent Owner’s mandatory notices); Pet. 1–2.

B. Real Parties-in-Interest

Petitioner identifies itself and ON Semiconductor Corporation as the real parties-in-interest. Pet. 1. Patent Owner identifies itself as the real party-in-interest. Paper 4, 1.

C. The '014 patent

The '014 patent, titled “Semiconductor Devices with Graded Dopant Regions,” issued on April 26, 2022. Ex. 1001, codes (45), (54). The '014 patent “relates to all semiconductor devices and systems,” including Bipolar Junction Transistors (BJT). *Id.* at 1:39–52.

The '014 patent explains that in bipolar junction transistors, minority carriers are the principal device conduction mechanism, but majority carriers also play a small but finite role in modulating the conductivity in such devices. Ex. 1001, 1:50–54. The '014 patent further explains that “[e]fforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier’s speed from emitter to collector.” *Id.* at 1:62–64. The '014 patent explains that this improvement has not been implemented in most semiconductor devices, including various power

MOSFETs and IGBTs, which “still use a uniformly doped ‘drift epitaxial’ region in the base.” *Id.* at 1:64–2:2. The ’014 patent implements a graded dopant concentration in these devices, which results in at least two important performance enhancements: “electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n+ buffer layer,” thereby improving “ t_{on} and t_{off} in the same device.” *Id.* at 3:42–47.

Figure 1 of the ’014 patent is reproduced below.

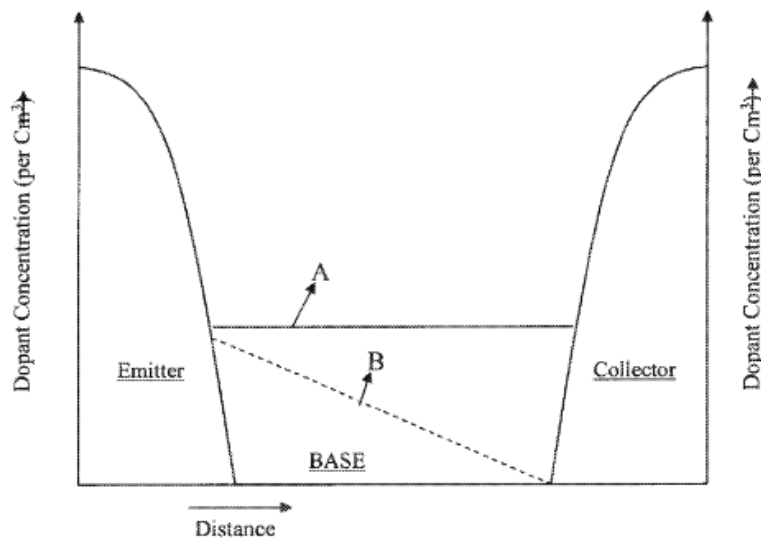


Figure 1 is labeled “Prior Art” and “illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base (“A”) and graded base (“B”).” Ex. 1001, 2:40–43, Fig. 1.

Figure 3A of the '014 patent is reproduced below.

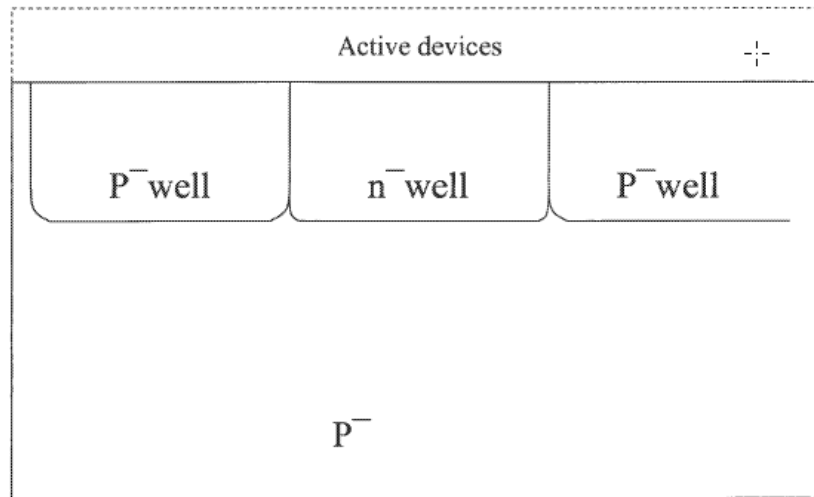


Figure 3A is labeled “Prior art” and shows a cross section of “a typical prior art IC with two wells (one n- well in which p-channel transistors are subsequently fabricated and one p-well in which n-channel transistors are subsequently fabricated).” Ex. 1001, 2:46–51, Fig. 3A.

Figure 5A of the '014 patent is reproduced below.

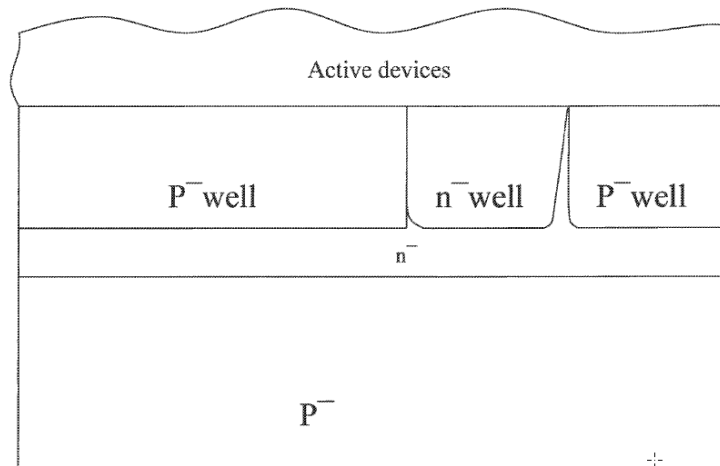


Figure 5A illustrates a cross section of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention to improve performance in each application. Ex. 1001, 2:58–61. In this

embodiment, “the subterranean n^- layer has a graded donor concentration” as may the n^- and p^- wells. *Id.* at 4:1–9

According to the '014 patent, “[s]purious minority carriers can be generated by clock switching in digital VLSI logic and memory ICs.” Ex. 1001, 3:51–52. The '014 patent states that these “unwanted carriers can discharge dynamically-held ‘actively held high’ nodes,” and serve to degrade performance of various types of devices, including CMOS digital images and DRAMs. *Id.* at 3:51–59. According to the '014 patent, “a novel technique is described” that “creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible.” *Id.* at 3:64–4:1. For example, a graded donor concentration in subterranean n^- layer may be used to “sweep the minority carriers deep into the substrate.” *Id.* at 4:1–3.

D. Illustrative Claim

Claims 1 and 21 are independent, with challenged claims 2–9 and 13–20 depending from claim 1 and challenged claims 22–28 depending from claim 21. Ex. 1001, 4:49–6:56. Claim 1 is representative of the challenged claims and is reproduced below.

1. An electronic system, the system comprising:

at least one semiconductor device, the at least one semiconductor device including:

a substrate of a first doping type at a first doping level having a surface;

a first active region disposed adjacent the surface with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first and second active regions towards an area of the substrate where there are no active regions; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface towards the area of the substrate where there are no active regions, wherein at least some of the transistors form digital logic of the semiconductor device.

Ex. 1001, 4:49–5:7 (spacing added to aid readability).

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 6):¹

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–9, 13, 14, 16–28	103(a)	Kawagoe ²
1, 2, 4–9, 13–23, 25–28	103(a)	Wieczorek ³ , Wolf ⁴

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, took effect on March 16, 2013. The ’014 patent claims priority to an application filed September 3, 2004. Ex. 1001, code (60). Thus, we apply the pre-AIA version of §103. See Pet. 5 n.1.

² US 6,043,114, issued Mar. 28, 2000 (Ex. 1007).

³ US 2003/0183856 A1, published Oct. 2, 2003 (Ex. 1006).

⁴ Stanley Wolf & Richard N. Tauber, *Silicon Processing for the VLSI Era*, Vols. 1–4 (Lattice Press 2000) (Ex. 1008).

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–9, 13, 14, 16–28	103(a)	Kawagoe, Gupta ⁵
1, 2, 4–9, 13–23, 25–28	103(a)	Wieczorek, Wolf, Gupta
19	103(a)	Kawagoe, Silverbrook ⁶
19	103(a)	Wieczorek, Wolf, Silverbrook

Petitioner also relies upon the declaration testimony of Dr. Travis Blalock, Ph.D. Ex. 1003.

III. ANALYSIS

A. Legal Standard

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and “the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In order to determine whether an invention would have been obvious at the time the application was filed, we consider the level of ordinary skill

⁵ US 6,163,877, issued Dec. 19, 2000 (Ex. 1014).

⁶ US 6,614,560 B1, issued Sept. 2, 2003 (Ex. 1046).

in the pertinent art. *Graham*, 383 U.S. at 17. In assessing the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quotation omitted).

Petitioner contends that one of ordinary skill in the art would have had “a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience.” Pet. 6 (citing Ex. 1003 ¶ 48). Petitioner further contends that “[a]dditional education might compensate for less experience, and vice-versa.” *Id.*

Patent Owner does not address the level of ordinary skill in the art.

On this record, we adopt Petitioner’s definition of the person of ordinary skill in the art as it appears consistent with the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (holding that the prior art itself can reflect the appropriate level of ordinary skill in the art).

C. Claim Construction

In an *inter partes* review proceeding, a patent claim is construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (as amended Oct. 11, 2018). This rule adopts the claim construction standard used by Article III federal courts, which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. Under this standard, the words of a claim are generally given their “ordinary and customary

meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *See Phillips*, 415 F.3d at 1312–13.

Petitioner contends that no claims terms require express construction to resolve the issues presented in the Petition. Pet. 6–7.

Patent Owner does not assert that any claim terms require express construction. *See generally*, Prelim. Resp.

Upon review of the record, we determine that no claim terms require express construction for purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Claims 1–9, 13, 14, and 16–28 in View of Kawagoe

Petitioner contends the subject matter of claims 1–9, 13, 14, and 16–28 would have been obvious in view of Kawagoe. Pet. 7–40.

1. Kawagoe

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device by forming an epitaxial layer over the surface of a semiconductor substrate body. Ex. 1007, 1:13–20, 2:31–35. According to Kawagoe, “[t]he epitaxial wafer is advantageous in that it is excellent in suppressing the soft errors and resisting to the latchup,”⁷ and also the gate

⁷ Petitioner submits Exhibit 1009 (Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Int’l Conf on VLSI Design, 429–434, IEEE 2008), which explains that “soft errors” are “random and not related to permanent hardware faults” and “[t]heir causes may be internal (e.g.,

insulating film formed over the epitaxial layer may have “excellent breakdown characteristics” that “drastically reduce the defect density of the gate insulating film” of a semiconductor integrated device. *Id.* at 1:33–40.

Kawagoe describes seven embodiments, including Embodiment 1 (Ex. 1007, 6:41–12:40, Figs. 1–8) and Embodiment 4 (*id.* at 14:46–19:63, Figs. 16–25). Figure 1, reproduced below, depicts the device of Embodiment 1.

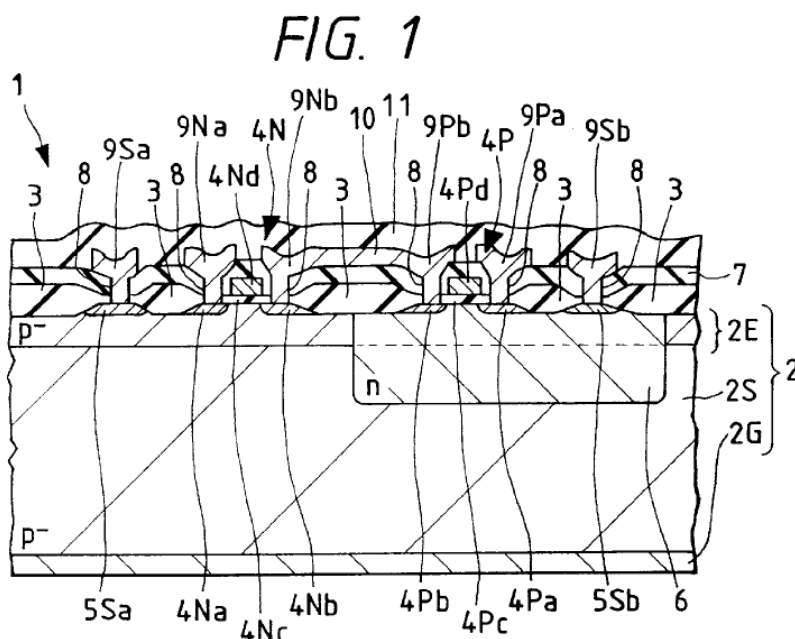


Figure 1 depicts “an essential portion of a semiconductor integrated circuit device” that includes semiconductor substrate body 2S, epitaxial layer 2E, and gettering layer 2G. *Id.* at 6:51–56, Fig. 1. Substrate body 2S and epitaxial layer 2E are doped with a p-type impurity in equal concentrations. *Id.* at 6:60–7:3, 10:51–55, 11:12–16. Embodiment 1 includes n-channel

interconnect coupling) or external (e.g., cosmic radiation),” including “alpha particles [that] are emitted when the nucleus of an unstable isotope decays to a lower energy state.” Ex. 1009, Abstract, 430. Dr. Blalock characterizes “latchup” as “a ‘short-circuit’ failure condition in poorly designed circuits.” Ex. 1003 ¶ 79.

MOS.FET (“nMOS”) 4N and p-channel MOS.FET (“pMOS”) 4P, the latter being formed in n-well 6, which is doped with n-type impurity and extends deeper than epitaxial layer 2E. *Id.* at 8:46–52, 9:32–40, 11:18–24, 11:43–50, Figs. 1, 5, 7.

Figure 23, reproduced below, depicts a semiconductor device of Embodiment 4 in the process of manufacture. *Id.* at 6:1–4, 17:11–13, 18:3–8.

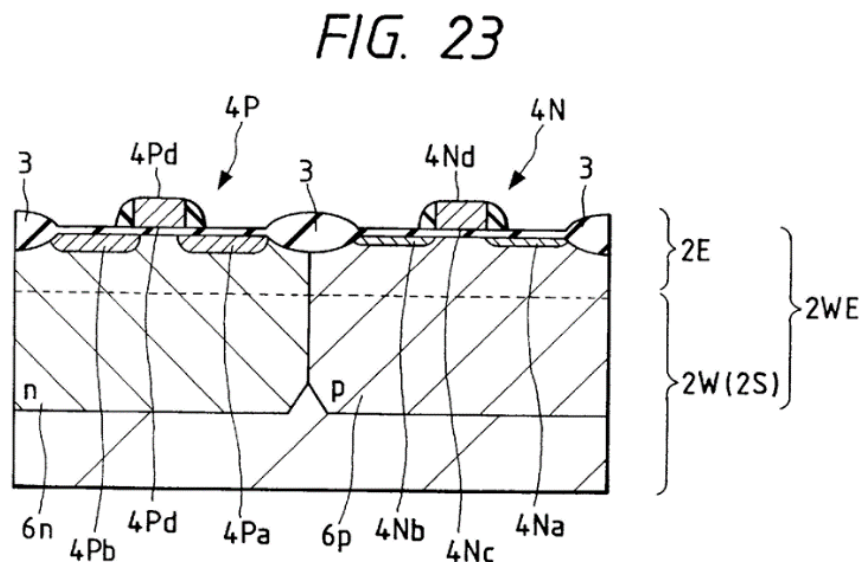


Figure 23 shows the semiconductor integrated circuit device of Embodiment 4, including p-well 6p formed with nMOS 4N and n-well 6n formed with pMOS 4P. *Id.* at 6:1–4, 15:26–32, 18:3–35. In Embodiment 4, p-well 6p and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction from the principal surface of epitaxial layer 2E. *Id.* at 15:62–16:2.

Petitioner relies on Kawagoe Figure 17, which is reproduced below and illustrates properties of the semiconductor device of Embodiment 4.

FIG. 17

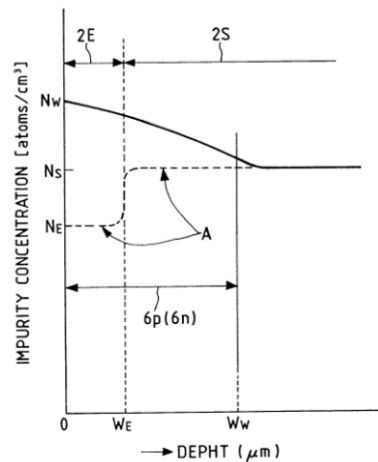


Figure 17 is a plot of impurity concentration as a function of depth in a semiconductor integrated circuit device and shows that “the impurity concentration of the p-well 6p and n-well 6n is given such a gradient that it is gradually lowered in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered.” Ex. 1007, 16:2–16:7. “Specifically, the electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced.” *Id.* at 16:7–11.

2. Analysis—Independent Claims 1 and 21

Petitioner argues that Kawagoe discloses the limitations of independent claims 1 and 21. Pet. 7–40. Patent Owner expressly contests only whether Kawagoe teaches or suggests a graded dopant concentration that will “aid carrier movement,” as recited in independent claims 1 and 21. Prelim. Resp. 3–18.

The preamble and first clause of independent claims 1 and 21 in combination require “An electronic system, [the system] comprising: at least

one semiconductor device, the at least one semiconductor device including:”⁸ Ex. 1001, 4:49–51, 6:4–6. To the extent the preamble is limiting, Petitioner contends that Kawagoe discloses a “semiconductor integrated circuit device,” such as a microcomputer and memories, that each constitute an electronic system. Pet. 7–8 (citing Ex. 1007, 1:13–23, 14:46–67, 24:28–31, 19:15–16, 20:1–33, 22:10–23:14, Figs. 16, 17, 23, 26(A), 28; Ex. 1003 ¶¶ 66–67). We find that, to the extent the preamble is limiting, Petitioner’s contention is sufficiently supported for purposes of institution.

Claims 1 and 21 recite “a substrate of a first doping type at a first doping level having a surface.” Ex. 1001, 4:52–53, 6:7–8. Petitioner contends that Kawagoe discloses a “semiconductor substrate body 2S” and epitaxial layer 2E, both having a first doping type (p-type), with the substrate as a whole having “a surface.” Pet. 9 (citing Ex. 1007, 14:61–15:12, 6:50–7:3, Fig. 23 (annotated by Petitioner to show the substrate in orange with a blue arrow identifying the surface)). Petitioner contends that Kawagoe discloses forming Figure 23’s twin-well CMOS device (Embodiment 4) on either Embodiment 1’s uniformly-doped epitaxial substrate or Embodiment 4’s optional latchup-resistant substrate. *Id.* at 11 (citing Ex. 1003 ¶ 74). According to Petitioner, one of ordinary skill in the art would have sought to use the uniformly-doped (“a first doping level”) epitaxial substrate of Embodiment 1 of Kawagoe, as opposed to Embodiment 4’s latchup-resistant substrate, to form the twin-well CMOS device of Figure 23 because this would optimize costs over latch-up resistance, and because a uniformly-doped epitaxial substrate “drastically

⁸ Petitioner uses bracketed language to show the difference between an identified pair of claims. Pet. 7, n.3. We use this convention as well.

reduce[s] the defect densities of the gate insulating films” of CMOS transistors. *Id.* at 11–12 (citing Ex. 1007, 12:8–40; Ex. 1003 ¶¶ 75, 79). We find that Petitioner’s contention for this limitation is sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “a first active region disposed adjacent the surface [of the substrate] with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed [in the surface thereof].” Ex. 1001, 4:54–57, 6:9:13. Petitioner contends that Kawagoe discloses “semiconductor regions 4Na and 4Nb” that are used “for forming the **source-drain regions** of the nMOS [n-channel transistor] 4N,” and which, in conjunction with the channel region between these regions, form part of the claimed first active region. Pet. 13–14 (citing Ex. 1007, 3:30–37, 8:46–67, 14:46–55, 15:26–40; Ex. 1003 ¶ 81; Ex. 1008B, 299–300) (modifications and emphasis by Petitioner). Petitioner further contends that regions 4Na and 4Nb have a second doping type (n-type) opposite in conductivity to the first doping type (p-type) of the substrate. *Id.* at 14. Petitioner also contends that nMOS transistor 4N is formed in the claimed first active region and that Kawagoe teaches forming multiple nMOS transistors in this region to minimize chip area, “as good layout practice dictates.” *Id.* at 14–15 (citing Ex. 1003 ¶ 82; Ex. 1014, 1:52–54, 2:17–21). We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed [in the surface thereof]” and “transistors formed in at least one of the first active region or second active region.” Ex. 1001, 4:58–62, 6:14–19. Petitioner contends that semiconductor regions

(source-drain regions) 4Pa and 4Pb are part of the claimed second active region, which also includes the channel region that is between them and below gate 4Pd. Pet. 16. According to Petitioner, as shown in Figure 23, pMOS transistor 4P is formed in the surface of this second active region, which is separate from and disposed adjacent to the first active region. *Id.* at 16–17. Petitioner contends that one of ordinary skill in the art would have also understood that multiple pMOS transistors could be formed in this region. *Id.* at 17. We find Petitioner’s contentions for these limitations are sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the [first and second active regions/surface] [towards/to] an area of the substrate where there are no active regions.” Ex. 1001, 4:63–67, 6:21–25. Petitioner contends that Figure 17 of Kawagoe illustrates the doping concentration from a top surface of the substrate, and shows that the dopant concentration is “gradually lowered in the depthwise direction *from the principal surface* (having an impurity concentration N_W) of the epitaxial layer 2E.” Pet. 19 (citing Ex. 1007, 15:62–16:40, Fig. 17) (emphasis by Petitioner). According to Petitioner, the dopant concentration is thus graded in the channel region of transistor 4N, which is a portion of the first active region formed at “the principal surface” of epitaxial layer 2E. *Id.* (citing Ex. 1003 ¶ 91); *see also id.* at 20 (noting the same dopant configuration for pMOS transistor 4P, i.e., the second active region) (citing Ex. 1007, 15:62–16:2).

Petitioner contends that Kawagoe explains that the downward-sloping graded dopant concentration aids the movement of carriers from the first and second active regions towards the bottom of the substrate where there are no

active regions. Pet. 21 (citing Ex. 1007, 16:2–11). Petitioner further contends that this conclusion is consistent with Patent Owner’s arguments in its district court claim construction briefing, in which Patent Owner asserted that the claims make clear that “[w]hen the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction” *Id.* at 22 (citing Ex. 1020, 2, 29). Petitioner also contends that its conclusions are consistent with Patent Owner’s arguments during prosecution of parent U.S. Patent No. 8,421,195 (“the ’195 patent”), in which the applicants argued that a downward-sloping graded dopant concentration was known to create an “inherent ‘built-in’ unidirectional electric field” that sweeps carriers down into the substrate (where there are no active regions). *Id.* at 22–23 (citing Ex. 1016, 289–290; Ex. 1003 ¶ 98).

Patent Owner asserts that the Petition fails to establish that Kawagoe teaches or suggests the “aid carrier movement” limitation of independent claims 1 and 21. Prelim. Resp. 3. Patent Owner reasons that a gradient may provide a force directing carriers within an active region towards a substrate, but there may be an additional force within an active region that counteracts this force, such that the graded dopant concentration will not “aid” the movement of carriers. *Id.* at 8–9. Patent Owner contends Petitioner and Dr. Blalock performed no analysis as to whether such additional forces exist in Kawagoe. *Id.* at 10. And, according to Patent Owner, it never argued before the district court or during prosecution of the ’195 patent that a “graded” dopant concentration will *necessarily* “aid” in the movement of carriers from the surface to the substrate.⁹ *Id.* at 3–5.

⁹ We need not resolve whether Patent Owner’s statements during prosecution are binding admissions, or constitute evidence that the graded

The active regions of Kawagoe have a graded dopant concentration, with the gradient gradually lowered in a direction from the surface of epitaxial layer 2E towards the substrate. Ex. 1007, 15:62–16:7. Both parties agree that a graded dopant concentration that is gradually lowered in the depthwise direction from the surface towards the substrate, absent additional forces, will aid carrier movement from the active regions towards the substrate (an area with no active regions).¹⁰ Ex. 1003 ¶¶ 94, 97; Ex. 1020, 2; PO Sur-reply 1–2 (Patent Owner agreeing that a downward-sloping graded dopant concentration will create a force that tends to move carriers). Patent Owner contends, however, that Petitioner has failed to analyze whether there are additional forces that would negate, or perhaps even reverse, the force provided by the graded dopant concentration in Kawagoe. PO Resp. 7–8, 11–12 (asserting that Dr. Blalock admitted that he did not

dopant concentration of Kawagoe would aid carrier movement towards the substrate, because the evidence of record is sufficient to support institution, regardless of whether Patent Owner’s prosecution statements are taken as binding admissions. The parties may, however, address during trial the scope and implication of Patent Owner’s assertions during prosecution, as well as before the district court.

¹⁰ Patent Owner notes that during prosecution of the ’195 patent, the Examiner, in applying a rejection under 35 U.S.C. § 112 ¶ 1, stated that in “a complex electronic device, movement of minority carriers is affected by multiple forces and fields” and, “without knowing other parameters of the device,” one cannot say whether the field would achieve the effect of “drawing all minority carriers from said substrate to said surface.” Prelim. Resp. 6 (citing Ex. 1016, 270). Patent Owner clearly disagreed with this conclusion, however, and the present claims do not require that all of the minority carriers are moved to the substrate, only that carrier movement is “aid[ed]” by the graded dopant concentration. Ex. 1016, 289–290. Thus, the Examiner’s prior statements appear to provide little guidance in this case.

calculate the net force on carriers); PO Sur-reply 1–2. But Dr. Blalock, in testimony provided from a different proceeding, testified that there are no opposing forces disclosed in Kawagoe, created for example by “[e]xternally applied voltages” or “some environmental effect.” Ex. 2058, 132:6–136:21, 139:13–17; Prelim. Reply 4. Nor does Patent Owner identify any structure, dopant, or field in Kawagoe that it contends would create an opposing force to counter the force created by the electrical field generated by the downward sloping gradient profile. Indeed, the fact that carriers are prevented from entering the active regions in Kawagoe, such as p-well 6p, appears to be strong evidence that the downward facing electric field is not negated or reversed by other fields or forces. As such, we are left with, at most, a material issue of fact that is best resolved on a complete trial record.

Patent Owner also asserts that the downward sloping gradient in Kawagoe actually prevents the movement of carriers from the substrate to the active regions, which is opposite to the direction recited in the claims. Prelim. Resp. 12–14. Both parties agree, however, that there are carriers in the active regions. Prelim. Sur-reply 6 (“Of course Kawagoe’s transistor, like any transistor, will have carriers in the active region.”); Ex. 1003 ¶ 95 (citing Ex. 1009, 431). As such, there is evidence that the graded dopant concentration of Kawagoe will aid carrier movement from the active regions towards the substrate where there are no active regions.

Patent Owner contends Kawagoe is concerned with single event upsets caused by α -particle strikes in the substrate, and there is no evidence that any single event upset would produce enough charge carriers to be noticeable or affect the operation of semiconductor devices. Prelim. Sur-reply 7 (citing IPR2023-01242, Paper 47 at 27). On this record, the question of whether an α -particle strike would generate sufficient carriers in the

active regions to affect the operation of the semiconductor device is a disputed issue of fact that is best resolved on a complete trial record.

Ex. 1003 ¶ 95 (Dr. Blalock testifying that when a strike occurs in the active region, numerous carriers (electrons) will be generated and directed towards the substrate by the graded dopant concentration of Kawagoe). We note, however, that the system claims of the '014 patent do not require that the number of carriers produced would disrupt the performance of the system. Ex. 1001, 4:49–5:7. Thus, whether an α -particle strike is *likely* (or how often they would statistically occur) in the active regions, or whether such a strike would produce a *disruptive number* of carriers, appears to be irrelevant.

Patent Owner further contends that there would have been no motivation to modify Kawagoe to move carriers in the active region. Prelim. Sur-reply 7–8. We agree with Petitioner, however, that the Petition does not propose any modification to Kawagoe's graded dopant concentration. Prelim. Reply 8. And, Petitioner provides sufficient evidence for purposes of institution to suggest that Kawagoe's graded dopant concentration would aid carrier movement (from any source) from the active regions towards the substrate (where there are no active regions). In view of the foregoing, we find that Petitioner's contentions for this limitation are sufficiently supported for purposes of institution.

Claims 1 and 21 also require “at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface [towards/to] the area of the substrate where there are no active regions.” Ex. 1001, 5:1–5, 6:26–30. Petitioner contends that Kawagoe discloses “p-well 6p” that is adjacent to a first active region and has a dopant concentration that gradually

decreases with depth. Pet. 23 (citing Ex. 1007, 8:66–67, 14:46–55, 15:26–40, 15:62–16:40; Ex. 1003 ¶ 99). Petitioner further contends that Kawagoe explains that the downward-sloping graded dopant concentration aids carrier movement from the surface of the epitaxial layer towards/to the area of the substrate where there are no active regions. *Id.* at 24–25 (citing Ex. 1007, 16:2–11). Patent Owner again disputes whether Petitioner provides sufficient evidence to show that the graded dopant concentration of Kawagoe will necessarily aid carrier movement from the surface to an area of the substrate where there are no active regions. Prelim. Resp. 9–18. Upon review of the evidence cited by Petitioner, and for the reasons discussed above, we find that Petitioner’s contention for this limitation is sufficiently supported for purposes of institution.

Claim 1 also requires “wherein at least some of the transistors form digital logic of the semiconductor device.” Ex. 1001, 5:5–7. Petitioner contends that Kawagoe teaches that the transistors in its active regions may form a CMOS circuit, be applied to a logic circuit such as a microcomputer, or be applied to a peripheral circuit region of DRAM. Pet. 28 (citing Ex. 1007, 8:46–52, 14:46–55, 15:26–40, 20:1–33, 22:10–29, 22:51–23:2, 24:28–31; Ex. 1008A, 810–811; Ex. 1003 ¶ 108). We find that Petitioner’s contention for this limitation is sufficiently supported for purposes of institution.

Claim 21 also requires “wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.” Ex. 1001, 6:30–33. Petitioner contends that the graded dopant concentration of Kawagoe is a combination of linear/quasilinear segments which result in a linear or nearly linear (quasilinear) dopant concentration. Pet. 29 (citing Ex. 1007, Fig. 17;

Ex. 1003 ¶ 109). We find that Petitioner’s contention for this limitation is sufficiently supported for purposes of institution.

In view of the foregoing, and on this preliminary record, Petitioner demonstrates sufficiently for purposes of institution that Kawagoe discloses, or teaches or suggests in combination with the knowledge of one of ordinary skill in the art, every limitation of claims 1 and 21. Accordingly, Petitioner demonstrates a reasonable likelihood that claims 1 and 21 would have been obvious over the disclosures of Kawagoe.

3. Analysis—Remaining Claims

Petitioner identifies where it contends the subject matter of claims 2–9, 13, 14, 16–20, and 22–28 is taught or suggested in Kawagoe. Pet. 29–40. Patent Owner does not, on this record, dispute Petitioner’s identifications, apart from its arguments discussed above with respect to independent claims 1 and 21.

Upon review of Petitioner’s arguments and supporting evidence, we determine that Petitioner demonstrates a reasonable likelihood that claims 2–9, 13, 14, 16–20, and 22–28 would have been obvious over Kawagoe.

E. Claims 1, 2, 4–9, 13–23, and 25–28 in view of Wieczorek and Wolf

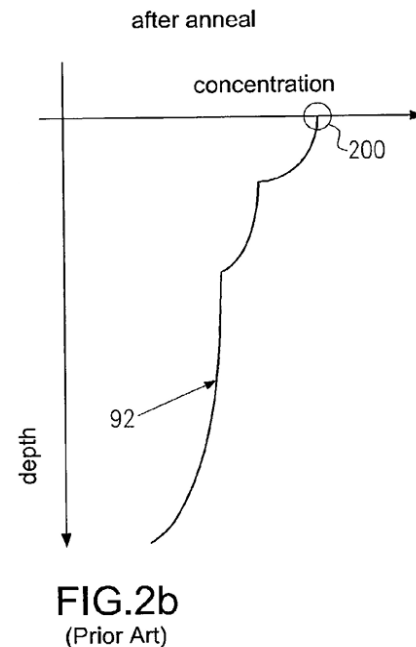
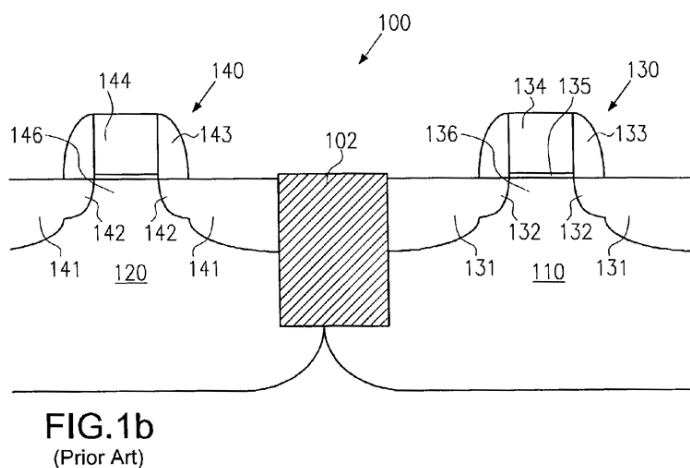
Petitioner contends that the subject matter of claims 1, 2, 4–9, 13–23, and 25–28 would have been obvious in view of the combined disclosures of Wieczorek and Wolf. Pet. 40–72. Patent Owner contests whether Wieczorek and Wolf teach or suggest the “aid carrier movement” limitation of independent claims 1 and 21. Prelim. Resp. 17–18.

1. Wieczorek

Wieczorek relates “to a semiconductor device, such as a field-effect transistor, having an improved retrograde dopant profile in a channel region

of the transistor element.” Ex. 1006 ¶ 2. Wieczorek explains that a retrograde channel dopant profile is one where “the concentration of dopants increases from the gate insulation layer to the areas located deeper down the channel region.” Ex. 1006 ¶ 6. According to Wieczorek, although a retrograde channel dopant profile is desirable, it is “very difficult to obtain.” *Id.* Wieczorek notes, for example, that “the dopant concentration immediately after the implantation process exhibits a desired retrograde dopant profile” (*id.* ¶ 9), but during heat treatment, “the initially retrograde profile in the vicinity of the surface of the semiconductor device . . . may have become substantially uniformly distributed” due to diffusion of the dopant atoms (*id.* ¶ 11).

Petitioner relies on Figures 1b and 2b (reproduced below), which Wieczorek uses to illustrate the prior art.



Wieczorek Figure 1b shows a conventional semiconductor device at an advanced manufacturing stage. Ex. 1006 ¶¶ 12, 20. The device includes P-channel transistor 140 with source and drain regions 141 in N-well

structure 120 and N-channel transistor 130 with source and drain regions 131 in P-well structure 110. *Id.* ¶ 12. Shallow trench isolation 102 separates N-well structure 120 from P-well structure 110. *Id.* ¶ 7. Wieczorek Figure 2b is a graph of dopant concentration versus depth in N-well structure 120 and P-well structure 110 and shows “a typical dopant profile with respect to the depth of the respective well structure” after ion implantation and heat treatment. *Id.* ¶¶ 9–11, 13, 21.

2. Wolf

Wolf is a four-volume textbook titled “Silicon Processing for the VLSI Era.” Ex. 1008. A portion of the textbook focuses on CMOS technology. Ex. 1008A, 807–40.

3. Analysis – Claims 1 and 21

a. Motivation to Combine

Petitioner relies on Wieczorek’s disclosure of a conventional prior art CMOS device. Pet. 40. Petitioner contends Wolf is “a well-known textbook,” and relies on Wolf for teaching “known fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS devices.” *Id.* at 41 (citing Ex. 1008A, Chapter 16; Ex. 1003 ¶ 133). According to Petitioner, a person of ordinary skill in the art would have understood and expected that the teachings of Wolf would apply to Wieczorek’s conventional CMOS device, and would have looked to Wolf for additional details related to such conventional CMOS devices. *Id.*

b. Claims 1 and 21

Claims 1 and 21 recite “An electronic system, [the system] comprising: at least one semiconductor device, the at least one semiconductor device including:” Ex. 1001, 4:51, 6:4–6. To the extent the

preamble is limiting, Petitioner contends that Wieczorek discloses a “semiconductor device 100” that constitutes an electronic system. Pet. 41–42 (citing Ex. 1006 ¶ 12, Fig. 1b; Ex. 1003 ¶¶ 134–135). On this record, Petitioner has shown sufficiently that Wieczorek teaches the recited subject matter of claims 1 and 21.

Claims 1 and 21 also recite “a substrate of a first doping type at a first doping level having a surface.” Ex. 1001, 4:52–53, 6:7–8. Petitioner contends that Wieczorek in combination with Wolf discloses this limitation. Pet. 42–46. In support, Petitioner provides an annotated version of Figure 1b of Wieczorek, which is reproduced below.

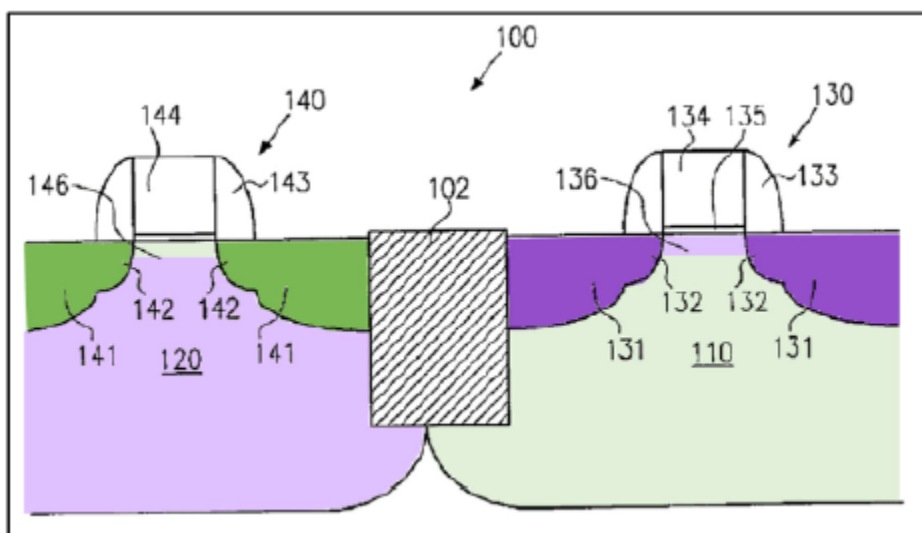


Figure 1b is annotated to show N-channel transistor 130 (nMOS) with source/drain regions 131–132 (purple) and channel region 136 (light purple) formed in P-well 110 (light green). *Id.* at 42–43 (citing Ex. 1006 ¶¶ 7, 12, 20–21; Ex. 1008C, 525, Fig. 8-1(e); Ex. 1003 ¶ 136). Figure 1b is also annotated to show P-channel transistor 140 (pMOS) with source/drain regions 141–142 (green) and channel region 146 (light green) formed in N-well 120 (light purple). *Id.* at 43.

Petitioner contends that Wieczorek explains that the P-well and N-well structures may be formed on any “appropriate substrate,” but does not explicitly specify what constitutes an “appropriate substrate.” Pet. 43 (citing Ex. 1006 ¶ 4; Ex. 1003 ¶ 137). Petitioner asserts, however, that one of ordinary skill in the art consulting Wolf would have understood that a “**uniform**, lightly doped *p*- or *n*- type substrate” is commonly used in twin-well CMOS devices and one of ordinary skill in the art would have found it obvious to use such a substrate in Wieczorek because “[d]oing so would amount to combining known prior art elements . . . according to known methods . . . to obtain predictable results.” *Id.* at 43–44 (citing Ex. 1008C, 523, 530; Ex. 1008B, 387–389; Ex. 1003 ¶¶ 138–139); *see id.* at 44 (asserting that the proposed combination would also be obvious to try because it “involves nothing more than choosing one of a finite number of known appropriate substrates that are described by Wolf as suitable for use in forming a twin-well CMOS device like Wieczorek’s”). Petitioner further contends that Wieczorek-Wolf’s substrate is a p-type non-epitaxial substrate (lower cost than an epitaxial substrate) which has a surface. *Id.* (citing Ex. 1008B, 382, Figs. 6–8(c); Ex. 1008C, 525, Fig. 8-1(e); Ex. 1003 ¶ 140). We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “a first active region disposed adjacent the surface [of the substrate] with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed [in the surface thereof].” Ex. 1001, 4:54–57, 6:9:13. Petitioner contends that Figure 1b of Wieczorek shows nMOS transistor 130 that includes “heavily N-doped **source and drain regions** 131, including lightly doped extensions 132” and “**channel region** 136,” which form a part of the claimed first

active region. Pet. 46 (citing Ex. 1006 ¶¶ 4, 12–13; Ex. 1003 ¶ 142; Ex. 1008B, 299). Petitioner further contends that nMOS transistor 130 is formed in the surface of the first active region, which is adjacent the surface of the substrate and has a second doping type (N-type) that is opposite in conductivity to the first doping type (P-type). *Id.* at 47 (citing Ex. 1006 ¶ 12; Ex. 1003 ¶ 143). Petitioner further contends Wieczorek teaches forming multiple transistors in its active regions. *Id.* (citing Ex. 1006 ¶ 4; Ex. 1003 ¶ 144; Ex. 1014, 1:52–54, 2:17–21). We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed [in the surface thereof].” Ex. 1001, 4:58–62, 6:14–19. Petitioner contends that P-channel transistor 140 of Wieczorek includes heavily P-doped source and drain regions 141, lightly doped extensions 142, and channel region 146, which are part of the claimed second active region. Pet. 49 (citing Ex. 1006 ¶¶ 4, 7, 12–13; Ex. 1003 ¶ 147). Petitioner further contends that this second active region is disposed adjacent the first active region and that one or more transistors, such as P-channel transistor 140, may be formed in the surface of this second active region. *Id.* at 49–50. We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claims 1 and 21 also recite “transistors formed in at least one of the first active region or second active region.” Ex. 1001, 4:61–62, 6:19–20. As discussed above, Petitioner contends that Wieczorek contemplates forming one or more transistors in each of the first and second active regions.

Pet. 47, 50. We find that Petitioner's contention for this limitation is sufficiently supported for purposes of institution.

Claims 1 and 21 also recite "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the [first and second active regions/surface] [towards/to] an area of the substrate where there are no active regions." Ex. 1001, 4:63–67, 6:21–25. Petitioner contends that the doping concentration of transistor 130 (including the channel region) in Wieczorek is shown in Figure 2b (reproduced above), and shows a dopant concentration that is highest at the surface of the substrate and decreases with depth. Pet. 51–53 (citing Ex. 1006 ¶¶ 4, 12–13, Figs. 2a-2b; Ex. 1008B, 298–301, Fig. 5-2; Ex. 1003 ¶¶ 152–153). Petitioner further contends that Wieczorek's downward-sloping graded dopant concentration aids carrier movement from the first and second active regions and surface towards/to an area of the substrate in which there are no active regions. *Id.* at 54 (citing Ex. 1003 ¶¶ 155, 156, 158; Ex. 1010, 2:27–32, 5:14–22).

Patent Owner contends the Petition fails to demonstrate that this limitation is disclosed in Wieczorek. Prelim. Resp. 17–18. Patent Owner reasons that Dr. Blalock did not calculate the slope of the graded concentration curve in Wieczorek, and could not have possibly done so because the reference "does not have any value from which one could calculate a slope." *Id.* And, because knowledge of the slope is essential to determine the magnitude of the force the dopant gradient places on the carriers, Patent Owner contends this limitation is not disclosed in Wieczorek. *Id.* at 18.

Petitioner demonstrates that Wieczorek discloses a downward-sloping gradient within both active regions. Pet. 53; Ex. 1006 ¶¶ 4, 12–13, Fig. 2b.

Petitioner further presents evidence that a downward-sloping gradient will, absent other forces, create an electric field that imparts a force on charge carriers, directing them deeper into the substrate where there are no active regions. Pet. 54; Ex. 1003 ¶¶ 154–158; Ex. 1010, 2:27–32, 5:14–22 (explaining that a downward-sloping graded dopant concentration will create an electric field that forces charge carriers deep into the substrate). As noted by Patent Owner, the strength of the electric field created by the downward-sloping gradient is not disclosed in Wieczorek. But the claims do not require any degree of net force on the carriers, only that their movement in the downward direction is “aid[ed].” On this record, any amount of net force in the direction towards the substrate will “aid carrier movement,” as recited in independent claims 1 and 21. And, absent any reason to believe that the net force on the carriers is not in the downward direction in Wieczorek, due for example to an undisclosed external electric field or environmental factors, Petitioner’s evidence is sufficient to support institution.

Claims 1 and 21 also require “at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the surface [towards/to] the area of the substrate where there are no active regions.” Ex. 1001, 5:1–5, 6:26–30. Petitioner contends that P-well structure 110 shown in annotated Figure 1b (light green) is adjacent to the first active region (purple/light purple), and the dopant concentration in P-well 110 gradually decreases with depth (Figure 2b). Pet. 56–57 (citing Ex. 1006 ¶¶ 12–13; Ex. 1003 ¶ 160). According to Petitioner, the downward-sloping gradient of Wieczorek was known to create a “built-in” electric field that moves carriers deep into the substrate, i.e., it aids carrier movement from the surface towards/to the area

of the substrate where there are no active regions. *Id.* at 57. For the reasons discussed above, although disputed by Patent Owner, we find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claim 1 also requires “wherein at least some of the transistors form digital logic of the semiconductor device.” Ex. 1001, 5:5–7. Petitioner contends that Wieczorek’s “complementary MOS transistor pair” is a “frequently used semiconductor device in modern integrated circuits” and was understood to form digital logical gates. Pet. 58 (Ex. 1006 ¶¶ 7, 26; Ex. 1008A, 810–811; Ex. 1003 ¶ 164). We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

Claim 21 also requires “wherein the graded dopant concentration is linear, quasilinear, error function, complementary error function, or any combination thereof.” Ex. 1001, 6:30–33. Petitioner contends that, as shown in Figure 2b, the graded dopant concentration is a combination of linear or nearly linear (quasilinear) segments. Pet. 58–59 (citing Ex. 1003 ¶ 165). We find that Petitioner’s contentions for this limitation are sufficiently supported for purposes of institution.

In view of the foregoing, Petitioner sufficiently demonstrates for purposes of institution that Wieczorek and Wolf teach or suggest every limitation of claims 1 and 21. Petitioner also provides an explanation, supported by factual underpinning, as to why one of ordinary skill in the art would have combined Wieczorek and Wolf. Accordingly, Petitioner demonstrates a reasonable likelihood that claims 1 and 21 would have been obvious over Wieczorek and Wolf.

4. *Analysis—Remaining Claims*

Generally relying on the same figures of Wieczorek and citations to Wolf, Petitioner identifies where it contends every limitation of claims 2, 4–9, 13–20, 22, 23, and 25–28 is disclosed in these references. Pet. 59–72. Patent Owner does not dispute, on this record, any of Petitioner’s arguments and evidence with respect to these claims, apart from its arguments with respect to independent claims 1 and 21. Upon review of Petitioner’s arguments and evidence, we find that Petitioner’s contentions with respect to the remaining claims are sufficiently supported for purposes of institution.

F. *Grounds Including Gupta*

1. *Gupta*

Gupta “relates to the field of complimentary metal oxide semiconductor (CMOS) circuits, and more particularly to automatically producing layouts for CMOS circuits.” Ex. 1014, 1:7–10. According to Gupta, “[a]s semiconductor chips become ever larger, incorporating ever more devices, it becomes increasingly important to minimize semiconductor area used by a given number of devices.” *Id.* at 1:28–31. Doing so “potentially [saves] millions of dollars.” *Id.* at 1:31–34. To accomplish this goal, Gupta discloses abutting multiple transistors to “form transistor chains.” *Id.* at 2:17–21, Fig. 4.

2. *Analysis*

As discussed above, several challenged claims require “transistors” or “devices.” Pet. 72 (citing claims 1, 4, 5, 13, 21, 25, 26). Petitioner contends that one transistor is sufficient to show “transistors” or “devices” may be formed in the relevant layers, but to the extent that the claims are interpreted to require multiple transistors or devices be formed, Gupta discloses such a

configuration. *Id.* at 72–77. Patent Owner, on this record, does not contest this assertion.

For the reasons set forth above, Petitioner demonstrates a reasonable likelihood that the challenged claims would have been obvious over Kawagoe or Wieczorek and Wolf. Thus, we do not address Petitioner’s additional arguments relying on the additional disclosures of Gupta.

G. Challenges Based on Silverbrook

Claim 19 depends from claim 1 and further requires “wherein the at least one semiconductor device is an image sensor.” Ex. 1001, 5:62–63. Petitioner contends that the subject matter of claim 19 would have been obvious over the combined disclosures of Kawagoe and Silverbrook, or Wieczorek, Wolf, and Silverbrook. Pet. 77–80.

1. Silverbrook

Silverbrook “relates substantially to the concept of a disposable camera having instant printing capabilities.” Ex. 1046, 1:8–9. Part of Silverbrook’s camera is an “Image Capture and Processing Chip” that performs “CMOS image sensing.” *Id.* at 6:41–49. The CMOS image sensing is accomplished by “a CMOS active pixel sensor array” manufactured using a “CMOS/DRAM/APS process.” *Id.* at 6:50–55.

2. Analysis

Petitioner contends that Silverbrook expressly seeks incorporation of existing CMOS designs into its image sensor device, and asserts that using the CMOS device designs of Kawagoe or Wieczorek/Wolf in Silverbrook’s CMOS image sensor would “achieve high packing density” at submicron dimensions, and would have also provided improved immunity to soft errors through appropriate well doping. Pet. 74–75.

Patent Owner does not, on this record, contest Petitioner's arguments with respect to claim 19.

Upon review of the arguments and prior art of record, we determine that Petitioner demonstrates sufficiently for purposes of institution where every limitation of claim 19 is disclosed or suggested in either Kawagoe and Silverbrook, or Wieczorek, Wolf, and Silverbrook. Accordingly, Petitioner demonstrates a reasonable likelihood that these claims would have been obvious over Kawagoe and Silverbrook, or Wieczorek, Wolf, and Silverbrook.

H. Timeliness of the Petition Under 35 U.S.C. § 315(b)

Pursuant to 35 U.S.C. § 315(b), “[a]n inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.” Patent Owner argues that the Petition should be dismissed because it is untimely. Prelim. Resp. 18. In particular, Patent Owner argues that Petitioner is in privity with [REDACTED] (collectively “Licensees”), who Patent Owner asserts are time-barred under 35 U.S.C. § 315(b). *Id.* at 19–20, 30.

Patent Owner advances several theories supporting its privity arguments, including that Petitioner serves as an “agent” of Licensees by exercising their “have made” rights under the license, that Petitioner is a beneficiary of the Licensee's agreements related to accused products, that Petitioner and Licensees are “preceding and succeeding owners of” licensed (or infringing) products,” that Petitioner's licensed sales encumber otherwise

infringing articles, and “Petitioners apparently indemnify the time-barred parties” for custom-made products. Prelim. Resp. 30–38

1. *Legal Standard*

Patent Owner does not assert that Petitioner was a party to, or named as a real party-in-interest in, any prior lawsuit involving the ’014 patent. “A person who is not a party to a suit generally has not had a ‘full and fair opportunity to litigate’ the claims and issues settled in that suit.” *Taylor v. Sturgell*, 553 U.S. 880, 892 (2008). Thus, in general, Petitioner should not be precluded from addressing the unpatentability of a patent based on the filing of previous complaints alleging infringement by [REDACTED]. *See id.* (noting that, in general, one is not bound by a judgment “in which he is not designated as a party or to which he has not been made a party by service of process”); *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319 (Fed. Cir. 2018) (noting the “general rule against nonparty preclusion”). This rule is deeply-rooted in the “historic tradition that everyone should have his own day in court.” *Taylor*, 553 U.S. at 892–93 (quoting *Richards v. Jefferson County*, 517 U.S. 793, 798 (1996)).

An exception to this deeply-rooted rule exists for parties that are in privity with a defendant in an earlier litigation. *See WesternGeco*, 889 F.3d at 1319 (noting that “the standards for the privity inquiry must be grounded in due process”). The Supreme Court in *Taylor* identified considerations where nonparty preclusion would be justified, including:

- (1) an agreement to be bound; (2) pre-existing substantive legal relationships between the person to be bound and a party to the judgment (e.g., “preceding and succeeding owners of property”); (3) adequate representation by someone with the same interests who was a party (e.g., “class actions” and “suits brought by trustees, guardians, and other fiduciaries”);

(4) assumption of control over the litigation in which the judgment was rendered; (5) where the nonparty to an earlier litigation acts as a proxy for the named party to relitigate the same issues; and (6) a special statutory scheme expressly foreclosing successive litigation by nonlitigants.

Id. (citing *Taylor*, 553 U.S. at 894–95).

As this list of considerations indicates, “the mere existence of some relationship between a petitioner and another entity is not sufficient” to place that petitioner in privity with that entity. *Google LLC v. DDC Technology, LLC*, IPR2023-00707, Paper 27 at 37 (PTAB Oct. 25, 2023). Instead, “that relationship must be related to [an earlier] lawsuit and be sufficiently close that it can be fairly said the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit,” or the evidence must demonstrate “that petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation.” *Id.*; *WesternGeco*, 889 F.3d at 1319; *see also Ventex Co. v. Columbia Sportswear North America, Inc.*, IPR2017-00651, Paper 148, at 10, 12 (PTAB Jan. 24, 2019) (precedential) (finding privity where the two parties “had a specially structured, preexisting, and well established business relationship with one another, including indemnification and exclusivity arrangements”).

A petitioner’s “initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner.” *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1244 (Fed. Cir. 2018). In order to raise such a dispute, “a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privity].” *Id.* The amount of evidence a patent owner must produce does not rise to the level of that required to overcome a burden of production. *Id.*

at 1244 n.8. One potential formulation of the amount of evidence required is “evidence that ‘reasonably brings into question the accuracy of a petitioner’s’” assertion that it is not time-barred. *Id.* (quoting *Atlanta Gas Light v. Bennett Regulator Guards, Inc.*, IPR2013-00453, Paper 88 (PTAB Jan. 6, 2015) (addressing the amount of evidence required from a patent owner to question a petitioner’s identification of the real parties-in-interest)). Although the “burden remains with the petitioner to establish” the timeliness of its petition, it need not respond until the patent owner reasonably brings into question the accuracy of its assertion that it is not time-barred. *Id.* at 1242.

2. *The Effect of the Earlier Suits Against [REDACTED] on the Timeliness of the Present Petition*

Patent Owner alleges that [REDACTED] are time-barred under § 315(b). Prelim. Resp. 26. As to [REDACTED], the present record does not contain any evidence tending to show that this is the case.

Section 315(b) bars institution of *inter partes* review only when “the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.” On this record, there is no evidence that [REDACTED] was ever served with a complaint alleging infringement of the ’014 patent. Prelim. Resp. 19 (asserting that Patent Owner filed a complaint against [REDACTED] with respect to patents other than the ’014 patent). Thus, on the present record, there is insufficient evidence to suggest that [REDACTED] is a time-barred party.

There is also no evidence, on the present record, that [REDACTED] was served with a complaint any earlier than [REDACTED] which is less than one

year before the filing of the Petition on December 11, 2023. Ex. 2019, 1; Pet. 82. Accordingly, the service of an infringement complaint on [REDACTED] does not, on the present record, render [REDACTED] time-barred under § 315(b).

Patent Owner argues that, because [REDACTED] [REDACTED] were served with an infringement complaint early enough to create a time bar, and because [REDACTED] was a real party-in-interest of [REDACTED] in that infringement case, [REDACTED] is time-barred under § 315(b). Prelim. Resp. 26 (arguing that [REDACTED] is time-barred because it was a real-party-in-interest to the [REDACTED] litigation). We are presented with no authority, however, for extending the time bar of Section 315(b) to a party [REDACTED] that was a real party-in-interest to a potentially time barred party [REDACTED]. Thus, Patent Owner has produced no evidence that [REDACTED] is a time-barred entity under § 315(b).

3. [REDACTED] *as Alleged Privies*

In the subsections below, we address Patent Owner’s arguments that [REDACTED] are privies of Petitioner under § 315(b).

a. *Agency*

Patent Owner argues that Petitioner acts as the Licensees’ “agent” by making accused products on their behalf under the “have made” clause of the license. Prelim. Resp. 36–38. We disagree.

First, Patent Owner’s agency argument is not based on the applicable legal standard. For purposes of privity under § 315(b), the relevant question is whether Petitioner is acting as an agent for [REDACTED] in filing a petition for *inter partes* review. *See Taylor*, 553 U.S. at 895 (“preclusion is appropriate when a nonparty later brings suit as an agent for a party who is bound by a judgment.”). As the Federal Circuit explains, the

rationale behind § 315(b)'s time bar is "to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation." *WesternGeco*, 889 F.3d at 1319. Here, Patent Owner does not assert that Petitioner is acting as an agent for [REDACTED] in this proceeding. Any such assertion would be appropriate only based on evidence suggesting that any of those entities, and in particular [REDACTED] is controlling Petitioner's conduct in the proceeding. See *Taylor*, 553 U.S. at 906 (cautioning that "preclusion is appropriate only if the putative agent's conduct of the suit is subject to the control of the party who is bound by the prior adjudication"). No such evidence is in this record.

Patent Owner argues that to be in privity with the Licensees, what matters is whether the prior action concerned a matter within the agency. Prelim. Resp. 36 (citing *Herrion v. Children's Hosp. Nat. Med. Ctr.*, 786 F. Supp. 2d 359 (D.D.C.), *aff'd*, 448 F. App'x 71 (D.C. Cir. 2011)). This conclusion, however, would significantly expand the analysis set forth in *Taylor*, which noted that preclusion is only appropriate "if the putative agent's conduct is subject to the control of the party who is bound by the prior adjudication." *Taylor*, 553 U.S. at 906 (explaining that "courts should be cautious about finding preclusion" on the basis of agency). Moreover, the privity inquiry must take into account the rationale behind § 315(b)'s preclusion provision, which "is to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation." *WesternGeco*, 889 F.3d at 1319. Patent Owner's broad interpretation would be inconsistent with this purpose.

Even if Patent Owner's argument that a general agency relationship is sufficient to demonstrate privity for purposes of nonparty preclusion were on solid legal footing, it lacks factual support in the record. An "essential

element[] of agency” is “the principal’s ‘right to direct or control the agent’s actions.’” *In re Google LLC*, 949 F.3d 1338, 1345 (Fed. Cir. 2022) (quoting *Meyer v. Holley*, 537 U.S. 280, 286 (2003)). Patent Owner does not argue in the Preliminary Response that [REDACTED] has or had such a right with respect to Petitioner, or vice-versa, much less direct us to any evidence that would tend to prove the existence of such a right. Prelim. Resp. 36–37.

b. Preceding and Succeeding Owners of Property

Patent Owner argues that Petitioner and [REDACTED] are “preceding and succeeding owners” of “licensed and/or infringing products that Petitioner makes and supplies to Licensees.” Prelim. Resp. 30 (citing *Taylor*, 553 U.S. at 894). It is true that entities who are “preceding and succeeding owners of property” can be in privity with one another. *Taylor*, 553 U.S. at 894. This rule, however, is based on property law and “is extended or denied in an effort to protect conflicting property interests rather than an effort to implement concepts of participation or representation.” 18A C. Wright, A. Miller, & E. Cooper, *Federal Practice and Procedure* § 4448 (3d. ed. 2023); *see also id.* at § 4462 (“Successive Property Relationships”) (“There is no independent reason to treat the defeated litigant as the representative of his transferee. Preclusion is limited to the property involved in the judgment.”). As noted above, our relevant analysis is based on the relationships between the parties with respect to the prior proceeding or the Petition (e.g., participation or representation), not on property interests. *See WesternGeco*, 889 F.3d at 1319 (noting that the privity requirement is used “to prevent successive challenges to a patent by

those who previously have had the opportunity to make such challenges in prior litigation”).

Moreover, the rule related to preceding and succeeding owners of property does not extend to the point where all manufacturers of allegedly infringing goods are in privity with the customers who buy those goods. *See, e.g., WesternGeco*, 889 F.3d at 1319–22 (the parties “had a contractual and fairly standard customer-manufacturer relationship regarding the accused product,” which “does not necessarily suggest that the relationship is sufficiently close that both” parties should be considered to be in privity); *Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1340–41 (Fed. Cir. 2018) (same); *Samsung Electronics Co. Ltd. v. Netlist Inc.*, IPR2022-00615, Paper 64 at 22–26 (PTAB June 30, 2023) (same).

Patent Owner’s evidence that Petitioner’s products are components of Licensees’ products does not come close to suggesting that “it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent” in the prior law suit, or that petitioner is serving as a proxy to allow any Licensee to again challenge the patent. *WesternGeco*, 889 F.3d at 1319. Thus, Patent Owner does not present evidence that lends support to a finding that Petitioner’s and Licensees’ status as preceding and succeeding owners of allegedly infringing products renders them privies for purposes of § 315(b).

c. Beneficiaries of License Agreement

Patent Owner argues that Petitioner and [REDACTED] are privies because Petitioner is a “beneficiary” of Patent Owner’s license to [REDACTED] which Patent Owner asserts is “directly related to” the accused products. Prelim. Resp. 33–34 (citing *Ventex*, Paper 148). We disagree. Unlike the

agreements in *Ventex*, Paper 148 at 12, Patent Owner’s license to Licensees is not evidence of a privity relationship between Petitioner and Licensees because Petitioner is not a party to the license agreement. Nor is there any argument that Petitioner is a third-party beneficiary of the license.

d. *Patent Exhaustion*

Patent Owner argues that the doctrine of patent exhaustion gives rise to privity because “after Petitioner sells products under the license, any downstream user of the article sold would have an exhaustion defense against [Patent Owner].” Prelim. Resp. 34. According to Patent Owner, “Ppetitioner is effectively providing rights to third-parties under the license and, therefore, is in privity with Licensees.” *Id.* at 35. We disagree. It is true that downstream purchasers and users of [REDACTED] products that incorporate products made by Petitioner and fall under the Licenses may have a license (or exhaustion) defense against any claim of infringement by Patent Owner. The relevant question for this proceeding, however, is ultimately whether the relationship between Petitioner and the Licensees, and in particular [REDACTED] is sufficiently close to justify denying Petitioner its day in court. *See Taylor*, 553 U.S. at 892. Patent Owner does not sufficiently explain why a license defense supports such a privity relationship between Petitioner and [REDACTED].

e. *Indemnification*

Patent Owner argues that Petitioner’s indemnity obligations support a finding of privity between Petitioner and the Licensees. Prelim. Resp. 35–36. As evidence of this alleged indemnification obligation, Patent Owner argues that Petitioner indemnifies Licensees. *Id.* at 35. Patent Owner also

directs us to the indemnification provisions found in Petitioner’s “standard sales agreement[.]” *Id.* (citing Ex. 2010, 3).

An agreement by a petitioner to indemnify a third party in an earlier infringement suit can give rise to a privity relationship between the petitioner and that third party. *Intel Corp. v. U.S. Int’l Trade Comm’n*, 946 F.2d 821, 839 (Fed. Cir. 1991). With respect to the ’014 patent, the evidence of record suggests that only one Licensee—[REDACTED]—is potentially time-barred. Petitioner’s indemnification provisions are directed to specific products sold by it. Ex. 2010. To the extent that Petitioner’s indemnification provisions could demonstrate a privity relationship sufficient to deny Petitioner its day in court, it must be with respect to a product it sold to [REDACTED]. The present record, however, does not identify any device or component of Petitioner that formed the basis for the previous infringement complaint against [REDACTED]. *See* Ex. 2018, 10–11 (identifying products [REDACTED] was accused of infringing before the district court). As such, we are not persuaded that the indemnification provisions of Petitioner’s “standard sales agreement” are relevant to any relationship with [REDACTED].

f. Conclusion as to Timeliness of the Petition

As noted above, privity concerns “whether the petitioner and the prior litigant’s relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit,” or “whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation.” *WesternGeco*, 889 F.3d at 1319. A petitioner’s “initial identification of the real parties in interest [and privies] should be accepted

unless and until disputed by a patent owner.” *Worlds*, 903 F.3d at 1244. In order to raise such a dispute, “a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy].” *Id.* Here, Patent Owner argues that it has produced such evidence in several respects, but, on the present record, none of the evidence in question tends to show that any time-barred Licensee is a privy of Petitioner for purposes of § 315(b). As such, we find the evidence of record does not tend to suggest that Petitioner is time-barred under 35 U.S.C. § 315(b), and does not call into question Petitioner’s assertion that the Petition is timely-filed.

IV. CONCLUSION

For the foregoing reasons, we determine that there is a reasonable likelihood that Petitioner would prevail with respect to at least one of the claims challenged in the Petition. In addition, we are persuaded on the present record that the Petition is not time-barred under 35 U.S.C. § 315(b). Accordingly, we institute an *inter partes* review of all challenged claims based on the grounds asserted in the Petition.

V. ORDER

For the foregoing reasons, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), *inter partes* review is instituted with respect to the grounds of unpatentability set forth in the Petition;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, notice is given of institution of trial commencing on the entry date of this Decision;

FURTHER ORDERED that, in view of the pending motion to seal, this Decision is being filed “Board and Parties Only”; and

FURTHER ORDERED that after conferring with Petitioner, Patent Owner shall, within one week of this Decision, submit to the Board via email to Trials@uspto.gov, a version of this Decision to be filed on the public record, with any redactions proposed by either party.

IPR2024-00263
Patent 11,316,014 B2

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