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Paper 35
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PUBLIC VERSION

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,
Petitioner,

v.

GREENTHREAD LLC,
Patent Owner.

IPR2023-01244
Patent 11,121,222 B2

Before JON B. TORNQUIST, CHRISTOPHER M. KAISER, and ELIZABETH M. ROESEL, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

A. Background and Summary

Semiconductor Components Industries, LLC ("Petitioner") filed a petition for an *inter partes* review (Paper 2 ("Pet.")) challenging claim 44 of U.S. Patent No. 11,121,222 B2 (Ex. 1001 ("the '222 patent")). In addition, Petitioner filed a paper explaining and ranking the parallel petitions challenging the '222 patent: the present Petition and the petition filed in IPR2023-01242. Paper 3. Greenthread, LLC ("Patent Owner") filed a Preliminary Response. Paper 18 ("Prelim. Resp."). With our authorization, Petitioner filed a Preliminary Reply (Paper 22, "Prelim. Reply"), and Patent Owner filed a Preliminary Sur-Reply (Paper 28, "Prelim. Sur-Reply").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted "unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons set forth below, we determine the information presented in the Petition establishes a reasonable likelihood that Petitioner would prevail with respect to the challenged claim. Accordingly, we institute an *inter partes* review of the challenged claim on all grounds challenged in the Petition.

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B. Real Parties-in-Interest

Each party identifies itself as a real party-in-interest. Pet. 1; Paper 5, 2. In addition, Petitioner identifies ON Semiconductor Corporation as a real party-in-interest. Pet. 1.

C. Related Matters

The parties identify several proceedings involving the '222 patent as related matters, including *Greenthread, LLC v. ON Semiconductor Corp.*, No. 1:23-cv-00443 (D. Del.); *Greenthread, LLC v. Western Digital Corp.*, No. 1:23-cv-00326 (D. Del.); *Greenthread, LLC v. Cirrus Logic, Inc.*, 1:23-cv-00369 (W.D. Tex.); *Greenthread, LLC v. Texas Instruments Inc.*, No. 2:23-cv-00157 (E.D. Tex.); *Greenthread, LLC v. OSRAM GmbH*, No. 2:23-cv-00179 (E.D. Tex.); *Greenthread, LLC v. OmniVision Technologies, Inc.*, No. 2:23-cv-00212 (E.D. Tex.); *Greenthread, LLC v. Monolithic Power Systems, Inc.*, No. 1:23-cv-00579 (D. Del.); *Greenthread, LLC v. Intel Corp.*, No. 6:22-cv-105 (W.D. Tex.); *Greenthread, LLC v. Intel Corp.*, No. 6:22-cv-01293 (W.D. Tex.); *Greenthread, LLC v. Micron Technology, Inc.*, No. 1:23-cv-00333 (D. Del.); *Intel Corp. v. Greenthread, LLC*, IPR2023-00420 (PTAB); *Intel Corp. v. Greenthread, LLC*, IPR2023-00552 (PTAB); *Dell Technologies Inc. v. Greenthread, LLC*, IPR2023-00509 (PTAB); and *Sony Group Corp. v. Greenthread, LLC*, IPR2023-00324 (PTAB). Pet. 1–3; Paper 5, 2–5. In addition, Petitioner challenges claims 1–9, 13–28, and 32–42 of the '222 patent in IPR2023-01242, currently pending. Paper 3, 3. Further, Patent Owner identifies two additional matters involving the '222 patent: *Cirrus Logic, Inc. v. Greenthread, LLC*, IPR2024-00020 (PTAB); and *Cirrus Logic, Inc. v. Greenthread, LLC*, IPR2024-00021 (PTAB). Paper 16, 2.

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D. The '222 Patent

The '222 patent, titled "Semiconductor Devices with Graded Dopant Regions," issued on September 14, 2021. Ex. 1001, codes (45), (54). The '222 patent "relates to all semiconductor devices and systems." *Id.* at 1:23–24. According to the '222 patent, in bipolar junction transistors, "[e]fforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector" versus the standard "uniformly doped base." *Id.* at 1:34–48. This improvement has not been implemented in "most semiconductor devices, including various power MOSFETs [and] IGBT's," which "still use a uniformly doped 'drift epitaxial' region in the base." *Id.* at 1:48–53. The invention of the '222 patent implements graded dopant concentration in these devices, which causes "[t]wo important performance enhancements." *Id.* at 3:4–31. These include sweeping electrons "from source to drain rapidly" and simultaneously causing holes to "be recombined closer to the n^+ buffer layer," which "can improve t_{on} and t_{off} in the same device." *Id.* at 3:31–35.

E. Challenged Claim

Petitioner challenges claim 44, which is reproduced below.

> 44. A CMOS Semiconductor device comprising:
>
> a surface layer;
>
> a substrate;
>
> an active region including a source and a drain, disposed on one surface of the surface layer;
>
> a single drift layer disposed between the other surface of the surface layer and the substrate, the drift layer having a graded concentration of dopants extending between the surface layer and the substrate, the drift layer further having

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a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions; and

at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

Ex. 1001, 8:21–39.

F. Asserted Unpatentability Challenges

Petitioner asserts that claim 44 is unpatentable based on the following challenges:

Claim Challenged	35 U.S.C. §	Reference(s)/Basis
44	103	Payne[1]
44	103	Sakai,[2] Kawagoe[3]

Petitioner relies on the declaration of Travis Blalock, Ph.D. (Ex. 1003, "Blalock Declaration").

II. ANALYSIS

A. Parallel Petitions

Petitioner filed two petitions challenging the '222 patent. Paper 3, 2. According to the Board's Patent Trial Practice Guide,[4] "one petition should be sufficient to challenge the claims of a patent in most situations," but "there may be circumstances in which more than one petition may be

[1] US 4,684,971, issued Aug. 4, 1987 (Ex. 1005).
[2] US 4,907,058, issued Mar. 6, 1990 (Ex. 1006).
[3] US 6,043,114, issued Mar. 28, 2000 (Ex. 1007).
[4] Patent Trial and Appeal Board Consolidated Trial Practice Guide (Nov. 2019), available at https://www.uspto.gov/TrialPracticeGuideConsolidated ("Trial Practice Guide").

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necessary." Trial Practice Guide 59. Petitioner explains that the two petitions filed here have "material differences" including "mutually exclusive claim sets," "significant differences in claim scope between claims of the two claim sets," and "different prior art and prior art combinations to better address the difference in claim scope." Paper 3, 3. In addition, Petitioner notes that the petition in IPR2023-01242 addresses a potential claim-construction dispute, requiring that petition to be longer than it might otherwise be. *Id.* at 4. Patent Owner has not challenged Petitioner's arguments for the institution of multiple petitions, despite having an opportunity to do so. Prelim. Resp. 1–25; Trial Practice Guide 60–61.

On the present record, we agree with Petitioner that the two petitions filed to challenge the claims of the '222 patent will not substantially burden the Board or the parties. The petitions in IPR2023-01242 and IPR2023-01244 challenge different claims, and those claims appear on the present record to have different claim scope, as Petitioner argues. Paper 3, 3 (arguing that claim 44, challenged in IPR2023-01244, recites "a 'surface layer,' a 'single drift layer,' and 'at least one well region disposed in the single drift layer,' which are not" recited in the claims challenged in IPR2023-01242); Ex. 1001, 4:39–8:39. In addition, there is little overlap between the prior art asserted in the two petitions, and what overlap there is—the use of Kawagoe in both petitions—is used in different prior-art combinations in each petition. *Compare* IPR2023-01242, Paper 2, 5 (asserting Kawagoe alone and in combination with Gupta or Silverbrook), *with* IPR2023-01244, Paper 2, 5 (asserting Kawagoe in combination with Sakai). Further, as Petitioner notes, the oral hearing (if requested) and depositions in the two proceedings may be combined, which would further

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reduce the burden placed on the Board and the parties. Accordingly, we do not exercise our discretion to deny either of the petitions challenging the '222 patent for being parallel petitions.

B. Legal Standards

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). The burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A claim is unpatentable under 35 U.S.C. § 103 if "the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains." 35 U.S.C. § 103. The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when present, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

To show obviousness, it is not enough to merely show that the prior art includes separate references covering each separate limitation in a challenged claim. *Unigene Labs., Inc. v. Apotex, Inc.*, 655 F.3d 1352, 1360 (Fed. Cir. 2011). "Rather, obviousness requires the additional showing that a person of ordinary skill at the time of the invention would have selected and combined those prior art elements in the normal course of research and

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development to yield the claimed invention." *Id.* (citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007)). "This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." *KSR*, 550 U.S. at 418–19. On the other hand, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.* at 418; *accord In re Translogic Tech., Inc.*, 504 F.3d 1249, 1259 (Fed. Cir. 2007). Nevertheless, "[a] factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning." *KSR*, 550 U.S. at 421.

C. Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art "would have had a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience." Pet. 7 (citing Ex. 1003 ¶¶ 52–55). According to Petitioner, "[a]dditional education might compensate for a deficiency in experience, and vice-versa." *Id.* On the present record, Patent Owner does not contest Petitioner's definition of a person of ordinary skill in the art. Prelim. Resp. 1–25.

In light of the record before us, and for purposes of this Decision, we adopt Petitioner's proposal regarding the level of ordinary skill in the art. Based on our review of the '222 patent and the prior art of record, we determine that the definition offered by Petitioner comports with the

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qualifications a person would have needed to understand and implement the teachings of the '222 patent and the prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (explaining that specific findings regarding ordinary skill level are not required "where the prior art itself reflects an appropriate level and a need for testimony is not shown") (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985)).

D. Claim Construction

In an *inter partes* review, we construe claim terms according to the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2022). Under *Phillips*, claim terms are afforded "their ordinary and customary meaning." *Phillips*, 415 F.3d at 1312. "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1313. "Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.*

Neither party proposes any claim terms for construction. Pet. 7–8; Prelim. Resp. 1–25. After considering the arguments and information presented in the Petition and Preliminary Response, we agree that we do not need to construe any terms expressly in order to determine whether to institute trial. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms

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need be construed that are in controversy, and only to the extent necessary to resolve the controversy.")).

E. Timeliness of Petition Under 35 U.S.C. § 315(b)

Patent Owner argues that "[t]he Petition should be dismissed because it is untimely." Prelim. Resp. 1. Specifically, Patent Owner argues that Petitioner is in privity with [redacted] who Petitioner asserts are time-barred under 35 U.S.C. § 315(b). *Id.* at 1–25. [redacted] *Id.* at 1 (quoting *Taylor v. Sturgell*, 553 U.S. 880, 894 (2008)). Further, Patent Owner argues, [redacted] Therefore, Petitioner has a [redacted] giving rise to privity." *Id.* at 1–2 (quoting *Taylor*, 553 U.S. at 895; *Applications in Internet Time, LLC v. RPX Corp.*, 897 F.3d 1336, 1360 (Fed. Cir. 2018)).

1. Legal Standard

"[T]he mere existence of some relationship between a petitioner and another entity is not sufficient" to place that petitioner in privity with that entity. *Google LLC v. DDC Technology, LLC*, IPR2023-00707, Paper 27 at 37 (PTAB Oct. 25, 2023). Instead, "that relationship must be related to [an earlier] lawsuit and be sufficiently close that it can be fairly said the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit." *Id.* In other words, privity concerns "whether the petitioner and the prior litigant's relationship—as it relates to the [earlier] lawsuit—is

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sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit," or "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319 (Fed. Cir. 2018).

A petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1244 (Fed. Cir. 2018). In order to raise such a dispute, "a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy]." *Id.* The amount of evidence a patent owner must produce does not rise to the level of that required to overcome a burden of production. *Id.* at 1244 n.8. Instead, the "burden remains with the petitioner to establish" the timeliness of its petition. *Id.* at 1242.

2. Whether We May Consider Petitioner's Preliminary Reply

As noted above, we authorized Petitioner to file a Preliminary Reply and Patent Owner to file a Preliminary Sur-Reply, both limited to addressing the issue of the timeliness of the Petition. Patent Owner argues that consideration of Petitioner's Preliminary Reply "is not appropriate," because "Petitioner could have reasonably foreseen" the timeliness arguments raised in the Preliminary Response when Petitioner was "filing its petition." Prelim. Resp. 23 (quoting *Sandoz Inc. v. Abbvie Biotechnology Ltd.*, IPR2018-00002, Paper 11 at 3 (PTAB Mar. 6, 2018)).

We disagree with this argument raised by Patent Owner. According to the Federal Circuit, a petitioner's "initial identification of the real parties

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in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds*, 903 F.3d at 1244. Thus, there is no requirement that a petitioner preemptively address a disputed issue of privity in its petition.

We also find that Patent Owner's foreseeability argument is factually unsupported. Although Patent Owner argues [redacted] Without more information, the [redacted] would not have suggested Patent Owner's privity argument because Petitioner was not involved in either one.

Accordingly, we consider Petitioner's Preliminary Reply, as well as Patent Owner's Preliminary Sur-Reply, in determining whether Petitioner has shown its Petition is timely.

3. The Effect of the Earlier Suit [redacted] *on the Timeliness of the Present Petition*

Patent Owner alleges that [redacted] are time-barred under § 315(b). Prelim. Resp. 1. [redacted] the present record does not contain any evidence tending to show that this is the case. Section 315(b) bars institution of *inter partes* review only when "the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent." On this record, there is no evidence that [redacted] any earlier than January 23, 2023, which is less than one year before the filing of the present petition on July 27, 2023. *Compare* Pet. 88, *with* Ex. 2019, 1. Accordingly, the service

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of [redacted] time-barred under § 315(b).

Patent Owner also argues that, [redacted] Prelim. Sur-Reply 10 (citing *Kofax Inc. v. Uniloc USA Inc.*, IPR2015-01207, Paper 24 at 4–5 (PTAB July 20, 2016)); *see* Prelim. Resp. 1–3 [redacted] In *Kofax*, the Board held that the real party-in-interest of a petitioner in a first *inter partes* review could be estopped under § 315(e)(1) from seeking institution of a second *inter partes* review once a final written decision had been issued in the first review. *Kofax*, IPR2015-01207, Paper 22 at 10–11. Sections 315(b) and 315(e)(1) both apply not only to the petitioner, but also the "real party in interest, or privy of the petitioner." Patent Owner implicitly argues that the ruling in *Kofax* should extend § 315(b) beyond its limits to bar an [redacted] Prelim. Sur-Reply 10. We see nothing in the Board's decision in *Kofax* that would justify extending § 315(b) so far beyond its statutory text, and Patent Owner provides us with none. Thus, Patent Owner has produced no evidence that [redacted] under § 315(b).[5]

[5] In the next five subsections, [redacted] provides additional support for our conclusion regarding Patent Owner's § 315(b) argument.

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4. [redacted]
Preceding and Succeeding Owners of Property

Patent Owner argues that [redacted] in the form of goods that either infringe the challenged patent's claims [redacted] because [redacted] Prelim. Resp. 13–17. It is true that entities who are "preceding and succeeding owners of property" can be in privity with one another. *Taylor*, 553 U.S. at 894. But it is also true that this rule does not extend to the point where all manufacturers of allegedly infringing goods are in privity with the customers who buy those goods. *See, e.g.*, *WesternGeco*, 889 F.3d at 1319–22 (the parties "had a contractual and fairly standard customer-manufacturer relationship regarding the accused product," which "does not necessarily suggest that the relationship is sufficiently close that both" parties should be considered to be in privity); *Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1340–41 (Fed. Cir. 2018) (same); *Samsung Electronics Co. Ltd. v. Netlist Inc.*, IPR2022-00615, Paper 64, at 22–26 (PTAB June 30, 2023) (same). Thus, to the extent that Patent Owner has produced evidence that [redacted] none of that evidence tends to show that [redacted] Even if a manufacturer-customer relationship with respect to accused products were evidence of privity, [redacted] because Patent Owner asserts unequivocally that [redacted] Prelim. Resp. 10.

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5. [redacted]

Patent Owner argues [redacted] Prelim. Resp. 16–17 (citing *Ventex Co. v. Columbia Sportswear North America, Inc.*, IPR2017-00651, Paper 148 (PTAB Jan. 24, 2019) (precedential)). We disagree. Unlike the agreements in *Ventex*, Paper 148 at 12, [redacted] Even if Petitioner were considered [redacted][6]

6. [redacted]

Patent Owner argues that the doctrine of patent exhaustion [redacted]

[6] In contract law, a third-party beneficiary is not a privy. *See, e.g., Pac. Gas & Elec. Co. v. United States*, 838 F.3d 1341, 1350–51 (Fed. Cir. 2016) ("Limited exceptions to the privity requirement have been recognized when a 'party standing outside of privity by contractual obligation stands in the shoes of a party within privity,' such as when a party can demonstrate that it was an intended third-party beneficiary under the contract."); *Prime Finish, LLC v. Cameo, LLC*, 487 F. App'x 956, 959 (6th Cir. 2012) ("Ordinarily, the obligations arising out of a contract are due only to those with whom it is made; a contract cannot be enforced by a person who is not a party to it or in privity with it, except . . . under certain circumstances, [such as] by a third-party beneficiary.").

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[redacted] Prelim. Resp. 17. According to Patent Owner, [redacted] *Id.* We disagree. It is true that [redacted] against any claim of infringement by Patent Owner. We do not see how such a defense [redacted]

7. [redacted]

Patent Owner argues that [redacted] Prelim. Resp. 18–19. As evidence of this alleged indemnification obligation, Patent Owner directs us to Petitioner's "Standard Terms and Conditions of Sale." *Id.* at 18 (citing Ex. 2010, 3). This evidence shows that Petitioner "agrees to defend any claim, suit or proceeding asserted against Buyer based upon a claim that any Product(s) . . . directly infringes any patent . . . effective in the USA and to pay settlements or costs and damages finally awarded in any such suit." Ex. 2010, 3. This agreement is contingent on Petitioner being "promptly notified in writing of the claim and given, at [Petitioner's] request and expense, sole control of the defense or response to such claim and all requested reasonable assistance by Buyer for defense of the same." *Id.* Moreover, Petitioner has the "sole discretion to (i) obtain for Buyer the right to use and sell the Product, (ii) replace or modify the Product(s) with non-infringing Product(s), or (iii) accept the return of the Product(s) and refund the purchase price less reasonable wear and tear" in lieu of defending against any infringement claim. *Id.*

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An agreement by a petitioner to indemnify a third party in an earlier infringement suit can give rise to a privity relationship between the petitioner and that third party. *Intel Corp. v. U.S. Int'l Trade Comm'n*, 946 F.2d 821, 839 (Fed. Cir. 1991). But not all indemnification agreements create privity between the parties to the agreement. An indemnification agreement does not give rise to privity where the indemnitor has the option either "to pay for any litigation defense expenses or for any damages related to infringement" or, in the alternative, "to modify or replace the equipment if an infringement claim [is] made," as opposed to being required "to defend [the indemnitee] from a patent infringement lawsuit, reimburse or pay for a lawsuit, cover any damages liability for any adverse patent infringement verdict against [the indemnitee], or initiate an invalidity challenge in one or more fora." *WesternGeco*, 889 F.3d at 1321. This describes precisely the option Petitioner has under the Standard Terms and Conditions of Exhibit 2010. Accordingly, we determine that, on the present record, the indemnification agreement of Exhibit 2010 does not [redacted]

Patent Owner speculates that, as [redacted] might have "received terms [even more] generous [than] the 'Standard' conditions [Petitioner] offers to any purchaser." Prelim. Resp. 18. But Patent Owner does not direct us to any such more generous terms in the evidence presently of record. *Id.* at 18–19. "A mere assertion that a third party is an unnamed [privy], without any support for that assertion, is insufficient to put the issue into dispute." *Worlds*, 903 F.3d at 1244. Moreover, Patent Owner does not dispute Petitioner's assertion that [redacted]

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[redacted] with respect to Patent Owner's lawsuit [redacted] Prelim. Reply 6. Thus, on the present record, Patent Owner has not directed us to any evidence that an indemnification obligation creates [redacted]

8. [redacted]

Patent Owner argues that Petitioner is [redacted] Prelim. Resp. 3–4, 19–20. Patent Owner argues that, "by making accused products [redacted] Petitioner acts within the definition of an agent by acting as "[s]omeone who is authorized to act for or in place of another." *Id.* at 20 (quoting Ex. 2041, 1) (second alteration in original). We disagree for three reasons.

First, Patent Owner's agency argument is not based on the applicable legal standard. For purposes of privity under § 315(b), the relevant question is whether [redacted] in filing a petition for *inter partes* review. The applicable principle is that "preclusion is appropriate when a nonparty later brings suit as an agent for a party who is bound by a judgment." *Taylor*, 553 U.S. at 895. As the Federal Circuit explains, the rationale behind § 315(b)'s time bar is "to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation." *WesternGeco*, 889 F.3d at 1319. Therefore, the relevant question is "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *Id.* Here, Patent Owner does not assert that [redacted] in this proceeding. Any such

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assertion would be appropriate only based on evidence that [redacted] *See Taylor*, 553 U.S. at 906 (cautioning that "preclusion is appropriate only if the putative agent's conduct of the suit is subject to the control of the party who is bound by the prior adjudication"). No such evidence is in this record.

Second, the case law cited by Patent Owner does not apply.[7] In each case, the alleged privy was the party asserting a defense of res judicata or collateral estoppel, not the party against whom collateral estoppel was asserted, as is the case here.[8] The privity issue was whether the party raising a res judicata or collateral estoppel defense was in privity with a defendant in a prior lawsuit brought by the same plaintiff. In *Herrion*, for example, the plaintiff brought successive lawsuits arising out of the same incident, and the defendants in the second suit asserted a res judicata defense. 448 F. App'x at 72. Applicable res judicata law required the court to consider whether the defendants in the second lawsuit were in privity with the defendant in the first lawsuit. *Id.* at 72–73 (finding privity existed for res judicata purposes). Similarly, in *John Street*, the court held that plaintiff's second lawsuit was barred by res judicata in part because the defendants were in privity with the

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[7] Prelim. Resp. 19–20 (citing *Herrion v. Children's Hosp. Nat. Med. Ctr.*, 786 F. Supp. 2d 359 (D.D.C.), *aff'd*, 448 F. App'x 71 (D.C. Cir. 2011); *John Street Leasehold, LLC v. Cap. Mgmt. Res., L.P.*, 283 F.3d 73 (2d Cir. 2002); *Fiumara v. Fireman's Fund Ins. Companies*, 746 F.2d 87 (1st Cir. 1984)).

[8] By asserting Petitioner is time-barred under § 315(b), Patent Owner is in effect asserting a collateral estoppel bar against Petitioner. *See WesternGeco*, 889 F.3d at 1318 ("Privity is essentially a shorthand statement that collateral estoppel is to be applied in a given case." (citing Consolidated Trial Practice Guide November 2019 at 15, available at https://www.uspto.gov/TrialPracticeGuideConsolidated)).

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defendants in the prior action. 283 F.3d at 75. Likewise in *Fiumara*, the court held that "the res judicata defense is unmistakably available" to the defendants "as persons in privity with" the defendants in a prior lawsuit brought by the same plaintiff. 746 F.2d at 92. The privity issue in each of these cases was entirely different from this case, where Patent Owner asserts that Petitioner is barred because Petitioner is in privity with the defendants in the prior lawsuit.

Third, even if Patent Owner's argument were on solid legal footing, it lacks factual support in the record. An "essential element[] of agency" is "the principal's 'right to direct or control the agent's actions.'" *In re Google LLC*, 949 F.3d 1338, 1345 (Fed. Cir. 2022) (quoting *Meyer v. Holley*, 537 U.S. 280, 286 (2003)). Patent Owner does not argue in the Preliminary Response that [redacted], much less direct us to any evidence that would tend to prove the existence of such a right. Prelim. Resp. 19–20. In the Preliminary Sur-Reply, Patent Owner argues that [redacted] because [redacted] Prelim. Sur-Reply 8 (citing Ex. 2010, 5; Ex. 2053) (alterations in original). Patent Owner does not, however, present any evidence that Petitioner manufactures products [redacted] *Cf. Google*, 949 F.3d at 1346 (contracts to "[a]ssembl[e] equipment based on information and instructions provided by Google" were "suggestive of an agency relationship" (first alteration in original)). Patent Owner also does not allege that any particular product [redacted] *See* Ex. 2010, 5 (providing different cancelation policies for "standard Product[s]" than for "Custom

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Product[s]"); Ex. 2053, 1 (touting Petitioner's ability to supply "System-on-Chip (SoC), Application Specific Integrated Circuit (ASIC), and other custom solutions," but not identifying any particular such products). Thus, Patent Owner does not direct us to any evidence that Petitioner [redacted]

9. Conclusion as to Timeliness of Petition

As noted above, privity concerns "whether the petitioner and the prior litigant's relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit," or "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *WesternGeco*, 889 F.3d at 1319. A petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds*, 903 F.3d at 1244. In order to raise such a dispute, "a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy]." *Id.* Here, Patent Owner argues that it has produced such evidence in several respects, but, on the present record, none of the evidence in question tends to show [redacted]

F. Challenge Based on Payne

Petitioner contends claim 44 would have been obvious in view of Payne. Pet. 5, 11–40. On the present record, Patent Owner does not dispute Petitioner's arguments. Prelim. Resp. 1–25.

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1. Payne

Payne "relates to complementary field effect transistors formed by ion implantation, and in particular to a structure and method of fabrication which permit high packing density." Ex. 1005, 1:5–8. According to Payne, CMOS devices "comprise n-channel and p-channel devices formed in the same substrate," and they were traditionally "formed by diffusion or implantation of a p-type 'tub' in an n-type silicon substrate so that the n-channel device is fabricated in the tub and the p-channel device is fabricated in the adjacent portion of the substrate." *Id.* at 1:9–18. This method "led to the constraint that the concentration at the surface in the tub was much greater than the surface concentration of the substrate." *Id.* at 1:18–21. To avoid this constraint, Payne states that one method was "to form the p-channel device in a second tub of n-conductivity type and higher impurity concentration than a more lightly doped substrate." *Id.* at 1:24–27. "Using either the single tub or twin tub approach, a considerable amount of semi-conductor area is needed due to the fact that the tub impurities will diffuse laterally as well as vertically during the drive-in to establish the desired tub depth." *Id.* at 1:34–38. Payne states that "[t]his is particularly troublesome in the twin-tub process since any significant overlap of the two tubs results in decreased doping concentration of each tub at the boundaries which can cause punch through or field inversion channeling during device operation." *Id.* at 1:39–43. This problem required large spacing of the source and drain regions of the transistors, and Payne seeks to avoid this need by "provid[ing] a CMOS structure and method of manufacture which requires little semiconductor space." *Id.* at 1:43–54.

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In particular, Payne's "device is fabricated in a silicon semiconductor substrate, 10, of 'N--' conductivity type which . . . is typically approximately 20 mils thick." Ex. 1005, 2:56–60. On this substrate, tub regions 15 and 17 are formed, one "having the same conductivity type as the substrate but higher impurity concentration" and the other having the opposite conductivity type. *Id.* at 3:35–39, 4:12–14, Figs. 2–5. Surface regions 18 and 20 are formed "covering essentially the same area as" tubs 15 and 17, with each region having the same conductivity type as the tub over which it lies but with higher impurity concentration. *Id.* at 4:31–5:17, Figs. 7–9, 11. Payne's CMOS device includes a "p-channel device [that] includes source and drain regions, 21 and 22, respectively, of P+ conductivity type formed with[in] the N surface region, 18" and an "n-channel device [that] includes source and drain regions, 23 and 24, of N+ conductivity type formed within the P surface region 20." *Id.* at 5:21–27, Fig. 10. Payne states that this approach can reduce the spacing between "source and drain regions of adjacent devices" from 12 microns to 5 microns. *Id.* at 5:54–6:19, Figs. 12, 13.

2. Analysis

Petitioner argues that Payne would have taught or suggested the limitations of claim 44. Pet. 5, 11–40. On the present record, Patent Owner does not disagree. Prelim. Resp. 1–25.

The preamble of claim 44 recites "[a] CMOS Semiconductor device." Ex. 1001, 8:21. Petitioner argues that Payne teaches the preamble. Pet. 12. Patent Owner does not dispute this argument. Prelim. Resp. 1–25. Payne discloses that "a primary object of [its] invention [is] to provide a CMOS structure and method of manufacture which requires little semiconductor

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space." Ex. 1005, 1:51–54. Thus, Petitioner has shown sufficiently that Payne teaches the preamble of claim 44.

Claim 44 recites "a surface layer." Ex. 1001, 8:22. Petitioner argues that Payne teaches or suggests this limitation, and Patent Owner does not dispute this argument. Pet. 12–14; Prelim. Resp. 1–25. Petitioner directs us to evidence that tends to show that Payne discloses a surface layer similar to that in the '222 patent. Ex. 1001, Fig. 5(b); Ex. 1003 ¶¶ 68–70; Ex. 1005, 2:50–60, 5:21–27, 6:57–59, Fig. 10; Ex. 1030, 6, 7, 9, 12, 13; Ex. 1033. In particular, Figure 5(b) of the '222 patent and Payne's Figure 10 show quite similar structures, and Patent Owner's district court claim construction brief identified the relevant structure in Figure 5(b) of the '222 patent as a surface layer. Ex. 1030, 7, 12. Thus, Petitioner has shown sufficiently that Payne teaches this limitation of claim 44.

Claim 44 recites "a substrate." Ex. 1001, 8:23. Petitioner argues that Payne teaches this limitation, and Patent Owner does not dispute this argument. Pet. 14–15; Prelim. Resp. 1–25. Payne discloses fabricating its CMOS device "in a silicon semiconductor substrate." Ex. 1005, 1:60–65, 2:50–60, Fig. 10. Thus, Petitioner has shown sufficiently that Payne teaches this limitation of claim 44.

Claim 44 recites "an active region including a source and a drain, disposed on one surface of the surface layer." Ex. 1001, 8:24–25. Petitioner argues that Payne teaches this limitation, and Patent Owner does not dispute this argument. Pet. 15–18; Prelim. Resp. 1–25. Payne discloses forming p-channel and n-channel transistors, each with source and drain regions. Ex. 1005, 1:5–19, 5:18–29, 6:57–59. Petitioner directs us to evidence that a person of ordinary skill in the art would have considered the transistors to be

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active regions. Ex. 1001, Fig. 5(b); Ex. 1030, 6–7, 11; Ex. 1003 ¶¶ 75–77; Ex. 1008B, 299–300. Thus, Petitioner has shown sufficiently that Payne teaches this limitation of claim 44.

Claim 44 recites "a single drift layer disposed between the other surface of the surface layer and the substrate." Ex. 1001, 8:26–27. Petitioner argues that Payne teaches this limitation, and Patent Owner does not dispute this argument. Pet. 18–21; Prelim. Resp. 1–25. Payne discloses a first tub region with a surface region in it that, on the present record, appears quite similar to the single drift layer and well region of the '222 patent. *Compare* Ex. 1003 ¶ 82; Ex. 1005, 3:28–43, 4:19–39, 5:7–17, 5:44–50, *with* Ex. 1001, Fig. 5(b); Ex. 1030, 7, 11. Thus, Petitioner has shown sufficiently that Payne teaches this limitation of claim 44.

Claim 44 recites "the drift layer having a graded concentration of dopants extending between the surface layer and the substrate." Ex. 1001, 8:27–29. Petitioner argues that Payne teaches this limitation, and Patent Owner does not dispute this argument. Pet. 21–24; Prelim. Resp. 1–25. Payne's Figure 11 shows a dopant concentration in tubs 15, 17 that decreases with increasing depth. Ex. 1005, 2:38–41, 5:14–17, 5:56–57, Figs. 10, 11. Thus, Petitioner has shown sufficiently that Payne teaches this limitation of claim 44.

Claim 44 recites "the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions." Ex. 1001, 8:29–34. Petitioner argues that Payne teaches this limitation, and Patent Owner does not dispute this argument. Pet. 24–33; Prelim. Resp. 1–25. Petitioner relies on the parent file history and cited references to argue

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that the presence of a graded dopant concentration similar to that in Payne "creates a 'built-in' electrical field that forces the movement of carriers into a particular direction" and that the direction in which carriers are forced with the concentration profile disclosed in Payne is downward, toward the substrate and away from the surface. Pet. 26–31 (citing Ex. 1010, 2:27–32, 5:14–22; Ex. 1020, 289–90) (emphasis omitted). Payne discloses that its active regions are located on the surface, rather than in the substrate. Ex. 1005, 1:5–15, 1:51–54, 2:50–60, 3:28–4:25, 4:31–5:12, 5:18–29, Figs. 1–10. Thus, Petitioner has shown sufficiently that Payne teaches this limitation of claim 44.

Claim 44 recites

> at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

Ex. 1001, 8:34–39. Petitioner argues that Payne teaches this limitation, and Patent Owner does not dispute this argument. Pet. 33–40; Prelim. Resp. 1–25. Petitioner argues that Payne's tub region 15 satisfies this claim limitation to the same extent as the well region that Patent Owner identifies in Figure 5(b) of the '222 patent, and that this layer has a graded dopant concentration. Pet. 34–36 (citing Ex. 1001, Fig. 5(b); Ex. 1030, 7; Ex. 1005, 1:65–68, 4:31–39, 4:63–5:14, 5:44–55, Figs. 10–11). Relying on Patent Owner's arguments during prosecution and district court claim construction, Petitioner contends that the presence of this layer creates a second "static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the area of the substrate where there are no active

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regions." Pet. 38–39; Ex. 1003 ¶¶ 117–121. Thus, Petitioner has shown sufficiently that Payne teaches this limitation of claim 44.

G. Challenges Based on the Combination of Sakai and Kawagoe

Petitioner contends that claim 44 would have been obvious in view of the combination of Sakai and Kawagoe. Pet. 5, 40–74. On the present record, Patent Owner does not dispute Petitioner's arguments. Prelim. Resp. 1–25.

1. Sakai

Sakai "relates to . . . a CMOS, in which an isolation region between two well regions of opposite conductivity types, each including an insulated gate field effect transistor . . . , is made very small in size to make possible a high-speed operation and large scale integration." Ex. 1006, 1:7–13. According to Sakai, "[i]n a conventional device . . . , in order to prevent the punch through and short channel effect," doped regions must be placed at least "several micrometers" apart, "which makes it difficult to increase the packing density of CMOS." *Id.* at 1:26–43. To increase the packing density, Sakai describes a process in which the CMOS is formed in "a double well structure, in which" shallow wells are formed within deep wells, and source and drain regions are formed within the shallow wells. *Id.* at 1:55–2:5.

2. Kawagoe

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device using an epitaxial wafer, i.e., a semiconductor wafer having a semiconductor single crystal epitaxial layer grown over a polished semiconductor substrate. Ex. 1007, 1:13–27, 2:31–35. According to Kawagoe, "[t]he epitaxial wafer is advantageous in that it is excellent in

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suppressing the soft errors and resisting to the latchup,"[9] as well as "drastically reduc[ing] the defect density of the gate insulating film" of a semiconductor integrated device. *Id.* at 1:33–40.

Kawagoe discloses various "[r]epresentative[]" processes, including processes in which the single crystal (epitaxial) layer contains an impurity of the same type and in the same concentration as the substrate body. Ex. 1007, 2:55–3:9. According to Kawagoe, the impurity concentration of the substrate body can be made higher than that of epitaxial layer "so that the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup." *Id.* at 4:1–8. Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device including a step of forming a semiconductor region (well) extending below the epitaxial layer and having an impurity concentration that decreases with increasing depth below the epitaxial layer. *Id.* at 3:10–25. According to Kawagoe, the well can be used for forming a complementary Metal-Oxide-Semiconductor.Field-Effect-Transistor ("MOS.FET") circuit. *Id.* at 3:32–38.

Kawagoe describes seven embodiments, including Embodiment 1 (Ex. 1007, 6:41–12:40, Figs. 1–8) and Embodiment 4 (*id.* at 14:46–19:64, Figs. 16–25). According to Embodiment 1, a semiconductor integrated

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[9] Petitioner submits Exhibit 1013 (Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Int'l Conf on VLSI Design, 429–434, IEEE 2008), which explains that "soft errors" are "random and not related to permanent hardware faults" and "[t]heir causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation)," including "alpha particles [that] are emitted when the nucleus of an unstable isotope decays to a lower energy state." Ex. 1013, Abstract, 430.

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circuit device includes semiconductor substrate body 2S, epitaxial layer 2E, and gettering layer 2G. *Id.* at 6:51–56, Fig. 1. Substrate body 2S and epitaxial layer 2E are doped with p-type impurity in equal concentrations. *Id.* at 6:60–7:3, 10:51–55, 11:12–16. Embodiment 1 includes n-channel MOS.FET ("nMOS") 4N and p-channel MOS.FET ("pMOS") 4P, the latter being formed in n-well 6, which is doped with n-type impurity and extends below the epitaxial layer. *Id.* at 8:46–52, 9:32–40, 11:18–24, 11:43–50, Figs. 1, 5, 7.

According to Embodiment 4, substrate body 2S and epitaxial layer 2E are doped with p-type impurity, and the impurity concentration of substrate body 2S is higher than that of epitaxial layer 2E "to improve the resistance to the latchup." Ex. 1007, 14:64–15:6, 15:13–17, 16:16–21, 19:59–63, Fig. 17. Embodiment 4 includes p-well 6*p* formed with nMOS 4N and n-well 6*n* formed with pMOS 4P. *Id.* at 15:26–40, 17:40–18:35, Figs. 16, 21–23. In Embodiment 4, the impurity concentration in p-well 6*p* and n-well 6*n* decreases with increasing depth below the epitaxial layer. *Id.* at 15:62–16:15, 17:55–61, Fig. 17. Kawagoe discloses that the concentration gradient reduces soft errors by attracting carriers (electrons) to the substrate and preventing them from entering the p-well. *Id.* at 16:2–11.

Petitioner relies on Kawagoe Figures 17 and 23, which illustrate Embodiment 4 and are reproduced below.

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FIG. 17

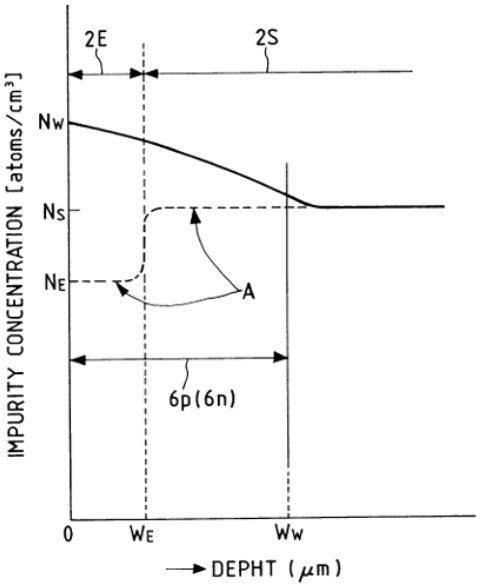

FIG. 23

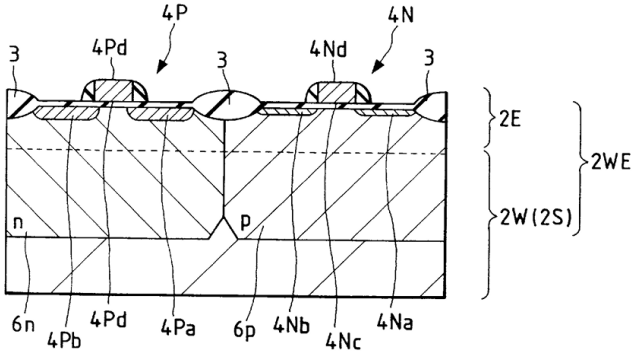

Figure 17 is a plot of impurity concentration as a function of depth in a semiconductor integrated circuit device, which shows "the p-well 6*p* and n-well 6*n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer 2E." Ex. 1007, 5:41–45, 15:62–16:40. Figure 23 shows a step in a process for manufacturing a semiconductor integrated circuit device, including p-well 6*p* formed with nMOS 4N and n-well 6*n* formed with pMOS 4P. *Id.* at 5:1–4, 15:26–32, 18:3–35.

3. Analysis

Petitioner argues that the combination of Sakai and Kawagoe would have taught or suggested the limitations of the challenged claims and that a person of ordinary skill in the art would have had reason to combine the teachings of Sakai and Kawagoe. Pet. 5, 40–74. On the present record, Patent Owner does not disagree. Prelim. Resp. 1–25.

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a) Reason to Combine Sakai and Kawagoe

Petitioner argues that a person of ordinary skill in the art would have had a reason to combine the teachings of Sakai with those of Kawagoe. Pet. 54–57. On the present record, Patent Owner does not dispute this argument. Prelim. Resp. 1–25. Petitioner argues specifically that the combination of Sakai and Kawagoe would have achieved both Sakai's benefit of improving the packing density of CMOS chips and Kawagoe's benefit of reducing soft errors. On the present record, Sakai discloses that "[i]t is an object of the present invention to provide a CMOS which is very high in packing density," and Kawagoe discloses that "the impurity concentration of" its wells "is given such a gradient that . . . the influence to be caused by the carriers (or electrons) due to the α-ray is lowered . . . so that the soft errors can be reduced." Ex. 1006, 1:55–56; Ex. 1007, 16:2–11. Petitioner directs us to evidence that a person of ordinary skill in the art would have known that "as geometries have been scaled down to produce circuits of greater density, alpha-particle-induced soft-error rates have also become a concern." Pet. 55; Ex. 1008B, 583. Accordingly, Petitioner has shown sufficiently, for purposes of this decision, that a person of ordinary skill in the art would have had a reason to combine the teachings of Sakai with those of Kawagoe.

b) Teachings of Sakai and Kawagoe

Petitioner argues that the combination of Sakai and Kawagoe would have taught or suggested the limitations of claim 44. Pet. 5, 40–67. On the present record, Patent Owner does not disagree. Prelim. Resp. 1–25.

The preamble of claim 44 recites "[a] CMOS Semiconductor device." Ex. 1001, 8:21. Petitioner argues that the combination of Sakai and

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Kawagoe teaches the preamble. Pet. 40–41. Patent Owner does not dispute this argument. Prelim. Resp. 1–25. Sakai "relates to a complementary semiconductor device (hereinafter referred to as 'CMOS')." Ex. 1006, 1:6–13. Thus, Petitioner has shown sufficiently that the combination of Sakai and Kawagoe teaches the preamble of claim 44.

Claim 44 recites "a surface layer." Ex. 1001, 8:22. Petitioner argues that the combination of Sakai and Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 41–43; Prelim. Resp. 1–25. Petitioner directs us to evidence that tends to show that Sakai discloses a surface layer similar to that in the '222 patent. Pet. 42 (citing Ex. 1001, Fig. 5(b); Ex. 1003 ¶¶ 127–129; Ex. 1005, 1:28–30, 1:68–2:5, 4:25–29, 5:53–55, 5:59, 6:16–17, Fig. 10D; Ex. 1030, 6, 7, 9, 12, 13; Ex. 1033). In particular, Figure 5(b) of the '222 patent and Sakai's Figure 10D show quite similar structures, and Patent Owner identified the relevant structure in Figure 5(b) of the '222 patent as a surface layer. Ex. 1030, 7, 12. Thus, Petitioner has shown sufficiently that the combination of Sakai and Kawagoe teaches this limitation of claim 44.

Claim 44 recites "a substrate." Ex. 1001, 8:23. Petitioner argues that the combination of Sakai and Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 43–45; Prelim. Resp. 1–25. Sakai discloses "a silicon substrate . . . made of N-silicon or P-silicon." Ex. 1006, 4:13–14. Thus, Petitioner has shown sufficiently that the combination of Sakai and Kawagoe teaches this limitation of claim 44.

Claim 44 recites "an active region including a source and a drain, disposed on one surface of the surface layer." Ex. 1001, 8:24–25. Petitioner argues that the combination of Sakai and Kawagoe teaches this limitation,

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and Patent Owner does not dispute this argument. Pet. 45–48; Prelim. Resp. 1–25. Sakai discloses forming p-channel and n-channel transistors, each with source and drain regions. Ex. 1006, 5:53–55, 5:64–6:4, 6:16–17, Fig. 10D. Petitioner directs us to evidence that a person of ordinary skill in the art would have considered the transistors to be active regions. Ex. 1001, Fig. 5(b); Ex. 1030, 6–7, 10–12; Ex. 1003 ¶¶ 133–138; Ex. 1008B, 299–300. Thus, Petitioner has shown sufficiently that the combination of Sakai and Kawagoe teaches this limitation of claim 44.

Claim 44 recites "a single drift layer disposed between the other surface of the surface layer and the substrate." Ex. 1001, 8:26–27. Petitioner argues that the combination of Sakai and Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 48–50; Prelim. Resp. 1–25. Sakai discloses a deep P-well region and a deep N-well region that, on the present record, appear quite similar to the single drift layer and well region of the '222 patent. *Compare* Ex. 1003 ¶¶ 140–143; Ex. 1006, 1:57–67, 5:56–6:4, 7:32–37, Fig. 10D, *with* Ex. 1001, Fig. 5(b); Ex. 1030, 7, 11, 16. Thus, Petitioner has shown sufficiently that the combination of Sakai and Kawagoe teaches this limitation of claim 44.

Claim 44 recites "the drift layer having a graded concentration of dopants extending between the surface layer and the substrate." Ex. 1001, 8:27–29. Petitioner argues that the combination of Sakai and Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 50–54; Prelim. Resp. 1–25. Sakai discloses that the dopant concentration in its shallow well regions is higher than the dopant concentration in its deep well regions. Ex. 1003 ¶¶ 144–151; Ex. 1006, 5:56–6:4. Petitioner argues that a person of ordinary skill in the art would

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have understood that, because these varying dopant concentrations were "formed 'through ion implantation techniques and thermal diffusion techniques,'" the concentration would gradually decrease with increasing depth. Pet. 51 (citing Ex. 1003 ¶¶ 144–151; Ex. 1006, 5:56–6:4, 6:24–28, 6:52–58, 8:35–38). In addition, Kawagoe discloses that the wells of its CMOS device "have their impurity concentrations gradually lowered in the depthwise direction." Ex. 1007, 15:62–16:40, Figs. 17, 23. Thus, Petitioner has shown sufficiently that the combination of Sakai and Kawagoe teaches this limitation of claim 44.

Claim 44 recites "the drift layer further having a first static unidirectional electric drift field to aid the movement of carriers from the surface layer to an area of the substrate where there are no active regions." Ex. 1001, 8:27–33. Petitioner argues that the combination of Sakai and Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 57–61; Prelim. Resp. 1–25. Relying on Patent Owner's prosecution history arguments, Petitioner argues that the presence of a graded dopant concentration in the combination of Sakai and Kawagoe "creates a 'built-in' unidirectional electric drift field . . . to aid the movement of minority carriers from the surface layer to an area of the substrate where there are no active regions." Pet. 59–60 (citing Ex. 1003 ¶¶ 160–165). Sakai discloses that its active regions are located on the surface, rather than in the substrate. Ex. 1006, Fig. 10D. Thus, Petitioner has shown sufficiently that the combination of Sakai and Kawagoe teaches this limitation of claim 44.

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Claim 44 recites

> at least one well region disposed in the single drift layer, the well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of carriers from the surface layer to the area of the substrate where there are no active regions.

Ex. 1001, 8:34–39. Petitioner argues that the combination of Sakai and Kawagoe teaches this limitation, and Patent Owner does not dispute this argument. Pet. 61–67; Prelim. Resp. 1–25. Petitioner contends that, in the combination of Sakai and Kawagoe, each shallow well is disposed in a single drift layer and has a graded dopant concentration. Pet. 61–63 (citing Ex. 1003 ¶¶ 169–174; Ex. 1006, 1:57–67, 5:56–6:4, 7:32–37, Figs. 10D, 11E; Ex. 1007, 15:62–16:7). Petitioner contends that the combination of Sakai and Kawagoe satisfies this claim limitation to the same extent as the well region Patent Owner identifies in Figure 5(b) of the '222 patent. *Id.* (citing Ex. 1001, Fig. 5(b); Ex. 1030, 7). Relying on Patent Owner's arguments during prosecution and district court claim construction, Petitioner contends that the presence of this layer creates a second "static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the area of the substrate where there are no active regions." Pet. 65–67; Ex. 1003 ¶¶ 175–178. Thus, Petitioner has shown sufficiently that the combination of Sakai and Kawagoe teaches this limitation of claim 44.

III. CONCLUSION

Upon consideration of the Petition, the Preliminary Response, the Preliminary Reply, the Preliminary Sur-Reply, and the evidence presented, we determine that Petitioner has shown a reasonable likelihood that it will

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prevail in showing that the challenged claim is unpatentable. In addition, we are persuaded on the present record that the Petition is not time-barred under 35 U.S.C. § 315(b). Accordingly, we institute an *inter partes* review of the challenged claim based on the grounds asserted in the Petition.

IV. ORDER

For the reasons given, it is:

ORDERED that an *inter partes* review is instituted with respect to the grounds asserted in the Petition;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision;

FURTHER ORDERED that, in view of the pending motion to seal, this Decision is being filed "Board and Parties Only"; and

FURTHER ORDERED that after conferring with Petitioner, Patent Owner shall, within one week of this Decision, submit to the Board via email to Trials@uspto.gov, a version of this Decision to be filed on the public record, with any redactions proposed by either party.

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