UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,
Petitioner

v.

GREENTHREAD LLC,
Patent Owner

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IPR2024-00264
U.S. Patent No. 10,734,481

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PETITIONER'S UPDATED EXHIBIT LIST

UPDATED EXHBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 10,734,481 to Rao (the "'481 Patent")
1002	Prosecution History of the '481 Patent
1003	Declaration of Travis Blalock, PhD
1004	Curriculum Vitae of Travis Blalock, PhD
1005	Publication Declaration of Sean O'Bryan for Maziasz ("O'Bryan Decl.")
1006	U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek")
1007	U.S. Patent No. 6,043,114 to Kawagoe, et al. ("Kawagoe")
1008A	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol 1, Lattice Press (2000) ("Wolf.1")
1008B	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 2, Lattice Press (2000) ("Wolf.2")
1008C	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 3, Lattice Press (2000) ("Wolf.3")
1008D	Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 4, Lattice Press (2000) ("Wolf.4")
1009	Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Intl Conf on VLSI Design, IEEE 2008 ("Wang")
1010	U.S. Patent No. 4,481,522 to Jastrzebski, et al. ("Jastrzebski")
1011	Publication Declaration of Martin L. Knott for Rabaey ("Knott Decl.")
1012	Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 ("Resnick Decl.")
1013	Publication Declaration of Rachel J. Watters for Wolf.3 and Wolf.4 ("Watters Decl.")
1014	U.S. Patent No. 6,163,877 to Gupta ("Gupta")
1015	U.S. Patent No. 6,534,805 to Jin ("Jin")
1016	Excerpts from the Prosecution History of U.S. Patent No. 8,421,195 (the "'195 Patent")
1017	Patent Owner's Proposed Constructions, *Greenthread, LLC, v. Intel Corp.*, Civil Action No. 6:22-cv-105 (W.D. Tex. Sep. 19, 2022)
1018	Defendants' Preliminary Proposed Constructions, *Greenthread, LLC, v. Intel Corp.*, Civil Action No. 6:22-cv-105 (W.D. Tex. Sep. 19, 2022)

Exhibit No.	Description
1019	Defendants' Opening Claim Construction Brief, *Greenthread, LLC, v. Intel Corp.*, Dkt. 82, Civil Action No. 6:22-cv-105 (W.D. Tex. Oct. 10, 2022)
1020	Patent Owner's Responsive Claim Construction Brief, *Greenthread, LLC, v. Intel Corp.*, Dkt. 96, Civil Action No. 6:22-cv-105 (W.D. Tex. Oct. 31, 2022)
1021	Defendants' Reply Claim Construction Brief, *Greenthread, LLC, v. Intel Corp.*, Dkt. 100, Civil Action No. 6:22-cv-105 (W.D. Tex. Nov. 14, 2022)
1022	Sze, *Semiconductor Devices Physics and Technology*, 2d Ed., John Wiley & Sons (2002)
1023	Maziasz and Hayes, *Layout Minimization of CMOS Cells*, Kluwer Academic Publishers (1992) ("Maziasz")
1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics, dated March 31, 2023
1025	Rabaey *et al.*, *Digital Integrated Circuits, A Design Perspective,* Prentice Hall Electronics and VLSI Series (2003) ("Rabaey")
1026	Gregory and Shafer, "Latch-Up In CMOS Integrated Circuits," IEEE Transactions on Nuclear Science, Volume 20, Issue 6 (1973)
1027	U.S. Patent Application Publication No. 2007/0045682 to Hong *et al*. ("Hong")
1028	Excerpts from the Prosecution History of U.S. Patent Application No. 10/934,915 (the "'915 App.")
1029	Excerpts from the Prosecution History of U.S. Patent No. 9,190,502 (the "'502 Patent")
1030	Excerpts from the Prosecution History of U.S. Patent Application No. 13/854,319 (the "'319 App.")
1031	U.S. Patent No. 4,160,985 to Kamins *et al.* ("Kamins")
1032	McGraw-Hill Dictionary of Scientific and Technical Terms (2003)
1033	U.S. Patent No. 9,647,070 to Rao (the "'070 Patent")
1034	U.S. Patent Application Publication No. 2003/0030488 to Hueting *et al.* ("Hueting")
1035	[Intentionally Omitted]

Exhibit No.	Description
1036	Proposed Claim Constructionsin the Intel Litigation, *Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.*, Civil Action No. 6:22-cv-105 (W.D. Tex.)
1037	Howe and Sodini, *Microelectronics, An Integrated Approach*, Prentice Hall Electronics and VLSI Series (1997) ("Howe")
1038	Hodges *et al.*, *Analysis and Design of Digital Integrated Circuits In Deep Submicron Technology,* 3rd Ed., McGraw-Hill (2004) ("Hodges")
1039	Publication Declaration of Martin L. Knott for Hodges ("Knott Decl.")
1040	Jaeger, *Microelectronic Circuit Design*, McGraw-Hill (1997) ("Jaeger")
1041	Kang and Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, McGraw-Hill (2003) ("Kang")
1042	U.S. Patent No. 6,614,560 to Silverbrook ("Silverbrook")
1043	Publication Declaration of Sylvia Hall-Ellis for Wolf
1044	Wong, H. P., et al. "CMOS active pixel image sensors fabricated using a 1.8-V, 0.25-µm CMOS technology." IEEE Transactions on Electron Devices 45.4 (1998): 889-894.
1045	Law360 Article "*Stays Pending IPR In Del. District Courts Are Here To Stay*," Kraning and Del Dotto, March 11, 2022.
1046	01242 Paper 32 - Decision granting Inter Partes Review - PO material
1047	01242 Paper 35 - Decision granting Inter Partes Review - public
1048	01243 Paper 31 - Decision granting Inter Partes Review - PO material
1049	01243 Paper 34 - Decision granting Inter Partes Review – public
1050	01244 Paper 32 - Decision granting Inter Partes Review - PO material
1051	01244 Paper 35 - Decision granting Inter Partes Review – public
1052	01242 Paper 22 - Petitioner's Authorized Reply to Patent Owner's Preliminary Response – confidential
1053	01243 Paper 21 - Petitioner's Authorized Reply to Patent Owner's Preliminary Response – confidential
1054	01244 Paper 22 - Petitioner's Authorized Reply to Patent Owner's Preliminary Response - confidential
1055	Authorization Email to Board

Dated: May 31, 2024

Respectfully submitted,

/Roger Fulghum/

Roger Fulghum
Reg. No. 39,678
Attorney for Petitioner
BAKER BOTTS L.L.P.
One Shell Plaza
910 Louisiana Street
Houston, TX 77002
T: (713) 229-1234
F: (713) 229-1522

CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. § 42.6(e), the undersigned certifies that on the 31st day of May, 2024, a complete and entire copy of this **PETITIONER'S UPDATED EXHIBIT LIST** was served on Patent Owner electronically via email to counsel for the Patent Owner:

Greenthread-OnSemi-MS@mckoolsmith.com

awhitehurst@mckoolsmith.com

nmatich@mckoolsmith.com

ajairam@mckoolsmith.com

smccommas@mckoolsmith.com

nozarkar@mckoolsmith.com

Dated: May 31, 2024

Respectfully submitted,

/Roger Fulghum/
Roger Fulghum
Reg. No. 39,678