

[REDACTED]

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

IPR2024-00264
Patent 10,734,481 B2

Before KRISTINA M. KALAN, JON B. TORNQUIST, and
MONICA S. ULLAGADDI, *Administrative Patent Judges*.

ULLAGADDI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Semiconductor Components Industries, LLC d/b/a onsemi (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–9, 13–27, and 31–36 (“the challenged claims”) of U.S. Patent No. 10,734,481 B2 (Ex. 1001, “the ’481 patent”), accompanied by the supporting Declaration of Dr. Travis Blalock (Ex. 1003). Greenthread, LLC (“Patent Owner”) filed a Preliminary Response. Paper 13 (“Prelim. Resp.”).

With our authorization, Petitioner filed a Preliminary Reply (Paper 15, “Prelim. Reply”), and Patent Owner filed a Preliminary Sur-reply (Paper 18, “Prelim. Sur-reply”).

We have authority to determine whether to institute an *inter partes* review. *See* 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Having considered the parties’ arguments and the evidence of record, we determine that, for the reasons discussed herein, Petitioner demonstrates a reasonable likelihood that it would prevail with respect to at least one of the challenged claims. We thus institute an *inter partes* review on all challenged claims on all asserted grounds. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1354, 1359–60 (2018).

II. BACKGROUND

A. *Real Parties in Interest*

Petitioner identifies Semiconductor Components Industries, LLC and ON Semiconductor Corporation as the real parties-in-interest. Pet. 1.

Patent Owner identifies Greenthread, LLC as the real party-in-interest.
Paper 4, 1.

B. Related Matters

The parties indicate that the '481 patent is involved in the following district court cases:

Greenthread, LLC v. Cirrus Logic, Inc., Case No. 1:23-cv-00369 (W.D. Tex.);

Greenthread, LLC v. OmniVision Technologies, Inc., Case No. 2:23-cv-00212 (E.D. Tex.);

Greenthread, LLC v. OSRAM GmbH et al., Case No. 2:23-cv-00179 (E.D. Tex.);

Greenthread, LLC v Texas Instruments Incorporated, Case No. 2:23-cv-00157 (E.D. Tex.); and

Greenthread, LLC v. Monolithic Power Systems, Inc., Case No. 1:23-cv-00579 (D. Del.).

Pet. 1; Paper 4, 2–3.

C. The '481 Patent

The '481 patent, titled “Semiconductor Devices with Graded Dopant Regions,” issued on August 4, 2020. Ex. 1001, codes (45), (54).¹ The '481

¹ The '481 patent issued from application No. 16/717,950, filed on Dec. 17, 2019, is a continuation of application No. 15/590,282, filed on May 9, 2017, now US Patent No. 10,510,842, which is a continuation of application No. 14/931,636, filed on Nov. 3, 2015, now US Patent No. 9,647,070, which is a continuation of application No. 14/515,584, filed on Oct. 16, 2014, now US Patent No. 9,190,502, which is a continuation of application No. 13/854,319, filed on Apr. 1, 2013, now abandoned, which is a continuation of application No. 11/622,496, filed on Jan. 12, 2007, now US Patent No. 8,421,195 (“the '195 patent”), which is a division of

patent “relates to all semiconductor devices and systems.” *Id.* at 1:36–37. According to the ’481 patent, in bipolar junction transistors, “[e]fforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier’s speed from emitter to collector.” *Id.* at 1:59–61. This improvement has not been implemented in “most semiconductor devices, including various power MOSFETs . . . [and] IGBT[s],” which “still use a uniformly doped ‘drift epitaxial’ region in the base.” *Id.* at 1:61–66. The invention of the ’481 patent implements graded dopant concentration in these devices, which causes “[t]wo important performance enhancements.” *Id.* at 3:42–43. These include sweeping electrons “from source to drain rapidly” and simultaneously causing holes to “be recombined closer to the n+ buffer layer,” which “can improve t_{ON} and t_{OFF} in the same device.” *Id.* at 3:43–47.

D. Illustrative Claim

Of the challenged claims, claims 1 and 20 are independent. Claim 1 is illustrative and reproduced below.

1. A semiconductor device, comprising:
 - [1.1] a substrate of a first doping type at a first doping level having first and second surfaces;
 - [1.2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
 - [1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

application No. 10/934,915, filed on Sep. 3, 2004, now abandoned. Ex. 1001, codes (21), (22), (60).

[1.4] transistors formed in at least one of the first active region or second active region;

[1.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and

[1.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

Ex. 1001, 4:50–5:3 (bracketed designations added by Petitioner (*see* Pet. 8–24, App. A, 1)).

E. Asserted Grounds

Petitioner presents the following challenges. Pet. 7.

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–9, 13–14, 16–27, 31–36	103(a) ²	Kawagoe ³
1, 2, 4–9, 13–22, 24–27, 31–36	103(a)	Wieczorek ⁴ , Wolf ⁵

² The Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) (“AIA”), included revisions to 35 U.S.C. §§ 102 and 103 that became effective after the effective filing date of the challenged claims. *See* Ex. 1001, codes (22), (60). Therefore, we apply the pre-AIA versions of 35 U.S.C. §§ 102 and 103(a).

³ US Patent No. 6,043,114, filed September 22, 1997, issued March 28, 2000, to Kawagoe et al. (Ex. 1007, “Kawagoe”).

⁴ US Patent Application Pub. No. 2003/0183856 A1, filed October 29, 2002, published October 2, 2003, to Wieczorek et al. (Ex. 1006, “Wieczorek”).

⁵ Petitioner cites four volumes for Wolf: STANLEY WOLF & RICHARD TAUBER, SILICON PROCESSING FOR THE VLSI ERA, VOLUME 1 – PROCESS TECHNOLOGY, 2nd ed., (Lattice Press 2000) (Ex. 1008A); STANLEY WOLF & RICHARD TAUBER, SILICON PROCESSING FOR THE VLSI ERA, VOLUME 2 – PROCESS INTEGRATION, (Lattice Press 2000) (Ex. 1008B); STANLEY WOLF &

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–9, 13–14, 16–27, 31–36	103(a)	Kawagoe, Gupta ⁶
1–2, 4–9, 13–22, 24–27, 31–36	103(a)	Wieczorek, Wolf, Gupta
19, 36	103(a)	Kawagoe, Silverbrook ⁷
19, 36	103(a)	Wieczorek, Wolf, Silverbrook

III. ANALYSIS

A. Legal Standards

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness.⁸ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

RICHARD TAUBER, SILICON PROCESSING FOR THE VLSI ERA, VOLUME 3 – THE SUBMICRON MOSFET, (Lattice Press 2000) (Ex. 1008C); and STANLEY WOLF & RICHARD TAUBER, SILICON PROCESSING FOR THE VLSI ERA, VOLUME 4 – DEEP-SUBMICRON PROCESS TECHNOLOGY, (Lattice Press 2000) (Ex. 1008D).

⁶ US Patent No. 6,163,877, filed November 5, 1996, issued December 19, 2000, to Gupta (Ex. 1014, “Gupta”).

⁷ US Patent No. 6,614,560 B1, filed July 10, 1998, issued September 2, 2003, to Silverbrook (Ex. 1042, “Silverbrook”).

⁸ Patent Owner presents no objective evidence of nonobviousness at this stage of the proceeding.

B. Timeliness of Petition Under 35 U.S.C. § 315(b)

Patent Owner argues that the Petition should be dismissed because it is untimely. Prelim. Resp. 18. Specifically, Patent Owner argues that Petitioner is in privity with [REDACTED]

[REDACTED] as “Licensees”—who Patent Owner asserts are time-barred under 35 U.S.C. § 315(b) and licensed under Greenthread patents, including the ’481 patent. *Id.* at 20–21, 25–26.

Patent Owner advances several theories supporting its privity arguments, including that Petitioner serves as an “agent” of Licensees by exercising their “have made” rights under the license, that Petitioner is a beneficiary of the Licensee’s agreements related to accused products, that Petitioner and Licensees “are ‘preceding and succeeding owners of’ the licensed and/or infringing products,” that Petitioner’s licensed sales encumber otherwise infringing articles, and “Petitioners apparently indemnify the time-barred parties” for custom-made products. Prelim. Resp. 18–39.

1. Legal Standard

Patent Owner does not assert that Petitioner was a party to, or named as a real party-in-interest in, any prior lawsuit involving the ’481 patent. “A person who is not a party to a suit generally has not had a ‘full and fair opportunity to litigate’ the claims and issues settled in that suit.” *Taylor v. Sturgell*, 553 U.S. 880, 892 (2008). Thus, in general, Petitioner should not be precluded from addressing the unpatentability of a patent based on the filing of previous lawsuits involving [REDACTED] *See id.* (explaining that, in general, one is not bound by a judgment “in which he is not designated as a party or to which he has not been made a party by

service of process”); *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319 (Fed. Cir. 2018) (noting the “general rule against nonparty preclusion”). This rule is deeply rooted in the “historic tradition that everyone should have his own day in court.” *Taylor*, 553 U.S. at 892–93 (quoting *Richards v. Jefferson County*, 517 U.S. 793, 798 (1996)).

An exception to this deeply-rooted rule exists for parties that are in privity with a defendant in an earlier litigation. *See WesternGeco*, 889 F.3d at 1319 (noting that “the standards for the privity inquiry must be grounded in due process”). The Supreme Court in *Taylor* identified considerations where nonparty preclusion would be justified, including:

- (1) an agreement to be bound; (2) pre-existing substantive legal relationships between the person to be bound and a party to the judgment (e.g., “preceding and succeeding owners of property”); (3) adequate representation by someone with the same interests who was a party (e.g., “class actions” and “suits brought by trustees, guardians, and other fiduciaries”); (4) assumption of control over the litigation in which the judgment was rendered; (5) where the nonparty to an earlier litigation acts as a proxy for the named party to relitigate the same issues; and (6) a special statutory scheme expressly foreclosing successive litigation by nonlitigants.

Id. (citing *Taylor*, 553 U.S. at 894–95).

As this list of considerations indicates, “the mere existence of some relationship between a petitioner and another entity is not sufficient” to place that petitioner in privity with that entity. *Google LLC v. DDC Technology, LLC*, IPR2023-00707, Paper 27 at 37 (PTAB Oct. 25, 2023). Instead, “that relationship must be related to [an earlier] lawsuit and be sufficiently close that it can be fairly said the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit,” or the evidence must demonstrate “that petitioner is simply serving as a proxy to allow another

party to litigate the patent validity question that the other party raised in an earlier filed litigation.” *Id.*; *WesternGeco*, 889 F.3d at 1319; *see also Ventex Co. v. Columbia Sportswear North America, Inc.*, IPR2017-00651, Paper 148, at 10, 12 (PTAB Jan. 24, 2019) (precedential) (finding privity where the two parties “had a specially structured, preexisting, and well-established business relationship with one another, including indemnification and exclusivity arrangements”).

A petitioner’s “initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner.” *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1244 (Fed. Cir. 2018). In order to raise such a dispute, “a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privity].” *Id.* The amount of evidence a patent owner must produce does not rise to the level of that required to overcome a burden of production. *Id.* at 1244 n.8. One potential formulation of the amount of evidence required is “evidence that ‘reasonably brings into question the accuracy of a petitioner’s’” assertion that it is not time-barred. *Id.* (quoting *Atlanta Gas Light v. Bennett Regulator Guards, Inc.*, IPR2013-00453, Paper 88 (PTAB Jan. 6, 2015) (addressing the amount of evidence required from a patent owner to question a petitioner’s identification of the real parties-in-interest)). Although the “burden remains with the petitioner to establish” the timeliness of its petition, it need not respond until the patent owner reasonably brings into question the accuracy of its assertion that it is not time-barred. *Id.* at 1242.

2. *The Effect of the Earlier Suit Against [REDACTED] on
the Timeliness of the Present Petition*

Patent Owner alleges that three non-parties, [REDACTED] [REDACTED] [REDACTED] are time-barred under § 315(b). Prelim. Resp. 18–39.

As to [REDACTED] the present record does not contain any evidence tending to show that this is the case. There is no evidence, on the present record, that [REDACTED] was served with a complaint any earlier than [REDACTED], which is less than one year before the filing of the Petition on December 11, 2023. *Compare* Pet. 81, with Ex. 2019 (cited at Prelim. Resp. 19). Accordingly, the service of an infringement complaint on [REDACTED] does not, on the present record, render [REDACTED] time-barred under § 315(b).⁹

Patent Owner argues that because [REDACTED] [REDACTED] were served with an infringement complaint early enough to create a time bar, and because [REDACTED] was a real party-in-interest of [REDACTED] in that infringement case, [REDACTED] is time-barred under § 315(b). Prelim. Resp. 18–19 (arguing that [REDACTED] is time-barred because it was a real party-in-interest to the [REDACTED] litigation). We are presented with no authority, however, for extending Section 315(b)’s time bar alleged to bar [REDACTED] as a real party in interest to [REDACTED] in the [REDACTED] litigation to further bar Petitioner in this proceeding as a conjectured privity of Petitioner. Thus, Patent Owner has produced no evidence that [REDACTED] is a time-barred entity under § 315(b).

⁹ In the next section, we address Patent Owner’s argument that [REDACTED] [REDACTED] and [REDACTED] are privies of Petitioner. Our findings as to [REDACTED] regarding privity provide additional support for our determination that service of a complaint against [REDACTED] does not give rise to a time bar.

3. Licensees as Alleged Privies

In the subsections below, we address Patent Owner’s arguments that Licensees are privies of Petitioner under § 315(b).

a) Agency

Patent Owner argues that Petitioner acts as the Licensees’ “agent” by making accused products on their behalf under the “have made” clause of the license. Prelim. Resp. 36–37. We disagree.

First, Patent Owner’s agency argument is not based on the applicable legal standard. For purposes of privity under § 315(b), the relevant question is whether Petitioner is acting as an agent for [REDACTED] or [REDACTED] in filing a petition for *inter partes* review. *See Taylor*, 553 U.S. at 895 (“preclusion is appropriate when a nonparty later brings suit as an agent for a party who is bound by a judgment”). As the Federal Circuit explains, the rationale behind § 315(b)’s time bar is “to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation.” *WesternGeco*, 889 F.3d at 1319. Here, Patent Owner does not assert that Petitioner is acting as an agent for [REDACTED] or [REDACTED] in this proceeding. Any such assertion would be appropriate only based on evidence that any of these entities is controlling Petitioner’s conduct in the proceeding. *See Taylor*, 553 U.S. at 906 (cautioning that “preclusion is appropriate only if the putative agent’s conduct of the suit is subject to the control of the party who is bound by the prior adjudication”). No such evidence is in this record.

Patent Owner argues that to be in privity with the Licensees, what matters is whether prior action concerned a matter within the agency. Prelim. Resp. 36 (citing *Herrion v. Children’s Hosp. Nat. Med. Ctr.*, 786 F. Supp. 2d 359 (D.D.C.), *aff’d*, 448 F. App’x 71 (D.C. Cir. 2011); *John Street*

Leasehold, LLC v. Cap. Mgmt. Res., L.P., 283 F.3d 73 (2d Cir. 2002); *Fiumara v. Fireman's Fund Ins. Companies*, 746 F.2d 87 (1st Cir. 1984)). This conclusion, however, would significantly expand the analysis set forth in *Taylor*, which noted that preclusion is only appropriate if the putative agent's conduct "is subject to the control of the party who is bound by the prior adjudication." *Taylor*, 553 U.S. at 906 (explaining that "courts should be cautious about finding preclusion" on the basis of agency). Moreover, the privity inquiry must take into account the rationale behind the preclusion provision in § 315(b), which "is to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation." *WesternGeco*, 889 F.3d at 1319. Patent Owner's broad interpretation would be inconsistent with this purpose.

Even if Patent Owner's argument that a general agency relationship is sufficient to demonstrate privity for purposes of nonparty preclusion were on solid legal footing, it lacks factual support in the record. An "essential element[] of agency" is "the principal's 'right to direct or control the agent's actions.'" *In re Google LLC*, 949 F.3d 1338, 1345 (Fed. Cir. 2020) (quoting *Meyer v. Holley*, 537 U.S. 280, 286 (2003)). Patent Owner does not argue in the Preliminary Response that [REDACTED], [REDACTED] [REDACTED] has or had such a right with respect to Petitioner, or vice versa, much less direct us to any evidence that would tend to prove the existence of such a right. *See generally* Prelim. Resp.

b) Preceding and Succeeding Owners of Property

Patent Owner argues that Petitioner and [REDACTED] [REDACTED] [REDACTED] are "preceding and succeeding owners" of "licensed and/or infringing products that Petitioner makes and supplies to Licensees." Prelim. Resp. 29 (citing *Taylor*, 553 U.S. at 894). It is true that entities who are "preceding and

succeeding owners of property” can be in privity with one another. *Taylor*, 553 U.S. at 894. This rule, however, is based on property law and “is extended or denied in an effort to protect conflicting property interests rather than an effort to implement concepts of participation or representation.” 18A C. Wright, A. Miller, & E. Cooper, Federal Practice and Procedure § 4448 (3d. ed. 2023); *see also id.* at § 4462 (“Successive Property Relationships”) (“There is no independent reason to treat the defeated litigant as the representative of his transferee. Preclusion is limited to the property involved in the judgment.”). As noted above, our relevant analysis is based on the relationships between the parties with respect to the prior proceedings or the Petition (e.g., participation or representation), not on property interests. *See WesternGeco*, 889 F.3d at 1319 (noting that the privity requirement is used “to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation”).

Moreover, the rule related to preceding and succeeding owners of property does not extend to the point where all manufacturers of allegedly infringing goods are in privity with the customers who buy those goods. *See, e.g., id.* at 1319–22 (the parties “had a contractual and fairly standard customer-manufacturer relationship regarding the accused product,” which “does not necessarily suggest that the relationship is sufficiently close that both” parties should be considered to be in privity); *Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1340–41 (Fed. Cir. 2018) (same); *Samsung Electronics Co. v. Netlist Inc.*, IPR2022-00615, Paper 64 at 22–26 (PTAB June 30, 2023) (same).

Patent Owner’s evidence that Petitioner’s products are components of Licensees’ products does not come close to suggesting that “it can be fairly

said that the petitioner had a full and fair opportunity to litigate the validity of the patent” in the prior lawsuit, or that or that petitioner is serving as a proxy to allow any Licensee to again challenge the patent. *WesternGeco*, 889 F.3d at 1319. Thus, Patent Owner does not present evidence that lends support to a finding that Petitioner’s and Licensees’ status as preceding and succeeding owners of allegedly infringing products renders them privies for purposes of § 315(b).

c) Beneficiaries of License Agreement

Patent Owner argues that Petitioner and Licensees are privies because Petitioner is a “beneficiary” of Patent Owner’s licenses to [REDACTED] and [REDACTED], which Patent Owner asserts are “directly related to” the accused products. Prelim. Resp. 32–33 (citing *Ventex*, IPR2017-00651, Paper 148). We disagree. Unlike the agreements in *Ventex*, Paper 148 at 12, Patent Owner’s licenses to Licensees are not evidence of a privity relationship between Petitioner and Licensees because Petitioner is not a party to the license agreements. Nor is there any argument that Petitioner is a third-party beneficiary of the licenses.

d) Patent Exhaustion

Patent Owner argues that the doctrine of patent exhaustion gives rise to privity because “after Petitioner sells products under the license, any downstream user of the article sold would have an exhaustion defense against [Patent Owner].” Prelim. Resp. 33–34. According to Patent Owner, “Petitioner is effectively providing rights to third-parties under the license and, therefore, is in privity with Licensees.” *Id.* at 34. We disagree. It is true that downstream purchasers and users of Licensees’ products that incorporate products made by Petitioner may have a license (or exhaustion) defense against any claim of infringement by Patent Owner. The relevant

question, however, is ultimately whether the relationship between Petitioner and the Licensees is sufficiently close to justify denying Petitioner its day in court. *See Taylor*, 553 U.S. at 892. Patent Owner does not sufficiently explain why a license defense supports such a privity relationship between Petitioner and Licensees.

e) Indemnification

Patent Owner argues that Petitioner's indemnity obligations support a finding of privity between Petitioner and the Licensees. Prelim. Resp. 34–35. As evidence of this alleged indemnification obligation, Patent Owner argues that Petitioner indemnifies Licensees. *Id.* at 34. Patent Owner also directs us to the indemnification provisions found in Petitioner's "Standard Terms and Conditions of Sale" agreement. *Id.* (citing Ex. 2010, 3).

An agreement by a petitioner to indemnify a third party in an earlier infringement suit can give rise to a privity relationship between the petitioner and that third party. *Intel Corp. v. U.S. Int'l Trade Comm'n*, 946 F.2d 821, 839 (Fed. Cir. 1991).

With respect to the '481 patent, the evidence of record suggests that only [REDACTED] [REDACTED] are potentially time-barred. Petitioner's indemnification provisions are directed to specific products sold by it. Ex. 2010. To the extent that Petitioner's indemnification provisions could demonstrate a privity relationship sufficient to deny Petitioner its day in court, it must be with respect to a product it sold to [REDACTED] or [REDACTED]. The present record, however, does not identify any device or component of Petitioner that formed the basis for the previous infringement complaint against [REDACTED] or [REDACTED]. *See, e.g.,* Ex. 2018, 10–11 (identifying products [REDACTED] was accused of infringing before the district court); *see generally* Prelim. Resp. As such, we are not persuaded that the indemnification

provisions of Petitioner’s “standard sales agreement” are relevant to any relationship with [REDACTED] or [REDACTED]

f) Conclusion as to Timeliness of the Petition

As noted above, privity concerns “whether the petitioner and the prior litigant’s relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit,” or “whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation.” *WesternGeco*, 889 F.3d at 1319. A petitioner’s “initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner.” *Worlds*, 903 F.3d at 1244. In order to raise such a dispute, “a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privity].” *Id.* Here, Patent Owner argues that it has produced such evidence in several respects, but, on the present record, none of the evidence in question tends to show that any time-barred Licensee is a privy of Petitioner for purposes of § 315(b). As such, we find the evidence of record does not tend to suggest that Petitioner is time-barred under 35 U.S.C. § 315(b), or call into question Petitioner’s assertion that the Petition is timely-filed.

C. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995)

(citing *Custom Accessories, Inc. v. Jeffrey–Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed.Cir.1986)..

According to Petitioner,

[a] person of ordinary skill in the art (“POSITA”) for the ’481 Patent would have had a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Additional education might compensate for less experience, and vice-versa.

Pet. 6 (citing Ex. 1003 ¶47).

Patent Owner does not dispute Petition’s definition of level of ordinary skill. *See generally* Prelim. Resp.

For the purposes of this Decision, we adopt Petitioner’s proposal regarding the level of one of ordinary skill in the art. The level of ordinary skill in the art is also reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

D. Claim Construction

In *inter partes* review proceedings such as this one, we construe claims using the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b), as articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. *See* 37 C.F.R. § 42.100(b). Petitioner states that they do not believe any terms need to be construed and that they take no position regarding claim construction at this time. Pet. 6–7. Patent Owner does not dispute Petitioner’s assertions. *See generally* Prelim. Resp. At this stage of the proceeding, we determine that we do not need to expressly construe any other terms to resolve the parties’ disputes on the current record. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need

only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

E. Ground 1–Asserted Obviousness over Kawagoe

Petitioner argues that claims 1–9, 13–14, 16–27, and 31–36 would have been obvious in view of Kawagoe. Pet. 7–40. Patent Owner presents arguments for this ground. Prelim. Resp. 3–16. For the reasons that follow, at this stage of the proceeding, we are persuaded that Petitioner sufficiently demonstrates a reasonable likelihood that it would prevail in showing that at least independent claim 1 would have been obvious in view of Kawagoe.

1. Overview of Kawagoe (Ex. 1007)

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device using an epitaxial wafer, i.e., a semiconductor wafer having a semiconductor single crystal epitaxial layer grown over a polished semiconductor substrate. Ex. 1007, 1:13–27, 2:31–35. According to Kawagoe, “[t]he epitaxial wafer is advantageous in that it is excellent in suppressing the soft errors and resisting to the latchup,”¹⁰ as well as “drastically reduc[ing] the defect density of the gate insulating film” of a semiconductor integrated device. *Id.* at 1:33–40.

¹⁰ Petitioner submits Exhibit 1009 (Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Int’l Conf on VLSI Design, 429–434, IEEE 2008), which explains that “soft errors” are “random and not related to permanent hardware faults” and “[t]heir causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation),” including “alpha particles [that] are emitted when the nucleus of an unstable isotope decays to a lower energy state.” Ex. 1009, Abstract, 430. Dr. Blalock characterizes “latchup” as “a ‘short-circuit’ failure condition in poorly designed circuits.” Ex. 1003 ¶ 76.

Kawagoe discloses various “representative” processes, including processes in which the single crystal (epitaxial) layer contains an impurity of the same type and in the same concentration as the substrate body. Ex. 1007, 2:55–3:9. According to Kawagoe, the impurity concentration of the substrate body can be made higher than that of epitaxial layer “so that the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup.” *Id.* at 4:1–8. Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device including a step of forming a semiconductor region (well) extending below the epitaxial layer and having an impurity concentration that decreases with increasing depth below the epitaxial layer. *Id.* at 3:10–25. According to Kawagoe, the well can be used for forming a complementary Metal-Oxide-Semiconductor Field-Effect Transistor (“MOS.FET”) circuit. *Id.* at 3:32–38.

Kawagoe describes seven embodiments, including Embodiment 1 (Ex. 1007, 6:41–12:40, Figs. 1–8) and Embodiment 4 (*id.* at 14:46–19:64, Figs. 16–25). According to Embodiment 1, a semiconductor integrated circuit device includes semiconductor substrate body 2S, epitaxial layer 2E, and gettering layer 2G. *Id.* at 6:51–56, Fig. 1. Substrate body 2S and epitaxial layer 2E are doped with p-type impurity in equal concentrations. *Id.* at 6:60–7:3, 10:51–55, 11:12–16. Embodiment 1 includes n-channel MOS.FET (“nMOS”) 4N and p-channel MOS.FET (“pMOS”) 4P, the latter being formed in n-well 6, which is doped with n-type impurity and extends below the epitaxial layer. *Id.* at 8:46–52, 9:32–40, 11:18–24, 11:43–50, Figs. 1, 5, 7.

According to Embodiment 4, substrate body 2S and epitaxial layer 2E are doped with p-type impurity, and the impurity concentration of substrate body 2S is higher than that of epitaxial layer 2E “to improve the resistance

to the latchup.” Ex. 1007, 14:64–15:6, 15:13–17, 16:16–21, 19:59–63, Fig. 17. Embodiment 4 includes p-well 6*p* formed with nMOS 4N and n-well 6*n* formed with pMOS 4P. *Id.* at 15:26–40, 17:40–18:35, Figs. 16, 21–23. In Embodiment 4, the impurity concentration in p-well 6*p* and n-well 6*n* decreases with increasing depth below the epitaxial layer. *Id.* at 15:62–16:15, 17:55–61, Fig. 17. Kawagoe discloses that the concentration gradient reduces soft errors by attracting carriers (electrons) to the substrate and preventing them from entering the p-well. *Id.* at 16:2–11.

Petitioner relies on Kawagoe Figures 17 and 23, which are reproduced below, and which illustrate Embodiment 4 and its properties.

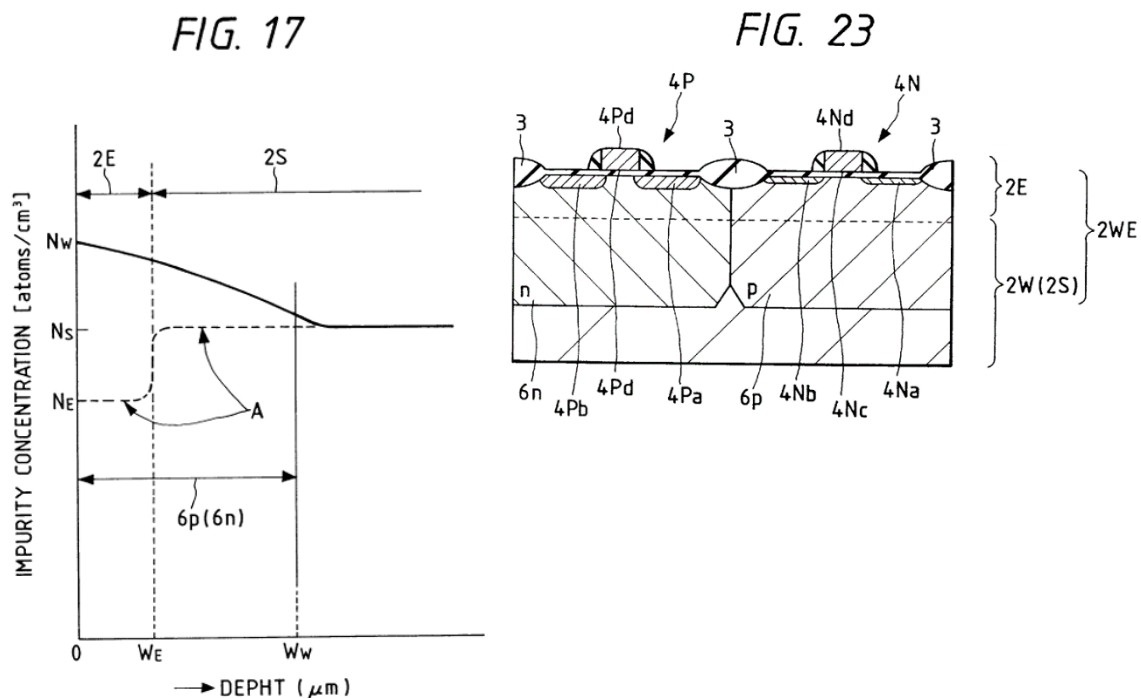


Figure 17 is a plot of impurity concentration as a function of depth in a semiconductor integrated circuit device, which shows “the p-well 6*p* and n-well 6*n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_w) of the epitaxial layer 2E.” Ex. 1007, 5:41–45,

15:62–16:40. Figure 23 shows a step in a process for manufacturing a semiconductor integrated circuit device, including p-well 6p formed with nMOS 4N and n-well 6n formed with pMOS 4P. *Id.* at 6:1–4, 15:26–32, 18:3–35.

2. Petitioner’s Initial Contentions for Claim 1

[preamble] A semiconductor device, comprising:

Petitioner contends that, “[t]o the extent it is limiting, Kawagoe discloses the preamble[] because Kawagoe is directed to a “semiconductor integrated circuit device,” and in particular, discloses a “CMOS (complementary metal-oxide semiconductor) device in Figure 23 (Embodiment 4), fabricated on a uniformly-doped epitaxial substrate taught in Embodiment 1.” Pet. 7–8 (citing Ex. 1007, code (54), 1:13–23, 14:46–67, Figs. 16–17, 23; Ex. 1003 ¶ 65; Pet. § VII.A.1.b); *see id.* at 8, n.4 (asserting that Figures 16–17 and 23 are directed to Kawagoe’s Embodiment 4).

[1.1] a substrate of a first doping type at a first doping level having first and second surfaces;

According to Petitioner, “Kawagoe discloses a substrate (‘semiconductor substrate 2’) of a first doping type (p-type) having a silicon ‘epitaxial layer 2E [] doped with a **p-type** impurity such as boron’ formed over non-epitaxial ‘semiconductor substrate body 2S [also] doped with a **p-type** impurity such as boron.’” Pet. 8 (citing Ex. 1007, 14:61–15:12, 6:50–7:3). In Petitioner’s annotated version of Kawagoe’s Figure 23, “[t]he substrate (orange) has top (‘first surface’) and bottom ([‘]second surface’) surfaces, as shown below.” *Id.* at 9 (citing Ex. 1003 ¶ 66); *see id.* at 9–13.

Petitioner contends that “Kawagoe teaches an epitaxial substrate (2S+2E), illustrated in Figure 20, in which the non-epitaxial silicon substrate body (2S) is either doped at the same or higher level compared to the

epitaxial silicon layer (2E).” Pet. 10. According to Petitioner, “Embodiment 1 describes a uniformly-doped epitaxial substrate in which the ‘epitaxial layer 2E is doped . . . in a concentration *equal* to the [concentration] of the semiconductor substrate body 2S, e.g., 1.3×10^{15} atoms/cm³.” *Id.* (citing Ex. 1007, code (57) 6:60–7:3, 2:57–3:9). Petitioner also contends that “Embodiment 4 introduces an optional latchup-resistant substrate in which ‘the impurity concentration of the semiconductor substrate body 2S is made *higher* than that of the epitaxial layer 2E . . . *to improve* the resistance to latchup.” *Id.* (citing Ex. 1007, 15:13–17; Ex. 1003 ¶¶ 69–70).

[1.2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

Petitioner contends that “Kawagoe discloses ‘semiconductor regions 4Na and 4Nb . . . for forming the *source-drain regions* of the nMOS [n-channel transistor] 4N.’” Pet. 14 (citing Ex. 1007, 8:66–67, 3:30–37, 8:46–52, 14:46–55, 15:26–40). “Source-drain regions 4Na/4Nb (purple) form part of the claimed first active region, which also includes the channel region (light purple) between source-drain regions 4Na/4Nb and below insulating film 4Nc.” *Id.* (citing Ex. 1007, 8:66–67, 3:30–37, 8:46–65, 14:46–55, 15:26–40; Ex. 1003 ¶ 78; Ex. 1008B, 299–300 (“The top surface of the [substrate] body consists of *active* or *transistor* regions as well as *passive* or (*field*) regions. The *active regions* are those in which transistor action occurs; i.e., the *channel* and the heavily doped *source* and *drain* regions.”), Figs. 5-2, 6-8(c), Figs. 6–10; Ex. 1008C, Fig. 8-1(e)).

Petitioner contends that, “[a]s shown in Figure 23, nMOS transistor 4N is formed in the surface of the first active region, which is adjacent the

first surface of the substrate.” Pet. 14–15 (citing Ex. 1003 ¶ 78). Petitioner further contends that “[s]emiconductor regions 4Na and 4Nb are doped with an *n-type impurity*’ and thus have a second doping type (n-type) opposite in conductivity to the first doping type (p-type) of the substrate.” *Id.* at 15 (citing Ex. 1007, Fig. 23, 8:67–9:3, 14:46–55, 15:26–40; Ex. 1003 ¶ 78). “While Figure 23 illustrates an exemplary nMOS transistor 4N in the first active region, a POSITA would have understood that Kawagoe teaches forming multiple nMOS transistors in this region to minimize chip area, as good layout practice dictates.” *Id.* (citing Ex. 1003 ¶ 79; Ex. 1014, 1:52–54, 2:17–21); *see id.* at 15–17.

[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

Petitioner contends that “Kawagoe discloses ‘semiconductor regions 4Pa and 4Pb . . . for forming the source-drain regions of the pMOS [p-channel transistor] 4P.’” Pet. 17 (citing Ex. 1007, 3:35–37, 8:46–52, 9:41–48, 15:26–40). Petitioner further contends that “[s]ource-drain regions 4Pa/4Pb (green) are part of the claimed second active region, which also includes the channel region (light green) between them and below gate 4Pd.” *Id.* (citing Ex. 1007, 8:46–67, 9:41–46, 14:46–55, 15:26–40; Ex. 1008B, 299–301, Figs. 5-1, 5-2, 6-4; Pet. § VII.A.1.c; Ex. 1003 ¶ 82). According to Petitioner, “[a]s shown in Figure 23, pMOS transistor 4P is formed in the surface of the second active region (green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple).” *Id.* (citing Ex. 1007, 14:46–55; Ex. 1003 ¶ 82). “Adjacent active regions are separated by an isolation region (*e.g.*, insulating film 3).” *Id.* (citing Ex. 1008A, 818–20, Fig. 16-11(f); Ex. 1003 ¶ 83); *see id.* at 18–19.

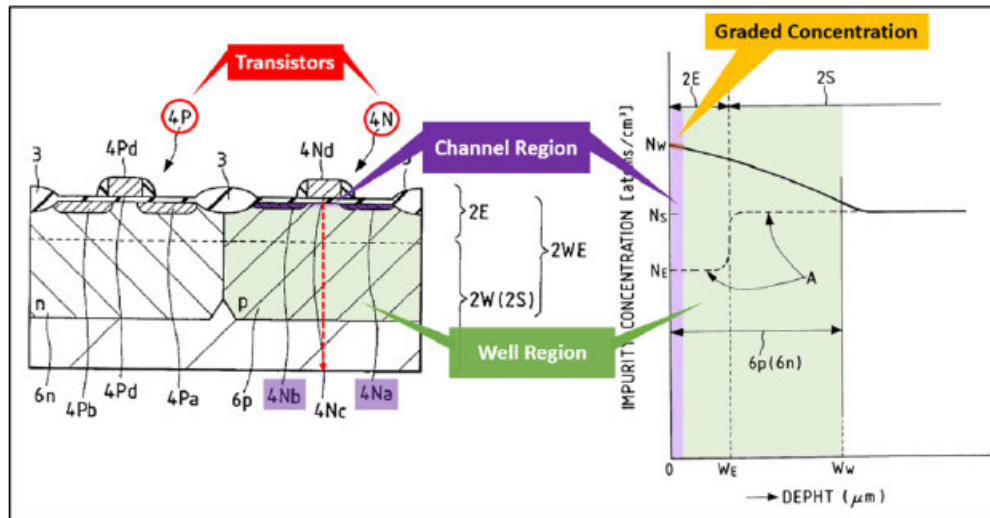
[1.4] transistors formed in at least one of the first active region or second active region;

Petitioner relies on its arguments for limitations 1.2 and 1.3 for teaching limitation 1.4. Pet. 19 (citing Pet. §§ VII.A.1.c–d; Ex. 1003 ¶ 86).

[1.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and

Petitioner contends that as illustrated in Figure 23, “a channel region (light purple) formed at the top surface of the substrate connects source-drain regions 4Na/4Nb (purple) of transistor 4N.” Pet. 19 (citing Ex. 1008B, 298 (“[a] channel region in the semiconductor under the gate electrode separates the source and drain”), 300–301 (“[w]hen positive bias is applied to an NMOS transistor gate . . . an *n*-type **channel** connects the **source** and **drain** regions”), Fig. 5-2; Ex. 1007, 8:60–67, 14:46–55, 15:26–30, 15:37–40; Ex. 1003 ¶ 87).

With respect to Petitioner’s annotated versions of Figures 23 and 17 reproduced below, Petitioner further contends that “Kawagoe’s Figure 17 . . . illustrates the doping concentration measured along the red dotted line in Figure 23 . . . which starts from the top surface of the substrate (depth=0) and includes the doping profile in the channel region (light purple).” *Id.* at 20 (citing Figs. 17, 23, 5:41–45).



Petitioner's annotated versions of Kawagoe's
 Figures 17 and 23. Pet. 20.

Petitioner further contends that, as the annotated version of “Figure 17 shows, the dopant concentration is ‘gradually lowered in the depthwise direction *from the principal surface* (having an impurity concentration N_w) of the epitaxial layer 2E.’” *Id.* (citing Ex. 1007, 5:41–45, 15:62–16:40). Citing Dr. Blalock’s testimony, Petitioner contends that “[t]he dopant concentration is thus graded in the channel region of transistor 4N, which is a portion of the first active region formed at ‘the principal surface’ of epitaxial layer 2E.” *Id.* (citing Ex. 1003 ¶ 88). Petitioner points to the prosecution history of the ’481 patent and argues that “the Examiner noted that ‘directional movement by doping gradient,’ like the claimed ‘aiding of carrier movement [] “from the first surface to the second surface of the substrate,”’ was ‘known in the art.’” Pet. 22 (citing Ex. 1002, 82; Ex. 1003 ¶ 44).

According to Petitioner,

Kawagoe further explains that such downward-sloping graded dopant concentrations aid the movement of carriers from the top

surface of the epitaxial layer (claimed “first surface”) to the bottom surface of the substrate (claimed “second surface”):

[T]he impurity concentration of the p-well 6p is given such a gradient that it is ***gradually lowered in the depthwise direction from the surface*** of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered. Specifically, the ***electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient*** ... so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p.

Id. at 22 (citing Ex. 1007, 16:2–11); *see id.* at 23, n.9 (“Kawagoe states that ‘electrons produced by the α -ray [are] . . . prevented from entering the p-well 6p’ This refers to electrons produced in the large substrate body below the wells.”) (citing Ex. 1007, 16:7–9; Ex. 1003 ¶ 91; Ex. 1009, Fig. 2).

Petitioner further contends that “Dr. Blalock explains that during a so-called single event upset (SEU), an α -ray generates millions of carriers, some of which are produced in or near the active regions at the surface of the substrate.” *Id.* at 23 (citing Ex. 1003 ¶¶ 91–92; Ex. 1009, 431 (“A[n] [α -]particle can induce SEU when it strikes at the ***channel region*** of an off nMOS transistor.”), Fig. 2). Petitioner also contends that “Kawagoe teaches that those carriers are ‘attracted to the substrate body by [the] concentration gradient’ of the graded dopant concentration illustrated in Figure 17.” *Id.* (citing Ex. 1007, 16:2–11). Petitioner further contends that

Kawagoe’s Figure 17 shows that the dopant concentration is downward-sloping with increasing depth towards/to the bottom of the substrate. . . . Applicant represented to Patent Office during prosecution of the parent ’195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an “inherent ‘built-in’ unidirectional electric field” that sweeps

carriers down into the substrate, as detailed below in [Petition]
§VII.A.1.g.

Id. at 23–24 (citing Ex. 1016, 289–290; Ex. 1003 ¶¶ 94–95).

[1.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

Petitioner contends that, as shown in its annotated version of Figure 23 . . . Kawagoe discloses ‘p-well 6p’ (light green) adjacent to the first active region (purple/light purple).” Pet. 24 (citing Ex. 1007, 8:66–67, 14:46–55, 15:26–40; Ex. 1003 ¶ 96). Petitioner further contends that “as shown in the dopant concentration profile (brown) of Figure 17 . . . the dopant concentration in p-well 6p—measured along the exemplary red dotted line in Figure 23—gradually decreases with depth.” *Id.* (citing Pet. § VII.A.1.f; Ex. 1007, 14:46–55, 15:62–16:40 (“p-well 6p and n-well 6n have their impurity concentrations *gradually lowered* in the depthwise direction from the principal surface (having an impurity concentration N_w) of the epitaxial layer 2E”), 16:11–15). Thus, according to Petitioner, “Kawagoe discloses a well region containing at least one graded dopant region (*e.g.*, the region highlighted in light green in both [Petitioner’s annotated version of] Figures 23 and 17) having a downward-sloping graded dopant concentration.” *Id.* at 25 (citing Ex. 1003 ¶ 97); *see id.* at 26–29.

3. Patent Owner’s Arguments for Claim 1

Patent Owner argues that the asserted references do not teach “at least one graded dopant concentration to aid carrier movement” as recited in claim 1 or a “graded dopant region to aid carrier movement” as recited in claim 20. Prelim. Resp. 3. According to Patent Owner:

Defendants assert that the specification does not provide guidance on how to assess or measure carrier movement. This is not true. The claims and the specification make clear that the electric field must move the carriers in a particular direction (from the surface layer to the substrate). *Whether the carrier movement has a particular speed or acceleration is beyond the scope of the claim*, as long as it meets the other limitations of the claim.

Id. at 4 (quoting Ex. 1020, 38) (emphasis added). With respect to the prosecution history statement cited by Petitioner—that “a downward-sloping graded dopant concentration was known in the prior art to create an ‘inherent “built-in” unidirectional electric field’ that sweeps carriers down,”—Patent Owner asserts that Petitioner’s quotation of this statement is incomplete. *Id.* (citing Ex. 1016, 286, 289). Patent Owner takes the position that it also argued “that the movement of carriers ‘[d]epend[s] on the particular slope of the graded concentration of dopant[s]’” and this statement was made in response “to an Office Action regarding a claim that required a ‘single static unidirectional electric drift field to aid the movement of carriers.’” *Id.*

Pointing to the Examiner’s findings during prosecution of the ’195 parent patent,¹¹ Patent Owner contends that Dr. Blalock examined only the direction of the slope and “did not look at the magnitude of the slope or other possible forces acting on a carrier.” Prelim. Resp. 10–11 (citing Ex. 2058, 91–92, 191–192). Patent Owner asserts that “the mere direction of

¹¹ Patent Owner contends that “during prosecution, the examiner said that in ‘a complex electronic device, movement of minority carriers is affected by multiple forces and fields’ and that a ‘drift field may attempt to apply a force on all minority carriers in a specific direction’ but that ‘without knowing other parameters of the device’ one cannot say whether the field would aid carrier movement.” Prelim. Resp. 6 (citing Ex. 1016, 270).

the gradient is *not* sufficient to determine whether there is a ‘net force.’” *Id.* at 11. According to Patent Owner, Kawagoe teaches the following:

Specifically, the electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p.

Id. at 12–13 (quoting Ex. 1007, 16:7–11 (emphases omitted)). In view of this disclosure, Patent Owner contends that Kawagoe teaches inhibiting carrier movement, not aiding carrier movement. *Id.* at 13. According to Patent Owner, Dr. Blalock admitted “that, according to Kawagoe, SEUs generate ‘electrons produced in the large substrate body below the wells’—far below the active regions.” *Id.* at 14 (citing Ex. 1003 ¶ 91 n.7). Patent Owner further contends that “Kawagoe does not address carriers in the ‘active region’” and “does not ‘aid carrier movement *from the first surface*’ because Kawagoe’s carriers are nowhere near what Petitioner identifies as the ‘first surface.’” *Id.* at 15.

According to Patent Owner, Dr. Blalock’s testimony cites Wang et al., *Single Event Upset: An Embedded Tutorial*, 21st International Conference on VLSI Design, IEEE 2008 (Ex. 1009, “Wang”), “a document whose public availability Petitioner has not established” and has a publication date of 2008, which is four years after the ’481 patent’s earliest possible priority date of September 3, 2004. *Id.* at 15 (citing Ex. 1003 ¶ 92; Pet. viii; Ex. 1009, 429). Even setting aside the potential issues of public availability and contemporaneity, Patent Owner asserts that Wang does not provide one of ordinary skill in the art “a reason to use Kawagoe in the active region” because Wang also indicates that carriers “are primarily generated deep in the device.” *Id.* at 16. According to Patent Owner, “Wang shows some

carriers in the active region, but never says that they are known to be a problem.” *Id.* (emphasis omitted).

During prosecution of the ’195 parent patent, the Examiner rejected claims under the pre-AIA version of 35 U.S.C. § 112, first paragraph and found that “movement of minority carriers is affected by multiple forces and fields” and that “it does not appear that simply the presence of ‘a unidirectional drift field’ in itself can achieve ‘drawing *all* minority carriers from said surface layer to said substrate.’” Ex. 1016, 289 (emphasis added). Patent Owner responded with following argument:

[A] unidirectional drift (electric) field necessarily affects all the present minority carriers in the same way - moving all minority carriers in the same direction because of the unidirectional drift due to the existence of the electric field. *See* “Physics and Technology of Semiconductor Devices,” A.S. Grove, pp. 224–225, John Wiley and Sons, Inc., New York, 1st Edition 1967 (“This same electric field will then be of such direction as to aid the motion of injected holes. Thus the injected minority carriers will now move not only by diffusion but also by drift due to the existence of this electric field.”). Depending on the particular slope of the graded concentration of dopant, all minority carriers are either swept “down” (from the surface layer to the substrate) or “up” (from the substrate to the surface layer). *See* Applicant’s Figs. 5(b) and 5(c).

Id. Patent Owner further argued that the Examiner’s finding

appears to not consider that the graded dopant concentration itself creates a “built-in” electrical field that forces the movement of carriers into a particular direction, whereby the “direction” of the electrical field and the resulting direction of the carrier movement depends *solely* on the slope of the graded concentration of dopant. With regard to the existence of a “built-in” electric field created by a graded dopant density, . . . *this inherent “built-in” unidirectional electric field is the additional parameter for ensuring that all minority carriers are being*

moved in one direction and which parameter the Office Action deemed to be missing from the disclosure.

Id. at 289–90 (emphases added). Also, “without conceding its position on this issue,” Patent Owner amended claims to eliminate reference to “*all* carriers” and instead, refer to “carriers.”¹² *Id.* at 290.

4. *Analysis of Claim 1*

At this stage of the proceeding, we determine that the statements made by Patent Owner during prosecution of the ’195 parent patent contradict its arguments in the present proceeding. *See generally* Prelim. Resp. Based on the present record, Patent Owner’s statements during prosecution support a preliminary finding that a graded dopant concentration is enough to teach aiding carrier movement in a particular direction. Patent Owner does not dispute that Kawagoe has a graded dopant concentration in the active region at this stage of the proceeding. *See generally* Prelim. Resp; Prelim. Sur-reply. Patent Owner also does not dispute that Kawagoe’s transistor has carriers in the active region. *See, e.g.*, Prelim. Sur-reply 6.

As to Patent Owner’s argument that Kawagoe does not disclose aiding the movement of carriers, but rather inhibiting carrier movement (*see* Prelim. Resp. 6, 12–13; Ex. 1007, 16:7–11), Petitioner responds that “the electric field in Kawagoe **both** helps carriers move from the active regions to the substrate (as in the challenged claims), **and** prevents carriers moving from the substrate to the p-well (as called out in Kawagoe). Prelim. Reply 6–

¹² The examined claims of the ’195 patent generally recited “a unidirectional drift field drawing all minority carriers from said surface layer to said substrate.” Ex. 1016, 286. Patent Owner amended the claims of the ’195 patent to recite “maintain[ing] a single static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.” *Id.*

7; *see also* Pet. 23 n.9. Petitioner presents testimony from Dr. Blalock in support of this position. *Id.* at 6 (citing Ex. 2058, 150:11–151:3).

Additionally, Petitioner contends that “[f]or a semiconductor device as in Kawagoe to operate, there must be carriers in the active region,” and as such, “the electric field from Kawagoe’s graded concentration would impact carriers both in the substrate and anywhere in the graded dopant region.” *Id.* at 7.

At this stage of the proceeding, Petitioner has the better position. The parties, however, are invited to further develop the evidence and arguments relevant to the above-identified issues during the course of this proceeding.

5. *Remaining Claims*

Petitioner relies on its showing for independent claim 1 to teach the limitations recited in independent claim 20. *See* Pet. 7–29. Petitioner also identifies where it contends the subject matter of dependent claims 2–9, 13–14, 16–19, 21–27, and 31–36 is disclosed in Kawagoe. *Id.* at 29–40.

In view of our determination that Petitioner establishes a reasonable likelihood for claim 1, and because Petitioner’s arguments and evidence for remaining claims 2–9, 13–14, 16–19, 20–27, and 31–36 (Pet. 29–40) are similar to Petitioner’s arguments and evidence for claim 1 (*id.* at 7–29) and are unopposed at this stage by Patent Owner (except for the issues discussed above with respect to independent claims 1 and 20), we determine that it is unnecessary to provide an explicit analysis of Petitioner’s challenges to the remaining claims in order to provide guidance to the parties for the upcoming trial. Consolidated Trial Practice Guide November 2019 (“CTPG”)¹³ at 64; *see* 37 C.F.R. § 42.108(a) (“When instituting *inter partes*

¹³ Available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”); *see SAS*, 138 S. Ct. at 1359–60 (holding that 35 U.S.C. § 314 forbids the Board’s prior “partial institution” practice).

F. Ground 2—Asserted Obviousness over Wieczorek and Wolf

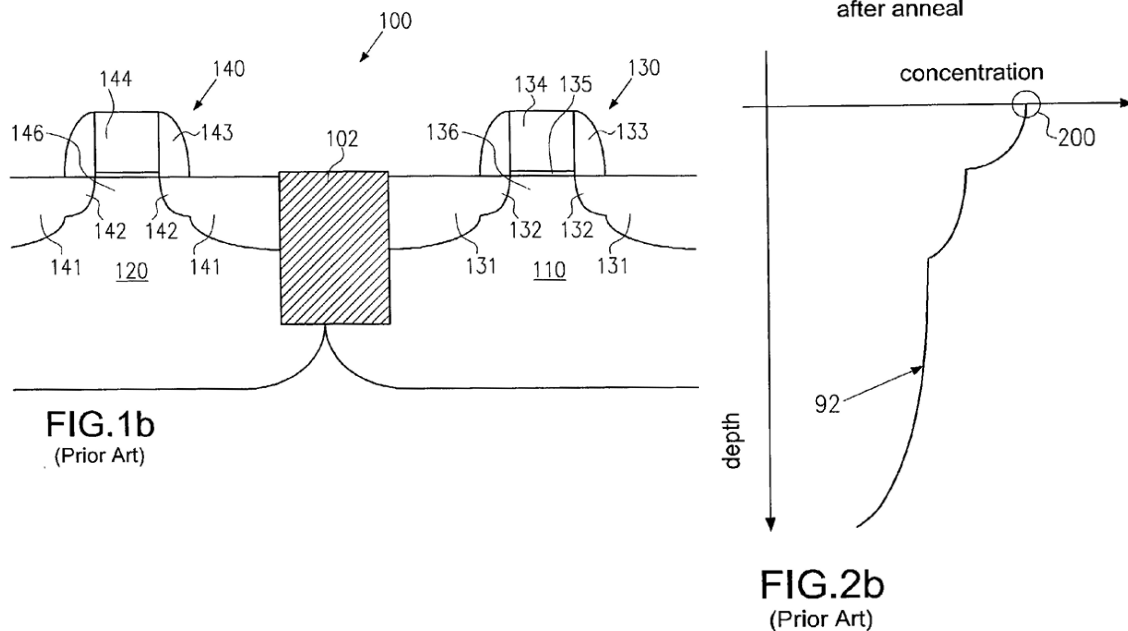
Petitioner argues that claims 1, 2, 4–9, 13–22, 24–27, 31–36 would have been obvious in view of Wieczorek and Wolf. Pet. 6, 40–71. Patent Owner does not present arguments for this ground. *See generally* Prelim. Resp. For the reasons that follow, at this stage of the proceeding, we are persuaded that Petitioner sufficiently demonstrates that at least independent claim 1 would have been obvious in view of Wieczorek and Wolf.

1. Overview of Wieczorek (Ex. 1006)

Wieczorek relates “to a semiconductor device, such as a field-effect transistor, having an improved retrograde dopant profile in a channel region of the transistor element.” Ex. 1006 ¶ 2. The Petition relies on Wieczorek’s description of the prior art, not its disclosed improvement. Pet. 40.

Wieczorek explains that a retrograde channel dopant profile is one where “the concentration of dopants increases from the gate insulation layer to the areas located deeper down the channel region.” Ex. 1006 ¶ 6. According to Wieczorek, a retrograde channel dopant profile is desirable, but “very difficult to obtain.” *Id.* Wieczorek states that “the dopant concentration immediately after the implantation process exhibits a desired retrograde dopant profile” (*id.* ¶ 9), but during heat treatment, “the initially retrograde profile in the vicinity of the surface of the semiconductor device . . . may have become substantially uniformly distributed” due to diffusion of the dopant atoms (*id.* ¶ 11).

Petitioner relies on Figures 1b and 2b, reproduced below, which Wieczorek uses to illustrate the prior art.



Wieczorek Figure 1b shows a conventional semiconductor device at an advanced manufacturing stage, including shallow trench isolation 102 separating N-well structure 120 from P-well structure 110. Ex. 1006 ¶¶ 7, 12, 20. The device includes P-channel transistor 140 with source and drain regions 141 in N-well structure 120 and N-channel transistor 130 with source and drain regions 131 in P-well structure 110. *Id.* ¶ 12. Wiecezorek Figure 2b is a graph of dopant concentration versus depth of N-well structure 120 and P-well structure 110 and shows “a typical dopant profile with respect to the depth of the respective well structure” after ion implantation and heat treatment. *Id.* ¶¶ 9–11, 13, 21.

2. Overview of Wolf (Exs. 1008A–1008D)

Wolf is a four-volume textbook titled “Silicon Processing for the VLSI Era.” Ex. 1008. A portion of the textbook focuses on CMOS technology. Ex. 1008A, 807–840.

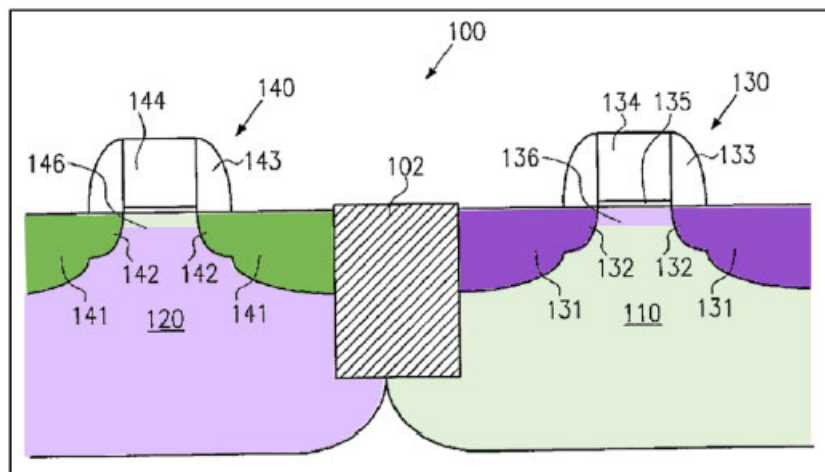
3. *Petitioner's Initial Contentions for Claim 1*

[preamble] A semiconductor device, comprising:

Petitioner contends that “[t]o the extent it is limiting, Wieczorek discloses the preamble because Wieczorek teaches a ‘semiconductor device.’” Pet. 41 (citing Ex. 1006, code (54), ¶¶ 2, 12; Ex. 1003 ¶ 129). Petitioner further contends that “Wieczorek’s Figure 1b illustrates a conventional twin-well CMOS semiconductor device.” Pet. 41 (citing Pet. § VII.B.1.b).

[1.1] a substrate of a first doping type at a first doping level having first and second surfaces;

Petitioner contends that its annotated version of “Wieczorek’s Figure 1b [reproduced below] illustrates a twin-well CMOS device, where N-channel transistor 130 (nMOS) with source/drain regions 131-132 (purple) and channel region 136 (light purple) is formed in P-well 110 (light green), and P-channel transistor 140 (pMOS) with source/drain regions 141-142 (green) and channel region 146 (light green) is formed in N-well 120 (light purple).” Pet. 42 (citing Ex. 1006 ¶¶ 7, 12, 20–21; Ex. 1008C, 525, Fig. 8-1(e); Ex. 1003 ¶ 130).



Petitioner’s annotated version of Wieczorek’s Fig. 1b. Pet. 43.

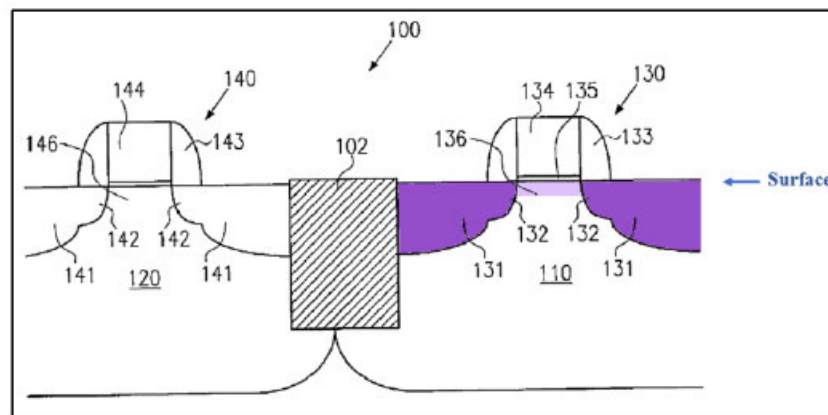
Petitioner contends that a “POSITA would have understood that a twin well approach ‘is independent of starting material type’ for the substrate.” *Id.* at 43 (citing Ex. 1008C, 524; Ex. 1006 ¶ 4; Ex. 1003 ¶ 131). According to Petitioner, “[b]ecause Wieczorek does not specify what constitutes an appropriate substrate, a POSITA would have been motivated to consult Wolf, which confirms that a ‘**uniform**, lightly doped *p*- or *n*-type substrate’ is commonly used in twin-well CMOS devices.” *Id.* (citing Ex. 1008C, 523, 530 (“With the twin-tub [(twin-well)] approach, two separate wells are formed for *n*- and *p*-channel transistors on a lightly doped substrate . . . of *n* or *p* material.”); Ex. 1008B, 387–389; Ex. 1003 ¶ 132). Petitioner contends that “[c]onsistent with Wieczorek’s teaching, a POSITA would have found it obvious to use a uniformly doped *n*- or *p*-type substrate (‘a substrate of a first doping type at a first doping level’) as a suitable substrate for Wieczorek’s CMOS device in Figure 1b.” *Id.* at 44 (citing Ex. 1003 ¶ 133).

Petitioner contends that combining Wieczorek and Wolf would amount to combining known prior art elements (*i.e.*, use of a uniform, lightly doped *n*- or *p*-type substrate with Wieczorek’s process for forming a conventional CMOS device) according to known methods (*i.e.*, known use of an “appropriate substrate” for the conventional process of forming the CMOS device in Wieczorek [0007]-[0013]) to obtain predictable results (*i.e.*, conventional CMOS device in Wieczorek’s Figure 1b). EX1003, ¶133. Doing so would have also been obvious to try because it involves nothing more than choosing one of a finite number of known appropriate substrates that are described by Wolf as suitable for use in forming a twin-well CMOS device like Wieczorek’s. *Id.* There would have been reasonable expectation of success because Wolf shows that a POSITA would have known how to use a uniformly doped *n*- or *p*-type substrate to form a twin-well CMOS device similarly as described in Wieczorek. *Id.*

Pet. 44–45.

[1.2] a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

Petitioner contends that “Wieczorek discloses ‘an N-channel transistor 130’ that includes ‘heavily N-doped **source and drain regions** 131, including lightly doped extensions 132,’ and ‘**channel region** 136.’” Pet. 46 (citing Ex. 1006 ¶¶ 4, 12, 13). Petitioner further contends “[t]he source-drain regions 131-132 (purple) form part of the claimed first active region, which also includes channel region 136 (light purple) between them.” *Id.* (citing Ex. 1006 ¶ 12; Ex. 1003 ¶ 136; Ex. 1008B, 299, 300, Figs. 5-2, 6-8(c), 6-10; Ex. 1008C, 525, Fig. 8-1(e)). Pointing to Petitioner’s annotated version of Wieczorek’s “Figure 1b [reproduced below], nMOS transistor 130 is formed in the surface of the first active region, which is adjacent the first surface of the substrate.” Pet. 47 (citing Ex. 1003 ¶ 136).



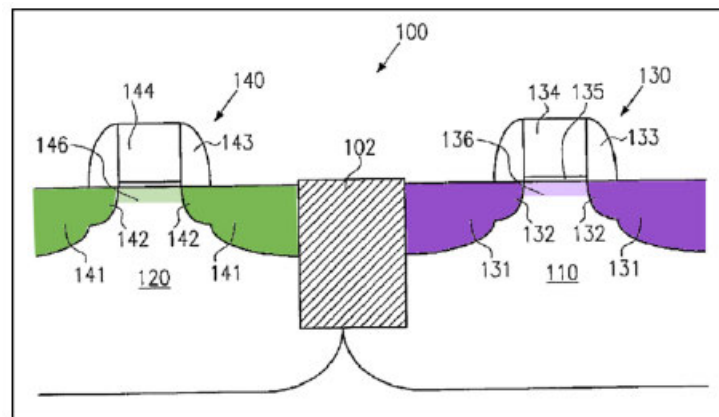
Petitioner’s annotated version Figure 1b of
Wieczorek. *Id.*

According to Petitioner, “[b]ecause the source-drain regions of the first active region are N-doped, Wieczorek-Wolf’s first active region has a second doping type (N-type) opposite in conductivity to the first doping type

(P-type) of the substrate.” *Id.* (citing Ex. 1006 ¶ 12; Ex. 1003 ¶ 137); *see id.* at 47–49.

[1.3] a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

Petitioner contends that “‘Wieczorek discloses “P-channel transistor 140,’ including ‘heavily P-doped source and drain regions 141, including lightly doped extensions 142,’ and ‘channel region 146.’” Pet. 49 (citing Ex. 1006 ¶¶ 4, 7, 12, 13; Ex. 1003 ¶ 141). “Source and drain regions 141-142 (green) are part of the claimed second active region, which also includes channel region 146 (light green) between them.” *Id.* (citing Ex. 1006 ¶ 12; Ex. 1008B, 298–301, Figs. 5-1, 5-2, 6-4; Pet. § VII.B.1.c; Ex. 1003 ¶ 141). Petitioner contends that as shown in its annotated version of Wieczorek’s Figure 1b reproduced below, “pMOS transistor 140 is formed in the surface of the second active region (green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple).” Pet. 49 (citing Ex. 1006 ¶ 12; Ex. 1003 ¶ 142).



Petitioner’s annotated version of Figure 1b of
Wieczorek. Pet. 50.

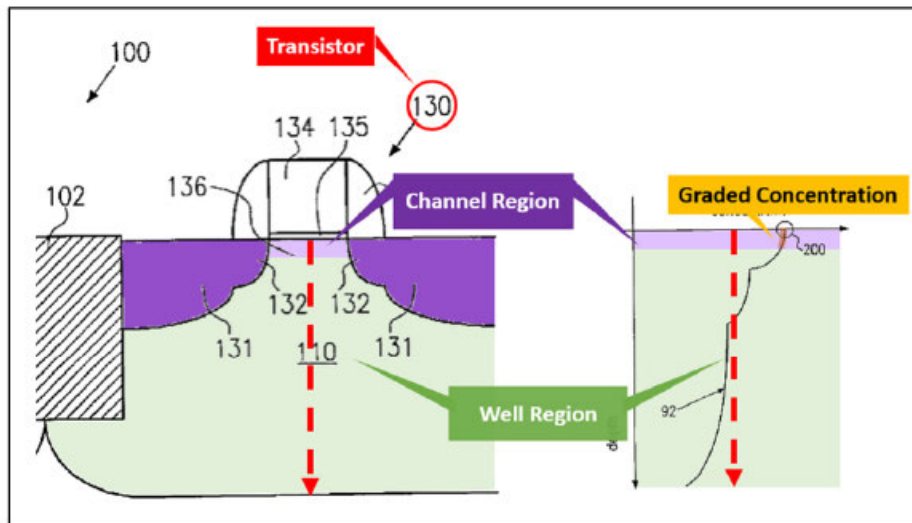
“Adjacent active regions are separated by an isolation region (*e.g.*, shallow trench isolation 102).” *Id.* (citing Ex. 1006 ¶ 7; Ex. 1008A, 818–20, Fig. 16-11(f); Ex. 1001, cl. 6, 26; Ex. 1003 ¶ 142; Pet. § VII.A.1.d).

[1.4] transistors formed in at least one of the first active region or second active region;

Petitioner relies on its arguments for limitations 1.2 and 1.3 for teaching limitation 1.4. Pet. 51 (citing Pet. §§ VII.B.c–d).

[1.5] at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and

Petitioner contends that, in Petitioner’s annotated versions of Wieczorek’s Figures 1b and 2b reproduced below, “channel region 136 (light purple) of nMOS transistor 130, formed at the top surface of the substrate, is a portion of the first active region. Pet. 51 (citing Ex. 1006 ¶¶ 4, 12, 13; Ex. 1008B, 298–301 (“The top surface of the [substrate] body consists of *active* or *transistor* regions as well as *passive* or (*field*) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source and drain*** regions.”), Fig. 5-2; Ex. 1003 ¶ 146).



Petitioner's annotated versions of Wieczorek's
Figures 1b and 2b. Pet. 52.

According to Petitioner, “[t]he doping concentration in the channel region is highlighted in brown in the doping profile of Figure 2b (above right), measured for example along the red dotted line in Figure 1b that traverses the channel region.” *Id.* (citing Ex. 1006 ¶¶ 9, 11, 13, Fig. 2a). Petitioner contends that, as its annotated version of Wieczorek's Figure 2b shows, “the dopant concentration is highest at the surface of the substrate and decreases with depth” and “[t]herefore, channel region 136 has a graded dopant concentration.” *Id.* (citing Ex. 1003 ¶ 147); *see id.* at 52–55.

Petitioner relies on the prosecution history of the '481 patent in substantially similar fashion as set forth above in Section III.E.2 with respect to Petitioner's first ground for challenge. Pet. 54–55.

[1.6] at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

Pointing to its annotated version of Figure 1b of Wieczorek, Petitioner contends that “Wieczorek discloses a ‘P-well structure 110’ (light green)

adjacent to the first active region (purple/light purple).” Pet. 56 (citing Ex. 1006 ¶¶ 12, 13; Ex. 1003 ¶ 154). Petitioner also contends that “the dopant concentration in P-well 110—measured along the exemplary red dotted line in Figure 1b—is gradually decreasing with depth.” *Id.* (citing Ex. 1006 ¶¶ 9, 11, 13; Ex. 1003 ¶ 154). Thus, according to Petitioner, “Wieczorek discloses a well region containing at least one graded dopant region (*e.g.*, the region highlighted in light green in both Figures 1b and 2b) having a downward-sloping graded dopant concentration.” *Id.* (citing Ex. 1003 ¶ 154; Ex. 1006, Figs. 1b, 2b).

4. Patent Owner’s Arguments for Claim 1

Pointing to Petitioner’s citation of Wieczorek’s Figure 2b with respect to the “graded dopant concentration” recited in claim 1, Patent Owner argues that Petitioner is again relying on Patent Owner’s alleged admissions made during prosecution of the ’195 parent patent. Prelim. Resp. 16–17 (citing Pet. 54–55). Patent Owner further contends that “Dr. Blalock admitted that he did not calculate the slope of the graded concentration curve in Wieczorek” and that “because the dopant gradient Petitioner points to in Figure 2[b] (and Wieczorek generally) does not have any values from which one could calculate a slope.” *Id.* at 17–18 (citing Ex. 2058, 191–192). As discussed above with respect to Kawagoe (*supra* § III.E.3), Patent Owner contends that a slope’s magnitude is essential “to determine the magnitude of the force the dopant gradient places on the carrier and thus the net force.” *Id.* at 18.

5. Analysis of Claim 1

For reasons substantially similar to those set forth above with respect to Kawagoe (*supra* § III.E.3), Patent Owner’s arguments are unavailing. At this stage of the proceeding, we do not agree that Dr. Blalock was required

to make any calculations to support a preliminary finding that Wieczorek's graded dopant concentration teaches "the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate" as recited in independent claim 1. As discussed above, Patent Owner's arguments contradict its statement made during prosecution of the '195 parent patent. At this stage of the proceeding, we disagree that Petitioner must make any additional showing beyond that of Wieczorek's graded dopant concentration, especially because Patent Owner also does not dispute that Wieczorek's transistor has carriers in the active region.

6. Remaining Claims

Petitioner relies on its showing for independent claim 1 to teach the limitations recited in independent claim 20. *See* Pet. 41–58. Petitioner argues that dependent claims 2, 4–9, 13–19, 21–22, 24–27, and 31–36 would have been obvious over Wieczorek and Wolf. Pet. 58–71.

In view of our determination that Petitioner establishes a reasonable likelihood for claim 1, and because Petitioner's arguments and evidence for remaining claims 2, 4–9, 13–19, 20–22, 24–27, and 31–36 (Pet. 58–71) are similar to Petitioner's arguments and evidence for claim 1 (*id.* at 41–58) and are unopposed at this stage by Patent Owner, we determine that it is unnecessary to provide an explicit analysis of Petitioner's challenges to the remaining claims. CTPG at 64; *see* 37 C.F.R. § 42.108(a); *SAS*, 138 S. Ct. at 1359–60.

G. Grounds 3 and 4—Asserted Obviousness over Kawagoe and Gupta and over Wieczorek, Wolf, and Gupta

Petitioner argues that claims 1–9, 13–14, 16–27, and 31–36 would have been obvious in view of Kawagoe in view of Gupta and that claims 1–2, 4–9, 13–22, 24–27, and 31–36 would have been obvious in view of

Wieczorek, Wolf, and Gupta. Pet. 6, 71–76. Patent Owner does not present separate arguments for these grounds besides those discussed above. *See generally* Prelim. Resp.

1. Overview of Gupta (Ex. 1014)

Gupta is entitled “Method and Apparatus for Optimizing Transistor Cell Layout with Integrated Transistor Folding.” Ex. 1014, code (54). Gupta “relates to the field of compl[e]mentary metal oxide semiconductor (CMOS) circuits, and more particularly to automatically producing layouts for CMOS circuits.” *Id.* at 1:7–10. Gupta explains that “[a]s semiconductor chips become ever larger, incorporating ever more devices, it becomes increasingly important to minimize semiconductor area used by a given number of devices.” *Id.* at 1:28–31. According to Gupta, doing so “potentially [saves] millions of dollars.” *Id.* at 1:31–34. To accomplish this goal, Gupta discloses abutting multiple transistors to “form transistor chains.” *Id.* at 2:17–21, Fig. 4.

2. Analysis

Petitioner asserts that grounds 3 and 4 “mirror” grounds 1 and 2, respectively, “except Gupta is explicitly combined with Kawagoe (Ground I) and Wieczorek-Wolf (Ground II) to render obvious elements under an interpretation of ‘transistors’ or ‘devices’ requiring a plurality of such devices.” Pet. 71 (citing Ex. 1003 ¶¶ 182–190); *see id.* at 71–76.

In view of our determination that Petitioner establishes a reasonable likelihood of showing unpatentability of claim 1 over Kawagoe and over Wieczorek and Wolf, we determine that it is unnecessary to provide an explicit analysis of Petitioner’s challenges to the remaining claims. CTPG at 64; *see* 37 C.F.R. § 42.108(a); *SAS*, 138 S. Ct. at 1359–60.

H. Grounds 5 and 6—Asserted Obviousness over Kawagoe and Silverbrook and over Wieczorek, Wolf, and Silverbrook

Petitioner argues that claims 19 and 36 would have been obvious in view of Kawagoe and Silverbrook and that claims 19 and 36 would have been obvious in view of Wieczorek, Wolf, and Silverbrook. Pet. 6, 76–77. Patent Owner does not present arguments for these grounds. *See generally* Prelim. Resp.

1. Overview of Silverbrook (Ex. 1046)

Silverbrook is entitled “Integrated Camera Circuit Including Image Sensor, Image Processing, and Printer Drive Circuits.” Ex. 1042, code (54). Silverbrook “relates substantially to the concept of a disposable camera having instant printing capabilities.” *Id.* at 1:8–9. Part of Silverbrook’s camera is an “Image Capture and Processing Chip” that performs “CMOS image sensing.” *Id.* at 6:41–49. The CMOS image sensing is accomplished by “a CMOS active pixel sensor array” manufactured using a “CMOS/DRAM/APS process.” *Id.* at 6:50–55.

2. Analysis

Petitioner contends that grounds 5 and 6 “mirror” grounds 1 and 2, respectively “except that Silverbrook is explicitly combined with Kawagoe of Ground I and Wieczorek-Wolf of Ground II to render obvious the implementation of the disclosed design in an image sensor.” Pet. 76. According to Petitioner, “[b]oth Kawagoe and Wieczorek-Wolf expressly disclose CMOS designs, and Silverbrook discloses use of a “CMOS image sensor.” *Id.* (citing Ex. 1042, 6:41–67).

In view of our determination that Petitioner establishes a reasonable likelihood of showing unpatentability of claim 1 over Kawagoe and over Wieczorek and Wolf, we determine that it is unnecessary to provide an

explicit analysis of Petitioner’s challenges to the remaining claims. CTPG at 64; *see* 37 C.F.R. § 42.108(a); *SAS*, 138 S. Ct. at 1359–60.

IV. CONCLUSION

After considering the evidence and arguments presented in the current record, we determine that Petitioner demonstrates a reasonable likelihood of success in proving that at least one of the challenged claims of the ’481 patent is unpatentable. We therefore institute trial on all challenged claims and grounds raised in the Petition. At this stage of the proceeding, we have not made a final determination as to the patentability of any challenged claim or as to the construction of any claim term. Any final determination will be based on the record developed during trial. We place Patent Owner on express notice that any argument not asserted in a timely-filed Response to the Petition, or in another manner permitted during trial, shall be deemed waived, even if that argument was presented in the Preliminary Response.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–9, 13–27, and 31–36 of the ’481 patent is instituted with respect to all grounds set forth in the Petition;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the ’481 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial;

FURTHER ORDERED that, in view of the pending motion to seal, this Decision is being filed “Board and Parties Only”; and

FURTHER ORDERED that after conferring with Petitioner, Patent Owner shall, within one week of this Decision, submit to the Board via

IPR2024-00264
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email to Trials@uspto.gov, a version of this Decision to be filed on the public record, with any redactions proposed by either party.

For PETITIONER:

Roger Fulghum
Mark Speegle
Ellyar Y. Barazesh
BAKER BOTTS L.L.P.
roger.fulghum@bakerbotts.com
mark.speegle@bakerbotts.com
ellyar.barazesh@bakerbotts.com

Daniel Anderson
ERNST, BROWN & DRAPER, PLLC
daniel.anderson@andersonpatents.com

For PATENT OWNER:

Alan Whitehurst
Nicholas Theodore Matich, IV
Arvind Jairam
Stuart McCommas
Archis “Neil” Ozarkar
MCKOOL SMITH, PC
awhitehurst@mckoolsmith.com
nmatich@mckoolsmith.com
ajairam@mckoolsmith.com
nozarkar@McKoolSmith.com