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Paper 34
Entered: February 21, 2024

PUBLIC VERSION

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

IPR2023-01243
Patent 10,510,842 B2

Before JON B. TORNQUIST, CHRISTOPHER M. KAISER, and ELIZABETH M. ROESEL, *Administrative Patent Judges.*

ROESEL, *Administrative Patent Judge.*

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

Semiconductor Components Industries, LLC ("Petitioner") filed a Petition (Paper 2, "Pet.") seeking an *inter partes* review of claims 1–18 of U.S. Patent No. 10,510,842 B2 (Ex. 1001, "the '842 Patent"). Greenthread, LLC ("Patent Owner") filed a Preliminary Response. Paper 17 ("Prelim. Resp."). With prior Board authorization, Petitioner filed a Preliminary Reply (Paper 21, "Prelim. Reply"), and Patent Owner filed a Preliminary Sur-reply (Paper 27, "Prelim. Sur-reply").

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). An *inter partes* review may not be instituted "unless . . . the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

After considering the parties' submissions, we determine that Petitioner shows the Petition is not time-barred under 35 U.S.C. § 315(b), and Petitioner also shows a reasonable likelihood that it would prevail in showing that at least one of the challenged claims is unpatentable. Therefore, we grant institution of an *inter partes* review.

Our findings and conclusions below are based on the record developed thus far. This is not a final decision as to the patentability of any challenged claim. Any final decision will be based on the full record developed during trial.

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B. Related Matters

Patent Owner states that it has asserted the '842 Patent in the following pending district court matters:

Greenthread, LLC v. Cirrus Logic, Inc., No. 1:23-cv-00369 (W.D. Tex. filed March 31, 2023);

Greenthread, LLC v Texas Instruments Inc., No. 2:23-cv-00157 (E.D. Tex. Filed April 6, 2023);

Greenthread, LLC v. OSRAM GmbH, No. 2:23-cv-00179 (E.D. Tex. filed April 19, 2023);

Greenthread, LLC v. ON Semiconductor Corp., No. 1:23-cv-00443 (D.Del. filed April 21, 2023);

Greenthread, LLC v. OmniVision Technologies, Inc., No. 2:23-cv-00212 (E.D. Tex. filed May 10, 2023); and

Greenthread, LLC v. Monolithic Power Systems, Inc., No. 1:23-cv-00579 (D. Del. filed May 26, 2023).

Paper 4, 2–3 (Patent Owner's mandatory notices).

The '842 Patent and related patents are being challenged by Cirrus Logic, Inc. in IPR2024-00001, IPR2024-00016, IPR2024-00017, IPR2024-00018, IPR2024-00019, IPR2024-00020, and IPR2024-00021, and related patents are being challenged by Petitioner in IPR2023-01242, IPR2023-01244, IPR2024-00263, IPR2024-00264, IPR2024-00265, and IPR2024-00266. *See* Paper 15, 2–3 (Patent Owner's updated mandatory notices listing related patents).

C. The '842 Patent (Ex. 1001)

The '842 Patent was issued December 17, 2019, and claims the benefit of a series of continuation applications, the earliest of which was

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filed September 3, 2004. Ex. 1001, codes (45), (22), (60). The '842 Patent is titled, "Semiconductor Devices with Graded Dopant Regions" and "relates to all semiconductor devices and systems." *Id.* at code (54), 1:32–33.

According to the '842 patent, in bipolar junction transistors, "[e]fforts have been made in graded base transistors to create an aiding drift field to enhance the diffusing minority carrier's speed from emitter to collector" versus the standard "uniformly doped base." Ex. 1001, 1:43–57. This improvement has not been implemented in "most semiconductor devices, including various power MOSFETs [and] IGBT's," which "still use a uniformly doped 'drift epitaxial' region in the base." *Id.* at 1:57–62. The invention of the '842 patent implements graded dopant concentration in these devices, which causes "[t]wo important performance enhancements." *Id.* at 3:12–39. These include sweeping electrons "from source to drain rapidly" and simultaneously causing holes to "be recombined closer to the n^+ buffer layer," which "can improve t_{on} and t_{off} in the same device." *Id.* at 3:39–43.

Figure 1 of the '842 Patent is reproduced below.

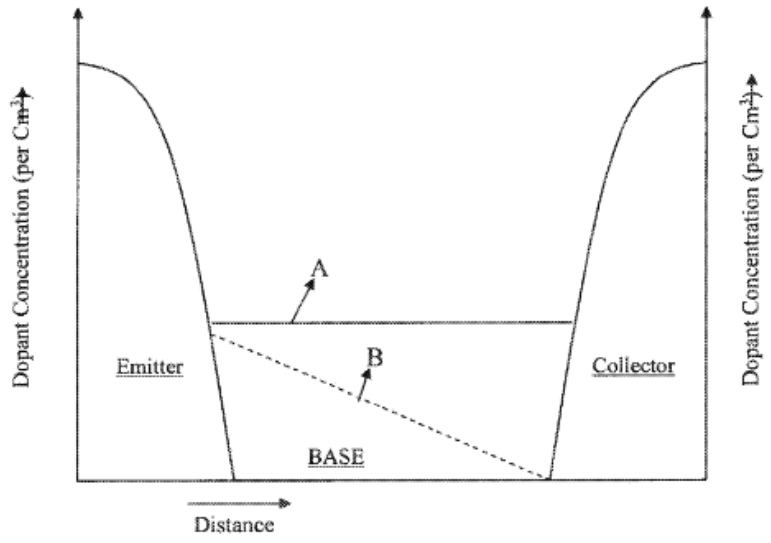

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Figure 1 is labeled "Prior Art" and shows a plot of dopant concentration versus distance. Ex. 1001, 1:62–63, Fig. 1. According to the '842 Patent, Figure 1 "illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base ("A") and graded base ("B")." *Id.* at 2:35–38.

Figure 3A of the '842 Patent is reproduced below.

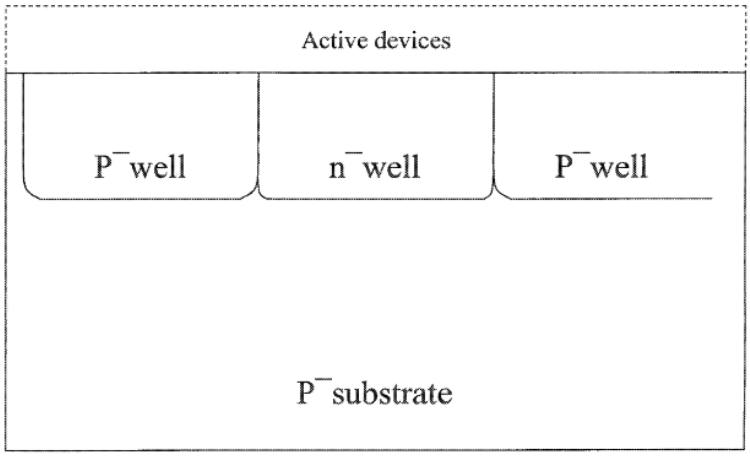

Figure 3A is labeled "Prior art (Twin well CMOS) for a CMOS integrated circuit" ("IC"). Ex. 1001, Fig. 3A. The figure shows a "typical" complementary metal-oxide-semiconductor ("CMOS") very large scale integrated circuit ("VLSI") device that employs "a twin well substrate, on which active devices are subsequently fabricated." *Id.* at 2:16–18; *see also id.* at 2:41–46 (Figure 3A shows a "commonly used prior art CMOS silicon substrate[]" having "a typical prior art IC with two wells (one n^-well in which p-channel transistors are subsequently fabricated and one p^-well in which n-channel transistors are subsequently fabricated).").

Figure 5A of the '842 Patent is reproduced below.

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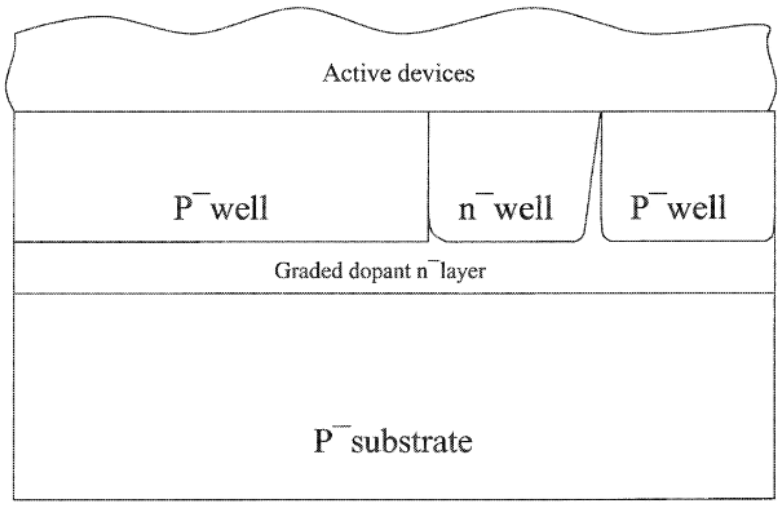

Figure 5A is labeled "A CMOS Substrate for digital, mixed[] signal, and sen[s]or[] IC's." Ex. 1001, Fig. 5A. The figure illustrates "a CMOS silicon substrate with two wells and an underlying layer," which is labeled "Graded dopant n^-layer." *Id.* at 2:54–58, Fig. 5A.

According to the '842 Patent, "[s]purious minority carriers can be generated by clock switching in digital VSLI logic and memory ICs." Ex. 1001, 3:47–48. The '842 Patent states that these "unwanted carriers" degrade performance of various types of devices, including digital imaging ICs. *Id.* at 3:49–55. According to the '842 Patent, "a novel technique is described herein which creates a drift field to sweep these unwanted minority carriers from the active circuitry at the surface into the substrate in a monolithic die as quickly as possible." *Id.* at 3:60–64. The '842 patent discloses that, "[i]n a preferred embodiment, the subterranean n^-layer has a graded donor concentration to sweep the minority carriers deep into the substrate." *Id.* at 3:64–66.

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D. Illustrative Claim

Petitioner challenges claims 1–18 (all claims) of the ’842 Patent. Claims 1 and 9 are independent, and claim 1 is illustrative of the claimed subject matter.

> 1. A semiconductor device, comprising:
>
> a substrate of a first doping type at a first doping level having first and second surfaces;
>
> a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;
>
> a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;
>
> transistors formed in at least one of the first active region or second active region; and
>
> at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

Ex. 1001, 4:45–60.

E. Asserted Challenges and Evidence

Petitioner asserts the following challenges to patentability:

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Claims Challenged	35 U.S.C. §[1]	Reference(s)/Basis
1, 2, 4–10, 12–18	103(a)	Kawagoe[2]
1, 2, 4–10, 12–18	103(a)	Kawagoe, Gupta[3]
1–3, 5–11, 13–18	103(a)	Wieczorek,[4] Wolf[5]
1–3, 5–11, 13–18	103(a)	Wieczorek, Wolf, Gupta

Pet. 5. Petitioner submits the declaration of Travis Blalock, Ph.D. Ex. 1003.

II. WHETHER THE PETITION IS TIME-BARRED

A. Patent Owner's Argument

Patent Owner argues that "[t]he Petition should be dismissed because it is untimely." Prelim. Resp. 1. Specifically, Patent Owner argues that Petitioner is in privity with [redacted]

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. Because the '842 Patent has an effective filing date before that date, we refer to the pre-AIA version of § 103. Ex. 1001, code (60).

[2] Ex. 1007, US 6,043,114, issued March 28, 2000 ("Kawagoe"). Petitioner asserts that Kawagoe is prior art under 35 U.S.C. §102(b). Pet. 4.

[3] Ex. 1014, US 6,163,877, issued December 19, 2000 ("Gupta"). Petitioner asserts that Gupta is prior art under 35 U.S.C. §102(b). Pet. 5.

[4] Ex. 1006, US 2003/0183856 A1, published October 2, 2003 ("Wieczorek"). Petitioner asserts that Wieczorek is prior art under 35 U.S.C. §§ 102(a), (e). Pet. 5.

[5] Ex. 1008, Stanley Wolf and Richard N. Tauber, *Silicon Processing for the VLSI Era*, Vols. 1–4, Lattice Press (2000) ("Wolf"). Petitioner asserts that Wolf was published and publicly available no later than 2002, and is prior art under 35 U.S.C. §102(b). Pet. 5 (citing Exs. 1012, 1013, 1036). Exhibit 1008 was submitted in four parts (A–D) and includes selected portions of Wolf. We cite to Wolf using its original page numbers and omit the exhibit part designations.

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who Petitioner asserts are time-barred under 35 U.S.C. § 315(b). *Id.* at 1–25. *Id.* at 1 (quoting *Taylor v. Sturgell*, 553 U.S. 880, 894 (2008)). Further, Patent Owner argues, Therefore, Petitioner has a giving rise to privity." *Id.* at 1–2 (quoting *Taylor*, 553 U.S. at 895; *Applications in Internet Time, LLC v. RPX Corp.*, 897 F.3d 1336, 1360 (Fed. Cir. 2018)).

B. Legal Standard

"[T]he mere existence of some relationship between a petitioner and another entity is not sufficient" to place that petitioner in privity with that entity. *Google LLC v. DDC Technology, LLC*, IPR2023-00707, Paper 27 at 37 (PTAB Oct. 25, 2023). Instead, "that relationship must be related to [an earlier] lawsuit and be sufficiently close that it can be fairly said the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit." *Id.* In other words, privity concerns "whether the petitioner and the prior litigant's relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit," or "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319 (Fed. Cir. 2018).

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A petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1243–44 (Fed. Cir. 2018). In order to raise such a dispute, "a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy]." *Id.* The amount of evidence a patent owner must produce does not rise to the level of that required to overcome a burden of production. *Id.* at 1244 n.8. Instead, the "burden remains with the petitioner to establish" the timeliness of its petition. *Id.* at 1242.

C. Petitioner's Preliminary Reply

As noted above, we authorized Petitioner to file a Preliminary Reply and Patent Owner to file a Preliminary Sur-Reply, both limited to addressing the issue of the timeliness of the Petition. Patent Owner argues that consideration of Petitioner's Preliminary Reply "is not appropriate," because "Petitioner could have reasonably foreseen" the timeliness arguments raised in the Preliminary Response when Petitioner was "filing its petition." Prelim. Resp. 23 (quoting *Sandoz Inc. v. Abbvie Biotechnology Ltd.*, IPR2018-00002, Paper 11 at 3 (PTAB Mar. 6, 2018)).

We disagree with this argument raised by Patent Owner. According to the Federal Circuit, a petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds*, 903 F.3d at 1244. Thus, there is no requirement that a petitioner preemptively address a disputed issue of privity in its petition.

We also find that Patent Owner's foreseeability argument is factually unsupported. Although Patent Owner argues [redacted]

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[redacted] Without more information, the [redacted] would not have suggested Patent Owner's privity argument because Petitioner was not involved in either one.

Accordingly, we consider Petitioner's Preliminary Reply, as well as Patent Owner's Preliminary Sur-Reply, in determining whether Petitioner has shown its Petition is timely.

D. Alleged Time Bar Based on Earlier Suit [redacted]

Patent Owner alleges that [redacted] are time-barred under § 315(b). Prelim. Resp. 1. [redacted] the present record does not contain any evidence tending to show that this is the case. Section 315(b) bars institution of *inter partes* review only when "the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent." On this record, there is no evidence that [redacted] any earlier than January 23, 2023, which is less than one year before the filing of the present petition on July 27, 2023. *Compare* Pet. 68, *with* Ex. 2019, 1. Accordingly, the service of [redacted] time-barred under § 315(b).

Patent Owner also argues that, [redacted] Prelim. Resp. 1–3, 9 [redacted]; Prelim.

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Sur-Reply 10 (citing *Kofax Inc. v. Uniloc USA Inc.*, IPR2015-01207, Paper 24 at 4–5 (PTAB July 20, 2016)). In *Kofax*, the Board held that the real party-in-interest of a petitioner in a first *inter partes* review could be estopped under § 315(e)(1) from seeking institution of a second *inter partes* review once a final written decision had been issued in the first review. *Kofax*, IPR2015-01207, Paper 22 at 10–11. Sections 315(b) and 315(e)(1) both apply not only to the petitioner, but also the "real party in interest, or privy of the petitioner." Patent Owner implicitly argues that the ruling in *Kofax* should extend § 315(b) beyond its limits to bar [redacted]. Prelim. Sur-Reply 10. We see nothing in the Board's decision in *Kofax* that would justify extending § 315(b) so far beyond its statutory text, and Patent Owner provides us with none. Thus, Patent Owner has produced no evidence that [redacted] under § 315(b).[6]

E. [redacted]

In the subsections below, we address Patent Owner's arguments [redacted] under § 315(b).

1. Preceding and Succeeding Owners of Property

Patent Owner argues that [redacted] and that such products either infringe the challenged patent [redacted] Prelim. Resp. 1, 13–17. It is true that entities who are

[6] In the next section, [redacted] provides additional support for our conclusion regarding Patent Owner's § 315(b) argument.

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"preceding and succeeding owners of property" can be in privity with one another. *Taylor*, 553 U.S. at 894. But it is also true that this rule does not extend to the point where all manufacturers of allegedly infringing goods are in privity with the customers who buy those goods. *See, e.g.*, *WesternGeco*, 889 F.3d at 1319–22 (the parties "had a contractual and fairly standard customer-manufacturer relationship regarding the accused product," which "does not necessarily suggest that the relationship is sufficiently close that both" parties should be considered to be in privity); *Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1340–41 (Fed. Cir. 2018) (same); *Samsung Electronics Co. Ltd. v. Netlist Inc.*, IPR2022-00615, Paper 64 at 22–26 (PTAB June 30, 2023) (same). Thus, to the extent that Patent Owner has produced evidence that [redacted] none of that evidence tends to show [redacted] Even if a manufacturer-customer relationship with respect to accused products were evidence of privity, [redacted] because Patent Owner asserts unequivocally that [redacted] Prelim. Resp. 10.

2. [redacted]

Patent Owner argues [redacted] Prelim. Resp. 16–17 (citing *Ventex Co. v. Columbia Sportswear North America, Inc.*, IPR2017-00651, Paper 148 (PTAB Jan. 24, 2019) (precedential)). We disagree. Unlike the agreements in *Ventex*, Paper 148 at 12, [redacted]

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[redacted] Even if Petitioner were considered [redacted][7]

3. Patent Exhaustion

Patent Owner argues that the doctrine of patent exhaustion [redacted] Prelim. Resp. 17. According to Patent Owner, [redacted] *Id.* We disagree. It is true that [redacted] against any claim of infringement by Patent Owner. We do not see how such a defense [redacted]

4. Indemnification

Patent Owner argues that [redacted] Prelim. Resp. 18–19. As

[7] In contract law, a third-party beneficiary is not a privy. *See, e.g., Pac. Gas & Elec. Co. v. United States*, 838 F.3d 1341, 1350–51 (Fed. Cir. 2016) ("Limited exceptions to the privity requirement have been recognized when a 'party standing outside of privity by contractual obligation stands in the shoes of a party within privity,' such as when a party can demonstrate that it was an intended third-party beneficiary under the contract."); *Prime Finish, LLC v. Cameo, LLC*, 487 F. App'x 956, 959 (6th Cir. 2012) ("Ordinarily, the obligations arising out of a contract are due only to those with whom it is made; a contract cannot be enforced by a person who is not a party to it or in privity with it, except . . . under certain circumstances, [such as] by a third-party beneficiary.") (alterations in original).

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evidence of this alleged indemnification obligation, Patent Owner directs us to Petitioner's "Standard Terms and Conditions of Sale." *Id.* at 18 (citing Ex. 2010, 3). This evidence shows that Petitioner "agrees to defend any claim, suit or proceeding asserted against Buyer based upon a claim that any Product(s) . . . directly infringes any patent . . . effective in the USA and to pay settlements or costs and damages finally awarded in any such suit." Ex. 2010, 3. This agreement is contingent on Petitioner being "promptly notified in writing of the claim and given, at [Petitioner's] request and expense, sole control of the defense or response to such claim and all requested reasonable assistance by Buyer for defense of the same." *Id.* Moreover, Petitioner has the "sole discretion to (i) obtain for Buyer the right to use and sell the Product, (ii) replace or modify the Product(s) with non-infringing Product(s), or (iii) accept the return of the Product(s) and refund the purchase price less reasonable wear and tear" in lieu of defending against any infringement claim. *Id.*

An agreement by a petitioner to indemnify a third party in an earlier infringement suit can give rise to a privity relationship between the petitioner and that third party. *Intel Corp. v. U.S. Int'l Trade Comm'n*, 946 F.2d 821, 839 (Fed. Cir. 1991). But not all indemnification agreements create privity between the parties to the agreement. An indemnification agreement does not give rise to privity where the indemnitor has the option either "to pay for any litigation defense expenses or for any damages related to infringement" or, in the alternative, "to modify or replace the equipment if an infringement claim [is] made," as opposed to being required "to defend [the indemnitee] from a patent infringement lawsuit, reimburse or pay for a lawsuit, cover any damages liability for any adverse patent infringement verdict against [the indemnitee], or initiate an invalidity challenge in one or

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more fora." *WesternGeco*, 889 F.3d at 1321. This describes precisely the option Petitioner would have under the Standard Terms and Conditions of Exhibit 2010. Accordingly, we determine that, on the present record, the indemnification agreement of Exhibit 2010 does not [redacted]

Patent Owner speculates that, as [redacted] might have "received terms [even more] generous [than] the 'Standard' conditions [Petitioner] offers to any purchaser." Prelim. Resp. 18. But Patent Owner does not direct us to any such more generous terms in the evidence presently of record. *Id.* at 18–19. "A mere assertion that a third party is an unnamed [privy], without any support for that assertion, is insufficient to put the issue into dispute." *Worlds*, 903 F.3d at 1244. Moreover, Patent Owner does not dispute Petitioner's assertion that [redacted] with respect to Patent Owner's lawsuit [redacted] Prelim. Reply 6. Thus, on the present record, Patent Owner has not directed us to any evidence that an indemnification obligation creates [redacted]

5. Agency

Patent Owner argues that Petitioner is [redacted] Prelim. Resp. 1, 3–4, 19–20. Patent Owner argues that, "by making accused products [redacted] Petitioner acts within the definition of an agent by acting as "[s]omeone who is authorized to act for or in place of another." *Id.* at 20 (quoting Ex. 2041, 1; alteration by Patent Owner). We disagree for three reasons.

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First, Patent Owner's agency argument is not based on the applicable legal standard. For purposes of privity under § 315(b), the relevant question is whether [redacted] in filing a petition for *inter partes* review. The applicable principle is that "preclusion is appropriate when a nonparty later brings suit as an agent for a party who is bound by a judgment." *Taylor*, 553 U.S. at 895. As the Federal Circuit explains, the rationale behind § 315(b)'s time bar is "to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation." *WesternGeco*, 889 F.3d at 1319. Therefore, the relevant question is "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *Id.* Here, Patent Owner does not assert that [redacted] in this proceeding. Any such assertion would be appropriate only based on evidence that [redacted] *See Taylor*, 553 U.S. at 906 (cautioning that "preclusion is appropriate only if the putative agent's conduct of the suit is subject to the control of the party who is bound by the prior adjudication"). No such evidence is in this record.

Second, the case law cited by Patent Owner does not apply.[8] In each case, the alleged privy was the party asserting a defense of res judicata or collateral estoppel, not the party against whom collateral estoppel was

[8] Prelim. Resp. 19–20 (citing *Herrion v. Children's Hosp. Nat. Med. Ctr.*, 786 F. Supp. 2d 359 (D.D.C.), *aff'd*, 448 F. App'x 71 (D.C. Cir. 2011); *John Street Leasehold, LLC v. Cap. Mgmt. Res., L.P.*, 283 F.3d 73 (2d Cir. 2002); *Fiumara v. Fireman's Fund Ins. Companies*, 746 F.2d 87 (1st Cir. 1984)).

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asserted, as is the case here.[9] The privity issue was whether the party raising a res judicata or collateral estoppel defense was in privity with a defendant in a prior lawsuit brought by the same plaintiff. In *Herrion*, for example, the plaintiff brought successive lawsuits arising out of the same incident, and the defendants in the second suit asserted a res judicata defense. 448 F. App'x at 72. Applicable res judicata law required the court to consider whether the defendants in the second lawsuit were in privity with the defendant in the first lawsuit. *Id.* at 72–73 (finding privity existed for res judicata purposes). Similarly, in *John Street*, the court held that plaintiff's second lawsuit was barred by res judicata in part because the defendants were in privity with the defendants in the prior action. 283 F.3d at 75. Likewise in *Fiumara*, the court held that "the res judicata defense is unmistakably available" to the defendants "as persons in privity with" the defendants in a prior lawsuit brought by the same plaintiff. 746 F.2d at 92. The privity issue in each of these cases was entirely different from this case, where Patent Owner asserts that Petitioner is barred because Petitioner is in privity with the defendants in the prior lawsuit.

Third, even if Patent Owner's argument were on solid legal footing, it lacks factual support in the record. An "essential element[] of agency" is "the principal's 'right to direct or control the agent's actions.'" *In re Google LLC*, 949 F.3d 1338, 1345 (Fed. Cir. 2022) (quoting *Meyer v. Holley*, 537 U.S. 280, 286 (2003)). Patent Owner does not argue in the Preliminary

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[9] By asserting Petitioner is time-barred under § 315(b), Patent Owner is in effect asserting a collateral estoppel bar against Petitioner. *See WesternGeco*, 889 F.3d at 1318 ("Privity is essentially a shorthand statement that collateral estoppel is to be applied in a given case." (citing Consolidated Trial Practice Guide November 2019 at 15, available at https://www.uspto.gov/TrialPracticeGuideConsolidated)).

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Response that [redacted], much less direct us to any evidence that would tend to prove the existence of such a right. Prelim. Resp. 19–20. In the Preliminary Sur-Reply, Patent Owner argues that [redacted] because [redacted] Prelim. Sur-Reply 8–9 (citing Ex. 2010, 5; Ex. 2053; alteration by Patent Owner). Patent Owner does not, however, present any evidence that Petitioner manufactures products b[redacted] *Cf. In re Google*, 949 F.3d at 1346 (contracts to "[a]ssembl[e] equipment based on information and instructions provided by Google" were "suggestive of an agency relationship;" first alteration in original). Patent Owner also does not allege that any particular product [redacted] *See* Ex. 2010, 5 (providing different cancelation policies for "standard Product[s]" than for "Custom Product[s]"); Ex. 2053, 1 (touting Petitioner's ability to supply "System-on-Chip (SoC), Application Specific Integrated Circuit (ASIC), and other custom solutions," but not identifying any particular such products). Thus, Patent Owner does not direct us to any evidence that Petitioner [redacted]

F. Conclusion as to Timeliness of the Petition

As noted above, privity concerns "whether the petitioner and the prior litigant's relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit," or "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed

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litigation." *WesternGeco*, 889 F.3d at 1319. A petitioner's "initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner." *Worlds*, 903 F.3d at 1244. In order to raise such a dispute, "a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy]." *Id.* Here, Patent Owner argues that it has produced such evidence in several respects, but, on the present record, none of the evidence in question tends to show [redacted]

III. REASONABLE LIKELIHOOD ANALYSIS

Petitioner challenges claims 1–18 of the '842 Patent on obviousness grounds. Pet. 4–67. At this stage, Patent Owner does not address the merits of Petitioner's challenges, limiting its preliminary response to the time-bar issue discussed above. Prelim. Resp. 1–25.

A. Legal Standards

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A patent claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that

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the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when presented, objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

Additionally, the obviousness inquiry typically requires an analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness")). Petitioner cannot satisfy its burden of proving obviousness by employing "mere conclusory statements," but "must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

B. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art ("POSITA") would have had "a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience." Pet. 8 (citing Ex. 1003 ¶¶ 47–50). According to Petitioner,

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"[a]dditional education might compensate for a deficiency in experience, and vice-versa." *Id.*

For purposes of this Decision, we apply Petitioner's articulation of the level of ordinary skill in the art. Based on our review of the '842 Patent and the asserted prior art references, we determine that the definition offered by Petitioner comports with the qualifications a person would have needed to understand and implement the teachings of the '842 Patent and the asserted prior art.

C. Claim Construction

In an *inter partes* review, we apply the same claim construction standard as would be used by a district court to construe a claim in a civil action involving the validity or infringement of a patent. 37 C.F.R. § 42.100(b). Under that standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *Id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc); *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365–66 (Fed. Cir. 2012). "The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (quoting *Vivid Techs., Inc. v. Am. Sci. Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Neither party proposes any claim terms for construction. Pet. 9; Prelim. Resp. 1–25. After considering the arguments and information presented in the Petition and Preliminary Response, we agree that we do not

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need to construe any terms expressly in order to determine whether to institute trial.

D. Challenges based on Kawagoe

Petitioner challenges claims 1, 2, 4–10, and 12–18 as obvious based on Kawagoe, alone or in combination with Gupta. Pet. 13–40, 62–67.

1. Kawagoe (Ex. 1007)

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device using an epitaxial wafer, i.e., a semiconductor wafer having a semiconductor single crystal epitaxial layer grown over a polished semiconductor substrate. Ex. 1007, 1:13–27, 2:31–35. According to Kawagoe, "[t]he epitaxial wafer is advantageous in that it is excellent in suppressing the soft errors and resisting to the latchup,"[10] as well as "drastically reduc[ing] the defect density of the gate insulating film" of a semiconductor integrated device. *Id.* at 1:33–40.

Kawagoe discloses various "[r]epresentative[]" processes, including processes in which the single crystal (epitaxial) layer contains an impurity of the same type and in the same concentration as the substrate body. Ex. 1007, 2:55–3:9. According to Kawagoe, the impurity concentration of the substrate body can be made higher than that of epitaxial layer "so that

[10] Petitioner submits Exhibit 1009 (Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Int'l Conf on VLSI Design, 429–434, IEEE 2008), which explains that "soft errors" are "random and not related to permanent hardware faults" and "[t]heir causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation)," including "alpha particles [that] are emitted when the nucleus of an unstable isotope decays to a lower energy state." Ex. 1009, Abstract, 430. Dr. Blalock characterizes "latchup" as "a 'short-circuit' failure condition in poorly designed circuits." Ex. 1003 ¶ 77.

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the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup." *Id.* at 4:1–8. Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device including a step of forming a semiconductor region (well) extending below the epitaxial layer and having an impurity concentration that decreases with increasing depth below the epitaxial layer. *Id.* at 3:10–25. According to Kawagoe, the well can be used for forming a complementary Metal-Oxide-Semiconductor.Field-Effect-Transistor ("MOS.FET") circuit. *Id.* at 3:32–38.

Kawagoe describes seven embodiments, including Embodiment 1 (Ex. 1007, 6:41–12:40, Figs. 1–8) and Embodiment 4 (*id.* at 14:46–19:64, Figs. 16–25). According to Embodiment 1, a semiconductor integrated circuit device includes semiconductor substrate body 2S, epitaxial layer 2E, and gettering layer 2G. *Id.* at 6:51–56, Fig. 1. Substrate body 2S and epitaxial layer 2E are doped with p-type impurity in equal concentrations. *Id.* at 6:60–7:3, 10:51–55, 11:12–16. Embodiment 1 includes n-channel MOS.FET ("nMOS") 4N and p-channel MOS.FET ("pMOS") 4P, the latter being formed in n-well 6, which is doped with n-type impurity and extends below the epitaxial layer. *Id.* at 8:46–52, 9:32–40, 11:18–24, 11:43–50, Figs. 1, 5, 7.

According to Embodiment 4, substrate body 2S and epitaxial layer 2E are doped with p-type impurity, and the impurity concentration of substrate body 2S is higher than that of epitaxial layer 2E "to improve the resistance to the latchup." Ex. 1007, 14:64–15:6, 15:13–17, 16:16–21, 19:59–63, Fig. 17. Embodiment 4 includes p-well 6*p* formed with nMOS 4N and n-well 6*n* formed with pMOS 4P. *Id.* at 15:26–40, 17:40–18:35, Figs. 16, 21–23. In Embodiment 4, the impurity concentration in p-well 6*p* and

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n-well 6*n* decreases with increasing depth below the epitaxial layer. *Id.* at 15:62–16:15, 17:55–61, Fig. 17. Kawagoe discloses that the concentration gradient reduces soft errors by attracting carriers (electrons) to the substrate and preventing them from entering the p-well. *Id.* at 16:2–11.

Petitioner relies on Kawagoe Figures 17 and 23, which illustrate Embodiment 4 and are reproduced below.

FIG. 17

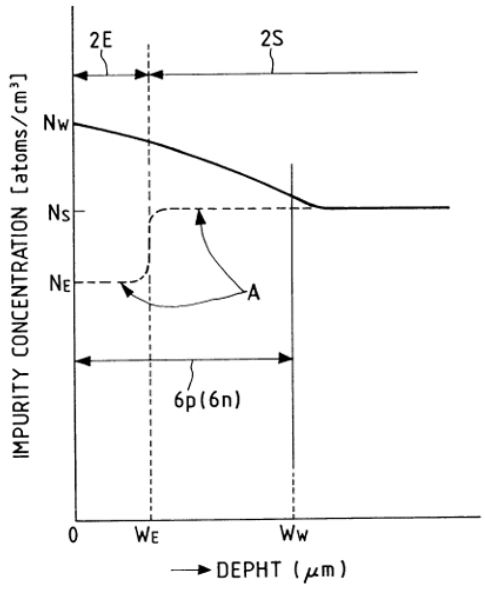

FIG. 23

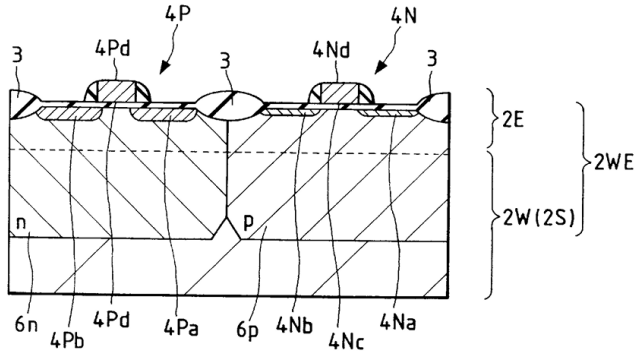

Figure 17 is a plot of impurity concentration as a function of depth in a semiconductor integrated circuit device, which shows "the p-well 6*p* and n-well 6*n* have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer 2E." Ex. 1007, 5:41–45, 15:62–16:40. Figure 23 shows a step in a process for manufacturing a semiconductor integrated circuit device, including p-well 6*p* formed with nMOS 4N and n-well 6*n* formed with pMOS 4P. *Id.* at 5:1–4, 15:26–32, 18:3–35.

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2. Gupta (Ex. 1014)

Gupta "relates to the field of complimentary [*sic*, complementary] metal oxide semiconductor (CMOS) circuits, and more particularly to automatically producing layouts for CMOS circuits." Ex. 1014, 1:7–10. According to Gupta, "[a]s semiconductor chips become ever larger, incorporating ever more devices, it becomes increasingly important to minimize semiconductor area used by a given number of devices." *Id.* at 1:28–31. Doing so "potentially [saves] millions of dollars." *Id.* at 1:31–34. To accomplish this goal, Gupta discloses abutting multiple transistors to "form transistor chains." *Id.* at 2:17–21, Fig. 4.

3. Claim 1

a) Preamble

The preamble of claim 1 recites a "semiconductor device." Ex. 1001, 4:45. Petitioner contends that Kawagoe discloses the preamble. Pet. 13–14 (citing Ex. 1007, code (54), 1:13–23, 14:46–67, Figs. 16, 17, 23). We find that Petitioner's contention for the claim 1 preamble is sufficiently supported for purposes of institution.

b) Element 1.1

Claim element 1.1 recites "a substrate of a first doping type at a first doping level having first and second surfaces." Ex. 1001, 4:46–47. Petitioner contends that Kawagoe discloses claim element 1.1, relying on a combination of Kawagoe's Embodiments 1 and 4. Pet. 13–19. Petitioner contends that "a substrate of a first doping type" is taught by Kawagoe's epitaxial substrate, including epitaxial layer 2E and substrate body 2S doped with p-type impurity, and that the recited "first and second surfaces" correspond to the top and bottom surfaces of the epitaxial substrate.

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Pet. 14–15 (citing Ex. 1007, 6:50–7:3, 14:61–15:12, 17:10–18:38, Figs. 20, 23). Petitioner contends that the recitation, "at a first doping level," is taught by Kawagoe's Embodiment 1, which has a uniformly-doped epitaxial substrate, with epitaxial layer 2E and substrate body 2S having the same impurity concentration. Pet. 16 (citing Ex. 1007, code (57), 2:57–3:9, 6:60–7:3). Petitioner contends that a POSITA would have understood that Kawagoe teaches forming a twin-well CMOS device on either a uniformly-doped epitaxial substrate, as described in Embodiment 1, or a non-uniformly doped latchup-resistant epitaxial substrate, as described in Embodiment 4. Pet. 16 (citing Ex. 1003 ¶ 72). Relying on Dr. Blalock's testimony and various prior art disclosures, Petitioner contends that a POSITA would have been motivated to use a uniformly-doped epitaxial substrate to form a twin-well CMOS device and would have had a reasonable expectation of success. Pet. 17–19 (citing Ex. 1003 ¶¶ 73–78; Ex. 1007, 1:33–40, 2:57–65, 8:40–52, 12:8–40, 14:58–60, 15:7–40, 19:49–63, Fig. 23; Ex. 1008, 381, 387–89, 406, 419, 523, 530; Ex. 1026, 1). We find that Petitioner's contention for claim element 1.1 is sufficiently supported for purposes of institution.

c) Elements 1.2 to 1.4

Claim element 1.2 recites "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed." Claim element 1.3 recites "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed." Claim element 1.4 recites "transistors formed in at least one of the first active region or second active region." Ex. 1001, 4:48–56.

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Petitioner contends that Kawagoe discloses claim elements 1.2 to 1.4, relying on Kawagoe's Embodiment 4. Pet. 19–25. Petitioner contends that "a first active region" (claim element 1.2) is taught by Kawagoe's "semiconductor regions 4Na and 4Nb . . . for forming the source-drain regions of the nMOS [n-channel transistor] 4N" together with the channel region between the source-drain regions. Pet. 20 (quoting Ex. 1007, 8:66–67; bracketed addition and ellipsis is Petitioner's). Petitioner contends that Kawagoe's semiconductor regions 4Na and 4Nb (corresponding to the "first active region") has a doping type (n-type) opposite to the doping type (p-type) of the substrate, as recited in claim element 1.2. Pet. 20–21. Petitioner contends that "a second active region" (claim element 1.3) is taught by Kawagoe's "semiconductor regions 4Pa and 4Pb . . . for forming the source-drain regions of the pMOS [p-channel transistor] 4P" together with the channel region between the source-drain regions. Pet. 23 (quoting Ex. 1007, 9:47–48; bracketed addition is Petitioner's). Although Petitioner quotes Kawagoe's description of Embodiment 1, Kawagoe discloses that Embodiment 4's CMOS circuit, including transistors nMOS 4N and pMOS 4P, is similarly constructed. Ex. 1007, 15:26–40 (cited at Pet. 20, 23).

Addressing claim elements 1.2 to 1.4, Petitioner provides annotations of Kawagoe Figure 23 identifying nMOS transistor 4N formed in the first active region and pMOS transistor 4P formed in the second active region. Pet. 20, 23. Petitioner contends that, "[w]hile Figure 23 illustrates an exemplary nMOS transistor 4N in the first active region, a POSITA would have understood that Kawagoe teaches forming multiple nMOS transistors in this region to minimize chip area, as good layout practice dictates." Pet. 21 (citing Ex. 1003 ¶ 80; Ex. 1014, 1:52–54, 2:17–21); *see also* Pet. 24

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(similar contention for pMOS transistor 4P in second active region, citing Ex. 1003 ¶ 85).

For its challenge based on Kawagoe and Gupta, Petitioner relies on Gupta to teach multiple chained PMOS transistors formed in a p-channel active region and multiple chained NMOS transistors formed in an n-channel active region. Pet. 64 (citing Ex. 1014, 4:12–43, Fig. 4). Citing Dr. Blalock's testimony, Petitioner contends that a POSITA would have been motivated to fabricate a CMOS chip according to the combined teachings of Kawagoe and Gupta to achieve high packing density at submicron dimensions and would have had a reasonable expectation of success. Pet. 65–66 (citing Ex. 1003 ¶¶ 172, 173). According to Petitioner, "a POSITA would have understood that each of the active regions of Kawagoe's . . . CMOS devices typically contain many transistors, as taught by Gupta and illustrated in Gupta's Figure 4." Pet. 67 (citing Ex. 1003 ¶ 175).

We find that Petitioner's contentions for claim elements 1.2 to 1.4 are sufficiently supported for purposes of institution.

d) Element 1.5

Claim element 1.5 recites "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate." Ex. 1001, 57–60. Petitioner contends that Kawagoe discloses claim element 1.5, relying on Kawagoe's Embodiment 4. Pet. 25–32. Petitioner contends that a "graded dopant concentration" is taught by Kawagoe Figure 17, which shows the dopant concentration in the channel region is "gradually lowered in the depthwise direction from the principal

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surface (having an impurity concentration NW) of the epitaxial layer 2E." Pet. 26 (citing Ex. 1007, 15:62–16:40). Petitioner contends that, in Kawagoe, the graded dopant concentration "aid[s] carrier movement from the first surface to the second surface of the substrate," as recited in claim element 1.5. Pet. 27–28. Petitioner relies on Kawagoe's disclosure that the concentration gradient attracts electrons to substrate body 2S. Pet. 28 (citing Ex. 1007, 16:2–11). Petitioner further contends that the downward-sloping dopant concentration in Kawagoe Figure 17 "aids carrier movement from the first surface to the second surface of the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario." Pet. 30 (citing Ex. 1003 ¶ 94). As support for that contention, Petitioner relies on the file history for U.S. Patent No. 8,421,195 ("the parent '195 patent") and references cited during examination. Pet. 30–32 (citing Ex. 1003 ¶ 94; Exs. 1010, 1016, 1031).

We find that Petitioner's contention for claim element 1.5 is sufficiently supported for purposes of institution.

e) Conclusion

We determine that Petitioner's contentions, as summarized above, show a reasonable likelihood of prevailing on its challenge to claim 1 based on Kawagoe, alone or in combination with Gupta.

4. Remaining Claims

In view of our determination that Petitioner establishes a reasonable likelihood for claim 1, and because Petitioner's arguments and evidence for remaining claims 2, 4–10, and 12–18 (Pet. 32–40) are similar to Petitioner's arguments and evidence for claim 1 (Pet. 13–32) and are unopposed at this

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stage by Patent Owner, we determine that it is unnecessary to provide an explicit analysis of Petitioner's challenges to the remaining claims in order to provide guidance to the parties for the upcoming trial. Consolidated Trial Practice Guide November 2019 ("CTPG")[11] at 64; *see* 37 C.F.R. § 42.108(a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim."); *see also SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018) (holding that 35 U.S.C. § 314 forbids the Board's prior "partial institution" practice).

E. Challenges based on Wieczorek and Wolf

Petitioner challenges claims 1–3, 5–11, and 13–18 as obvious based on Wieczorek and Wolf, by themselves, or with Gupta. Pet. 41–67.

1. Wieczorek (Ex. 1006)

Wieczorek relates "to a semiconductor device, such as a field-effect transistor, having an improved retrograde dopant profile in a channel region of the transistor element." Ex. 1006 ¶ 2. The Petition relies on Wieczorek's description of the prior art, not its disclosed improvement. Pet. 11, 40.

Wieczorek explains that a retrograde channel dopant profile is one where "the concentration of dopants increases from the gate insulation layer to the areas located deeper down the channel region." Ex. 1006 ¶ 6. According to Wieczorek, a retrograde channel dopant profile is desirable, but "very difficult to obtain." *Id.* Wieczorek states that "the dopant concentration immediately after the implantation process exhibits a desired retrograde dopant profile" (*id.* ¶ 9), but during heat treatment, "the initially

[11] *Available at* https://www.uspto.gov/TrialPracticeGuideConsolidated.

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retrograde profile in the vicinity of the surface of the semiconductor device . . . may have become substantially uniformly distributed" due to diffusion of the dopant atoms (*id.* ¶ 11).

Petitioner relies on Figures 1b and 2b (reproduced below), which Wieczorek uses to illustrate the prior art.

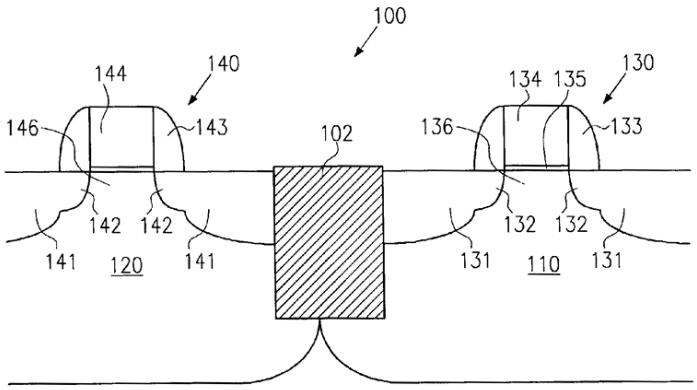

FIG.1b
(Prior Art)

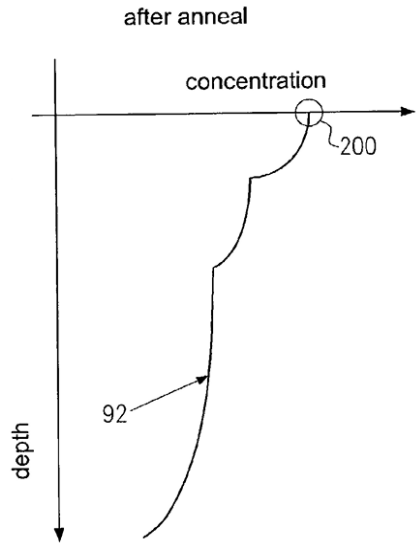

FIG.2b
(Prior Art)

Wieczorek Figure 1b shows a conventional semiconductor device at an intermediate manufacturing stage, including shallow trench isolation 102 separating N-well structure 120 from P-well structure 110. Ex. 1006 ¶¶ 7, 20. The device includes P-channel transistor 140 with source and drain regions 141 in N-well structure 120 and N-channel transistor 130 with source and drain regions 131 in P-well structure 110. *Id.* ¶ 12. Wieczorek Figure 2b is a graph of dopant concentration versus depth of N-well structure 120 and P-well structure 110 and shows "a typical dopant profile with respect to the depth of the respective well structure" after ion implantation and heat treatment. *Id.* ¶¶ 9–11, 13, 21.

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2. Wolf (Ex. 1008)

Wolf is a four-volume textbook titled "Silicon Processing for the VLSI Era." Ex. 1008. Chapter 16 focuses on CMOS technology. Ex. 1008, xxiv–xxv, 807–40.

3. Reasons to Combine Wieczorek and Wolf

Petitioner argues that a "POSITA would have been motivated to combine Wieczorek with Wolf." Pet. 40 (citing Ex. 1003 ¶¶ 121, 122). Petitioner argues that Wieczorek describes "a conventional prior-art CMOS device" and "Wolf is a well-known textbook that teaches known fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS devices." *Id.* (citing Ex. 1006 ¶¶ 4, 7, 8, 12, 20, 21, Fig. 1b; Ex. 1008, Chap. 16). According to Petitioner, a POSITA would have "understood and expected that the teachings of Wolf would apply to Wieczorek's conventional CMOS device" and "looked to Wolf for additional details related to conventional CMOS devices." Pet. 40–41. We find that Petitioner's arguments and evidence concerning reasons to combine Wieczorek and Wolf are sufficient for purposes of institution.

4. Claim 1

a) Preamble

The preamble of claim 1 recites a "semiconductor device." Ex. 1001, 4:45. Petitioner contends that Wieczorek discloses the preamble. Pet. 41 (citing Ex. 1006 ¶ 12). We find that Petitioner's contention for the claim 1 preamble is sufficiently supported for purposes of institution.

b) Element 1.1

Claim element 1.1 recites "a substrate of a first doping type at a first doping level having first and second surfaces." Ex. 1001, 4:46–47.

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Petitioner relies on Wieczorek in combination with Wolf for claim element 1.1. Pet. 41. Petitioner contends that Wieczorek Figure 1b illustrates a conventional twin-well CMOS device, that Wieczorek does not specify what constitutes an appropriate substrate for making the device, and that Wolf teaches that a "uniform, lightly doped p- or n-type substrate" is commonly used in twin-well CMOS devices. Pet. 41–42 (citing Ex. 1003 ¶¶ 124–126; Ex. 1006 ¶¶ 4, 7, 12, 20, 21, Fig. 1b; Ex. 1008, 387–89, 523–25, 530, Fig. 8-1(e)). Relying on Dr. Blalock's testimony, Petitioner contends that "a POSITA would have found it obvious to use a uniformly doped n- or p-type substrate ('a substrate of a first doping type at a first doping level') as a suitable substrate for Wieczorek's CMOS device in Figure 1b." Pet. 43 (citing Ex. 1003 ¶ 127). Petitioner states that, "[f]or purpose of claim mapping, Wieczorek-Wolf's substrate is taken as a p-type nonepitaxial substrate." Pet. 44. Petitioner contends that, "[c]onsistent with the teachings of Wolf," Wieczorek's Figure 1b substrate has top and bottom surfaces corresponding to the "first and second surfaces" of claim element 1.1. *Id.* (providing annotation of Wieczorek Figure 1b identifying first and second surfaces). We find that Petitioner's contention for claim element 1.1 is sufficiently supported for purposes of institution.

c) Elements 1.2 to 1.4

Claim element 1.2 recites "a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed." Claim element 1.3 recites "a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed." Claim element 1.4 recites "transistors

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formed in at least one of the first active region or second active region." Ex. 1001, 4:48–56.

Petitioner contends that Wieczorek-Wolf teaches claim elements 1.2 to 1.4. Pet. 45–50. Petitioner contends that "a first active region" (claim element 1.2) is taught by Wieczorek's source-drain regions 131, 132 together with channel region 136 of N-channel transistor 130. Pet. 45–46 (citing Ex. 1006 ¶¶ 4, 7, 12, 13, Fig. 1b). Petitioner contends that, "[b]ecause the source-drain regions of the first active region are N-doped, Wieczorek-Wolf's first active region has a second doping type (N-type) opposite in conductivity to the first doping type (P-type) of the substrate," as recited in claim element 1.2. Pet. 46 (citing Ex. 1003 ¶ 131; Ex. 1006 ¶ 12). Petitioner contends that "a second active region" (claim element 1.3) is taught by Wieczorek's source-drain regions 141, 142 together with channel region 146 of P-channel transistor 140, "which is separate from and disposed adjacent to the first active region." Pet. 48–49 (citing Ex. 1006 ¶¶ 4, 7, 12, 13, Fig. 1b).

Addressing claim elements 1.2 to 1.4, Petitioner provides annotations of Wieczorek Figure 1b identifying transistor 130 formed in the first active region and transistor 140 formed in the second active region. Pet. 46, 49. Petitioner contends that, "[w]hile Figure 1b illustrates a single exemplary nMOS transistor 130 formed in the first active region, a POSITA would have understood that Wieczorek teaches forming multiple nMOS transistors in the first active region to minimize chip area, as good layout practice dictates." Pet. 46 (citing Ex. 1003 ¶ 132; Ex. 1006 ¶ 4; Ex. 1014, 1:52–54, 2:17–21); *see also* Pet. 49 (similar contention for pMOS transistor 140 in second active region, citing Ex. 1003 ¶ 137; Ex. 1006 ¶ 4).

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For its challenge based on Wieczorek, Wolf, and Gupta, Petitioner relies on Gupta to teach multiple chained PMOS transistors formed in a p-channel active region and multiple chained NMOS transistors formed in an n-channel active region. Pet. 64 (citing Ex. 1014, 4:12–43, Fig. 4). Citing Dr. Blalock's testimony, Petitioner contends that a POSITA would have been motivated to fabricate a CMOS chip according to the combined teachings of Wieczorek, Wolf, and Gupta to achieve high packing density at submicron dimensions and would have had a reasonable expectation of success. Pet. 65–66 (citing Ex. 1003 ¶¶ 172, 173). According to Petitioner, "a POSITA would have understood that each of the active regions of . . . Wieczorek's CMOS devices typically contain many transistors, as taught by Gupta and illustrated in Gupta's Figure 4." Pet. 67 (citing Ex. 1003 ¶ 175).

We find that Petitioner's contentions for claim elements 1.2 to 1.4 are sufficiently supported for purposes of institution.

d) Element 1.5

Claim element 1.5 recites "at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate." Ex. 1001, 4:57–60. Petitioner contends that Wieczorek-Wolf teaches claim element 1.5. Pet. 50–55. Petitioner contends that a "graded dopant concentration" is taught by Wieczorek Figure 2b, which Petitioner contends shows that the dopant concentration is "downward-sloping from the top surface of the substrate and all the way through the entire depth of the channel region . . . and the underlying well-region." Pet. 51–52 (citing Ex. 1003 ¶ 141; Ex. 1006 ¶¶ 9, 11, 13, Figs. 1b, 2b). Petitioner contends that "Wieczorek's downward-sloping graded dopant concentration aids

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carrier movement from the first surface to the second surface of the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario." Pet. 52–53 (citing Ex. 1003, ¶¶ 142, 143). As support for that contention, Petitioner relies on essentially the same arguments and evidence concerning the parent '195 patent's file history and cited references as Petitioner presents for claim element 1.5 based on Kawagoe. *Compare* Pet. 53–54, *with* Pet. 30–32.

We find that Petitioner's contention for claim element 1.5 is sufficiently supported for purposes of institution.

e) Conclusion

We determine that Petitioner's contentions, as summarized above, show a reasonable likelihood of prevailing on its challenge to claim 1 based on Wieczorek and Wolf, by themselves or in combination with Gupta.

5. Remaining Claims

In view of our determination that Petitioner establishes a reasonable likelihood for claim 1, and because Petitioner's arguments and evidence for remaining claims 2, 3, 5–11, and 13–18 (Pet. 54–62) are similar to Petitioner's arguments and evidence for claim 1 (Pet. 41–54) and are unopposed at this stage by Patent Owner, we determine that it is unnecessary to provide an explicit analysis of Petitioner's challenges to the remaining claims in order to provide guidance to the parties for the upcoming trial. CTPG at 64; 37 C.F.R. § 42.108(a); *SAS*, 138 S. Ct. at 1359–60.

IV. CONCLUSION

After considering the Petition and the Preliminary Response, we determine that the Petition is not time-barred, and the information presented

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establishes a reasonable likelihood that Petitioner would prevail in showing that at least one claim of the '842 Patent is unpatentable. Accordingly, we institute an *inter partes* review of all challenged claims on all grounds asserted against those claims in the Petition. 37 C.F.R. § 42.108(a); *SAS*, 138 S. Ct. at 1359–60; *see also* Guidance on the Impact of SAS on AIA Trial Proceedings (April 26, 2018).[12]

V. ORDER

It is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–18 of the '842 Patent is instituted commencing on the entry date of this Decision;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of trial;

FURTHER ORDERED that, in view of the pending motion to seal, this Decision is being filed "Board and Parties Only;" and

FURTHER ORDERED that after conferring with Petitioner, Patent Owner shall, within one week of this Decision, submit to the Board via email to Trials@uspto.gov, a version of this Decision to be filed on the public record, with any redactions proposed by either party.

[12] Available at https://www.uspto.gov/patents-application-process/patent-trial-and-appeal-board/trials/guidance-impact-sas-aia-trial.

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