

[REDACTED]

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC
Petitioner,

v.

GREENTHREAD, LLC,
Patent Owner.

IPR2024-00265
Patent 9,190,502 B2

Before JEFFREY W. ABRAHAM, JON B. TORNQUIST, and
MONICA S. ULLAGADDI, *Administrative Patent Judges*.

ABRAHAM, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Semiconductor Components Industries, LLC (“Petitioner”) filed a Petition requesting *inter partes* review of claims 7–12 of U.S. Patent No. 9,190,502 B2 (Ex. 1001, “the ’502 patent”). Paper 1 (“Pet.”). Greenthread, LLC (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 14 (“Prelim. Resp.”). With authorization, Petitioner subsequently filed a Preliminary Reply (Paper 16, “Prelim. Reply”) and Patent Owner filed a Preliminary Sur-reply (Paper 19, “Prelim. Sur-reply”).

An *inter partes* review may not be instituted “unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence set forth by Petitioner and Patent Owner, we determine that the information presented in the Petition demonstrates a reasonable likelihood that Petitioner would prevail on at least one of the challenged claims of the ’502 patent. Accordingly, we institute an *inter partes* review as to all of the challenged claims of the ’502 patent on all of the grounds of unpatentability set forth in the Petition.

II. BACKGROUND

A. *Related Matters*

The parties indicate that the ’502 patent is at issue in the following proceedings:

Greenthread, LLC v. Cirrus Logic, Inc., No. 1:23-cv-00369 (W.D. Tex. filed March 31, 2023);

Greenthread, LLC v. Texas Instruments Inc., No. 2:23-cv-00157 (E.D. Tex. filed April 6, 2023);

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Greenthread, LLC v. OSRAM GmbH, No. 2:23-cv-00179 (E.D. Tex. filed April 19, 2023);

Greenthread, LLC v. OmniVision Technologies, Inc.,
No. 2:23-cv-00212 (E.D. Tex. filed May 10, 2023);

Greenthread, LLC v. Monolithic Power Systems, Inc.,
No. 1:23-cv-00579 (D. Del. filed May 26, 2023); and

Cirrus Logic et al. v. Greenthread, LLC, IPR2024-00018, before the
Patent Trial and Appeal Board, filed October 27, 2023.

Pet. 1–2; Paper 4, 2–3 (Patent Owner’s mandatory notices).

Petitioner further indicates that “U.S. Patent Nos. 11,121,222 and
10,510,842 (child patents to the ’502 Patent), but not the ’502 Patent itself,
are the subject of” other proceedings:

*Greenthread, LLC v. ON Semiconductor Corporation and
Semiconductor Components Industries, LLC*, No. 1:23-cv-00443 (D. Del.
filed April 21, 2023); and

Semiconductor Components Industries, LLC v. Greenthread, LLC,
IPR2023-01242, -01243, -01244, before the Patent Trial and Appeal Board,
filed July 27, 2023.

Pet. 3.

B. Real Parties-in-Interest

Petitioner identifies itself and ON Semiconductor Corporation as the
real parties-in-interest. Pet. 1. Patent Owner identifies itself as the real
party-in-interest. Paper 4, 2.

C. The ’502 patent

The ’502 patent, titled “Semiconductor Devices with Graded Dopant
Regions,” issued on November 17, 2015. Ex. 1001, codes (45), (54). The

'502 patent “relates to all semiconductor devices and systems,” including Bipolar Junction Transistors (BJT). Ex. 1001, 1:17–30.

The '502 patent explains that in bipolar junction transistors, minority carriers are the principal device conduction mechanism, but majority carriers also play a small but finite role in modulating the conductivity in such devices. Ex. 1001, 1:27–30. The '502 patent further explains that “[e]fforts have been made in graded base transistors to create an ‘aiding drift field’, to enhance the diffusing minority carrier’s speed from emitter to collector” versus the standard “uniformly doped base” bipolar junction transistors. Ex. 1001, 1:38–40. The '502 patent explains that this improvement has not been implemented in most semiconductor devices, including various power MOSFETs and IGBTs, which “still use a uniformly doped drift epitaxial region in the base.” Ex. 1001, 1:40–44. The invention of the '502 patent implements a graded dopant concentration in these devices, which results in two important performance enhancements: “electrons can be swept from source to drain rapidly, while at the same time holes can be recombined closer to the n+ buffer layer,” thereby improving “t(on) and t(off) in the same device.” Ex. 1001, 3:13–18.

Figure 1 of the '502 Patent is reproduced below.

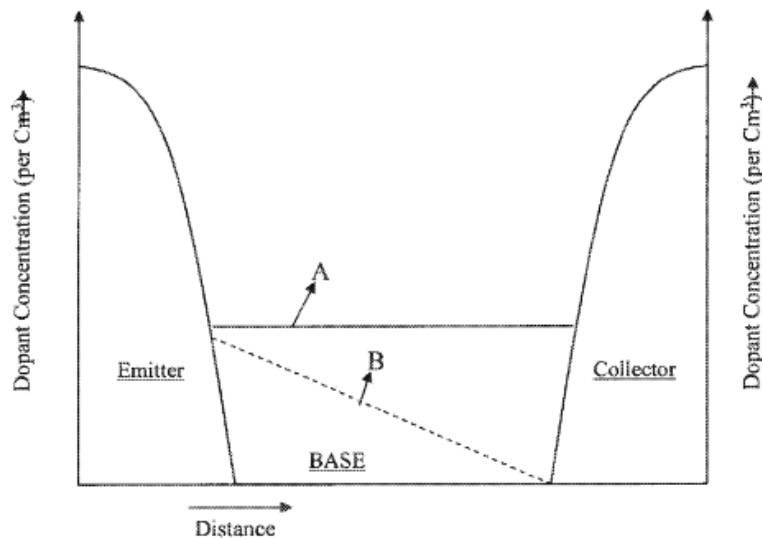


Figure 1 is labeled “Prior Art” and “illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, A—uniform base, and B—graded base.” Ex. 1001, 2:17–19.

Figure 3A of the ’502 patent is reproduced below.

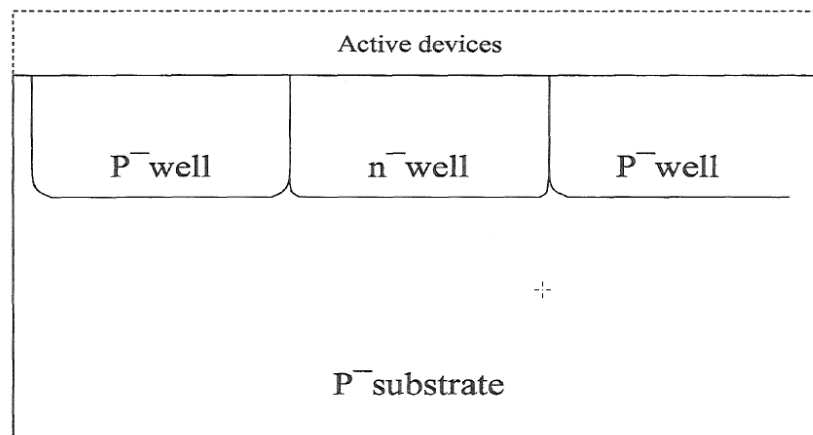


Figure 3A is labeled “Prior art” and shows a cross-sectional view of a “commonly used CMOS silicon substrate with two wells (one n- well in which p-channel transistors are subsequently fabricated and one p- well in

which n-channel transistors are subsequently fabricated).” Ex. 1001, 2:22–27, Fig. 3A.

Figure 5A of the ’014 patent is reproduced below.

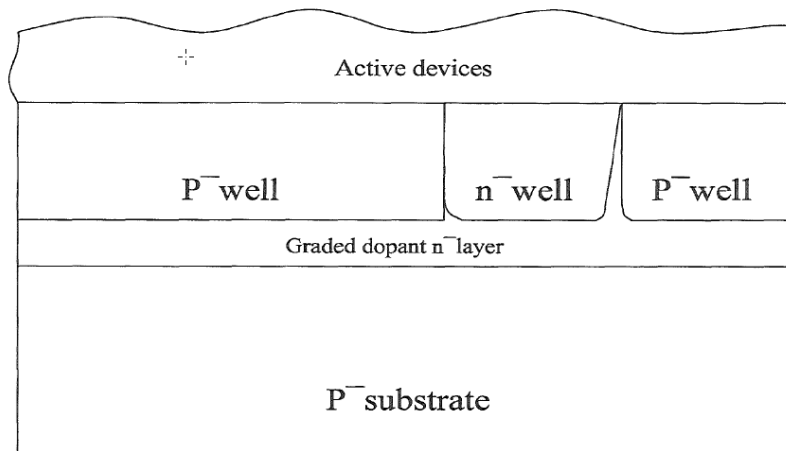


Figure 5A illustrates a cross section of a CMOS silicon substrate with two wells and an underlying layer using embodiments of the invention.

Ex. 1001, 2:31–35. According to the ’502 patent, “[s]purious minority carriers can be generated by clock switching in digital VSLI logic and memory ICs,” and these “unwanted carriers can discharge dynamically-held ‘actively held high’ nodes,” and serve to degrade performance of various types of devices, including digital imaging ICs. Ex. 1001, 3:25–34. The ’502 patent further explains that “a novel technique has been described here by creating a drift field to sweep these unwanted minority carriers into the substrate as quickly as possible, from the active circuitry at the surface.” Ex. 1001, 3:39–42. In particular, “[i]n a preferred embodiment, the subterranean n–layer has a graded donor concentration to sweep the minority carriers deep into the substrate.” Ex. 1001, 3:42–44.

D. Illustrative Claim

Claim 7 is the only independent claim challenged, and is reproduced below.

7. A semiconductor device comprising:
- a surface layer;
 - a substrate;
 - an active region including a source and a drain, disposed on one surface of said surface layer;
 - a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate;
 - and
 - at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Ex. 1001, 4:52–67.

E. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 6):¹

Claim(s) Challenged	35 U.S.C. §	Reference(s)
7, 12	103	Payne ²
7–12	103	Sakai, ³ Kawagoe ⁴
9–11	103	Payne, Wolf ⁵
8	103	Payne, Parrillo ⁶
12	103	Payne, Silverbrook ⁷
7–12	103	Sakai, Kawagoe, Silverbrook

Petitioner also relies upon the declaration testimony of Travis Blalock, Ph.D. Ex. 1003.

III. ANALYSIS

A. Legal Standard

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016). The burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, took effect on March 16, 2013. The ’502 patent claims priority to an application filed September 3, 2004. Ex. 1001, code (60). Thus, we apply the pre-AIA version of § 103. *See* Pet. 5 n.1.

² US 4,684,971, issued Aug. 4, 1987 (Ex. 1005).

³ US 4,907,058, issued Mar. 6, 1990 (Ex. 1006).

⁴ US 6,043,114, issued Mar. 28, 2000 (Ex. 1007).

⁵ Stanley Wolf & Richard N. Tauber, *Silicon Processing for the VLSI Era*, Vols. 1–4 (Lattice Press 2000) (Ex. 1008).

⁶ US 4,435,896, issued Mar. 13, 1984 (Ex. 1025).

⁷ US 6,614,560 B1, issued Sept. 2, 2003 (Ex. 1048).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and “the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In order to determine whether an invention would have been obvious at the time the application was filed, we consider the level of ordinary skill in the pertinent art. *Graham*, 383 U.S. at 17. In assessing the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (quotation omitted).

Petitioner contends that one of ordinary skill in the art would have had “a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience.” Pet. 8 (citing Ex. 1003 ¶¶ 57–60). Petitioner further contends that “[a]dditional education might compensate for a deficiency in experience, and vice-versa.” Pet. 8.

Patent Owner does not address the level of ordinary skill in the art. *See generally*, Prelim. Resp.

On this record, we adopt Petitioner’s unchallenged definition of the person of ordinary skill in the art as it appears consistent with the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (holding that the prior art itself can reflect the appropriate level of ordinary skill in the art).

C. Claim Construction

In an *inter partes* review proceeding, a patent claim is construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (as amended Oct. 11, 2018). This rule adopts the same claim construction standard used by Article III federal courts, which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. Under this standard, the words of a claim are generally given their “ordinary and customary meaning,” which is the meaning the term would have to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *See Phillips*, 415 F.3d at 1312–13.

Petitioner contends that no claim terms require express construction to resolve the issues presented in the Petition. Pet. 8.

Patent Owner does not assert that any claim terms require express construction. *See generally*, Prelim. Resp.

Upon review of the record, we determine that no claim terms require express construction for purposes of this Decision. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent

necessary to resolve the controversy.”)(quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

D. Claims 7 and 12 – Alleged Obviousness in view of Payne

Petitioner contends claims 7 and 12 would have been obvious in view of Payne. Pet. 13–43. Patent Owner contends that Petitioner fails to demonstrate that Payne discloses all of the limitations in claims 7 and 12. Prelim. Resp. 1–15.

1. Payne (Ex. 1005)

Payne “relates to complementary field effect transistors formed by ion implantation, and in particular to a structure and method of fabrication which permit high packing density.” Ex. 1005, 1:5–8. According to Payne, CMOS devices “comprise n-channel and p-channel devices formed in the same substrate,” and are traditionally “formed by diffusion or implantation of a p-type ‘tub’ in an n-type silicon substrate so that the n-channel device is fabricated in the tub and the p-channel device is fabricated in the adjacent portion of the substrate.” Ex. 1005, 1:9–18. This method “led to the constraint that the concentration at the surface in the tub was much greater than the surface concentration of the substrate.” Ex. 1005, 1:18–21. Payne states that one proposed method to avoid this constraint was “to form the p-channel device in a second tub of n-conductivity type and higher impurity concentration than a more lightly doped substrate.” Ex. 1005, 1:24–27. “Using either the single tub or twin tub approach, a considerable amount of semiconductor area is needed due to the fact that the tub impurities will diffuse laterally as well as vertically during the drive-in to establish the desired tub depth.” Ex. 1005, 1:34–38. Payne states that “[t]his is particularly troublesome in the twin-tub process since any significant

overlap of the two tubs results in decreased doping concentration of each tub at the boundaries which can cause punch through or field inversion channeling during device operation.” Ex. 1005, 1:39–43. This problem required large spacing of the source and drain regions of the transistors, and Payne seeks to avoid this need by “provid[ing] a CMOS structure and method of manufacture which requires little semiconductor space.” Ex. 1005, 1:43–54.

In particular, Payne’s “device is fabricated in a silicon semiconductor substrate, 10, of ‘N–’ conductivity type which . . . is typically approximately 20 mils thick.” Ex. 1005, 2:56–60. On this substrate, tub regions 15 and 17 are formed, one “having the same conductivity type as the substrate but higher impurity concentration” and the other having the opposite conductivity type. Ex. 1005, 3:35–39, 4:12–14, Figs. 2–5. Surface regions 18 and 20 are formed “covering essentially the same area as” tubs 15 and 17, with each region having the same conductivity type as the tub over which it lies but with higher impurity concentration. Ex. 1005, 4:31–5:17, Figs. 7–9, 11. Payne’s CMOS device includes a “p-channel device [that] includes source and drain regions, 21 and 22, respectively, of P+ conductivity type formed with[in] the N surface region, 18” and an “n-channel device [that] includes source and drain regions, 23 and 24, of N+ conductivity type formed within the P surface region 20.” Ex. 1005, 5:21–27, Fig. 10. Payne states that this approach can reduce the spacing between “source and drain regions of adjacent devices” from 12 microns to 5 microns. Ex. 1005, 5:54–6:19, Figs. 12, 13.

2. *Analysis*

a. *Claim 7*

Petitioner argues that Payne would have taught or suggested the limitations of claim 7. Pet. 10–37. As noted above, Patent Owner disagrees. Prelim. Resp. 1–15. We address the parties’ arguments and evidence below.

The preamble of claim 7 recites “[a] semiconductor device comprising.” Ex. 1001, 4:52. Petitioner argues that Payne teaches the preamble, directing us to Payne’s disclosure that “a primary object of [its] invention [is] to provide a CMOS structure and method of manufacture which requires little semiconductor space.” Pet. 13–14 (quoting Ex. 1005, 1:51–54). Patent Owner does not dispute this argument. Thus, Petitioner has shown sufficiently, at this stage of the proceeding, that Payne teaches the preamble of claim 7.

Claim 7 recites “a surface layer.” Ex. 1001, 4:53. Petitioner argues that Payne teaches or suggests this limitation, and Patent Owner does not dispute this argument. Pet. 14–16. Petitioner directs us to evidence that tends to show that Payne discloses a surface layer similar to that in the ’502 patent. Ex. 1001, Fig. 5(b); Ex. 1003 ¶¶ 76–78; Ex. 1005, 2:50–60, 5:21–27, 6:57–59, Fig. 10; Ex. 1030, 6, 7, 9, 12, 13; Ex. 1033. In particular, Figure 5(b) of the ’502 patent and Payne’s Figure 10 show quite similar structures, and Patent Owner’s district court claim construction brief identified the relevant structure in Figure 5(b) of the ’502 patent as a surface layer. Ex. 1030, 7, 12. Thus, Petitioner has shown sufficiently, at this stage of the proceeding, that Payne teaches this limitation of claim 7.

Claim 7 next recites “a substrate.” Ex. 1001, 4:54. Petitioner argues that Payne teaches this limitation, and Patent Owner does not dispute this argument. Pet. 16–17. Payne discloses fabricating its CMOS device “in a

silicon semiconductor substrate.” Ex. 1005, 1:60–65, 2:50–60, Fig. 10.

Thus, Petitioner has shown sufficiently, at this stage of the proceeding, that Payne teaches this limitation of claim 7.

Claim 7 recites “an active region including a source and a drain, disposed on one surface of said surface layer.” Ex. 1001, 4:55–56. Petitioner argues that Payne teaches this limitation, and Patent Owner does not dispute this argument. Pet. 17–20. Payne discloses forming p-channel and n-channel transistors, each with source and drain regions. Ex. 1005, 1:5–19, 5:18–29, 6:57–59. Petitioner directs us to evidence that a person of ordinary skill in the art would have considered the transistors to be active regions. Ex. 1001, Fig. 5(b); Ex. 1030, 6–7, 11; Ex. 1003 ¶¶ 83–85; Ex. 1008B, 299–300. Thus, Petitioner has shown sufficiently, at this stage of the proceeding, that Payne teaches this limitation of claim 7.

Claim 7 recites “a single drift layer disposed between the other surface of said surface layer and said substrate.” Ex. 1001, 4:57–58. Petitioner argues that Payne discloses or suggests this limitation, and Patent Owner does not dispute this argument. Pet. 21–23. Payne discloses a first tub region with a surface region in it that, on the present record, appears quite similar to the single drift layer and well region of the ’502 patent. *Compare* Ex. 1003 ¶ 89–92; Ex. 1005, 3:28–43, 4:19–39, 5:7–17, 5:44–50, Fig. 10, *with* Ex. 1001, Fig. 5(b); Ex. 1030, 7, 11. Thus, Petitioner has shown sufficiently, at this stage of the proceeding, that Payne teaches this limitation of claim 7.

Claim 7 further recites “said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.” Ex. 1001, 4:58–62. Petitioner first argues the ’502 patent admits that

graded-dopant concentrations were known, and that it was known to grade the dopant concentration in CMOS devices to affect the movement of minority carriers. Pet. 24 (citing Ex. 1001, 1:38–2:9, 2:17–19, Figs. 1, 3(a)–3(d)). Petitioner also argues that Payne teaches or suggests a graded-dopant concentration because Payne’s Figure 11 shows a dopant concentration in tubs 15, 17 that decreases with increasing depth. Pet. 24–26 (citing Ex. 1005, 2:38–41, 2:56–59, 5:14–17, 5:48–57, Figs. 10, 11; Ex. 1003 ¶¶ 94–98). Patent Owner does not dispute these contentions.

Regarding the “first static unidirectional electric drift field to aid the movement of minority carriers” limitation, Petitioner relies on the parent file history and cited references, arguing that “Payne’s downward-sloping graded-dopant concentration aids the movement of minority carriers from the surface layer to the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario.” Pet. 27. In particular, Petitioner directs us to the Patent Owner’s⁸ representation to the Patent Office that “the graded dopant concentration itself creates a *‘built-in’ electrical field* that forces the movement of carriers into a particular direction, whereby *the ‘direction’ of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.*” Pet. 27–28 (quoting Ex. 1040, 289–290 (bold and italics added by Petitioner)). Petitioner also asserts that the direction in which carriers are forced with the concentration profile disclosed in Payne is downward, toward the substrate and away from the surface. Pet. 28–31 (quoting and

⁸ Patent Owner acknowledges that it was the “Applicant” referred to. Prelim. Resp. 3–4.

citing Ex. 1040, 237–238, 253–254, 289–290; citing Ex. 1003 ¶¶ 99–113; Ex. 1005, 5:7–17, 5:44–55; Ex. 1009, 2:11–16, 2:67–3:18, Fig. 2; Ex. 1010, 2:27–32, 5:14–22; Ex. 1013, 431; Ex. 1030, 7, 24; Ex. 1005, Fig. 11).

Patent Owner argues that Petitioner fails to show that Payne discloses the “aid in the movement of minority carriers” claim limitation. Prelim. Resp. 1–11. Specifically, Patent Owner contends that Petitioner incorrectly “assumes that ‘graded dopant concentration’ would *necessarily* ‘aid the movement of minority carriers,’” and thereby effectively reads the “aid the movement of minority carriers” limitation out of the claims. Prelim. Resp. 1–2. Patent Owner also asserts that Petitioner mischaracterizes the statements made during prosecution, and that other evidence in the record “confirms that ‘graded’ does not mean ‘aided.’” Prelim. Resp. 4–9 (emphasis omitted). Additionally, Patent Owner contends that we should reject the testimony from Petitioner’s declarant, Dr. Blalock, because he looked only at the direction of the slope of the graded dopant concentration, i.e., the direction of force acting on the carriers, and not the numerical value of the slope, i.e., the magnitude of the force acting on the carriers, or the presence of other possible forces acting on the carriers. Prelim. Resp. 9–10. Patent Owner contends this approach is flawed because Dr. Blalock failed to determine whether there is a “net force” acting on the carriers to actually aid the movement of carriers in a particular direction. Prelim. Resp. 9–10; Sur-reply 1–2.

After considering the parties’ arguments and information on the present record, we determine that Petitioner has shown sufficiently, for purposes of institution, that Payne discloses or suggests the “first static unidirectional electric drift field to aid the movement of minority carriers” limitation of claim 7.

Contrary to Patent Owner's assertions, Petitioner is not arguing or assuming that "'graded dopant concentrations' equals 'aid carrier movement,'" nor is Petitioner attempting to read out the "aid the movement of minority carriers" element. Prelim. Resp. 2; Prelim. Reply 2–3. Instead, Petitioner presents evidence demonstrating that a graded dopant concentration results in an electric field, which exerts a force on charged particles that will move, or aid movement, of the carriers in a specific direction. Pet. 26–31. For example, Petitioner correctly indicates that during prosecution, Patent Owner stated that "the graded dopant concentration itself creates a 'built-in' electrical field that forces the movement of carriers into a particular direction," and that "this inherent 'built-in' unidirectional field is the additional parameter for ensuring that all minority carriers are being moved in one direction." Ex. 1040, 289–290.

Additionally, Dr. Blalock offered an explanation of the scientific relationship between aiding the movement of carriers and a graded dopant concentration, stating "if you have a downward-sloping graded dopant concentration, we know from the basic physics that that will lead to an electric field and that will create a force, which tends to move the carriers." Ex. 2058, 166:1–6; Ex. 1003 ¶¶ 100–101. This testimony is consistent with the statement in the '502 patent itself that the "relative slope of the donor concentration . . . creates a suitable aiding drift electric field." Ex. 1001, 2:46–49.

Patent Owner attempts to explain away the statements made during prosecution, arguing that it "never said that all graded dopant concentrations aid the movement of minority carriers" and that "Ppetitioner does not quote [Patent Owner's] full statement." Prelim. Resp. 4–5. These arguments, however, are unavailing. Petitioner has accurately quoted the statements

made during prosecution, and those statements speak for themselves. *See* Pet. 27–28; Ex. 1040, 289–290.

As to Patent Owner’s argument that Petitioner and Dr. Blalock improperly restrict their analysis to the direction of the slope in asserting that Payne discloses aiding the movement of minority carriers, we disagree. According to Patent Owner, “a mere downward sloping gradient does *not* necessarily ‘aid the movement of minority carriers’” because “other forces besides a dopant gradient can act on a carrier, and that ‘additional force’ *‘may be larger than the force created by the gradient.’*” Prelim. Resp. 7, 9. (quoting Ex. 2058, 137–138). Patent Owner thus argues that Petitioner and Dr. Blalock fail to provide sufficient evidence to support institution because they do not address the magnitude of the force created by the graded dopant concentration, whether any other forces are acting on the carriers, and the magnitude of those forces. Prelim. Resp. 9–10, 13–15.

Patent Owner’s arguments, however, are inconsistent with the representations it made during prosecution. In particular, during prosecution, Patent Owner argued that a graded dopant concentration creates an electric field that forces the movement of carriers in a particular direction, without any discussion of calculating the numerical magnitude of the slope, whether any other forces are present, or the comparative magnitude of all forces present. *See* Ex. 1040, 289–290. Furthermore, although Patent Owner now directs us to the Examiner’s statement that “movement of minority carriers is affected by multiple forces and fields, . . . it does not appear that simply the presence of a ‘unidirectional drift field’ in itself can achieve ‘drawing all minority carriers from said surface layer to said substrate,’” to support its arguments (*see* Prelim. Resp. 6), Patent Owner previously represented to the Patent Office that it disagreed with the

Examiner's position (Ex. 1040, 289).

Additionally, Patent Owner does not direct us to any discussion in the '502 patent regarding a specific slope value that is necessary to "aid the movement of minority carriers," either in isolation or in the presence of other forces that may act upon the carriers. Nor does Patent Owner direct us to any authority suggesting we should demand more from the prior art disclosure in Payne than is provided in the disclosure of the '502 patent.

In view of this, we determine Petitioner's assertion that Payne discloses a "unidirectional electric drift field to aid the movement of minority carriers" because Payne has a graded dopant concentration is reasonable and sufficient for purposes of institution. There is no evidence on this record that any other forces are present or acting upon the carriers in Payne's system. Prelim. Reply 4 (stating the prior art references "do not contemplate any . . . opposing force,"); Sur-reply 2 (discussing, without disputing, Petitioner's statement). At this stage of the proceeding, we credit Dr. Blalock's testimony that "the graded dopant concentration led to an electric field, which assisted, aided, actually put a little force on the carriers to help them move from the first surface down towards the -- to the second surface of the substrate." Ex. 2058, 72:3–9, 101:12–16 ("I mean, we're talking about graded concentrations and how that leads to an electric field which exerts a force on carriers and so, yeah, those are fundamental aspects of how a semiconductor operates."); Ex. 1003 ¶¶ 99–103. Dr. Blalock's testimony is consistent with, and supported by, other evidence in the record, and disputed only by attorney argument.

For all of the foregoing reasons, Petitioner has shown sufficiently, at this stage of the proceeding, that Payne teaches the "said drift layer having a graded concentration of dopants generating a first static unidirectional

electric drift field to aid the movement of minority carriers” limitation of claim 7.

Lastly, claim 7 recites “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.”

Ex. 1001, 4:63–67. Petitioner contends that Payne’s surface region 18 disposed in tub region 15 is an example of a well region disposed in Payne’s single drift layer, and that this layer has a graded dopant concentration. Pet. 35–38 (citing Ex. 1001, Fig. 5(b); Ex. 1030, 7; Ex. 1005, 1:65–68, 4:31–39, 4:63–5:14, 5:44–55, Figs. 10–11). Petitioner further contends that Payne discloses the recited well region to the same extent as the well region that Patent Owner identifies in Figure 5(b) of the ’502 patent. Pet. 35–36. Patent Owner does not dispute these arguments.

Relying on the same arguments discussed above, including Patent Owner’s arguments during prosecution and in its district court claim construction brief, Petitioner contends that the presence of the downward-sloping graded-dopant concentration in the well region creates a second “static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate.” Pet. 39–41; Ex. 1003 ¶¶ 122–126. Patent Owner likewise relies on the same arguments addressed above. Thus, for the same reasons discussed previously, Petitioner has shown sufficiently, at this stage of the proceeding, that Payne teaches this limitation of claim 7.

Upon review of Petitioner’s arguments and supporting evidence, we determine that Petitioner demonstrates a reasonable likelihood that claim 7 would have been unpatentable as obvious over Payne.

b. *Claim 12*

Claim 12 depends from claim 7 and further recites that “the semiconductor device is an image sensor device.” Ex. 1001, 5:11–12. Petitioner argues that Payne teaches that its techniques can be applied to devices which form “part of an integrated circuit including many other devices.” Pet. 41–42 (quoting Ex. 1005, 2:52-55). According to Petitioner, a person of ordinary skill in the art “would understand one example of such an application would be an image sensor.” Pet. 42 (citing Ex. 1003 ¶ 127). Patent Owner does not dispute these arguments. In view of the foregoing, Petitioner has shown sufficiently, at this stage of the proceeding, that Payne teaches the additional limitation of claim 12.

3. *Conclusion*

Upon review of Petitioner’s arguments and supporting evidence, we determine that Petitioner demonstrates a reasonable likelihood that claims 7 and 12 would have been unpatentable as obvious over Payne.

E. *Claims 9–11 – Alleged Obviousness in view of Payne and Wolf*

Petitioner contends that the subject matter of claims 9–11 would have been obvious in view of the combined disclosures of Payne and Wolf. Pet. 74–79. Patent Owner does not separately dispute or challenge Petitioner’s arguments or evidence beyond the arguments discussed above with regard to Payne. *See* Prelim. Resp. 1–15.

1. *Wolf (Ex. 1008)*

Wolf is a four-volume textbook titled “Silicon Processing for the VLSI Era.” Ex. 1008. A portion of the textbook focuses on CMOS technology. Ex. 1008A, 807–40.

2. Analysis

Petitioner contends that Payne is directed to CMOS devices, and Wolf, which published over 20 years after Payne was filed, teaches “fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS.” Pet. 74–75. According to Petitioner, a person of ordinary skill in the art “would have therefore understood and expected that the teachings of Wolf would apply to Payne, and would have looked to Wolf for advances in CMOS technology and additional process details to the extent not covered in Payne.” Pet. 75.

a. Claim 9

Claim 9 depends from claim 7 and further recites that “the semiconductor device is a central processing unit (CPU).” Ex. 1001, 5:5–6. Petitioner argues that a person of ordinary skill in the art would have “known to fabricate microprocessors (CPUs) using CMOS technology to achieve the benefits of ‘lower power-dissipation’.” Pet. 76 (quoting Ex. 1008B (Wolf), 368–370; citing Ex. 1003 ¶ 197). Petitioner also contends that it would have been obvious to fabricate known CPUs using Payne’s technology to benefit from increased packing density, and that a person of ordinary skill in the art would have had a reasonable expectation of success because “Payne’s twin-well CMOS process was a known improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing known CPUs, designed for implementation using CMOS technology.” Pet. 76 (citing Ex. 1003 ¶¶ 197–201). Petitioner also argues using Payne’s technology to form CPUs involved the combination of familiar elements, according to known methods, to yield predictable results. Pet. 76.

Patent Owner does not present any additional challenges to Petitioner's arguments and evidence. *See generally*, Prelim. Resp.

Upon review of the arguments and prior art of record, we determine that Petitioner demonstrates sufficiently for purposes of institution that Payne and Wolf disclose or suggest the limitations of claim 9, and that a person of ordinary skill in the art would have had reason to combine the teachings of Payne and Wolf, and would have had a reasonable expectation of successfully achieving the claimed invention.

b. *Claim 10*

Claim 10 depends from claim 7 and further recites that “the semiconductor device is a DRAM device.” Ex. 1001, 5:7–8. Petitioner contends that a person of ordinary skill in the art would have

known to fabricate DRAM devices for “the advantages of cost per bit, device density, and flexibility of use (i.e., both read and write operations are possible) [which] have made DRAMs the most widely used form of semiconductor memory to date,” and to do so using CMOS technology to take advantage of “lower power dissipation [] and smaller soft error rates.”

Pet. 77 (quoting Ex. 1008B, 587, 596–597; citing Ex. 1003 ¶ 202).

Petitioner also contends that it would have been obvious to fabricate known DRAM devices using Payne's technology to benefit from increased packing density, and that a person of ordinary skill in the art would have had a reasonable expectation of success because “Payne's improved CMOS process was an improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing a known DRAM designed for implementation using CMOS technology.”

Pet. 77–78 (citing Ex. 1003 ¶¶ 202–205). Additionally, Petitioner argues that using Payne's technology to form DRAMs involved the combination of

familiar elements, according to known methods, to yield predictable results.
Pet. 77–78.

Patent Owner does not present any additional challenges to
Petitioner’s arguments and evidence. *See generally*, Prelim. Resp.

Upon review of the arguments and prior art of record, we determine
that Petitioner demonstrates sufficiently for purposes of institution that
Payne and Wolf disclose or suggest the limitations of claim 10, and that a
person of ordinary skill in the art would have had reason to combine the
teachings of Payne and Wolf, and would have had a reasonable expectation
of successfully achieving the claimed invention.

c. Claim 11

Claim 11 depends from claim 7 and further recites that “the
semiconductor device is a flash memory device.” Ex. 1001, 5:9–10.
Petitioner contends that a person of ordinary skill in the art would have
“known to fabricate semiconductor flash memory devices to achieve the
benefits of ‘high density [], small-die size, lower cost, and hot-electron
writability of EPROMs, together with the easy erasability, on-board
reprogrammability, and electron tunneling erasure features of EEPROMs,’
and to do so using CMOS technology for ‘lower power-dissipation.’”
Pet. 78 (quoting Ex. 1008B, 632–34; Ex. 1008A 808–810; citing Ex. 1003
¶ 206).

Petitioner also contends that it would have been obvious to fabricate
known DRAM devices using Payne’s technology to benefit from increased
packing density, and that a person of ordinary skill in the art would have had
a reasonable expectation of success because “Payne’s improved CMOS
process was an improvement over conventional twin-well CMOS process

and would have been used for its intended purpose in manufacturing a known flash memory designed for implementation using CMOS technology.” Pet. 79 (citing Ex. 1003 ¶¶ 206–210). Additionally, Petitioner argues using Payne’s technology to form DRAMs involved the combination of familiar elements, according to known methods, to yield predictable results. Pet. 79.

Patent Owner does not present any additional challenges to Petitioner’s arguments and evidence. *See generally*, Prelim. Resp.

Upon review of the arguments and prior art of record, we determine that Petitioner demonstrates sufficiently for purposes of institution that Payne and Wolf disclose or suggest the limitations of claim 11, and that a person of ordinary skill in the art would have had reason to combine the teachings of Payne and Wolf, and would have had a reasonable expectation of successfully achieving the claimed invention.

3. Conclusion

Based on the foregoing, we determine that Petitioner demonstrates a reasonable likelihood that claims 9–11 would have been unpatentable as obvious over Payne and Wolf.

Because Petitioner has demonstrated a reasonable likelihood that at least one challenged claim of the ’502 patent is unpatentable over the prior art of record, we institute an *inter partes* review. And because we find some grounds sufficient for institution, we institute on all grounds in the petition. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1353 (2018) (“The agency cannot curate the claims at issue but must decide them all.”); *see also PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute as requiring “a simple yes-or-no institution choice respecting a

petition, embracing all challenges included in the petition”). Nevertheless, in order to further guide the parties after institution, we provide the following observations.

F. Claims 7–12 – Alleged Obviousness in view of Sakai and Kawagoe

Petitioner contends that the subject matter of claims 7–12 would have been obvious in view of the combined disclosures of Sakai and Kawagoe. Pet. 43–74. In addition to the arguments discussed above, Patent Owner asserts that Petitioner’s Sakai and Kawagoe-based arguments are deficient. Prelim. Resp. 1–13.

1. Sakai (Ex. 1006)

Sakai “relates to . . . a CMOS, in which an isolation region between two well regions of opposite conductivity types, each including an insulated gate field effect transistor . . . , is made very small in size to make possible a high-speed operation and large scale integration.” Ex. 1006, 1:7–13. According to Sakai, “[i]n a conventional device . . . , in order to prevent the punch through and short channel effect,” doped regions must be placed at least “several micrometers” apart, “which makes it difficult to increase the packing density of CMOS.” Ex. 1006, 1:26–43. To increase the packing density, Sakai describes a process in which the CMOS is formed in “a double well structure, in which” shallow wells are formed within deep wells, and source and drain regions are formed within the shallow wells. Ex. 1006, 1:55–2:5.

2. Kawagoe (Ex. 1007)

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device using an epitaxial wafer, i.e., a semiconductor wafer having a semiconductor single crystal epitaxial layer grown over a polished

semiconductor substrate. Ex. 1007, 1:13–27, 2:31–35. According to Kawagoe, “[t]he epitaxial wafer is advantageous in that it is excellent in suppressing the soft errors and resisting to the latchup,”⁹ and also has “excellent breakdown characteristics” that “drastically reduce the defect density of the gate insulating film” of a semiconductor integrated device. Ex. 1007, 1:33–40.

Kawagoe discloses various “representative” processes, including processes in which the single crystal (epitaxial) layer contains an impurity of the same type and in the same concentration as the substrate body.

Ex. 1007, 2:55–3:9. According to Kawagoe, the impurity concentration of the substrate body can be made higher than that of the epitaxial layer “so that the resistance of the semiconductor substrate body can be relatively lowered to improve the resistance to the latchup.” Ex. 1007, 4:1–8.

Kawagoe discloses a process for manufacturing a semiconductor integrated circuit device including a step of forming a semiconductor region (well) extending below the epitaxial layer and having an impurity concentration that decreases with increasing depth below the epitaxial layer. Ex. 1007, 3:10–25. According to Kawagoe, the well can be used for forming a complementary Metal-Oxide-Semiconductor Field-Effect Transistor (“MOS.FET”) circuit. Ex. 1007, 3:32–38.

⁹ Petitioner submits Exhibit 1013 (Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Int’l Conf on VLSI Design, 429–434, IEEE 2008), which explains that “soft errors” are “random and not related to permanent hardware faults” and “[t]heir causes may be internal (e.g., interconnect coupling) or external (e.g., cosmic radiation),” including “alpha particles [that] are emitted when the nucleus of an unstable isotope decays to a lower energy state.” Ex. 1013, Abstract, 430.

FIG. 23

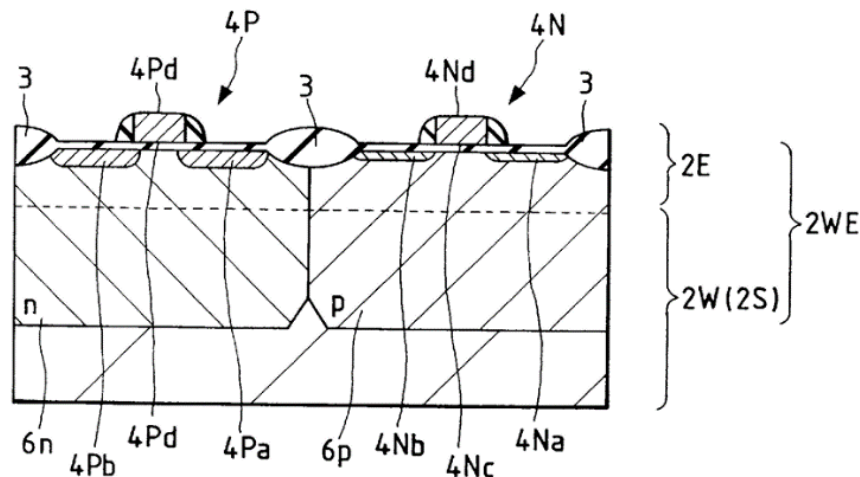


Figure 23 shows a step in a process for manufacturing the semiconductor integrated circuit device of Embodiment 4, including p-well 6p formed with nMOS 4N and n-well 6n formed with pMOS 4P. Ex. 1007, 6:1–4, 15:26–32, 18:3–35. Substrate body 2S and epitaxial layer 2E are doped with p-type impurity, and the impurity concentration of substrate body 2S is higher than that of epitaxial layer 2E “to improve the resistance to the latchup.”

Ex. 1007, at 14:64–15:6, 15:13–17, 16:16–21, 19:59–63, Fig. 17. In Embodiment 4, the impurity concentration in p-well 6p and n-well 6n decreases with increasing depth below the epitaxial layer. Ex. 1007, 15:62–16:15, 17:55–61, Fig. 17. Kawagoe discloses that the concentration gradient reduces soft errors by attracting carriers (electrons) to the substrate and preventing them from entering the p-well. Ex. 1007, 16:2–11.

Petitioner relies on Kawagoe Figure 17, which is reproduced below and illustrates properties of the semiconductor device of Embodiment 4.

FIG. 17

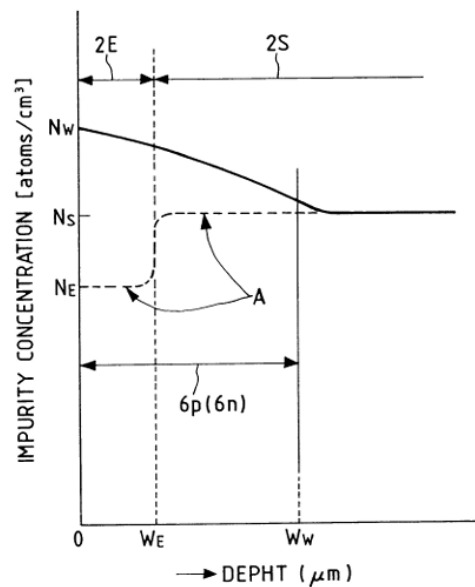


Figure 17 is a plot of impurity concentration as a function of depth in a semiconductor integrated circuit device, which shows “the p-well $6p$ and n-well $6n$ have their impurity concentrations gradually lowered in the depthwise direction from the principal surface (having an impurity concentration N_w) of the epitaxial layer $2E$.” Ex. 1007, 5:41–45, 15:62–16:40.

3. Analysis

Petitioner presents arguments and evidence in support of its contention that Sakai and Kawagoe disclose or suggest each limitation of claim 7, and that a person of ordinary skill in the art would have had reason to combine the teachings of the references. Pet. 43–68. At this stage, Patent Owner disputes only Petitioner’s contention that Sakai and Kawagoe disclose or suggest the “aid the movement of minority carriers” claim limitation. Prelim. Resp. 1–13.

As noted above, because we have determined we will institute, we do not need to resolve this issue now. Nevertheless, we provide the following comments to guide the parties.

Petitioner contends that the combined teachings of Sakai and Kawagoe disclose or suggest a single drift layer having a downward-sloping dopant concentration, similar to what is shown in Kawagoe Figure 17. Pet. 52–59. Similar to its arguments regarding Payne discussed above, Petitioner contends that in light of Patent Owner’s representations to the Patent Office, Sakai-Kawagoe’s graded dopant concentration creates a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Pet. 60–62 (citing Ex. 1007, FIG.17; EX1003 ¶¶ 167–170). Petitioner also notes that Kawagoe teaches that its graded dopant profile causes carriers to move to the substrate. Pet. 58 (citing Ex. 1007, 16:2–11, 21:20–23).

In addition to the arguments discussed above with regard to Payne, Patent Owner argues that Kawagoe does not disclose aiding the movement of carriers, but rather inhibiting carrier movement, because Kawagoe states that the concentration gradient “prevent[s] [electrons] from entering the p-well.” Ex. 1007, 16:7–11; Prelim. Resp. 6, 12–13.

In response, Petitioner contends that “the electric field in Kawagoe **both** helps carriers move from the active regions to the substrate (as in the challenged claims), **and** prevents carriers moving from the substrate to the p-well (as called out in Kawagoe).” Prelim Reply 7. Petitioner presents testimony from Dr. Blalock in support of this position. Prelim. Reply 6–7 (citing Ex. 2058, 150:11–151:3). Additionally, Petitioner contends that “[f]or a semiconductor device as in Kawagoe to operate, there must be carriers in the active region. And the electric field from Kawagoe’s graded

concentration would impact carriers both in the substrate and anywhere in the graded dopant region.” Prelim. Reply 7.

Patent Owner does not dispute that Kawagoe’s transistor has carriers in the active region. *See* Prelim. Sur-reply 6. Nor does Patent Owner meaningfully dispute that Kawagoe has a graded dopant concentration in the active region. *See generally* Prelim. Resp.; Prelim. Sur-reply. In addition, Kawagoe states that carriers are “attracted to the substrate body . . . by that concentration gradient.” Ex. 1007, 16:7–9. Based on this undisputed evidence, coupled with Patent Owner’s statement during prosecution that a “graded dopant concentration itself creates a ‘built in’ electrical field that forces the movement of carriers in a particular direction,” and that “this inherent ‘built-in’ unidirectional electric field is the additional parameter for ensuring that all minority carriers are being moved in one direction” (Ex. 1040, 289–290), we determine that the weight of the evidence on the present record favors Petitioner. The parties, however, are invited to further develop the evidence and arguments relevant to this issue during the course of this proceeding.

G. Timeliness of the Petition Under 35 U.S.C. § 315(b)

Pursuant to 35 U.S.C. § 315(b), “[a]n inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent.” Patent Owner argues that the Petition should be dismissed because it is untimely. Prelim. Resp. 16. In particular, Patent Owner argues that Petitioner is in privity with [REDACTED] (collectively “Licensees”),

who Patent Owner asserts are time-barred under 35 U.S.C. § 315(b) and licensed under the '502 patent. Prelim. Resp. 24–35.

Patent Owner advances several theories supporting its privity arguments, including that Petitioner serves as an “agent” of Licensees by exercising their “have made” rights under the license, that Petitioner is a beneficiary of the Licensee’s agreements related to accused products, that Petitioner and Licensees “are ‘preceding and succeeding owners of’ the licensed and/or infringing products,” that Petitioner’s licensed sales encumber otherwise infringing articles, and “Petitioners apparently indemnify the time-barred parties” for custom-made products. Prelim. Resp. 16–36.

1. *Legal Standard*

Patent Owner does not assert that Petitioner was a party to, or named as a real party-in-interest in any prior lawsuit involving the '502 patent. “A person who is not a party to a suit generally has not had a ‘full and fair opportunity to litigate’ the claims and issues settled in that suit.” *Taylor v. Sturgell*, 553 U.S. 880, 892 (2008). Thus, in general, Petitioner should not be precluded from addressing the unpatentability of a patent based on the filing of previous lawsuits involving [REDACTED]. *See id.* (explaining that, in general, one is not bound by a judgment “in which he is not designated as a party or to which he has not been made a party by service of process”); *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319 (Fed. Cir. 2018) (noting the “general rule against nonparty preclusion”). This rule is deeply-rooted in the “historic tradition that everyone should have his own day in court.” *Taylor*, 553 U.S. at 892–93 (quoting *Richards v. Jefferson County*, 517 U.S. 793, 798 (1996)).

An exception to this deeply-rooted rule exists for parties that are in privity with a defendant in an earlier litigation. *See WesternGeco*, 889 F.3d at 1319 (noting that “the standards for the privity inquiry must be grounded in due process”). The Supreme Court in *Taylor* identified considerations where nonparty preclusion would be justified, including:

- (1) an agreement to be bound; (2) pre-existing substantive legal relationships between the person to be bound and a party to the judgment (e.g., “preceding and succeeding owners of property”); (3) adequate representation by someone with the same interests who was a party (e.g., “class actions” and “suits brought by trustees, guardians, and other fiduciaries”); (4) assumption of control over the litigation in which the judgment was rendered; (5) where the nonparty to an earlier litigation acts as a proxy for the named party to relitigate the same issues; and (6) a special statutory scheme expressly foreclosing successive litigation by nonlitigants.

Id. (citing *Taylor*, 553 U.S. at 894–95).

As this list of considerations indicates, “the mere existence of some relationship between a petitioner and another entity is not sufficient” to place that petitioner in privity with that entity. *Google LLC v. DDC Technology, LLC*, IPR2023-00707, Paper 27 at 37 (PTAB Oct. 25, 2023). Instead, “that relationship must be related to [an earlier] lawsuit and be sufficiently close that it can be fairly said the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit,” or the evidence must demonstrate “that petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation.” *Id.*; *WesternGeco*, 889 F.3d at 1319; *see also Ventex Co. v. Columbia Sportswear North America, Inc.*, IPR2017-00651, Paper 148, at 10, 12 (PTAB Jan. 24, 2019) (precedential) (finding privity where the two parties “had a specially structured, preexisting, and well established

business relationship with one another, including indemnification and exclusivity arrangements”).

A petitioner’s “initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner.” *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1244 (Fed. Cir. 2018). In order to raise such a dispute, “a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privy].” *Id.* The amount of evidence a patent owner must produce does not rise to the level of that required to overcome a burden of production. *Id.* at 1244 n.8. One potential formulation of the amount of evidence required is “evidence that ‘reasonably brings into question the accuracy of a petitioner’s’” assertion that it is not time-barred. *Id.* (quoting *Atlanta Gas Light v. Bennett Regulator Guards, Inc.*, IPR2013-00453, Paper 88 (PTAB Jan. 6, 2015) (addressing the amount of evidence required from a patent owner to question a petitioner’s identification of the real parties-in-interest)). Although the “burden remains with the petitioner to establish” the timeliness of its petition, it need not respond until the patent owner reasonably brings into question the accuracy of its assertion that it is not time-barred. *Id.* at 1242.

2. *Whether we May Consider Petitioner’s Preliminary Reply*

As noted above, we authorized Petitioner to file a Preliminary Reply and Patent Owner to file a Preliminary Sur-reply. Patent Owner argues that Petitioner’s Preliminary Reply is not appropriate because Petitioner “could have reasonably foreseen” Patent Owner’s untimeliness arguments when filing its Petition because “Greenthread and Petitioner were actively litigating essentially the same privity issues in IPR2023-01242,

IPR2023-01243, and IPR2023-01244 at the time the instant petition was filed,” and therefore “Petitioner’s decision not to address the privity issues in its petition was a deliberate choice.” Prelim. Resp. 37.

We disagree with Patent Owner’s argument. According to the Federal Circuit, a petitioner’s “initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner.” *Worlds*, 903 F.3d at 1244. Thus, there is no requirement that a petitioner preemptively address a disputed issue of privity in its petition.

Despite the treatment of privity issues in IPR2023-01242, IPR2023-01243, and IPR2023-01244, Petitioner is not required to address potential arguments that Patent Owner may raise in its Preliminary Response. This is especially true where Patent Owner’s assertions of privity, for the reasons set forth below, are not sufficient to reasonably call into question Petitioner’s assertion that the Petition is timely.

Accordingly, we consider Petitioner’s Preliminary Reply, as well as Patent Owner’s Preliminary Sur-Reply, in determining whether Petitioner has shown its Petition is timely.

3. The Effect of the Earlier Suits Against [REDACTED] on the Timeliness of the Present Petition

Patent Owner alleges that three non-parties, [REDACTED], are time-barred under § 315(b). Prelim. Resp. 22–23.

As to [REDACTED], the present record does not contain any evidence tending to show that this is the case. There is no evidence, on the present record, that [REDACTED] was served with a complaint any earlier than [REDACTED], which is less than one year before the filing of the Petition on December 11, 2023. *Compare* Pet. 94, *with* Ex. 2009 (cited at Prelim. Resp. 17).

Accordingly, the service of an infringement complaint on [REDACTED] does not, on the present record, render [REDACTED] time-barred under § 315(b).¹⁰

Patent Owner argues that because [REDACTED] was served with an infringement complaint early enough to create a time bar, and because [REDACTED] was a real party-in-interest of [REDACTED] in that infringement case, [REDACTED] is time-barred under § 315(b). Prelim. Resp. 23–24 (arguing that [REDACTED] is time-barred because it “was a real-party-in-interest to the [REDACTED] litigation”). We are presented with no authority, however, for extending the time bar of Section 315(b) to a party that may be a real-party-in-interest to a conjectured privity of a petitioner. Thus, Patent Owner has produced no evidence that [REDACTED] is a time-barred entity under § 315(b).

4. [REDACTED] *as Alleged Privies*

In the subsections below, we address Patent Owner’s arguments that [REDACTED] are privies of Petitioner and Petitioner’s real party-in-interest, ON Semiconductor¹¹, under § 315(b).

a. *Agency*

Patent Owner argues that “Petitioner is Licensees’ contractor exercising their rights under the license, including by making accused products on their behalf under the ‘have made’ clause.” Prelim. Resp. 34. Patent Owner argues that “[t]herefore, Petitioner is Licensees’ agent and is in privity with Licensees.” *Id.* at 35. We disagree.

¹⁰ In the next section, we address Patent Owner’s argument that [REDACTED] are privies of Petitioner. Our findings as to [REDACTED] regarding privity provide additional support for our determination that service of a complaint against [REDACTED] does not give rise to a time bar.

¹¹ Petitioner identifies ON Semiconductor Corporation (“ON Semiconductor”) as a real party-in-interest. Pet. 1.

First, Patent Owner's agency argument is not based on the applicable legal standard. For purposes of privity under § 315(b), the relevant question is whether Petitioner is acting as an agent for [REDACTED] in filing a petition for *inter partes* review. The applicable principle is that "preclusion is appropriate when a nonparty later brings suit as an agent for a party who is bound by a judgment." *Taylor*, 553 U.S. at 895. As the Federal Circuit explains, the rationale behind § 315(b)'s time bar is "to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation." *WesternGeco*, 889 F.3d at 1319. Therefore, the relevant question is "whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation." *Id.* Here, Patent Owner does not assert that Petitioner is acting as an agent for [REDACTED] in this proceeding. Any such assertion would be appropriate only based on evidence that at least one of these parties is controlling Petitioner's conduct in the proceeding. *See Taylor*, 553 U.S. at 906 (cautioning that "preclusion is appropriate only if the putative agent's conduct of the suit is subject to the control of the party who is bound by the prior adjudication"). No such evidence is in this record.

Patent Owner argues that to be in privity with the Licensees, what matters is whether the prior action concerned a matter within the agency. Prelim. Resp. 33 (citing *Herrion v. Children's Hosp. Nat. Med. Ctr.*, 786 F. Supp. 2d 359 (D.D.C.), *aff'd*, 448 F. App'x 71 (D.C. Cir. 2011)); *see also* Prelim. Resp. 34 (citing *John Street Leasehold, LLC v. Cap. Mgmt. Res., L.P.*, 283 F.3d 73 (2d Cir. 2002); *Fiumara v. Fireman's Fund Ins. Companies*, 746 F.2d 87 (1st Cir. 1984). Here, Patent Owner's agency argument stems from its contention that it "granted [REDACTED], and

b. *Preceding and Succeeding Owners of Property*

Patent Owner argues that Petitioner and [REDACTED] are “preceding and succeeding owners” of “licensed and/or infringing products.” Prelim. Resp. 27–28 (citing *Taylor*, 553 U.S. at 894). It is true that entities who are “preceding and succeeding owners of property” can be in privity with one another. *Taylor*, 553 U.S. at 894. This rule, however, “is extended or denied in an effort to protect conflicting property interests rather than an effort to implement concepts of participation or representation.” 18A C. Wright, A. Miller, & E. Cooper, Federal Practice and Procedure § 4448 (3d. ed. 2023); *see also id.* at § 4462 (“Successive Property Relationships”) (“There is no independent reason to treat the defeated litigant as the representative of his transferee. Preclusion is limited to the property involved in the judgment.”). As noted above, our relevant analysis is based on the relationships between the parties with respect to the prior proceedings or the Petition (e.g., participation or representation), not on property interests. *See WesternGeco*, 889 F.3d at 1319 (noting that the privity requirement is used “to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation”).

Moreover, the rule related to preceding and succeeding owners of property does not extend to the point where all manufacturers of allegedly infringing goods are in privity with the customers who buy those goods. *See, e.g., id.* at 1319–22 (the parties “had a contractual and fairly standard customer-manufacturer relationship regarding the accused product,” which “does not necessarily suggest that the relationship is sufficiently close that both” parties should be considered to be in privity); *Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1340–41 (Fed. Cir. 2018) (same); *Samsung*

Electronics Co. Ltd. v. Netlist Inc., IPR2022-00615, Paper 64 at 22–26
(PTAB June 30, 2023) (same).

Patent Owner’s evidence that Petitioner’s products are components of Licensees’ products (*see* Prelim. Resp. 28–30) does not come close to suggesting that “it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent” in the prior lawsuit, or that petitioner is serving as a proxy to allow any Licensee to again challenge the patent. *WesternGeco*, 889 F.3d at 1319. Thus, Patent Owner does not present evidence that lends support to a finding that Petitioner’s and Licensees’ status as preceding and succeeding owners of allegedly infringing products renders them privies for purposes of § 315(b).

c. Beneficiaries of License Agreement

Patent Owner argues that Petitioner and Licensees are privies because Petitioner is a “beneficiary” of Patent Owner’s licenses to [REDACTED], which Patent Owner asserts are “directly related to” the accused products. Prelim. Resp. 30–31 (citing *Ventex*, IPR2017-00651, Paper 148). We disagree. Unlike the agreements in *Ventex*, Paper 148 at 12, Patent Owner’s licenses to Licensees are not evidence of a privity relationship between Petitioner and Licensees because Petitioner is not a party to the license agreements. Nor is there any argument that Petitioner is a third-party beneficiary of the licenses.

d. Patent Exhaustion

Patent Owner argues that the doctrine of patent exhaustion gives rise to privity because “after Petitioner sells products under the license, any downstream user of the article sold would have an exhaustion defense against Greenthread.” Prelim. Resp. 31. According to Patent Owner,

“Petitioner is effectively providing rights to third-parties under the license and, therefore, is in privity with Licensees.” Prelim. Resp. 31–32. We disagree. It is true that downstream purchasers and users of Licensees’ products that incorporate products made by Petitioner may have a license (or exhaustion) defense against any claim of infringement by Patent Owner. The relevant question, however, is ultimately whether the relationship between Petitioner and the Licensees is sufficiently close to justify denying Petitioner its day in court. *See Taylor*, 553 U.S. at 892. Patent Owner does not sufficiently explain why a license defense supports such a privity relationship between Petitioner and Licensees.

e. Indemnification

Patent Owner argues that Petitioner’s indemnity obligations support a finding of privity between Petitioner and the Licensees. Prelim. Resp. 32–33. As evidence of this alleged indemnification obligation, Patent Owner argues that Petitioner indemnifies Licensees. Prelim. Resp. 32. Patent Owner also directs us to the indemnification provisions found in Petitioner’s “Standard Terms and Conditions of Sale” agreement. Prelim. Resp. 32. (citing Ex. 2010, 3).

An agreement by a petitioner to indemnify a third party in an earlier infringement suit can give rise to a privity relationship between the petitioner and that third party. *Intel Corp. v. U.S. Int’l Trade Comm’n*, 946 F.2d 821, 839 (Fed. Cir. 1991).

With respect to the ’502 patent, the evidence of record suggests that only [REDACTED] are potentially time-barred. Petitioner’s indemnification provisions are directed to specific products sold by it. Ex. 2010. To the extent that Petitioner’s indemnification provisions could

demonstrate a privity relationship sufficient to deny Petitioner its day in court, it must be with respect to a product it sold to [REDACTED]. The present record, however, does not sufficiently identify any device or component of Petitioner that formed the basis for the previous infringement complaint against [REDACTED]. *See, e.g.*, Ex. 2018, 10–11 (identifying products [REDACTED] was accused of infringing before the district court). As such, we are not persuaded that the indemnification provisions of Petitioner’s “standard sales agreement” are relevant to any relationship with [REDACTED]
[REDACTED]

f. Conclusion as to Timeliness of the Petition

As noted above, privity concerns “whether the petitioner and the prior litigant’s relationship—as it relates to the [earlier] lawsuit—is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit,” or “whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier filed litigation.” *WesternGeco*, 889 F.3d at 1319. A petitioner’s “initial identification of the real parties in interest [and privies] should be accepted unless and until disputed by a patent owner.” *Worlds*, 903 F.3d at 1244. In order to raise such a dispute, “a patent owner must produce *some* evidence that tends to show that a particular [time-barred] third party should be named a [privity].” *Id.* Here, Patent Owner argues that it has produced such evidence in several respects, but, on the present record, none of the evidence in question tends to show that any of the assertedly time-barred Licensees is a privity of Petitioner. Therefore, we find the evidence of record does not

tend to suggest that Petitioner is time-barred under 35 U.S.C. § 315(b), or call into question Petitioner's assertion that the Petition is timely-filed.

IV. CONCLUSION

For the reasons discussed above, we are persuaded on the present record that the Petition is not time-barred under 35 U.S.C. § 315(b). Further, because Petitioner has demonstrated a reasonable likelihood that at least one challenged claim of the '502 patent is unpatentable over the prior art of record, we institute an *inter partes* review. And because we find some grounds sufficient for institution, we institute on all grounds in the petition. *See SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1353 (2018) (“The agency cannot curate the claims at issue but must decide them all.”); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute as requiring “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

At this stage of the proceeding, we have not made a final determination with respect to the patentability of any challenged claim or any underlying factual or legal issue.

V. ORDER

For the foregoing reasons, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), *inter partes* review is instituted with respect to the grounds of unpatentability set forth in the Petition;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, notice is given of institution of trial commencing on the entry date of this Decision;

FURTHER ORDERED that, in view of the pending motion to seal, this Decision is being filed “Board and Parties Only”; and

FURTHER ORDERED that after conferring with Petitioner, Patent Owner shall, within one week of this Decision, submit to the Board via email to Trials@uspto.gov, a version of this Decision to be filed on the public record, with any redactions proposed by either party.

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