

Declaration of Mary K. Bolin
Petition for *Inter Partes* Review of
U.S. Patent No. 8,506,649 B2

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ABSOLUTE SOFTWARE CORP. and ABSOLUTE SOFTWARE, INC.,
Petitioners

v.

SOFTEX LLC,
Patent Owner

U.S. Patent No. 8,506,649 B2
Issue Date: August 13, 2013

Title: ELECTRONIC DEVICE SECURITY AND TRACKING SYSTEM AND METHOD

DECLARATION OF DR. MARY K. BOLIN

I, Mary K. Bolin, declare as follows:

I. INTRODUCTION

1. I am Emeritus Professor at the University of Nebraska, Lincoln Libraries. I have held the following positions: Professor and Catalog and Metadata Librarian, Digital Initiatives and Special Collections Department, University of Nebraska—Lincoln Libraries (2015–2020); Professor and Chair, Discovery and Resource Management and Coordinator of Collection Development, University of Nebraska, Lincoln Libraries (2004–2015); Lecturer, San José State University School of Information: Lecturer, (2008–present); Head of the Technical Services Department, University of Idaho Library (1993–2003; promoted to Professor in 1999); Head of the Cataloging Department, University of Idaho Library (1986–1993; promoted to Associate Professor and tenured in 1991); Head of Records Maintenance Section, Cataloging Department, University of Georgia Libraries (1981–1986).

2. Over the course of my work as a librarian, professor, researcher, student research supervisor, and author of numerous scholarly papers and other publications, I have had extensive experience with cataloging records and online library management systems built around Machine-Readable Cataloging (MARC) standards. I also have substantial experience in authenticating printed documents and establishing the date when they were accessible to ordinarily skilled researchers.

3. Attachment A is my full resume.

4. I have been retained by counsel for Absolute Software Corp. and Absolute Software, Inc. (collectively, “Defendants”) to evaluate, authenticate, and establish the dates of public availability of certain documents in the above-captioned cases. For my

time performing this service, I am being paid my usual hourly fee. I have no financial interest in this litigation, or affiliation with Defendants. My compensation is not dependent upon the outcome of, or my testimony in, this litigation or any other proceeding, including before the U.S. Patent Office.

A. Documents of Interest

- Document 1. Archived at <https://web.archive.org/web/20020802143350/http://www.ztrace.com:80/> is the homepage of the ztrace laptop security system as it appeared on August 2, 2002.
- Document 2. Archived at <https://web.archive.org/web/20020604051951/http://www.ztrace.com:80/zSecuritySuite.asp> is the homepage of the Security Suite software from ztrace as it appeared on June 4, 2002
- Document 3. Archived at https://web.archive.org/web/20050307101451/http://www.ztrace.com/data_sheet/zSecuritySuite.pdf is the datasheet on the ztrace laptop security system security suite as it appeared on March 7, 2005.
- Document 4. Archived at: <https://web.archive.org/web/20020810160306/http://www.ztrace.com:80/zTraceGold.asp> is the homepage of the ztrace Gold software as it appeared on August 10, 2002
- Document 5. Archived at: <https://web.archive.org/web/20020604052039/http://www.ztrace.com:80/zPass.asp> is the homepage of the zpass software as it appeared on June 4, 2002.
- Document 6. Archived at: <https://web.archive.org/web/20020604050748/http://www.ztrace.com:80/zEncrypt.asp> is the homepage of the zEncrypt software as it appeared on June 4, 2002.
- Document 7. Archived at <https://web.archive.org/web/20020810155003/http://www.ztrace.com:80/zControl.asp> is the homepage of the zcontrol software as it appeared on August 10, 2002
- Document 8. Archived at: <https://web.archive.org/web/20020604050138/http://www.ztrace.com:80/zAssetTrack.asp> JennDoc8ExIzassettrack6-4-2002 is the homepage of the zAssetTrack software as it appeared on June 4, 2002.
- Document 9. Archived at: <https://web.archive.org/web/20020613180259/http://www.ztrace.com:80/zTraceWhy.asp> is a page that addresses why to use the ztrace software as it appeared on June 13, 2002.
- Document 10. Archived at: <https://web.archive.org/web/20020405211735/http://www.ztrace.com:80/faq.asp> is the page of FAQs on ztrace as it appeared on April 5, 2002.
- Document 11. Archived at: <https://web.archive.org/web/20021002045822/http://www.ztrace.com:80/guarantee.asp> is the ztrace guarantee page as it appeared on October 2, 2002.

Declaration of Mary K. Bolin
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- Document 12. Archived at:
<https://web.archive.org/web/20020606100347/http://www.ztrace.com/Corporate.asp> is a page with ztrace corporate information as it appeared on June 6, 2002.
- Document 13. Archived at:
<https://web.archive.org/web/20020814065623/http://www.ztrace.com:80/zTraceHow.asp> is a page with ztrace how-to information as it appeared on August 14, 2002.
- Document 14. Archived at:
<https://web.archive.org/web/20020604025540/http://www.ztrace.com:80/AboutzTrace.asp> is a page with information about ztrace corporate information as it appeared on June 4, 2002.
- Document 15. Archived at:
https://web.archive.org/web/20021019100311/http://www.ztrace.com/pr_releases/HpEducational.pdf is a page with a ztrace press release as it appeared on October 19, 2002.
- Document 16. Archived at:
<https://web.archive.org/web/20030820024638/http://www.ztrace.com:80/PressReleases.asp> is a page with a ztrace press release as it appeared on March 8, 2003.
- Document 17. Archived at
https://web.archive.org/web/20040518054736/http://www.ztrace.com/pr_releases/zControl.pdf is a page with a ztrace press release as it appeared on May 18, 2004.
- Document 18. Archived at:
<https://web.archive.org/web/20021201205738/http://ztrace.com:80/PressReleases.asp> is a page with a ztrace press releases as it appeared on December 1, 2002
- Document 19: Archived at:
https://web.archive.org/web/20031006153759/http://www.ztrace.com:80/pr_releases/Yale.pdf is a page with a ztrace press release as it appeared on October 6, 2003
- Document 20. Archived at:
https://web.archive.org/web/200208101ztrace60306/http://www.ztrace.com/data_sheet/zTraceGold.pdf is a page with a ztrace Gold datasheet as it appeared on August 10, 2002
- Document 21. Archived at:
https://web.archive.org/web/20020604052039/http://www.ztrace.com/data_sheet/zPass.pdf is a page with a zPass datasheet as it appeared on June 4, 2002
- Document 22. Archived at:
https://web.archive.org/web/20020604050748/http://www.ztrace.com/data_sheet/zEncrypt.pdf is a page with a zEncrypt datasheet as it appeared on June 4, 2002
- Document 23. Archived at:
<https://web.archive.org/web/20020814064818/http://www.ztrace.com/zControlHow.asp> is a page on how zcontrol works as it appeared on August 14, 2002
- Document 24. Archived at:
<https://web.archive.org/web/20020613175359/http://www.ztrace.com/zControlWhy.asp> is a page on why one should use zcontrol as it appeared on June 13, 2002
- Document 25:
<https://web.archive.org/web/20020613174133/http://www.ztrace.com/zAssetTrackHow.asp> is a page on how zassettrack works as it appeared on June 13, 2002

- Document 26. Archived at:
<https://web.archive.org/web/20020613175056/http://www.ztrace.com/zAssetTrackWhy.asp> is a page on why one should use zassettrack as it appeared on June 13, 2002
- Document 27. Archived at: <https://archive.org/details/windowsxpunleash00ogle/page/24/mode/2up?q=requirements> is a book on Windows XP as it appeared on June 13, 2003
- Document 28. *386 DX microprocessor hardware reference*, written and published by Intel in 1990.
- Document 29. *Operating systems :design and implementation* by Andrew S. Tanenbaum. Prentice – Hall 1987.
- Document 30. Goronkin, Herb, and Yang Yang. "High-performance emerging solid-state memory technologies." *MRS bulletin* 29, no. 11 (2004): 805-813.
DOI: <https://doi.org/10.1557/mrs2004.232>
- Document 31. Bez, Roberto, Emilio Camerlenghi, Alberto Modelli, and Angelo Visconti. "Introduction to flash memory." *Proceedings of the IEEE* 91, no. 4 (2003): 489-502.
- Document 32. Comer, Douglas. *Operating system design: the Xinu approach, Linksys version*. CRC Press, 2011.
- Document 33. Archived at:
<https://web.archive.org/web/20021201205738/http://ztrace.com:80/PressReleases.asp> is the homepage of ztrace technologies as it appeared on August 11, 2003.
- Document 34. Archived at:
<https://web.archive.org/web/20030811223300/http://www.ztrace.com:80/zControl.asp> is the webpage of zcontrol software as it appeared on August 11, 2003.
- Document 35. Baig, Edward C. *CyberSpeak: Unlock the secrets of security for your laptop*, USA Today, April 9 2002. Archived at:
<https://web.archive.org/web/20060504120338/http://www.usatoday.com:80/tech/columnist/2002/04/10/baig.htm> is an article on laptop security from *USA Today* as it appeared on May 4, 2006.
- Document 36. Archived at:
<https://web.archive.org/web/20021025034410/http://www.ztrace.com/sites/yahoo50/yil.com.html> is a page on the ztrace website that refers to *Yahoo Internet Magazine URL Guide* from July 2002, as it appeared on October 25, 2002.

B. Methodology

5. I searched each of these documents in the archive.org “Wayback Machine,” and in the case of Document 27, 28, and 29, in the OCLC database and the online library catalogs of institutions who have these books in their collections.

6. *Use of MARC Records*. The “Machine Readable Cataloging” standard, also known as “MARC,” is an industry-wide standard method of organizing library catalog

information. The Library of Congress first developed MARC in the 1960s. A MARC-compatible library is one that has a catalog consisting of individual MARC records for each of its works. Today, MARC is the primary communication protocol for the transfer and storage of bibliographic metadata in libraries.

7. OCLC is a database of MARC records used by libraries worldwide. When an OCLC-participating institution acquires a work, it creates a MARC record for this work in its computer catalog system, and OCLC automatically supplies the date of creation. The MARC record creation date reflects the date on which (or shortly after) the item was first acquired and catalogued. Once the MARC record is created by a cataloger at an OCLC-participating member institution, it is instantaneously available to any OCLC-participating members, and, therefore available to the public.

8. A MARC record comprises several fields, each of which contains specific data about the work. Each field is identified by a standardized, unique, three-digit code corresponding to the type of data that follows. For example, a work's title is recorded in field 245, the primary author of the work is recorded in field 100, an item's International Standard Book Number ("ISBN") is recorded in field 020, an item's Library of Congress call number is recorded in field 050, and the publication date is recorded in field 260 or 264 under the subfield "c." If a work is a periodical, then its publication frequency is recorded in field 310, and the publication dates (*e.g.*, the first and last publication) are recorded in field 362, which is also referred to as the enumeration/chronology field. The library that created the record is recorded in field 040 in subfield "a" with a unique library code. When viewing the MARC record online via OCLC's Connexion database, hovering over this code with the mouse reveals the name of the library. I used this method of

“mousing over” the library codes in the OCLC database to identify the originating library for all of the MARC records in this declaration, as well as the “display holdings” command to see a list of libraries that own the item. In the MARC records in the OCLC Connexion database, MARC field 040 contains the OCLC symbols of institutions transcribing, creating, and modifying the record.

9. OCLC was created “to establish, maintain and operate a computerized library network and to promote the evolution of library use, of libraries themselves, and of librarianship, and to provide processes and products for the benefit of library users and libraries, including such objectives as increasing availability of library resources to individual library patrons and reducing the rate of rise of library per-unit costs, all for the fundamental public purpose of furthering ease of access to and use of the ever-expanding body of worldwide scientific, literary and educational knowledge and information.”¹ Among other services, OCLC and its members are responsible for maintaining the WorldCat database (<http://www.worldcat.org/>), which is used by independent and institutional libraries throughout the world. OCLC is the international cooperative to which libraries catalog records and others pay to access MARC records. The MARC records referenced in this declaration, extracted from the OCLC database, were generated in the ordinary course of business. Further, I personally located and downloaded each of these records associated with the documents on which my declaration focuses.

10. OCLC provides its members online access to MARC records through its OCLC Connexion database. When an OCLC member institution acquires a work, it

¹ Third Article, Amended Articles of Incorporation of OCLC Online Computer Library Center, Incorporated (available at <http://www.oclc.org/en-US/membership/councils.html>).

creates a MARC record for this work in its computer catalog system in the ordinary course of its business. MARC records created at the Library of Congress are batch-loaded into the OCLC database through a subscription to MARC Distribution Services daily or weekly. Once the MARC record is created by a cataloger at an OCLC member institution or is tape-loaded from the Library of Congress, it is then made available to any other OCLC members online, and, therefore, made available to the public.

11. When an OCLC member institution creates a new record, OCLC automatically supplies the date of creation for that record. The MARC record creation date reflects the date on which, or shortly after which, the item was first acquired or cataloged.

12. The date of creation for the MARC record appears in the fixed field (008), characters 00 through 05. Field 005 is a 16 digit field that records the Date characters `yyyymmdd` including 4 for the year, 2 for the month, and 2 for the day. The Date entered on file never changes. These dates are automatically supplied by the OCLC system and cannot be changed by the user. When the MARC record is created in OCLC, it is available throughout the world to other libraries and in WorldCat, the public version of OCLC Connexion. Thus, the date of creation of the MARC record by a cataloger at an OCLC member institution reflects when the underlying item is accessible to the public.

13. I searched each of these documents in the archive.org “Wayback Machine,” and in the case of Document 27, 28, and 29, in the OCLC database and the online library catalogs of institutions who have these books in their collections. OCLC, www.oclc.org, is a large shared database used by libraries around the world to create and exchange

cataloging data, using MARC format, which is a universal communications format for that data.

14. For those documents for which there is a record in OCLC, I determined when the record was created and which libraries own the item. I then visited the website of the library or libraries that own the item, searched their library catalog, and determined when the item was added to the library's collection.

15. I am familiar with many online catalogs, databases, and search engines. In preparing for this declaration, I used authoritative information systems such as the above-mentioned WorldCat (<https://www.worldcat.org>), the online catalog of the Library of Congress (<https://catalog.loc.gov>), shared research databases such as Google Scholar, ResearchGate, and CiteSeerX, the online catalog of a number of large research libraries such as the University of Nebraska—Lincoln, as well as subscription databases such as IEEEExplore. These records are identified and discussed in this declaration.

16. I am familiar with the creation and editing of documents in formats that include PDF and html. I have created numerous PDF documents over the last 25 years, using the capabilities of Microsoft Word and Google Documents to either save as a PDF or print to a PDF file. I am very familiar with the Adobe Acrobat software and have used it many times to edit the text of a PDF, to combine multiple documents into one PDF file, and so on. The properties of a PDF document show the date it was created and any subsequent date when it was altered, revised, or edited. These properties can be viewed in Acrobat or Adobe Reader by using the "File > Properties" menu and in a browser window by clicking three dots in the upper right and choosing "Document Properties." The creation date cannot be changed.

17. Likewise, I have created and edited numerous html files, i.e., web pages, over the last 25 years. I have used software such as Dreamweaver and have also edited the html code “by hand.” The PDF documents, e.g., press releases, that are examined in this declaration can be viewed with a web browser and the html source code can be displayed. The information in the source code includes the date that the document was archived, which is also part of the URL for that particular capture. For example, the html source code for Document 15 contains the URL [/web/20021019100311/http://web.archive.org/screenshot/http://www.ztrace.com/pr_releases/HpEducational.pdf](http://web.archive.org/web/20021019100311/http://web.archive.org/screenshot/http://www.ztrace.com/pr_releases/HpEducational.pdf), showing the date of capture and the full location and filename of the PDF file.

A. Document 1

18. The following are my opinions with respect to the authenticity and public availability of Document 1.

1. Authentication of Document 1

19. Document 1 is archived at: <https://web.archive.org/web/20020802143350/http://www.ztrace.com:80/> and is the homepage of the ztrace laptop security system as it appeared on August 2, 2002.

20. Attachment B is a PDF of Document 1 as it appeared on that date

2. Public Availability of Document 1

21. Based on the fact that Document 1 was captured by archive.org on August 2, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

B. Document 2

22. The following are my opinions with respect to the authenticity and public availability of Document 2.

3. *Authentication of Document 2*

23. Document 2 is archived at:

<https://web.archive.org/web/20020604051951/http://www.ztrace.com:80/zSecuritySuite.asp> is the homepage of the Security Suite software from ztrace as it appeared on June 4, 2002.

24. Attachment C is a PDF of Document 2 as it appeared on that date.

4. *Public Availability of Document 2*

25. Based on the fact that Document 2 was captured by archive.org on June 4, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

C. Document 3

26. The following are my opinions with respect to the authenticity and public availability of Document 3.

5. *Authentication of Document 3*

27. Document 3 is archived at:

https://web.archive.org/web/20050307101451/http://www.ztrace.com/data_sheet/zSecuritySuite.pdf is the datasheet on the ztrace laptop security system security suite as it appeared on March 7, 2005. The PDF properties of that document have a creation date of March 27, 2002.

28. Attachment D is a PDF of Document 3 as it appeared on March 7, 2005.

29. Attachment D1 is a screenshot of the PDF properties of Document 3.

6. *Public Availability of Document 3*

30. Based on the fact that the PDF properties of Document 3 show a creation date of March 27, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

D. Document 4

31. The following are my opinions with respect to the authenticity and public availability of Document 4.

7. *Authentication of Document 4*

32. Document 4 is Archived at:

<https://web.archive.org/web/20020810160306/http://www.ztrace.com:80/zTraceGold.asp>

and is the homepage of the ztrace Gold software as it appeared on August 10, 2002.

33. Attachment E is a PDF of Document 4 as it appeared on that date.

8. *Public Availability of Document 4*

34. Based on the fact that Document 4 was captured by archive.org on August 10, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

E. Document 5

35. The following are my opinions with respect to the authenticity and public availability of Document 5.

9. *Authentication of Document 5*

36. Document 5 is archived at:

<https://web.archive.org/web/20020604052039/http://www.ztrace.com:80/zPass.asp> is the

homepage of the zpass software as it appeared on June 4, 2002.

37. Attachment F is a PDF of Document 5 as it appeared on that date.

10. Public Availability of Document 5

38. Based on the fact that Document 5 was captured by archive.org on June 4, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

F. Document 6

39. The following are my opinions with respect to the authenticity and public availability of Document 6.

11. Authentication of Document 6

40. Document 6. Archived at:

<https://web.archive.org/web/20020604050748/http://www.ztrace.com:80/zEncrypt.asp> is the homepage of the zEncrypt software as it appeared on June 4, 2002.

41. Attachment G is a PDF of Document 6 as it appeared on that date.

12. Public Availability of Document 6

42. Based on the fact that Document 6 was captured by archive.org on June 4, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

G. Document 7

43. The following are my opinions with respect to the authenticity and public availability of Document 7.

13. Authentication of Document 7

44. Document 7. Archived at:

<https://web.archive.org/web/20020810155003/http://www.ztrace.com:80/zControl.asp>

is the homepage of the zcontrol software as it appeared on August 10, 2002.

45. Attachment H is a PDF of Document 7 as it appeared on that date.

14. Public Availability of Document 7

46. Based on the fact that Document 7 was captured by archive.org on August 10, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

H. Document 8

47. The following are my opinions with respect to the authenticity and public availability of Document 8.

15. Authentication of Document 8

48. Document 8. Archived at:

[https://web.archive.org/web/20020604050138/http://www.ztrace.com:80/zAssetTrack.as](https://web.archive.org/web/20020604050138/http://www.ztrace.com:80/zAssetTrack.asp)

[p](https://web.archive.org/web/20020604050138/http://www.ztrace.com:80/zAssetTrack.asp) is the homepage of the zAssetTrack software as it appeared on June 4, 2002.

49. Attachment I is a PDF of Document 8 as it appeared on that date.

16. Public Availability of Document 8

50. Based on the fact that Document 8 was captured by archive.org on June 4, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

I. Document 9

51. The following are my opinions with respect to the authenticity and public availability of Document 9.

17. Authentication of Document 9

52. Document 9. Archived at:

<https://web.archive.org/web/20020613180259/http://www.ztrace.com:80/zTraceWhy.asp>

is a page that addresses why to use the ztrace software as it appeared on June 13, 2002.

53. Attachment J is a PDF of Document 9 as it appeared on that date.

18. Public Availability of Document 9

54. Based on the fact that Document 9 was captured by archive.org on June 13, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

J. Document 10

55. The following are my opinions with respect to the authenticity and public availability of Document 10.

19. Authentication of Document 10

56. Document 10. Archived at:

<https://web.archive.org/web/20020405211735/http://www.ztrace.com:80/faq.asp> is the page of FAQs on ztrace as it appeared on April 5, 2002.

57. Attachment K is a PDF of Document 10 as it appeared on that date.

20. Public Availability of Document 10

58. Based on the fact that Document 10 was captured by archive.org on April 5, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

K. Document 11

59. The following are my opinions with respect to the authenticity and public availability of Document 11.

21. Authentication of Document 11

60. Document 11. Archived at:

<https://web.archive.org/web/20021002045822/http://www.ztrace.com:80/guarantee.asp>

is the ztrace guarantee page as it appeared on October 2, 2002.

61. Attachment L is a PDF of Document 11 as it appeared on that date.

22. Public Availability of Document 11

62. Based on the fact that Document 11 was captured by archive.org on October 2, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

L. Document 12

63. The following are my opinions with respect to the authenticity and public availability of Document 12.

23. Authentication of Document 12

64. Document 12. Archived at:

<https://web.archive.org/web/20020606100347/http://www.ztrace.com/Corporate.asp> is a

page with ztrace corporate information as it appeared on June 6, 2002.

65. Attachment M is a PDF of Document 12 as it appeared on that date.

24. Public Availability of Document 12

66. Based on the fact that Document 12 was captured by archive.org on June 6, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

M. Document 13

67. The following are my opinions with respect to the authenticity and public availability of Document 13.

25. Authentication of Document 13

68. Document 13. Archived at:

<https://web.archive.org/web/20020814065623/http://www.ztrace.com:80/zTraceHow.asp>

is a page with ztrace how-to information as it appeared on August 14, 2002.

69. Attachment N is a PDF of Document 13 as it appeared on that date.

26. Public Availability of Document 13

70. Based on the fact that Document 13 was captured by archive.org on August 14, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

N. Document 14

71. The following are my opinions with respect to the authenticity and public availability of Document 14.

27. Authentication of Document 14

72. Archived at:

[https://web.archive.org/web/20020604025540/http://www.ztrace.com:80/AboutzTrace.as](https://web.archive.org/web/20020604025540/http://www.ztrace.com:80/AboutzTrace.asp)

[p](https://web.archive.org/web/20020604025540/http://www.ztrace.com:80/AboutzTrace.asp) is a page with information about ztrace corporate information as it appeared on June 4, 2002.

73. Attachment O is a PDF of Document 14 as it appeared on that date.

28. Public Availability of Document 14

74. Based on the fact that Document 14 was captured by archive.org on June 4, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

O. Document 15

75. The following are my opinions with respect to the authenticity and public availability of Document 15.

29. Authentication of Document 15

76. Document 15. Archived at:
https://web.archive.org/web/20021019100311/http://www.ztrace.com/pr_releases/HpEducational.pdf is a page with a ztrace press release as it appeared on October 19, 2002.

77. Attachment P is a screenshot of Document 15 as it appeared on that date.

30. Public Availability of Document 15

78. Based on the fact that Document 15 was captured by archive.org on October 19, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

P. Document 16

79. The following are my opinions with respect to the authenticity and public availability of Document 16.

31. Authentication of Document 16

80. Document 16. Archived at:
<https://web.archive.org/web/20030820024638/http://www.ztrace.com:80/PressReleases.asp> is a page with a ztrace press release as it appeared on August 20, 2003.

81. Attachment Q is a PDF of Document 16 as it appeared on that date.

32. Public Availability of Document 16

82. Based on the fact that Document 16 was captured by archive.org on August 20, 2003, it would have been publicly available on that date and could have been found by a skilled researcher.

Q. Document 17

83. The following are my opinions with respect to the authenticity and public availability of Document 17.

33. Authentication of Document 17

84. Document 17 .Archived at https://web.archive.org/web/20040518054736/http://www.ztrace.com/pr_releases/zControl.pdf is a page with a ztrace press release as it appeared on May 18, 2004.

85. Attachment R is a PDF of Document 17 as it appeared on that date.

86. The PDF properties of that document show a creation date of July 30, 2003. The properties also show a revision date that is one hour earlier than the creation date. This is a common situation and indicates that the PDF of Document 17 was created sometime between its publication date of January 2003 and July of 2003 and then exported from a computer, website or database and uploaded. When a file is copied or moved, that may result in a new creation date with a “revision” that shows that it was downloaded or copied before being uploaded to a new site.

87. Attachment R is a PDF of Document 17 downloaded from http://www.ztrace.com/pr_releases/zControl.pdf

88. Attachment RA is a screenshot of the PDF properties of Document 17, showing a creation date of July 30, 2003.

34. Public Availability of Document 17

89. Based on the fact that the PDF properties of Document 17 show a creation date of July 30, 2003, it would have been publicly available on that date and could have been found by a skilled researcher.

R. Document 18

90. The following are my opinions with respect to the authenticity and public availability of Document 18.

35. Authentication of Document 18

91. Document 18. Archived at:
<https://web.archive.org/web/20021201205738/http://ztrace.com:80/PressReleases.asp> is a page with a ztrace press releases as it appeared on December 1, 2002.

92. Attachment S is a PDF of Document 18 as it appeared on that date.

36. Public Availability of Document 18

93. Based on the fact that Document 18 was captured by archive.org on December 1, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

S. Document 19

94. The following are my opinions with respect to the authenticity and public availability of Document 19.

37. Authentication of Document 19

95. Document 19: Archived at:
https://web.archive.org/web/20031006153759/http://www.ztrace.com:80/pr_releases/Yale.pdf is a page with a ztrace press release as it appeared on October 6, 2003.

96. The PDF properties of that document show a creation date of August 20, 2003.

97. Attachment T is a screenshot of Document 19 as it appeared on October 6, 2003.

98. Attachment TA is a screenshot of the PDF properties of Document 19, showing a creation date of August 20, 2003.

38. Public Availability of Document 19

99. Based on the fact that the PDF properties of Document 19 show, a creation date of August 20, 2003, it would have been publicly available on that date and could have been found by a skilled researcher.

T. Document 20

100. The following are my opinions with respect to the authenticity and public availability of Document 20.

39. Authentication of Document 20

101. Document 20. Archived at:
https://web.archive.org/web/20020810160306/http://www.ztrace.com/data_sheet/zTraceGold.pdf is a page with a ztrace Gold datasheet as it appeared on August March 19, 2003.

102. Attachment U is a screenshot of Document 20 as it appeared on that date.

40. Public Availability of Document 20

103. Based on the fact that Document 20 was captured by archive.org on March 19, 2003, it would have been publicly available on that date and could have been found by a skilled researcher.

U. Document 21

104. The following are my opinions with respect to the authenticity and public availability of Document 21.

41. Authentication of Document 21

105. Document 21. Archived at:

https://web.archive.org/web/20020604052039/http://www.ztrace.com/data_sheet/zPass.pdf is a page with a zPass datasheet as it appeared on June May 10, 2003.

106. Attachment V is a screenshot of Document 21 as it appeared on that date.

42. Public Availability of Document 21

107. Based on the fact that Document 21 was captured by archive.org on May 10, 2003, it would have been publicly available on that date and could have been found by a skilled researcher.

V. Document 22

108. The following are my opinions with respect to the authenticity and public availability of Document 22.

43. Authentication of Document 22

109. Document 22. Archived at:

https://web.archive.org/web/20020604050748/http://www.ztrace.com/data_sheet/zEncrypt.pdf is a page with a zEncrypt datasheet as it appeared on May 10, 2003.

110. Attachment W is a screenshot of Document 22 as it appeared on that date.

44. Public Availability of Document 22

111. Based on the fact that Document 22 was captured by archive.org on May 10, 2003, it would have been publicly available on that date and could have been found by a skilled researcher.

W. Document 23

112. The following are my opinions with respect to the authenticity and public availability of Document 23.

45. Authentication of Document 23

113. Document 23. Archived at:

<https://web.archive.org/web/20020814064818/http://www.ztrace.com/zControlHow.asp>

is a page on how zcontrol works as it appeared on August 14, 2002.

114. Attachment X is a PDF of Document 23 as it appeared on that date.

46. Public Availability of Document 23

115. Based on the fact that Document 23 was captured by archive.org on August 14, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

X. Document 24

116. The following are my opinions with respect to the authenticity and public availability of Document 24.

47. Authentication of Document 24

117. Document 24. Archived at:

<https://web.archive.org/web/20020613175359/http://www.ztrace.com/zControlWhy.asp>

is a page on why one should use zcontrol as it appeared on June 13, 2002.

118. Attachment Y is a PDF of Document 24 as it appeared on that date.

48. Public Availability of Document 24

119. Based on the fact that Document 24 was captured by archive.org on June 13, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

Y. Document 25

120. The following are my opinions with respect to the authenticity and public availability of Document 25.

49. Authentication of Document 25

121. Document 25 is archived at <https://web.archive.org/web/20020613174133/http://www.ztrace.com/zAssetTrackHow.asp> is a page on how zassettrack works as it appeared on June 13, 2002.

122. Attachment Z is a PDF of Document 25 as it appeared on that date.

50. Public Availability of Document 25

123. Based on the fact that Document 25 was captured by archive.org on June 13, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

Z. Document 26

124. The following are my opinions with respect to the authenticity and public availability of Document 26.

51. Authentication of Document 26

125. Document 26. Archived at: <https://web.archive.org/web/20020613175056/http://www.ztrace.com/zAssetTrackWhy.asp> is a page on why one should use zAssetTrack as it appeared on June 13, 2002.

126. Attachment AA is a PDF of Document 26 as it appeared on that date.

52. Public Availability of Document 26

127. Based on the fact that Document 26 was captured by archive.org on June 13, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

128. Document 27. Archived at:

<https://archive.org/details/windowsxpunleash00ogle/page/24/mode/2up?q=requirements>

is a book on Windows XP as it appeared on June 13, 2012 Attachment BB is a PDF of Document 27 as it appeared on that date.

129. There is a MARC record for Document 27 in OCLC with a creation date of July 10, 2001.

130. There is a MARC record in the online catalog of Brigham Young University with a cataloging date of March 28, 2002.

131. Attachment CC is a MARC record from OCLC for Document 27. It has a record creation date of July 10, 2001.

132. Attachment DD is a PDF of a MARC record from the BYU catalog for Document 27.

53. Public Availability of Document 27

133. Based on the fact that Document 27 was captured by archive.org on June 13, 2012, that there is a MARC record in OCLC with a creation date of July 10, 2001, and a MARC record in the online catalog of Brigham Young University with a cataloging date of March 28, 2002, it would have been publicly available in July of 2001, and no later than March 28, 2002, and could have been found by a skilled researcher.

AA. Document 28

134. The following are my opinions with respect to the authenticity and public availability of Document 28, 386 DX microprocessor hardware reference manual, Intel. Mt. Prospect, Ill.: Intel Corp., 1990.

54. Authentication of Document 28

135. There is a MARC record in OCLC for Document 28 with a creation date of August 9, 1990. There is a MARC record in the online catalog of the Indiana University – Purdue University Indianapolis Library with a creation date in the 005 field of June 4, 1997.

136. Attachment EE is a MARC record from OCLC for Document 28. It has a record creation date of August 9, 1990.

137. Attachment FF is a screenshot of the MARC record from the IUPUI library, showing a creation date of June 4, 1997.

55. Public Availability of Document 28

138. Based on the fact that there is a MARC record in OCLC for Document 28 with a creation date of August 9, 1990, and a MARC record in the online catalog of the IUPUI library with a cataloging date of June 4, 1997, it would have been publicly available in August 1990, and no later than June 1997, and could have been found by a skilled research.

BB. Document 29

139. The following are my opinions with respect to the authenticity and public availability of Document 29, *Operating systems: design and implementation* by Andrew S. Tanenbaum. Prentice – Hall 198760.

56. Authentication of Document 29

140. There is a MARC record in OCLC for Document 29 with a creation date of July 16, 1986. There is a MARC record in the online catalog of Brigham Young University with a creation date of August 27, 1997. Attachment GG is a MARC record from OCLC for Document 29.

141. Attachment HH is a MARC record for Document 29 from the BYU library, showing a creation date of August 27, 1997.

57. Public Availability of Document 29

142. Based on the fact that there is a MARC record in OCLC for Document 29 with a creation date of July 16, 1986, and a MARC record in the online catalog of the BYU library with a cataloging date of August 27, 1997, it would have been publicly available in July 1986, and no later than August 1997, and could have been found by a skilled researcher.

CC. Document 30

143. The following are my opinions with respect to the authenticity and public availability of Document 30, Goronkin, Herb, and Yang Yang. "High-performance emerging solid-state memory technologies." *MRS bulletin* 29, no. 11 (2004): 805-813. DOI: <https://doi.org/10.1557/mrs2004.232>.

58. Authentication of Document 30

144. There is a MARC record in OCLC for the print version of the *MRS Bulletin*, the print journal where Document 30 was published in 2004 Document 30 with a creation date of July 2, 1985. Many libraries have indicated ownership of this print journal, which is now available online as well. The online version of the journal is found in both the Cambridge and Springer journal databases, with an online publication date of 2011;

however, Indiana University Libraries catalog lists the print version of the journal, and lists the volumes it owns, which includes volume 29, from 2004, which contains Document 30.

145. Attachment II is a MARC record from OCLC for Document 30.

146. Attachment JJ is a record for Document 30 from the Indiana University library, listing print volumes that include volume 29, 2004.

59. Public Availability of Document 30

147. Based on the fact that there is a MARC record in OCLC for Document 30 with a creation date of July 2, 1985, and a record in the online catalog of the Indiana University library that lists print holdings including the volume that contains Document 30, it would have been publicly available in when it was published in print in 2004, and could have been found by a skilled researcher.

DD. Document 31

148. The following are my opinions with respect to the authenticity and public availability of Document 31, Bez, Roberto, Emilio Camerlenghi, Alberto Modelli, and Angelo Visconti. "Introduction to flash memory." *Proceedings of the IEEE* 91, no. 4 (2003): 489-502.

60. Authentication of Document 31

149. Document 31 is found in IEEE Xplore with a publication date of April 2003. The PDF properties show a creation date of July 31, 2001.

150. Attachment KK is the IEEE results page from IEEE Xplore for Document 31.

151. Attachment LL the PDF of Document 31, retrieved from IEEE Xplore.

152. Attachment MM is a screenshot of the PDF properties for Document 31, showing a creation date of July 31, 2001.

61. Public Availability of Document 31

153. Based on the fact that Document 31 is found in IEEE Xplore with a publication date of April 2003, and has a PDF creation date of July 31, 2001, Document 31 would have been publicly available in April 2003 and could have been found by a skilled researcher.

EE. Document 32

154. The following are my opinions with respect to the authenticity and public availability of Document 32, Comer, Douglas. *Operating system design: the Xinu approach, Linksys version*. CRC Press 2012.

62. Authentication of Document 32

155. There is a MARC record in OCLC for Document 32 with a creation date of September 20, 2011. There is a MARC record in the online catalog of the Ohio State University Library with a creation date of March 27, 2012.

156. Attachment NN is a MARC record from OCLC for Document 32, showing a creation date of September 20, 2011.

157. Attachment OO is a MARC record for Document 32 from the Ohio State University library catalog, showing a creation date of March 27, 2012.

63. Public Availability of Document 32

158. Based on the fact that there is a MARC record in OCLC for Document 32 with a creation date of September 20, 2011, and a MARC record in the online catalog of

the OSU library with a cataloging date of March 27, 2012, it would have been publicly available no later than March 2012, and could have been found by a skilled researcher.

FF. Document 33

159. The following are my opinions with respect to the authenticity and public availability of Document 33.

64. Authentication of Document 33

160. Document 33. Archived at <https://web.archive.org/web/20021201205738/http://ztrace.com:80/PressReleases.asp> is a page of ztrace technologiespress releases as it appeared on December 1, 2002.

161. Attachment PP is a screenshot of Document 33 as it appeared on that date.

65. Public Availability of Document 33

162. Based on the fact that Document 33 was captured by archive.org on December 1, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

GG. Document 34

163. The following are my opinions with respect to the authenticity and public availability of Document 34.

66. Authentication of Document 34

164. Document 34. Archived at: <https://web.archive.org/web/20030811223300/http://www.ztrace.com:80/zControl.asp> is the webpage of zcontrol software as it appeared on August 11, 2003.

165. Attachment QQ is a screenshot of Document 34 as it appeared on that date.

67. Public Availability of Document 34

166. Based on the fact that Document 34 was captured by archive.org on August 11, 2003, it would have been publicly available on that date and could have been found by a skilled researcher.

HH. Document 35

167. The following are my opinions with respect to the authenticity and public availability of Document 35.

68. Authentication of Document 35

168. Document 35. Baig, Edward C. *CyberSpeak: Unlock the secrets of security for your laptop*, USA Today, April 9 2002. Archived at: <https://web.archive.org/web/20060504120338/http://www.usatoday.com:80/tech/columnist/2002/04/10/baig.htm> is an article on laptop security from *USA Today* as it appeared on May 4, 2006.

169. Attachment RR s a PDF of Document 35 as it appeared on that date.

69. Public Availability of Document 35

170. Based on the fact that Document 35 was captured by archive.org on May 4, 2006, it would have been publicly available on that date and could have been found by a skilled researcher.

II. Document 35

171. The following are my opinions with respect to the authenticity and public availability of Document 35.

70. Authentication of Document 35

172. Document 35. Baig, Edward C. *CyberSpeak: Unlock the secrets of security for your laptop*, USA Today, April 9 2002. Archived at:

<https://web.archive.org/web/20060504120338/http://www.usatoday.com:80/tech/columnist/2002/04/10/baig.htm> is an article on laptop security from *USA Today* as it appeared on May 4, 2006.

173. Attachment RR s a PDF of Document 35 as it appeared on that date.

71. Public Availability of Document 35

174. Based on the fact that Document 35 was captured by archive.org on May 4, 2006, it would have been publicly available on that date and could have been found by a skilled researcher.

JJ. Document 36

175. The following are my opinions with respect to the authenticity and public availability of Document 36.

176. Authentication of Document 36

177. Archived at:

<https://web.archive.org/web/20021025034410/http://www.ztrace.com/sites/yahoo50/yil.com.html> is a page on the ztrace website that refers to *Yahoo Internet Magazine URL Guide* from July 2002, as it appeared on October 25, 2002.

178. Attachment SS s a PDF of Document 36 as it appeared on that date.

72. Public Availability of Document 36

179. Based on the fact that Document 36 was captured by archive.org on October 25, 2002, it would have been publicly available on that date and could have been found by a skilled researcher.

* * *

Declaration of Mary K. Bolin
Inter Partes Review of
U.S. Patent No. 8,506,649 B2

180. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine, imprisonment, or both, under Section 1001 of Title 18 of the U.S. Code. I state under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed this December 6, 2023, in Lincoln, Nebraska.

A handwritten signature in black ink, appearing to read "Mary K. Bolin", is written over a light gray, textured rectangular background.

Mary K. Bolin

Attachment A

Mary K. Bolin, PhD
2433 U Street
Lincoln, Nebraska 68503
mary@marykbolin.com

Mary K. Bolin, PhD

Professor Emeritus
University Libraries
University of Nebraska—Lincoln
mbolin2@unl.edu

Lecturer,
School of Information
San José State University
mary.bolin@sjsu.edu

EDUCATION

PhD, Educational Studies (Educational Leadership and Higher Education), 2007, University of Nebraska

Dissertation: *A Typology and Discourse Analysis of the Status and Appointments of Librarians at Land Grant Universities* (available at digitalcommons.unl.edu)

MA, English, 1999, University of Idaho

Thesis: *Grace: A Contrastive Analysis of a Biblical Semantic Field* (available at digitalcommons.unl.edu)

MSLS, 1981, University of Kentucky

BA, Linguistics, 1976, University of Nebraska—Lincoln

WORK EXPERIENCE

Center for Digital Research in the Humanities. Fellow, 2019- Emeritus, 2020-

University of Nebraska--Lincoln Libraries: Professor and Catalog and Metadata Librarian, Digital Initiatives and Special Collections, 2015-2020. Emeritus, 2020-

University of Nebraska—Lincoln Libraries: Professor and Chair, Discovery and Resource Management, 2004-2015; Coordinator of Collection Development, 2012-2015

University of Idaho Library: Head, Technical Services Department, 1993-2003. Promoted to Professor in 1999

University of Idaho Library: Head, Cataloging Department, 1986-1993. Promoted to Associate Professor and tenured, 1991

University of Georgia Libraries: Head, Records Maintenance Section, Cataloging Department, 1981-1986

Teaching:

San José State University School of Information:

LIBR 281, Metadata. 2009-

LIBR 248, Introduction to Cataloging and Classification. 2013-

LIBR 202, Information Retrieval. 2008-2013

Associate Coordinator, Gateway PhD program, San Jose State University, 2021-2022

American Library Association

Cataloging for Non-Catalogers, Online Continuing Education Course, 2017-

Intermediate Cataloging for Non-Catalogers, Online Continuing Education Course, 2018-

Lyrasis

Webinar on BibFrame, taught twice a year, 2020-

Quick and Clean Cataloging, Parts 1, 2, and 3. 2022-

Independent Study in Idaho

Library Science C415, Technical Services for Small Libraries, 2004-2013

Library Science C416, Library Services to Rural Libraries, 2004-2013

Library Science C422, Use of the School Library, 1999-2013

Library Science C425/525, Organization and Management of Small Libraries,
1988-2013

Library Science C427, Library or Media Center Practicum, 1995-2013

Gateway PhD Program (San Jose State University and Queensland University of Technology).
SJSU supervisor for two PhD students, 2015-

Gateway PhD Program (San Jose State University and Manchester Metropolitan University).
Associate Coordinator, 2021-2022

Consulting

Expert witness for multiple attorneys employed by Wolf, Greenfield & Sacks, P.C.,
Hughes Hubbard & Reed LLP, and other firms. 2017-

Editing

Language and academic editing for [EditSprings](#), a service for international scholars, 2020-

SCHOLARSHIP

Refereed Publications:

(Publications available from [digitalcommons.unl.edu](#))

Pytlík Zillig, Brian, and Mary K. Bolin. (Forthcoming 2023). "Visualization of Semantic Primes
in Texts from Early Modern English Drama." *Journal of the Japanese Association for the Digital
Humanities*.

Bolin, Mary K. (2022). *Refocusing Academic Libraries through Learning and Discourse: The
Idea of a Library*. Chandos/Elsevier.

Bolin, Mary K. (2022). "Academic Libraries and Writing Centers: Collaborations at US Public
Research Universities." *School of Information Student Research Journal*, 11(2). Retrieved from
<https://scholarworks.sjsu.edu/ischoolsrj/vol11/iss2/2>

Bolin, Mary K. (2022). *Refocusing Academic Libraries through Learning and Discourse: The
Idea of a Library*. Oxford, UK: Chandos/Elsevier.

Bolin, Mary K. (2022). "Metadata, Catalog Systems, Linked Data, and the Evolving ILS." In: Sandra Hirsh (Ed.), *Information Services Today: An Introduction*. 3rd ed. New York: Rowman and Littlefield.

Wintermute, Harriet E., and Bolin, Mary K. (2018). "Metadata Generators for Backlog Reduction: Metadata Maker Streamlines Cataloging and Facilitates Transition. *Technical Services Quarterly* 35(2) doi: <https://doi.org/10.1080/07317131.2018.1422879>

Bolin, Mary K. (2018). "Metadata, Catalog Systems, Linked Data, and the Evolving ILS." In: Sandra Hirsh (Ed.), *Information Services Today: An Introduction*. 2nd ed. New York: Rowman and Littlefield.

Bolin Mary K. (2017). *The 21-century Academic Library: Global Patterns of Organization and Discourse*. Oxford: Chandos Publishing. (Chandos Information Professional Series)

Bolin, Mary K. (2017). Linguistics and LIS: A Research Agenda." *SLIS Student Research Journal*, 7:1.
Retrieved from <http://scholarworks.sjsu.edu/slissrj/vol7/iss1/2>

Bolin, Mary K. (2014). "Open Access Web Resources for Library Continuing Education and Training." In S. Hines (Ed.), *Revolutionizing the Development of Library and Information Professionals: Planning for the Future* (pp. 107- 124). Hershey, PA: .
doi:10.4018/978-1-4666-4675-9.ch008.

Bolin, Mary K. (2014). "The Language of Academic Librarianship: The Discourse of Promotion and Tenure. *Advances in Library Administration and Organization* 32.

Bolin, Mary K. "Librarian Status at US Research Universities: Extending the Typology." *Journal of Academic Librarianship* 34:4 (September 2008)

Bolin, Mary K. "A Typology of Librarian Status at Land Grant Universities." *Journal of Academic Librarianship*, 34: 3 (May 2008)220:230.

Bolin, Mary K. "The Library and the Computer Center: Organizational Patterns at Land Grant Universities." *Journal of Academic Librarianship*, 31:1 (2005)

Eckwright, Gail Z. and Mary K. Bolin. "The Hybrid Librarian: The Affinity of Collection Management with Technical Services and the Organizational Benefits of an Individualized Assignment." *Journal of Academic Librarianship*, 27:6 (2001)452:457.

Bolin, Mary K. "Catalog Design, Catalog Maintenance, Catalog Governance," *Library Collections, Acquisitions, and Technical Services*. 24: (2000)53-63.

Bolin, Mary K. "The Collegial Environment and the Functional Organization," *Journal of Library Administration*. 29:2(1999):49-61.

Bolin, Mary K. "Cataloging Environmental Impact Statements and Related Documents," *Resource Sharing and Library Networks*. 14:1(1999): 21-40.

Bolin, Mary K. "Waiting for the Electrician or Someone like Him: Client-Centered Technical Services" Proceedings of the Association of College and Research Libraries National Conference, Nashville, April 1997.

< http://www.ala.org/Content/ContentGroups/ACRL1/Nashville_1997_Papers/Bolin.htm >

Grants:

Electronic Theses and Dissertations. Seed Grant from University of Idaho Office of Research, 2002. Co PI with Gail Z. Eckwright. \$6500.

Interoperability of Metadata for Thematic Research Collections. Grant to the Center for Digital Research in the Humanities from the Institute of Museum and Library Services 2005-2008.

Project Team Member.

http://unlcms.unl.edu/cas/center-for-digital-research-in-the-humanities/projects/pages/iom_files/IOM_Final_Narrative_Report_July_2008.pdf

Other Publications:

Library Philosophy & Practice. Peer-reviewed electronic library science journal. Mary K. Bolin and Gail Z. Eckwright, founders and editors. <http://digitalcommons.unl.edu/libphilprac>

Library Science C415, Technical Services for Small Libraries, through Independent Study in Idaho. 2004.

Library Science C416, Library Services to Rural Libraries, through Independent Study in Idaho. 2004.

Library Science C422, Use of the School Library, through Independent Study in Idaho. Revised 1999.

Library Science C425/525, Organization and Management of Small Libraries through Independent Study in Idaho. Revised 2005.

Library Science C427, Library or Media Center Practicum, Independent Study in Idaho. Revised 1999.

Presentations:

Bolin, Mary K. "BibFrame and the MARC Cataloging Environment: an Introduction." Lyrisis Webinar, June 16, 2020, August 17, 2021.. Recording available <http://lyrisis.adobeconnect.com/paufo9e0dm30/>

Pytlík Zillig, Brian, and Mary K. Bolin. "A Little More than Kin, a Little Less than Kind": the Semantic Field Grace in Early Modern English" Poster Session, Text Encoding Initiative Meeting, Graz, Austria, September 18, 2019

Pytlík Zillig, Brian, and Mary K. Bolin. "Shakespeare and the Enumeration of Semantic Primes." Research Paper Presentation, Text Encoding Initiative Meeting, Tokyo, Japan, September 13, 2018

"Library Philosophy and Practice: Creating and Maintaining an Open-Access E-Journal," Presentation to UNCL meeting (libraries at campuses of the University of Nebraska), Lincoln, Nebraska, March 20, 2008.

Presentation to "Thinking outside the Borders" participants on the open-access electronic journal Library Philosophy and Practice and its role in the international library community. University of Nebraska—Lincoln Libraries, October 24, 2007

Panel discussion on open access electronic journals. GWLA directors' meeting. Linda K. Hall Library, Kansas City, Missouri. April 2007.

"Waiting for the Electrician or Someone Like Him: Client-Centered Technical Services." Association of College and Research Libraries National Conference, Nashville, April 5, 1997.

" 'Some Problems of an Editor': the Idaho Librarian from Manuscript to Published Issue," Joint Annual Conference of the Idaho Library Association and the Washington Library Association, Spokane, Washington, April 6, 1995.

"Automating Idaho's Libraries: a Historical Perspective." Idaho Library Association Annual Conference, Idaho Falls, October 4, 1990.

"Small Library Management." Idaho Library Association Spring Conference, Lewiston, Idaho, May 13, 1989.

"No More 'Good Workers': Excellence and Academic Library Classified Staff." Association of College and Research Libraries 5th Annual Conference, Cincinnati, April 7, 1989.

"Communication to and from Cataloging Departments." Heads of Cataloging Discussion Group, American Library Association Midwinter Meeting, San Antonio, January 1988.

Discussion Leader at the LAMA (Library Administration and Management) Management Exchange. American Library Association Annual Meeting, San Francisco, June 1987.

"Staff Turnover." Heads of Cataloging Discussion Group, American Library Association Midwinter Meeting, Chicago, January 1987.

SELECTED PROFESSIONAL SERVICE

Reviewer. *Resources for College Libraries*. Linguistics bibliography, Spring 2020.

Peer reviewer for ALISE National Conference presentations, Spring 2020.

Peer reviewer for *Journal of Academic Librarianship*, 2012-

Peer reviewer for refereed journal, *Western Nigerian Journal of Medical Sciences* (<http://www.wnjms.org/>), a publication of Ladoke Akintola University of Technology (LAUTECH) Teaching Hospital, 2008-

PhD Reviewer for students from Aligarh Muslim University, India, 2010-

Outside reviewer for numerous library faculty promotion and tenure cases in US universities.

University of Nebraska--Lincoln

Chair, University Libraries Faculty, 2018

Faculty Senate Academic Rights and Responsibilities Committee, 2016- Chair, 2018-19

Faculty Senate – 2004-2008; 2008-2011

Faculty Senate Executive Committee 2004-2008

Academic Planning Committee (APC), 2005-2008; Vice Chair, 2006-2007; Chair, 2007-2008

Aesthetic Review Committee 2006-2007

APC monitor for academic program reviews: Department of Political Science, 2005;
Department of Educational Psychology 2006
Pacific Northwest Library Association:

Editor, *PNLA Quarterly*, December 2002-December 2013

Idaho Library Association:

Editor, *The Idaho Librarian*, September 1990-January 1996

Attachment B

The Wayback Machine - <https://web.archive.org/web/20020802143350/http://www.ztrace.com:80/>



What if YOUR laptop gets stolen?

2 August 2002

Login name

Password

NEWS

zHome **Get It Now!** **News** **Question Desk** **zLab** **Media Room** **zTrace Corporate**

zTRACE GOLD **zCONTROL** **zPASS** **zASSET TRACK** **zENCRYPT** **zSECURITY SUITE**

Welcome to zTrace!
The invisible laptop security system



Tell-a-Friend
Register now!

Privacy at zTrace
zGuarantee

GET zTrace NOW

reviewed by **TRUSTe** site privacy statement



TechTV Cybercrime
zTrace featured on TechTV Cybercrime



Hewlett-Packard
zTrace selected for HP Educational Program



www.zTrace.com

Copyright © 1999-2002 zTrace, Inc. All rights reserved.
Use of this Web site constitutes acceptance of the zTrace Use Agreement and **Privacy Policy**.

Attachment C

The Wayback Machine - <https://web.archive.org/web/20020604051951/http://www.ztrace.com:80/zSecuritySuite...>



4 June 2002

Login name

Password

zHome	Get It Now!	News	Question Desk	zLab	Media Room	zTrace Corporate
ZTRACE GOLD	ZCONTROL	ZPASS	ZASSET TRACK	ZENCRYPT	ZSECURITY SUITE	

zSecurity Suite



What Is It?

ZTRACE ZSECURITY SUITE is a comprehensive set of software applications that aids in the recovery of stolen or missing computers, protects sensitive data in case of unauthorized access and effectively monitors hardware and software assets for tracking.

ZTRACE ZSECURITY SUITE is comprised of ZTRACE GOLD, PASS, ZENCRYPT, ZCONTROL and ZASSET TRACK. Collectively, these applications provide the optimum wrap around security solution for your organization's mobile computing fleet. ZAGENT is the stealth core platform that provides integration and interface controls for the ZTRACE ZSECURITY solution and offers extensible functionality for tight integration with future components. There are no icons, files, directories, sounds or ANYTHING visible on the computer, providing total invisibility to the user.



Why Do You Need It?

ZTRACE ZSECURITY SUITE affords single installation of the ZTRACE circle of complete mobile care-integrated software for tracing and recovery, data protection and encryption, and asset management. More importantly, integrated functionality enhances an enterprise's protection against the current menace of laptop misuse both outside and inside its walls. The special capabilities of zAGENT technology, together with a unique recovery service staffed by the ZTRACE Recovery Team, equip a mobile computing fleet of laptops and computers with security measures that wrap themselves around the entire mobile-security problem. With the FBI itself a victim of laptop theft, it is time to protect against theft, recover critical data and equipment and to fully monitor the computing fleet.

How Does It Work?

Protect.

Secure your entire machine so that if an unauthorized user attempts to access it, sensitive data is made completely invisible.

"You can't steal what you can't see."

Alexander Kesler, Founder and President of zTrace

Monitor.

Watch the use patterns of your laptop fleet and concentrate on those running unauthorized applications. Monitor software license compliance and hardware configuration for upgrade paths and lease deadlines.

Recover.

If your computer is out of your direct control, make the data invisible, encrypt it, recover it and then delete it. Your data is critical. And then, since your computer has already identified its location to ZTRACE and with the cooperation of law enforcement and the ZTRACE Recovery Team, physically recover your laptop.

[Download Product Information Sheet](#)



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Attachment D

zSECURITY SUITE™



What Is It?

zTRACE zSECURITY SUITE is a comprehensive set of software applications that aids in the recovery of stolen or missing computers, protects sensitive data in case of unauthorized access and effectively monitors hardware and software assets for tracking.

zTRACE zSECURITY SUITE is comprised of zTRACE GOLD, zPASS, zENCRYPT, zCONTROL and zASSET TRACK. Collectively, these applications provide the optimum wrap around security solution for your organization's mobile computing fleet. zAGENT is the stealth core platform that provides integration and interface controls for the zTRACE zSECURITY solution and offers extensible functionality for tight integration with future components. zTRACE zSECURITY SUITE is a comprehensive set of software applications that aids in the recovery of stolen or missing computers, protects sensitive data in case of unauthorized access and effectively monitors hardware and software assets for tracking.

Lightshot Screenshot

Attachment D1

zSECURITY SUITE™

Document properties

File name: zSecuritySuite.pdf

File size: 100 KB

Title: zSecuritySuite.pdf

Author: andrey

Subject: -

Keywords: -

Created: 3/27/02, 3:35:36 AM

Modified: 3/27/02, 3:35:36 AM

Application: PScript5.dll Version 5.2

PDF producer: Acrobat Distiller 5.0 (Windows)

PDF version: 1.3

Page count: 1

Page size: 8.50 x 11.00 in (portrait)

Fast web view: Yes

Close

What
if YOUR laptop
gets
stolen?



of laptop misuse both outside and inside its walls. The special capabilities of zAGENT technology, together with a unique recovery service staffed by the zTRACE Recovery Team, equip a mobile computing fleet of laptops and computers with security measures that wrap themselves around the entire mobile-security problem. With the FBI itself a victim of laptop theft, it is time to protect against theft, recover critical data and equipment and to fully monitor the computing fleet.

How Does It Work?

Protect.

Secure your entire machine so that if an unauthorized user attempts to access it

Lightshot Screenshot

Attachment E

The Wayback Machine - <https://web.archive.org/web/20020810160306/http://www.ztrace.com:80/zTraceGold.asp>



[zHome](#) [Get It Now!](#) [News](#) [Question Desk](#) [zLab](#) [Media Room](#) [zTrace Corporate](#)

[ZTRACE GOLD](#) [ZCONTROL](#) [ZPASS](#) [ZASSET TRACK](#) [ZENCRYPT](#) [ZSECURITY SUITE](#)

Login name
 Password



[GO](#)

[Privacy at zTrace](#)

[zGuarantee](#)

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zTrace
NOW**

[Get It Now!](#)

What Is It?

ZTRACE GOLD is an invisible software security application that traces the location of missing laptops for recovery.

ZTRACE GOLD is undetectable and unerasable on a laptop's hard drive. The computer completes a handshake with the ZSERVER at every Internet connection. If the laptop is reported missing, a patent pending process occurs for the ZTRACE Recovery Team to identify the computer's exact physical location. The ZTRACE Recovery Team coordinates with local law enforcement for a completely outsourced recovery solution; the entire tracing and monitoring service resides with ZTRACE. For enterprises, ZTRACE GOLD provides a flexible solution that can be managed internally by an organization's own internal security department or outsourced with the ZTRACE Recovery Team.



[Why Do You Need It?](#)
[How Does It Work?](#)



zFlash Clip

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<https://web.archive.org/web/20020810160306/http://www.ztrace.com:80/zTraceGold.asp>

1/1

Absolute Exhibit No. 1034
Page 052

Attachment F

The Wayback Machine - <https://web.archive.org/web/20020604052039/http://www.ztrace.com:80/zPass.asp>



4 June 2002

Login name

Password

zHome	Get It Now!	News	Question Desk	zLab	Media Room	zTrace Corporate
ZTRACE GOLD	ZCONTROL	ZPASS	ZASSET TRACK	ZENCRYPT	ZSECURITY SUITE	

zPass

What Is It?

"You can't steal what you can't see."
Alexander Kesler, Founder and President of zTrace

ZPASS is an invisible password application, based on the ZAGENT core, that detects and triggers specific actions to protect sensitive computer data. Once an unauthorized user fails to enter the required password, ZPASS immediately makes all sensitive files and directories invisible, preventing access to any protected data. At the same time, the computer stays fully functional, fooling the unauthorized user into believing that there is nothing even worth stealing on the machine. Every subsequent keyboard or mouse action is recorded for future identification of search intentions.

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Why Do You Need It?

How Does It Work?

GO

NEWS



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zGuarantee

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Attachment G

The Wayback Machine - <https://web.archive.org/web/20020604050748/http://www.ztrace.com:80/zEncrypt.asp>



4 June 2002

Login name

Password

[zHome](#)[Get It Now!](#)[News](#)[Question Desk](#)[zLab](#)[Media Room](#)[zTrace Corporate](#)[ZTRACE GOLD](#)[ZCONTROL](#)[ZPASS](#)**zEncrypt**

What Is It?

ZENCRYPT is an invisible encryption application that encrypts important computer files. ZENCRYPT works in conjunction with ZTRACE GOLD and/or ZPASS to immediately encrypt all sensitive data on the laptop as soon as an unauthorized-access warning has been received.

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www.zTrace.com

Attachment H

The Wayback Machine - <https://web.archive.org/web/20020810155003/http://www.ztrace.com:80/zControl.asp>



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[ZTRACE GOLD](#) [ZCONTROL](#) [ZPASS](#) [ZASSET TRACK](#) [ZENCRYPT](#) [ZSECURITY SUITE](#)

Login name

Password

[GO](#)



What Is It?

ZCONTROL is an invisible software security application, based on ZAGENT core technology, that retrieves files, deletes sensitive information and maintains data privacy AFTER computer loss.

 [Download Product Information Sheet](#)



[Why Do You Need It?](#)

[How Does It Work?](#)

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Attachment I

The Wayback Machine - <https://web.archive.org/web/20020604050138/http://www.ztrace.com:80/zAssetTrack.asp>



4 June 2002

Login name

Password

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[ZTRACE GOLD](#) [ZCONTROL](#) [ZPASS](#) [ZASSET TRACK](#) [zEncrypt](#) [ZSECURITY SUITE](#)

zAsset Track

What Is It?

ZASSET TRACK is an invisible asset-tracking application that gathers and analyzes hardware and software information about each laptop in the enterprise and stores the data in a centralized server where it can be mined by the corporate administrator.

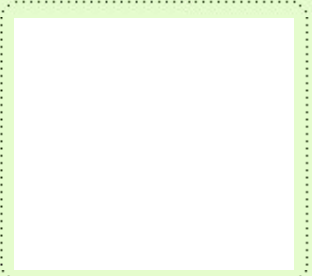
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- ▶ Why Do You Need It?
- ▶ How Does It Work?

GO

NEWS



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Attachment J

The Wayback Machine - <https://web.archive.org/web/20020613180259/http://www.ztrace.com:80/zTraceWhy.asp>



13 June 2002

Login name

Password



- Privacy at zTrace

- zGuarantee



Why Do You Need It?

What if your laptop gets stolen or just turns up missing? The possible scenarios are endless. Imagine coming back from lunch one day and your laptop has simply vanished. Must be an inside job since your office is secure. Even with the increased security at airports, there's still the significant risk someone grabs your computer case instead of his own. Can you really trust the cleaning staff in the hotel or your fellow conference attendees? Have you ever left something in a taxi and tried to get it back?

Any chance you'll ever see your laptop again? Even if you file a police report, how will the physical location of your mobile notebook computer be determined? Up until now, there has been no viable solution. The FBI states that less than 2% of laptops are ever recovered. Over 300,000 laptops were reported stolen last year. Do you want to be one of those statistics?

ZTRACE Technologies recognized the downsides of the wonderful world of mobile computing -- mobility and portability. This all started because ZTRACE's founder found his home burglarized and the thief didn't steal the laptop. That started the "what ifs" that led to the development of ZTRACE GOLD.

[Download Product Information Sheet](#)



- How Does It Work?
- What Is It?

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Attachment K

The Wayback Machine - <https://web.archive.org/web/20020405211735/http://www.ztrace.com:80/faq.asp>



5 April 2002

Login name

Password

zHome

Get It Now!

Question Desk

zLab

Media Room

zTrace Corporate

zQuestion Form

FAQ

Product Support

1. Who is zTrace, Inc?
2. How do I contact zTrace for product and investment information?
3. How does zTrace™ Gold work?
4. What Operating Systems are supported by zTrace?
5. Can zTrace be operational on a dual-boot system?
6. Will software protect only laptops?
7. How do I install zTrace?
8. How long does it take to install zTrace?
9. Do I need to install zTrace applications on each PC individually in an enterprise setting?
10. What happens to my registration information? Is it secure?
11. Can anyone tell if zTrace is protecting my computer?
12. How do I report my computer stolen to activate tracking?
13. What happens if the stolen PC does not connect to the Internet?
14. How am I notified when my computer is found?
15. Can zTrace identify a phone number that is unlisted or using Caller ID blocking?
16. Can the user hear the modem when zTrace makes a call?
17. What happens if the Internet method of connection is changed?
18. Can zTrace work through firewalls to reach the Internet?
19. Can I remove zTrace™? How?
20. Can I unsubscribe from zTrace™ Services?
21. What if I sell my computer and buy a new one?
22. How do I change my PIN number if I forget it?
23. How do I get my password if I forget it?
24. How do I modify my account information?
25. Can zTrace co-exist with anti-virus software?

More Questions?

Just e-mail question@zTrace.com and a member of the zTrace™ staff will respond.

1. Who is zTrace, Inc?

zTrace Technologies is a premier provider of innovative security software and services designed to meet the challenging data security and asset protection demands of today's mobile computing environment. Serving enterprise, government, education, and consumer markets, zTrace is fast-tracked to be the global leader in mobile computing security. For more information about zTrace products, visit www.ztrace.com or telephone (877) zTrace-2

2. How do I contact zTrace for product and investment information?

See <http://www.ztrace.com>. For product information, contact info@zTrace.com and for investment information, contact investor@zTrace.com.

3. How does zTrace™Gold work?

zTrace Gold is an invisible software application that traces a missing laptop's location for recovery. The computer completes a handshake with the zServer at every Internet connection. If the laptop is reported missing, proprietary steps occur for the zTrace Recovery Team to identify the computer's exact physical location and then get it back. Rest easily with zTrace protecting your computer!

4. What Operating Systems are supported by zTrace?

zTrace™ will run on Desktop and Laptop Computers with Windows XP, 2000, ME, 98. 386 DX or higher, 16 MB RAM, 2M HD space.

5. Can zTrace be operational on a dual-boot system?

Yes when used with one of the Windows Operating Systems listed above.

6. Will software protect only laptops?

No. zTrace™ will protect laptops and desktop computers, at home or in the enterprise.

7. How do I install zTrace?

For individual installations, follow the registration and installation wizard on the zTrace web site - please click [here](#).

8. How long does it take to install zTrace?

It takes just a few seconds for an individual installation.

9. Do I need to install zTrace applications on each PC individually in an enterprise setting?

Enterprise installations are managed from a central location and installed invisibly.

10. What happens to my registration information? Is it secure?

Your personal information is held securely at our company location. Our servers are entirely secured, so that your registration details are not available to outside sources on any network or Internet connection. To see our Privacy Policy, click [here](#).

11. Can anyone tell if zTrace is protecting my computer?

There are no icons, files, directories, sounds or ANYTHING visible on the computer, providing total invisibility to the user.

12. How do I report my computer stolen to activate tracking?

You can report the theft by e-mail, telephone or fax, whichever is most convenient for you: call the toll-free number: (877) zTrace-2; send an e-mail to theft-report@zTrace.com, or a fax to (617) 507-6489.

13. What happens if the stolen PC does not connect to the Internet?

zTrace Gold becomes active only when the computer connects to the Internet. As soon as the computer connects, zTrace detects its location. After you file a report, zTrace™ uses the next connection to detect the location of the computer.

14. How am I notified when my computer is found?

The information you entered during registration and specific additional information on the theft report will be used to notify you when your computer is found.

15. Can zTrace identify a phone number that is unlisted or using Caller ID blocking?

zTrace Gold supports intelligent telephone dialing capabilities to trace location through any public or

private phone system, including dial-out prefixes, international calls, and can even capture blocked or unlisted calls through caller ID.

16. Can the user hear the modem when zTrace makes a call?

No - The modem speakers are turned off during the call.

17. What happens if the Internet method of connection is changed?

zTrace works as before! If the method of Internet connection is changed (e.g. cable modem to dial up) - the software is intelligent and determines the best method to connect to the Internet in a stealth fashion. zTrace works with any type of Internet connection, including dial-up, cable modem, DSL, T1 and wireless. It recognizes and traces through both internal and external networks for LAN/WAN configurations to pinpoint actual location of stolen laptop.

18. Can zTrace work through firewalls to reach the Internet?

Yes - the core technology penetrates the majority of firewalls and proxy servers to automatically to provide optimum security in a corporate setting. This increases the chances of tracing and recovery in corporate espionage cases.

19. Can I remove zTrace™? How?

A subscriber can remove the program from his/her computer using a personalized password that can be requested from [here](#).

20. Can I unsubscribe from zTrace™ Services?

Yes, you can unsubscribe from zTrace™ by uninstalling zTrace™ from your computer. If you want the uninstall instructions emailed to you, email us at uninstall@ztrace.com.

21. What if I sell my computer and buy a new one?

zTrace™ will service your new computer. Just resubmit your registration, and your new computer will be zTrace™ protected too. The new owner of your computer will have to subscribe for the service to get zTrace™, or you can simply cancel your subscription with that computer.

22. How do I change my PIN number if I forget it?

Contact support@zTrace.com.

23. How do I get my password if I forget it?

Contact support@zTrace.com.

24. How do I modify my account information?

Log on to the zTrace customer site and select "Update Registration Information".

25. Can zTrace co-exist with anti-virus software?

Absolutely. zTrace operates totally undetected by all known anti-virus programs.

More Questions?

Just e-mail question@zTrace.com and a member of the zTrace™ staff will respond.

Attachment L

The Wayback Machine - <https://web.archive.org/web/20021002045822/http://www.ztrace.com:80/guarantee.asp>

[:: Tell-a-Friend](#)[:: Privacy at zTrace](#) [:: zGuarantee](#) [:: zHome](#)

1 October 2002

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[zTrace Corporate](#) [Contact us](#)



z Guarantee

100% Satisfaction zGuarantee

If your PC or laptop is stolen, zTrace guarantees to locate it within 30 days after it has been reported to zTrace. If it's not found in 30 days and you have zTrace Gold, we will refund the money you have paid us in full.

Your satisfaction is guaranteed.

Login Name

Password

laptop gets stolen?

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Attachment M



6 June 2002

Login name

Password

**Corporate**

Special Deals

We have volume pricing and promotions for Corporations/Small Businesses!

Please fill out the form below so our sales representative can quote you an appropriate rate!

Name:

Organization:

Email Address:

Phone Number:

Fax Number:

Number of Computers to Secure:

Where did you hear about us?

Urgency:

 ☐ Privacy at zTrace☐ zGuarantee**GET
zTrace
NOW**

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Attachment N

The Wayback Machine - <https://web.archive.org/web/20020814065623/http://www.ztrace.com:80/zTraceHow.asp>



zHome	Get It Now!	News	Question Desk	zLab	Media Room	zTrace Corporate
ZTRACE GOLD	ZCONTROL	ZPASS	ZASSET TRACK	ZENCRYPT	ZSECURITY SUITE	

Login name

Password



● Privacy at zTrace

● zGuarantee

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zTrace
NOW**

How Does It Work?

ZTRACE GOLD is installed on the laptop's hard drive and registered with the ZSERVER with a unique identification. Every time the laptop is connected to the Internet, ZTRACE GOLD checks with the ZSERVER to determine the laptop's status. ZTRACE GOLD operates in stealth mode, with no directories, files, icons, or sounds ever appearing on the laptop.

In the event of theft, the owner notifies the ZTRACE Monitoring Center via phone, e-mail, fax, or the Web. The ZSERVER tracking system is activated and waits for the next connection of that laptop to the Internet.

ZTRACE GOLD works with any type of Internet connection, including dial-up, cable modem, DSL, T1 and wireless. It recognizes and traces through both internal and external networks for LAN/WAN configurations to pinpoint actual location of the missing laptop. ZTRACE GOLD supports intelligent telephone dialing capabilities to trace the location through any public or private phone system, including dial-out prefixes, international calls, and can even capture blocked or unlisted calls through caller ID.

When the missing computer connects to the Internet, the stealth application receives a signal from the zSERVER and the computer reports its own location.

 [Download Product Information Sheet](#)



► Why Do You Need It?

► What Is It?

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www.zTrace.com

Attachment O

The Wayback Machine - <https://web.archive.org/web/20020604025540/http://www.ztrace.com:80/AboutzTrace.asp>



3 June 2002

Login name

Password



About zTrace

[Privacy at zTrace](#)[zGuarantee](#)

Mission & Vision

[Company History](#)
[The management team](#)

Today's mobile computing devices-laptops, PDAs, pocket PCs, tablet PCs, and smart wireless phones-are lighter, smaller, more powerful, and can store more data than ever imagined before. These devices are already widely deployed and their continued rapid adoption rate clearly endorses their attractiveness and their value.

Unfortunately, the same attributes that make mobile computing devices so amazingly useful, also make them incredibly susceptible to loss-due to theft or to mishap. For example, it's highly unlikely to not find an individual or business that hasn't suffered from losing a laptop.

Everyday, a remarkable amount of critical, proprietary business information-strategic and tactical-is stored along with private personal data on these devices. The trouble is that the devices and the data are traveling around mostly unprotected, vulnerable to loss or misuse.

ZTRACE has seized the opportunity to solve this problem. Simply put, we provide the "peace of mind" sought by mobile computing users in these security conscious times with a powerful suite of software solutions and services.

Security is now a top business priority. Enterprises that previously made investments in network infrastructure, mission-critical software applications, e-commerce, and the mobile computing devices themselves are poised to aggressively increase their spending on security.

At ZTRACE, we believe that software solutions and complementary services like ours that protect, monitor, and recover mobile computing devices-and the data stored on them-will soon become a ubiquitous requirement. ZTRACE plans to be your protection everywhere.

Company Description

ZTRACE Technologies is a premier provider of innovative security software and services designed to meet the challenging data security and asset protection demands of today's mobile computing environment. Serving enterprise, government, education, and consumer markets, ZTRACE is fast-tracked to be the global leader in mobile computing security. ZTRACE is a privately held company based in the Boston area.



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Attachment P



Press Release

Contact : P. Margit Tritt
zTrace Technologies
Tel: 303-828-5313
margit@zTrace.com

ZTRACE SECURITY SUITE incorporated into HP educational program

BOSTON, MA, April 2, 2002 -- ZTRACE™ Technologies today announced a new program to provide security applications for Hewlett-Packard Company's educational customers. ZTRACE security applications enable recovery of missing computers, identify the source of theft, protect the sensitive data in case of unauthorized access or break-in and effectively monitor and manage hardware and software information for asset tracking and software licensing compliance.

Schools and universities across the country recognize the value of notebook computers for students and staff. While small size and portability make notebooks a convenient choice, these very properties make the computers susceptible to theft or loss. ZTRACE is working with HP and the HP Campus Advan provide best-of-breed security applications to secure an institution's investment in

Attachment Q



19 August 2003

Products
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Question Desk

zLab

Media Room

zTrace Corporate



Login Name

Password

PRESS RELEASES

ZTRACE IN THE NEWS

INDUSTRY NEWS

Press Releases

**zTrace Participates in SoftwareToGo rollout in CompUSA 225 stores**
Boston, MA, August 7, 2003

 [Download](#)

**zTrace Technologies Partners with Xylos to Track Down Stolen PCs and Recover Information After Theft in Belgium and Luxembourg**
Boston, MA, August 1, 2003

 [Download](#)

**ZCONTROL Released**
Boston, MA, January 15, 2003

 [Download](#)

**ZTRACE SECURITY SUITE incorporated into HP educational program**
Boston, MA, April 2, 2002

 [Download](#)

**ZTRACE GOLD 5.0 Released**
Boston, MA, February 4, 2002

 [Download](#)

**ZTRACE Partners with Softline to offer laptop security in Europe**
Boston, MA, October 1, 2001

 [Download](#)

**ZTRACE Partners with Athena Security to Reduce Laptop Theft**
Boston, MA, July 12, 2001

 [Download](#)

**ZTRACE Crests into View at the PC-Expo**
Boston, MA, July 9, 2001

 [Download](#)

**ZTRACE Highly Visible at COMDEX**
Boston, MA, November 25, 2000

 [Download](#)

Attachment R



Press Release

zControl Released

Boston, MA, January 15, 2003 - zTrace Technologies today announces the release of zControl, the latest security software in the zTrace mobile device protection and recovery series. zControl is an invisible security application, based on zAgent core technology, that recovers files and deletes private information, maintaining data integrity, after a computer has been lost.

zControl addresses the questions of data security on a mobile device if the device is stolen or lost. zControl is stealth software that provides automated, remote and invisible control of the data stored on a computer. Through the zControl web-based interface an owner of the missing computer can communicate with his/her computer ordering the remote and invisible deletion of files, recovery of data to the zServer and remote encryption of data. Also, zControl allows to make specified files invisible, therefore adding an additional level of protection. zControl is able to display messages remotely to communicate to the thief or the person in possession of the missing device, and can even render the device unusable.

zControl, through its ability to encrypt and extract data remotely, is effective in preventing strategic information from being compromised. Since zControl is able to delete information upon loss of the computer, it is able to protect a company's network infrastructure from possible electronic attack from the stolen device. It can also be used by the owner to extract personal information saved in the computer, such as credit card numbers, PINS, and photographs, to maintain privacy.

Alexander Kesler, President and Founder of zTrace Technologies, said, "Computer theft and loss is rampant in today's business environment. With zControl, each individual and company knows that no matter what happens to the computer, the data necessary to keep working and keep business flowing will be protected and available to them even though the physical computer may not be."

Gary Bloom, Vice President of Sales of zTrace Technologies, said "zControl is the perfect complement to our zTrace Gold product. While zTrace Gold provides a stealth solution for protecting and retrieving your hardware, zControl provides a stealth solution for protecting and retrieving your valuable data. The two products, which comprise our zSecurity Pack, combine to offer a complete solution for your mobile assets, securing both hardware and data!"

About zTrace Technologies

zTrace Technologies is a premier provider of innovative security software and services designed to meet the challenging data security and asset protection demands of today's mobile computing environment. Serving enterprise, government, education, and consumer markets, zTrace is fast-tracked to be the global leader in mobile computing security. For more information about zTrace products, visit <http://www.zTrace.com> or call (877) zTrace-2.

Attachment RA

Document properties

File name: zControl.pdf

File size: 62.2 KB

Title: file:///Y:\pr_releases\zControl_pdf.html

Author: andrey

Subject: -

Keywords: -

Created: 7/30/03, 10:29:26 AM

Modified: 7/30/03, 9:30:02 AM

Application: PScript5.dll Version 5.2

PDF producer: Acrobat Distiller 5.0 (Windows)

PDF version: 1.4

Page count: 1

Page size: 8.26 x 11.19 in (portrait)

Fast web view: Yes

Close

Boston, MA, Jan
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zControl, through its ability to encrypt and extract data remotely, is effective in preventing strategic information from being compromised. Since zControl is able to delete information upon loss of the computer, it is able to protect a company's network infrastructure from possible electronic attack from the stolen device. It can also be used by the

Lightshot Screenshot

Attachment S

[:: Tell-a-Friend](#)[:: zGuarantee](#)**What if YOUR laptop gets stolen?**

1 December 2002

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Boston, MA, April 2,

2002

ZTRACE GOLD 5.0 Released[Download](#)

Boston, MA, February 4, 2002

ZTRACE Partners with Athena Security to Reduce Laptop Theft[Download](#)

Boston, 12 July 2001

ZTRACE Crests into View at the PC-Expo[Download](#)

Boston, 9 July 2001

ZTRACE Highly Visible at COMDEX[Download](#)

Boston, 25 November 2000

Attachment T



Yale University Selects zTrace to Provide Laptop Protection to Students

Boston, MA, August 20, 2003 - zTrace Technologies announces its partnership with Yale University to provide zTrace Gold and zControl, its laptop tracking, recovery and data protection products, to Yale students in a joint effort to reduce computer theft. Students will be able to purchase zTrace Gold and zControl products and services through a custom zTrace website designed for Yale as well as through the Office of Security Education at Yale University.

A computer running the stealth-mode zTrace Gold completes a virtual handshake with the zTrace server every time the computer's owner connects to the Internet. If that computer is stolen or lost, the owner reports it missing and puts the server on alert. The next time that the computer is used to make a connection to the Internet, zTrace Gold is able to pinpoint the computer's exact location so that authorities are able to recover and return it.

Attachment TA

Yale Unive

TraceTM
Technologies

Pro

Boston, MA, August
partnership with Ya
laptop tracking, reco
joint effort to redu
zTrace Gold and zC
website designed for
at Yale University.

es announces its
and zControl, its
Yale students in a
able to purchase
a custom zTrace
Security Education

A computer running the stealth-mode zTrace Gold completes a virtual handshake with the zTrace server every time the computer's owner connects to the Internet. If that computer is stolen or lost, the owner reports it missing and puts the server on alert. The next time that the computer is used to make a connection to the Internet, zTrace Gold is able to pinpoint the computer's exact location so that authorities are able to recover and return it.

Document properties

File name:	Yale.pdf
File size:	64.1 KB
Title:	file:///Y:\pr_releases\Yale_pdf.html
Author:	andrey
Subject:	-
Keywords:	-
Created:	8/20/03, 10:13:54 AM
Modified:	8/20/03, 9:14:34 AM
Application:	PScript5.dll Version 5.2
PDF producer:	Acrobat Distiller 5.0 (Windows)
PDF version:	1.4
Page count:	1
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Lightshot Screenshot

Attachment U

Attachment V

zPass.pdf

1 / 1 | 150%

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zPASS™



What Is It?

"You can't steal what you can't see."
- Alexander Kesler, Founder and President of zTrace

zPASS is an invisible password application, based on the zAGENT core, that detects and triggers specific actions to protect sensitive computer data. Once an unauthorized user fails to enter the required password, zPASS immediately makes all sensitive files and directories invisible, preventing access to any protected data. At the same time, the computer stays fully functional, fooling the unauthorized user into believing that there is nothing even worth stealing on the machine. Every keyboard, mouse, board or mouse action is recorded for

Attachment W

zEncrypt™



zEncrypt is an invisible encryption application that encrypts important computer files. zEncrypt works in conjunction with zTRACE GOLD and/or zPASS to immediately encrypt all sensitive data on the laptop as soon as an unauthorized-access warning has been received.

Attachment X

The Wayback Machine - <https://web.archive.org/web/20020814064818/http://www.ztrace.com:80/zControlHow.asp>



[zHome](#) [Get It Now!](#) [News](#) [Question Desk](#) [zLab](#) [Media Room](#) [zTrace Corporate](#)

[ZTRACE GOLD](#) [ZCONTROL](#) [ZPASS](#) [ZASSET TRACK](#) [ZENCRYPT](#) [ZSECURITY SUITE](#)

Login name

Password



[GO](#)

How Does It Work?

ZCONTROL is an invisible software application that provides automated control of a computer's data even AFTER loss has occurred. Action can be triggered by time delays, failed passwords or a ZTRACE loss report. Predefined actions can include retrieving files, deleting sensitive information and displaying a message to the current user.

Decide which files and directories are critical and define actions you want to occur if the computer falls out of your control. Make predefined files and directories invisible or further protected by encrypting them with ZENCRYPT when ZCONTROL is triggered. Predefined sensitive data can be deleted before unauthorized access. Display a personalized message on the missing computer's screen to communicate with the current user. The ZCONTROL web based user interface enables personal control of the computer's data even AFTER theft or loss.



[Why Do You Need It?](#)

[What Is It?](#)

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Attachment Y

The Wayback Machine - <https://web.archive.org/web/20020613175359/http://www.ztrace.com:80/zControlWhy.asp>




13 June 2002
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[ZTRACE GOLD](#)
[ZCONTROL](#)
[ZPASS](#)
[ZASSET TRACK](#)
[ZENCRYPT](#)
[ZSECURITY SUITE](#)






Why Do You Need It?

Laptops with large storage capacity are becoming desktop replacements and that data is valuable. If the computer with this data is lost or stolen, there could be significant negative ramifications. Consider these questions.

How long would you be non-productive? What strategic information could be compromised? Real examples of this type of information include pending mergers, new product intellectual property, business strategies and launch plans, and previously undisclosed financial operating results.

What tactical information could be compromised? Examples include private employment compensation details, proposals to clients, plans for organizational changes, and the myriad of similar information that can be gained from reading a person's email, calendar, contacts, or collection of documents and spreadsheets.

What information about the company's network or computing infrastructure would be revealed that could facilitate an electronic attack? Examples of this type of information include usernames and passwords, dial in numbers, IP addressing schemes, DNS naming conventions, ISPs used, mail servers, and other networking details related to connecting the laptop to the corporate or Internet environment.

What personal information about the laptop owner can be obtained? Examples include personal financial information, confidential family matters, loss of prized digital photographs, credit card numbers and PINS.

 [Download Product Information Sheet](#)



- What Is It?
- How Does It Work?



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The Wayback Machine - <https://web.archive.org/web/20020613174133/http://www.ztrace.com:80/zAssetTrackHo...>

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Password

zHome	Get It Now!	News	Question Desk	zLab	Media Room	zTrace Corporate
zTRACE GOLD	zCONTROL	zPASS	zASSET TRACK	zEncrypt	zSECURITY SUITE	

zAsset Track

How Does It Work?

zASSET TRACK gathers vital information about PCs and laptops deployed in the enterprise and stores this information at a centralized server for easy access. A web interface provides a single point of control for inventory updates and reporting.

zASSET TRACK lowers the total cost of ownership by centralizing lease information and locating machines instantly when they are needed. It detects hardware configurations and computer performance characteristics to improve planning and budgeting by identifying PCs for retirement and replacement, and accelerating the roll-out of operating systems and software packages. zASSET TRACK detects installed software and license information to monitor software license compliance and adherence to corporate software policies.



- ▶ Why Do You Need It?
- ▶ What Is It?

● Privacy at zTrace

● zGuarantee

**GET
zTrace
NOW**

zASSET TRACK provides a series of customized reports that include:

- Software summary by manufacturer and category
- Software audits and compliance reports
- Hardware audits and analysis reports
- Readiness reports for upgrades
- Operating systems and service pack information
- System serial numbers
- Storage usage
- Workstation information - end user name, login name, machine name, IP address, LAN address, MAC address, etc.
- Enterprise - level reports structured by customizable groupings.



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Attachment AA

The Wayback Machine - <https://web.archive.org/web/20020613175056/http://www.ztrace.com:80/zAssetTrackW...>



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Login name

Password

zHome	Get It Now!	News	Question Desk	zLab	Media Room	zTrace Corporate
ZTRACE GOLD	ZCONTROL	ZPASS	ZASSET TRACK	zEncrypt	ZSECURITY SUITE	

zAsset Track

Why Do You Need It?

Maintaining a full and current inventory of your fleet of mobile computers can be time consuming and potentially inaccurate. By definition, mobile computers are being moved around constantly and tracking the physical location of the computer, as well hardware components and software licensing, can be problematic.

Imagine having full asset tracking capabilities from a single point of control for your entire enterprise and being able to answer the following questions immediately.

- Which PCs have the minimal hardware configuration for Windows XP?
- Is this enterprise in full compliance with our software license agreements?
- Which PCs get returned to the leasing company when the contract lapses?
- Which PCs do not conform to the new configuration standards?
- What software applications are running on mobile PCs?
- Identify potential hardware cannibalization.



- [How Does It Work?](#)
- [What Is It?](#)

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Attachment BB



Windows XP unleashed

by Terry William Ogletree



Publication date	2002
Topics	Microsoft Windows (Computer file), Operating systems (Computers)
Publisher	Sams
Collection	inlibrary; printdisabled; internetarchivebooks
Contributor	Internet Archive
Language	English
Access-restricted-item	true
Addeddate	2012-03-13 15:52:11
Asin	0672322803
Boxid	IA179801
Camera	Canon EOS 5D Mark II
City	[Indianapolis, Ind.]
Donor	alibris
Edition	1. printing
External-identifier	urn:oclc:record:1036904063  urn:lcp:windowsxpunleash00ogle:lcpdf:a8cc93d2-0693-4ce5-aea6-68b4ba9a0644 urn:lcp:windowsxpunleash00ogle:epub:35c00ad6-b211-44fc-b1c7-e7ff81aad579
Extramarc	University of Alberta Libraries
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Terms of Service (last updated 12/31/2014)

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WorldCat: Windows XP

OCLC 47939031		No holdings in LDL - 103 other holdings					
Books	Rec Stat c	Entered	20010710	Replaced	20220504164323.5		
Type	a	ELvl	4	Src	Audn	Ctrl	Lang eng
BLvl	m	Form		Conf	Biog	MRec	inu
		Cont		GPub	LitF	Indx	
Desc	a	Ills	a	Fest	DtSt	Dates	2002,

010 2001093496

040 DLC [#b](#) eng [#c](#) [DLC](#) [#d](#) [UKM](#) [#d](#) [TXA](#) [#d](#) [BTCTA](#) [#d](#) [YDXCP](#) [#d](#) [BAKER](#) [#d](#) [INTCL](#) [#d](#) [OCLCF](#) [#d](#) [OCLCO](#) [#d](#) [BEDGE](#) [#d](#) [OCLCQ](#) [#d](#) [SEO](#) [#d](#) [OCLCA](#) [#d](#) [OCLCO](#)

015 GBA1V6989 [#2](#) bnb

019 48881804 [#a](#) 49349893

020 0672322803

020 9780672322808

042 pcc

050 00 QA76.76.O63 [#b](#) O3435 2002

082 00 005.4/469 [#2](#) 21

090

049 LDLL

100 1_ Ogletree, Terry William.

245 10 Windows XP / [#c](#) Terry William Ogletree ; contributing authors, Walter Glenn and Rima Regas.

246 30 Microsoft Windows XP unleashed

260 Indianapolis, IN : [#b](#) Sams Pub., [#c](#) 2002.

300 xxii, 880 pages : [#b](#) illustrations ; [#c](#) 24 cm

336 text [#b](#) txt [#2](#) rdacontent

337 unmediated [#b](#) n [#2](#) rdamedia

338 volume [#b](#) nc [#2](#) rdacarrier

505 00 [#g](#) pt. I. [#t](#) Architecture and Installation -- [#g](#) 1. [#t](#) Looking Inside Windows XP Professional -- [#g](#) 2. [#t](#) Before You Install or Upgrade -- [#g](#) 3. [#t](#) Installing and Upgrading Windows XP -- [#g](#) 4. [#t](#) Unattended Installation and Sysprep -- [#g](#) pt. II. [#t](#) Desktop, File Management, General Configuration -- [#g](#) 5. [#t](#) Configuring Accessibility Options -- [#g](#) 6. [#t](#) Understanding the Startup Process -- [#g](#) 7. [#t](#) Up Front: The New Desktop -- [#g](#) 8. [#t](#) Other Applications and Accessories -- [#g](#) 9. [#t](#) Working with Files and Folders -- [#g](#) 10. [#t](#) Using Microsoft Outlook Express for E-mail, News, and More -- [#g](#) pt. III. [#t](#) Administration, User Management, Technical Issues -- [#g](#) 11. [#t](#) Running Legacy Applications under Windows XP -- [#g](#) 12. [#t](#) Installing and Removing Applications -- [#g](#) 13. [#t](#) Command Prompt Tools -- [#g](#) 14. [#t](#) Using the Control Panel -- [#g](#) 15. [#t](#) Managing Local Users -- [#g](#) 16. [#t](#) Auditing Windows XP Using the Event Viewer -- [#g](#) 17. [#t](#) Printing with Windows XP -- [#g](#) 18. [#t](#) Managing Disks and Partitions -- [#g](#) 19. [#t](#) Using the Task Manager -- [#g](#) 20. [#t](#) Windows XP Registry -- [#g](#) 21. [#t](#) Using Backup on Windows XP -- [#g](#) 22. [#t](#) Performance Monitoring, Logs, and Alerts -- [#g](#) 23. [#t](#) Be Paranoid: Disaster Recovery Planning -- [#g](#) 24. [#t](#) Configuring Your Computer for Local Area Networking -- [#g](#) 25. [#t](#) Configuring Your Computer for an Internet Connection -- [#g](#) 26. [#t](#) Joining a Domain and the Active Directory -- [#g](#) pt. IV. [#t](#) Multimedia -- [#g](#) 27. [#t](#) Overview of Windows XP Multimedia Features -- [#g](#) 28. [#t](#) Capturing Images and Video and Using Windows Movie Maker -- [#g](#) 29. [#t](#) Windows Media Player 8 -- [#g](#) pt. V. [#t](#) Appendices -- [#g](#) A. [#t](#) Introduction to Transmission Control Protocol/Internet Protocol -- [#g](#) B. [#t](#) Overview of the Lightweight Directory Access Protocol and Microsoft's Active Directory -- [#g](#) C. [#t](#) Using Windows XP on a Notebook Computer -- [#g](#) D. [#t](#) Basics of Internet Information Server.

630 00 [#u](#) Microsoft Windows (Computer file).

650 _0 [#u](#) Operating systems (Computers).

630 04 Microsoft Windows (Computer file)

650 _6 Systèmes d'exploitation (Ordinateurs) [#0](#) (CaQQLa)201-0029698

650 _7 operating systems. [#2](#) aat [#0](#) (CStmoGRI)aat300235851
650 _7 Systèmes d'exploitation. [#2](#) eclas
630 07 Microsoft Windows (Computer file) [#2](#) fast [#0](#) (OCoLC)fst01367862
650 _7 Operating systems (Computers) [#2](#) fast [#0](#) (OCoLC)fst01046280
700 1_ Glenn, Walter J.
700 1_ Regas, Rima.
938 Baker & Taylor [#b](#) BKTY [#c](#) 49.99 [#d](#) 37.49 [#i](#) 0672322803 [#n](#) 0003775960 [#s](#) active
938 Baker and Taylor [#b](#) BTCP [#n](#) 2001093496
938 YBP Library Services [#b](#) YANK [#n](#) 100274635
029 1_ AU@ [#b](#) 000022977613
029 1_ AU@ [#b](#) 000023704388
029 1_ NZ1 [#b](#) 6997384
029 1_ YDXCP [#b](#) 100274635

Action Status	Delete Holdings _	Export _	Label _	Produce _	Update Holdings _	Validate _
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Attachment DD

Leader *****a22*****a*4500
001 ## a2884616
003 ## SIRSI
008 ## 020318s2001 inua 001 0 eng
015 ## \$a GBA2-21116
016 7# \$a 0672322803
\$2 Uk
020 ## \$a 0672322803 (pbk.) :
\$c £36.50
035 ## \$a (RGT0)UKBPGBA221116-B
035 ## \$a (0CoLC)ocn370554110
040 ## \$a WLABNL
\$c WLABNL
\$d Uk
\$d UPB
079 ## \$a ocm50403069
100 1# \$a Ogletree, Terry William.
245 10 \$a Windows XP unleashed /
\$c Terry William Ogletree, contributing authors Walter Glenn and Rima
Regas.
246 34 \$a Microsoft Windows XP unleashed
260 ## \$a Indianapolis, Ind :
\$b Sams,
\$c 2001.
300 ## \$a xxii, 880 p. :
\$b ill. ;
\$c 24 cm.
336 ## \$a text
\$2 rdacontent
337 ## \$a unmediated
\$2 rdamedia
338 ## \$a volume
\$2 rdacarrier
500 ## \$a Includes index.
596 ## \$a LEE
630 00 \$a Microsoft Windows (Computer file)
650 #0 \$a Operating systems (Computers)
650 #0 \$a Windows (Computer programs)
700 1# \$a Glenn, Walter J.
700 1# \$a Regas, Rima.
977 ## \$a QA 76.76 .063 03435 2001
583 ## \$a cat
\$b b
\$c 20020328
\$k krw
\$5 UPB

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MARC Template

WorldCat: 386 DX microprocessor hardware reference manual

OCLC	22199965	No holdings in LDL - 13 other holdings							
Books	▼	Rec Stat	c	Entered	19900809	Replaced	20220617060757.2		
Type	a	ELvl		Src	d	Audn		Ctrl	
BLvl	m	Form		Conf	0	Biog		MRec	
		Cont		GPub		LitF	0	Indx	0
Desc	a	Ills	a	Fest	0	DtSt	s	Dates	1990 ,
040 TEC \$b eng \$c TEC \$d BAKER \$d YDXCP \$d OCLCF \$d Functions ▼ OCLCO \$d OCLCA \$d OCLCQ \$d OCLCO									
020		155512111X						Functions	▼
020		9781555121112						Functions	▼
050	4	TK7888.4 \$b .I592 1990						Functions	▼
090		\$b						Functions	▼
049		LDLL						Functions	▼
110	2_	Intel Corporation.						Functions	▼
245	1 0	386 DX microprocessor hardware reference						Functions	▼
260		Mt. Prospect, Ill. : \$b Intel Corp., \$c 1990.						Functions	▼
300		1 volume (various pagings) : \$b illustrations ; \$c						Functions	▼
336		text \$b txt \$2 rdacontent						Functions	▼
337		unmediated \$b n \$2 rdamedia						Functions	▼
338		volume \$b nc \$2 rdacarrier						Functions	▼
650	_0	Intel 80386 (Microprocessor).						Functions	▼
650	_0	Microcomputers.						Functions	▼
650	_0	Microprocessors.						Functions	▼
650	6	Intel 80386 (Microprocesseur) \$0 (CaQQLa)201-						Functions	▼
650	6	Micro-ordinateurs. \$0 (CaQQLa)201-0064171						Functions	▼
650	7	microcomputers. \$2 aat \$0						Functions	▼
650	7	Intel 80386 (Microprocessor) \$2 fast \$0						Functions	▼
650	7	Microcomputers. \$2 fast \$0 (OCoLC)fst01019642						Functions	▼
650	7	Microprocessors. \$2 fast \$0 (OCoLC)fst01020008						Functions	▼
938		Baker & Taylor \$b BKTY \$c 20.00 \$d 24.95 \$i						Functions	▼
938		YBP Library Services \$b YANK \$n 1159359						Functions	▼
020	1	9781555121112						Functions	▼

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LEADER 00000cam a2200000 a 45 0

001 3400849

005 19970604235300.0

008 910107c19901989ilua 00010 eng d

020 a| 1555121314

035 a| (Sirsi)3400849

035 a| ABH7215IP

035 a| (OCoLC)22927744

040 a| YRM c| YRM

049 b| I-UL

050 4 a| QA76.8.I2928 b| I58 1990

110 2 0 a| Intel Corporation. =| ^A63470

245 1 0 a| 386 DX microprocessor programmer's reference manual.

260 0 a| Mt. Prospect, IL : b| Intel Corp., c| 1990, c1989.

300 a| 1 v. (various pagings) : b| ill. ; c| 23 cm.

500 a| At head of title: Intel.

500 a| "Order number: 230985-003" -- Cover.

650 0 a| Microprocessors x| Programming. =| ^A543481

650 0 a| Intel 80386 (Microprocessor) x| Programming. =| ^A568180

596 a| 42

999 a| QA76.8.I2928 I58 1990 i| 30000021827765 j| QA 000076.8 .I2928 I58 1990 I| STACKS m| I-UNIVLIB n| STACKS w| LC

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WorldCat: Operating systems

OCLC 14001792	No holdings in LDL - 508 other holdings							
Books ▼	Rec Stat c	Entered 19860716	Replaced 20220714125831.3					
Type a	ELvl	Src	Audn	Ctrl	Lang eng			
BLvl m	Form	Conf 0	Biog	MRec	Ctry nju			
	Cont b	GPub	LitF 0	Indx 1				
Desc a	Ills a	Fest 0	DtSt s	Dates 1987 ,				

>010 86018752
 >040 DLC \$b eng \$c DLC \$d FIL \$d MUQ \$d NLGGC \$d BTCTA \$d YDXCP \$d OCLCG \$d AU@ \$d DEBBG \$d ZWZ \$d OCLCQ \$d GBVCP \$d OCLCO \$d OCLCF \$d DEBSZ \$d BEDGE \$d OCLCQ \$d TULIB \$d OCLCQ \$d ERD \$d OCLCQ \$d VZT \$d OCLCO \$d OCLCQ \$d UKBTH \$d OCLCA \$d OCLCO \$d NAM \$d OCLCO \$d OCL
 >019 16018350 \$a 881263754 \$a 944143945 \$a 1109614052
 >020 0136374069
 >020 9780136374060
 >020 0136373313 \$q (pbk.)
 >020 9780136373315 \$q (pbk.)
 >050 00 QA76.76.O63 \$b T36 1987
 >080 681.3
 >080 0 518.741
 >082 0 005.4/3 \$2 19
 >084 54.54 \$2 bcl
 >084 ST 260 \$2 rvk
 >084 DAT 400f \$2 stub
 >090 \$b
 >049 LDLL
 >100 1 Tanenbaum, Andrew S., \$d 1944- \$e author.
 >245 10 Operating systems : \$b design and implementation / \$c Andrew S. Tanenbaum.
 >264 1 Englewood Cliffs, N.J. : \$b Prentice-Hall, \$c [1987]
 >264 4 \$c ©1987
 >300 xvi, 719 pages : \$b illustrations ; \$c 25 cm.
 >336 text \$b txt \$2 rdacontent
 >337 unmediated \$b n \$2 rdamedia
 >338 volume \$b nc \$2 rdacarrier
 >490 1 Prentice-Hall software series
 >504 Includes bibliographical references (pages 342-349) and index.
 >530 Also issued online.

Attachment HH

Leader *****cam*a22*****a*4500
001 ## a1016740
003 ## SIRSI
008 ## 860716s1987 njua b 00110 eng
010 ## \$a 86018752 //r87
020 ## \$a 0136374069 :
\$c \$34.95
035 ## \$a (MARC)
035 ## \$a (MARCCat)
035 ## \$a (OCoLC)ocn368099027
040 ## \$d UPB
050 00 \$a QA76.76.063
\$b T36 1987
079 ## \$a ocm14001792
082 0# \$a 005.4/3
\$2 19
100 10 \$a Tanenbaum, Andrew S.,
\$d 1944-
245 10 \$a Operating systems :
\$b design and implementation /
\$c Andrew S. Tanenbaum.
260 0# \$a Englewood Cliffs, N.J. :
\$b Prentice-Hall,
\$c ©1987.
300 ## \$a xvi, 719 p. :
\$b ill. ;
\$c 25 cm.
336 ## \$a text
\$2 rdacontent
337 ## \$a unmediated
\$2 rdamedia
338 ## \$a volume
\$2 rdacarrier
440 #0 \$a Prentice-Hall software series
504 ## \$a Includes bibliographical references (p. 342-349).
500 ## \$a Includes index.
596 ## \$a LEE
650 #0 \$a Operating systems (Computers)
959 ## \$a cat:d:eb;der MPH9500
962 ## \$a LEE-LIB
988 ## \$a 4/16/1990
\$b 4/16/1990
\$c 4/12/1990
989 1L \$a QA 76.76 .063 T36 1987
\$w LC
\$h sci
\$i 31197205650515
\$d 8/27/1997
\$n 37
\$o .COMMENT. RUSH RESERVE! CS 444/AUREL CORNELL.
\$q 19
\$5 1/1

Attachment II

WorldCat: MRS bulletin

OCLC		12225171		LDL Holdings/LH - 186 other holdings			
Continuing Resources		Rec Stat	c	Entered	19850702	Replaced	20230210154503.0
Type	a	ELvl		Src	c	G Pub	Ctrl
BLvl	s	Form		Conf	0	Freq	m
S/L	0	Orig		EntW		Regl	r
Desc	a	SrTp	p	Cont		DtSt	c
						Alph	a
						Dates	1982,9999
010	sf 93092134 #z sn 85009886						
040	NSD #b eng #c #d NSD #d NST #d NSD #d HUL #d NSD #d NST #d NSD #d MYG #d NST #d WAU #d NST #d DLC #d OCL #d SYS #d NLM #d OCLCQ #d MYG #d HNK #d NSD #d CIT #d IUL #d OCLCQ #d UKMGB #d NLM #d OCLCQ #d IUL #d OCLCF #d CUS #d OCL #d IUL #d OCLCQ #d OCLCO #d PUL #d OCLCO						
012	#k 1 #l 1 #m 1						
016	7_	100971398 #2 DNLM					
016	7_	012412549 #2 Uk					
019	932532514 #a 1011900381 #a 1013416130 #a 1029238652 #a 1035336940 #a 1051666696 #a 1065252645 #a 1080601958 #a 1114930576 #a 1156195250 #a 1157027299 #a 1190743658 #a 1197770773 #a 1224907663 #a 1242768743 #a 1242811479 #a 1246489464						
022	0_	0883-7694 #l 0883-7694 #2 1					
030	MRSBEA						
032	006365 #b USPS						
037	#b Materials Research Society, 9800 McKnight Rd., Suite 327, Pittsburgh, PA 15237						
042	nsdp #a pcc						
050	14	TA401 #b .M78					
050	00	WMLC 93/1272					
082	10	620 #2 11					
090							
049	LDLL						
210	0_	MRS bull.					
222	_0	MRS bulletin					
245	00	MRS bulletin / #c Materials Research Society.					
246	3_	Materials Research Society bulletin					
260	#3 1982- : #a University Park, PA : #b Materials Research Society						
260	3_	#3 -1997 : #a Pittsburgh, PA : #b Materials Research Society					
260	3_	#3 1998- : #a Warrendale, PA : #b Materials Research Society					
300	volumes						
310	Monthly, #b <Dec. 1990->						
321	Bimonthly						
336	text #b txt #2 rdacontent						
337	unmediated #b n #2 rdamedia						
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Abstract:

This paper mainly focuses on the development of the NOR flash memory technology, with the aim of describing both the basic functionality of the memory cell used so far and the main cell architecture consolidated today. The NOR cell is basically a floating-gate MOS transistor, programmed by channel hot electron and erased by Fowler-Nordheim tunneling. The main reliability issues, such as charge retention and endurance, are discussed, together with an understanding of the basic physical mechanisms responsible. Most of these considerations are also valid for the NAND cell, since it is based on the same concept of floating-gate MOS transistor. Furthermore, an insight into the multilevel approach, where two bits are stored in the same cell, is presented. In fact, the exploitation of the multilevel approach at each technology node allows an increase of the memory efficiency, almost doubling the density at the same chip size, enlarging the application range and reducing the cost per bit. Finally, NOR flash cell scaling issues are covered, pointing out the main challenges. Flash cell scaling has been demonstrated to be really possible and to be able to follow Moore's law down to the 130-nm technology generations. Technology development and consolidated know-how is expected to sustain the scaling trend down to 90- and 65-nm technology nodes. One of the crucial issues to be solved to allow cell scaling below the 65-nm node is the tunnel oxide thickness reduction, as tunnel thinning is limited by intrinsic and extrinsic mechanisms.

 Contents

SECTION I.

Introduction



The semiconductor market, for the long term, has been continuously increasing, even if with some valleys and peaks, and this growing trend is expected to continue in the coming years (see Fig. 1). A large amount of this market, about 20%, is given by the semiconductor memories, which are divided into the following two branches, both based on the complementary metal–oxide–semiconductor (CMOS) technology (see Fig. 2).

- The volatile memories, like SRAM or DRAM, that although very fast in writing and reading (SRAM) or very dense (DRAM), lose the data contents when the power supply is turned off.
- The nonvolatile memories, like EPROM, EEPROM, or Flash, that are able to balance the less-aggressive (with respect to SRAM and DRAM) programming and reading performances with nonvolatility, i.e., with the capability to keep the data content even without power supply.

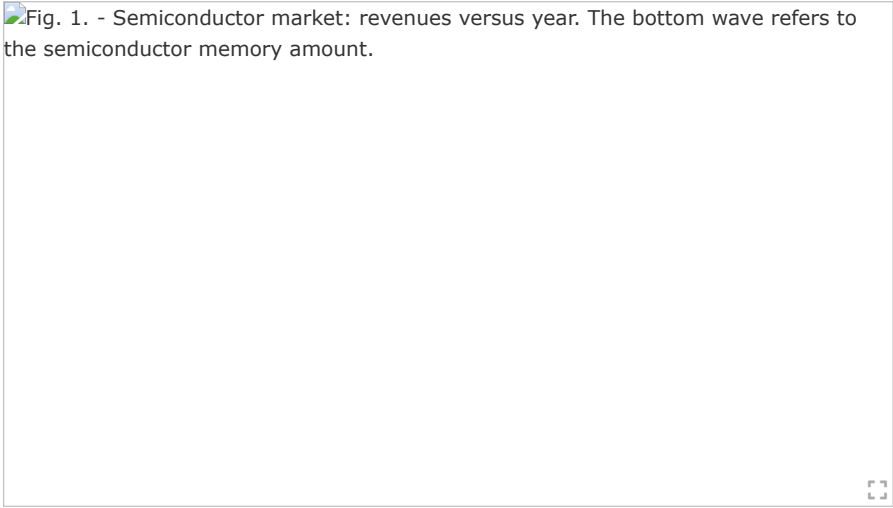
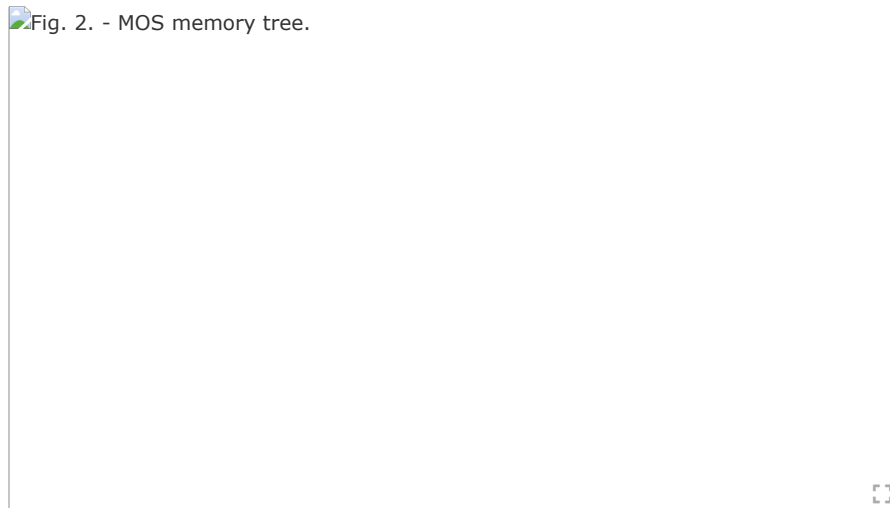
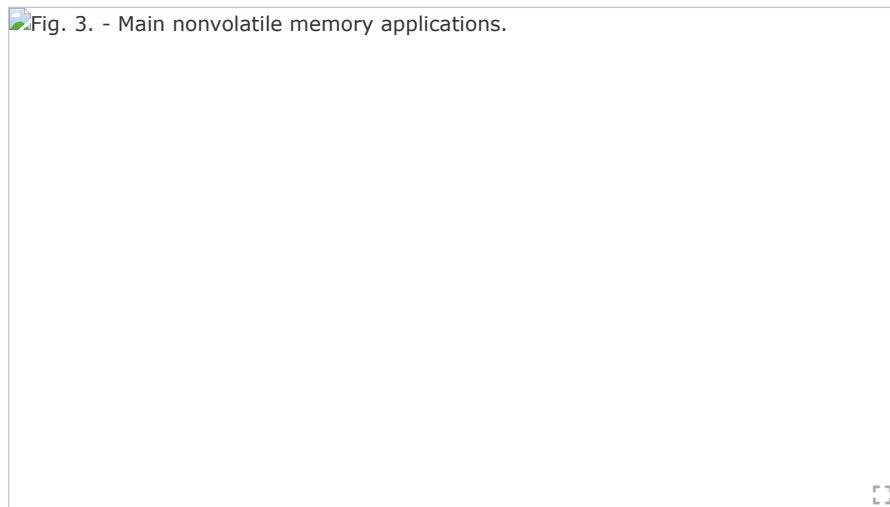
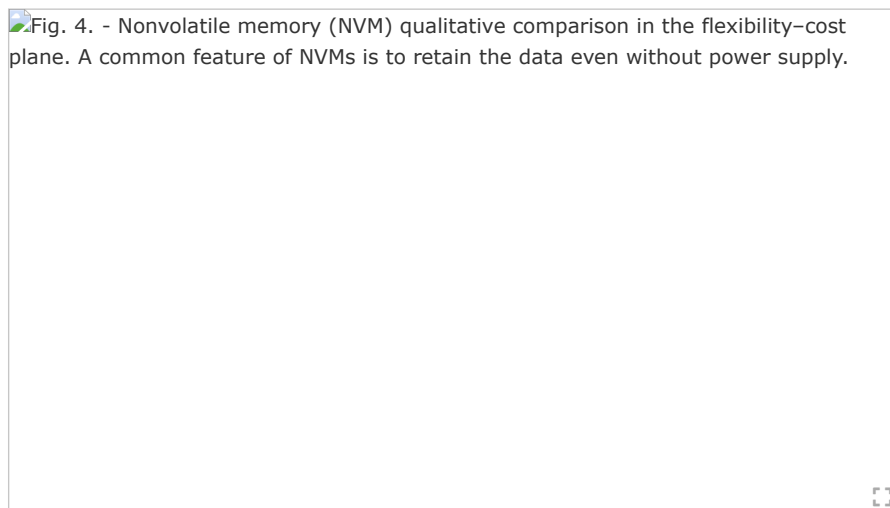
Fig. 1. - Semiconductor market: revenues versus year. The bottom wave refers to the semiconductor memory amount.

Fig. 1. Semiconductor market: revenues versus year. The bottom wave refers to the semiconductor memory amount.

 Fig. 2. - MOS memory tree.**Fig. 2.** MOS memory tree. Fig. 3. - Main nonvolatile memory applications.**Fig. 3.** Main nonvolatile memory applications. Fig. 4. - Nonvolatile memory (NVM) qualitative comparison in the flexibility-cost plane. A common feature of NVMs is to retain the data even without power supply.**Fig. 4.** Nonvolatile memory (NVM) qualitative comparison in the flexibility-cost plane. A common feature of NVMs is to retain the data even without power supply.

Thanks to this characteristic, the nonvolatile memories offer the system a different opportunity and cover a wide range of applications, from consumer and automotive to computer and communication (see Fig. 3).

The different nonvolatile memory families can be qualitatively compared in terms of flexibility and cost (see Fig. 4). Flexibility means the possibility to be programmed and erased many times on the system with minimum granularity (whole chip, page, byte, bit); cost means process complexity and in particular silicon occupancy, i.e., density or, in simpler words, cell size. Considering the flexibility-cost plane, it turns out that Flash offers the best compromise between these two parameters, since they have the smallest cell size (one transistor cell) with a very good flexibility (they can be electrically written on field more than 100 000 times, with byte programming and sectors erasing).

 Fig. 5. - The family tree of Flash memory cell architecture. The actual industry standard are: 1) The nor for code and data storage application and 2) nand only for data storage.



Fig. 5. The family tree of Flash memory cell architecture. The actual industry standard are: 1) The nor for code and data storage application and 2) nand only for data storage.

The most relevant phenomenon of this past decade in the field of semiconductor memories has been the explosive growth of the Flash memory market, driven by cellular phones and other types of electronic portable equipment (palm top, mobile PC, mp3 audio player, digital camera, and so on). Moreover, in the coming years, portable systems will demand even more nonvolatile memories, either with high density and very high writing throughput for data storage application or with fast random access for code execution in place.

Based on these market needs, a well-known way to classify Flash products and the relative technologies is that of defining two major application segments:

- code storage, where the program or the operating system is stored and is executed by the microprocessor or microcontroller;
- data (or mass) storage, where data files for image, music, and voice are recorded and read sequentially.

Different type of Flash cells and architectures have been proposed in the past (see Fig. 5). They can be divided in terms of access type, parallel or serial, and in terms of the utilized programming and erasing mechanism, Fowler–Nordheim tunneling (FN), channel hot electron (CHE), hot-holes (HH), and source-side hot electron (SSHE). Among all of these architectures, today two can be considered as industry standard: the common ground NOR Flash [1]– [3], that due to its versatility is addressing both the code and data storage segments, and the NAND Flash, optimized for the data storage market [4], [5].

In the following, the basic concepts, the reliability issues, the evolution, and scaling trends will be presented only for the NORFlash cell, but most of these considerations are also valid for the NAND

since both of them are based on the concept of floating-gate MOS transistor.

SECTION II.

nor Flash Cell

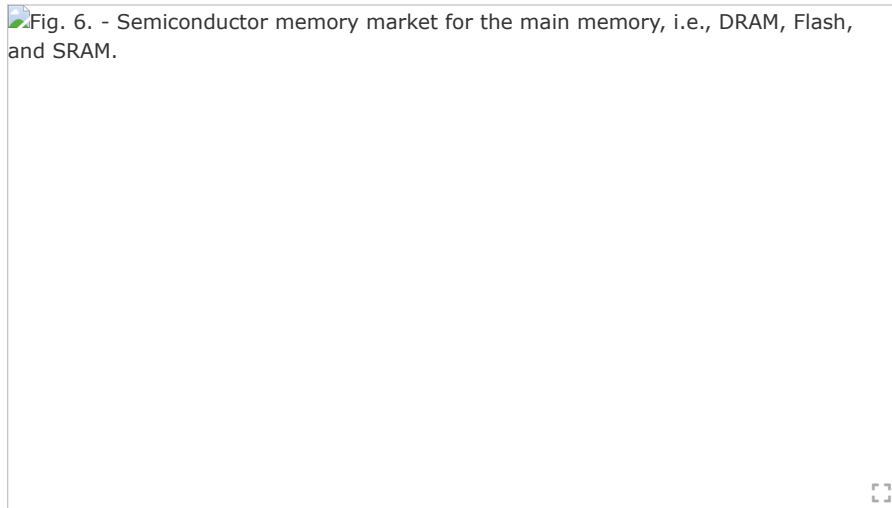
Fig. 6. - Semiconductor memory market for the main memory, i.e., DRAM, Flash, and SRAM.

Fig. 6. Semiconductor memory market for the main memory, i.e., DRAM, Flash, and SRAM.

In 1971, Frohman-Bentchkowsky presented a floating gate transistor in which hot electrons were injected and stored [6], [7]. From this original work, the erasable programmable read only memory (EPROM) cell, programmed by CHE and erased by ultraviolet (UV) photoemission, has been developed. The EPROM technology became the most important nonvolatile memory in the 1980s. In the same period, the Flash EEPROM was proposed, basically an EPROM cell, with the possibility to be electrically erased [8]. The name Flash was given to represent the fact that the whole memory array could be erased in the same (fast) time.

The first Flash product was presented in 1988 [9]. In terms of applications, initially Flash products were mainly used as an “EPROM replacement,” offering the possibility to be erased on system, avoiding the cumbersome UV erase operation. But the Flash market did not take off until this technology was proven to be reliable and manufacturable. In the late 1990s, the Flash technology exploded as the right nonvolatile memory for code and data storage, mainly for mobile applications. Starting from 2000, the Flash memory can be considered a really mature technology: more than 800 million units of 16-Mb equivalent NOR Flash devices were sold in that year.

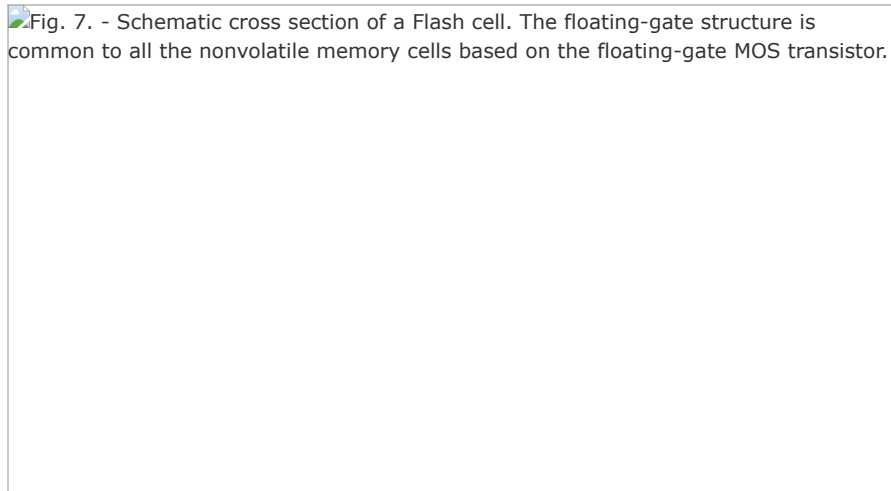
Fig. 7. - Schematic cross section of a Flash cell. The floating-gate structure is common to all the nonvolatile memory cells based on the floating-gate MOS transistor.

Fig. 7. Schematic cross section of a Flash cell. The floating-gate structure is common to all the nonvolatile memory cells based on the floating-gate MOS transistor.

In Fig. 6, the Flash market is reported and compared with the DRAM and SRAM one [10]. It can be seen that the Flash market became and has stayed bigger than the SRAM one since 1999. Moreover, the Flash market is forecasted to be above \$20 billion in three or four years from now, reaching the DRAM market amount, and only smoothly following the DRAM oscillating trend, driven by the personal computer market. In fact, portable systems for communications and consumer markets, which are the drivers of the Flash market, are forecasted to continuously grow in the coming years.

In the following, we briefly describe the basics of the Flash cell functionality.

Fig. 8. - Schematic energy band diagram (lower part) as referred to a floating gate MOSFET structure (upper part). The left side of the figure is related to a neutral cell, while the right side to a negatively charged cell.

Fig. 8. Schematic energy band diagram (lower part) as referred to a floating gate MOSFET structure (upper part). The left side of the figure is related to a neutral cell, while the right side to a negatively charged cell.

A. Basic Concept

Fig. 9. - (a) nor Flash array equivalent circuit. (b) Flash memory cell cross section.

Fig. 9. (a) nor Flash array equivalent circuit. (b) Flash memory cell cross section.

A Flash cell is basically a floating-gate MOS transistor (see Fig. 7), i.e., a transistor with a gate completely surrounded by dielectrics, the floating gate (FG), and electrically governed by a capacitively coupled control gate (CG). Being electrically isolated, the FG acts as the storing

electrode for the cell device; charge injected in the FG is maintained there, allowing modulation of the “apparent” threshold voltage (i.e., V_T seen from the CG) of the cell transistor. Obviously the quality of the dielectrics guarantees the nonvolatility, while the thickness allows the possibility to program or erase the cell by electrical pulses. Usually the gate dielectric, i.e., the one between the transistor channel and the FG, is an oxide in the range of 9–10 nm and is called “tunnel oxide” since FN electron tunneling occurs through it. The dielectric that separates the FG from the CG is formed by a triple layer of oxide–nitride–oxide (ONO). The ONO thickness is in the range of 15–20 nm of equivalent oxide thickness. The ONO layer as interpoly dielectric has been introduced in order to improve the tunnel oxide quality. In fact, the use of thermal oxide over polysilicon implies growth temperature higher than 1100 °C, impacting the underneath tunnel oxide. High-temperature postannealing is known to damage the thin oxide quality.

If the tunnel oxide and the ONO behave as ideal dielectrics, then it is possible to schematically represent the energy band diagram of the FG MOS transistor as reported in Fig. 8. It can be seen that the FG acts as a potential well for the charge. Once the charge is in the FG, the tunnel and ONO dielectrics form potential barriers.

The neutral (or positively charged) state is associated with the logical state “1” and the negatively charged state, corresponding to electrons stored in the FG, is associated with the logical “0.”

The “NOR” Flash name is related to the way the cells are arranged in an array, through rows and columns in a NOR-like structure. Flash cells sharing the same gate constitute the so-called wordline (WL), while those sharing the same drain electrode (one contact common to two cells) constitute the bitline (BL). In this array organization, the source electrode is common to all of the cells [Fig. 9(a)].

A scanning electron microscope (SEM) cross section along a bitline of a Flash array is reported in Fig. 9(b), where three cells can be observed, sharing two by two the drain contact and the sourceline. This picture can be better understood considering the layout of a cell (see Fig. 10) and the two schematic cross sections, along the y direction (bitline) and the x direction (wordline). The cell area is given by the x pitch times the y pitch. The x pitch is given by the active area width and space, considering also that the FG must overlap the oxide field. The y pitch is constituted by the cell gate length, the contact-to-gate distance, half contact, and half sourceline. It is evident, as reported in Fig. 9(b), that both contact and sourceline are shared between two adjacent cells.

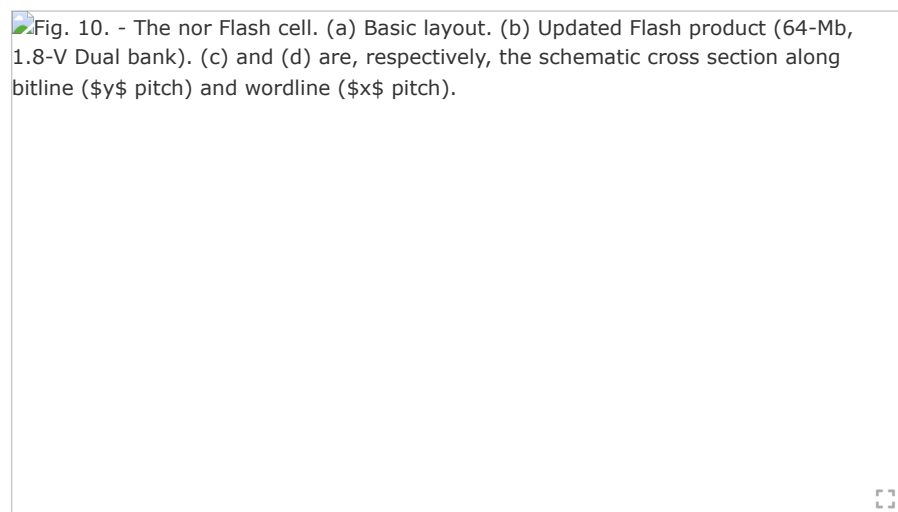
Fig. 10. - The nor Flash cell. (a) Basic layout. (b) Updated Flash product (64-Mb, 1.8-V Dual bank). (c) and (d) are, respectively, the schematic cross section along bitline (y pitch) and wordline (x pitch).

Fig. 10. The nor Flash cell. (a) Basic layout. (b) Updated Flash product (64-Mb, 1.8-V Dual bank). (c) and (d) are, respectively, the schematic cross section along bitline (y pitch) and wordline (x pitch).



Fig. 11. Floating-gate MOSFET reading operation.

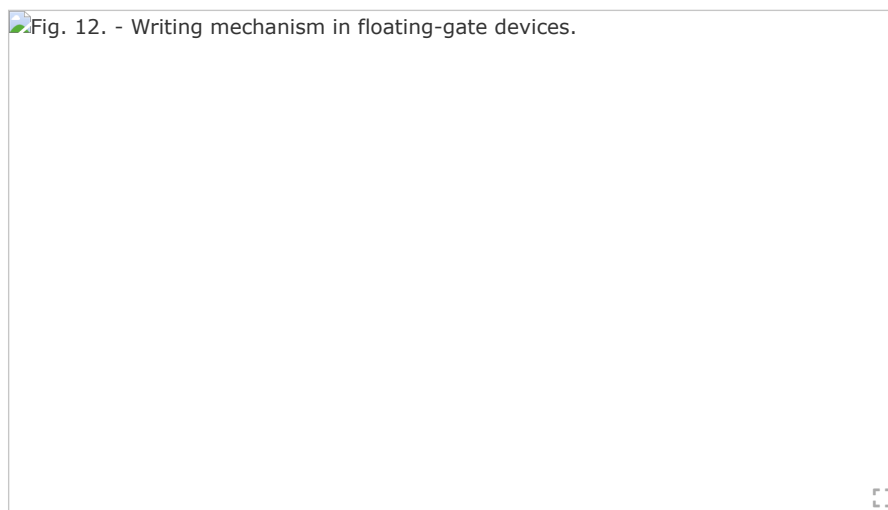


Fig. 12. Writing mechanism in floating-gate devices.

B. Reading Operation

The data stored in a Flash cell can be determined measuring the threshold voltage of the FG MOS transistor. The best and fastest way to do that is by reading the current driven by the cell at a fixed gate bias. In fact, as schematically reported in Fig. 11, in the current–voltage plane two cells, respectively, logic “1” and “0” exhibit the same transconductance curve but are shifted by a quantity—the threshold voltage shift (ΔV_T)—that is proportional to the stored electron charge Q .

Hence, once a proper charge amount and a corresponding ΔV_T is defined, it is possible to fix a reading voltage in such a way that the current of the “1” cell is very high (in the range of tens of microamperes), while the current of the “0” cell is zero, in the microampere scale. In this way, it is possible to define the logical state “1” from a microscopic point of view as no electron charge (or positive charge) stored in the FG and from a macroscopic point of view as large reading current. Vice versa, the logical state “0” is defined, respectively, by electron charge stored in the FG and zero reading current.

C. Writing Operation

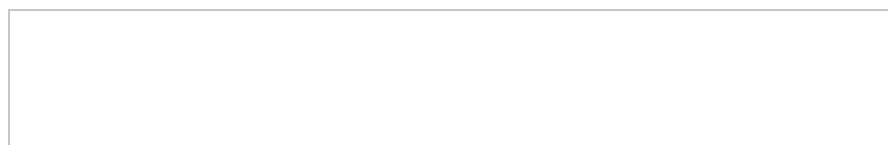
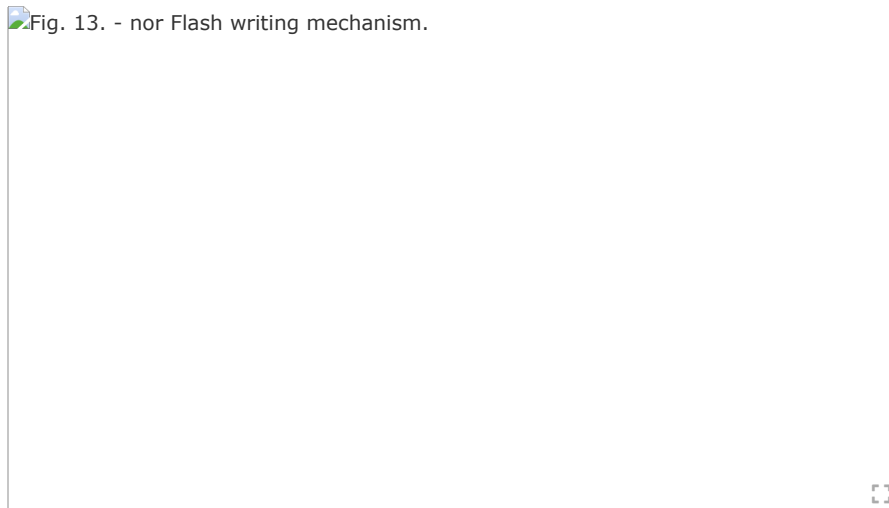


 Fig. 13. - nor Flash writing mechanism.**Fig. 13.** nor Flash writing mechanism.

Considering Fig. 8, the problem of writing an FG cell corresponds to the physical problem of forcing an electron above or across an energy barrier. The problem can be solved exploiting different physical effects [11]. In Fig. 12, the three main physical mechanisms used to write an FG memory cell are sketched.

- The CHE mechanism, where electrons gain enough energy to pass the oxide–silicon energy barrier, thanks to the electric field in the transistor channel between source and drain. In fact, the electron energy distribution presents a tail in the high energy side that can be modulated by the longitudinal electric field.
- The photoelectric effect, where electrons gain enough energy to surmount the barrier thanks to the interaction with a photon with energy $h\nu$ larger than the barrier itself. For silicon–dioxide, this corresponds to UV radiation. This mechanism is the one originally used in EPROM's products to erase the entire device.
- The Fowler–Nordheim electron tunneling mechanism is a quantum-mechanical tunnel induced by an electric field. Applying a strong electric field (in the range of 8–10 MV/cm) across a thin oxide, it is possible to force a large electron tunneling current through it without destroying its dielectric properties.

A NOR Flash memory cell is programmed by CHE injection in the FG at the drain side and it is erased by means of the FN electron tunneling through the tunnel oxide from the FG to the silicon surface (see Fig. 13).

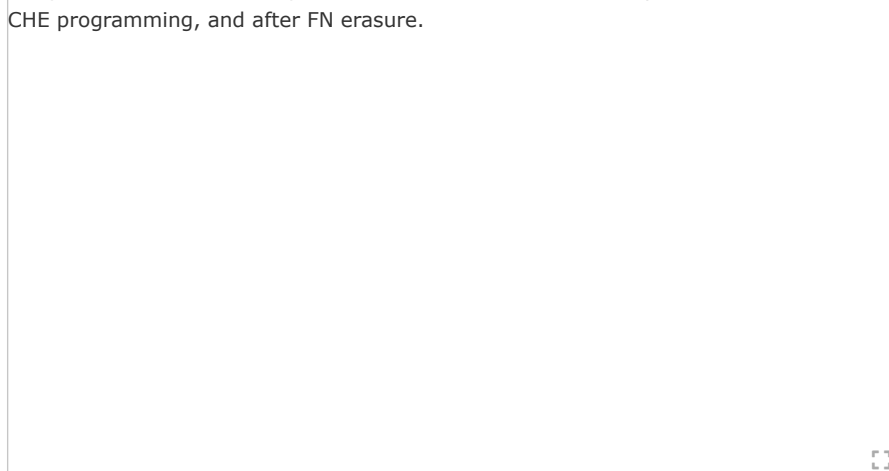
 Fig. 14. - Threshold voltage distribution of a 1-Mb Flash array after UV erasure, after CHE programming, and after FN erasure.

Fig. 14. Threshold voltage distribution of a 1-Mb Flash array after UV erasure, after CHE programming, and after FN erasure.

SECTION III. Reliability

Many issues have to be addressed when, from the theoretical model of a single cell, a Flash product has to be realized, integrating millions of cells in an array. Nonvolatility implies at least ten years of charge retention, and the data must be stored in a cell after many read/program/erase cycles. The confidence in Flash memory reliability has grown together with the understanding of the single memory cell failure mechanisms.

The high degree of testability [12] allows the detection at wafer level of latent defects which may cause single-cell failures related to programming disturbs, data retention, and oxide defects [13], thus making Flash one of the most reliable nonvolatile memories.

A. Threshold Voltage Distribution

When dealing with a large array of cells, e.g., from tens of thousands to one million, it is very important to understand the type of dispersion given by the large set of cells. The best way to do it is to compare the threshold voltage distribution of the whole array, considering it after UV erasure—that can be considered as the reference state—after CHE programming and after FN erasing.

Fig. 14 shows typical distributions of cell threshold voltages in a large memory array. The UV-erased distribution is pretty narrow and symmetrical. A more accurate analysis would reveal a Gaussian distribution due to random variations of critical dimensions, thickness, and doping which contribute to cause a dispersion of threshold voltages, either directly or through coupling ratios.

The programmed distribution is wider than the UV-erased one, but it is still symmetrical. The enlargement occurs because most of the parameters that cause V_T dispersion of UV-erased cells also impact the threshold shift of programmed cells.

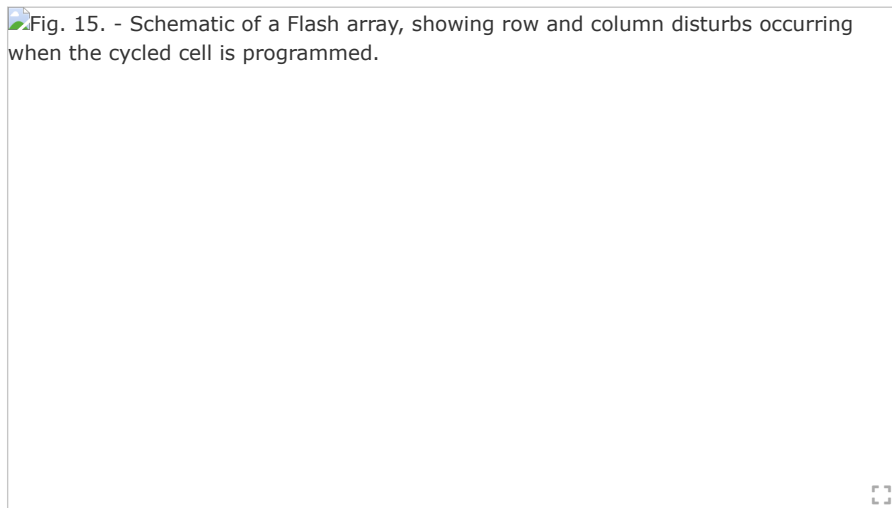
 **Fig. 15.** - Schematic of a Flash array, showing row and column disturbs occurring when the cycled cell is programmed.

Fig. 15. Schematic of a Flash array, showing row and column disturbs occurring when the cycled cell is programmed.

The distribution of threshold voltages after electrical erase is much wider and heavily asymmetrical. A more detailed analysis would show that the bulk of the distribution is again a Gaussian with a standard deviation larger than the one of programmed cells. Cells in this part of the distribution are referred to as “normal” cells. But there is also an exponential tail at low V_T , composed of cells that erase faster than the average, also called “tail” cells.

The dispersion of threshold voltages of normal cells is due to coupling ratio variations, and it has been accurately modeled [14]. Instead, the understanding of the tail cells, although of key importance, is more difficult. In fact, as these cells erase faster than normal cells with the same applied voltage, one should assume that they are somehow “defective.” However, they are just too numerous for being associated with extrinsic defects.

Different models have been presented with the aim to explain the tail cells. For example, a distribution in the polycrystalline structure of the FG, with a barrier height variation at the grain boundaries, would give rise to a local enhancement of the tunnel barrier [15]. Another model explains the tail cells as due to randomly distributed positive charges in the tunnel oxide [16]. This model is solidly based on the well-known existence of donor-like bulk oxide traps and on calculations that show the huge increase of the tunnel current density caused by the presence of an elementary positive charge closed to injecting electrode.

Independently from a consolidated model, it can be stated that the exponential tail of the erased distribution is mostly related to structural imperfections, i.e., intrinsic defects, and it can be minimized by process optimization (for example, working on silicon surface preparation, tunnel oxidation, FG polysilicon optimization) but not eliminated. Flash products must be designed taking into account the existence of such a tail.

B. Program Disturb

The failure mechanisms referred to as “program disturbs” concern data corruption of written cells caused by the electrical stress applied to these cells while programming other cells in the memory array. Two types of program disturbs must be taken into account: row and column disturbs, also referred as gate and drain stress, as schematically reported in Fig. 15, representing a portion of a cell array.

Row disturbs are due to gate stress applied to a cell while programming other cells on the same wordline. If a high voltage is applied to the selected row, all the other cells of that row must withstand the gate stress without losing their data. Depending on the data stored in the cells, data can be lost either by a leakage in the gate oxide or by a leakage in the interpoly dielectric.

Column disturbs are due to drain stress applied to a cell while programming other cells on the same bitline. Under this condition, programmed cells can lose charge by FN tunneling from the FG to the drain (soft erasing). The program disturb depends on the number of cells along bitline and wordline and then depends strongly on the sector organization. The most effective way to prevent disturb propagation is to use block select transistor in a divided bitline and wordline organization to completely isolate each sector. Program disturb really could be a critical issue in Flash memory, and cells and circuits must be designed with safety margins versus the stress sensitivity.

C. Data Retention

As in any nonvolatile memory technology, Flash memories are specified to retain data for over ten years. This means the loss of charge stored in the FG must be as minimal as possible. In updated Flash technology, due to the small cell size, the capacitance is very small and at an operative programmed threshold shift—about 2 V—corresponds a number of electrons in the order of 10^3 to 10^4 . A loss of 20% in this number (around 2–20 electrons lost per month) can lead to a wrong read of the cell and then to a data loss.

Possible causes of charge loss are: 1) defects in the tunnel oxide; 2) defects in the interpoly dielectric; 3) mobile ion contamination; and 4) detrapping of charge from insulating layers surrounding the FG.

The generation of defects in the tunnel oxide can be divided into an extrinsic and an intrinsic one. The former is due to defects in the device structure; the latter to the physical mechanisms that are used to program and erase the cell. The tunnel oxidation technology as well as the Flash cell architecture is a key factor for mastering a reliable Flash technology.

The best interpoly dielectric considering both intrinsic properties and process integration issues has been demonstrated to be a triple layer composed of ONO. For several generations, all Flash technologies have used ONO as their interpoly dielectric.

The problem of mobile ion contamination has been already solved on the EPROM technology, taking particular care with the process control, but in particular using high phosphorus content in intermediate dielectric as a gettering element. [17], [18]. The process control and the intermediate dielectric technology have also been implemented in the Flash process, obtaining the same good results.

Electrons can be trapped in the insulating layers surrounding the floating gate during wafer processing, as a result of the so-called plasma damage, or even during the UV exposure normally used to bring the cell in a well-defined state at the end of the process. The electrons can subsequently detrapp with time, especially at high temperature. The charge variation results in a variation of the floating gate potential and thus in cell V_T decrease, even if no leakage has actually occurred. This apparent charge loss disappears if the process ends with a thermal treatment able to remove the trapped charge.

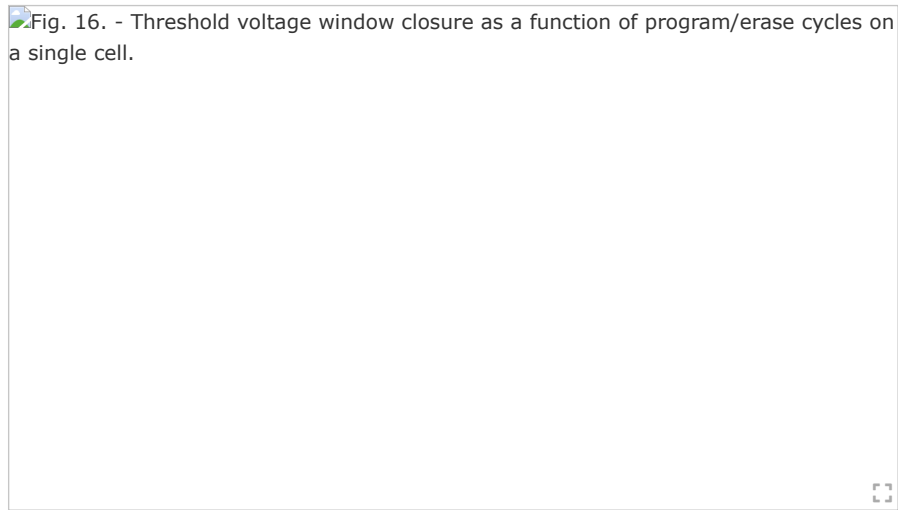
Fig. 16. - Threshold voltage window closure as a function of program/erase cycles on a single cell.

Fig. 16. Threshold voltage window closure as a function of program/erase cycles on a single cell.

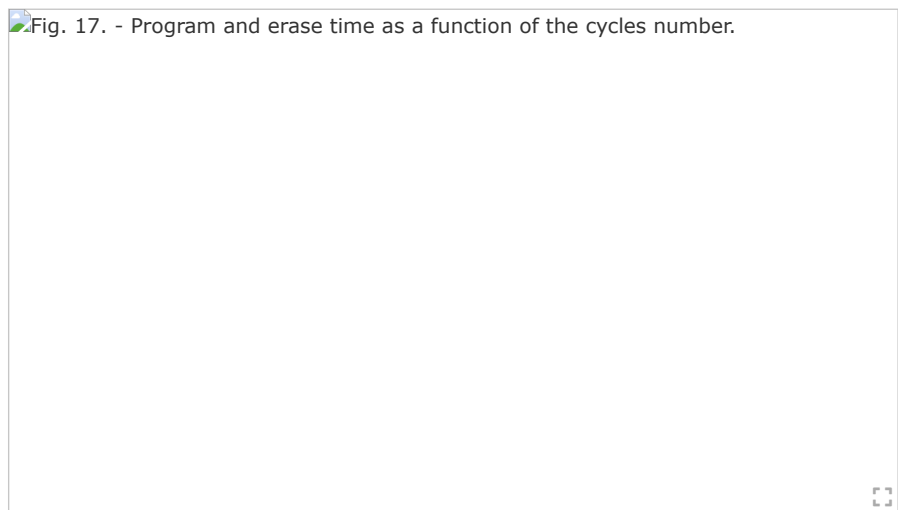
Fig. 17. - Program and erase time as a function of the cycles number.

Fig. 17. Program and erase time as a function of the cycles number.

The retention capability of Flash memories has to be checked by using accelerated tests that usually adopt screening electric fields and hostile environments at high temperature.

D. Programming/Erasing Endurance

 Fig. 18. - Anomalous SILC modeling. The leakage is caused by a cluster of positive charge generated in the oxide during erase (left-hand side). The multitrapped assisted tunneling is used to model SILC: trap parameters are energy and position.



Fig. 18. Anomalous SILC modeling. The leakage is caused by a cluster of positive charge generated in the oxide during erase (left-hand side). The multitrapped assisted tunneling is used to model SILC: trap parameters are energy and position.

Flash products are specified for 10^5 erase/program cycles. Cycling is known to cause a fairly uniform wear-out of the cell performance, mainly due to tunnel oxide degradation, which eventually limits the endurance characteristics [19]. A typical result of an endurance test on a single cell is shown in Fig. 16. As the experiment was performed applying constant pulses, the variations of program and erase threshold voltage levels are described as “program/erase threshold voltage window closure” and give a measure of the tunnel oxide aging. In real Flash devices, where intelligent algorithms are used to prevent V_T window closing, this effect corresponds to a program and erase times increase (see Fig. 17).

 Fig. 19. - Data retention tests at room temperature.



Fig. 19. Data retention tests at room temperature.

In particular, the reduction of the programmed threshold with cycling is due to trap generation in the oxide and to interface state generation at the drain side of the channel, which are mechanisms specific to hot-electron degradation. The evolution of the erase threshold voltage reflects the dynamics of net fixed charge in the tunnel oxide as a function of the injected charge. The initial lowering of the erase V_T is due to a pile-up of positive charge which enhances tunneling efficiency, while the long-term increase of the erase V_T is due to a generation of negative traps.

Cycling wear-out can be reduced by proper device engineering and by optimization of the tunnel oxide process. However, once process and product are qualified for a given endurance specification, no major problems should come from lot-to-lot variation.

Actually, endurance problems are mostly given by single-cell failures, which present themselves like a retention problem after program/erase cycles. In fact, a high field stress on thin oxide is known to increase the current density at low electric field. The excess current component, which causes a significant deviation from the current–voltage curves from the theoretical FN characteristics at low field, is known as stress-induced leakage current (SILC). SILC is clearly attributed to stress-induced oxide defects and, as far as a conduction mechanism, it is attributed to a trap assisted tunneling (see Fig. 18). The main parameters controlling SILC are the stress field, the amount of charge injected during the stress, and the oxide thickness. For fixed stress conditions, the leakage current increases strongly with decreasing oxide thickness [20]– [22].

The effect of cycling on data retention cannot be referred to in the typical cell, but must be studied considering a wide array of cells, looking in particular to the tail distribution. In Fig. 19, we report the results of retention test on a 1-Mb array of cells with 8-nm tunnel oxide in order to enhance the SILC defects in single cells. Retention tests have been performed on arrays cycled 10 and 10^5 times [23]. As can be seen, the amount of cells that lose charge after three years are much more in the case of longer endurance. Data retention after cycling is the issue that definitely limits the tunnel oxide thickness scaling. For very thin oxide, below 8–9 nm, the number of leaky cells becomes so large that even error-correction techniques cannot fix the problem.

Fig. 20. - $D V_T$ as a function of the pulse number for three different channel lengths (the upper axis also shows the gate voltage at each programming step).

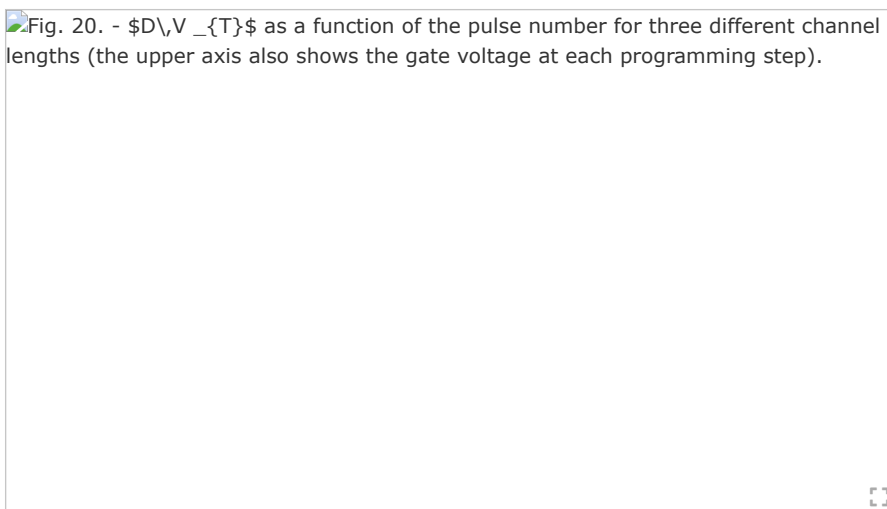


Fig. 20. $D V_T$ as a function of the pulse number for three different channel lengths (the upper axis also shows the gate voltage at each programming step).

SECTION IV. Multilevel Concept

An attractive way to speed up the scaling of Flash memory is offered by the multilevel (ML) concept [24]. The idea is based on the ability to precisely control the amount of charge stored into the floating gate in order to set the threshold voltage V_T of a memory cell within any of a number of different voltage ranges, corresponding to different logical levels. A cell operated with 2^n different levels is capable of storing n bits, the case $n = 1$ being the conventional single-bit cell.

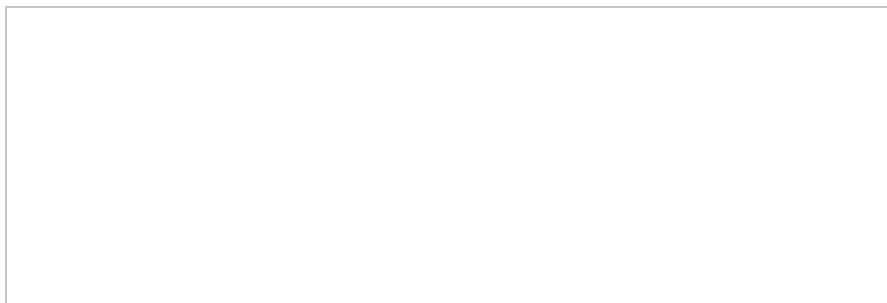


Fig. 21. - Schematic of the control-gate voltage pulses.

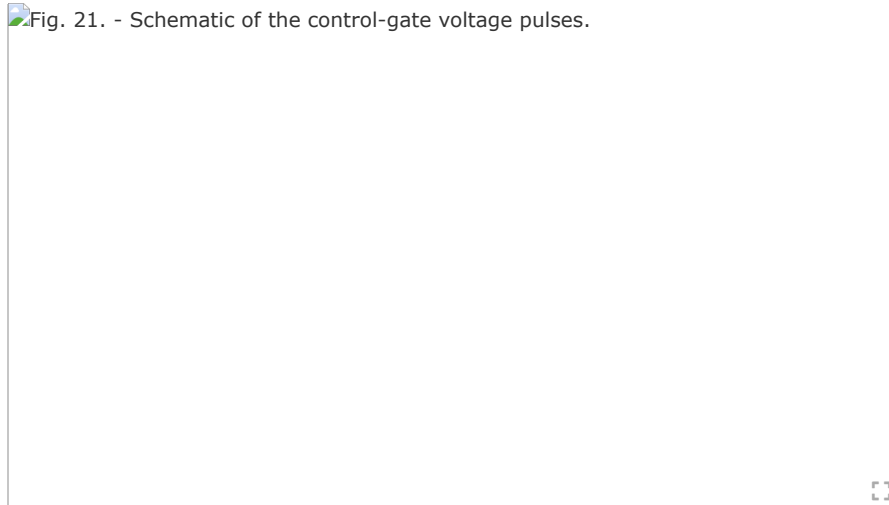


Fig. 21. Schematic of the control-gate voltage pulses.

Fig. 22. - Parallel multilevel sensing architecture. $\text{MSB} = \text{most significant bit}$; $\text{LSB} = \text{less significant bit}$.

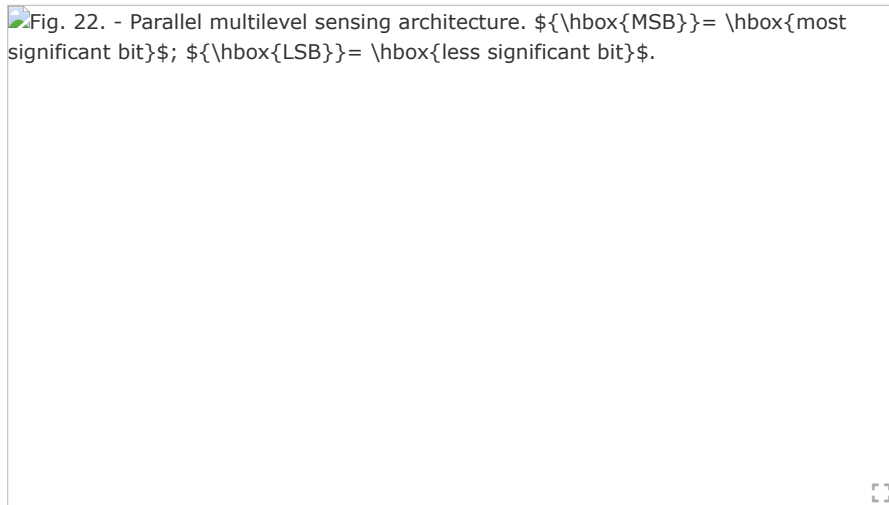


Fig. 22. Parallel multilevel sensing architecture. MSB = most significant bit; LSB = less significant bit.

Three main issues must be afforded when going from conventional to ML Flash [25]. A high programming accuracy is required to obtain narrow V_T distributions; reading operation implies multiple, either serial or parallel, comparison with suitable references to determine the cell status, requiring accurate and fast current sensing; V_T window and read voltage are larger while read margins are smaller than the single-bit case, this for allocating all levels, requiring improved reliability and/or error-correction circuitry. These key points will be discussed with reference to a common-ground NOR architecture.

A. Multilevel Flash Programming

CHE programming has been shown to give, under proper conditions, a linear relationship with unit slope between programming gate voltage V_{GP} and V_T variation [26], independently of cell parameters (see Fig. 20). Very tight V_T distributions can be obtained by combining a program-and-verify technique with a staircase V_{GP} ramp (see Fig. 21). In fact, this method should theoretically lead to a V_T distribution width for any state not larger than ΔV_{GP} . Indeed, neglecting any error due to sense amplifier inaccuracy or voltage fluctuations, the last programming pulse applied to a cell will cause its threshold voltage to be shifted above the program verify decision level by an amount at most as large as ΔV_{GP} . It follows that by decreasing ΔV_{GP} , it is possible to increase the programming accuracy. Obviously, this is paid in terms of a larger number of programming pulses together with verify phases and, therefore, with a longer programming time.

Hence, the best accuracy/time tradeoff must be chosen for each case considering the application specification.

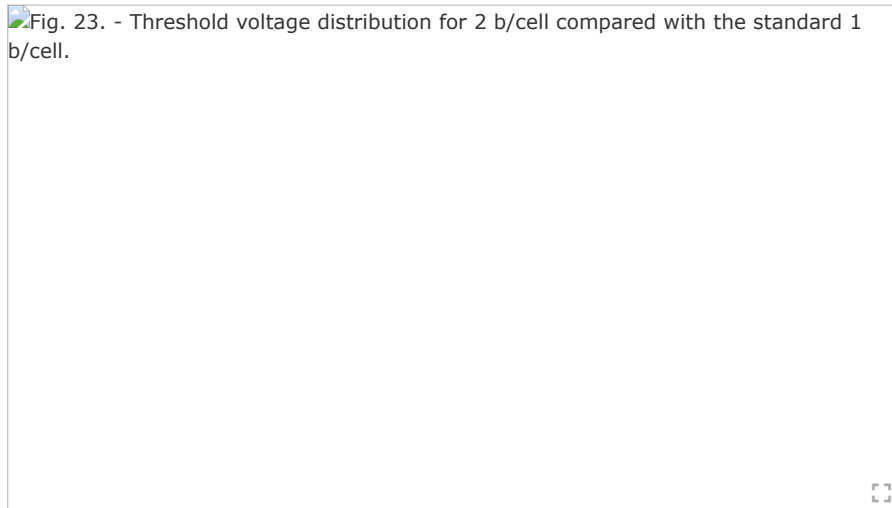
 Fig. 23. - Threshold voltage distribution for 2 b/cell compared with the standard 1 b/cell.

Fig. 23. Threshold voltage distribution for 2 b/cell compared with the standard 1 b/cell.

However, high programming throughput, equal to 1-b/cell devices, is normally achieved via a large internal program parallelism, which is possible because cells need a low programming current in ML staircase programming. To do that, ML devices operate with a program write buffer, whose typical length is 32–64 bytes, i.e., 128–256 cell data length.

Also, evolution to 3–4 b/cell will not have an impact on programming throughput. In fact, program pulses and verify phases increase proportionally with the number of bits per cell, thus keeping roughly constant the effective byte programming time.

Despite a not-negligible programming current, another advantage in using CHE programming for multilevel devices is to avoid the appearance of erratic bits that instead can be a potential failure mode affecting FN programming. In fact, erratic bit behavior was observed in the FN erase of standard NOR memories [27] but, for its nature, it should be present in every tunneling process [28].

B. Reading Operation

In order to have a fast reading operation in the NOR cell, a parallel sensing approach can be used [29]. The cell current, obtained in reading conditions, is simultaneously compared with three currents provided by suitable reference cells (see Fig. 22). The comparison results are then converted to a binary code, whose content can be 11, 01, 10, or 00, due to the multilevel nature. In Fig. 23, we report the threshold voltage distribution of a 2-b/cell memory. The 11, 10, and 01 cell distribution will give rise to a different current distribution, measured at fixed V_{read} , while the 00 cell distribution does not drain current as well as the programmed level of a standard 1-b/cell device. High read data rate, via page or burst mode, is normally supported by large internal read parallelism.

A parallel sensing approach does not seem transferable to 3- or 4-b/cell generations because of the exponential increase, $2^n - 1$, in comparators number, respectively 7 or 15 per cell, that means exponential increase in sensing area and current consumption. At this moment, a serial sensing approach, e.g., dichotomic, or a mixed serial-parallel is considered the more suitable approach. Serial sensing is also useful for a 2-b/cell device when high-speed random access is not necessary, e.g., in Flash Cards applications.

C. Data Retention

One of the main concerns about multilevel is the reduced margin toward the charge loss, compared with the 1-b/cell approach. We can basically divide the problem of data retention into two different issues.

The first is related to the extrinsic charge loss, i.e., to a single bit that randomly can have different behaviors with respect to the average and that usually form a tail in a standard distribution. It is well known that extrinsic charge loss strongly depends on tunnel oxide retention electric field and that this issue can become more critical if an enhanced cell threshold range has to be used to allocate the 2^n levels [30]. This problem is usually solved with the introduction of the error correction code (ECC), whose correction power must be chosen as a function of the technology and of the specification required to the memory products.

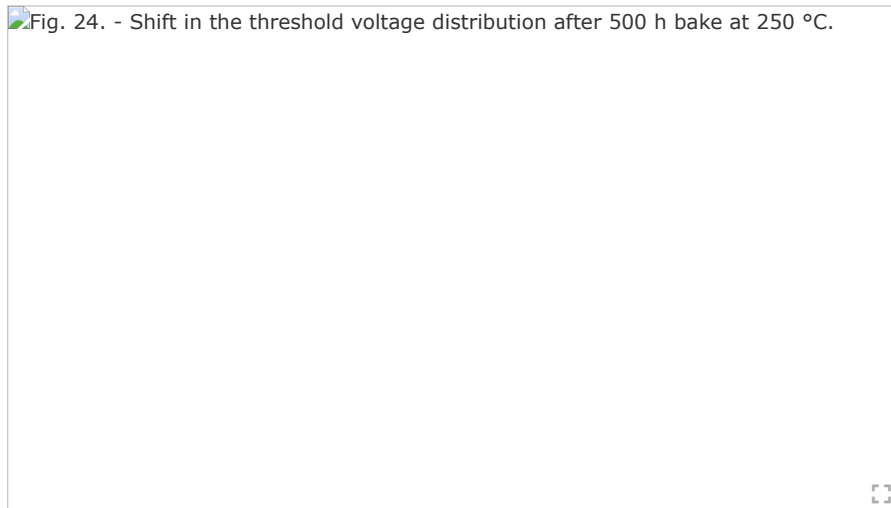
 Fig. 24. - Shift in the threshold voltage distribution after 500 h bake at 250 °C.

Fig. 24. Shift in the threshold voltage distribution after 500 h bake at 250 °C.

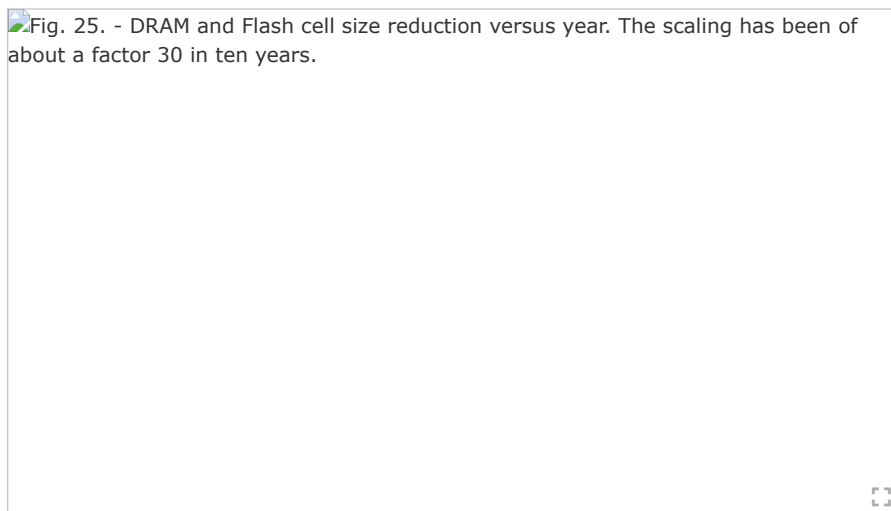
 Fig. 25. - DRAM and Flash cell size reduction versus year. The scaling has been of about a factor 30 in ten years.

Fig. 25. DRAM and Flash cell size reduction versus year. The scaling has been of about a factor 30 in ten years.

The second one is related to the intrinsic charge loss, i.e., to the behaviors of the Gaussian part of a cell distribution, that must be characterized and defined as a function of the different level distributions. In order to study the data retention on multilevel memories, usually tests at high-temperature bake on programmed cells are performed. A result of data retention after bake (500 h, 250 °C) is shown in Fig. 24, on one million cells [31].

The maximum V_T shift, which occurs for the uppermost level, is about 0.1 V. This means the spacing between levels is reduced by a very small amount. It is interesting to note that the three programmed levels are shifted by an amount proportional to their respective programmed ΔV_T , so that the spacing between adjacent levels is reduced by only a fraction of the observed maximum shift.

SECTION V.**Evolution and Scaling Trend**

The Flash memories were commercially introduced in the early 1990s and since that time they have been able to follow the Moore law or, better, the scaling rules imposed by the market. Fig. 25 reports in a logarithmic scale the Flash cell size as a function of time, from 1992 to 2002. It turns out that the reduction of the cell size has been about a factor 30 in those ten years, closely following the scaling of the DRAM, today still considered as the reference memory technology that sets the pace to the technology node evolution. More specifically, the NOR Flash cell has scaled from $4.2 \mu\text{m}^2$ for the $0.6\text{-}\mu\text{m}$ technology node to the present cell size of $0.16 \mu\text{m}^2$ at the $0.13\text{-}\mu\text{m}$ node.

Moreover, considering the multilevel approach for the Flash cell with the capability to store two bits in the same cell, as presented in Section IV, not only the scaling trend but even the bit size itself is well aligned with the DRAM one.

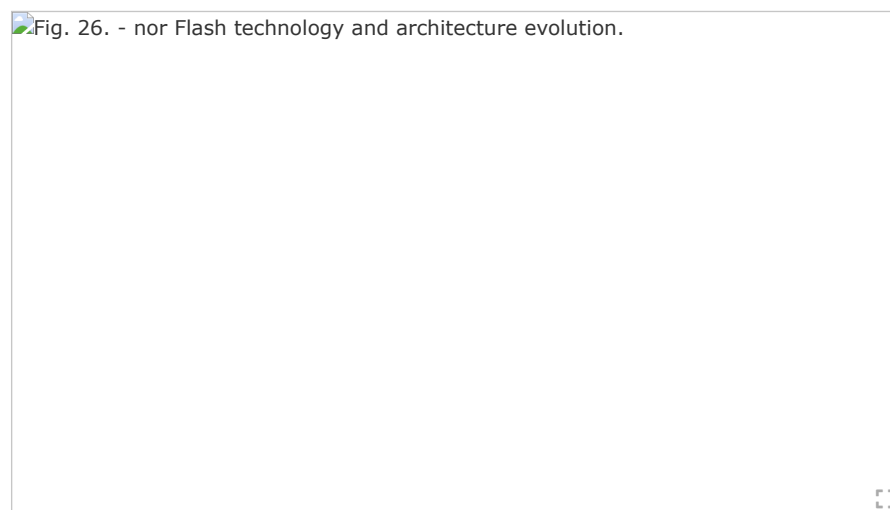


Fig. 26. nor Flash technology and architecture evolution.

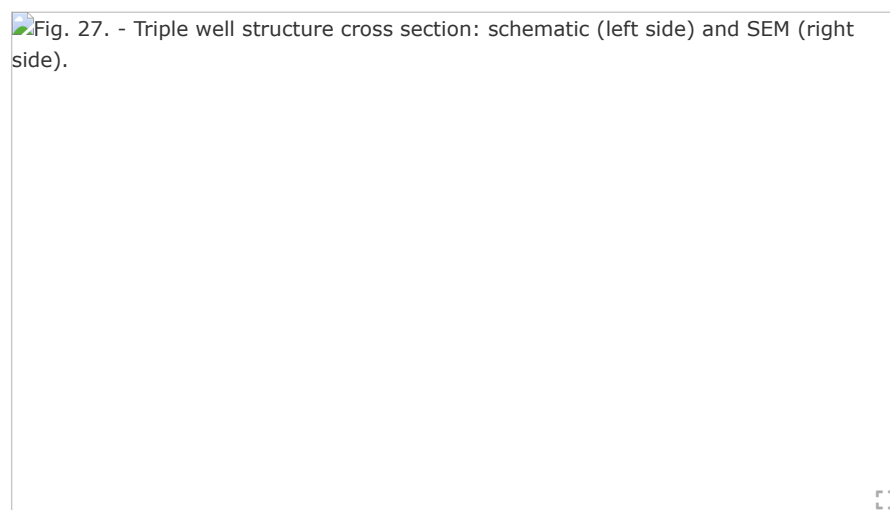


Fig. 27. Triple well structure cross section: schematic (left side) and SEM (right side).

Together with the Flash cell scaling, there has also been an evolution of the Flash product specification and application. Three main generations can be considered, well differentiated as a technology node, process complexity, and specification.

- *First generation (1990–1997).* The Flash applications were mainly “EPROM replacement.” The products were characterized by a single array (bulk), with memory density from 256 kb to 2 Mb. The program and erase algorithms were controlled externally and all the product were dual voltage: 12 V for the write operations and 5 V for the power supply. Cycling specification was limited to 10^4 .
- *Second generation (1995–2000).* The Flash memory has become the right nonvolatile memory technology for code storage application, where software updates must be performed on the field. In particular, portable systems, mainly cellular phones, were strongly interested in this feature.

The cellular phone applications brought a lot of innovations:

- The density was increased from 1 to 16 Mb and sectors were introduced, instead of a single (bulk) array, in order to allow different use of the memory (some sectors can be used to store code while others to store data, with different requirements in terms of cycling). Sector density was from 10 to 256 kb.
- A single voltage supply pin (5 or 3 V according to the system specification) substituted the two high-voltage and low-voltage pins previously used. The need to be programmed on field, without the possibility to have the high voltage from an external pin, has developed the technology to internally generate the writing voltages using charge-pump techniques. A high-voltage supply is sometimes still used, but limited to the first programming operation in the system manufacturing line, to improve the throughput.
- Algorithms to perform all the operation on the array—reading programming and erasing—were embedded into the device in order to avoid the need for an external microcontroller.
- 10^5 writing cycles were introduced as a specification. More than effectively needed by the system, this high endurance is the result of a highly reliable technology.
- *Third generation (from 1998 on).* The portable system specifications push toward Flash memory products that look more and more like an application-specific memory. Obviously, the density is one of the most important parameters, and devices well beyond 64 Mb will be realized entering the Flash in the gigabit era. The sectorization is becoming more complex, and dual or multiple bank devices have already been presented. In these devices, different groups of sectors (banks) can be differently managed: at the same time one sector belonging to a bank can be read while another one, inside a different bank, can be programmed or erased. Also, following the general trend of reducing the power supply, the device supply is scaling to 1.8 V (with the consequent difficulties of internally generating high voltages starting from this low supply voltage value) and will go down to 1.2 V. Another issue, becoming more and more important, is the high data throughput, in particular considering the density increase. Burst mode is often used in order to speed up the reading operation and quickly download the software content, reaching up to 50 MB/s.

The introduction of the different generation as well as the reduction of the cell size has been made possible by the developments of Flash technology and process, and of cell architecture.

For what concerns the process architecture, all the main technology steps that have allowed the evolution of the CMOS technology have also been used for Flash. In Fig. 26, the different cell cross sections as a function of the different technology node are reported. For every generation, the main innovative introduced steps are pointed out. It turns out that the evolution of the different generations has been sustained by an increased process complexity, from the one gate oxide and one metal process with standard local oxidation of silicon isolation at the $0.8\text{-}\mu\text{m}$ technology node, to the two gate oxides, three metals, and shallow trench isolation at the $0.13\text{-}\mu\text{m}$ node. In between is the introduction of tungsten plug, of self-aligned silicided junctions and gates, and the wide use of chemical mechanical polishing steps. But one of the most crucial technologies for Flash evolution was the high-energy implantation development that has allowed the introduction of the triple well architecture (see Fig. 27). With this process module, further development of the single-voltage products has been possible, allowing the easy management of the negative voltage required

to erase the cell and, furthermore, the possibility to completely change the erasing scheme of the cell.

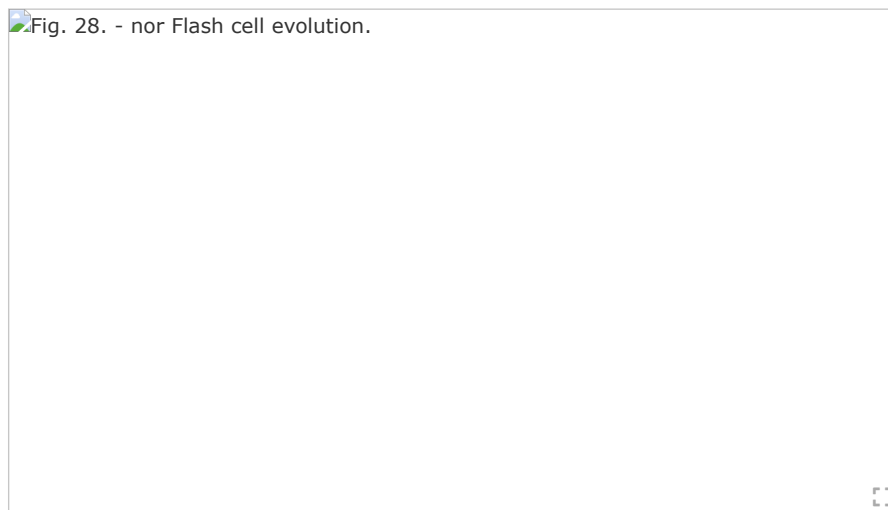


Fig. 28. nor Flash cell evolution.

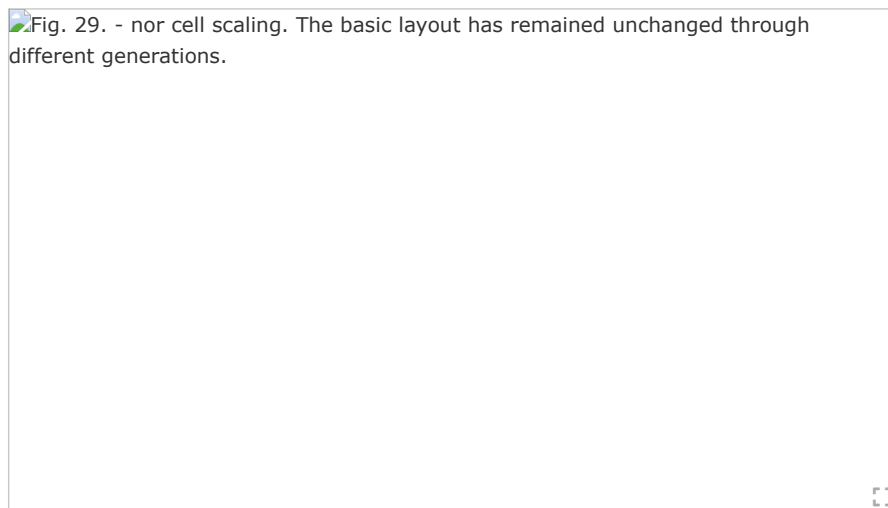


Fig. 29. nor cell scaling. The basic layout has remained unchanged through different generations.

In fact, as reported in Fig. 28, the cell programming and erasing applied voltages have been changed as a function of the different generation, always staying inside the CHE programming and the FN erasing. The first generation of cells was erased, applying the high voltage to the source junction and then extracting electrons from the FG-source overlap region (source erase scheme). This way was too expensive in terms of parasitic current, as the working conditions were very close to the junction breakdown. Moving to the second generation with the single-voltage devices, the voltage drop between the source and the FG was divided, applying a negative voltage to the control gate and lowering the source bias to the external supply voltage (negative gate source erase scheme).

Finally, with the exploitation of the triple well also for the array, the erasing potential is now divided between the negative CG and the positive bulk (the isolated p-well) of the array, moving the tunneling region from the source to the whole cell channel (channel erase scheme). In this way, electrons are extracted from the FG all along the channel without any further parasitic current contribution from the source junction, consequently reducing the erase current amount of about three orders of magnitude; the latter being a clear benefit for battery saving in portable low-voltage applications.

The NOR Flash cell is forecasted to scale again following the International Technology Roadmap of Semiconductors (ITRS) [32]. The introduction of the 130-nm technology node has occurred in 2002–2003 with a cell size of $0.16 \mu\text{m}^2$ [33], following the $10\text{-}\lambda^2$ golden rule for the cell area scaling, where λ is the technology node. The representation of the memory cell size in terms of number of λ^2 is a usual way to compare different technology with the same metric; for example, the DRAM cell size is today quoted to stay in the range of $6\text{--}8 \lambda^2$.

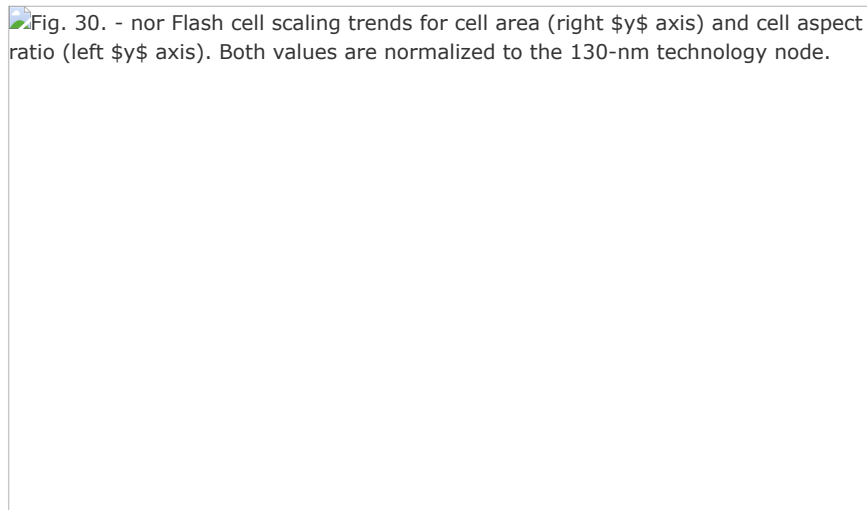
Fig. 30. - nor Flash cell scaling trends for cell area (right y axis) and cell aspect ratio (left y axis). Both values are normalized to the 130-nm technology node.

Fig. 30. nor Flash cell scaling trends for cell area (right y axis) and cell aspect ratio (left y axis). Both values are normalized to the 130-nm technology node.

The next technology step for the NOR Flash will be the 90-nm technology node in 2004–2005. The cell size is expected to stay in the range of $10\text{--}12 \lambda^2$, translating to a cell area of $0.1\text{--}0.08 \mu\text{m}^2$. As reported again in Fig. 29, the cell basic layout and structure has remained unchanged through the different generations. The area scales through the scaling of both the x and y pitch. Basically, this must be done contemporarily reducing the active device dimensions, effective length (L_{eff}) and width (W_{eff}), and the passive elements, such as contact dimension, contact to gate distance, and so on.

For future generation technology nodes, i.e., the 65 nm in 2007 and the 45 nm in 2010, as forecasted by ITRS, the Flash cell reduction will face challenging issues. In fact, while the passive elements will follow the standard CMOS evolution, benefiting from all the technology steps and process modules proposed for the CMOS logic (like advanced lithography for contact size, copper for metallization in very tight pitch), the active elements will be limited in the scaling. In particular, the effective channel length will be limited by the possibility to further scale the active dielectric, i.e., the tunnel oxide and the interpoly ONO. As already presented in Section III, the tunnel oxide thickness scaling is limited by intrinsic issues related to the Flash cell reliability, in particular the charge retention one, especially after many writing cycles. Although the direct tunneling, preventing the ten-year retention time, occurs at $6\text{--}7$ nm, SILC considerations push the tunnel thickness limit to no less than $8\text{--}9$ nm. Moreover, the effective width reduction could be limited by the read current reduction, strongly proportional to the W_{eff} , then impacting the access time.

Scaling the technology node, while the cell x pitch will more and more approach the 2λ , the y -pitch scaling will be limited by the cell gate scaling. Hence, for the 65- and 45-nm technology nodes, it is expected to have smaller cell size but with an increased number of λ^2 , from 10 to 14. In particular, the cell aspect ratio, i.e., the y pitch over the x pitch, will continue to rise, due to the slowdown of the L_{eff} reduction. Fig. 30 reports the cell area and the cell-aspect ratio versus the technology node, both normalized at 130 nm. As can be observed, the cell area will be roughly one half at 90 nm (same number of $10\text{--}12 \lambda^2$) and will decrease, but with slower trend at 65 and 45 nm. The cell-aspect ratio will continue to increase, almost doubling the one at 130 nm when the technology node will reach 45 nm.

SECTION VI.
Summary

With more than ten years of consolidated know-how and thanks to its flexibility and cost characteristics, Flash memory is today a largely utilized, well-consolidated, and mature technology for nonvolatile memory application.

Flash sales represent a considerable amount of the overall semiconductor market. In particular, the NOR Flash is today the most diffused architecture, being able to serve both the code and the data storage market.

The cell is basically a floating-gate MOS transistor, programmed by CHE and erased by Fowler–Nordheim tunneling. The main reliability issues, like charge retention and endurance, have been extensively studied and the physical mechanism well understood in such a way to guarantee the present specification requirements.

The Flash cell scaling has been demonstrated to be really possible and to be able to follow the Moore's law down to the 130-nm technology generations. The technology development and the consolidated know-how will sustain the scaling trend down to the 90- and 65-nm technology nodes as forecasted by the ITRS.

One of the crucial issues to be solved to allow cell scaling below the 65-nm node is the tunnel oxide thickness reduction, as tunnel thinning is limited by intrinsic (direct tunneling) and extrinsic (SILC) mechanisms.

At each technology node, the multilevel approach will increase the memory efficiency, almost doubling the density at the same chip size, enlarging the application range, and reducing the cost per bit.

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Introduction to Flash Memory

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Invited Paper

The most relevant phenomenon of this past decade in the field of semiconductor memories has been the explosive growth of the Flash memory market, driven by cellular phones and other types of electronic portable equipment (palm top, mobile PC, mp3 audio player, digital camera, and so on). Moreover, in the coming years, portable systems will demand even more nonvolatile memories, either with high density and very high writing throughput for data storage application or with fast random access for code execution in place. The strong consolidated know-how (more than ten years of experience), the flexibility, and the cost make the Flash memory a largely utilized, well-consolidated, and mature technology for most of the nonvolatile memory applications. Today, Flash sales represent a considerable amount of the overall semiconductor market.

Although in the past different types of Flash cells and architectures have been proposed, today two of them can be considered as industry standard: the common ground NOR Flash, that due to its versatility is addressing both the code and data storage segments, and the NAND Flash, optimized for the data storage market.

This paper will mainly focus on the development of the NOR Flash memory technology, with the aim of describing both the basic functionality of the memory cell used so far and the main cell architecture consolidated today. The NOR cell is basically a floating-gate MOS transistor, programmed by channel hot electron and erased by Fowler–Nordheim tunneling. The main reliability issues, such as charge retention and endurance, will be discussed, together with the understanding of the basic physical mechanisms responsible. Most of these considerations are also valid for the NAND cell, since it is based on the same concept of floating-gate MOS transistor.

Furthermore, an insight into the multilevel approach, where two bits are stored in the same cell, will be presented. In fact, the exploitation of the multilevel approach at each technology node allows the increase of the memory efficiency, almost doubling the density at the same chip size, enlarging the application range, and reducing the cost per bit.

Finally, the NOR Flash cell scaling issues will be covered, pointing out the main challenges. The Flash cell scaling has been demonstrated to be really possible and to be able to follow the Moore's law down to the 130-nm technology generations. The technology development and the consolidated know-how is expected to sustain the scaling trend down to the 90- and 65-nm technology nodes as forecasted by the International Technology Roadmap of Semiconductors. One of the crucial issues to be solved

to allow cell scaling below the 65-nm node is the tunnel oxide thickness reduction, as tunnel thinning is limited by intrinsic and extrinsic mechanisms.

Keywords—Flash evolution, Flash memory, Flash technology, floating-gate MOSFET, multilevel, nonvolatile memory, NOR cell, scaling.

I. INTRODUCTION

The semiconductor market, for the long term, has been continuously increasing, even if with some valleys and peaks, and this growing trend is expected to continue in the coming years (see Fig. 1). A large amount of this market, about 20%, is given by the semiconductor memories, which are divided into the following two branches, both based on the complementary metal–oxide–semiconductor (CMOS) technology (see Fig. 2).

- The volatile memories, like SRAM or DRAM, that although very fast in writing and reading (SRAM) or very dense (DRAM), lose the data contents when the power supply is turned off.
- The nonvolatile memories, like EPROM, EEPROM, or Flash, that are able to balance the less-aggressive (with respect to SRAM and DRAM) programming and reading performances with nonvolatility, i.e., with the capability to keep the data content even without power supply.

Thanks to this characteristic, the nonvolatile memories offer the system a different opportunity and cover a wide range of applications, from consumer and automotive to computer and communication (see Fig. 3).

The different nonvolatile memory families can be qualitatively compared in terms of flexibility and cost (see Fig. 4). Flexibility means the possibility to be programmed and erased many times on the system with minimum granularity (whole chip, page, byte, bit); cost means process complexity and in particular silicon occupancy, i.e., density or, in simpler words, cell size. Considering the flexibility-cost plane, it turns out that Flash offers the best compromise between these two parameters, since they have the smallest cell size

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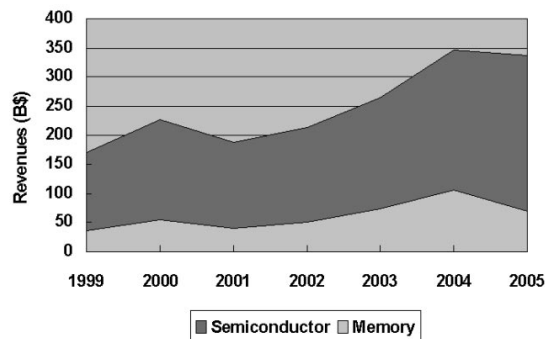


Fig. 1. Semiconductor market: revenues versus year. The bottom wave refers to the semiconductor memory amount.

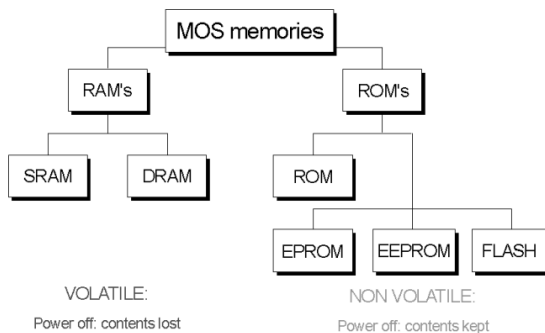


Fig. 2. MOS memory tree.

	Cell Phone	Consumer	Automotive	Computer & Communication
EPROM	Analog, Residential	Games, Set Top Box	Engine Mgt.	HDD, Copiers, Fax, Switching
FLASH	Digital (GSM)	Set Top Box, PDA	All Power Train, Car Navigation, ABS, GPS	HDD, PC Bios, CDROM
EEPROM	Digital (GSM)	Audio, Video	All Car Body	PC SPD, Graphic boards, Printers



Fig. 3. Main nonvolatile memory applications.

(one transistor cell) with a very good flexibility (they can be electrically written on field more than 100 000 times, with byte programming and sectors erasing).

The most relevant phenomenon of this past decade in the field of semiconductor memories has been the explosive growth of the Flash memory market, driven by cellular phones and other types of electronic portable equipment (palm top, mobile PC, mp3 audio player, digital camera, and so on). Moreover, in the coming years, portable systems will demand even more nonvolatile memories, either with high density and very high writing throughput for data storage application or with fast random access for code execution in place.

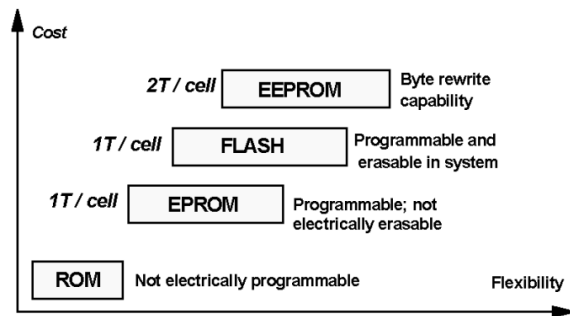


Fig. 4. Nonvolatile memory (NVM) qualitative comparison in the flexibility–cost plane. A common feature of NVMs is to retain the data even without power supply.

Based on these market needs, a well-known way to classify Flash products and the relative technologies is that of defining two major application segments:

- code storage, where the program or the operating system is stored and is executed by the microprocessor or microcontroller;
- data (or mass) storage, where data files for image, music, and voice are recorded and read sequentially.

Different type of Flash cells and architectures have been proposed in the past (see Fig. 5). They can be divided in terms of access type, parallel or serial, and in terms of the utilized programming and erasing mechanism, Fowler–Nordheim tunneling (FN), channel hot electron (CHE), hot-holes (HH), and source-side hot electron (SSHE). Among all of these architectures, today two can be considered as industry standard: the common ground NOR Flash [1]–[3], that due to its versatility is addressing both the code and data storage segments, and the NAND Flash, optimized for the data storage market [4], [5].

In the following, the basic concepts, the reliability issues, the evolution, and scaling trends will be presented only for the NOR Flash cell, but most of these considerations are also valid for the NAND since both of them are based on the concept of floating-gate MOS transistor.

II. NOR FLASH CELL

In 1971, Frohman-Bentchkowsky presented a floating gate transistor in which hot electrons were injected and stored [6], [7]. From this original work, the erasable programmable read only memory (EPROM) cell, programmed by CHE and erased by ultraviolet (UV) photoemission, has been developed. The EPROM technology became the most important nonvolatile memory in the 1980s. In the same period, the Flash EEPROM was proposed, basically an EPROM cell, with the possibility to be electrically erased [8]. The name Flash was given to represent the fact that the whole memory array could be erased in the same (fast) time.

The first Flash product was presented in 1988 [9]. In terms of applications, initially Flash products were mainly used as an “EPROM replacement,” offering the possibility to be erased on system, avoiding the cumbersome UV erase oper-

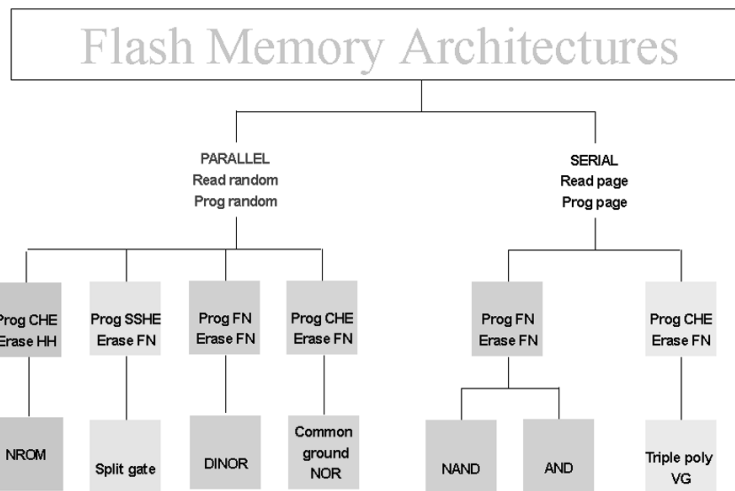


Fig. 5. The family tree of Flash memory cell architecture. The actual industry standard are: 1) The NOR for code and data storage application and 2) NAND only for data storage.

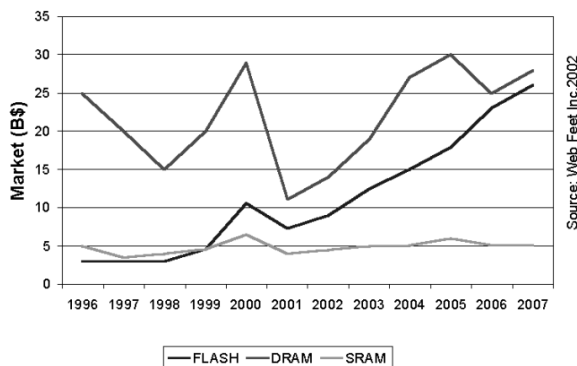


Fig. 6. Semiconductor memory market for the main memory, i.e., DRAM, Flash, and SRAM.

ation. But the Flash market did not take off until this technology was proven to be reliable and manufacturable. In the late 1990s, the Flash technology exploded as the right non-volatile memory for code and data storage, mainly for mobile applications. Starting from 2000, the Flash memory can be considered a really mature technology: more than 800 million units of 16-Mb equivalent NOR Flash devices were sold in that year.

In Fig. 6, the Flash market is reported and compared with the DRAM and SRAM one [10]. It can be seen that the Flash market became and has stayed bigger than the SRAM one since 1999. Moreover, the Flash market is forecasted to be above \$20 billion in three or four years from now, reaching the DRAM market amount, and only smoothly following the DRAM oscillating trend, driven by the personal computer market. In fact, portable systems for communications and consumer markets, which are the drivers of the Flash market, are forecasted to continuously grow in the coming years.

In the following, we briefly describe the basics of the Flash cell functionality.

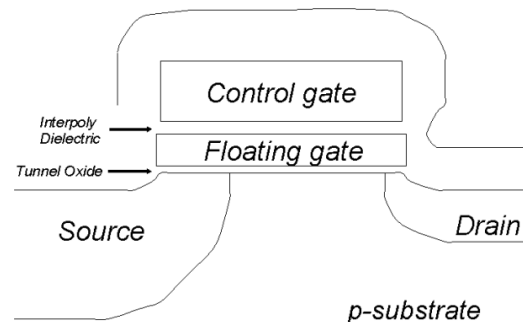


Fig. 7. Schematic cross section of a Flash cell. The floating-gate structure is common to all the nonvolatile memory cells based on the floating-gate MOS transistor.

A. Basic Concept

A Flash cell is basically a floating-gate MOS transistor (see Fig. 7), i.e., a transistor with a gate completely surrounded by dielectrics, the floating gate (FG), and electrically governed by a capacitively coupled control gate (CG). Being electrically isolated, the FG acts as the storing electrode for the cell device; charge injected in the FG is maintained there, allowing modulation of the “apparent” threshold voltage (i.e., V_T seen from the CG) of the cell transistor. Obviously the quality of the dielectrics guarantees the non-volatility, while the thickness allows the possibility to program or erase the cell by electrical pulses. Usually the gate dielectric, i.e., the one between the transistor channel and the FG, is an oxide in the range of 9–10 nm and is called “tunnel oxide” since FN electron tunneling occurs through it. The dielectric that separates the FG from the CG is formed by a triple layer of oxide–nitride–oxide (ONO). The ONO thickness is in the range of 15–20 nm of equivalent oxide thickness. The ONO layer as interpoly dielectric has been introduced in order to improve the tunnel oxide quality. In fact, the

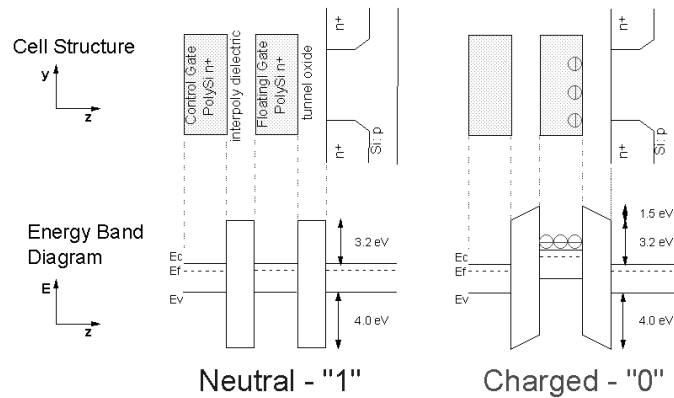


Fig. 8. Schematic energy band diagram (lower part) as referred to a floating gate MOSFET structure (upper part). The left side of the figure is related to a neutral cell, while the right side to a negatively charged cell.

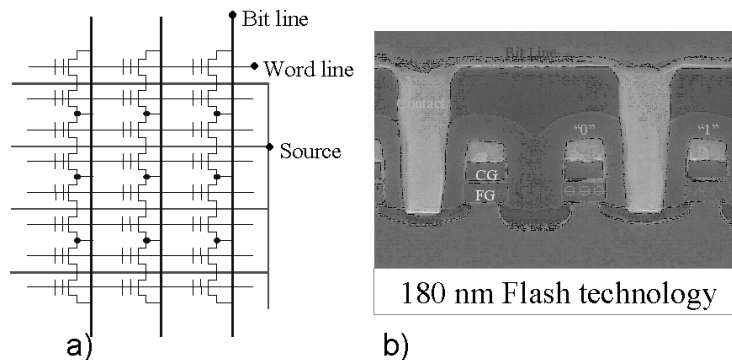


Fig. 9. (a) NOR Flash array equivalent circuit. (b) Flash memory cell cross section.

use of thermal oxide over polysilicon implies growth temperature higher than 1100 °C, impacting the underneath tunnel oxide. High-temperature postannealing is known to damage the thin oxide quality.

If the tunnel oxide and the ONO behave as ideal dielectrics, then it is possible to schematically represent the energy band diagram of the FG MOS transistor as reported in Fig. 8. It can be seen that the FG acts as a potential well for the charge. Once the charge is in the FG, the tunnel and ONO dielectrics form potential barriers.

The neutral (or positively charged) state is associated with the logical state “1” and the negatively charged state, corresponding to electrons stored in the FG, is associated with the logical “0.”

The “NOR” Flash name is related to the way the cells are arranged in an array, through rows and columns in a NOR-like structure. Flash cells sharing the same gate constitute the so-called wordline (WL), while those sharing the same drain electrode (one contact common to two cells) constitute the bitline (BL). In this array organization, the source electrode is common to all of the cells [Fig. 9(a)].

A scanning electron microscope (SEM) cross section along a bitline of a Flash array is reported in Fig. 9(b), where three cells can be observed, sharing two by two the drain

contact and the sourceline. This picture can be better understood considering the layout of a cell (see Fig. 10) and the two schematic cross sections, along the y direction (bitline) and the x direction (wordline). The cell area is given by the x pitch times the y pitch. The x pitch is given by the active area width and space, considering also that the FG must overlap the oxide field. The y pitch is constituted by the cell gate length, the contact-to-gate distance, half contact, and half sourceline. It is evident, as reported in Fig. 9(b), that both contact and sourceline are shared between two adjacent cells.

B. Reading Operation

The data stored in a Flash cell can be determined measuring the threshold voltage of the FG MOS transistor. The best and fastest way to do that is by reading the current driven by the cell at a fixed gate bias. In fact, as schematically reported in Fig. 11, in the current–voltage plane two cells, respectively, logic “1” and “0” exhibit the same transconductance curve but are shifted by a quantity—the threshold voltage shift (ΔV_T)—that is proportional to the stored electron charge Q .

Hence, once a proper charge amount and a corresponding ΔV_T is defined, it is possible to fix a reading voltage in such

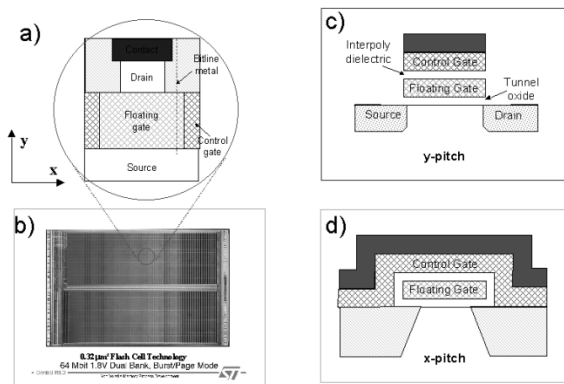


Fig. 10. The NOR Flash cell. (a) Basic layout. (b) Updated Flash product (64-Mb, 1.8-V Dual bank). (c) and (d) are, respectively, the schematic cross section along bitline (y pitch) and wordline (x pitch).

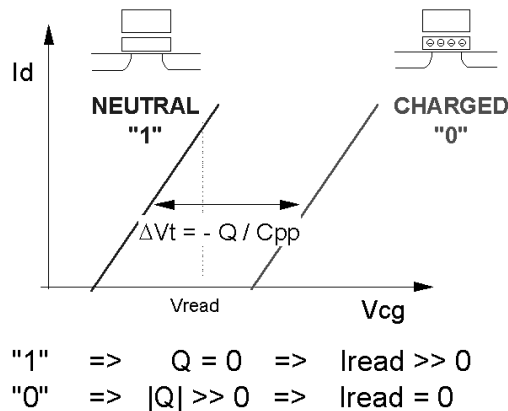


Fig. 11. Floating-gate MOSFET reading operation.

a way that the current of the “1” cell is very high (in the range of tens of microamperes), while the current of the “0” cell is zero, in the microampere scale. In this way, it is possible to define the logical state “1” from a microscopic point of view as no electron charge (or positive charge) stored in the FG and from a macroscopic point of view as large reading current. Vice versa, the logical state “0” is defined, respectively, by electron charge stored in the FG and zero reading current.

C. Writing Operation

Considering Fig. 8, the problem of writing an FG cell corresponds to the physical problem of forcing an electron above or across an energy barrier. The problem can be solved exploiting different physical effects [11]. In Fig. 12, the three main physical mechanisms used to write an FG memory cell are sketched.

- The CHE mechanism, where electrons gain enough energy to pass the oxide–silicon energy barrier, thanks to the electric field in the transistor channel between source and drain. In fact, the electron energy distribution presents a tail in the high energy side that can be modulated by the longitudinal electric field.

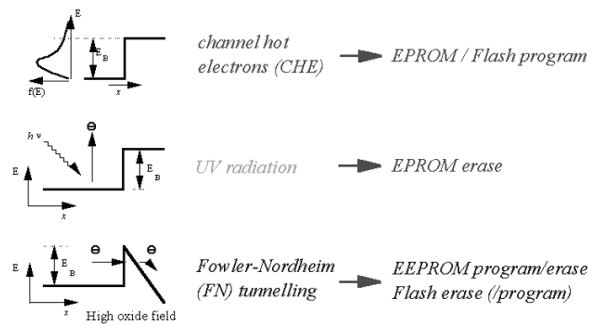


Fig. 12. Writing mechanism in floating-gate devices.

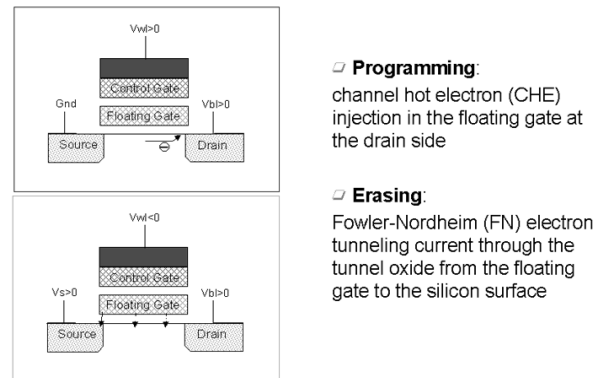


Fig. 13. NOR Flash writing mechanism.

- The photoelectric effect, where electrons gain enough energy to surmount the barrier thanks to the interaction with a photon with energy $h\nu$ larger than the barrier itself. For silicon–dioxide, this corresponds to UV radiation. This mechanism is the one originally used in EPROM’s products to erase the entire device.
- The Fowler–Nordheim electron tunneling mechanism is a quantum-mechanical tunnel induced by an electric field. Applying a strong electric field (in the range of 8–10 MV/cm) across a thin oxide, it is possible to force a large electron tunneling current through it without destroying its dielectric properties.

A NOR Flash memory cell is programmed by CHE injection in the FG at the drain side and it is erased by means of the FN electron tunneling through the tunnel oxide from the FG to the silicon surface (see Fig. 13).

III. RELIABILITY

Many issues have to be addressed when, from the theoretical model of a single cell, a Flash product has to be realized, integrating millions of cells in an array. Nonvolatility implies at least ten years of charge retention, and the data must be stored in a cell after many read/program/erase cycles. The confidence in Flash memory reliability has grown together with the understanding of the single memory cell failure mechanisms.

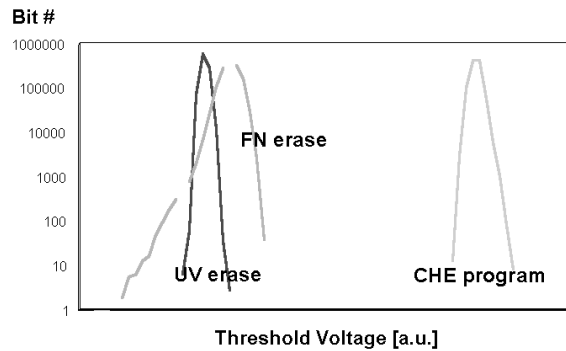


Fig. 14. Threshold voltage distribution of a 1-Mb Flash array after UV erasure, after CHE programming, and after FN erasure.

The high degree of testability [12] allows the detection at wafer level of latent defects which may cause single-cell failures related to programming disturbs, data retention, and oxide defects [13], thus making Flash one of the most reliable nonvolatile memories.

A. Threshold Voltage Distribution

When dealing with a large array of cells, e.g., from tens of thousands to one million, it is very important to understand the type of dispersion given by the large set of cells. The best way to do it is to compare the threshold voltage distribution of the whole array, considering it after UV erasure—that can be considered as the reference state—after CHE programming and after FN erasing.

Fig. 14 shows typical distributions of cell threshold voltages in a large memory array. The UV-erased distribution is pretty narrow and symmetrical. A more accurate analysis would reveal a Gaussian distribution due to random variations of critical dimensions, thickness, and doping which contribute to cause a dispersion of threshold voltages, either directly or through coupling ratios.

The programmed distribution is wider than the UV-erased one, but it is still symmetrical. The enlargement occurs because most of the parameters that cause V_T dispersion of UV-erased cells also impact the threshold shift of programmed cells.

The distribution of threshold voltages after electrical erase is much wider and heavily asymmetrical. A more detailed analysis would show that the bulk of the distribution is again a Gaussian with a standard deviation larger than the one of programmed cells. Cells in this part of the distribution are referred to as “normal” cells. But there is also an exponential tail at low V_T , composed of cells that erase faster than the average, also called “tail” cells.

The dispersion of threshold voltages of normal cells is due to coupling ratio variations, and it has been accurately modeled [14]. Instead, the understanding of the tail cells, although of key importance, is more difficult. In fact, as these cells erase faster than normal cells with the same applied voltage, one should assume that they are somehow “defective.” However, they are just too numerous for being associated with extrinsic defects.

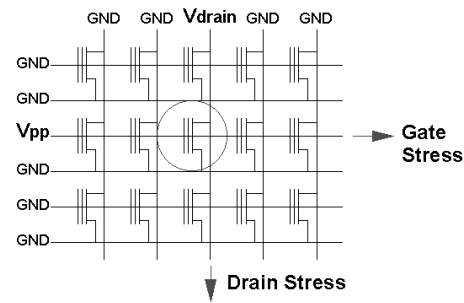


Fig. 15. Schematic of a Flash array, showing row and column disturbs occurring when the cycled cell is programmed.

Different models have been presented with the aim to explain the tail cells. For example, a distribution in the polycrystalline structure of the FG, with a barrier height variation at the grain boundaries, would give rise to a local enhancement of the tunnel barrier [15]. Another model explains the tail cells as due to randomly distributed positive charges in the tunnel oxide [16]. This model is solidly based on the well-known existence of donor-like bulk oxide traps and on calculations that show the huge increase of the tunnel current density caused by the presence of an elementary positive charge closed to injecting electrode.

Independently from a consolidated model, it can be stated that the exponential tail of the erased distribution is mostly related to structural imperfections, i.e., intrinsic defects, and it can be minimized by process optimization (for example, working on silicon surface preparation, tunnel oxidation, FG polysilicon optimization) but not eliminated. Flash products must be designed taking into account the existence of such a tail.

B. Program Disturb

The failure mechanisms referred to as “program disturbs” concern data corruption of written cells caused by the electrical stress applied to these cells while programming other cells in the memory array. Two types of program disturbs must be taken into account: row and column disturbs, also referred as gate and drain stress, as schematically reported in Fig. 15, representing a portion of a cell array.

Row disturbs are due to gate stress applied to a cell while programming other cells on the same wordline. If a high voltage is applied to the selected row, all the other cells of that row must withstand the gate stress without losing their data. Depending on the data stored in the cells, data can be lost either by a leakage in the gate oxide or by a leakage in the interpoly dielectric.

Column disturbs are due to drain stress applied to a cell while programming other cells on the same bitline. Under this condition, programmed cells can lose charge by FN tunneling from the FG to the drain (soft erasing). The program disturb depends on the number of cells along bitline and wordline and then depends strongly on the sector organization. The most effective way to prevent disturb propagation is to use block select transistor in a divided bitline and wordline

organization to completely isolate each sector. Program disturb really could be a critical issue in Flash memory, and cells and circuits must be designed with safety margins versus the stress sensitivity.

C. Data Retention

As in any nonvolatile memory technology, Flash memories are specified to retain data for over ten years. This means the loss of charge stored in the FG must be as minimal as possible. In updated Flash technology, due to the small cell size, the capacitance is very small and at an operative programmed threshold shift—about 2 V—corresponds a number of electrons in the order of 10^3 to 10^4 . A loss of 20% in this number (around 2–20 electrons lost per month) can lead to a wrong read of the cell and then to a data loss.

Possible causes of charge loss are: 1) defects in the tunnel oxide; 2) defects in the interpoly dielectric; 3) mobile ion contamination; and 4) detrapping of charge from insulating layers surrounding the FG.

The generation of defects in the tunnel oxide can be divided into an extrinsic and an intrinsic one. The former is due to defects in the device structure; the latter to the physical mechanisms that are used to program and erase the cell. The tunnel oxidation technology as well as the Flash cell architecture is a key factor for mastering a reliable Flash technology.

The best interpoly dielectric considering both intrinsic properties and process integration issues has been demonstrated to be a triple layer composed of ONO. For several generations, all Flash technologies have used ONO as their interpoly dielectric.

The problem of mobile ion contamination has been already solved on the EPROM technology, taking particular care with the process control, but in particular using high phosphorus content in intermediate dielectric as a gettering element. [17], [18]. The process control and the intermediate dielectric technology have also been implemented in the Flash process, obtaining the same good results.

Electrons can be trapped in the insulating layers surrounding the floating gate during wafer processing, as a result of the so-called plasma damage, or even during the UV exposure normally used to bring the cell in a well-defined state at the end of the process. The electrons can subsequently detrapp with time, especially at high temperature. The charge variation results in a variation of the floating gate potential and thus in cell V_T decrease, even if no leakage has actually occurred. This apparent charge loss disappears if the process ends with a thermal treatment able to remove the trapped charge.

The retention capability of Flash memories has to be checked by using accelerated tests that usually adopt screening electric fields and hostile environments at high temperature.

D. Programming/Erasing Endurance

Flash products are specified for 10^5 erase/program cycles. Cycling is known to cause a fairly uniform wear-out of the cell performance, mainly due to tunnel oxide degradation, which eventually limits the endurance characteristics [19]. A

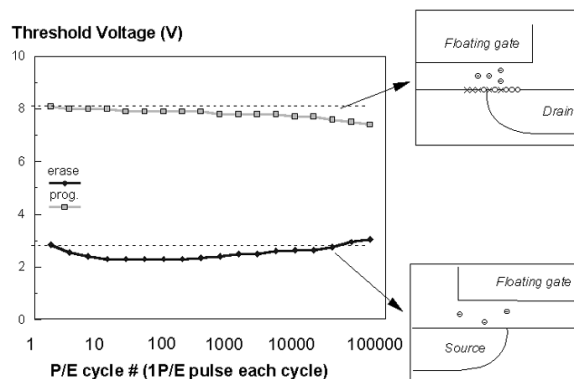


Fig. 16. Threshold voltage window closure as a function of program/erase cycles on a single cell.

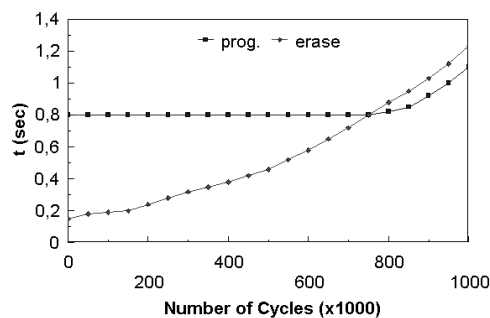


Fig. 17. Program and erase time as a function of the cycles number.

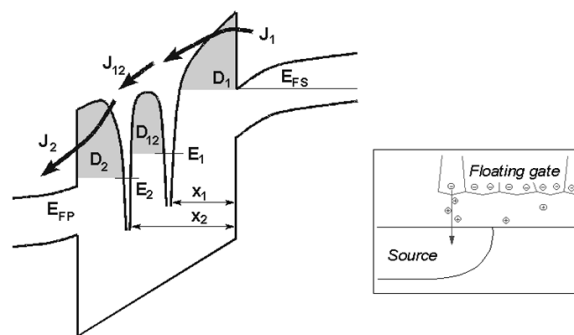


Fig. 18. Anomalous SILC modeling. The leakage is caused by a cluster of positive charge generated in the oxide during erase (left-hand side). The multitrapp assisted tunneling is used to model SILC: trap parameters are energy and position.

typical result of an endurance test on a single cell is shown in Fig. 16. As the experiment was performed applying constant pulses, the variations of program and erase threshold voltage levels are described as “program/erase threshold voltage window closure” and give a measure of the tunnel oxide aging. In real Flash devices, where intelligent algorithms are used to prevent V_T window closing, this effect corresponds to a program and erase times increase (see Fig. 17).

In particular, the reduction of the programmed threshold with cycling is due to trap generation in the oxide and to interface state generation at the drain side of the channel, which are mechanisms specific to hot-electron degradation.

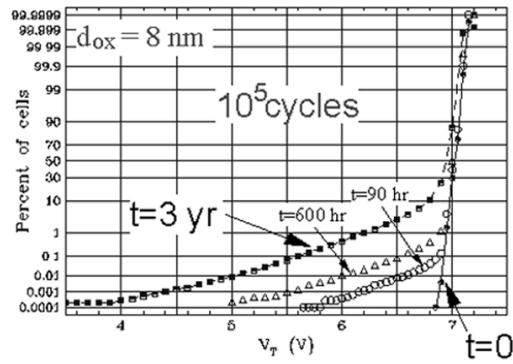
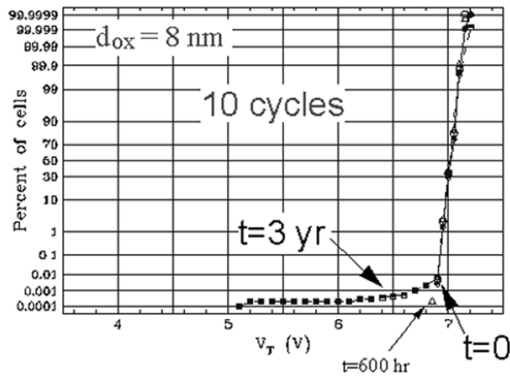


Fig. 19. Data retention tests at room temperature.

The evolution of the erase threshold voltage reflects the dynamics of net fixed charge in the tunnel oxide as a function of the injected charge. The initial lowering of the erase V_T is due to a pile-up of positive charge which enhances tunneling efficiency, while the long-term increase of the erase V_T is due to a generation of negative traps.

Cycling wear-out can be reduced by proper device engineering and by optimization of the tunnel oxide process. However, once process and product are qualified for a given endurance specification, no major problems should come from lot-to-lot variation.

Actually, endurance problems are mostly given by single-cell failures, which present themselves like a retention problem after program/erase cycles. In fact, a high field stress on thin oxide is known to increase the current density at low electric field. The excess current component, which causes a significant deviation from the current-voltage curves from the theoretical FN characteristics at low field, is known as stress-induced leakage current (SILC). SILC is clearly attributed to stress-induced oxide defects and, as far as a conduction mechanism, it is attributed to a trap assisted tunneling (see Fig. 18). The main parameters controlling SILC are the stress field, the amount of charge injected during the stress, and the oxide thickness. For fixed stress conditions, the leakage current increases strongly with decreasing oxide thickness [20]–[22].

The effect of cycling on data retention cannot be referred to in the typical cell, but must be studied considering a wide array of cells, looking in particular to the tail distribution. In Fig. 19, we report the results of retention test on a 1-Mb array of cells with 8-nm tunnel oxide in order to enhance the SILC defects in single cells. Retention tests have been performed on arrays cycled 10 and 10^5 times [23]. As can be seen, the amount of cells that lose charge after three years are much more in the case of longer endurance. Data retention after cycling is the issue that definitely limits the tunnel oxide thickness scaling. For very thin oxide, below 8–9 nm, the number of leaky cells becomes so large that even error-correction techniques cannot fix the problem.

IV. MULTILEVEL CONCEPT

An attractive way to speed up the scaling of Flash memory is offered by the multilevel (ML) concept [24]. The idea is

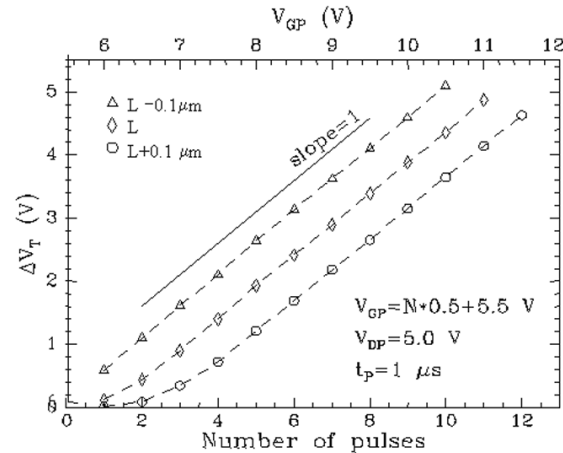


Fig. 20. $D V_T$ as a function of the pulse number for three different channel lengths (the upper axis also shows the gate voltage at each programming step).

based on the ability to precisely control the amount of charge stored into the floating gate in order to set the threshold voltage V_T of a memory cell within any of a number of different voltage ranges, corresponding to different logical levels. A cell operated with 2^n different levels is capable of storing n bits, the case $n = 1$ being the conventional single-bit cell.

Three main issues must be afforded when going from conventional to ML Flash [25]. A high programming accuracy is required to obtain narrow V_T distributions; reading operation implies multiple, either serial or parallel, comparison with suitable references to determine the cell status, requiring accurate and fast current sensing; V_T window and read voltage are larger while read margins are smaller than the single-bit case, this for allocating all levels, requiring improved reliability and/or error-correction circuitry. These key points will be discussed with reference to a common-ground NOR architecture.

A. Multilevel Flash Programming

CHE programming has been shown to give, under proper conditions, a linear relationship with unit slope between programming gate voltage V_{GP} and V_T variation [26], independently of cell parameters (see Fig. 20). Very tight V_T distri-

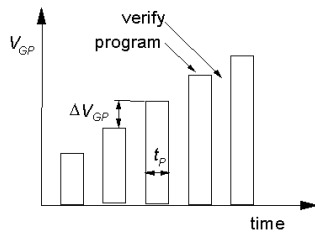


Fig. 21. Schematic of the control-gate voltage pulses.

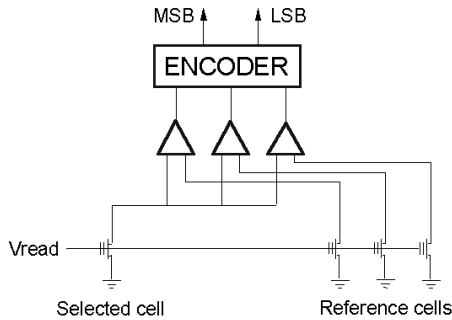


Fig. 22. Parallel multilevel sensing architecture.
MSB = most significant bit; LSB = less significant bit.

butions can be obtained by combining a program-and-verify technique with a staircase V_{GP} ramp (see Fig. 21). In fact, this method should theoretically lead to a V_T distribution width for any state not larger than ΔV_{GP} . Indeed, neglecting any error due to sense amplifier inaccuracy or voltage fluctuations, the last programming pulse applied to a cell will cause its threshold voltage to be shifted above the program verify decision level by an amount at most as large as ΔV_{GP} . It follows that by decreasing ΔV_{GP} , it is possible to increase the programming accuracy. Obviously, this is paid in terms of a larger number of programming pulses together with verify phases and, therefore, with a longer programming time. Hence, the best accuracy/time tradeoff must be chosen for each case considering the application specification.

However, high programming throughput, equal to 1-b/cell devices, is normally achieved via a large internal program parallelism, which is possible because cells need a low programming current in ML staircase programming. To do that, ML devices operate with a program write buffer, whose typical length is 32–64 bytes, i.e., 128–256 cell data length.

Also, evolution to 3–4 b/cell will not have an impact on programming throughput. In fact, program pulses and verify phases increase proportionally with the number of bits per cell, thus keeping roughly constant the effective byte programming time.

Despite a not-negligible programming current, another advantage in using CHE programming for multilevel devices is to avoid the appearance of erratic bits that instead can be a potential failure mode affecting FN programming. In fact, erratic bit behavior was observed in the FN erase of standard NOR memories [27] but, for its nature, it should be present in every tunneling process [28].

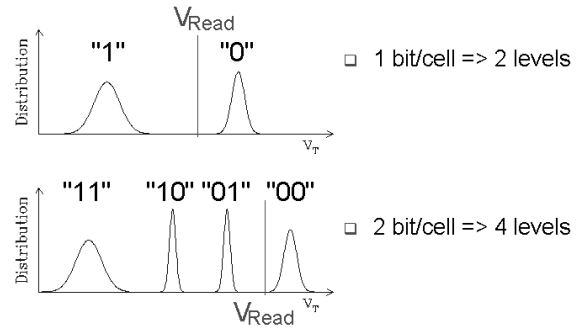


Fig. 23. Threshold voltage distribution for 2 b/cell compared with the standard 1 b/cell.

B. Reading Operation

In order to have a fast reading operation in the NOR cell, a parallel sensing approach can be used [29]. The cell current, obtained in reading conditions, is simultaneously compared with three currents provided by suitable reference cells (see Fig. 22). The comparison results are then converted to a binary code, whose content can be 11, 01, 10, or 00, due to the multilevel nature. In Fig. 23, we report the threshold voltage distribution of a 2-b/cell memory. The 11, 10, and 01 cell distribution will give rise to a different current distribution, measured at fixed V_{read} , while the 00 cell distribution does not drain current as well as the programmed level of a standard 1-b/cell device. High read data rate, via page or burst mode, is normally supported by large internal read parallelism.

A parallel sensing approach does not seem transferable to 3- or 4-b/cell generations because of the exponential increase, $2^n - 1$, in comparators number, respectively 7 or 15 per cell, that means exponential increase in sensing area and current consumption. At this moment, a serial sensing approach, e.g., dichotomic, or a mixed serial-parallel is considered the more suitable approach. Serial sensing is also useful for a 2-b/cell device when high-speed random access is not necessary, e.g., in Flash Cards applications.

C. Data Retention

One of the main concerns about multilevel is the reduced margin toward the charge loss, compared with the 1-b/cell approach. We can basically divide the problem of data retention into two different issues.

The first is related to the extrinsic charge loss, i.e., to a single bit that randomly can have different behaviors with respect to the average and that usually form a tail in a standard distribution. It is well known that extrinsic charge loss strongly depends on tunnel oxide retention electric field and that this issue can become more critical if an enhanced cell threshold range has to be used to allocate the 2^n levels [30]. This problem is usually solved with the introduction of the error correction code (ECC), whose correction power must be chosen as a function of the technology and of the specification required to the memory products.

The second one is related to the intrinsic charge loss, i.e., to the behaviors of the Gaussian part of a cell distribution,

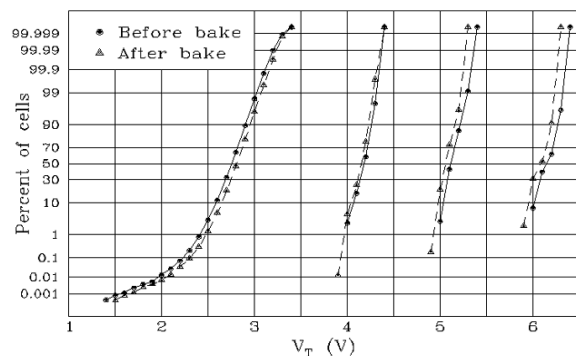


Fig. 24. Shift in the threshold voltage distribution after 500 h bake at 250 °C.

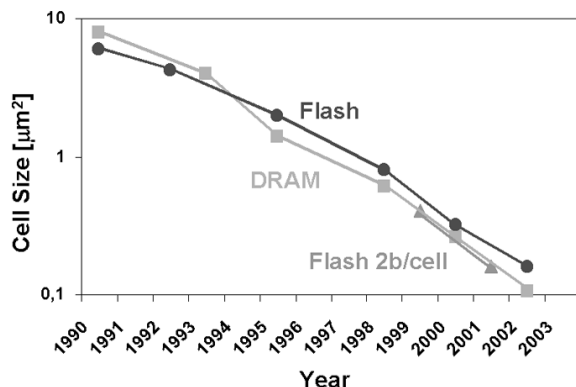


Fig. 25. DRAM and Flash cell size reduction versus year. The scaling has been of about a factor 30 in ten years.

that must be characterized and defined as a function of the different level distributions. In order to study the data retention on multilevel memories, usually tests at high-temperature bake on programmed cells are performed. A result of data retention after bake (500 h, 250 °C) is shown in Fig. 24, on one million cells [31].

The maximum V_T shift, which occurs for the uppermost level, is about 0.1 V. This means the spacing between levels is reduced by a very small amount. It is interesting to note that the three programmed levels are shifted by an amount proportional to their respective programmed ΔV_T , so that the spacing between adjacent levels is reduced by only a fraction of the observed maximum shift.

V. EVOLUTION AND SCALING TREND

The Flash memories were commercially introduced in the early 1990s and since that time they have been able to follow the Moore law or, better, the scaling rules imposed by the market. Fig. 25 reports in a logarithmic scale the Flash cell size as a function of time, from 1992 to 2002. It turns out that the reduction of the cell size has been about a factor 30 in those ten years, closely following the scaling of the DRAM, today still considered as the reference memory technology that sets the pace to the technology node evolution. More specifically, the NOR Flash cell has scaled from 4.2 μm^2 for the 0.6- μm technology node to the present cell size of 0.16 μm^2 at the 0.13- μm node.

Moreover, considering the multilevel approach for the Flash cell with the capability to store two bits in the same cell, as presented in Section IV, not only the scaling trend but even the bit size itself is well aligned with the DRAM one.

Together with the Flash cell scaling, there has also been an evolution of the Flash product specification and application. Three main generations can be considered, well differentiated as a technology node, process complexity, and specification.

- *First generation (1990–1997).* The Flash applications were mainly “EPROM replacement.” The products were characterized by a single array (bulk), with memory density from 256 kb to 2 Mb. The program and erase algorithms were controlled externally and all the product were dual voltage: 12 V for the write operations and 5 V for the power supply. Cycling specification was limited to 10^4 .
- *Second generation (1995–2000).* The Flash memory has become the right nonvolatile memory technology for code storage application, where software updates must be performed on the field. In particular, portable systems, mainly cellular phones, were strongly interested in this feature. The cellular phone applications brought a lot of innovations:
 - The density was increased from 1 to 16 Mb and sectors were introduced, instead of a single (bulk) array, in order to allow different use of the memory (some sectors can be used to store code while others to store data, with different requirements in terms of cycling). Sector density was from 10 to 256 kb.
 - A single voltage supply pin (5 or 3 V according to the system specification) substituted the two high-voltage and low-voltage pins previously used. The need to be programmed on field, without the possibility to have the high voltage from an external pin, has developed the technology to internally generate the writing voltages using charge-pump techniques. A high-voltage supply is sometimes still used, but limited to the first programming operation in the system manufacturing line, to improve the throughput.
 - Algorithms to perform all the operation on the array—reading programming and erasing—were embedded into the device in order to avoid the need for an external micro-controller.
 - 10^5 writing cycles were introduced as a specification. More than effectively needed by the system, this high endurance is the result of a highly reliable technology.
- *Third generation (from 1998 on).* The portable system specifications push toward Flash memory products that look more and more like an application-specific memory. Obviously, the density is one of the most important parameters, and devices well

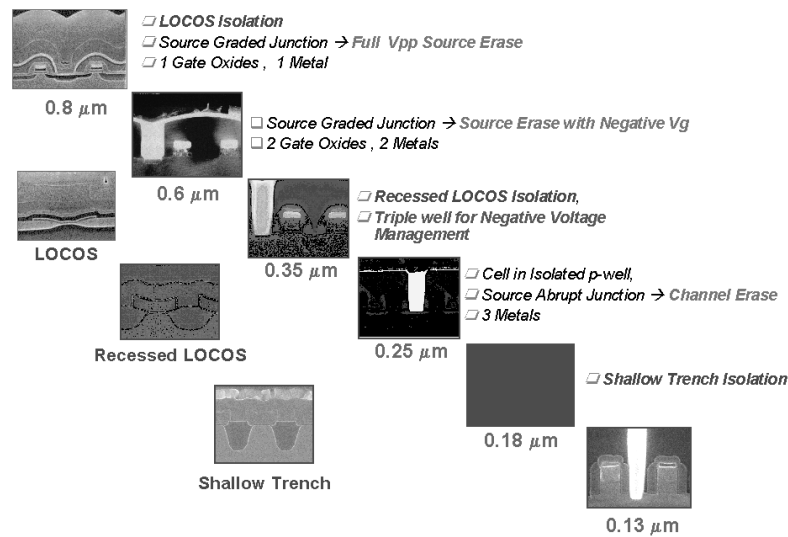


Fig. 26. NOR Flash technology and architecture evolution.

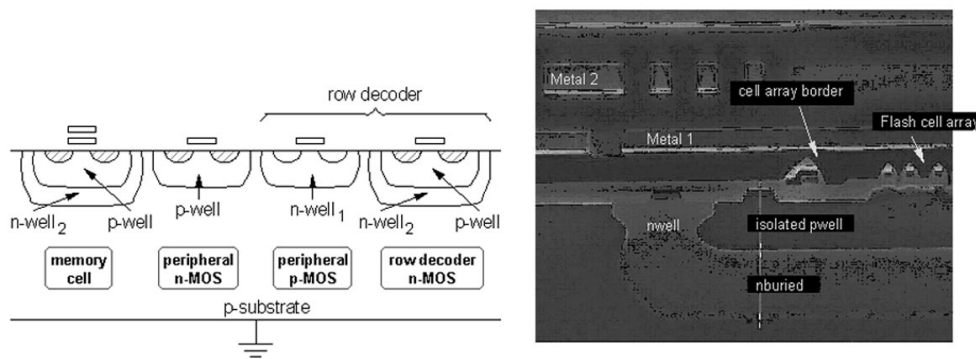


Fig. 27. Triple well structure cross section: schematic (left side) and SEM (right side).

beyond 64 Mb will be realized entering the Flash in the gigabit era. The sectorization is becoming more complex, and dual or multiple bank devices have already been presented. In these devices, different groups of sectors (banks) can be differently managed: at the same time one sector belonging to a bank can be read while another one, inside a different bank, can be programmed or erased. Also, following the general trend of reducing the power supply, the device supply is scaling to 1.8 V (with the consequent difficulties of internally generating high voltages starting from this low supply voltage value) and will go down to 1.2 V. Another issue, becoming more and more important, is the high data throughput, in particular considering the density increase. Burst mode is often used in order to speed up the reading operation and quickly download the software content, reaching up to 50 MB/s.

The introduction of the different generation as well as the reduction of the cell size has been made possible by the developments of Flash technology and process, and of cell architecture.

For what concerns the process architecture, all the main technology steps that have allowed the evolution of the

CMOS technology have also been used for Flash. In Fig. 26, the different cell cross sections as a function of the different technology node are reported. For every generation, the main innovative introduced steps are pointed out. It turns out that the evolution of the different generations has been sustained by an increased process complexity, from the one gate oxide and one metal process with standard local oxidation of silicon isolation at the 0.8- μm technology node, to the two gate oxides, three metals, and shallow trench isolation at the 0.13- μm node. In between is the introduction of tungsten plug, of self-aligned silicided junctions and gates, and the wide use of chemical mechanical polishing steps. But one of the most crucial technologies for Flash evolution was the high-energy implantation development that has allowed the introduction of the triple well architecture (see Fig. 27). With this process module, further development of the single-voltage products has been possible, allowing the easy management of the negative voltage required to erase the cell and, furthermore, the possibility to completely change the erasing scheme of the cell.

In fact, as reported in Fig. 28, the cell programming and erasing applied voltages have been changed as a function of the different generation, always staying inside the CHE programming and the FN erasing. The first generation of cells

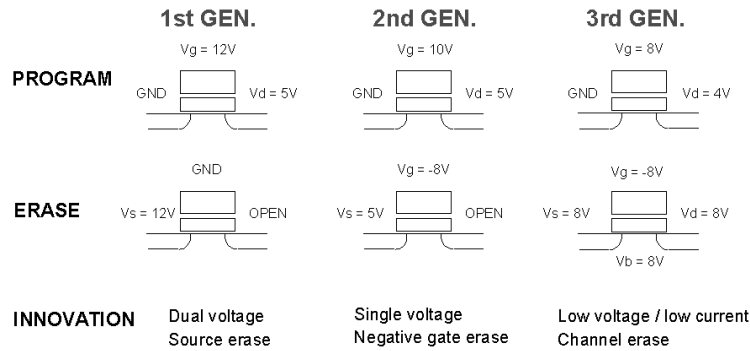


Fig. 28. NOR Flash cell evolution.

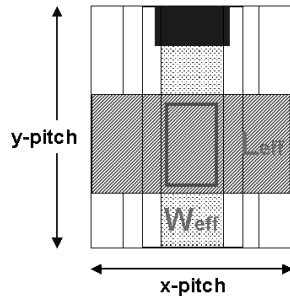


Fig. 29. NOR cell scaling. The basic layout has remained unchanged through different generations.

was erased, applying the high voltage to the source junction and then extracting electrons from the FG-source overlap region (source erase scheme). This way was too expensive in terms of parasitic current, as the working conditions were very close to the junction breakdown. Moving to the second generation with the single-voltage devices, the voltage drop between the source and the FG was divided, applying a negative voltage to the control gate and lowering the source bias to the external supply voltage (negative gate source erase scheme).

Finally, with the exploitation of the triple well also for the array, the erasing potential is now divided between the negative CG and the positive bulk (the isolated p-well) of the array, moving the tunneling region from the source to the whole cell channel (channel erase scheme). In this way, electrons are extracted from the FG all along the channel without any further parasitic current contribution from the source junction, consequently reducing the erase current amount of about three orders of magnitude; the latter being a clear benefit for battery saving in portable low-voltage applications.

The NOR Flash cell is forecasted to scale again following the International Technology Roadmap of Semiconductors (ITRS) [32]. The introduction of the 130-nm technology node has occurred in 2002–2003 with a cell size of $0.16 \mu\text{m}^2$ [33], following the $10\text{-}\lambda^2$ golden rule for the cell area scaling, where λ is the technology node. The representation of the memory cell size in terms of number of λ^2 is a usual way to compare different technology with the same metric; for example, the DRAM cell size is today quoted to stay in the range of $6\text{--}8 \lambda^2$.

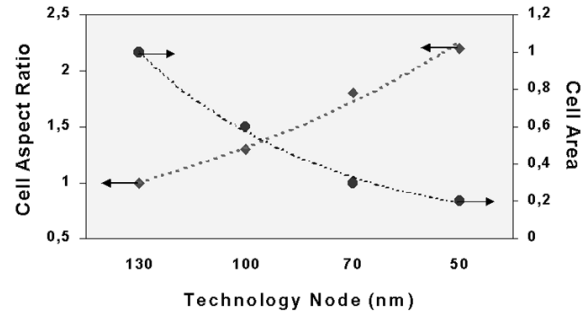


Fig. 30. NOR Flash cell scaling trends for cell area (right y axis) and cell aspect ratio (left y axis). Both values are normalized to the 130-nm technology node.

The next technology step for the NOR Flash will be the 90-nm technology node in 2004–2005. The cell size is expected to stay in the range of $10\text{--}12 \lambda^2$, translating to a cell area of $0.1\text{--}0.08 \mu\text{m}^2$. As reported again in Fig. 29, the cell basic layout and structure has remained unchanged through the different generations. The area scales through the scaling of both the x and y pitch. Basically, this must be done contemporarily reducing the active device dimensions, effective length (L_{eff}) and width (W_{eff}), and the passive elements, such as contact dimension, contact to gate distance, and so on.

For future generation technology nodes, i.e., the 65 nm in 2007 and the 45 nm in 2010, as forecasted by ITRS, the Flash cell reduction will face challenging issues. In fact, while the passive elements will follow the standard CMOS evolution, benefiting from all the technology steps and process modules proposed for the CMOS logic (like advanced lithography for contact size, copper for metallization in very tight pitch), the active elements will be limited in the scaling. In particular, the effective channel length will be limited by the possibility to further scale the active dielectric, i.e., the tunnel oxide and the interpoly ONO. As already presented in Section III, the tunnel oxide thickness scaling is limited by intrinsic issues related to the Flash cell reliability, in particular the charge retention one, especially after many writing cycles. Although the direct tunneling, preventing the ten-year retention time, occurs at $6\text{--}7$ nm, SILC considerations push the tunnel thickness limit to no less than $8\text{--}9$ nm. Moreover, the effective

width reduction could be limited by the read current reduction, strongly proportional to the W_{eff} , then impacting the access time.

Scaling the technology node, while the cell x pitch will more and more approach the 2λ , the y -pitch scaling will be limited by the cell gate scaling. Hence, for the 65- and 45-nm technology nodes, it is expected to have smaller cell size but with an increased number of λ^2 , from 10 to 14. In particular, the cell aspect ratio, i.e., the y pitch over the x pitch, will continue to rise, due to the slowdown of the L_{eff} reduction. Fig. 30 reports the cell area and the cell-aspect ratio versus the technology node, both normalized at 130 nm. As can be observed, the cell area will be roughly one half at 90 nm (same number of $10\text{--}12\lambda^2$) and will decrease, but with slower trend at 65 and 45 nm. The cell-aspect ratio will continue to increase, almost doubling the one at 130 nm when the technology node will reach 45 nm.

VI. SUMMARY

With more than ten years of consolidated know-how and thanks to its flexibility and cost characteristics, Flash memory is today a largely utilized, well-consolidated, and mature technology for nonvolatile memory application.

Flash sales represent a considerable amount of the overall semiconductor market. In particular, the NOR Flash is today the most diffused architecture, being able to serve both the code and the data storage market.

The cell is basically a floating-gate MOS transistor, programmed by CHE and erased by Fowler–Nordheim tunneling. The main reliability issues, like charge retention and endurance, have been extensively studied and the physical mechanism well understood in such a way to guarantee the present specification requirements.

The Flash cell scaling has been demonstrated to be really possible and to be able to follow the Moore's law down to the 130-nm technology generations. The technology development and the consolidated know-how will sustain the scaling trend down to the 90- and 65-nm technology nodes as forecasted by the ITRS.

One of the crucial issues to be solved to allow cell scaling below the 65-nm node is the tunnel oxide thickness reduction, as tunnel thinning is limited by intrinsic (direct tunneling) and extrinsic (SILC) mechanisms.

At each technology node, the multilevel approach will increase the memory efficiency, almost doubling the density at the same chip size, enlarging the application range, and reducing the cost per bit.

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on the development of Flash memory, studying the device physics related to the programming/erasing mechanisms and participating to the process architecture definition. Then he was Project Leader of the Flash memory device process development for single power supply application from 1994 to 1997, and for multilevel products since 1998. Currently, he is Section Manager in the Non-Volatile Memory Process Development Group of the Central Research and Development Department of STMicroelectronics. He has authored many papers, conference contributions, and patents on topics related to nonvolatile memories. He was lecturer in Electron Device Physics at the University of Milan and in Non-Volatile Memory Devices at the University of Padova and Polytechnic of Milan. He is a member of the Symposium on VLSI Technology Technical Program Committee.



Emilio Camerlenghi was born in Bergamo, Italy, in 1959. He received the Ph.D. degree in physics (curriculum in solid state physics) from the University of Milan, Milan, Italy, in 1984.

In 1985, he joined the Central Research and Development Department, VLSI Process Development Group of STMicroelectronics, Agrate Brianza, Italy, working on nonvolatile memories process architectures. Until 1989, he was engaged in development of the 1.2- μm EPROM technology, with the main objective of studying

the memory cell hot-electron programming physics and developing the memory cell device. From 1990 to 1992, he became responsible of the development of the new generation 0.6- μm EPROM process architecture. In 1992, he joined the Flash development team, where he was Project Leader of the 0.6- μm Flash technology, designed to realize both double (5–12 V) and single (5 V only) power supply devices. In 1995, he was in charge of leading the ST part of an advanced project (a codevelopment between STM and a U.S. company) whose target was to demonstrate the functionality of an innovative Flash memory virtual-ground architectural concept. In the 1997–1998 years, he was appointed to lead the development of the 0.25- μm Flash process architecture for low-voltage power supply applications. Since 1998, he has been Section Manager of High Performance Flash Memory in the Non-Volatile Memory Process Development Group of the Central Research and Development Department, STMicroelectronics; under his responsibility, the 0.18- μm , 0.15- μm generations were developed and qualified, while the 0.13- μm technology is at present in the qualification phase. He has authored many conference papers and patents on nonvolatile memory related topics. He is currently a member of the IEDM conference subcommittee on “Integrated Circuits and Manufacturing.”



Alberto Modelli was born in Milan, Italy, in 1953. He received the Ph.D. degree in physics from the University of Milan in 1978.

In 1978, he joined the Device Physics Laboratory of the Research and Development Department, STMicroelectronics, Agrate Brianza, Italy, where he initially worked on the development of silicon solar cells and later on the physics and electrical characterization of the Si/SiO₂ system. In 1994, he joined the Non-Volatile Memory Process Development

Group of STMicroelectronics, where he has been working on the reliability of flash memories. Since 1996, he has been in charge of multilevel flash development. He is author or coauthor of over 40 publications, one book, and five patents on the above-mentioned topics.



Angelo Visconti was born in Como, Italy, in 1966. He received the Ph.D. degree in physics, *cum laude*, from the University of Milan, Como, in 1997. His thesis was on the feasibility of optical temporal solitons in quadratic nonlinear materials.

Beginning in 1987, he worked for ten years as a hardware and software designer and project leader for industrial automation systems. In 1997, he joined the Central Research and Development Department of STMicroelectronics,

Agrate Brianza, Italy, in the Non-Volatile Memory Process Development Group. His first activities were about the study and characterization of channel erase and programming currents in Flash cells. Afterward, he was involved in the development of a 0.18- μm CMOS high-density Flash memory process. His interests are the characterization, reliability, and multilevel applications of Flash cells. He is author or coauthor of several publications and patents in the nonvolatile memory field and nonlinear optical field. He is currently a Lecturer of Non-Volatile Memory Devices at the University of Padova, Padova, Italy.

Attachment MM

Introduction to Flash Memory

ROBERTO BEZ, EMILIO CA...

D VISCONTI

Invited Paper

The most relevant phenomenon of the evolution of semiconductor memories has been the growth of the Flash memory market, driven by the demand of electronic portable equipment (palm top computers, digital camera, and so on). More portable systems will demand even more memory, together with high density and very high performance storage application or with fast random access in place. The strong consolidated know-how (experience), the flexibility, and the cost effectiveness of the nonvolatile memory applications have sent a considerable amount of the over...

Although in the past different types of architectures have been proposed, today two of them are the industry standard: the common ground truth is addressing both the code and data storage segments, and the NAND Flash, optimized for the data storage market.

This paper will mainly focus on the development of the NOR Flash memory technology, with the aim of describing both the basic functionality of the memory cell used so far and the main cell architecture consolidated today. The NOR cell is basically a floating-gate MOS transistor, programmed by channel hot electron and erased by Fowler–Nordheim tunneling. The main reliability issues, such as charge retention and endurance, will be discussed, together with the understanding of the basic physical mechanisms responsible. Most of these considerations are also valid for the NAND cell, since it is based on the same concept of floating-gate MOS transistor.

node is the tunnel oxide thickness, which is limited by intrinsic and extrinsic factors.

memory, Flash technology, volatile memory, NOR cell, and so on.

In the long term, has been the evolution of the market, with some valleys and peaks, expected to continue in the future. The amount of this market, the evolution of semiconductor memories, which are divided into the following two branches, both based on the complementary metal–oxide–semiconductor (CMOS) technology (see Fig. 2).

- The volatile memories, like SRAM or DRAM, that although very fast in writing and reading (SRAM) or very dense (DRAM), lose the data contents when the power supply is turned off.
- The nonvolatile memories, like EPROM, EEPROM, and Flash, are able to balance the trade-off between speed and density.

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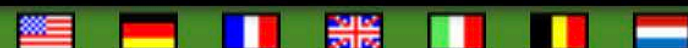
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ZCONTROL

What Is It?

ZCONTROL is an invisible software security application, based on ZAGENT core technology, that retrieves files, deletes sensitive information and maintains data privacy AFTER computer loss.

Why Do You Need It?

Laptops with large storage capacity are becoming desktops replacements and that data is valuable. If the computer with this data is lost or stolen, there could be significant negative ramifications. Consider these questions.

How long would you be non-productive? What strategic information could be compromised? Real examples of this type of information include pending mergers, new product intellectual property, business strategies and launch plans, and previously undisclosed financial operating results.

What tactical information could be compromised? Examples include private employment compensation details, proposals to clients, plans for organizational changes, and the myriad of similar information that can be gained from reading a person's email, calendar, contacts, or collection of documents and spreadsheets.

What information about the company's network or computing infrastructure would be revealed that could facilitate an electronic attack? Examples of this type of information include usernames and passwords, dial in numbers, IP addressing schemes, DNS naming conventions, ISPs used, mail servers, and other networking details related to connecting the laptop to the corporate or Internet environment.

What personal information about the laptop owner can be obtained? Examples include personal financial information, confidential family matters, loss of prized digital photographs, credit card numbers and PINS.



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**CyberSpeak**

Edward C. Baig

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04/09/2002 - Updated 09:30 PM ET

Unlock the secrets of security for your laptop

Not long before the outbreak of the Persian Gulf War, a London crook lifted a laptop computer out of a parked car belonging to a British military officer. The computer eventually was recovered, but classified material supposedly was on the machine's hard drive, and the hapless officer was court-martialed and demoted.

Sadly, there is war again overseas, but then, as now, you need not harbor military secrets to fret about a potential laptop heist. Whether it's your personal finance data on Quicken or proprietary marketing plans that must be kept from an unscrupulous competitor, civilians routinely carry revealing bits best kept out of foreign hands. Of course, even when the stored information isn't so hush-hush, a bad guy (or gal) will gladly fence a notebook for a quick dollar.

According to the 2002 Computer Security Institute/FBI Computer Crime and Security Survey, the theft of laptops led to an average financial loss of \$89,000 among the corporations and government agencies who responded. (Only a small percentage of the sum actually relates to the hardware cost.)

Safeware, an insurance firm that will let you take out a policy on a laptop, reports that 591,000 notebooks were snared in 2001, a 53% rise over the previous year.

Lately, given the more stringent security measures implemented at airports since Sept. 11, the problem appears to be getting worse. Travelers are forced to remove laptops from their bags, and some passengers are inadvertently leaving the computers behind at checkpoints or absent-mindedly grabbing the wrong one. (Many models do look alike.) And crooks might be licking their chops over the high-tech booty coming through the X-ray scanner, provided the presence of armed soldiers doesn't discourage them.

You might lessen the likelihood of someone mistakenly walking off with your machine in the terminal by affixing permanent labels with your name and office number or by using colorful tape to make your notebook stand out.

Indeed, you can safeguard your portable with common sense.

Consider that, as dopey as it seems, some folks actually stick Post-it notes with corporate network passwords on the outside of the machine. That's like handing a bank robber the combination to the vault. I don't mean to be unsympathetic here, but **YOU PEOPLE DESERVE TO GET RIPPED OFF.**

Your car may stop you from falling asleep at the wheel

It's the middle of the night and you're alone, driving along a monotonous stretch of highway. The eyes are growing heavy. You are an accident waiting to happen.

Suddenly, a voice barks out: "Tell me the name of the first person you ever dated" or "Where is it that you work?" If you're slow to respond or give an incorrect answer, the car turns into a virtual alarm clock on wheels.

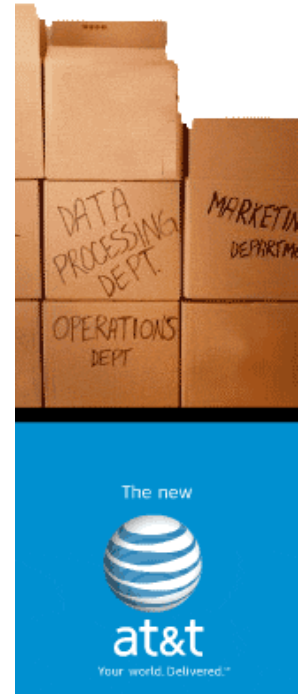
A window opens, the horn honks or the radio changes stations and raises the volume. You may be read aloud a pop trivia quiz or told a joke. Or even sprayed with water.

If all that doesn't rouse you, the system may book a motel room or direct you to the nearest rest stop.

Seem far-fetched? IBM researchers were recently granted a patent for an Artificial Passenger "telematics" system, a method of keeping fatigued drivers out of danger. Big Blue telematics guru Raj Desai says cars could be outfitted with a variation of the system within three years. (Telematics is a term that describes a gaggle of wireless safety, security, communications and entertainment services in a car, including remote diagnostics and e-mail.)

The ultimate cost of the system will be left to the manufacturer or provider. IBM's breakthrough is in detecting when the person at the wheel is about to enter la-la land.

Drowsy drivers are identified via a combination of speech and dialogue software. Slurred speech and changes in pitch are giveaways. Dashboard cameras may also pick up lip or eye movements.



Another tip: Kindly say no when the friendly fellow smiling at Junior volunteers to watch your laptop bag while you take the kid to the bathroom. Chances are he isn't an industrial spy, but why risk it?

The technology is speaker-independent. But you'll also be able to personalize the system so Artificial Passenger will know the name of that first love and what it will take to wake you up, a spritz of H2O, perhaps.

In your hotel room or office, you may be able to thwart the casual thief with a simple lock or alarm, and there are many on the market. Among the accessories being sold at the Targus Web site, for example, is a new \$120 **DEFCON Authenticator**, a USB-based biometrics device that uses your fingerprint in lieu of a password to grant access to the operating system. No need for paranoia, but many computer crimes are inside jobs.

A splash sure beats a crash.

— Edward C. Baig

I travel with an old standby called the Kensington **MicroSaver Security Cable**, which fits into a small slot on most notebooks. As with a bicycle cable, you wrap the \$45 steel cable around a desk or other immovable object to prevent an intruder from wandering off with the machine. Of course, if someone really wants the thing, they can snip the cord.

When the stored information is worth more to you than the physical hardware, you can load third-party programs to encrypt or scramble files so others can't read them. IBM recently started planting a security chip on the motherboards inside many new ThinkPad models. The chip, which adds about \$25 to the laptop cost, lets you encrypt files on the hard drive.

I recently put a new multipurpose laptop security package to the test, the \$99 **Anti-Theft PC Card** from Caveo Technology in Cambridge, Mass. The software and PC card combo product, for Windows machines only, aims to protect the computer and the information stored inside. It does so by sounding an alarm when someone grabs the machine and leaves your workspace. It also will prevent an unauthorized person from booting up. And you can encrypt confidential files.

The Caveo installation went fairly smoothly on a Windows 98 laptop, although I wasn't initially able to shut down the computer when asked to reboot. (I had to turn it off manually.) During setup, you choose a "theft perimeter," ranging from a distance of about five to 10 feet up to about 30 feet or more. An alarm goes off if someone takes the machine outside this predetermined zone.

You also can set up the system so that an alarm is activated whenever the screen saver comes on. Alternatively, you can create something called a "motion password," triggered when you physically position the machine in three distinct patterns. It's awkward. For example, you might activate the alarm by, in precise order, tilting the machine left, then right, then left again; the idea is that you can protect the machine with an alarm even when the computer is powered down.

If the alarm does go off, you must enter a 16-digit emergency PIN, different from the shorter PIN you use to boot up. All of this functioned properly, but after my testing was done, I had a hard time removing Caveo from my laptop, even with the help of a company techie. I suppose that speaks well for keeping the machine out of harm's way if a thief gets hold of it, but Caveo will need to address the issue for owners who want to legitimately uninstall the software.

So what happens if, despite your best intentions, your computer is pilfered anyway? Three services, **CompuTrace** from Absolute Software in Vancouver, British Columbia, **CyberAngel** from Computer Sentry Software in Nashville, and **zTrace** from zTraceTechnologies in Waltham, Mass., might just help you recapture the goods. Think of them as LoJacks for your laptop.

When an unsuspecting crook connects the laptop modem via a dialup or broadband hookup, software agents on the computer surreptitiously connect to a central monitoring center or the company's respective servers, blowing the cover on the IP address or phone number (via caller ID) used to call in. The modem speaker is kept silent. Working with law enforcement, these security companies can, we hope, locate your computer. The annual cost of monitoring for an individual ranges from \$50 to \$60. Coming soon: schemes for remotely retrieving, encrypting or wiping out files that get into the wrong hands.

I can offer one final tidbit to help you protect crucial content, if not the actual machine: Back up data as if your livelihood depends on it. As a British officer discovered a decade ago, apparently it does.

Send e-mail to Ed at ebaig@usatoday.com.



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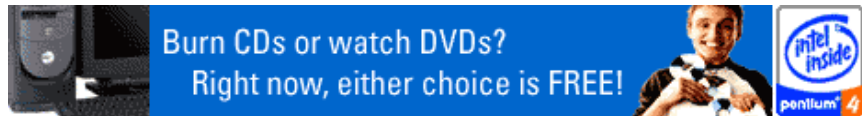
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Y URL Guide

NEWSLETTER

July 2002



The URL Index is the fastest way to get from our magazine to one of the sites we mention in it. We're handy when you have the paper edition of Y-Life next to the computer -- and even when you don't!

We've indexed all the Web sites we mention in this issue (Volume 8, Number 7) in section-by-section, page-by-page order. Happy exploring!

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