Nader Bagherzadeh, Ph.D.

Expertise

- Digital Signal Processing Architectures
- Processor Architectures (VLIW, Superscalar)
- VLSI Design
- Computer Networks & Digital Telecommunication
- Computer Graphics
- Memory System Architecture
- DRAM, SRAM, EEPROM, and Flash memory
- Automotive Computing
- Error Detection and Correction
- Machine Learning Accelerators

Contact Information:

Cell: (949) 400 5167
Office: (949) 824 8720
Email: nader@uci.edu
Office Address:
EH 4209
Electrical Engineering and Computer Science Department
University of California, Irvine
Irvine, CA 92697

Education

Year	College/University	Degree
1987	The University of Texas at Austin	Ph.D., Computer Engineering
1979	The University of Texas at Austin	MS, Electrical Engineering
1977	The University of Texas at Austin	BS (with honors), Electrical Engineering

Employment History

From: 1987 **University of California at Irvine**
To: Present Irvine, CA
Position: *2003- Present: Professor, Department of Electrical Engineering and Computer Science*
1998-2002: Professor and Chair, ECE/EECS Department
1993-1997: Associate Professor, ECE Department
1987-1992: Assistant Professor, ECE Department

From:	1980	**AT&T Bell Labs**
To:	1984	Holmdel, NJ
	Position:	*Member of Technical Staff, No.5 ESS Hardware/Software T1Line Interface Design*

Awards and Honors

1973-77	Dean's honor roll for six semesters; UT Austin
1984	Outstanding achievement award; AT&T Bell Labs
2002	Best Paper award in IEEE Transactions on VLSI Design
2002	Best Student Paper award in the proceedings of ASPDAC'02
2014	Khwarizmi International Award
2014	IEEE Fellow
2015	Professor of the Year for the EECS Department, UCI
2020	Best Paper award in the proceedings of IEEE EDGE Computing

Consulting History

From:	2006	**STEC**
To:	2008	Irvine, CA
	Duties:	Flash memory CODEC design and evaluation

From:	2006	**Tialinx**
To:	2008	Newport Beach, CA
	Duties:	Radar DSP board design and evaluation

From:	2000	**Morpho Technologies**
To:	2005	Irvine, CA
	Duties:	Co-Founder; DSP design for communication and multimedia systems

Litigation Support Experience

Date:	2024	**Kirkland & Ellis LLP**
	Case	*TCL Electronics Holdings Ltd. vs. Intellectual Ventures I LLC*
	Project:	Expert Witness for TCL
	Status:	IPR pending
	Contact:	Russell Levine 300 North LaSalle Chicago, IL 60654 Direct Dial: (312) 862 2466 Rusell.levine@kirkland.com

Date:	2024	**Covington & Burling LLP**
	Case	*Redstone Logics LLC v. Samsung Electronics Co., Ltd.*
	Project:	Expert Witness for Samsung Electronics Co., Ltd.
	Status:	IPR pending
	Contact:	Ali Mojibi 1999 Avenue of the Stars Los Angeles, CA 90067-4643 (424) 332 4803 amojibi@cov.com

Date:	2023	**Finnegan, LLP**
	Case	TBD
	Project:	Expert Witness for Nissan Motor Co.
	Status:	In progress
	Contact:	Luke McCammon 901 New York Avenue, N.W. Washington, D.C., 20001 Direct Dial: (202) 408-4273 Luke.McCammon@finnegan.com

Date:	2023	**REICHMAN JORGENSEN LEHMAN & FELDBERG LLP**
	Case	TBD
	Project:	Expert Witness for Valtrus Innovation Ltd
	Status:	In progress
	Contact:	Patrick Colsher 100 Marine Parkway, Suite 300 Redwood Shores, CA 94065 Direct Dial: (650) 623-1427 pcolsher@reichmanjorgensen.com

Date:	2023	**McKool Smith**
	Case	*TexasLDPC Inc. v Broadcom Inc., LSI Corporation, Avago Technologies U.S., Inc.; C.A. No. 18-1966-SB*
	Project:	Expert Witness for Broadcom
	Status:	Dismissed without prejudice
	Contact:	Steven Rizzi One Manhattan West

395 9th Avenue, 50th Floor
New York, NY 10001
(212) 402-9809
srizzi@McKoolSmith.com

Date: 2023 **Caldwell Cassidy & Curry**
Case BeSang Inc. v. Intel and/or Micron, CIVIL ACTION NO. 2:23-CV-00028-JRG-RSP and Case No. 3:23-cv-00113-HZ
Project: Expert Witness for BeSang
Status: Stay
Contact: Bjorn A. Blomquist
2121 North Pearl Street, Suite 1200
Dallas, Texas 75201
Office Line: (214) 888-4960
Mobile: (608) 790-0902
bblomquist@caldwellcc.com

Date: 2023 **Mintz**
Case Daedalus v. Qualcomm Inc. and Samsung Electronics Co.
Project: Expert Witness for Daedalus Prime LLC
Status: ITC, provided technical support without rendering an opinion in a report. Case is closed.
Contact: Peter F. Snell
pfsnell@mintz.com
212 692 6850
Chrysler Center
666 Third Avenue
New York, NY 10017
212 935 3000
mintz.com

Date: 2022 **Arnold & Porter**
Case Rex Computing, Inc. v. Cerebras Systems Inc.
Project: Expert Witness for Rex Computing, IPR Petition by Cerebras
Status: Board sided with Rex and did not grant the petition
Contact: Nicolas Lee,
44th Floor, 777 South Figueroa Street

Los Angeles, CA 90017
Direct Tel.: (213) 243-4156
Company: (213) 243-4000
nicholas.lee@arnoldporter.com

Date: 2022 **Quinn Emanuel Urquhart & Sullivan, LLP,**
Case MediaTek Inc. v. NXP Semiconductors N.V.
Project: Expert Witness for Media Tek
Status: Settled
Contact: Jordan B. Kaericher
865 S Figueroa St 10th Floor
Los Angeles, CA 90017
Direct Tel.: (213) 443-3843
Company: (213) 443-3000
jordankaericher@quinnemanuel.com

Date: 2022 **Bartlit Beck LLP**
Case Viasat vs. Kioxia and Western Digital, Patent Litigation Consulting
Project: Expert Witness for Viasat. Provided declaration
Status: IPR; Board decided in favor of Viasat
Contact: Scott McBride
54 West Hubbard Street
Chicago, IL 60654
Direct Tel.: (312) 494-4436
scott.mcbride@bartlitbeck.com

Date: 2022 **Arch & Lake LLP**
Case Autel v. Hunter Engineering Company
Project: Expert Witness for Autel. Provided patent analysis
Status: Inactive
Contact: Hao Tan,
203 N La Salle St #2100,
Chicago, IL 60601
Direct Tel.: (312) 558-1368
haotan@archlakelaw.com

Date: 2022 **Adhoot & Wolfson PC and Miller Shah LLP**
Case Winnie Clark et al v. American Honda Motor Co., Inc.,
Project: Brief discussion for the Class; no additional duties
Status: Class Action Consideration
Contact: Christopher Stiner
Adhoot/Wolfson: (888) 333-8996

cstiner@ahdootwolfson.com

Date: 2021 **Kilpatrick Townsend, LLP**
Case Autel Intelligent Tech. Corp., LTD vs. Orange Electronic Co., LTD
Project: Expert Witness for Autel. Provided IPR declaration
Status: Pending IPR Decision
Contact: David A. Reed,
Suite 2800, 1100 Peachtree Street NE
Atlanta, GA 30309-4528
Direct Tel.: (404) 745-2548
Company: (404) 815-6500
dreed@kilpatricktownsend.com

Date: 2021 **Desmarais LLP**
Case AMD, QCM, and STM vs. Monterey Research
Project: Expert Witness for Monterey. Provided IPR declarations and was deposed.
Status: Settled
Contact: Jordan Malz,
230 Park Avenue
New York, NY 10169
Direct Tel.: (212) 351-5497
Company: (212) 351-3400
JMalz@desmaraisllp.com
www.desmaraisllp.com

Date: 2020 **Devlin Law Firm LLC**
Case Engagement for Assistance with Certain Patents Asserted by Flash-Control, LLC
Project: Expert Witness for Flash Control. Provided IPR declaration and was deposed.
Status: Pending IPR Decision
Contact: Jim Lennon,
1526 Gilpin Avenue
Wilmington, Delaware 19806
Tel.: (302) 449-9010
Cell: (302) 593-4486
www.devlinlafirm.com

Date: 2019 **The Honorable David O. Carter**

Case	Limestone Memory Systems vs. Micron Technology, et al.
Project:	Special Master for Judge Carter
Status:	Settled
Contact:	Judge David O. Carter, Ronald Reagan Federal Building, United States Courthouse 411 West Fourth Street, Courtroom 9D Santa Ana, CA 92701-4516

Date:	2018	**Arnold & Porter Kaye Scholer LLP**
	Case	Samsung Electronics Co. Ltd. vs. Home Semiconductor Corp.
	Project:	Expert Witness for Samsung
	Status:	Case dismissed
	Contact:	Ali Sharifahmadian, 601 Massachusetts Ave., NW Washington, DC 20001-3743 (202) 942 6370 Ali.Sharifahmadian@arnoldporter.com

Date:	2018	**Fried, Frank, Harris, Shriver & Jacobson LLP**
	Case	Intel Corp. vs. Godo Kaisha IP Bridge 1
	Project:	Expert Witness for IP Bridge
	Status:	Closed IPR
	Contact:	Robert Masters, 801 17th Street, NW Washington, DC 20006 (202) 639 7370 robert.masters@friedfrank.com

Publications

Journals Refereed

j1 P. Suhler, N. Bagherzadeh, M. Malek, and N. Iscoe, "Software authorization systems," *IEEE Software*, pp. 34-41, September 1986.

j2 A. Guzman, E. Krall, P. McGehearty, and N. Bagherzadeh, "Performance of symbolic applications on a parallel architecture," *International Journal of Parallel Programming*, vol. 16, no.3, pp. 183-214, 1987.

j3 Y. Moon, N. Bagherzadeh, and J. Sklansky, "A macropipelined multicomputer architecture for image analysis," *Journal of the Optical Society of America*, pp. 951-962, 1989.

j4 D. Blough and N. Bagherzadeh, "Near-optimal message routing and broadcasting in faulty hypercubes," *International Journal of Parallel Programming*, vol. 19, no. 5, pp. 405-423, 1990.

j5 N. Bagherzadeh, S. Heng, and C. Wu, "A parallel asynchronous garbage collection algorithm for distributed systems," *IEEE Transactions on Knowledge and Data Engineering*, vol. 3, no. 1, pp. 100-107, March 1991.

j6 A. Kavianpour and N. Bagherzadeh, "Application of three-valued logic for distributed termination detection," *International Journal of Computers and Electrical Engineering*, vol. 17, no. 2, pp. 65-74, 1991.

j7 A. Kavianpour and N. Bagherzadeh, "Finding circular shapes in an image on a pyramid architecture," *Pattern Recognition Letters,* vol. 13, no. 12, pp. 843-848, December 1992.

j8 N. Bagherzadeh and K. Hawk, "Parallel implementation of the auction algorithm on the Intel hypercube," *Journal of Computer and Software Engineering*, vol. 1, no. 1, pp. 17-32, 1993.

j9 A. Abnous, C. Christensen, J. Gray, J. Lenell, A. Naylor, and N. Bagherzadeh, "Design and implementation of the 'Tiny RISC' microprocessor," *Journal of Microprocessors and Microsystems,* vol. 16, no. 4, pp.187-193, 1992.

j10 A. Abnous and N. Bagherzadeh, "Pipelining and bypassing in a VLIW processor," *IEEE Transactions on Parallel and Distributed Systems*, vol. 5, no. 6, pp. 658-664, June 1994.

j11 A. Kavianpour and N. Bagherzadeh, "A systematic approach for mapping application tasks in hypercubes," *IEEE Transactions on Computers*, vol. 42, no. 6, pp. 742-746, June 1993.

j12 A. Kavianpour and N. Bagherzadeh, "Parallel algorithms for line detection on a pyramid architecture," *International Journal of Pattern Recognition and Artificial Intelligence*, Vol. 8, no.1, pp. 337-349, 1994.

j13 C. Bowen and N. Bagherzadeh, "Image processing applications in C++ on a hypercube multicomputer," *International Journal of Computers and Electrical Engineering*, vol. 19, no. 5, pp. 351-364,1993.

j14 A. Kavianpour, S. Shoari, and N. Bagherzadeh, "A new approach for circle detection on multiprocessors," *Journal of Parallel and Distributed Computing*, vol. 20, no. 2, pp. 256-260, February 1994.

j15 S. Latifi and N. Bagherzadeh, "Incomplete star: An incrementally scalable network based on the star graph," *IEEE Transactions on Parallel and Distributed Systems*, vol. 5, no. 1, pp. 97-102, January 1994.

j16 N. Bagherzadeh, N. Nassif, and S. Latifi, "A routing and broadcasting scheme on faulty star graphs," *IEEE Transactions on Computers*, Vol 42, no. 11, pp 1398-1403, November 1993.

j17 J. Gray, A. Naylor, A. Abnous, and N. Bagherzadeh, "VIPER: a VLIW integer microprocessor," *IEEE Journal of Solid States and Circuits*, Vol. 28, no. 12, pp 1377-1383, December 1993.

j18 J. Lenell and N. Bagherzadeh, "A performance comparison of several superscalar processor models with a VLIW processor," *Journal of Microprocessors and Microsystems*, Vol 18, no. 3, pp 232-242, 1994.

j19 A. Kavianpour, N. Bagherzadeh, and S. Shoari, “Finding elliptical shapes in an image using a pyramid architecture, ” *International Journal of Computers and Electrical Engineering*, vol. 21, no. 1, pp. 69-75, Jan 1995.

j20 S. Latifi, M. M. de Azevedo, and N. Bagherzadeh, “A star-based I/O-bounded network for massively parallel systems,” *IEE Proceedings-Computers and Digital Techniques*, Vol. 142, No. 1, January 1995.

j21 M. M. de Azevedo, N. Bagherzadeh, and S. Latifi, "Broadcasting algorithms for the star-connected cycles interconnection network," *Journal of Parallel and Distributed Computing*, 25, 209-222 (1995).

j22 S. Wallace and N. Bagherzadeh, "Performance issues of a superscalar microprocessor," *Microprocessors and Microsystems*, Vol. 19, No. 4, pp 187-199 (1995).

j23 A. Abnous and N. Bagherzadeh, "Architectural design and analysis of a VLIW processor," *International Journal of Computers and Electrical Engineering*, Vol 21, No. 2, pp 119-142 (1995).

j24 T. Kato and N. Bagherzadeh, "A novel superscalar architecture using scheduling patterns and performance analysis," *The Transactions of the Institute of Electronics, Information, and Communication Engineers D-I*, Vol.J78-D-I, No. 9, pp 809-819 (1995).

j25 N. Bagherzadeh and M. Dowd, "Computation in faulty stars," *IEEE Transactions on Reliability*, Vol 44, No. 1, pp 114-119 (1995).

j26 N. Bagherzadeh, M. Dowd, and S. Latifi, "A well-behaved enumeration of star graphs," *IEEE Transactions on Parallel and Distributed Systems*, Vol 6, No. 5, pp 531-535, May (1995).

j27 M. M. de Azevedo, N. Bagherzadeh, M. Dowd, and S. Latifi, "Some topological properties of star connected cycles," *Information Processing Letters*, 58, pp 81-85 (1996).

j28 N. Bagherzadeh, M. Dowd, and N. Nassif, "Embedding an arbitrary binary tree into the star graph," *IEEE Transactions on Computers*, Vol 45, No. 4, pp 475-481 (1996).

j29 N. Bagherzadeh and M. Dowd, "Problems on routing bounded distance assignments in hypercubes," *Computer Systems-Science and Engineering*, Vol 11, No. 4, pp 221-226, July (1996).

j30 S. Latifi and N. Bagherzadeh, "On cluster-star graph and its properties," *Computer Systems-Science and Engineering*, Vol 11, No. 3, pp 145-149, May (1996).

j31 S. Shoari and N. Bagherzadeh, "Computation of the fast fourier transform on the star-connected cycle networks," *International Journal of Computers and Electrical Engineering*, Vol 22, No. 4, pp 235-246 (1996).

j32 N. Nassif and N. Bagherzadeh, "A grid embedding into the star graph for image analysis solutions," *Information Processing Letters*, Vol. 60, No. 5, pp 255-260 (1996).

j33 S. Latifi, N. Bagherzadeh, and R. Gajjala, "Fault-tolerant embedding of linear arrays and rings in the star graph," *International Journal of Computers and Electrical Engineering*, Vol 23, No. 2, pp 95-107 (1997).

j34 S. Latifi and N. Bagherzadeh, "On embedding rings into a star-related network," *Information Sciences*, Vol. 99, No. 1-2, pp 21-35 (1997)

j35 S. Shoari, N. Bagherzadeh, T. Milner, and J. S. Nelson, "Moment algorithms for blood vessel detection in infrared images of laser-heated skin," *International Journal of Computers and Electrical Engineering,* Vol 23, No. 5, January (1998).

j36 M. M. de Azevedo, N. Bagherzadeh, M. Dowd, and S. Latifi, "Average distance and routing algorithms in the star-connected cycles interconnection network," *International Journal of Science and Technology-Special Issue of Computer in Scientia Iranica,* Vol. 3, No. 4, (1997).

j37 N. Bagherzadeh, M. Dowd, and S. Latifi, "Faster Column Operations in Star Networks," *Telecommunication Systems,* Vol. 10, Nos. 1, 2 (1998).

j38 M. M. de Azevedo, N. Bagherzadeh, and S. Latifi, "Low expansion packings and embeddings of hypercubes into star graphs: a performance-oriented approach," *IEEE Transactions on Parallel and Distributed Systems,* Vol. 9, No. 3, (1998).

j39 S. Shoari, N. Bagherzadeh, D. Goodman, T.E. Milner, D. J. Smithies, and J.S. Nelson, "A parallel algorithm for pulsed laser infrared tomography," *Pattern Recognition Letters,* 19 (1998).

j40 S. Wallace and N. Bagherzadeh, "A scalable register file architecture for superscalar processors," *Microprocessors and Microsystems,* Vol. 22, No. 1, (1998).

j41 S. Wallace and N. Bagherzadeh, "Modeled and measured instruction fetching performance for superscalar microprocessors," *IEEE Transactions on Parallel and Distributed Systems,* Vol. 9, No. 6, (1998).

j42 N. Nassif and N. Bagherzadeh, "Image component labeling on the star graph using divide and conquer," *IEE Proceedings-Computers and Digital Techniques,* Vol. 145, No. 1, (1998).

j43 M. Lee, G. Lu, H. Singh, N. Bagherzadeh, F. Kurdahi, E. Filho, and V. Castro Alves, "MorphoSys A Reconfigurable Computing Chip," *IEEE Circuits and Systems Newsletter,* Vol. 10, No 1, March/April 1999.

j44 M. Lee, H. Singh, G. Lu, N. Bagherzadeh, F. Kurdahi, E. Filho, and V. Castro Alves, "Design and Implementation of the MorphoSys Reconfigurable Computing

Processor," *Journal of Signal Processing Systems for Signal, Image, and Video technology,* Vol. 24, No. 2/3, pp. 147-164, March 2000.

j45 H. Singh, M. Lee, G. Lu, F. Kurdahi, N. Bagherzadeh, and E. Filho, "MorphoSys: An Integrated Reconfigurable System for Data-Parallel and Computation-Intensive Applications," *IEEE Transactions on Computers,* Vol. 49, No. 5, pp. 465-481 (2000).

j46 R. Maestre, F. Kurdahi, M. Fernandez, R. Hermida, N. Bagherzadeh, and H. Singh, "Kernel scheduling techniques for efficient solution of space exploration in reconfigurable computing," *EUROMICRO Journal of Systems Architecture on Modern Methods and Tools in Digital System Design*, 2000.

j47 R. Maestre, F. Kurdahi, M. Fernandez, R. Hermida, N. Bagherzadeh, and H. Singh, "A Formal Approach to Context Scheduling for Multi-context Reconfigurable Architectures," *IEEE Transactions on VLSI Design-Special Issue on Reconfigurable Computing*, Vol. 9, Issue 1, pp. 173-185, Feb 2001.

j48 R. Maestre, F. Kurdahi, M. Fernandez, R. Hermida, N. Bagherzadeh, and H. Singh, "A Framework for Reconfigurable Computing: Task Scheduling and Context Management," *IEEE Transactions on VLSI Design-Special Issue on System Level Design*, Vol. 9, Issue 6, pp. 858-873, Dec 2001 (Best Paper Award).

j49 P. Chou, J. Liu, D. Li, and N. Bagherzadeh, "IMPACCT: Methodology and Tools for Power-Aware Embedded Systems," *Kluwer Design Automation of Embedded Systems*, pp. 205-232, October 2002.

j50 J. Liu, P. Chou, and N. Bagherzadeh, "Power-Aware Task Motion for Enhancing Dynamic Range of Embedded Systems with Renewable Energy Sources in Proceedings of the Workshop on Power Aware Computer Systems," in *Lecture Notes in Computer Science* (LNCS), Springer-Verlag, pp. 84--99. 2002.

j51 R. Maestre, F. Kurdahi, M. Fernandez, R. Hermida, N. Bagherzadeh, and H. Singh, "A Framework for Reconfigurable Computing: Task Scheduling and Context Management-a Summary," *Circuits and Systems Magazine*, IEEE, Vol. 2, Issue 4, pp. 48-51, 2002.

j52 M. Sanchez-Elez, H. Du, N. Tabrizi, Y. Lung, N. Bagherzadeh, and M. Fernandez, "Algorithm Optimizations and Mapping Scheme for Interactive Ray Tracing on a Reconfigurable Architecture," *Computers & Graphics*, 2003

j53 G. Venkataramani, W. Najjar, F. Kurdahi, N. Bagherzadeh, W. Bohm and J. Hammes, "Automatic Compilation to a Coarse-grained Reconfigurable System-on-Chip," *ACM Trans. on Embedded Computing Systems*, November 2003.

j54 B. Gorjiara, N. Bagherzadeh, and P. Chou, "Ultra-fast and Efficient Algorithm for Energy Optimization by Gradient-based Stochastic Voltage and Task Scheduling,"

ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 12 , Issue 4 (September 2007)

j55 J. Bahn, S. Lee, and N. Bagherzadeh, "Design of a Router for Network-on-Chip," *International Journal of High Performance Systems Architecture,* 2007 - Vol. 1, No.2 pp. 98 - 105

j56 A. Niktash, H. Parizi, and N. Bagherzadeh, "A Reconfigurable Processor for Forward Error Correction," *ARCS 2007,* LNCS 4415, pp. 1-13, 2007

j57 J. Bahn and N. Bagherzadeh, "Design of Simulation and Analytical Models for a 2D-meshed Asymmetric Adaptive Router," *Computers & Digital Techniques, IET,* Volume 2, Issue 1, January 2008 Page(s):63 - 73

j58 F. Rivera, M. Sanchez-Elez, R. Hermida, and N. Bagherzadeh, "Scheduling methodology for conditional execution of kernels onto multicontext reconfigurable architectures," *Computers & Digital Techniques, IET,* Volume 2, Issue 3, May 2008 Page(s):199 - 213

j59 J. Bahn, S. Lee, Y. Yang, J. Yang, and N. Bagherzadeh, "On Design and Application Mapping of a Network-on-Chip (NoC) Architecture," *Parallel Processing Letters (PPL),* Volume: 18, Issue: 2 (June 2008), pp. 239 - 255

j60 N. Tabrizi and N. Bagherzadeh, "An ASIC Design and Formal Analysis of a Novel Pipelined and Parallel Sorting Accelerator," *Integration, The VLSI Journal,* Volume 41, Issue 1 (January 2008), Pages 65-75

j61 S. Lee, J. Bahn, Y. Yang, and N. Bagherzadeh, "A Generic Network Interface architecture for a Networked Processor Array (NePA)," *ARCS 2008,* LNCS 4934, pp. 247–260, 2008

j62 J. Bahn, J. Yang, W. Hu, and N. Bagherzadeh, "Parallel FFT Algorithms on Network-on-Chips," *Journal of Circuits, Systems, and Computers* 18(2): 255-269, 2009.

j63 F. Bagci, F. Kluge, T. Ungerer, and N. Bagherzadeh, "Optimisations for LocSens - an Indoor Location Tracking System Using Wireless Sensors," *International Journal of Sensor Networks (IJSNET)*, Vol. 6, Nos. 3/4, 2009.

j64 J. Bahn and N. Bagherzadeh, "On-Chip Interconnection Network with an Efficient Parallel Buffer
Structure and Generic Traffic," *Scientia Iranica*, Computer Science & Engineering and Electrical Engineering. Vol. 16, No. 2, pp. 104-118, 2009.

j65 M. Sanchez-Elez, N. Bagherzadeh, and R. Hermida, "A Framework for Low Energy Data Management in Reconfigurable Multi-Context Architectures," *Journal of Systems Architecture*, 2009, Pages 127-139

j66 S. Lee and N. Bagherzadeh, "A Variable Frequency Link for a Power-Aware Network-on-Chip (NoC))," *INTEGRATION, the VLSI Journal,* 42 (2009) 479–485

j67 S. Lee and N. Bagherzadeh, "A High Level Power Model for Network-on-Chip (NoC) Router," *Computers and Electrical Engineering,* 35 (2009) 837–845

j68 Y. Yang, J. Bahn, S. Lee, J. Yang, and N. Bagherzadeh, "Parallel Processing for Block Ciphers on a Fault Tolerant Networked Processor Array," *International Journal of High Performance Systems Architecture,* Vol. 2, Nos. 3/4, 2010

j69 J. Yang, S. Lee, C. Chen, and N. Bagherzadeh, "Ray Tracing on a Networked Processor Array," *International Journal of Electronics*, 2010, 97(10):1193-1205

j70 F. Bagci, T. Ungerer, and N. Bagherzadeh, "Multi-level Security in Wireless Sensor Networks," *International Journal on Advances in Software*, Vol. 4, No. 6, 2010.

j71 C. Wang, W. Hu, S. Lee, and N. Bagherzadeh, "Area and Power-Efficient Innovative Congestion-Aware Network-on-Chip," *Journal of Systems Architecture*, Volume 57 Issue 1, Pages 24-38, January, 2011

j72 A. Hatanaka and N. Bagherzadeh, "A Scheduling Approach for Distributed Resource Architectures with Scarce Communication Resources," *Int. J. High Performance Systems Architecture,* Vol. 3, No. 1, Pages 12-22, 2011

j73 C. Wang and N. Bagherzadeh, "High-throughput Differentiated Service Provision Router Architecture for Wireless Network-on-Chip," *Int. J. High Performance Systems Architecture,* Vol. 4, No. 1, Pages 38-56, 2012

j74 F. Bolanos, J. Aedo, F. Rivera, and N. Bagherzadeh, "Mapping and Scheduling in Heterogeneous NoC through Population-Based Incremental Learning," *Journal of Universal Computer Science,* vol. 18, no. 7 (2012), 901-916

j75 W. Hu, C. Chen, J. Bahn, and N. Bagherzadeh, "Parallel Low-Density Parity Check Decoding on a Network-on-Chip-Based Multiprocessor Platform," *IET Computers & Digital Techniques*, Vol. 6, Issue. 2, pp. 86–94, 2012

j76 A. Hatanaka and N. Bagherzadeh, "A Software Pipelining Algorithm of Streaming Applications with Low Buffer Requirements," *Transactions D: Computer Science & Engineering and Electrical Engineering,* Vol. 19, No. 3, Pages 627-634, 2012

j77 H. Abdullah, H. A. Elsadek, H. E. ElDeeb, and N. Bagherzadeh, "Fractional Derivatives Based Scheme for FDTD Modeling of nth-Order Cole–Cole Dispersive Media," *IEEE Antennas and Wireless Propagation Letters,* Vol. 11, Pages 281-284, 2012

j78 A. Alhussien, C. Wang, and N. Bagherzadeh, "Design and Evaluation of a High Throughput Robust Router for Network-on-Chip," *IET Computers & Digital Technique,* Vol. 6, Issue. 3, pp. 173–179, 2012

j79 C. Wang, W. Hu, and N. Bagherzadeh, "A Load-Balanced Congestion-Aware Wireless Network-on-Chip Design for Multi-Core Platforms," *Microprocessors and Microsystems,* Vol. 36, Issue. 7, pp. 555-570, 2012

j80 S. Azampanah, A. Khademzadeh, N. Bagherzadeh, M. Janidarmian, and R. Shojaee "Contention-Aware Selection Strategy for Application-Specific Network-on-Chip," *IET Computers & Digital Technique,* Vol. 7, Issue. 3, pp. 105-114, 2013

j81 F. Bolanos, F. Rivera, J.E. Aedo, and N. Bagherzadeh, "From UML Specifications to Mapping and Scheduling of Tasks into a NoC, with Reliability Considerations," *Journal of Systems Architecture,* Vol. 59, Issue 7, pp. 429-440, 2013

j82 X. Wang, M. Yang, Y. Jiang, M. Palesi, P. Liu, T. Mak, and N. Bagherzadeh, "Efficient Multicast Schemes for 3-D Networks-on-Chip," *Journal of Systems Architecture,* Vol. 59, Issue 9, pp. 693-708, 2013

j83 A. Alhussien, F. Verbeek, B. van Gastel, N. Bagherzadeh, and J. Schmaltz, "Fully Reliable Dynamic Routing Logic for a Fault-Tolerant NoC Architecture," *Journal of Integrated Circuits and Systems,* Vol. 8, Issue. 1, pp. 43-53, 2013

j84 C. Wang, W. Hu, and N. Bagherzadeh, "Scalable Load Balancing Congestion-Aware Network-on-Chip Router Architecture," *Journal of Computer and System Sciences,* Vol. 79, Issue. 4, pp. 421-439, 2013

j85 A. Demiriz, N. Bagherzadeh, and A. Alhussein, "Using Constraint Programming for the Design of Network-on-Chip Architectures," *Computing (Springer),* DOI 10.1007/s00607-013-0359-4, 2013

j86 C. Wang and N. Bagherzadeh, "Design and Evaluation of a High Throughput QoS-Aware and Congestion-Aware Router Architecture for Network-on-Chip," *Microprocessors and Microsystems,* Vol. 38, Issue. 4, pp. 304-315, 2014

j87 A. Del Barrio, N. Bagherzadeh, and R. Hermida, "Ultra-Low-Power Adder Stage Design for Exascale Floating Point Units," *ACM Transactions on Embedded Computing Systems(TECS),* Vol. 13, Issue. 3, Article No. 105, March 2014

j88 R. Mirzaee, K. Navi, and N. Bagherzadeh, "High-Efficient Circuits for Ternary Addition," *VLSI Design*, Volume 2014, Article ID 534587, pp.1-15, 2014

j89 S. Angizi, E. Alkaldy, N. Bagherzadeh, and K. Navi, "Novel Robust Single Layer Wire Crossing Approach for Exclusive OR Sum of Products Logic Design with Quantum-

Dot Cellular Automata," *Journal of Low Power Electronics*, Vol. 10, No. 2, pp. 259-271, 2014

j90 A. Demiriz, N. Bagherzadeh, and O. Ozturk, "Voltage Island Based Heterogeneous NoC Design Through Constraint Programming," *Computers and Electrical Engineering (Elsevier),* 40 (2014) 307-316

j91 W. Hu, C. Wang, and N. Bagherzadeh, "Design and Analysis of a Mesh-Based Wireless Network-on-Chip," *Journal of Supercomputing (Springer)*, DOI 10.1007/s11227-014-1341-4, 22 November, 2014

j92 F. Sharifi, M. H. Moaiyeri, K. Navi, and N. Bagherzadeh, "Quaternary Full Adder Cells Based on Carbon Nanotube FETs," *Journal of Computer. Electronics (Springer)*, DOI 10.1007/s10825-015-0714-0, 2015

j93 M. Khayambashi, P. Yaghini, A. Eghbal, and N. Bagherzadeh, "Analytical Reliability Analysis of 3D NoC under TSV Failure," *ACM Journal on Emerging Technologies in Computing Systems*, Vol. 11, No. 4, Article 43, April 2015

j94 H. Karkhaneh, J-M. Liu, A. Ghorbani, and N. Bagherzadeh, "Fiber Dispersion Effects in Injection-Locked Optical OFDM Systems," *Optical and Quantum Electronics (Springer)*, DOI 10.1007/s11082-015-0197-z (2015)

j95 P. Yaghini, A. Eghbal, S. Yazdi, N. Bagherzadeh, and M. Green, "Capacitive and Inductive TSV-to-TSV Resilient Approaches for 3D ICs," *IEEE Transactions on Computers*, Vol. 65, No. 3, pp. 693-705, March 2016, Digital Object Identifier no. 10.1109/TC.2015.2498550

j96 A. Demiriz, N. Bagherzadeh, and A. Alhussein, "Using Constraint Programming for the Design of Network-on-Chip Architectures," *Computing* (Springer), (2015) 97:579–592, DOI 10.1007/s00607-013-0359-4

j97 P. Yaghini, A. Eghbal, M. Khayambashi, and N. Bagherzadeh, "Coupling Mitigation in 3-D Multiple-Stacked Devices," *IEEE Transactions on VLSI Systems*, Vol. 23, Issue: 12, 2015

j98 S. Angizi, F. Danehdaran, S. Sarmadi, N. Bagherzadeh, and K. Navi, "An Ultra-High Speed and Low Complexity Quantum-Dot Cellular Automata Full Adder," *Journal of Low Power Electronics*, Vol. 11, No. 2, pp. 173-180(8), 2015

j99 A. Eghbal, P. Yaghini, N. Bagherzadeh, and M. Khayambashi, "Analytical Fault Tolerance Assessment and Metrics for TSV-Based 3D Network-on-Chip," *IEEE Transactions on Computers*, Vol. 64, No. 12, pp. 3591-2604, December (2015); Digital Object Identifier no. 10.1109/TC.2015.2401016

j100 S. Angizi, M. Moaiyeri, S. Farrokhi, K. Navi, and N. Bagherzadeh, "Designing Quantum-dot Cellular Automata Counters with Energy Consumption Analysis," *Microprocessors and Microsystems*, 2015, DOI: http://dx.doi.org/10.1016/j.micpro.2015.07.011

j101 S. Angizi, S. Sayedsalehi, A. Roohi, N. Bagherzadeh, and K. Navi, "Design and Verification of New n-Bit Quantum-Dot Synchronous Counters Using Majority Function-Based JK Flip-Flops," *Journal of Circuits, Systems, and Computers*, Vol. 24, No. 10 (2015) 1550153 (17 pages); DOI: 10.1142/S0218126615501534

j102 R. Mirzaee, M. Jasemi, A. Valizadeh, and N. Bagherzadeh, "On the Design of Fully Symmetrical Bridge-Style Circuits," *IETE Journal of Research*, (2015); DOI: 10.1080/03772063.2015.1065712

j103 M. Jasemi, R. Mirzaee, K. Navi, and N. Bagherzadeh, "Voltage Mirror Circuit by Carbon Nanotube Field Effect Transistors for Mirroring Dynamic Random Access Memories in Multiple-Valued Logic and Fuzzy Logic," *IET Circuits, Devices, and Systems*, Vol. 9, Iss5, pp. 343-352, (2015); DOI: 10.1049/iet-cds.2014.0295

j104 F. Sharifi, M. H. Moaiyeri, K. Navi, and N. Bagherzadeh, "Robust and Energy Efficient Carbon Nanotube FET-Based MVL Gates: A Novel Design Approach," *Microelectronics Journal (Elsevier)*, 46 (2015) 1333-1342.

j105 P. Yaghini, A. Eghbal, S. Yazdi, N. Bagherzadeh, "On the Design of Hybrid Routing Mechanism for Mesh-Based Network-on-Chip," *INTEGRATION, the VLSI journal*, 50 (2015) 183-192, http://dx.doi.org/10.1016/j.vlsi.2014.12.006

j106 M. Moaiyeri, N. Khastoo, M. Nasiri, K. Navi, and N. Bagherzadeh "An Efficient Analog-to-Digital Converter Based on Carbon Nanotube FETs," *Journal of Low Power Electronics*, Vol. 12, 150-157, 2016. doi:10.1166/jolpe.2016.1432

j107 F. Sharifi, M. Moaiyeri, K. Navi, and N. Bagherzadeh, "Ultra-Low-Power Carbon Nanotube FET-Based Quaternary Logic Gates," *International Journal of Electronics*," Vol. 103, No. 9, pp. 1524-1537, 2016, http://dx.doi.org/10.1080/21681724.2016.1138506

j108 M. Agyeman, A. Ahmadinia, and N. Bagherzadeh, "Performance and Energy Aware Inhomogeneous 3D Networks-on-Chip Architecture Generation," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 27, No. 6, pp. 1756-1769, June 2016, Digital Object Identifier no. 10.1109/TPDS.2015.2457444

j109 H. Shabani, A. Roohi, A. Reza, M. Reshadi, N. Bagherzadeh, and R. DeMara, "Loss-Aware Switch Design and Non-Blocking Detection Algorithm for Intra-Chip Scale Photonic Interconnection Networks," *IEEE Transactions on Computers*, Vol. 65, No. 6, pp. 1789-1801, June 2016, Digital Object Identifier no. 10.1109/TC.2015.2458866

j110 M. Daliri, K. Navi, R. Mirzaee, S. Daliri, and N. Bagherzadeh "A New Approach for Designing Compressors with a New Hardware-Friendly Mathematical Method for Multi-Input XOR gates," *IET Circuits, Devices, and Systems*, Vol. 11, Iss. 1 pp. 46-57, 2016, Doi: 10.1049/iet-cds.2016.0041

j111 M. Daliri, R. Mirzaee, K. Navi, and N. Bagherzadeh "Ternary Cyclic Redundancy Check by a New Hardware-Friendly Ternary Operator," *Microelectronics Journal*, pp. 126-137, 2016, http://dx.doi.org/10.1016/j.mejo.2016.04.018

j112 R. Salamat, M. Khayambashi, M. Ebrahimi, and N. Bagherzadeh "A Resilient Routing Algorithm with Formal Reliability Analysis for Partially Connected 3D-NoCs," *IEEE Transactions on Computers*, Vol. 65, No. 11, pp. 3265-3279, 2016, Digital Object Identifier no. 10.1109/TC.2016.2532871

j113 F. Sharifi, A. Panahi, H. Sharifi, K. Navi, N. Bagherzadeh, and H. Thaliyal, "Design of Quaternary 4–2 and 5–2 Compressors for Nanotechnology," *Computers and Electrical Engineering*," pp. 64-74, 2016, http://dx.doi.org/10.1016/j.compeleceng.2016.11.006

j114 A. Bozorgmehr, M. Moaiyeri, K. Navi, and N. Bagherzadeh "Ultra-Efficient Fuzzy Min/Max Circuits Based on Carbon Nanotube FETs," *IEEE Transactions on Fuzzy Systems*, 2017, DOI 10.1109/TFUZZ.2017.2697404

j115 M. Daliri, R. Mirzaee, K. Navi, and N. Bagherzadeh "High-Performance Ternary Operators for Scrambling," *INTEGRATION the VLSI Journal*, 59 (2017), http://dx.doi.org/10.1016/j.vlsi.2017.03.010

j116 H. Zhao, N. Bagherzadeh, and J. Wu, "A General Fault-Tolerant Minimal Routing for Mesh Architectures," *IEEE Transactions on Computers*," Vol. 66, No. 7, pp. 1240-1246, 2017, Digital Object Identifier no. 10.1109/TC.2017.2651828

j117 Z. Ghaderi, M. Ebrahimi, Z. Navabi, E. Bozorgzadeh, and N. Bagherzadeh, "SENSIBle: A Highly Scalable SENsor DeSIgn for Path-Based Age Monitoring in FPGAs," *IEEE Transactions on Computers*," Vol. 66, No. 5, pp. 919-926, 2017, Digital Object Identifier no. 10.1109/TC.2016.2622688

j118 M. Bagherian, M. Daliri, A. Abdoli, K. Navi, and N. Bagherzadeh, "A 3D Universal Structure Based on Molecular-QCA and CNT Technologies," *Journal of Molecular Structure*, MOLSTR 22439, (2016), 10.1016/j.molstruc.2016.04.025

j119 A. Noghondar, M. Rishadi, and N. Bagherzadeh, " Reducing bypass-based network-on-chip latency using priority mechanism," IET Computers & Digital Techniques, pp. 1-8, 2017, doi: 10.1049/iet-cdt.2016.0161

j120 M. Bagherian, M. Moaiyeri, S. Angizi, N. Bagherzadeh, and K. Navi, " Quantum-dot cellular automata circuits with re duce d external fixed inputs," Microprocessors and Microsystems, 50 (2017) 154-163, http://dx.doi.org/10.1016/j.micpro.2017.03.009

j121 M. Berarzadeh, S. Mohammadyan, K. Navi, and N. Bagherzadeh, "A Novel Low Power Exclusive-OR via Cell Level-based Design Function in Quantum Cellular Automata," *Journal of Computational Electronics* (*Springer*), DOI 10.1007/s10825-017-0986-7, April, 2017

j122 S. Tabrizchi, A. Panahi, F. Sharifi, K. Navi, and N. Bagherzadeh, " Method for Designing Ternary Adder Cells Based on CNFETs," *IET Circuits, Devices & Systems*, doi: 10.1049/iet-cds.2016.0443, (2017)

j123 F. Verbeek, P. Yaghini, A. Eghbal, and N. Bagherzadeh, "Deadlock Verification of Cache Coherence Protocols and Communication Fabrics," *IEEE Transactions on Computers*, Vol. 66, No. 2, Digital Object Identifier no. 10.1109/TC.2016.2584060, February 2017

j124 Z. Rouhani, S. Angizi, M. Taheri, K. Navi, N. Bagherzadeh, "Towards Approximate Computing with Quantum-Dot Cellular Automata," *Journal of Low Power Electronics*, Vol. 13, No. 1, pp 29-35, doi:10.1166/jolpe.2017.1475, 2017

j125 Z. Ghaderi, N. Bagherzadeh, and A. Albaqsami, " STABLE: Stress-Aware Boolean Matching to Mitigate BTI-Induced SNM Reduction in SRAM-Based FPGAs," *IEEE Transactions on Computers*, Vol. 67, No. 1, Digital Object Identifier no. 10.1109/TC.2017.2725952, 2017

j126 M. Bagherian, M. Moaiyeri, K. Navi, and N. Bagherzadeh, " An Energy and Cost Efficient Majority-based RAM Cell in Quantum-dot Cellular Automata," *Results in Physics (Elsevier)*, https://doi.org/10.1016/j.rinp.2017.08.067, 2017

j127 A. Arasteh, M. Moaiyeri, M. Taheri, K. Navi, and N. Bagherzadeh, " An Energy and Area Efficient 4:2 Compressor Based on FinFETs," *Integration the VLSI Journal*, DOI: 10.1016/j.vlsi.2017.09.010, (60) October 2017

j128 S. Angizi, Z. He, N. Bagherzadeh, and D. Fan, "Design and Evaluation of a Spintronic In-Memory Processing Platform for Nonvolatile Data Encryption," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 37. No. 9, Digital Object Identifier 10.1109/TCAD.2017.2774291, September 2018

j129 F. Khubrani, N. Bagherzadeh, and N. Meshkati, "Importance of Safety Culture at Pre-Operational Phase to Prevent Nuclear Plant Accidents," *International Journal of Atomic and Nuclear Physics*, 2017

j130 R. Salamat, M. Khayambashi, M. Ebrahimi, and N. Bagherzadeh, " LEAD: An Adaptive 3D-NoC Routing Algorithm with Queuing-theory Based Analytical

Verification," *IEEE Transactions on Computers*, Vol. 67, No. 8, Digital Object Identifier no. 10.1109/TC.2018.2801298, August 2018

j131 R. Mirzaee, M. Daliri, K. Navi, and N. Bagherzadeh, "A Single Parity-Check Digit for One Trit Error Detection in Ternary Communication Systems: Gate-Level and Transistor-Level Designs," *Journal of Multiple-Valued Logic and Soft Computing*, 29 3-4), August 2017

j132 M. Agyeman, A. Ahmadinia, and N. Bagherzadeh, "Energy and Performance-aware Application Mapping for Inhomogeneous 3D Networks-on-Chip," *Journal of Systems Architecture* 89 (2018) 103-117, https://doi.org/10.1016/j.sysarc.2018.08.002

j133 F. Khodaparast, M. Reshadi, and N. Bagherzadeh, "Application Partitioning and Mapping for Bypass Channel Based NoC," *Computers and Electrical Engineering (Elsevier)*, 71 (2018) 676-691, https://doi.org/10.1016/j.compeleceng.2018.08.016

j134 F. Danehdaran, M. Bagherian, K. Navi, and N. Bagherzadeh, "Design and Power Analysis of New Coplanar One-Bit Full-Adder Cell in Quantum-Dot Cellular Automata," *Journal of Low Power Electronics*, Vol. 14, 1-11, 2018

j135 A. Alqahtani, Z. Ren, J. Lee, and N. Bagherzadeh, "System-Level Analysis of 3D ICs with Thermal TSVs," *ACM Journal on Emerging Technologies in Computing Systems*, Vol. 14, No. 3, Article 37. Pub. date: October 2018, https://doi.org/10.1145/3264736

j136 A. Haghighathoseini, H. Bobarshad, F. Saghafi, M. Rezaei, and N. Bagherzadeh, "Hospital Enterprise Architecture Framework (Study of Iranian University Hospital Organization)," International Journal of Medical Informatics, https://doi.org/10.1016/j.ijmedinf.2018.03.009

j137 Z. Ghaderi, A. Alqahtani, and N. Bagherzadeh, "AROMa: Aging-Aware Deadlock-Free Adaptive Routing Algorithm and Online Monitoring in 3D NoCs," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 29, No. 4, April 2018, Digital Object Identifier no. 10.1109/TPDS.2017.2780173

j138 A. Charif, A. Coelho, M. Ebrahimi, N. Bagherzadeh, and N. Zergainoh, "First-Last: A Cost-Effective Adaptive Routing Solution for TSV-Based Three-Dimensional Networks-on-Chip," *IEEE Transactions on Computers*, Vol. 67, No. 10, October 2018, Digital Object Identifier no. 10.1109/TC.2018.2822269

j139 M. Kim, A. Del Barrio, L. Tavares Oliveira, R. Hermida, and N. Bagherzadeh, "Efficient Mitchell's Approximate Log Multipliers for Convolutional Neural Networks," *IEEE Transactions on Computers*, Vol. 68, No. 5, May 2019, Digital Object Identifier no. 10.1109/TC.2018.2880742

j140 A. Shahkarami, H. Bobarshad, and N. Bagherzadeh, "A Stream-Sensitive Distributed Approach for Configuring Cascaded Classifier Topologies in Real-Time Large-Scale

Stream Mining Systems," *SN Applied Sciences*, (2019), https://doi.org/10.1007/s42452-019-0565-6

j141 M. Torabzadekashi, S. Rezaei, A. Heydari, H. Bobarshad, V. Alves, and N. Bagherzadeh, "Computational Storage: an Efficient and Scalable Platform for Big Data and HPC Applications," *Journal of Big Data*, (2019) 6:100, https://doi.org/10.1186/s40537-019-0265-5

j142 A. Mehranzadeh, A. Khademzadeh, N. Bagherzadeh, and M. Rishadi, "DICA: Destination Intensity and Congestion-aware Output Selection Strategy for Network-on-Chip Systems," *IET Computers & Digital Techniques*, doi: 10.1049/iet-cdt.2018.5154, 2020.

j143 S. Tabrizchi, M. Taheri, K. Navi, and N. Bagherzadeh, "Novel CNFET Ternary Circuit Techniques for High-Performance and Energy-Efficient Design," *IET Circuits, Devices & Systems*, doi: 10.1049/iet-cds.2018.5036

j144 M. Zahmatkesh, S. Tabrizchi, S. Mohammadyan, K. Navi, and N. Bagherzadeh, "Robust Coplanar Full Adder Based on Novel Inverter in Quantum Cellular Automata," *International Journal of Theoretical Physics* (2019) 58:639–655, https://doi.org/10.1007/s10773-018-3961-6

j145 M. Soleymani, M. Reshadi, and N. Bagherzadeh, "CLBM: Controlled Load-Balancing Mechanism for Congestion Management in Silicon Interposer NoC Architecture," *Journal of Systems Architecture*, https://doi.org/10.1016/j.sysarc.2019.07.003, 98 (2019) 102-113

j146 F. Danehdaran, S. Angizi, M. Bagherian, K. Navi, and N. Bagherzadeh, "A combined three and five inputs majority gate-based high performance coplanar full adder in quantum-dot cellular automata," *Int. j. inf. tecnol.*, https://doi.org/10.1007/s41870-019-00365-z

j147 L. Garcia Morales, J.E. Aedo Cobo, and N. Bagherzadeh, "A New Approach to the Population-Based Incremental Learning algorithm using Virtual Regions for Task Mapping on NoCs, *Journal of Systems Architecture*, https://doi.org/10.1016/j.sysarc.2019.01.013, p. 443-454, 2019

j148 M. Toulabinejad, M. Taheri, K. Navi, and N. Bagherzadeh, "Toward Efficient Implementation of Basic Balanced Ternary Arithmetic Operations in CNFET Technology," *Microelectronics Journal* (Elsevier), 90 (2019) 267-277, https://doi.org/10.1016/j.mejo.2019.05.010

j149 S. Nikbakht and N. Bagherzadeh, "Divisible load scheduling of image processing applications on the heterogeneous star and tree networks using a new genetic algorithm," *Concurrency and Computation Practice and Experience* (Wiley), (2019), https://doi.org/10.1002/cpe.5498

j150 P. Sadri, M. Wahiduzzaman, S. Isklam, I. Krivorotov, M. Nilsson, N. Bagherzadeh, and O. Boyraz, "Array of Symmetric Nanohole Dimers with High Sensitivity for Detection of Changes in an STT-RAM Ultrathin Dielectric Layer," *Journal of the Optical Society of America B*, Vol. 36 No. 11, (2019), https://doi.org/10.1364/JOSAB.36.003090

j151 M. Moghadam, E. Masoumi, N. Bagherzadeh, D. Ramsingh, G.P. Li, and Z. Kain, "A Machine-Learning Approach to Predicting Hypotensive Events in ICU Settings," *Computers in Biology and Medicine*, https://doi.org/10.1016/j.compbiomed.2020.103626, 2020.

j152 H. Zhao, N. Bagherzadeh, Q. Wang, and Y. Wang, "A Fine-Grained Source-Throttling Method for Mesh Architectures," *IEEE Access*, *Special Section on Artificial Intelligence in Parallel and Distributed Computing*, Volume 8, 2020, Digital Object Identifier 10.1109/ACCESS.2020.2967459

j153 A. Albaqsami, M. Hosseini, M. Jasemi, and N. Bagherzadeh, "Adaptive HTF-MPR: An Adaptive Heterogeneous TensorFlow Mapper Utilizing Bayesian Optimization and Genetic Algorithms," *ACM Trans. Intell. Syst. Technol*.,11, 5, Article 55 (August 2020), https://doi.org/10.1145/3396949

j154 A. Bozorgmehr, M. Khaleqi, M. Moaiyeri, K. Navi, and N. Bagherzadeh, "A high-performance fully programmable membership function generator based on 10 nm gate-all-around CNTFETs," *International Journal of Electronics and Communications*, https://doi.org/10.1016/j.aeue.2020.153293

j155 E. Montoya, J. Chen, R. Ngelale, H. Lee, H. Tseng, L. Wan, E. Yang, P. Braganca, O. Boyraz, N. Bagherzadeh, M. Nilsson, and I. Krivorotov, "Immunity of Nanoscale Magnetic Tunnel Junctions with Perpendicular Magnetic Anisotropy to Ionizing Radiation," *Scientific Reports (Natureresearch)*, https://doi.org/10.1038/s41598-020-67257-2, (2020)

j156 M. Jasemi, S. Hessabi, and N. Bagherzadeh, "Reliable and Energy Efficient MLC STT-RAM Buffer for CNN Accelerators," *Computers and Electrical Engineering*, https://doi.org/10.1016/j.compeleceng.2020.106698

j157 J. Talafy, F. Zokaee, H. Zarandi, and N. Bagherzadeh, "A High Performance Multi-Bit Output Logic-in-Memory Adder," *IEEE Transactions on Emerging Topics in Computing*, DOI 10.1109/TETC.2020.2982951,

j158 P. Sadri, M. Wahiduzzaman, M. Shafiqul Islam, E. Montoya, I. Krivorotov, N. Bagherzadeh, and O. Boyraz, "Effect of Magnesium Oxide Adhesion Layer on Resonance Behavior of Plasmonic Nanostructures," *Applied Physics Letters*, 116, 241601 (2020); https://doi.org/10.1063/5.0008665

j159 Z. Ren, A. Alqahtani, N. Bagherzadeh, and J. Lee, "Thermal TSV Optimization and Hierarchical
Floorplanning for 3D Integrated Circuits," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, https://doi.org/10.1109/TCPMT.2020.2970382, Volume: 10, Issue: 4, April 2020

j160 A. Bozorgmehr, M. Khaleqi, M. Moaiyeri, K. Navi, and N. Bagherzadeh, "A Novel Digital Fuzzy System for Image Edge Detection Based on Wrap-Gate Carbon Nanotube Transistors," *Computers and Electrical Engineering*, 87 (2020) 106811, https://doi.org/10.1016/j.compeleceng.2020.106811

j161 M. Jasemi, S. Hessabi, and N. Bagherzadeh, "Enhancing Reliability of Emerging Memory Technology for Machine Learning Accelerators," *IEEE Transactions on Emerging Topics in Computing*, DOI 10.1109/TETC.2020.2984992, (2020).

j162 S. Hosseini, M. Reshadi, and Nader Bagherzadeh, "Flow Mapping on Mesh-Based Deep Learning Accelerator, "*Journal of Parallel Distributed Computing*," 144 (2020) 80-97, https://doi.org/10.1016/j.jpdc.2020.04.011

j163 A. Tajari, H. Zarandi, and N. Bagherzadeh, "IRHT: An SDC Detection and Recovery Architecture Based on Value Locality of Instruction Binary Codes," ***Microprocessors and Microsystems***
Volume 77, September 2020, 103159, https://doi.org/10.1016/j.micpro.2020.103159

j164 S. Hosseini, M. Reshadi, N. Bagherzadeh, and A. Khademzadeh, "Data Scheduling and Placement in Deep Learning Accelerator," *Cluster Computing*, https://doi.org/10.1007/s10586-021-03355-8, (2021)

j165 M. Kim, A. Del Barrio, H. Kim, and N. Bagherzadeh, "The Effects of Approximate Multiplication on Convolutional Neural Networks," *IEEE Transactions on Emerging Topics in Computing*, Digital Object Identifier 10.1109/TETC.2021.3050989, (2021)

j166 M. Taheri, N. Shafiee, F. Sharifi, M. Moaiyeri, K. Navi, and N. Bagherzadeh, "Energy Efficient Hybrid Full Adder Design for Digital Signal Processing in Nanoelectronics," *Analog Integrated Circuits and Signal Processing*, (2021), https://doi.org/10.1007/s10470-021-01831-0

j167 R. Murillo, A. Del Barrio, G. Botella, M. S. Kim, H. Kim, and N. Bagherzadeh, "PLAM: A Posit Logarithm-Approximate Multiplier," *IEEE Transactions on Emerging Topics in Computing*, Digital Object Identifier, DOI 10.1109/TETC.2021.3109127, (2021)

j168 M. Hosseini, M. Ebrahimi, P. Yaghini, and N. Bagherzadeh, "Near Volatile and Non-Volatile Memory Processing in 3D Systems," *IEEE Transactions on Emerging Topics in Computing*, Digital Object Identifier, https://doi.org/10.1109/TETC.2021.3115495, (2021)

j169 S. Nabiee, M. Harding, J. Hersh, and N. Bagherzadeh, "Hybrid U-Net: Semantic Segmentation of High-resolution Satellite Images to Detect War Destruction," *Machine Learning with Applications*, https://doi.org/10.1016/j.mlwa.2022.100381, (2022)

j170 H. Kim, M. Alnemari, and N. Bagherzadeh, "A Storage-Efficient Ensemble Classification Using Filter Sharing on Binarized Convolutional Neural Networks," *PeerJ Computer Science*. (2022), Vol. 8. http://dx.doi.org/10.7717/peerj-cs.924

j171 A. Ding, Y. Qiao, and N. Bagherzadeh, "BNN an Ideal Architecture for Acceleration with Resistive in Memory Computation," *IEEE Transactions on Emerging Topics in Computing*, DOI 10.1109/TETC.2023.3237778, (2023)

j172 M. Moghadam, E. Masoumi, S. Kendale, and N. Bagherzadeh, "Predicting hypotensive events in the ICU settings using patient's short-term physiological history and contextual data," *Computer Methods and Programs in Biomedicine* (2023) https://doi.org/10.1016/j.cmpbup.2023.100100

Journals (other)

jo1 F. Mehdipour and N. Bagherzadeh, "New memory technology supports parallel processing," *Defense Electronics*, pp. 54-58, November 1990.

jo2 S. Shoari, A. Kavianpour, and N. Bagherzadeh, "Pyramid simulation of image processing Applications, "*Image and Vision Computing*, Vol. 12, No. 8, pp. 523-529, October 1994.

jo3 F. Kurdahi, N. Bagherzadeh, P. Athanas, and J. Muniz, "Guest Editors' Introduction: Configurable Computing*," IEEE Design and Test of Computers: Special Issue on Configurable Computing*, March/April 2000.

jo4 N. Bagherzadeh, "Guest Editor for Special Issue: Reconfigurable and Scalable High Performance Architectures*,*" *International Journal of High Performance Systems Architecture*, Vol. 1, No. 2, 2007.

jo5 H. Sarbazi-Azad and N. Bagherzadeh: Editorial notes: Special Issue on On-Chip Parallel and Network-Based Systems. *Microprocessors and Microsystems* - Embedded Hardware Design 36(7): 529-530 (2012)

jo6 H. Sarbazi-Azad and N. Bagherzadeh: Multicore Computing Systems: Architecture, Programming Tools, and Applications, *Journal of Computer and Systems Sciences*, 79(4): 403-405 (2013)

Patents

p1 A. Eghbal, P. Yaghini, and N. Bagherzadeh, "Three-Dimensional NoC Reliability Evaluation," US 11,093,673 B2, Date of Patent: August 17, 2021

Book Chapters

b1 D. Blough and N. Bagherzadeh, "An efficient fault-tolerant routing algorithm for hypercube systems," *Advances in Parallel Computing*, Vol. 2, New York: North-Holland Press, 1989.

b2 M. Villa-Uriol, F. Kuester, N. Bagherzadeh, A. Perez, and J. M. McCarthy, "Chapter on Humanoids and Biomedical Applications, Kinematics Synthesis of Avatar Skeletons from Visual Data," *On Advances in Robot Kinematics*, Kluwer Academic Publishers, Sestri Levante, Italy, pp. 171-180, 2004.

b3 M. Sanchez-Elez, M. Fernandez, N. Bagherzadeh, R. Hermida, F. Kurdahi, and R Maestre, "A Coarse-Grain Dynamically Reconfigurable System and Compilation Framework," *Vassliadis and Soudris, Eds.,* pp. 181-215, Springer, 2007.

b4 S. Lee and N. Bagherzadeh, "Chapter 9: Energy/Power Issues in Network-on-Chip," *Network-on-Chips: Theory and Practice, CRC Press,* 2009*,* ISBN: 9781420079784.

b5 F. Hosseinzadeh, N. Bagherzadeh, A. Khademzadeh and M. Janidarmian, " Fault-Tolerant Optimization for Application-Specific Network-on-Chip Architecture," *IAENG Transactions on Engineering Technologies, Lecture Notes in Electrical Engineering (Springer),* Chapter 26, pp. 363-381, 2014.

b6 F. Bolanos, F. Rivera, J. Aedo, and N. Bagherzadeh, "Task Mapping in Heterogeneous NoC by Means of Population-Based Incremental Learning," *Advances in Intelligent Systems: Reviews, Book Series, Vol. 1,* 2017

b7 B. Barhami, M. Jamali, N. Bagherzadeh, and G. Morales, "Wireless Network-on-Chip Architecture A Comprehensive Review," *Horizons in Computer Science Research, Nova Science Publishers, Inc.*, Volume 16, 2018.

Conferences Refereed

c1 M. Lee, J. Fiene, C. Wu, N. Bagherzadeh, and G. Brown, "Network facility for a reconfigurable computer architecture," *Proceedings of 1985 Distributed Computing Symposium*, pp. 264-271, 1985.

c2 C. Wu, M. Lee, C. Sudtikitpisan, J. Moaddeb, G. Brown, W. Lin, N. Bagherzadeh, and D. Vaughn, "Prototype of star architecture; a status report," *AFIPS Proceedings, NCC*, pp. 191-201, 1985.

c3 N. Bagherzadeh, K. Tseng and C. Wu, "Erratic non-uniform traffic behavior of a multiple minicomputer network," *Proceedings of the International Symposium Mini and Microcomputer and Their Applications*, pp. 39-42, November 1986.

c4 N. Bagherzadeh and C. Wu, "Distributed synchronous garbage collection using broadcasting," *Proceedings of the 20th Hawaii International Conference on System Sciences*, pp. 362-369, January 1987.

c5 N. Bagherzadeh and C. Wu, "Annotations for parallelism," *Proceedings of the 6th Phoenix Conference on Computers and Communications*, pp. 346-350, February 1987.

c6 N. Bagherzadeh, T. Kerola, W. Leddy, and R. Brice, "On parallel execution of the traveling salesman problem on a neural network model," *First International Conference on Neural Networks*, San Diego, California, pp. 317-324, June 21-24, 1987.

c7 N. Bagherzadeh, B. Kandu, S. Heng, and C. Wu, "Network simulation of a synchronous garbage collection algorithm," *Symposium on the Simulation of Computer Networks,* Colorado Springs, Colorado, pp. 215-222, August 1987.

c8 A. Guzman, E. Krall, P. McGehearty, and N. Bagherzadeh, "Effects of Applications on the performance of a parallel architecture," *HICSS-21,* January 1988.

c9 Y. Moon, N. Bagherzadeh, and J. Sklansky, "Assignment of tasks to multiple processors for image processing, "*Pattern Recognition for Advanced Missile System Conference*, Huntsville, Alabama, November 1988.

c10 Y. Moon, N. Bagherzadeh, and J. Sklansky, "Macropipelined multicomputer systems for image analysis," *SPIE OE/LASE '89 Conference on High Speed Computing II*, Los Angeles, California, January 1989.

c11 D. Blough, N. Bagherzadeh, and R. Sehgal, "A new fault-tolerant routing algorithm for hypercube systems," *Proceedings of the Third Annual Parallel Processing Symposium*, pp. 130-137, March 1989.

c12 N. Nassif and N. Bagherzadeh, "A new method for distributed termination detection," *Proceedings of the Third Annual Parallel Processing Symposium*, pp. 300-310, March 1989.

c13 D. Blough and N. Bagherzadeh, "A new fault-tolerant routing algorithm for hypercube systems," *International Workshop on Hardware Fault Tolerance in Multiprocessors,* University of Illinois, pp. 52-54, June 1989.

c14 A. Mendez, N. Bagherzadeh, and F. Mehdipour, "Three dimensional mass memory compatible with parallel processing architectures," *Proceedings of the Fourth Annual Parallel Processing Symposium*, Fullerton, California, pp. 34-42, April 1990.

c15 K. Tsai, K. Kim, and N. Bagherzadeh, "A hierarchical mesh architecture," *Proceedings of the Fourth Annual Parallel Processing Symposium*, Fullerton, California, pp. 459-477, April 1990.

c16 A. Kavianpour and N. Bagherzadeh, "A three coloring algorithm for distributed termination detection of non-FIFO distributed systems," *Proceedings of the Fourth Annual Parallel Processing Symposium*, Fullerton, California, pp. 708-718, April 1990.

c17 N. Bagherzadeh, "Broadcasting on faulty hypercubes," *Proceedings of the Fourth Annual Parallel Processing Symposium*, Fullerton, California, pp. 730-732, April 1990.

c18 A. Abnous and N. Bagherzadeh, "Special features of a VLIW architecture," *Proceedings of the Fifth Annual Parallel Processing Symposium*, Fullerton, California, pp. 224-227, 1991.

c19 A. Kavianpour and N. Bagherzadeh, "Parallel Hough Transform for image processing on a pyramid architecture," *Proceedings of the International Conference on Parallel Processing*, pp. 395-398, August 1991.

c20 A. Abnous, R. Potasman, N. Bagherzadeh, and A. Nicolau, "A percolation based VLIW architecture," *Proceedings of the International Conference on Parallel Processing*, pp. 144-148, August 1991.

c21 K. Tsai, Y. Kim, and N. Bagherzadeh, "Hypermesh: a combined quad tree and mesh network for parallel processing," *Proceedings of the International Conference on Parallel Processing*, pp. 696-697, August 1991.

c22 N. Bagherzadeh and K. Hawk, "Parallel implementation of the auction algorithm on the Intel Hypercube," *Proceedings of the Sixth Annual Parallel Processing Symposium*, pp. 443-447, March 1992.

c23 A. Abnous, C. Christensen, J. Gray, J. Lenell, A. Naylor and N. Bagherzadeh, "VLSI design of the Tiny RISC microprocessor," *Proceedings of the Custom Integrated Circuits Conference*, pp. 30.4.1-5, May 1992.

c24 A. Abnous and N. Bagherzadeh, "Pipelining and bypassing in a VLIW processor," *Proceedings of the International Symposium on Computer Architecture*, p. 434, May 1992.

c25 S. Latifi, S. Zheng, and N. Bagherzadeh, "Optimal ring embedding in hypercubes with faulty links," *Proceedings of the International Fault-Tolerant Computing Symposium*, pp. 178-184, July 1992.

c26 T. Kato, K. Suginuma, and N. Bagherzadeh, "On design and performance analysis of a superscalar architecture," *Proceedings of the International Conference on Parallel Processing*, August 1992.

c27 J. Lenell, S. Wallace and N. Bagherzadeh, "A 20MHz CMOS Reorder Buffer for a Superscalar Microprocessor," *Proceedings of the NASA VLSI Conference*, 1992.

c28 T. Kato, T. Ono and N. Bagherzadeh, "Performance Analysis and Design Methodology for a Scalable Superscalar Architecture," *Proceedings of the MICRO-25 Conference*, Portland, Oregon, 1992.

c29 T. Kato, T. Ono and N. Bagherzadeh, "A Novel Superscalar Architecture with Predetermined Scheduling Patterns," *Proceedings of the International Conference on Parallel and Distributed Systems*, Taiwan, 1992.

c30 T. Kato, T. Ono and N. Bagherzadeh, "Data Cache Architecture of the Superscalar by Scheduling Patterns," *HICSS'2*6, 1993.

c31 J. Gray, A. Naylor, A. Abnous and N. Bagherzadeh, "VIPER: A 25-MHz, 100-MIPS Peak VLIW Microprocessor," *Proceedings of the Custom Integrated Circuits Conference*, 1993.

c32 S. Latifi, M. de Azevedo and N. Bagherzadeh, "The Star Connected Cycles: A Fixed-Degree Network for Parallel Processing," *International Conference on Parallel Processing*, St. Charles, IL, August 1993.

c33 A. Fijany, G. Kwan, and N. Bagherzadeh, "A fast algorithm for parallel computation of multibody dynamics on MIMD parallel architectures," *Proceedings of Computing in Aerospace 9 AIAA,* San Diego, California, October 1993.

c34 S. Shoari, A. Kavianpour, and N. Bagherzadeh, "Pyramid simulation of image processing Applications, " *Proceedings of Computing in Aerospace 9 AIAA,* San Diego, California, October 1993.

c35 A. Kavianpour, N. Bagherzadeh, and S. Shoari, "Finding elliptical shapes in an image using a pyramid architecture, "*International Symposium on Speech, Image Processing, and Neural Networks,* Hong Kong, 1994.

c36 M. M. de Azevedo, S. Latifi, and N. Bagherzadeh, "On packing and embedding hypercubes into star graphs," *Proceedings of the VI Brazilian Symposium on Computer Architecture and High Performance Computing (VI SBAC-PAD)*, Caxambu, Minas Gerais, Brazil, August 1-5, pp. 3-19, (1994).

c37 M. M. de Azevedo, N. Bagherzadeh, and S. Latifi, "Fault-diameter of the star-connected cycles interconnection network," *Proceedings of the 28th Annual Hawaii*

International Conference on System Sciences (HICSS-28), Vol. II (Software technology), Maui, Hawaii, January 3-6, pp. 469-478, 1995.

c38 M. M. de Azevedo, N. Bagherzadeh, and S. Latifi, "Embedding meshes in the star-connected cycles interconnection network," *10th International Conference on mathematical and computer modeling and Scientific Computing* Boston, July 5-8 (1995).

c39 S. Wallace, N. Dagli, and N. Bagherzadeh, "Design and implementation of a 100 Mhz Reorder Buffer," *37th Midwest Symposium on Circuits and Systems,* 1994.

c40 M. M. de Azevedo, S. Latifi, and N. Bagherzadeh "Low expansion packings and embeddings of hypercubes into star graphs," *Proceedings of the IEEE 15th Annual International Phoenix Conference on Computers and Communications*, Phoenix, March 27-29, pp. 115-122 (1996).

c41 M. M. de Azevedo, N. Bagherzadeh, and S. Latifi, "Variable-dilation embeddings of hypercubes into star graphs: performance metrics, mapping functions, and routing," *Euro-Par,* Lyon, France, 1996.

c42 N. Nassif and N. Bagherzadeh, "Image analysis solutions and grid embedding on the star," *Proceedings of the 1996 SCS Simulation Multiconference*, New Orleans, April 8-11, pp. 396-402 (1996).

c43 M. Gulati and N. Bagherzadeh, "Performance study of a multithreaded superscalar microprocessor," *Proceedings of the Second International Symposium on High-Performance Computer Architecture*, San Jose (California), February, pp. 291-301 (1996).

c44 S. Wallace and N. Bagherzadeh, "Instruction fetching mechanism for superscalar microprocessors," *Euro-Par,* Lyon, France, 1996.

c45 S. Wallace and N. Bagherzadeh, "A scalable register file architecture for dynamically scheduled processors," *PACT,* Boston, 1996.

c46 M. Loikkanen and N. Bagherzadeh, "A fine-grain multithreading superscalar architecture," *PACT,* Boston, 1996.

c47 K. Suginuma and Nader Bagherzadeh, "Z-cache, a new cache mechanism for computer graphics," *Proceedings of MTAC '97*.

c48 S. Wallace and Nader Bagherzadeh, "Multiple branch and block prediction," *Proceedings of HPCA-3*, pp. 94-103 (1997).

c49 S. Shoari, N. Bagherzadeh, D. Goodman, T. E. Milner, D. J. Smithies, and J. S. Nelson, "Parallel algorithm for pulsed laser infrared tomography," *Proceedings of the 7th Annual Meeting of the American Society for Laser Medicine and Surgery*, (1997)

c50 S. Latifi and N. Bagherzadeh, "Incomplete star graph: an alternative interconnection network for massively parallel systems," *Proceedings of the 26th Hawaii International Conference on System Science*, Vol. II, pp. 660-667, Jan 1993.

c51 S. Latifi and N. Bagherzadeh, "The clustered-star graph: a new topology for large interconnection networks," *7th International Parallel Processing Symposium*, pp. 514-518, April 1993.

c52 J. Lenell and N. Bagherzadeh, "A performance comparison of several superscalar processor models with a VLIW processor," *7th International Parallel Processing Symposium*, pp. 44-48, April 1993.

c53 N. Bagherzadeh, N. Nassif, and S. Latifi, "A routing scheme on faulty star graphs," *Pacific Rim International Symposium on Fault Tolerant Computing,* pp. 214-218, Australia, December 1993.

c54 S. Wallace, N. Dagli, and N. Bagherzadeh, "Design and implementation of a 100 MHz centralized instruction window for a superscalar microprocessor," *Proceedings of the IEEE International Conference on Computer Design: VLSI in Computers and Processors,* pp. 96-101, Austin, October 1994.

c55 S. Latifi and N. Bagherzadeh, "Hamiltonicity of the clustered-star graph with embedding Applications," *PDPTA '96 International*, pp. 734-744.

c56 H. Liu, F Etemadi, G. Lu, N. Bagherzadeh, and F. Kurdahi "Implementation of an all-digital CAP transceiver," *Proceedings of the International Conference on Computer Simulation,* Sept 1-4, Lebanon, 1997.

c57 H. Singh, M. Lee, G. Lu, F. Kurdahi, N. Bagherzadeh, T. Lang, R. Heaton, and F. Filho "Morphosys: An Integrated Re-Configurable Architecture," *Proceedings of the NATO Symposium on System Concepts and Integration*, Monterey, CA, April 1998.

c58 R. Maestre, F. J. Kurdahi, N. Bagherzadeh, H. Singh, R. Hermida, and M. Fernandez, "Kernel Scheduling in Reconfigurable Computing," *Proceedings of DATE*, pp. 90-96, Munich, March 1999.

c59 G. Lu, M. Lee, M. Singh, N. Bagherzadeh, F. Kurdahi and E. Filho, "MorphoSys: A Reconfigurable Processor Targeted for High-Performance Image Applications," *Proceedings of the Reconfigurable Architecture Workshop at the 11th IPP.S/SPDP'99*, pp. 661-9, Puerto Rico, April 1999.

c60 G. Lu, H. Singh, M. Lee, N. Bagherzadeh, F. Kurdahi, E. Filho, and V. Castro Alves, "MorphoSys Dynamically Reconfigurable System-on-chip," *Proceedings of the First NASA/DOD Workshop on Evolvable Hardware, EH 99*, pp. 152-160, Pasadena, California, July 1999.

c61 G. Lu, H. Singh, M. Lee, N. Bagherzadeh, F. Kurdahi and E. Filho, "The Morphosys Parallel Reconfigurable Syste," *Proceedings of the EURO-PAR 99*, pp. 727-734, 1999, Toulouse, France.

c62 R. Maestre, M. Fernandez, R. Hermida, and N. Bagherzadeh, "A Framework for Scheduling and Context Allocation in Reconfigurable Computing*," Proceedings of the International Symposium on System Synthesis*, pp. 134-140, San Jose, California, November 1999.

c63 R. Maestre, F. J. Kurdahi, M. Fernandez, R. Hermida, N. Bagherzadeh, and H. Singh, "Optimal vs. Heuristic Approaches to Context Scheduling for Multi-Context Reconfigurable Architectures," *Proceedings of the International Symposium on Field-Programmable Custom Computing Machines*, Napa, California, April 2000.

c64 R. Maestre, F. J. Kurdahi, M. Fernandez, N. Bagherzadeh, and H. Singh, "Configuration Management in Multi-Context Reconfigurable Systems for Simultaneous Performance and Power Optimizations," *Proceedings of the International Symposium on System Synthesis*, Madrid, Spain, Nov. 2000.

c65 H. Singh, M. Lee, G. Lu, F. Kurdahi, N. Bagherzadeh, E. Filho, and Rafael Maestre, "MorphoSys: A Case Study of A Reconfigurable System for Multimedia Applications," *Proceedings of Design Automation Conference (DAC 2000)*, Los Angeles, California, June 2000.

c66 R. Maestre, M. Fernandez, R. Hermida, F. Kurdahi, N. Bagherzadeh, and H. Singh, "Analysis and Evaluation of Context Scheduling Heuristics for Multi-Context Reconfigurable Architectures," *Proceedings of ICCD 2000*.

c67 H. Singh, M. Lee, G. Lu, F. Kurdahi, N. Bagherzadeh, and E. Filho, "MorphoSys: A Reconfigurable Architecture for Multimedia Applications," *Workshop on Reconfigurable Computing at the International Conference on Parallel Architectures and Compilations, PACT '98*.

c68 J. Liu, P. Chou, N. Bagherzadeh, and F. Kurdahi, "Power-Aware Scheduling under Timing Constraints for Mission-Critical Embedded Systems," in *Proc. 38th Design Automation Conference*, Las Vegas, NV, June 2001. pp. 840-845.

c69 J. Liu, P. Chou, N. Bagherzadeh, and F. Kurdahi, "A Constraint-based Application Model and Scheduling Techniques for Power-aware Systems", in, *Proc. International Symposium on Hardware/Software Codesign*, Copenhagen, Denmark, April 2001. pp. 153-158.

c70 M. Ahamed, H. Eldeeb, S. Nassar, and N. Bagherzadeh, "Design and Implementation of Automatic Parallel Detection Layer," *IEEE Conference on Systems, Man, and Cybernetics*, October 2001, pp. 2371-2376.

c71 G. Venkataramani, W. Najjar, F. Kurdahi, N. Bagherzadeh, W. Böhm, "A compiler framework for Mapping Applications to a coarse-grained reconfigurable computer architecture," *CASES 2001*, pp. 116-125.

c72 M. Sanchez-Elez, M. Fernandez, R. Hermida, R. Maestre, F. Kurdahi, and N. Bagherzadeh, "A Data Scheduler for Multi-Context Reconfigurable Architectures," *14th International Symposium on System Synthesis*, October 2001, pp. 177-182.

c73 D. Li, P. Chou, and N. Bagherzadeh, "Mode Selection and Mode-Dependency Modeling for Power-Aware Embedded Systems," in *Proc. 7th Asia South Pacific Design Automation Conference* (ASPDAC'02), January 2002. pp. 697-704. Best Student Paper Award.

c74 J. Liu, P. Chou and N. Bagherzadeh, "Communication Speed Selection for Embedded Systems with Networked Voltage-Scalable Processors*," Proceedings of the 10th International Symposium on Hardware/Software Codesign (CODES'02)*, Estes Park, CO, May 2002. pp. 169-174.

c75 J. Liu, P. Chou and N. Bagherzadeh, "Combined Functional Partitioning and Communication Speed Selection for Networked Voltage-Scalable Processors," in *Proceedings of the International Symposium on System Synthesis*, October 2002. pp. 14-19.

c76 M. Sainz, N. Bagherzadeh and A. Susin, "Carving 3D Models from Uncalibrated Views," *5th IASTED International Conference Computer Graphics and Imaging (CGIM 2002),* August 12-14, 2002 Kauai, Hawaii, USA. pp. 144-149.

c77 S. Latifi S, S.Q. Zheng, and N. Bagherzadeh, "Hamiltonian Path and Cycle in Hypercubes with Faulty Links," *Proceedings Fifth International Conference on Algorithms and Architectures for Parallel Processing. IEEE Comput. Soc*. 2002, pp. 471-8. Los Alamitos, CA, USA.

c78 M. Sainz, N. Bagherzadeh and A. Susin, "Hardware Accelerated Voxel Carving," *1st Ibero-American Symposium in Computer Graphics (SIACG 2002),* July 2-5, 2002 Guimarães, Portugal. pp. 289-297.

c79 H. Parizi, A. Niktash, N. Bagherzadeh, and F. Kurdahi, "MorphoSys: A Coarse Grain Reconfigurable Architecture for Multimedia Applications," *Euro-Par 2002 Parallel Processing. 8th International Euro-Par Conference. Proceedings (Lecture Notes in Computer Science Vol.2400*). Springer-Verlag. 2002, pp. 844-8, Berlin, Germany.

c80 A. Paar, M. Anido, and N. Bagherzadeh, "A Novel Predication Scheme for a SIMD System-on-chip," *Euro-Par 2002 Parallel Processing. 8th International Euro-Par Conference. Proceedings (Lecture Notes in Computer Science Vol.2400).* Springer-Verlag. 2002, pp. 834-43. Berlin, Germany.

c81 M. Anido, N. Tabrizi, H. Du, M. Sanchez-Elez, and N. Bagherzadeh, "Interactive Ray Tracing Using a SIMD Reconfigurable Architecture," *Proceedings 14th Symposium on Computer Architecture and High Performance Computing. IEEE Computer. Soc.*2002, pp.20-28. Brazil.

c82 M. Anido, A. Paar, and N. Bagherzadeh, "A Novel Method for Improving the Operation Autonomy of SIMD Processing Elements," *Proceedings 15th Symposium on Integrated Circuits and Systems Design. IEEE Comput. Soc. 2002,* pp.49-54, Los Alamitos, CA, USA.

c83 M. Sainz, N. Bagherzadeh and A. Susin, "Recovering 3D Metric Structure and Motion from Multiple Uncalibrated Cameras," *Proceedings of International Conference on Information Technology: Coding and Computing,* pp. 268-273, April 2002.

c84 M. Sanchez-Elez, M. Fernandez, R. Maestre, R. Hermida, N. Bagherzadeh, and F. Kurdahi, "A Complete Data Scheduler for Multi-Context Reconfigurable Architectures," *Design, Automation and Test in Europe Conference and Exhibition,(DATE)* 2002, 4-8 March 2002, pp. 547-552.

c85 M. Anido, A. Paar, and N. Bagherzadeh, "Improving the Operation Autonomy of SIMD Processing Elements by Using Guarded Instructions and Pseudo Branches," *Digital System Design, 2002. Proceedings. Euromicro Symposium on,* 4-6 Sept. 2002, pp. 148-155.

c86 C. Pan, N. Bagherzadeh, A. H. Kamalizad, and A. Koohi, "Design and Analysis of a Programmable Single-chip Architecture for DVB-T Base-band Receiver," *Design, Automation and Test in Europe Conference and Exhibition, (DATE),2003*, March 3-7, 2003, pp. 468 -473.

c87 H. Du, M. Sanchez-Elez, N. Tabrizi, N. Bagherzadeh, M. Anido, and M. Fernandez, "Interactive Ray Tracing on Reconfigurable SIMD MorphoSys," *Design Automation and Test in Europe Conference and Exhibition, 2003*, March 3-7, 2003, pp. 144-149.

c88 M. Sanchez-Elez, M. Fernandez, M. Anido, H. Du, N. Bagherzadeh, R. Hermida, "Low Energy Data Management for Different On-chip Memory Levels in Multi-Context Reconfigurable Architectures," *Design, Automation and Test in Europe Conference and Exhibition*, (DATE) 2003, March 3-7, 2003, pp. 36-41.

c89 H. Du, M. Sanchez-Elez, N. Tabrizi, N. Bagherzadeh, M. Anido, and M. Fernandez, "Interactive Ray Tracing on Reconfigurable SIMD MorphoSys," *Proceedings of the*

ASP-DAC 2003. Asia and South Pacific Design Automation Conference 2003 (Cat. No.03EX627), IEEE. 2003, pp. 471-6. Piscataway, NJ, USA.

c90 M. Sainz, A. Susin, A. Cervantes, and N. Bagherzadeh, "Persepolis: Recovering History with a Handheld Camera," *Eurographics* 2003 (EG'03).

c91 M. Sainz, A. Susin, and N. Bagherzadeh, "MTMesh: Image Based Mesh Reconstruction and Rendering," *In Proceedings of the IAESTED Conference in Visualization, Imaging and Image Processing (VIIP'03)*, 2003.

c92 Sainz, A. Susin, and N. Bagherzadeh, "Camera Calibration of Long Image Sequences with the Presence of Occlusions," *Proceeding of the International Conference in Image Processing 2003 (ICIP'03),* Barcelona.

c93 Li, P. Chou and N. Bagherzadeh, "Topology Selection for Energy Minimization in Embedded Networks," in *Proc. Asia South-Pacific Design Automation Conference* (ASPDAC'03), Kitakyushu, Japan, January 2003. pp. 693-696.

c94 Villa-Uriol, M. Sainz, F. Kuester, and N. Bagherzadeh, "Automatic creation of three-dimensional avatars," *Proceedings of SPIE-IS&T Electronic Imaging*, SPIE Vol. 5013 (2003), January 21-22, 2003 Santa Clara, California, USA. pp. 14-25.

c95 H. Du, M. Sanchez-Elez, N. Tabrizi, and N. Bagherzadeh, M. Fernandez, "MorphoSys: a Reconfigurable Architecture Optimized for Ray Tracing," *Cool-Chips VI*, 2003, April 16-18, Yokohama, Japan.

c96 A. Paar, H. Du, and N. Bagherzadeh, "A Component Oriented Simulator for HW/SW Co-Designs, *First Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia)in conjunction with IEEE/ACM CODES-ISSS 2003 Conference*, Newport Beach, CA.

c97 A. Koohi, N. Bagherzadeh, and Chengzhi Pan, "A Fast Parallel-Solomon Decoder on a Reconfigurable Architecture," *IEEE/ACM CODES-ISSS 2003 Conference*, Newport Beach, CA.

c98 M. Villa-Uriol, A. Perez, F. Kuester, and N. Bagherzadeh, "Image-Based Avatar Reconstruction," *Proceedings of the NSF Lake Tahoe Workshop on Collaborative Virtual Reality and Visualization*, (2003).

c99 A. H. Kamalizad, C. Pan, and N. Bagherzadeh, "Fast Parallel FFT on a Reconfigurable Computation Platform," *Proceedings of the 15th Symposium on Computer Architecture and High Performance Computing*, 10-12 November 2003, pp. 254-259.

c100 M. Villa-Uriol, G. Chaudhary, F. Kuester, T.C. Hutchinson, and N. Bagherzadeh, "Extracting 3D from 2D: Selection Basis for Camera Calibration," *Proceedings of the*

7th IASTED International Conference on Computer Graphics and Imaging (CGIM 2004), pp. 315-321.

c101 N. Tabrizi, N. Bagherzadeh, A. Kamalizad, and H. Du, "MaRS: A Macro-Pipelined Reconfigurable System," *Computing Frontiers (CF'04),* April 14-16, Ischia, Italy, pp. 343-349.

c102 B. Gorji-Ara, P. Chou, N. Bagherzadeh, M. Reshadi, and D. Jensen, "Fast and Efficient Voltage Scheduling by Evolutionary Slack Distribution," *Proceedings of the ASP-DAC 2004,* Jan. 2004, pp. 659-662.

c103 B. Gorji-Ara, N. Bagherzadeh, and P. Chou, "An Efficient Voltage Scaling Algorithm for Complex SoCs with few Number of Voltage Modes," *Proceedings of the 2004 International Symposium on Low Power Electronics and Design (ISLPED 2004)*, August 9-11, 2004, pp. 381-386.

c104 F. Rivera, M. Sanchez-Elez, M. Fernandez, R. Hermida, and N. Bagherzadeh, "Efficient Mapping of Hierarchical Trees on Coarse-Grain Reconfigurable Architectures," *Proceedings of CODES+ISSS 2004*, 8-10 September 2004, pp. 30-35.

c105 A. Kamalizad, R. Plettner, C. Pan, and N. Bagherzadeh, "Fast Parallel Soft Viterbi Decoder Mapping on a Reconfigurable DSP Platform," *IEEE International SOC Conference*, 12-15 September, 2004, pp. 3-6.

c106 J. Hahn, D. Li, Q. Xie, P. Chou, N. Bagherzadeh, D. Jensen, and A. Tribble, "Power Reduction in JTRS Radios with ImpacctPro," *IEEE Military Communications Conference* (*MILCOM 2004),* 31 Oct. - 03 Nov. 2004, pp. 204-210.

c107 F. Rivera, M. Sanchez-Elez, M. Fernandez, R. Hermida, and N. Bagherzadeh, "Low Power Data Prefetch for 3D Image Applications on Coarse-Grain Reconfigurable Architectures," *Proceedings of the 19th IEEE International Parallel and Distributed Processing Symposium (2005)*, 04-08 April 2005, pp. 171b-171b.

c108 A. Kamalizad, N. Tabrizi, N. Bagherzadeh, and A. Hatanaka, "A Programmable DSP Architecture for Wireless Communication Systems," *16th IEEE International Conference on Application-Specific Systems, Architecture Processors (ASAP 2005)*, 23-25 July 2005, pp. 231-238.

c109 F. Rivera, M. Sanchez-Elez, M. Fernandez, and N. Bagherzadeh, "An Approach to execute Conditional Branches onto SIMD Multi-Context Reconfigurable Architectures," *Proceedings of the 8th Euromicro Conference on Digital System Design*, 30 Aug - 03 September, 2005, pp. 396-402.

c110 N. Tabrizi and N. Bagherzadeh, "An ASIC Design of a Novel Pipelined and Parallel Sorting Accelerator for a Multiprocessor-on-a-chip," *Proceedings of the 6th International Conference on ASIC (ASICON 2005),* 24-27 Oct-20 Oct 2005, pp. 46-49.

c111 A. Niktash. R. Masetre, and N. Bagherzadeh, "A Case Study of Performing OFDM Kernels on a Novel Reconfigurable DSP Architecture," *IEEE Military Communications Conference (MILCOM 2005)*, 17-20 October 2005, pp. 1813-1818.

c112 H. Parizi, A. Niktash, A. Kamalizad, and N. Bagherzadeh, "A Reconfigurable Architecture for Wireless Communication Systems," *Third International Conference on Information Technology: New Generations, (ITNG 2006)*, 10-12 April 2006, pp. 250-255.

c113 J. Davila, A. de Torres, J. M. Sanchez, M. Sanchez-Elez, N. Bagherzadeh, and F. Rivera, "Design and Implementation of a Rendering Algorithm in a SIMD Reconfigurable Architecture (MorphoSys)," *Proceedings of Design, Automation, and Test in Europe (DATE 2006),* 6-10 March 2006, pp. 6.

c114 S. Lee, J. Bahn, and N. Bagherzadeh, "Design of a Feasible On-Chip Interconnection Network for a Chip Multiprocessor (CMP)," *19th SBAC,* October 2007.

c115 S. Lee and N. Bagherzadeh, "Increasing the Throughput of an Adaptive Router in Network-on-Chip (NoC)," *Proceedings of the 4th International Conference on Hardware/software codesign and system synthesis, 2006. CODES+ISSS '06,* 22-25 Oct. 2006 Page(s):82 - 87

c116 F. Rivera, M. Sanchez-Elez, M. Fernandez, R. Hermida, and N. Bagherzadeh, "Configuration Scheduling for Conditional Branch Execution onto Multi-Context Reconfigurable Architectures," *International Conference on Field Programmable Logic and Applications, 2006. FPL '06*, 28-30 Aug. 2006, Page(s):1 – 8.

c117 A. Niktash, H. Parizi, and N. Bagherzadeh, "A Multi-Standard Viterbi Decoder for Mobile Applications Using a Reconfigurable Architecture," *Vehicular Technology Conference, 2006. VTC-2006 Fall. 2006 IEEE 64th,* Page(s):1 – 5.

c118 N. Tabrizi and N. Bagherzadeh, "A Distributed and Shared Register File for a Multiprocessor-on-Chip to Support Real-Time Applications," *The 9th International Conference on Advanced Communication Technology,* Dec. 2006 Page(s):215 – 220.

c119 N. Tabrizi and N. Bagherzadeh, "A Parallel Sort Engine with Dynamic Memory for a Multiprocessor-on-a-Chip," *Proceedings of the Fourth IASTED International Conference, Circuits, Signals, and Systems,* November, 2006 Page(s):169 – 174.

c120 A. Niktash, H. Parizi, and N. Bagherzadeh, "A Study of Implementation of IEEE 802.11 a Physical Layer on a Heterogeneous Reconf1gurable Platform," *The 9th International Conference on Advanced Communication Technology,* Volume 3, 12-14 Feb. 2007 Page(s):2101 – 2105.

c121 B. Gorjiara, N. Bagherzadeh, and P. Chou, "Integrating Power Management into Distributed Real-time Systems at Very Low Implementation Cost," *Asia and South Pacific Design Automation Conference, 2007. ASP-DAC '07.,* 23-26 Jan. 2007 Page(s):872 – 877.

c122 A. Hatanaka and N. Bagherzadeh, "A Modulo Scheduling Algorithm for a Coarse-Grain Reconfigurable Array Template," *IEEE International Parallel and Distributed Processing Symposium, 2007. IPDPS 2007,* 26-30 March 2007 Page(s):1 – 8.

c123 A. Niktash, H. Parizi, and N. Bagherzadeh, "Application of a Heterogeneous Reconfigurable Architecture to OFDM Wireless Systems," *IEEE International Symposium on Circuits and Systems, 2007. ISCAS 2007,* 27-30 May 2007 Page(s):2586 – 2589.

c124 S. Lee, J. Bahn, and N. Bagherzadeh, "Design of a Feasible On-Chip Interconnection Network for a Chip Multiprocessor (CMP)," *19th International Symposium on Computer Architecture and High Performance Computing, 2007. SBAC-PAD 2007,* 24-27 Oct. 2007 Page(s):211 – 218.

c125 J. Bahn, S, Lee, and N. Bagherzadeh, "On Design and Analysis of a Feasible Network-on-Chip (NoC) Architecture," *International Conference on Information Technology, ITNG 2007.*

c126 H. Eldeeb, H. Elsadek, H. Abdallah, and N. Bagherzadeh, "FDTD Accelerator for Calculating SAR Distributed Inside Human Head due to Radiation from Wireless Devices," *EMTS 2007 International URSI Commission B - Electromagnetic Theory Symposium.,* July 26-28, 2007 Ottawa, ON, Canada.

c127 A. Niktash, H. Parizi, A. H. Kamalizad, and N. Bagherzadeh, "PHY 23-3 - RECFEC: A Reconfigurable FEC Processor for Viterbi, Turbo, Reed-Solomon and LDPC Coding," *IEEE Wireless Communications and Networking Conference, 2008. WCNC 2008,* March 31 2008-April 3 2008 Page(s):605 – 610.

c128 J. Bahn, J. Yang, and N. Bagherzadeh, "Parallel FFT Algorithms on Network-on-Chips," *Fifth International Conference on Information Technology: New Generations, 2008. ITNG 2008,* 7-9 April 2008 Page(s):1087 – 1093.

c129 N. Bagherzadeh and M. Matsuura, "Performance Impact of Task-to-Task Communication Protocol in Network-on-Chip," *Fifth International Conference on Information Technology: New Generations, 2008. ITNG 2008,* 7-9 April 2008 Page(s):1101-1106.

c130 J. Bahn and N. Bagherzadeh, "Efficient Parallel Buffer Structure and Its Management Scheme for a Robust Network-on-Chip (NoC) Architecture," *13th International CSI Computer Conference (CSICC 2008),* Kish Island, Iran, 2008.

c131 W. Trumler, S. Schlingmann, T. Ungerer, J. Bahn, and N. Bagherzadeh, "Self-optimized Routing in a Network-on-a-Chip," *20th IFIP World Computer Congress,* Milano, Italy 7-10 September 2008.

c132 H. Elsadek, H. Eldeeb, H. Abdallah, M. Desouky and N. Bagherzadeh, "Specific Absorption Rate Calculation using Parallel Finite Difference Time Domain," *WORLDCOMP'08*, Las Vegas, July 2008.

c133 F. Bagci, T. Ungerer, and N. Bagherzadeh, "ESTR – Energy Saving Token Ring Protocol for Wireless Sensor Networks," *WORLDCOMP'08 Conference, Proceedings of the International Conference on Wireless Networks (ICWN 08)*, Las Vegas, July 2008.

c134 F. Bagci, F. Kluge, T. Ungerer, and N. Bagherzadeh, "LocSens- An Indoor Location Tracking System using Wireless Sensors," *Proceedings of the First IEEE International Workshop on Sensor Networks (SN 2008)*, St. Thomas, VI, USA, August 2008.

c135 W. Hu, J. Bahn, and N. Bagherzadeh, "Parallel LDPC Decoding on a Network-on-Chip Based Multiprocessor Platform," *Computer Architecture and High Performance Computing, 2009, SBAC-PAD '09*, Sao Paulo, October 2009, Pages 35-40.

c136 A. Hatanaka and N. Bagherzadeh, "Scheduling Techniques for Multi-Core Architectures," *Proceedings of 6th International Conference on Information Technology: New Generations, 2009, ITNG '09,* Las Vegas 2009, Pages 865-870.

c137 W. Hu, C Chen, and N. Bagherzadeh, "A Spectral-Based Partitioning Algorithm for Parallel LDPC Decoding on a Multiprocessor Platform," SoC Design Conference, New Port Beach, CA 2009, Pages 245-248.

c138 Y. Yang, J. Bahn, S. Lee and N. Bagherzadeh, "Parallel and Pipeline Processing for Block Cipher Algorithms on a Network-on-Chip," *Proceedings of 6th International Conference on Information Technology: New Generations, 2009, ITNG '09,* Las Vegas 2009, Pages 849-854.

c139 S. Lee, C. Wilkerson, M. Zhang, R. Yavatkar, S. Lu, and N. Bagherzadeh, "Low Power Adaptive Pipeline Based on Instruction Isolation," *10th Int'l Symposium on Quality Electronic Design ISQED 2009,* Pages 788-793.

c140 F. Bagci, J. Wolf, T. Ungerer, and N. Bagherzadeh, "Mobile Agents for Wireless Sensor Networks," *ICWN'09 - The 2009 International Conference on Wireless Networks*, Las Vegas, USA, July 13-16, 2009

c141 F. Bagci, T. Ungerer, and N. Bagherzadeh, "SecSens - Security Architecture for Wireless Sensor Networks," *Third International Conference on Sensor Technologies and Applications, SENSORCOMM 2009,* Pages 449-454.

c142 J. Huseynov, S. Baliga, M. Dillencourt, L. Bic, and N. Bagherzadeh, "Gas-Leak Localization Using Distributed Ultrasonic Sensors," *Smart Sensor Phenomena, Technology, Networks, and System, Proc. of SPIE Vol. 7293 72930Z-18,* 2009.

c143 H. Abdullah, J. Yang, N. Bagherzadeh, and K. Hussein, "Parallel Electric Field Integral Equation Solver for Arbitrary Shaped Conducting Bodies," *Progress In Electromagnetics Research Symposium,* Beijing, China, March 23-27, 2009, Pages 1661-1666

c144 C. Wang, W Hu, N. Bagherzadeh, and S Lee, "Area and Power-Efficient Innovative Network-on-Chip Architecture," *18th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP)2010,* Pages 533-539.

c145 F. Penczek, S. Herhut, S. Scholz, A Shafarenko, J, Yang, C. Chen, N. Bagherzadeh, and C. Grelck, "Message Driven Programming with S-Net Methodology and Performance," *39th International Conference on Parallel Processing Workshops (ICPPW), 2010,* Pages 405-412.

c146 A. Alhussien, C. Wang, and N. Bagherzadeh, "A Scalable Delay Insensitive Asynchronous NoC with Adaptive Routing," *IEEE 17th International Conference on Telecommunications (ICT) 2010,* Pages 995-1002.

c147 C. Wang, W Hu, and N. Bagherzadeh, "Congestion-Aware Network-on-Chip Router Architecture," *15th CSI International Symposium on Computer Architecture and Digital Systems (CADS) 2010,* Pages 137-144.

c148 H. Eldeeb, H. Elsadek, M. Dessokey, H. Abdullah, and N. Bagherzadeh, "High Performance Parallel Computing for FDTD Numerical Technique in Electromagnetic Calculations for SAR Distribution Inside Human Head," *14th WSEAS International Conference on Computer*, July 23-25 2010, Corfu, Greece.

c149 H. Abdullah, H. Elsadek, H. Eldeeb, and N. Bagherzadeh, "High Performance Grid Computation of the Scattered Field Formulation for Nth Order Debye Modeling of the General Dispersive Media," *International Conference on Bioinformatics and Computational Biology, BIOCOMP'11*, July 18-21, 2011, Monte Carlo Resort, Las Vegas, Nevada, USA.

c150 C. Wang, W Hu, and N. Bagherzadeh, "A Wireless Network-on-Chip Design for Multicore Platforms," *2011 19th International Euromicro Conference on Parallel, Distributed and Network-Based Processing,* Pages 409-416

c151 J. Yang, C. Chun, N. Bagherzadeh, and S. Lee "Load Balancing for Data-Parallel Applications on Network-on-Chip Enabled Multi-Processor Platform," *2011 19th International Euromicro Conference on Parallel, Distributed and Network-Based Processing,* Pages 439-446

c152 C. Wang, W Hu, and N. Bagherzadeh, "Design and Evaluation of a High Throughput QoS-Aware and Congestion-Aware Router Architecture for Network-on-Chip," *2012 20th International Euromicro Conference on Parallel, Distributed and Network-Based Processing,* Pages 457-464

c153 W. Hu, C. Wang, and N. Bagherzadeh, "Design and Analysis of a Mesh-based Wireless Network-on-Chip," *2012 20th International Euromicro Conference on Parallel, Distributed and Network-Based Processing*, Pages 483-490

c154 S. Azampanah, A. Khademzadeh, N. Bagherzadeh, M. Janidarmian, and R. Shojaee "LATEX: New Selection Policy for Adaptive Routing in Application-Specific NoC," *PDP 2012*, Pages 515-519

c155 A. Alhussien, N. Bagherzadeh, F. Verbeek, B. van Gastel, and J. Schmaltz "A Formally Verified Deadlock-Free Routing Function in a Fault-Tolerant NoC Architecture," *SBCCI 2012*, Pages 1-6

c156 A. Eskandari, A. Khademzadeh, N. Bagherzadeh, and M. Janidarmian "Quality of Service Optimization for Network-on-Chip Using Bandwidth-Constraint Mapping Algorithm," *PDP 2013*, Pages 504-508

c157 A. Demiriz, N. Bagherzadeh, and A. Alhussien "CPNoC: On Using Constraint Programming in Design of Network-on-Chip Architecture," *PDP 2013*, Pages 486-493

c158 A. Demiriz and N. Bagherzadeh "On Heterogeneous Network-on-Chip Design Based on Constraint Programming," NoCArc, MICRO 2013, Pages 29-34

c159 J. Bahn and N. Bagherzadeh "A Generic Traffic Model for On-Chip Interconnection Networks," NoCArc, 2008, Pages 22-29

c160 W. Hu and N. Bagherzadeh "DMesh: a Diagonally-Linked Mesh Network-on-Chip Architecture," *NoCArc*, 2008, Pages 14-20

c161 P. Yaghini, A. Eghbal, and N. Bagherzadeh "A GALS Router for Asynchronous Network-on-Chip," *MES '14 Proceedings of International Workshop on Manycore Embedded Systems,* 2014

c162 A. Eghbal, P. Yaghini, S. Yazdi, and N. Bagherzadeh, "TSV-to-TSV Inductive Coupling Aware Coding Scheme for 3D Network-on-Chip," *Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2014 IEEE International Symposium on*, pp. 92–97, Oct 2014.

c163 F. Hosseinzadeh, N. Bagherzadeh, A. Khademzadeh, M. Janidarmian, and F. Karimi, "Improving Reliability in Application-Specific 3D Network-on-Chip," *Proceedings of the World Congress on Engineering and Computer Science 2012 Vol I WCECS*, October 24-26, 2012, San Francisco, USA.

c164 R. Salamat, M. Ebrahimi, and N. Bagherzadeh, "An Adaptive, Low Restrictive and Fault Resilient Routing Algorithm for 3D Network-on-Chip," *2015 23rd Euromicro International Conference on Parallel, Distributed, and Network-Based Processing*, DOI 10.1109/PDP.2015.91, pp. 392-395, 2015.

c165 A. Eghbal, P. Yaghini, and N. Bagherzadeh, "Capacitive Coupling Mitigation for TSV-Based 3D ICs," *2015 IEEE 33rd VLSI Test Symposium (VTS)*, (2015)

c166 M. S. Rusli, O. C. Yee, M. N. Marsono, P. Yaghini, N. Bagherzadeh, D. Patti, V. Dieei, and M. Palesi, "An Energy Aware Transmission Control in Wireless Network-on-Chip," *Recent Advances in Computer Science*, (ISBN: 978-1-61804-297-2), pp. 24-33, 2015,

c167 H. Elsadek, H. Eldeeb, H. Abdallah, and N. Bagherzadeh, "SAR Distribution over whole Human Body Existed in the Field of Mobile Base Station Antenna," *International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO), 2015 IEEE MTT-S*, https://doi.org/10.1109/NEMO.2015.7415033, Ottawa, Canada

c168 P. Yaghini, A. Eghbal, S. Yazdi, and N. Bagherzadeh "Accurate System-level TSV-to-TSV Capacitive Coupling Fault Model for 3D-NoC," *NOCS 2015,* Vancouver, BC, Canada, DOI: http://dx.doi.org/10.1145/2786572.2786598

c169 Q. Zhao, M. Rajaei, I. Krivorotov, M. Nilsson, N. Bagherzadeh, and O. Boyraz "Optical Investigation of Radiation Induced Conductivity Changes in STT-RAM Cells," *Conference on Lasers and Electro-Optics, OSA Technical Digest (online) (Optical Society of America 2016,* DOI https://doi.org/10.1364/CLEO_QELS.2016.FM3B.2

c170 F. Verbeek, P. Yaghini, A. Eghbal, and N. Bagherzadeh "ADVOCAT: Automated Deadlock Verification for On-chip Cache coherence and Interconnects," *DATE 2016,* Dresden, Germany

c171 R. Salamat, M. Ebrahimi, N. Bagherzadeh, and F. Verbeek, "CoBRA: Low Cost Compensation of TSV Failures in 3D-NoC," *2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT),* DOI 10.1109/DFT.2016.7684081,

c172 Z. Ghaderi, A. Alqahtani, and N. Bagherzadeh, "Online Monitoring and Adaptive Routing for Aging Mitigation in NoCs," *2017 DATE,* DOI https://doi.org/10.23919/DATE.2017.7926960, 27-31 March 2017, Lausanne, Switzerland

c173 M. Nilsson, I. Krivorotov, O. Boyraz, N. Bagherzadeh, R. Ngelale, B. Adolf, J. Chen, E. Montoya, H. Lee, C. Sha, S. Mohammadi, P. Sadri, H. Tseng, L. Wan, and E. Yang, "Effect of Ionizing Radiation on STT-RAM Multilayers," *GOMAC 2017.*

c174 P. Sadri, M. Khan, Q. Zhao, I. Krivorotov, M. Nilsson, N. Bagherzadeh, and O. Boyraz, "Plasmonic Detection of Possible Defects in Multilayer Nanohole Array Consisting of Essential Materials in Simplified STT-RAM Cell," 2017 *SPIE Optics and Photonics Conference,* San Diego, CA.

c175 A. Albaqsami, M. Hosseini, and N. Bagherzadeh, "HTF-MPR: A Heterogeneous TensorFlow Mapper Targeting Performance using Genetic Algorithms and Gradient Boosting Regressors," *DATE* (2018), 978-3-9819263-0-9/DATE18/c 2018 EDAA

c176 M. Torabzadehkashi, S. Rezaei, V. Alves, and N. Bagherzadeh, "CompStor: An In-Storage Computation Platform for Scalable Distributed Processing," *2018 IEEE International Parallel and Distributed Processing Symposium Workshops*, DOI 10.1109/IPDPSW.2018.00195

c177 L. Morales, J. Aedo, and N. Bagherzadeh, "Simulation-Based Evaluation Strategy for Task Mapping Approaches in WNoC Platforms," *26th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (2018)*, DOI 10.1109/PDP2018.2018.00104

c178 M. Kim, A. Del Barrio, R. Hermida, and N. Bagherzadeh, "Low-Power Implementation of Mitchell's Approximate Logarithmic Multiplication for Convolutional Neural Networks," *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, DOI: 10.1109/ASPDAC.2018.8297391

c179 H. Kim, M. Kim, A. Del Barrio, and N. Bagherzadeh, "A Cost-Efficient Iterative Truncated Logarithmic Multiplication for Convolutional Neural Networks," *2019 IEEE 26th Symposium on Computer Arithmetic (ARITH)*, DOI 10.1109/ARITH.2019.00029

c180 M. Torabzadehkashani, S. Rezaei, A. Heydarigorji, H. Bobarshad, A. Alves, and N. Bagherzadeh, "Catalina: In-Storage Processing Acceleration for Scalable Big Data Analytics," *2019 27th Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP)*, DOI 10.1109/PDP.2019.00069

c181 S. Mohammadi, M. Jasemi, S. Talebi, N. Bagherzadeh, and M. Green, "A Radiation Hard Sense Circuit for Spin Transfer Torque Random Access Memory," *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, DOI: 10.1109/ISCAS.2019.8702416

c182 S. Shahhosseini, A. Albaqsami, M. Jasemi, and N. Bagherzadeh, "Partition Pruning: Parallelization-Aware Pruning for Dense Neural Networks," *28th Euromicro*

International Conference on Parallel, Distributed and Network-Based Processing (PDP), 2020, DOI 10.1109/PDP50117.2020.00052

c183 M. Alnemari and N. Bagherzadeh, "Efficient Deep Neural Networks for Edge Computing," *2019 IEEE International Conference on Edge Computing (EDGE),* **Best Paper**, DOI 10.1109/EDGE.2019.00014

c184 P. Sadri, M. Wahiduzzaman, M. Shafiqul Islam, I. Krivorotov, M. Nilsson, N. Bagherzadeh, and O. Boyraz, "Array of Symmetric Nanohole Dimers for STT-RAM Ultrathin Layer Sensing," *CLEO 2019*

c185 Z. Ren, A. Alqahtani, N. Bagherzadeh, and J. Lee, "Thermal Analysis of 3D ICs with TSVs Placement Optimization," *Proceedings of the ASME 2019 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems*, October 7-9, 2019, Anaheim, CA

c186 S. Sadri, M. Wahiduzzaman, M. Bayer, M. Islam, E. Montoya, I. Krivorotov, M. Nilsson, N. Bagherzadeh, and O. Boyraz, "Effect of Tantalum and MgO Adhesion Layers on Plasmonic Nanostructures," *SPIE Nanoscience + Engineering*, 2019, San Diego, California.

c187 M. Torabzadehkashi, A. Heydarigorji, S. Rezaei, H. Bobarshad, V. Alves, and N. Bagherzadeh, "Accelerating HPC Applications Using Computational Storage Devices," *HPCC*, 2019

c188 L. Tavares, M. S. Kim, A. Del Barrio, N. Bagherzadeh, and R. Menotti, "Design of Power-Efficient FPGA Convolutional Cores with Approximate Log Multiplier," *European Symposium on Artificial Neural Networks, Computational Intelligence and Machine Learning*, April 2019

c189 L. Alhubail and N. Bagherzadeh, "Power and Performance Optimal NoC Design for CPU-GPU Architecture Using Formal Models," *DATE-19*, 2019

c190 L. Alhubail, M. Jasemi, and N. Bagherzadeh, "NoC Design Methodologies for Heterogeneous Architecture," *2020 28th Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP)*, DOI 10.1109/PDP50117.2020.00052

c191 M. Moghadam, E. Masoumi, N. Bagherzadeh, D. Ramsingh, and Z. Kain, "Supervised Machine-Learning Algorithms in Real-time Prediction of Hypotensive Events," *2020 42nd Annual International Conference of the IEEE Engineering in Medicine & Biology*,

c192 M. Hosseini, M. Ebrahimi, P. Yaghini, and N. Bagherzadeh, "Application Characterization for Near Memory Processing," *2021 29th Euromicro International*

Conference on Parallel, Distributed and Network-Based Processing (PDP), DOI 10.1109/PDP52278.2021.00031

c193 P. Sadri-Moshkenani, M. Wahiduzzaman Khan, Md Shafiqul Islam, D. Shi, E. Montoya, I. Krivorotov, N. Bagherzadeh, and O. Boyraz, "Optoelectronic Readout of STT-RAM Memory Cells Using Plasmon Drag Effect," *CLEO 2021*

c194 Y. Qiao, M. Alnemari, and N. Bagherzadeh, "A Two-Stage Efficient 3-D CNN Framework for EEG Based Emotion Recognition," *23rd IEEE International Conference on Industrial Technology (ICIT 2022)*, August 2022.

c195 H. Kaeley, Y. Qiao, and N. Bagherzadeh, "Support for Stock Trend Prediction Using Transformers and Sentiment Analysis," *IISES 18th Economics and Finance Conference*, London 2023. https://doi.org/10.48550/arXiv.2305.14368

Professional Associations and Achievements

- Fellow Member, Institute of Electrical and Electronics Engineers (IEEE)
- Member, IEEE Computer Society

Extramural Funding (over 8 million dollars)

- (with Dan Gajski, Lubomir Bic, and Kane Kim), 32 node Intel hypercube, *Information and Computer Science and Engineering (CISE) Research Instrumentation - NSF*, $187,274, 1990. This equipment is shared with other co-principles to study parallelism.

- (with Jack Sklansky), "Multiprocessor Architecture for Image Processing," $26,700. A MICRO Research Proposal with Rockwell International, 1990-91.

- (with Alex Nicolau), "Design of a RISC Based Multiprocessor for a Fine-Grain Optimizing Compiler," $33,900. A MICRO Research Proposal with Northrop Corporation, 1990-91.

- (with Dan Gajski), "Design of a RISC Cluster VLSI Chip," $120,000. A Western Digital Fellowship in VLSI Systems Engineering; support for two students for two years at $30,000 per fellow per year (this amount includes a stipend of $18,000, tuition and fees, $3,000 for their project, and the remainder for the use of the Electrical and Computer Engineering Department)

- (with Kevin Tsai and Jack Sklansky), "A Hypermesh Architecture for Image Multiprocessing," $20,000. A MICRO Research Proposal with Rockwell International, 1990-1991.

- ARMY faculty fellowship, $10,000, 1990.

- From Sony Corporation for support of advanced computer architecture design, $30,000, Tokyo, Japan, 1990.

- NASA/ASEE faculty fellowship, $10,000, 1991.

- From NKK Corporation for support of advanced computer architecture design, $129,000, Tokyo, Japan, 1991-92.

- "A Quantitative Performance Comparison of a VLIW and Superscalar Architectures," $30,000, a MICRO Research Proposal with Unitec, 1992-93.

- From Asahi Chemical for support of advanced computer architecture design, $40,000, 1993-94.

- (with Douglas Blough), Intel MICRO project for iPSC/860 list price ($265,000) plus cash donation from the state ($15,000), 1994.

- "Software techniques for improving the efficiency of superscalar microprocessors," ($25,000 from Unitech Research Inc), ($11,247 from UC MICRO), 1995.

- (with Fadi Kurdahi), "Digital QAM structures," ($20,000 from SMC), ($14,288 from UC MICRO), 1995.

- (with Fadi Kurdahi), "Design and efficient VLSI implementation of a transceiver chip," ($20,000 from SMC), ($11,869 from UC MICRO), 1996.

- (with Fadi Kurdahi), "A study of high-speed LAN transceiver chips," ($20,000 from SMC), ($11,824 from UC MICRO), 1997.

- (with Fadi Kurdahi), "Dynamically reprogrammable architecture: a new approach to adaptive computing," $1,182,000 DARPA, 1997-2000.

- (with Fadi Kurdahi), "CISE-NSF-CNPq collaboration research," $150,000, NSF-CNPq, 1998-2000

- (with Fadi Kurdahi), "Dynamically reprogrammable architecture: a new approach to adaptive computing," $280,000 DARPA Supplemental Funding, 2000-2001

- (with Pai Chou, Scott Jordan, Fadi Kurdahi, and J.L. Gaudiot-USC), "IMPAC^{2}T: integrated management of power aware computation and communication technologies," $750, 000, DARPA-ITO, 2000-2002

- (with Fadi Kurdahi), "Synthesis of mission-specific processors," $500,000, NSF-ITR, 2000-2003

- (with Fadi Kurdahi), "Using low power reconfigurable computing for high-speed and wireless network appliances," $200,000, CoRe (with Broadcom), 2000-2002

- (with Hutchinson, Kuester, Shinozuka, and Warschauer), "Expanding Engineering Thinking: Interactive Visualization of Numerical Models", $410,000, NSF, 2002-2005

- (with Chou), "Mission Aware Power Management," $680, 000, DARPA PACC Phase II, 2002-2004

- "Design and Implementation of Automatic Parallel Detection Layer,", $24,000, NSF-INT (Egypt), 2001-2003

- (with Faryar, Yang, and Bobrow), "ITR-Dev. of Intelligent Infrastructure For Hazard Mitigation," $300,000, NSF, 2002-2005.

- "Development of FDTD Accelerator for 3D Mutual Interaction Between Human Body and Radiation From Wireless Devices," $28,500, NSF, 2005-2008

- "Autonomic and Organic Real-time SoC Design," €5,000, Bavaria California Technology Center (BaCaTec), 2004-2006

- "Task Management on a Reconfigurable Architecture," €10,200, Uuniversidad Complutense, Madrid**,** 2006-2007

- "Multicore Computing," €4,000, Bavaria California Technology Center (BaCaTec), 2008-2009

- "US-Egypt Cooperative Research: Health Hazards due to Radiation from Mobile Base Stations," $50,000, NSF, Office of International Science & Engineering, 2010-2012

- (with Nilsson, Miller, Detwiler, and Boyraz), "Nuclear Science and Security Consortium: Nuclear Engineering," $2,500,000, NNSA, 2011-2016

- (with Li and Kurdahi), "Plug Load Energy Reporting and Display," $49,335, California Energy Resources Conservation and Development Commission, 2013-2014

- (with Boyraz, Krivorotov, and Nilsson), "Radiation Characterization of STT-RAM Devices," $1,050,000, DTRA, 2016-2018; Additional One Year; $350,000, 2020-2021

- (with Jaeho Lee), "3D IC Thermal Management Based on TSV Placement Optimization and Novel Materials," $270,000, 2017-2020