

← → ↻ <https://past.date-conference.com/proceedings-archive/2002/YEAR.HTM> 67% ☆



MARCH 25—29, 2019
FLORENCE, ITALY
FIRENZE FIERA

DESIGN, AUTOMATION AND TEST IN
EUROPE THE EUROPEAN EVENT FOR



MAIN PAGE
DATE 2002
Proceedings:
Table of Content
Abstracts
Session Index
Author Index

Design,
Automation
and Test
in Europe

D·A·T·E 02

Proceedings

Edited by Carlos Delgado Kloos
Jose da Franca

Le Palais des Congrès, Paris, France
March 4-8, 2002

www.date-conference.com

Sponsored by
EDAA
EDAC
IEEE Computer Society TTTC
IEEE Computer Society DATC
ECSI
ACM/SIGDA
IAS



← → ↻ https://past.date-conference.com/proceedings-archive/2002/YEAR.HTM 67% ☆

DATE 19
MARCH 25—29, 2019
FLORENCE, ITALY
FIRENZE FIERA
DESIGN, AUTOMATION AND TEST IN EUROPE THE EUROPEAN EVENT FOR

MAIN PAGE
DATE 2002
Proceedings:
Table of Content
Abstracts
Session Index
Author Index

1 of 5 Automatic Zoom

Technical Program Committee

Bashir Al-Hashimi, Southampton U, UK
Daniel Auvergne, LIRMM, FR
Florence Azais, LIRMM, FR
Carlos Azeredo Leme, ChipIdea, PT
Erich Barke, Hannover U, DE
Alfredo Benso, Politecnico di Torino, IT
Reinaldo A. Bergamaschi, IBM, US
Michel Berkelaar, Magma Design Automation, NL
Gerard, Berry, Esterel Technologies, FR
Christian Berthet, STMicroelectronics, FR
Shuvra S. Bhattacharya, Maryland U, US
David Blaauw, Motorola, US
Massimo Bombana, Siemens ICN, IT
Frank Brglez, NC State U, US
Randal E. Bryant, Carnegie Mellon U, US
Klaus Buchenrieder, Infineon Technologies, DE
Jean-Paul Calvez, IRESTE-Nantes U, FR
Paolo Camurati, Politecnico di Torino, IT
Flavio Canavero, Politecnico di Torino, IT
Marco Carilli, STMicroelectronics, FR
Gunnar Carlsson, Ericsson Radio Systems, SE
Johan Catrysse, KHBO, BE
Sreejit Chakravarty, Intel, US
Victor Champac, INAOE, MX
Abijit Chatterjee, GATECH, US
Kuang-Chien Cheng, Verplex Systems, US
Peter Y.K. Cheung, Imperial College, UK
Vivek Chickermane, IBM, US
Juan Chico, CNM Seville, ES
Kiyoun Choi, Seoul National U, KR
Marcello Coppola, STMicroelectronics, FR
Jordi Cortadella, UP Catalunya, ES
Bernard Courtois, TIMA, FR
Jan Craninckx, Alcatel Microelectronics, BE
Walter Daems, KU Leuven, BE
Carl Das, IMEC, BE
Ali Dasdan, Synopsis, US
Giovanni De Micheli, Stanford U, US
Carlos Delgado Kloos, Carlos III de Madrid U, ES
Serge Demidenko, Massey U, NZ
Carsten Demuth, Infineon Technologies, DE
Alex Doboli, New York State U, US
Rolf Drechsler, Bremen U, DE
Nikil Dutt, UC Irvine, US
George E. Economakos, Athens NTU, GR
Martyn Edwards, UMIST, UK
Stephen A. Edwards, Columbia U, US
Petru Eles, Linköping U, SE
Ibrahim Elfadel, IBM, US
Marc Engels, IMEC, BE
Luis Entrena, Carlos III de Madrid U, ES

xxxi

Rolf Ernst, TU Braunschweig, DE
Hans Eveking, TU Darmstadt, DE
Peter Feldmann, CeLight, US
Uwe Feldmann, Infineon Technologies, DE
Francisco Fernandez, IMSE-CNMI, U Seville, ES
Joan Figueras, UP Catalunya, ES
Franco Fiori, Politecnico di Torino, IT

Limor Frick, Intel, ISR
 Marie-Lise Flottes, LIRMM, FR
 William Fornaciari, Politecnico di Milano, IT
 Norbert Fristacky, Slovak TU, SK
 Hideo Fujiwara, Nara IT, JP
 Daniel Gajski, UC Irvine, US
 Jim Garside, Manchester U, UK
 Catherine Gebotys, Waterloo U, CA
 Daniel Geist, IBM Haifa Research Lab, ISR
 Eberhard Gerbracht, TU Braunschweig, DE
 Vassilios Gerousis, Infineon Technologies, DE
 Georges Gielen, KU Leuven, BE
 Dimitris Gizopoulos, Pireaus U, GR
 Manfred Glesner, TU Darmstadt, DE
 Michael Goessel, Potsdam U, DE
 Helmut Graeb, TU Munich, DE
 Miltos Grammatikakis, ISD SA, GR
 Werner Grass, Passau U, DE
 Thorsten Groetker, Synopsys, DE
 Guido Gronthoud, Philips, NL
 Herbert Gruenbacher, Carinthia Tech. Inst., AT
 Herve Guegan, Mentor Graphics Anacad, FR
 Rajesh Gupta, UC Irvine, US
 David Harris, Harvard Mudd College, US
 Ian G. Harris, Massachusetts U, US
 Peter Harrod, ARM, UK
 Reiner Hartenstein, Kaiserslautern U, DE
 Takashi Hasegawa, Fujitsu, JP
 Sybille Hellebrand, Innsbruck U, AT
 Joerg Henkel, NEC, US
 Roman Hermida, Madrid Complutense U, ES
 Hiromi Hiraishi, Kyoto Sangyo U, JP
 Mokhtar Hirech, Synopsys, US
 H. Peter Hofstee, IBM, US
 Nuno Horta, IST, PT
 Harry Hsieh, UC Berkeley, US
 Jose Luis Huertas, CNM Seville, ES
 Ed Huijbregts Magma Design Automation, NL
 Sorin Huss, TU Darmstadt, DE
 Thomas Ifström, Robert Bosch GmbH, DE
 Margarida F. Jacome, U Texas at Austin, US
 Jörn W. Janneck, UC Berkeley, US
 Axel Jantsch, Royal Inst. of Technology, SE
 Ahmed Jerraya, TIMA Grenoble, FR
 Frank M. Johannes, TU Munich, DE
 Werner John, FhG-IZM, DE
 Andreas Kaiser, IEMN-ISEN, FR
 Bozena Kaminska, Fluence Technology, US
 Ramesh Karri, Polytech U Brooklyn, US

xxxii

Tom Kazmierski, Southampton U, UK
 Udo Kebschull, Leipzig U, DE
 Hans Kerkhoff, Twente U, NL
 David Kinniment, Newcastle U, UK
 Kozo Kinoshita, Osaka Gaukin U, JP
 Michael Kishinevsky, Intel, US
 Bernd Kleinjohann, Paderborn U/C-LAB, DE
 Gernot Koch, Bridges2Silicon Inc, US
 Michael Koch, Stralsund FH, DE
 Juergen Koehl, IBM Deutschland GmbH, DE
 Cheng-Kok Koh, Purdue U, US
 Agnieszka Konczykowska, Alatel R&I, FR
 Reiner Kress, Infineon Technologies, DE
 Thomas Kropf, Robert Bosch GmbH, DE
 Wido Kruijtzter, Philips, NL
 Bram Kruseman, Philips, NL
 Ernest S. Kuh, UC Berkeley, US
 Sandip Kundu, Intel, US
 Wolfgang Kunz, Kaiserslautern U, DE
 Fadi Kurdahi, Morpho Technologies, US
 Christian Landrault, LIRMM, FR
 Rudy Lauwereins, IMEC, BE
 Luciano Lavagno, P Torino, IT
 Edward Lee, UC Berkeley, US
 Domine Leenaerts, Philips, NL
 Rainer Leupers, Dortmund U, DE
 Regis Leveugle, TIMA Grenoble, FR
 Stan Liao, Synopsys, US
 Jens Lienig, Robert Bosch GmbH, DE
 Vanko Litovski, Elektronski Fakultet, YU
 Monica Lobetti Bodoni, Siemens ICN SpA, IT
 Juan Carlos Lopez, Castilla-La Mancha U, ES
 Weikko Loukusa, Nokia, FIN

Patrick Lysaght, Xilinx, UK
 Fadi Maamari, LogicVision Inc, US
 Enrico Macii, P Torino, IT
 Jan Madsen, TU Denmark, DK
 Kenneth Mandl, Teradyne Inc, US
 Stefano Manetti, Florence U, IT
 Hans Manhaeve, Q-Star Test, BE
 Diana Marculescu, Carnegie Mellon U, US
 Erik Jan Marinissen, Philips, NL
 Grant Martin, Cadence Design Systems, US
 Natividad Martinez Madrid, FZI Karlsruhe, DE
 Peter Maxwell, Agilent, US
 Ken McMillan, Cadence Berkeley Labs, US
 Fernando Medeiros, Seville U, ES
 Renu Mehra, Clearwater Networks, US
 Thomas F. Melham, Glasgow U, UK
 Bart Mesman, Philips, NL
 Cecilia Metra, Bologna U, IT
 Volker Meyer zu Bexten, TEMIC Semiconductors GmbH, DE
 Shin-ichi Minato, NTT, JP
 Miguel Miranda, IMEC, BE
 Yukiya Miura, Tokyo U, JP
 Klaus Mueller-Glaser, Karlsruhe U, DE

xxxiii

Peter Muhmentahler, Infineon Technologies, DE
 Tamal Mukherjee, Carnegie Mellon U, US
 Michael Münch, Alcatel, BE
 Rajeev Murgai, Fujitsu, US
 Michel Nakhla, Carleton U, CA
 Sanjiv Narayan, Cadence Design Systems, IND
 Zainalabedin Navabi, Northeastern U, US
 Wolfgang Nebel, OFFIS/Oldenburg U, DE
 Michael Nicolaidis, iRoC Technologies, FR
 Dimitris Nikolas, Patras U, GR
 Pascal Nouet, LIRMM, FR
 Franc Novak, Jozef Stefan Institute, SL
 Enrico Novarini, STMicroelectronics, IT
 Kasia Nowak, Philips, NL
 Steven Nowick, Columbia U, US
 Hermann Obermeier, Infineon Technologies, DE
 Arlindo Oliveira, IST / INESC ID, PT
 Hidetoshi Onodera, Kyoto U, JP
 Alex Orailoglu, UC San Diego, US
 Ralph Otten, TU Eindhoven, NL
 Ian Page, Imperial College, UK
 Sri Parameswaran, Queensland U, AU
 Abelardo Pardo, Carlos III de Madrid U, ES
 Antonis Paschalis, Athens U, GR
 Robert Pasko, IMEC, BE
 Adam Pawlak, ITE, PL
 Massoud Pedram, Southern California U, US
 Zebo Peng, Linköping U, SE
 Ian Phillips, ARM Ltd, UK
 Joel Phillips, Cadence Design Systems, US
 Stanislaw Piestrak, TU Wrocław, PL
 Jose Pineda, Philips, NL
 Carl Pixley, Motorola, US
 Jonas Plantin, Ericsson Radio Systems AB, SE
 Dhiraj Pradhan, Bristol U, UK
 Paolo Prinetto, Politecnico di Torino, IT
 Elke Radeke, Incony AG, DE
 Martin Radetzki, Sci-Worx GmbH, DE
 Franz Rammig, Paderborn U/C-LAB, DE
 Marc Renaudin, TIMA Grenoble, FR
 Marta Rencz, Budapest TU, HU
 Michel Renovell, LIRMM, FR
 Jochen Rivoir, Agilent, DE
 Angel Rodriguez-Vazquez, CNM Seville, ES
 Jerzy Rosenblit, Arizona U, US
 Wolfgang Rosenstiel, FZI Karlsruhe/Tübingen U, DE
 Franz Rossler, Thesys GmbH, DE
 Frederic Rousseau, TIMA Grenoble, FR
 Bruno Rouzeyre, LIRMM, FR
 Kaushik Roy, Purdue U, US
 Adoracion Rueda, CNM Seville, ES
 Imtraud Rugen-Herzig, Infineon Technologies, DE
 Jerzy Rutkowski, Silesian TU, PL
 Frank Sabath, Wehrwissenschaftliches Inst., DE
 Sachin Sapatnekar, Minnesota U, US
 Michel Sarlotte, Thales Communications, FR

vvvii

Gabriele Saucier, Design and Reuse, FR
 Patrick Schaumont, UC Los Angeles, US
 Reimar Scherer, TU Dresden, DE
 Guido Schumacher, Oldenburg U, DE
 Peter Schwarz, FhG IIS/EAS Dresden, DE
 Donatella Sciuto, P Milano, IT
 Carl Sechen, Washington U, US
 Ralf Seepold, FZI Karlsruhe, DE
 Jaume Segura, Illes Balears U, ES
 Bran Selic, Rational, US
 Tom Shiple, Synopsys, FR
 Samvel Shoukourian, Virage Logic, US
 Etienne Sicard, INSA, FR
 Joseph Sifakis, Verimag, FR
 Luis Miguel Silveira, IST / INESC, PT
 Jerry Soden, Sandia National Labs, US
 Ralf Sommer, Infineon Technologies, DE
 Matteo Sonza Reorda, Politecnico di Torino, IT
 Mircea Stan, Virginia U, US
 Janusz Starzyk, Ohio U, US
 Thomas Steinecke, Infineon Technologies, DE
 Franz-Josef Stewing, Materna GmbH, DE
 Michiel Steyaert, KU Leuven, BE
 Leon Stok, IBM, US
 Bernd Straube, FhG IIS/EAS Dresden, DE
 Steve Sunter, LogicVision Inc, CA
 Atsushi Takahashi, Tokyo IT, JP
 Steffen Tarnick, Satcon, DE
 Jürgen Teich, Paderborn U, DE
 Joao Paulo Teixeira, IST, PT
 Lothar Thiele, ETH Zurich, CH
 Claudio Turchetti, Ancona U, IT
 Raimund Ubar, Tallinn TU, EE
 Dirk Van Troyen, De Nayer Inst, BE
 Guy Vandenbosch, KU Leuven, BE
 Gerd Vandersteen, IMEC, BE
 Moshe Vardi, Rice U, US
 Ingrid Verbauwhede, UCLA, US
 Tiziano Villa, PARADES, IT
 Eugenio Villar, Cantabria U, ES
 Flavio Wagner, UFRGS BRZ, MX
 Duncan M. Walker, Texas A&M U, US
 Piet Wambacq, IMEC, BE
 Norbert Wehn, Kaiserslautern U, DE
 Wayne Wolf, Princeton U, US
 Martin D.F. Wong, U Texas at Austin, US
 Cheng-Wen Wu, National Tsing Hua U, ROC
 SungJoo Yoo, IMAG, FR
 Roberto Zafalon, ST Microelectronics, IT
 Gerhard Zimmermann, Kaiserslautern U, DE
 Yervant Zorian, LogicVision Inc, US
 Mark Zwolinski, Southampton U, UK

XXXV

←→↺

https://past.date-conference.com/proceedings-archive/2002/YEAR.HTM67%★

☑👤📌☰

DATE 19

MARCH 25—29, 2019

FLORENCE, ITALY

FIRENZE FIERA

DESIGN, AUTOMATION AND TEST IN EUROPE THE EUROPEAN EVENT FOR



MAIN PAGE

DATE 2002

Proceedings:

Table of Content

Abstracts

Session Index

Author Index

DATE 2002 TABLE OF CONTENTS

Sessions: [\[Keynote\]](#) [\[1A\]](#) [\[1B\]](#) [\[1C\]](#) [\[1D\]](#) [\[1E\]](#) [\[2A\]](#) [\[2B\]](#) [\[2C\]](#) [\[2D\]](#) [\[2E\]](#) [\[2F\]](#) [\[3A\]](#) [\[3B\]](#) [\[3C\]](#) [\[3D\]](#) [\[3E\]](#) [\[3F\]](#) [\[4A\]](#) [\[4B\]](#) [\[4C\]](#) [\[4D\]](#) [\[4E\]](#) [\[5A\]](#) [\[5B\]](#) [\[5C\]](#) [\[5D\]](#) [\[5E\]](#) [\[6A\]](#) [\[6B\]](#) [\[6C\]](#) [\[6D\]](#) [\[6E\]](#) [\[6F\]](#) [\[7A\]](#) [\[7B\]](#) [\[7C\]](#) [\[7D\]](#) [\[7E\]](#) [\[8A\]](#) [\[8B\]](#) [\[8C\]](#) [\[8D\]](#) [\[8E\]](#) [\[9A\]](#) [\[9B\]](#) [\[9C\]](#) [\[9D\]](#) [\[9E\]](#) [\[9G\]](#) [\[10A\]](#) [\[10B\]](#) [\[10C\]](#) [\[10D\]](#) [\[10E\]](#) [\[Posters\]](#)

[DATE Executive Committee](#)

[Technical Program Chairs](#)

[Vendors Committee](#)

[DATE Sponsors Committee](#)

[Technical Program Committee](#)

[Reviewers](#)

[Welcome to DATE 2002](#)

[Best Paper Awards](#)

[Tutorials](#)

[Master Courses](#)

[Call for Papers DATE 2003](#)

Plenary — Keynote Session

Moderator: *J. da Franca, ChipIdea, PT*

On Nanoscale Integration and Gigascale Complexity in the Post .Com World [p. 12]
Hugo De Man, Professor, KU Leuven, Senior Research Fellow, IMEC, BE

Global Responsibilities in SOC Design [p. 12]
Taylor Scanlon, President & CEO, Virtual Silicon Technology, US

1A: Hot Topic — How to Choose Semiconductor IP?

Organizer: *Yervant Zorian, Virage Logic, US*

Moderator: *Nic Mokhoff, EE Times, US*



How to Choose Semiconductor IP? -- Embedded Processors [p. 14]
I. Phillips



Make Your SOC Design a Winner: Select the Right Memory IP [p. 15]
V. Ratford



How to Choose Semiconductor IP: Embedded Software [p. 16]
G. Martin



IP Day: How to Choose Semiconductor IP? [p. 17]
P. Bricaud

1B: Formal Verification of Complex Designs

Moderators: *L Fix, Intel, ISR; T. Kroopf, Bosch, DE*



Formal Verification of the Pentium 4 Floating-Point Multiplier [p. 20]
R. Kaivola and N. Narasimhan



Using Rewriting Rules and Positive Equality to Formally Verify Wide-Issue Out-of-Order Microprocessors with a Reorder Buffer [p. 28]
M. Velez



Automatic Verification of In-Order Execution In Microprocessors with Fragmented Pipelines and Multicycle Functional Units [p. 36]
P. Mishra, N. Dutt, A. Nicolau, and H. Tomiyama



A Case Study for the Verification of Complex Timed Circuits: IPCMOS [p. 44]
M. Peña, J. Cortadella, E. Pastor, and A. Smirnov

1C: Cooling Layout Arrangements

Moderators: *R.H.J.M. Otten, TU Eindhoven, NL; M.D.F. Wong, Texas U, US*



FPGA Placement by Thermodynamic Combinatorial Optimization [p. 54]
J. De Vicente, J. Lanchares, and R. Hermida



An Enhanced Q-Sequence Augmented with Empty-Room-Insertion and Parenthesis Trees [p. 61]
C. Zhuang, Y. Kajitani, K. Sakarushi, and L. Jin



Arbitrary Convex and Concave Rectilinear Module Packing Using TCG [p. 69]
J. Lin, H. Chen, and Y. Chang

1D: Defect Oriented Test

Moderators: *J. Segura, Illes Balears U, ES; H. Manhaeve, Q-Star Test, BE*



Page 7

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1039

-   A Test Design Method for Floating Gate Defects (FGD) in Analog Integrated Circuits [p. 78]
M. Pronath, H. Graeb, and K. Antreich
-   Exact Grading of Multiple Path Delay Faults [p. 84]
S. Padmanaban and S. Tragoudas
-   Modeling Techniques and Tests for Partial Faults in Memory Devices [p. 89]
Z. Al-Ars and A. van de Goor
-   A New ATPG Algorithm to Limit Test Set Size and Achieve Multiple Detections of All Faults [p. 94]
S. Lee, B. Cobb, J. Dworak, M. Grimala, and M. Mercer

1E: [Power Analysis and Management in Networks and Processors](#)

Moderators: E. Macii, Politecnico di Torino, IT; K. Roy, Purdue U, US

-   Low Power Error Resilient Encoding for On-Chip Data Buses [p. 102]
D. Bertozzi, L. Benini, and G. De Micheli
-   Managing Power Consumption in Networks on Chip [p. 110]
T. Simunic and S. Boyd
-   Competitive Analysis of Dynamic Power Management Strategies for Systems with Multiple Power Savings States [p. 117]
S. Irani, R. Gupta, and S. Shukla
-   AccuPower: An Accurate Power Estimation Tool for Superscalar Microprocessors [p. 124]
D. Ponomarev, G. Kucuk, and K. Ghose

2A: [Panel – What is the Right IP Business Model?](#)

Organizer: Y. Zorian, Virage Logic, US

Moderator: K. Bartleson, Synopsys, US

*Panellists: J. Tully, Gartner Dataquest, US; G. Toomajanian, Dain Rauscher Wessels, US;
E. Desai, Desai's Technology Research, US; M. Hosseini, WIT Soundview, US; V. Essi, AH&H, UA*

-   IP is All About Implementation and Customer Satisfaction [p. 132]
V. Essi, Jr.

2B: [SAT and BDD Techniques](#)

Moderators: T. Shiple, Synopsys, FR; R. Drechsler, Bremen U, DE

-   Using Problem Symmetry in Search Based Satisfiability Algorithms [p. 134]
E. Goldberg, M. Prasad, and R. Brayton
-   BerkMin: A Fast and Robust Sat-Solver [p. 142]
E. Goldberg and Y. Novikov
-   Dynamic Scheduling and Clustering in Symbolic Image Computation [p. 150]
G. Cabodi, P. Camurati, and S. Quer

2C: [Technology and Interconnect Issues in Low Power Design](#)

Moderators: S. Huss, TU Darmstadt, DE; D. Auvergne, LIRMM, F

-   Wire Placement for Crosstalk Energy Minimization in Address Buses [p. 158]
L. Macchiariulo, E. Macii, and M. Poncino
-   Dynamic VTH Scaling Scheme for Active Leakage Power Reduction [p. 163]
C. Kim and K. Roy
-   Profile-Based Dynamic Voltage Scheduling Using Program Checkpoints [p. 168]
A. Azevedo, I. Issenin, R. Cornea, R. Gupta, N. Dutt, A. Veidenbaum, and A. Nicolau
-   Sizing Power/Ground Meshes for Clocking and Computing Circuit Components [p. 176]
A. Mukherjee, K. Wang, L. Chen, and M. Marek-Sadowska

2D: [Advanced Mixed Signal Test](#)

Moderators: J. Huertas, CNM-IMSE, ES; B. Kaminska, Fluence Technology, US

-   A Signature Test Framework for Rapid Production Testing of RF Circuits [p. 186]
R. Voorakaranam, S. Cherubal, and A. Chatterjee
-   Analog IP Testing: Diagnosis and Optimization [p. 192]
C. Guardiani, P. McNamara, L. Daldoss, S. Saxena, S. Zanella, W. Xiang, and S. Liu
-   A New Design Flow and Testability Measure for the Generation of a Structural Test and BIST for Analogue and Mixed-Signal Circuits [p. 197]
C. Hoffmann
-   Built-In Dynamic Current Sensor for Hard-to-Detect Faults in Mixed-Signal ICs [p. 205]
Y. Lechuga, R. Mozuelos, M. Martinez, and S. Bracho

2E: [Collaborative Design – Web-Services, Infrastructure, Applications](#)

Qualcomm v. Network System Technologies

IPR2024-00338

Qualcomm Exhibit 1039

Moderators: *A. Sauer, FHG EAS/IIS, DE; A. Pavlak, ITE Warsaw, PL*

-   E-Design Based on the Reuse Paradigm [p. 214]
L. Gharni, A. Ghrab, M. Hamdoun, B. Missaoui, K. Skiba, and G. Saucier
-   Internet-Based Collaborative Test Generation with MOSCITO [p. 221]
A. Schneider, K. Diener, E. Ivask, J. Raik, R. Ubar, P. Miklos, T. Cibáková, and E. Gramatová
-   A Two-Tier Distributed Electronic Design Framework [p. 227]
T. Kazmierski and N. Clayton
-   Embedded System Design Based On Webservices [p. 232]
A. Rettberg and W. Thronicke

2F: [Panel -- Who Owns the Platform?](#)

Organizer/Moderator: *W. Wolf, Princeton U, US*
Panellists: *M. Pinto, Agers, US; P. Paulin, STMicroelectronics, CA; C. Rowen, Tensilica, US;*
O. Levia, Improv Systems, US; G. Saucier, Design-Reuse, FR; V. Gerousis, Infineon, DE

-   Who Owns the Platform? [p. 238]

3A: [Embedded Tutorial -- The Need for Infrastructure IP in SoCs](#)

Organizer: *D. Gizopoulos, Piraeus U, GR*
Moderator: *G. Smith, Gartner Dataquest, US*
Speakers: *M. Milligan, HPL Technologies, US; Y. Zorian, Virage Logic, US; S. Pateras, LogicVision, US; M. Nicolaidis, iRoC Technologies, FR*

-   IP for Embedded Robustness [p. 240]
M. Nicolaidis
-   Embedded Diagnosis IP [p. 242]
S. Pateras
-   Embedded Robustness IPs [p. 244]
E. Dupont, M. Nicolaidis, and P. Rohr

3B: [Advances in Logic Synthesis](#)

Moderators: *M. Berkelaar, Magma Design Automation, NL; W. Kuw, Kaiserslautern U, DE*

-   CHESMIN: A Heuristic for State Reduction in Incompletely Specified Finite State Machines [p. 248]
S. Gören and F. Ferguson
-   Generalized Early Evaluation in Self-Timed Circuits [p. 255]
M. Thornton, K. Fazel, R. Reese, and C. Traver
-   Dual Threshold Voltage Domino Logic Synthesis for High Performance with Noise and Power Constraint [p. 260]
S. Jung, K. Kim, and S. Kang

3C: [Novel Applications of Symbolic Techniques to Analogue and Digital Circuit Design](#)

Moderators: *F. Fernández, IMSE-CNM, ES; A. Konczykowska, Alcatel R&I, FR*

-   A Fitting Approach to Generate Symbolic Expressions for Linear and Nonlinear Analog Circuit Performance Characteristics [p. 268]
W. Daems, G. Gielen, and W. Sansen
-   Parameter Controlled Automatic Symbolic Analysis of Nonlinear Analog Circuits [p. 274]
R. Popp, J. Oehmen, L. Hedrich, and E. Barke
-   Constructing Symbolic Models for the Input/Output Behavior of Periodically Time-Varying Systems Using Harmonic Transfer Matrices [p. 279]
P. Vanasch, G. Gielen, and W. Sansen
-   Taylor Expansion Diagrams: A Compact, Canonical Representation with Applications to Symbolic Verification [p. 285]
M. Ciesielski, P. Kalla, Z. Zeng, and B. Rouzeyre

3D: [Hot Topic -- EDA Tools for RF: Myth or Reality?](#)

Organizers: *L. Guarnieri, Barcelona Design, US; E. Chen, Celestry Design Technologies, US*
Moderator: *C. Ajluni, Wireless Systems Design, US*
Presenters: *S. Savage, Cypress Semiconductors, US; M. Hershenson, Barcelona Design, US; X. Zhang, Celestry Design Technologies, US*

-   EDA Tools for RF: Myth or Reality? [p. 292]

3E: [Platform-Based Design and Virtual-Component Reuse](#)

Moderators: *W. Wolf, Princeton U, US; N. Martínez Madrid, FZI Karlsruhe, DE*

-   Dynamic Runtime Re-Scheduling Allowing Multiple Implementations of a Task for Platform-Based Designs [p. 296]
T. Lee, W. Wolf, and J. Henkel
-   Techniques to Evolve a C++ Based System Design Language [p. 302]
R. Pasko, S. Vernalde, and P. Schaumont

-   A Mixed-Signal Design Reuse Methodology Based on Parametric Behavioural Models with Non-Ideal Effects [p. 310]
A. Ginés, E. Peralías, A. Rueda, N. Madrid, and R. Seepold

3F2: [Analogue Circuit Characterisation and Simulation](#)

Moderators: A. Rodríguez-Vázquez, IMSE-CNM, ES; D. Leenaerts, Philips, NL

-   Test Structure for $I_C(V_{BE})$ Parameter Determination of Low Voltage Applications [p. 316]
W. Rahajandraibe, C. Dufaza, D. Auvergne, B. Citaldella, B. Majoux, and V. Chowdhury
-   Global Optimization Applied to the Oscillator Problem [p. 322]
S. Lamps and S. Laur

4A: [Panel – MEDEA+ and ITRS Roadmaps](#)

Organizer: W. Rosenstiel, FZI/Tuebingen U, DE

Moderator: G. Mathéron, Director of MEDEA+ Office, FR

Panelists: J. Borel, STMicroelectronics, US; G. Mathéron, MEDEA+ Office; A. Jerraya, TIMA, Grenoble, FR;

S. Resve, UC Berkeley, US; M. Rogers, Intel, US; W. Rosenstiel, FZI/Tuebingen U, DE;

I. Rugen-Herzig, Infineon Technologies, DE; F. Theeuwes, Philips Research, NL

-   MEDEA+ and ITRS Roadmaps [p. 328]

4B: [Asynchronous Circuits and Clock Scheduling](#)

Moderators: M. Renaudin, TIMA, Grenoble, FR; L. Lavagno, Politecnico di Torino, IT

-   A Burst-Mode Oriented Back-End for the Balsa Synthesis System [p. 330]
T. Chelcea, S. Nowick, A. Bardley, and D. Edwards
-   Detecting State Coding Conflicts in STGs Using Integer Programming [p. 338]
V. Khomenko, M. Koutry, and A. Yakovlev
-   Verifying Clock Schedules in the Presence of Cross Talk [p. 346]
S. Hassoun, E. Calvillo-Gómez, and C. Cromer

4C: [Analogue and Mixed-Signal Systems](#)

Moderators: A. Kaiser, ISEN, FR; P. Wambacq, IMEC, BE

-   Analysis of Nonlinearities in RF Front-End Architectures Using a Modified Volterra Series Approach [p. 352]
M. Gaffioul, P. Wambacq, G. Vandersteen, and S. Donnay
-   Systematic Design of a 200 Ms/S 8-bit Interpolating A/D Converter [p. 357]
J. Vandenbussche, E. Lauwers, K. Uytendhoe, M. Steyaert, and G. Gielen
-   Bio-Inspired Analog VLSI Design Realizes Programmable Complex Spatio-Temporal Dynamics on a Single Chip [p. 362]
R. Carmona, F. Jiménez-Garrido, R. Domínguez-Castro, S. Espejo, and A. Rodríguez-Vázquez

4D: [BIST Diagnosis and DFT](#)

Moderators: M. Flottes, LIRMM, FR; A. Benzo, Politecnico di Torino, IT

-   An Incremental Algorithm for Test Generation in Illinois Scan Architecture Based Designs [p. 368]
A. Pandey and J. Patel
-   Gate Level Fault Diagnosis in Scan-Based BIST [p. 376]
I. Bayraktaroglu and A. Orailoglu
-   An Interval-Based Diagnosis Scheme for Identifying Failing Vectors in a Scan-BIST Environment [p. 382]
C. Liu, K. Chakrabarty, and M. Goessel
-   Reducing Test Application Time Through Test Data Mutation Encoding [p. 387]
S. Reda and A. Orailoglu

4E: [Code and Memory Optimization in Co-Design](#)

Moderators: R. Leupers, TU Aachen, DE; R. Ernst, TU Braunschweig, DE

-   Hardware/Software Trade-Offs for Advanced 3G Channel Coding [p. 396]
H. Michel, A. Worm, N. Wehn, and M. Münch
-   An Efficient Compiler Technique for Code Size Reduction Using Reduced Bit-Width ISAs [p. 402]
A. Halambi, A. Shrivastava, P. Birwas, N. Dutt, and A. Nicolau
-   Assigning Program and Data Objects to Scratchpad for Energy Reduction [p. 409]
S. Steinke, L. Wehmeyer, B. Lee, and P. Marwedel

5A: [Hot Topic – Network on a Chip](#)

Moderator/Organizer: G. De Micheli, Stanford U, US

-   Networks on Chip: A New Paradigm for Systems on Chip Design [p. 418]
G. De Micheli and T. Benini

-   Communication Mechanisms for Parallel DSP Systems on a Chip [p. 420]
J. Williams, N. Heintze, and B. Ackland
-   Networks on Silicon: Combining Best-Effort and Guaranteed Services [p. 423]
K. Goossens, P. Wielage, A. Peeters, and J. van Meerbergen

5B: Low Power Architectures and Software

Moderators: W. Nebel, OFFIS, DE; M. Miranda, IMEC, BE

-   Data Reuse Exploration Techniques for Loop-Dominated Applications [p. 428]
T. Van Achteren, G. Deconinck, F. Catthoor, and R. Lauwereins
-   EAC: A Compiler Framework for High-Level Energy Estimation and Optimization [p. 436]
I. Kadayif, M. Kandemir, N. Vijaykrishnan, M. Irwin, and A. Sivasubramanian
-   Power Savings in Embedded Processors through Decode Filer Cache [p. 443]
W. Tang, R. Gupta, and A. Nicolau
-   Hardware-Assisted Data Compression for Energy Minimization in Systems with Embedded Processors [p. 449]
L. Benini, D. Bruni, A. Macii, and E. Macii

5C: Nitty Gritty Details of Layout Design

Moderators: E. Barke, Hannover U, DE; P. Groeneveld, Magma Design Automation, NL

-   Analysis of Noise Avoidance Techniques in DSM Interconnects Using a Complete Crosstalk Noise Model [p. 456]
M. Becker, V. Zolotov, D. Blaauw, R. Panda, and I. Hajj
-   Hierarchical Current Density Verification for Electromigration Analysis in Arbitrary Shaped Metallization Patterns of Analog Circuits [p. 464]
G. Jerke and J. Lienig
-   A Polynomial Time Optimal Diode Insertion/Routing Algorithm for Fixing Antenna Problem [p. 470]
L. Huang, X. Tang, H. Xiang, D. Wong, and I. Liu

5D: SoC and System Test

Moderators: Y. Zorian, LogicVision, US; D. Gizopoulos, Piraeus U, GR

-   Test Planning and Design Space Exploration in a Core-Based Environment [p. 478]
E. Cota, L. Carro, M. Lubaszewski, and A. Oratloglu
-   A Hierarchical Test Scheme for System-On-Chip Designs [p. 486]
J. Li, H. Huang, J. Chen, C. Su, C. Wu, C. Cheng, S. Chen, C. Hwang, and H. Lin
-   Efficient Wrapper/TAM Co-Optimization for Large SOCs [p. 491]
V. Iyengar, K. Chakrabarty, E. Marinissen
-   Beyond UML to an End-of-Line Functional Test Engine [p. 499]
A. Baldini, A. Benso, P. Prinetto, S. Mo, and A. Taddei

5E: Modelling and Synthesis of Embedded Systems

Moderators: J. López, Castilla-La Mancha U, ES; F. Rousseau, TIMA, Grenoble, FR

-   Event Model Interfaces for Heterogeneous System Analysis [p. 506]
K. Richter and R. Ernst
-   Energy-Efficient Mapping and Scheduling for DVS Enabled Distributed Embedded Systems [p. 514]
M. Schmitz, B. Al-Hashimi, and P. Eles
-   A Layered, Codesign Virtual Machine Approach to Modeling Computer Systems [p. 522]
J. Paul and D. Thomas
-   Automatic Evaluation of the Accuracy of Fixed-Point Algorithms [p. 529]
D. Ménard and O. Sentieys

6A: Panel -- Power Crisis in SoC Design: Strategies for Constructing Low-Power, High-Performance SoC Designs

Organizer: K. Brock, Virtual Silicon Technology, US

Moderator: C. Edwards, Electronic Times, UK

Panelists: R. Lamoo, Alcatel, BE; U. Schlichtmann, Infineon Technologies, DE; A. Domic, Synopsys, US; J. Benkoski, Monterey, US; D. Overhauser, Simplex, US; M. Kliment, Virtual Silicon, US

-   Power Crisis in SoC Design: Strategies for Constructing Low-Power, High-Performance SoC Designs [p. 538]

6B: Reconfigurable Architectures

Moderators: R. Hartenstein, Kaiserslautern U, DE; U. Kebschull, Leipzig U, DE

-   A Video Compression Case Study on a Reconfigurable VLIW Architecture [p. 540]
D. Rizzo and O. Colavin

-   A Complete Data Scheduler for Multi-Context Reconfigurable Architectures [p. 547]
M. Sánchez-Élez, M. Fernández, R. Masstre, R. Hermida, N. Bagherzadeh, and F. Kurdahi
-   Highly Scalable Dynamically Reconfigurable Systolic Ring-Architecture for DSP Applications [p. 553]
G. Sassatelli, L. Torres, P. Benoit, T. Gil, C. Diou, G. Cambon, and J. Galy
-   (Self-)reconfigurable Finite State Machines: Theory and Implementation [p. 559]
J. Teich and M. Köster

6C: [Analogue Modelling, Layout and Sizing](#)

Moderators: H. Graeb, TU Munich, DE; G. Gielen, KU Leuven, BE

-   A Linear-Centric Simulation Framework for Parametric Fluctuations [p. 568]
E. Acar, S. Nassif, and L. Pileggi
-   Automatic Generation of Common-Centroid Capacitor Arrays with Arbitrary Capacitor Ratio [p. 576]
M. Dessouky and D. Sayed
-   Analog Circuit Sizing Using Adaptive Worst-Case Parameter Sets [p. 581]
R. Schwencker, F. Schenkel, M. Pronath, and H. Graeb
-   High-Frequency Nonlinear Amplifier Model for the Efficient Evaluation of Inband Distortion Under Nonlinear Load-Pull Conditions [p. 586]
G. Vandersteen, P. Wambacq, S. Donnay, and F. Verbeyst

6D: [Test Resource Partitioning for Embedded Cores](#)

Moderators: Z. Peng, Linköping U, SE; B. Rouzeyre, LIRMM, FR

-   Effective Software Self-Test Methodology for Processor Cores [p. 592]
N. Kranitz, A. Paschalis, D. Gizopoulos, and Y. Zorian
-   Test Resource Partitioning and Reduced Pin-Count Testing Based on Test Data Compression [p. 598]
A. Chandra and K. Chakrabarty
-   Improving Compression Ratio, Area Overhead, and Test Application Time for System-on-a-Chip Test Data Compression/Decompression [p. 604]
P. Gonciari, B. Al-Hashimi, and N. Nicolici
-   Problems Due to Open Faults in the Interconnections of Self-Checking Data-Paths [p. 612]
M. Favalli and C. Metra

6E: [System Level Simulation and Modelling](#)

Moderators: B. Al-Hashimi, Southampton U, UK; P. Schwarz, FhG IIS/EAS Dresden, DE

-   Automatic Generation of Fast Timed Simulation Models for Operating Systems in SoC Design [p. 620]
S. Yoo, G. Nicosescu, L. Gauthier, and A. Jerraya
-   Window-Based Susceptance Models for Large-Scale RLC Circuit Analyses [p. 628]
Z. Zheng, L. Pileggi, M. Beattie, and B. Krauter
-   A Linear-Centric Modeling Approach to Harmonic Balance Analysis [p. 634]
P. Li and L. Pileggi
-   An Energy Estimation Method for Asynchronous Circuits with Application to an Asynchronous Microprocessor [p. 640]
P. Pérez and A. Martín

6F: [Hot Topic -- Deep Submicron Design and Timing Closure](#)

Moderator/Organizer: R. Otten, TU Eindhoven, NL

Speakers: R. Camposano, Synopsys, US; P. Groeneveld, Magma Design Automation, US; R. Otten, TU Eindhoven, NL

-   Design Automation for Deepsubmicron: Present and Future [p. 650]

7A: [Panel -- Reconfigurable SoC -- What Will it Look Like?](#)

Organizer: D. Davis, Actel, US

Moderator: B. Lewis, Gartner/Dataquest, US

Panelists: I. Bolsens, Xilinx, US; B. Gupta, STMicroelectronics, US; R. Lauwersins, IMEC, BE; Y. Tanurhan, Actel Corporation, US; C. Wheddon, Quicksilver Technology, US

-   Reconfigurable SoC . What Will it Look Like? [p. 660]

7B: [Layout Aware Logic Synthesis](#)

Moderators: A. Oliveira, INESC, PT; R. Murgai, Fujitsu Labs., US

-   Congestion-Aware Logic Synthesis [p. 664]
D. Pandini, L. Pileggi, and A. Srojewas
-   Layout Driven Decomposition with Congestion Consideration [p. 672]
T. Kutschebauch and L. Stok
-   Improving Placement under the Constant Delay Model [p. 677]
K. Sulimma, W. Kunz, I. Neumann, and L. van Ginneken

-   Crosstalk Alleviation for Dynamic PLAs [p. 683]
T. Tien, T. Tsai, and S. Chang

7C: Buffering and Tapering

Moderators: *J. Lienig, Bosch, DE; F. Johannes, TU Munich, DE*

-   Flip-Flop and Repeater Insertion for Early Interconnect Planning [p. 690]
R. Lu, G. Zhong, C. Koh, and K. Chao
-   Congestion Estimation with Buffer Planning in Floorplan Design [p. 696]
W. Wong, C. Sham, and F. Young
-   Maze Routing with Buffer Insertion under Transition Time Constraints [p. 702]
L. Huang, M. Lai, D. Wong, and Y. Gao
-   Optimal Transistor Tapering for High-Speed CMOS Circuits [p. 708]
L. Ding and P. Mazumder

7D: Automatic Design Debug and TPG

Moderators: *P. Teixeira, INESC-IST, PT; B. Straube, FHG IIS/EAS Dresden, DE*

-   Incremental Diagnosis and Correction of Multiple Faults and Errors [p. 716]
A. Veneris, J. Liu, M. Amiri, and M. Abadir
-   Test Enrichment for Path Delay Faults Using Multiple Sets of Target Faults [p. 722]
I. Pomeranz and S. Reddy
-   FACTOR: A Hierarchical Methodology for Functional Test Generation and Testability Analysis [p. 730]
V. Vedula and J. Abraham

7E: Object Oriented System Specification and Design

Moderators: *W. Grass, Passau U, DE; E. Villar, Cantabria U, ES*

-   An Environment for Dynamic Component Composition for Efficient Co-Design [p. 736]
F. Doucet, S. Shukla, R. Gupta, and M. Otsuka
-   Functional Verification for SystemC Descriptions Using Constraint Solving [p. 744]
F. Ferrandi, M. Rendine, and D. Sciuto
-   The Modelling of Embedded Systems Using HASoC [p. 752]
M. Edwards and P. Green
-   A Functional Specification Notation for Co-Design of Mixed Analog-Digital Systems [p. 760]
A. Dobol and R. Vemuri

8A: Hot Topic -- UML: Using the Unified Modeling Language for Embedded System Specification

Moderator/Organizer: *L. Lavagno, Politecnico di Torino, IT*

-   The Real-Time UML Standard: Definition and Application [p. 770]
B. Selic
-   UML for Embedded Systems Specification and Design: Motivation and Overview [p. 773]
G. Martin
-   A UML-Based Design Methodology for Real-Time and Embedded Systems [p. 776]
G. de Jong

8B: Real-Time Embedded Systems

Moderators: *Z. Peng, Linköping U, SE; J. Sifakis, VERIMAG, FR*

-   Minimum Energy Fixed-Priority Scheduling for Variable Voltage Processor [p. 782]
G. Quan and X. Hu
-   A Dynamic Voltage Scaling Algorithm for Dynamic-Priority Hard Real-Time Systems Using Slack Time Analysis [p. 788]
W. Kim, J. Kim, and S. Min
-   Extending Synchronous Languages for Generating Abstract Real-Time Models [p. 795]
G. Logothetis and K. Schneider

8C: Interconnect Modelling

Moderators: *J. Phillips, Cadence Berkeley Labs, US; L. Silveira, IST/INESC, PT*

-   An Interconnect-Aware Methodology for Analog and Mixed Signal Design, Based on High Bandwidth (Over 40 Ghz) On-Chip Transmission Line Approach [p. 804]
D. Goren, M. Zelikson, T. Galambos, R. Gordin, B. Livshitz, A. Amir, A. Sherman, and I. Wagner
-   Closed-Form Crosstalk Noise Metrics for Physical Design Applications [p. 812]
L. Chen and M. Marek-Sadowska

  Formulation of Low-Order Dominant Poles for Y-Matrix of Interconnects [p. 820]
Q. Xu and P. Mazumder

  Library Compatible CeFF for Gate-Level Timing [p. 826]
B. Sheehan

8D: [On-Line Testing and Fault Tolerance](#)

Moderators: L. Bouzaida, STMicroelectronics, FR; A. Singh, Auburn U, US

  Self-Checking Scheme for the On-Line Testing of Power Supply Noise [p. 832]
C. Metra, L. Schiano, B. Riccò, and M. Favalli

  Automatic Modifications of High Level VHDL Descriptions for Fault Detection or Tolerance [p. 837]
R. Leveugle

  Exploiting Idle Cycles for Algorithm Level Re-Computing [p. 842]
K. Wu and R. Karri

  New Techniques for Speeding-Up Fault-Injection Campaigns [p. 847]
L. Berrojo, I. González, F. Corno, M. Sonza Reorda, G. Squillero, L. Entrena, and C. López

8E: [Design Space Evaluation](#)

Moderators: J. Teich, Paderborn U, DE; W. Kruijtzter, Philips Research, NL

  System Design for Flexibility [p. 854]
C. Haubelt, J. Teich, K. Richter, and R. Ernst

  Accurate Area and Delay Estimators for FPGAs [p. 862]
A. Nayak, M. Haldar, A. Choudhary, and P. Banerjee

  A Powerful System Design Methodology Combining OCAPI and Handel-C for Concept Engineering [p. 870]
K. Buchenrieder, A. Pyttel, and A. Sedlmeier

  Automated Concurrency Re-Assignment in High Level System Models for Efficient System-Level Simulation [p. 875]
N. Savoiu, S. Shukla, and R. Gupta

9A: [Hot Topic -- From System Specification to Layout: Seamless Top-Down Design Methods for Analogue and Mixed Signal Applications](#)

Moderators/Organizers: I. Rugen-Herzig, Infineon Technologies, DE; R. Sommer, Infineon Technologies, DE

  From System Specification To Layout: Seamless Top-Down Design Methods for Analog and Mixed-Signal Applications [p. 884]
R. Sommer, I. Rugen-Herzig, E. Hennig, U. Gatti, P. Malcovati, F. Maloberti, K. Einwich, C. Clauss, P. Schwarz, and G. Noessing

9B: [Architectural Level Synthesis](#)

Moderators: P. Eles, Linköping U, SE; B. Mesman, Philips/TU Eindhoven, NL

  Memory System Connectivity Exploration [p. 894]
P. Gruen, N. Dutt, and A. Nicolau

  Performance-Area Trade-Off of Address Generators for Address Decoder-Decoupled Memory [p. 902]
S. Hettiaratchi, P. Cheung, and T. Clarke

  Multiple-Precision Circuits Allocation Independent of Data-Objects Length [p. 909]
M. Molina, J. Mendias, and R. Hermida

9C: [Advanced Linear Modelling Techniques](#)

Moderators: P. Feldmann, Celight Inc, US; G. Vandersteen, IMEC, BE

  Efficient Model Reduction of Linear Time-Varying Systems via Compressed Transient System Function [p. 916]
E. Gad and M. Nakhla

  Passive Constrained Rational Approximation Algorithm Using Nevanlinna-Pick Interpolation [p. 923]
C. Coelho, L. Silveira, and J. Phillips

  Model Reduction in the Time-Domain Using Laguerre Polynomials and Krylov Methods [p. 931]
Y. Chen, V. Balakrishnan, C. Koh, and K. Roy

9D: [Memory Testing and ATPG Issues](#)

Moderators: H. Obermeir, Infineon Technologies, DE; M. Sonza Reorda, Politecnico di Torino, IT

  An Optimal Algorithm for the Automatic Generation of March Tests [p. 938]
A. Benso, S. Di Carlo, G. Di Natale, and P. Prinetto

  Minimal Test for Coupling Faults in Word-Oriented Memories [p. 944]
A. van de Goor, M. Abadir, and A. Carlin

  Maximizing Impossibilities for Untestable Fault Identification [p. 949]

Session Index
Author Index

M. Hsiao

-   Automated Modeling of Custom Digital Circuits for Test [p. 954]
S. Bose

9E: [Embedded Software Performance Analysis and Optimization](#)

Moderators: H. Hsieh, UC Riverside, US; R. Lauwereins, IMEC, BE

-   False Path Elimination in Quasi-Static Scheduling [p. 964]
G. Arrigoni, L. Duchini, C. Passerone, L. Lavagno, and Y. Watanabe
-   A Data Analysis Method for Software Performance Prediction [p. 971]
G. Bontempi and W. Kruijtzter
-   A Code Transformation-Based Methodology for Improving I-Cache Performance of DSP Applications [p. 977]
N. Liveris, N. Zervas, D. Soudris, and C. Goutis
-   A Compiler-Based Approach for Improving Intra-Iteration Data Reuse [p. 984]
M. Kandemir

9G: [Technical Plenary -- 40 Years of EDA](#)

Moderator: A. Jerraya, TIMA, Grenoble, FR

-   European CAD from the 60's to the New Millenium [p. 992]
Joseph Borel, J.B.-R&D Consulting, FR

10A: [Hot Topic -- Design Technology for Networked Reconfigurable FPGA Platforms](#)

Organizer/Moderator: I. Bolsens, Xilinx, US Speakers: D. Verkest, IMEC, BE; S. Guccione, Xilinx, US; S. Singh, Xilinx, US

-   Design Technology for Networked Reconfigurable FPGA Platforms [p. 994]
S. Guccione, D. Verkest, and I. Bolsens

10B: [High-Level Synthesis and Asynchronous Pipelines](#)

Moderators: N. Dutt, UC Irvine, US; M. Renaudin, TIMA, Grenoble, FR

-   High-Speed Non-Linear Asynchronous Pipelines [p. 1000]
R. Ozdag, P. Beesel, M. Singh, and S. Nowick
-   Single-Track Asynchronous Pipeline Templates Using 1-of-N Encoding [p. 1008]
M. Ferretti and P. Beesel
-   Power-Manageable Scheduling Technique for Control Dominated High-Level Synthesis [p. 1016]
C. Chen and M. Sarrafzadeh
-   Practical Instruction Set Design and Compiler Retargetability Using Static Resource Models [p. 1021]
Q. Zhao, B. Mesman, and T. Basten

10C: [Coupling and Switching Noise Modelling within Integrated Circuits](#)

Moderators: E. Sicard, INSA, FR; G. Vandenbosch, KU Leuven, BE

-   Hierarchical Simulation of Substrate Coupling in Mixed-Signal ICs Considering the Power Supply Network [p. 1028]
T. Brandner and R. Weigel
-   Fast Method to Include Parasitic Coupling in Circuit Simulations [p. 1033]
B. Van Thienen and G. Vandenbosch
-   Accurate Estimating Simultaneous Switching Noises by Using Application Specific Device Modeling [p. 1038]
L. Ding and P. Mazumder
-   Macromodeling of Digital I/O Ports for System EMC Assessment [p. 1044]
I. Stievano, F. Canavero, I. Maio, Z. Chen, D. Becker, and G. Katopis

10D: [Panel -- Formal Verification Techniques: Industrial Status and Perspectives](#)

Organizer: I. Mousa, TNI-Valtoys, FR

Moderator: R. Pacalet, ENST Paris, FR

Panelists: J. Blasquez, Texas Instruments, Villeneuve-Loubet, FR; M. van Hulst, Philips, Eindhoven, NL;
A. Fedeli, STMicroelectronics, Agrate, IT; J. Lambert, TNI-Valtoys, FR; D. Borriens, TIMA-UJF, FR;
C. Hanoch, Verisity, FR; P. Bricaud, Mentor Graphics, FR

-   Formal Verification Techniques: Industrial Status and Perspectives [p. 1050]

10E: [Power Optimization for Embedded Processors](#)

Moderators: W. Fornaciari, Politecnico di Milano, IT; L. Lavagno, Politecnico di Torino, IT

-   Low Power Embedded Software Optimization Using Symbolic Algebra [p. 1052]
A. Peymandoust, T. Simunic, and G. De Micheli

-   An Adaptive Dictionary Encoding Scheme for SOC Data Buses [p. 1059]
T. Lv, W. Wolf, J. Henkel, and H. Lekatsas
-   Power Efficient Embedded Processor IP's through Application-Specific Tag Compression in Data Caches [p. 1065]
P. Petrov and A. Orailoglu
-   Systematic Power-Performance Trade-Off in MPEG-4 by Means of Selective Function Inlining Steered by Address Optimization Opportunities [p. 1072]
M. Palkovic, M. Miranda, and F. Cathoor

Poster Sessions

-   An Approach to Model Checking for Nonlinear Analog Systems [p. 1080]
W. Hartong, L. Hedrich, and E. Barks
-   Speeding up SAT for EDA [p. 1081]
S. Pilarski and G. Hu
-   Search-Based SAT Using Zero-Suppressed BDDs [p. 1082]
F. Aloul, M. Mreimneh, and K. Sakallah
-   An Encoding Technique for Low Power CMOS Implementations of Controllers [p. 1083]
M. Martinez, M. Avedillo, J. Quintana, M. Koegst, S. Rülke, and H. Süße
-   Composition Trees in Finding Best Variable Orderings for ROBDDs [p. 1084]
E. Dubrova
-   A Direct Mapping System for Datapath Module and FSM Implementation into LUT-Based FPGAs [p. 1085]
J. Abke and E. Barks
-   Concurrent and Selective Logic Extraction with Timing Consideration [p. 1086]
P. Rezvani and M. Pedram
-   Improved Technology Mapping for PAL-Based Devices Using a New Approach to Multi-Output Boolean Functions [p. 1087]
D. Kania
-   Efficient and Effective Redundancy Removal for Million-Gate Circuits [p. 1088]
M. Berkelaar and K. van Eijk
-   Visualization of Partial Order Models in VLSI Design Flow [p. 1089]
A. Bytsov, M. Koutny, and A. Yakovlev
-   High-Level Modeling and Design of Asynchronous Arbiters for On-Chip Communication Systems [p. 1090]
J. Rigaud, L. Fesquet, M. Renaudin, and J. Quartana
-   Power-Efficient Trace Caches [p. 1091]
J. Hu, N. Vijaykrishnan, M. Kandemir, and M. Irwin
-   Reducing Cache Access Energy in Array-Intensive Applications [p. 1092]
M. Kandemir and I. Kolcu
-   The Use of Runtime Configuration Capabilities for Networked Embedded Systems [p. 1093]
C. Nitsch and U. Keeschull
-   A SAT Solver Using Software and Reconfigurable Hardware [p. 1094]
I. Skliarova and A. Ferrari
-   A New Time Model for the Specification, Design, Validation and Synthesis of Embedded Real-Time Systems [p. 1095]
R. Münzenberger, M. Dörfel, F. Slomka, and R. Hofmann
-   Improved Constraints for Multiprocessor System Scheduling [p. 1096]
M. Grajcar and W. Grass
-   A Fast Johnson-Mobius Encoding Scheme for Fault Secure Binary Counters
K.S. Papadomanolakis, A.P. Kakarountas, N. Sklavos and C.E. Goutis
-   Maximizing Conditional Reuse by Pre-Synthesis Transformations [p. 1097]
O. Penalba, J. Mendias, and R. Hermida
-   Control Circuit Templates for Asynchronous Bundled-Data Pipelines [p. 1098]
S. Tugrinvizut and P. Beesel
-   Transforming Arbitrary Structures into Topologically Equivalent Slicing Structures [p. 1099]
O. Peyran and W. Zhuang
-   A New Formulation for SOC Floorplan Area Minimization Problem [p. 1100]
C. Lee, Y. Lin, W. Fu, C. Chang, and T. Hsieh
-   Non-Rectangular Shaping and Sizing of Soft Modules in Floorplan Design [p. 1101]
C. Chu and F. Young
-   EZ Encoding: A Class of Irredundant Low Power Codes for Data Address and Multiplexed Address Buses [p. 1102]
Y. Aghaghi, M. Pedram, and F. Fallah
-   Estimation of Power Consumption in Encoded Data Buses [p. 1103]
A. Garcia, L. Kabulepa, and M. Glesner

-   Optimization Techniques for Design of General and Feedback Linear Analog Amplifier with Symbolic Analysis [p. 1104]
T. Hsieh
-   Critical Comparison among Some Analog Fault Diagnosis Procedures Based on Symbolic Techniques [p. 1105]
A. Luchetta, S. Manetti, and M. Piccirilli
-   The Selective Pull-Up (SP) Noise Immunity Scheme for Dynamic Circuits [p. 1106]
M. Stan and A. Panigrahi
-   Substrate Parasitic Extraction for RF Integrated Circuits [p. 1107]
A. Cathelin, D. Saias, D. Belot, Y. Leclercq, and F. Clement
-   A Complete Phase-Locked Loop Power Consumption Model [p. 1108]
D. Duarte, N. Vijaykrishnan, and M. Irwin
-   Statistical Timing Driven Partitioning for VLSI Circuits [p. 1109]
C. Ababei and K. Bazargan
-   DAISY-CT: A High-Level Simulation Tool for Continuous-Time DeltaSigma Modulators [p. 1110]
K. Francken, M. Vogels, E. Martens, and G. Gielen
-   Automated Optimal Design of Switched-Capacitor Filters [p. 1111]
A. Hassibi and M. Hershenson
-   On-Chip Inductance Models: 3D or Not 3D? [p. 1112]
T. Lin, M. Beattie, and L. Pileggi
-   Simple and Efficient Approach for Shunt Admittance Parameters Calculations of VLSI On-Chip Interconnects on Semiconducting Substrate [p. 1113]
H. Tmeri, B. Nauwelaers, K. Maex, D. De Roest, M. Stucchi, and S. Vandenberghoe
-   Compact Macromodel for Lossy Coupled Transmission Lines [p. 1114]
R. Khazaka and M. Nakhla
-   An EMC-Compliant Design Method of High-Density Integrated Circuits [p. 1115]
J. Levant and M. Ramdani
-   Finding a Common Fault Response for Diagnosis during Silicon Debug [p. 1116]
I. Pomeranz, J. Rajski, and S. Reddy
-   IDD_T Testing of Embedded CMOS SRAMs [p. 1117]
S. Kumar, R. Makki, and D. Binkley
-   Fault Detection and Diagnosis Using Wavelet Based Transient Current Analysis [p. 1118]
S. Bhunia and K. Roy
-   An Efficient Test and Diagnosis Scheme for the Feedback Type of Analog Circuits with Minimal Added Circuits [p. 1119]
J. Lin, C. Lee, and J. Chen
-   On the Use of an Oscillation-Based Test Methodology for CMOS Micro-Electro-Mechanical Systems [p. 1120]
V. Beroulle, Y. Bertrand, L. Latorre, and P. Nouet
-   Directed-Binary Search in Logic BIST Diagnostics [p. 1121]
R. Kapur, T. Williams, M. Mercer
-   An Evolutionary Approach to the Design of On-Chip Pseudorandom Test Pattern Generators [p. 1122]
M. Favalli and M. Dalpasso
-   Fault Isolation Using Tests for Non-Isolated Blocks [p. 1123]
I. Pomeranz and Y. Zorian
-   A Heuristic for Test Scheduling at System Level [p. 1124]
M. Flottes, J. Pouget, and B. Rouzeyre
-   Formulation of SOC Test Scheduling as a Network Transportation Problem [p. 1125]
S. Koranne and V. Choudhary
-   A Novel Methodology for the Concurrent Test of Partial and Dynamically Reconfigurable SRAM-Based FPGAs [p. 1126]
M. Gericota, G. Alves, M. Silva, and J. Ferreira
-   Efficient On-Line Testing Method for a Floating-Point Iterative Array Divider [p. 1127]
A. Drozd, M. Lobachev, and J. Drozd
-   An Instruction-Level Methodology for Power Estimation and Optimization of Embedded VLIW Cores [p. 1128]
A. Bona, M. Sami, D. Sciuto, V. Zaccaria, C. Silvano, and R. Zafalon
-   The Fraunhofer Knowledge Network (FKN) for Training in Critical Design Disciplines [p. 1129]
A. Sauer, G. Elst, L. Krahn, and W. John
-   Comparative Analysis and Application of Data Repository Infrastructure for Collaboration-Enabled Distributed Design Environments [p. 1130]
L. Indruciak, M. Glesner, and R. Reis
-   FlexBench: Reuse of Verification IP to Increase Productivity [p. 1131]
S. Stöhr, M. Simmons, and J. Geisbauer
-   Mappability Estimation of Architecture and Algorithm [p. 1132]
J. Soininen, J. Kreku, and Y. Qu

-   Behavioural Modelling of Operational Amplifier Faults Using VHDL-AMS [p. 1133]
P. Wilson, J. Ross, M. Zvolinski, A. Brown, and Y. Kiliç
-   A Parallel LCC Simulation System [p. 1134]
K. Hering
-   Error Simulation Based on the SystemC Design Description Language [p. 1135]
F. Bruschi, M. Chiamanti, F. Ferrandi, and D. Sciuto
-   Towards a Kernel Language for Heterogeneous Computing [p. 1136]
D. Björklund and J. Lilius
-   Top-Down System Level Design Methodology Using SpecC, VCC and SystemC [p. 1137]
L. Cai, D. Gajski, P. Krutzinger, and M. Olivares
-   Automatic Topology-Based Identification of Instruction-Set Extensions for Embedded Processors [p. 1138]
L. Pozzi, M. Vuletic, and P. Ierns
-   Steady State Calculation of Oscillators Using Continuation Methods [p. 1139]

ally static (circuit switching) and local scheduling dynamic (packet switching). Performance guarantees (i.e. absolute certainty instead of probabilistic behaviour) are more easily given for global static scheduling than for local dynamic scheduling. The way packets are buffered and scheduled in routers, and the effects on performance guarantees has been the subject of intense research. Fundamentally, sharing and guarantees are conflicting, and efficiently combining guaranteed traffic with best-effort traffic is hard [7].

Second, programmable wires may be slower than using dedicated IP-to-IP wires, which may contain some buffers. In a NOS a packet must traverse a number of routers. When scheduling statically, a packet need not incur more than a pipeline delay per hop. But for dynamic scheduling the header of each packet must be inspected before it can be sent to the appropriate output port. Contention and congestion may further delay a packet. Finally, a packet header uses some of the communication bandwidth.

Although a NOS based on packet-switching has its costs (packetisation, routers, buffering, harder to give guarantees) it is essential for an IP re-use strategy because it enables compositional and scalable integration of the IPs. Moreover, a NOS infrastructure (such as routers and protocol stack) can be re-used and its design cost amortised over multiple designs.

The issues raised in this section can be mapped to the OSI protocol stack [4]. Below we discuss the three lower layers that are specific to the hardware architecture of the network.

The *physical layer* defines how a single bit is sent over a physical medium (such as a wire, bus, optical link, radio waves). For a NOS it deals with signal voltages and slopes, wire sizing, etc. of inter-router wires. The preceding discussions motivate why a router-based NOS eases the implementation of the physical on-chip wires.

The *data-link layer* ensures reliable (lossless, fault-free) communication over a single data link. It considers cross-talk and fault-tolerance (both transient soft errors and hard errors). For shared and especially broad-cast media (such as busses), the medium access sublayer deals with contention for the link. Examples are bus arbitration, and router-to-router flow control.

The *network layer* has two main functions for a given network. First, delivering packets, more specifically, routing, congestion control, and scheduling over multiple links. Second, network management, including accounting, monitoring, management or steering, and internetworking.

3. Guaranteed Services are essential

In this section we discuss the remainder of the OSI protocol stack, and then show why the services offered by this stack

passing, shared memory, etc.) [8]. Thus the interconnecting network has to be flexible, in terms of the services that it offers. This is the task of the top four OSI layers. They are independent of the network hardware architecture, *end to end* (the network is transparent), and *peer to peer* (between entities at the same level of abstraction, such as task to task). We now list these layers, starting with the lowest.

The aim of the *transport layer* is to provide reliable *end-to-end services over connections*, through packetisation, end-to-end connection management (perhaps over multiple networks), (de)multiplexing multiple transport connections over network connections, and so on. Examples of services per connection are: uncorrupted transmission, lossless transmission, in-order delivery, throughput, jitter (delay variation), and latency. Flow control avoids data loss by aligning IP production and consumption rates.

In the *session layer* multiple connections are combined into services such as multicast, half duplex and full duplex connections. Synchronisation of multiple connections (of audio and video streams, for example), and token management for mutual exclusion and atomic (chains of) transactions (e.g. test and set, swap) may also be offered.

The *presentation layer* converts the application view on data to a view more appropriate for transport and vice versa. Examples are encryption and endian-ness conversions.

In the *application layer* communication is natural to applications, running on IPs. This could be bit streams obeying the MP3 standard, video frames, or Java byte code.

We now return to the question of programming. A NOS consists of a set of IPs and a NOS that must be (dynamically) *configured*. For a given user function, computation is mapped to functional IPs (e.g. tasks to processors) and communication to the NOS. The number of configurations can be large and they may be generated at run-time by an application manager. To avoid unnecessary design iterations, we need to be sure of correctness of the combination of static hardware (the IPs and their interconnect) and dynamic software (the configurations) as early as possible in the design flow. Programming must be predictable; this can be ensured by basing it on a NOS that offers guaranteed services.

A NOS with guaranteed services simplifies programming individual IPs in three ways. First, some IPs have inherent performance requirements, such as a minimum throughput (for real-time streaming data), or bounded latency (for interrupts). A NOS with guaranteed services eases their integration. Second, an IP communicates using the NOS. Requests for services make its assumptions and dependencies on the NOS explicit, structuring the design and programming of the IP. Third, an IP can also be simpler when using guaranteed

2

services because it has fewer possible interactions (a stricter contract) with its environment. A service request may be granted or denied by the network. Communication failures are therefore restricted to the configuration phase of the IP, instead of every communication action, so simplifying the IP's programming model.

Guaranteed services offer the following advantages for the composition of IPs. First, services that are guaranteed to an IP are not affected by other IPs in the network, making reasoning about the IP in isolation possible. This is essential for a *compositional construction* (design and programming) of SOSs. When IPs, assumed to be correct, are combined in a system it must be clear that the system will function as a whole. This holds both at the time of design and at run time. Current systems often fail this requirement. Consider a bus; adding an IP influences the electrical parameters (like load) of the bus, as well as the existing traffic patterns. The latter can seriously affect cache behaviour and hence embedded processor performance. Second, a NOS that offers guaranteed services must accurately model its resources to offer those services. This makes costs of the NOS explicit early in the design of a SOS. At run-time an application or quality-of-service manager reconfigures the SOS. This can only be effective when the NOS is observable and controllable, but above all, predictable in terms of performance and cost. Third, a NOS

use time-division-multiplexed circuit switching. Routers use virtual output queuing for BE traffic. GT traffic is tightly scheduled to minimise buffering. Routers do not drop or reorder packets, the former due to fine-grain link-level flow control. A variant of the iSLIP switch-scheduling algorithm [6] is used for BE traffic. BE traffic use all spare capacity in the network, i.e. bandwidth that is not reserved or unused by GT traffic. Network interfaces implement multipath and multi-channel ordering, and channel flow control.

5. Conclusions

In the IP re-use model communication between the many IP cores is key. We have shown that a network on silicon (NOS) eases the design of systems on silicon (SOSs) at the levels of hardware design and software programming.

A NOS hardware architecture based on a packet-switched router network allows average-case wire dimensioning, and reduces wire congestion around IPs. It breaks the fatal global timing closure loop by separating inter-IP from intra-IP communication, and can so reduce global design iterations. The OSI protocol stack structures the communication complexity in the router network (the physical to network layers) and the programming model (the transport to application layers).

While a protocol stack offers diverse services on a single hardware architecture, we show that predictability, in the

based on guaranteed services concentrates communication failures to (re)configuration points. When the NOS declines a service request from an IP, only that IP is affected. Fall-back strategies are much easier for local configuration-time failure than for global failure at any point caused by any of the communicating parties.

4. The Æthereal Network-on-Silicon

The ÆTHEREAL NOS intends to support both guaranteed and best-effort services. We can only list some salient features here, to indicate our current direction.

We use a combination of circuit and packet switching, in the spirit of ATM [1]. A channel implements a simplex point-to-point communication between two network interfaces (possibly with multiple paths). A channel can have a combined throughput and latency guarantee (GT), or be best effort (BE), with an unspecified finite latency upper bound. Delivery order is not guaranteed over different paths or channels. A connection combines multiple channels and can include flow control and reordering for lossless in-order (multicast) transmission. The programming model is concurrent and distributed: IPs can set up and remove connections in a pipelined fashion, and at the same time. Configurations that have been computed off-line can be efficiently loaded and extended or changed at run time. GT channels are created and removed with BE packets that reserve a path through the network, subject to resource availability.

BE packets use worm-hole source routing, and GT streams

form of guaranteed services, greatly benefits programming a SOS at two levels. Individual IPs with real-time requirements are more easily integrated, and the NOS's actions are restricted by the contract, simplifying the IP's IO. At the NOS level, programming of IPs is compositional because their services are independent of each other. Quality-of-service managers can effectively observe and steer a NOS because it behaves predictably in terms of performance and cost.

We believe that a NOS must be a synthesis of hardware architecture and software programming model with guaranteed services at its core. In the ÆTHEREAL NOS we aim to do so efficiently.

References

- [1] ATM Forum. *ATM User-Network Interface Specification*. 1994
- [2] R. E. Bryant, et al. Limitations and challenges of computer-aided design technology for CMOS VLSI. *Proc. of the IEEE*, 89(3):341–365, March 2001.
- [3] W. J. Dally and B. Towles. Route packets, not wires: On-chip interconnection networks. In *DAC*, pages 684–689, June 2001.
- [4] J. D. Day and H. Zimmerman. The OSI reference model. In *Proceedings of the IEEE*, volume 71, pages 1334–1340, 1983.
- [5] P. Guerrier. *Un Réseau D'Interconnexion pour Systèmes Intégrés*. PhD thesis, Université Paris vi, Mar. 2000.
- [6] N. McKeown. iSLIP: A scheduling algorithm for input-queued switches. *IEEE Transactions on Networking*, 7(2), Apr. 1999.
- [7] J. Rexford and K. G. Shin. Support for multiple classes of traffic in multicomputer routers. In *LNCSS* 853, 1994.
- [8] M. Sgroi, et al. Addressing the system-on-a-chip interconnect woes through communication-based design. In *DAC'2001*