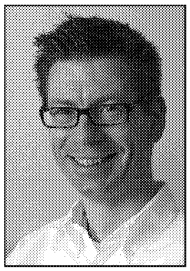

Home
Contact
Research
Publications
Students
Teaching
Mountains
MTB

Kees Goossens's Publications Page

Skip to

- overview
- network-on-chip papers
- theorem-proving papers
- technical notes
- Aethereal press coverage

Here is a list of my publications, in reverse chronological order. Note that the copyright on some of the files below may not be owned by me, please comply with the owner's conditions. Files are provided to allow browsing of documents, much like in a paper library. Let me know if you have problems retrieving a file.

To get started

- network-on-chip architecture and design flow
  - Aethereal overview
  - router with both guaranteed and best-effort service or with guaranteed service only
  - network interface
  - design flow
  - use cases
  - mapping and routing
  - configuration
- composability and predictability
  Composability is also known as performance virtualisation for independent development of applications.
  Predictability is also known as hard or firm real time.
  - real-time memory controller
  - real-time arbiter
  - composable arbiter
  - real time and low power
- network-on-chip applications
  - monitoring and debug

NST_Q0003645

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

- monitoring and debug
  - monitoring and monitoring and design flows
  - communication-centric debug
- digital TV; set-top box; DVB-T
- hardwired network on chip in FPGA
- network on chip as a test access mechanism (TAM)
- network on chip as internet router switch fabric

Journal and conference papers and book chapters

1. **"Efficient multicast support in buffered crossbars using networks on chip"**
   Iria Varela Senin, Lotfi Mhamdi, and Kees Goossens.
   In Proc. Global Telecommunications Conference, December 2009.
   bibtex
2. **"An on-chip interconnect and protocol stack for multiple communication paradigms and programming models"**
   Andreas Hansson and Kees Goossens.
   In Int'l Conf. on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2009.
   bibtex
3. **"Dynamic Workload Peak Detection For Slack Management"**
   Aleksandar Milutinovic, Kees Goossens, and Gerard Smit.
   In Proc. Int'l Symposium on Systems on Chip (SoC), October 2009.
   bibtex
4. **"Multi-Path Routing in Time-Division-Multiplexed**

NST_Q0003646

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

Networks on Chip"
Radu Stefan and Kees Goossens.
In Proc. IFIP Int'l Conference on Very Large Scale Integration (VLSI-SoC), October 2009.
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5. **"Efficient Service Allocation in Hardware Using Credit-Controlled Static-Priority Arbitration"**
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In Proc. Embedded and Real-Time Computing Systems and Applications (RTCSA), August 2009.
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6. **"Conservative dynamic energy management for real-time dataflow applications mapped on multiple processors"**
Anca Molnos and Kees Goossens.
In Proc. Euromicro Symposium on Digital System Design (DSD), August 2009.
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7. **"Composable resource sharing based on latency-rate servers"**
Benny Akesson, Andreas Hansson, and Kees Goossens.
In Proc. Euromicro Symposium on Digital System Design (DSD), August 2009.
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8. **"Internet-router buffered crossbars based on networks on chip"**
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9. **"A network-on-chip monitoring infrastructure for communication-centric debug of embedded multi-processor SoCs"**
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10. **"Modeling reconfiguration**

NST_Q0003647

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

10. **"Modeling reconfiguration in a FPGA with a hardwired network on chip"**
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11. **"aelite: A Flit-Synchronous Network on Chip with Composable and Predictable Services"**
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In Proc. Design, Automation and Test in Europe Conference and Exhibition (DATE), April 2009.
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12. **"A High-Level Debug Environment for Communication-Centric Debug"**
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13. **"Enabling Application-Level Performance Guarantees in Network-Based Systems on Chip by Applying Dataflow Analysis"**
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In IET Computers & Digital Techniques, 2009.
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14. **"CoMPSoC: A template for composable and predictable multi-processor system on chips"**
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NST_Q0003648

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003649

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003650

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003651

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003652

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003653

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003654

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003655

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003656

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003657

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IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003658

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003659

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003660

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IPR2024-00338
Qualcomm Exhibit 1040

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NST_Q0003661

Qualcomm v. Network System Technologies
IPR2024-00338
Qualcomm Exhibit 1040

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Qualcomm v. Network System Technologies
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Qualcomm Exhibit 1040

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Press coverage

- Networks on Processors Improve On-Chip Communications, David Geer. Computer Volume 42, Issue 3, March 2009. DOI
- Nikkei Microdevices coverage of DATE 2006 (in Japanese).
- NE Asia Online coverage of DATE 2006.

  Investigating NoCs In addition to the SPIRIT announcement, Philips Research Laboratories also presented the results of an investigation into the utility of using network-on-chip (NoC) technology to interconnect multiple ICs. NoC technology is viewed as a replacement to the on-chip bus, and offers advantages such as the ability to interconnect multiple IP cores, and increased data freedom in handling data between IP cores. Compared to a bus, however, it also suffers penalties in terms of chip area and dissipation. Philips Research Labs redesigned an existing bus-type application-specific IC (ASIC) for TVs to use NoC technology, and evaluated the resulting disadvantages. The change from bus to NoC increased chip area by 4.4%, and the 300MHz operating frequency of the NoC region increased dissipation by 10.8%. When the network configuration was changed from 2x2 to 1x3, however, the operating frequency of the NoC region dropped to 160MHz, with an increase in dissipation of only 5.4%. The 1x3 configuration does reduce the degree of network freedom, however.

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According to Kees Goossens of Philips Research Labs, the investigation indicated that the penalty is sufficiently low. As a result, designer interest in NoCs is rising, and he commented that the development of the first SoCs using NoC technology would be started in 2007.

- EETimes coverage of MPSOC 2005
- EE times coverage of DATE 2005

In developing its Aethereal Network-on-Silicon (NoS), Philips decided to use a combination of circuit and packing switching, a la asynchronous transfer mode, to enable communications between IP blocks. Philips managers described NoS as "a hardware architecture with a programming model based on the OSI reference model, which allows the structuring of communication complexity from the physical implementation up to the application in a number of layers." In this way a communications-centric architecture in an SoC can be used to serve numerous specific applications, possibly leading one day to an entire application-specific SoC industry.

- August 2003 Nikkei Microdevices Aethereal coverage (in Japanese)

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