PTO/SB/14 (08-05)
Approved for use through 07/31/2006. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL 040529
	Application Number	
Title of Invention	INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Andrei		RADULESCU	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Eindhoven	Country Of Residence[i]	NL
Citizenship under 37 CFR 1.41(b)[i]	NL		

Mailing Address of Applicant:

Address 1	Prof. Holstlaan 6		
Address 2			
City	Eindhoven	State/Province	
Postal Code	5656 AA	Country[i]	NL

Applicant 2 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kees	Gerard Willem	GOOSSENS	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Eindhoven	Country Of Residence[i]	NL
Citizenship under 37 CFR 1.41(b)[i]	NL		

Mailing Address of Applicant:

Address 1	Prof. Holstlaan 6		
Address 2			
City	Eindhoven	State/Province	
Postal Code	5656 AA	Country[i]	NL

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL 040529
	Application Number	
Title of Invention	INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS	

Customer Number	24737		
Email Address	jeanne.rusciano@philips.com	Add Email	Remove Email

Application Information:

Title of the Invention	INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS		
Attorney Docket Number	NL 040529	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter			
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	
Publication Information:			
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)			
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not been and will not be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.			

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ US Representative (37 CFR 11.9)
Customer Number	24737		

Domestic Priority Information:

This section allows for the applicant to claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c). Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Priority Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

PTO/SB/14 (08-05)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL 040529
	Application Number	
Title of Invention	INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS	

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
04102189.0	EP	2004-05-18	(•) Yes ( ) No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Remove

Assignee 1

If the Assignee is an Organization check here. [X]

Organization Name	KONINKLIJKE PHILIPS ELECTRONICS, N.V.		
Mailing Address Information:			
Address 1	GROENEWOUDSEWEG 1		
Address 2			
City	EINDHOVEN	**State/Province**	
Country [i]	NL	Postal Code	5621 BA
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the **Add** button. Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Michael E. Marion/			Date (YYYY-MM-DD)	2006-11-02
First Name	Michael E.	Last Name	Marion	Registration Number	32266

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY (includes Reference to PCT International Applications)	ATTORNEY'S DOCKET NUMBER **PHNL040529 US**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention the specification of which (check only one item below):

☐ entitled:

☐ is attached hereto.

☐ was filed as United States application

Serial No

on

and was amended

on

☒ was filed as PCT international application

Number PCT/IB2005/051580

on 13 May 2005

and was amended under PCT Article 19

on (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C.119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or of any PCT international application having a filing date before that of the application of which priority is claimed.

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. 119:

COUNTRY	APPLICATION NUMBER	DATE OF FILING DAY, MONTH, YEAR	PRIORITY CLAIMED UNDER 35 USC 119
Europe	**04102189.0**	**18 May 2004**	**YES**

Combined Declaration For Patent Application and Power of Attorney (Continued) (includes Reference to PCT International Applications)	Attorneys Docket Number **PHNL040529 US**

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)

Jack E. Haken, Reg. No. 26,902 Michael E. Marion, Reg. No. 32, 266 Edward M. Blocker, Reg. No. 30,245	Direct Telephone Calls to: (name and telephone number) (914)332-0222

201	FULL NAME OF INVENTOR	FAMILY NAME **RADULESCU**	FIRST GIVEN NAME **Andrei**	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY **Eindhoven**	STATE OR FOREIGN COUNTRY **The Netherlands**	COUNTRY OF CITIZENSHIP **Romania**
	POST OFFICE ADDRESS	POST OFFICE ADDRESS **Prof. Holstlaan 6**	CITY **5656 AA Eindhoven**	STATE & ZIP CODE/COUNTRY **The Netherlands**
202	FULL NAME OF INVENTOR	FAMILY NAME **GOOSSENS**	FIRST GIVEN NAME **Kees**	SECOND GIVEN NAME **Gerard Willem**
	RESIDENCE & CITIZENSHIP	CITY **Eindhoven**	STATE OR FOREIGN COUNTRY **The Netherlands**	COUNTRY OF CITIZENSHIP **The Netherlands**
	POST OFFICE ADDRESS	POST OFFICE ADDRESS **Prof. Holstlaan 6**	CITY **5656 AA Eindhoven**	STATE & ZIP CODE/COUNTRY **The Netherlands**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true: and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United states Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202
DATE 08 December 2005	DATE 08 December 2005

U.S. DEPARTMENT OF COMMERCE- Patent and Trademarks Office

(July 1994)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Atty. Docket
RADULESCU et al.	NL 040529
Serial No.	Group Art Unit
Filed: CONCURRENTLY	Ex.

INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

Commissioner for Patents
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

1. (original) Integrated circuit having a plurality of processing modules (M, S) being connected with an interconnect means (N), wherein a first processing module (M) communicates to a second processing module (S) using transactions, comprising:

- a first wrapper means (WM1) associated to said second processing module (S) for buffering data from said second processing module (S) to be transferred over the interconnect means (N) until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered.

2. (original) Integrated circuit according to claim 1, further comprising:

- a second wrapper means (WM2) associated to said first processing module (M) for buffering data from said first processing module (M) to be transferred over the interconnect means (N) until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered.

3. (currently amended) Integrated circuit according to claim 1~~or 2~~, wherein

- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data in response to a first and second unbuffer signal or a first and second combination of a group of signals, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

4. (currently amended) Integrated circuit according to claim 1~~or 2~~, wherein

- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data according to a first and second unbuffer flag, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

5. (currently amended) Integrated circuit according to claim 1~~or 2~~, wherein

- at least one of said first and second wrapper means (WM1, WM2) comprises a determination unit (BLDU1, BLDU2) for determining the optimal first or second amount of data to be buffered according to

communication properties of the communication between said first and second processing module (M, S).

6. (currently amended) Integrated circuit according to claim 1~~or 2~~, wherein

- at least one of said first and second wrapper means (WM1, WM2) comprises a determination unit (BLDU1, BLDU2) for determining the optimal moment for sending the data in said first or second wrapper means (WM1, WM2) according to communication properties of the communication between said first and second processing module (M, S).

7. (original) Integrated circuit according to claim 3, wherein

- said first unbuffer signal is initiated by said second processing module (S) and said second unbuffer signal is initiated by said first processing module (M).

8. (original) Integrated circuit according to claim 4, wherein

- the setting of said first unbuffer flag is initiated by said second processing module (S) and the setting of said second unbuffer flag is initiated by said first processing module (M).

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Page 10

9. (currently amended) Integrated circuit according to claim 3~~or 4~~, wherein

- said first processing module (M) is adapted to initiate said first and/or said second unbuffer signal.

10. (original) Integrated circuit according to claim 4, wherein

- said first processing module (M) is adapted to initiate the setting of said first and/or second unbuffer flag.

11. (currently amended) Integrated circuit according to claim 1 ~~or 2~~, wherein

- said first and second processing modules (M, S) communicate with each other using a message-passing communication scheme, wherein the messages contain message header,

- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

12. (currently amended) Integrated circuit according to claim 1 ~~or 2~~, wherein

- said first and second processing modules (M, S) communicate

with each other using a packet based communication scheme, wherein the packets contain packet header,

- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

13. (original) Method for buffering data in an integrated circuit having a plurality of processing modules (M, S) being connected with an interconnect means (N), wherein a first processing module (M) communicates to a second processing module (S) using transactions, comprising the steps of:

- buffering data from said second processing module (S) to be transferred over the interconnect means (N) until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered.

14. (original) Data processing system, comprising:

- a plurality of processing modules (M, S) being connected with an interconnect means (N), wherein a first processing module (M) communicates to a second processing module (S) using transactions, comprising:

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Page 12

- a first wrapper means (WM1) associated to said second processing module (S) for buffering data from said second processing module (S) to be transferred over the interconnect means (N) until a first amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered.

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Page 13

REMARKS

The foregoing amendments to the claims were made solely to avoid filing the claims in the multiple dependent form so as to avoid the additional filing fee.

The amendment to the claims does not address issues of patentability and Applicants respectfully reserve all rights they may have under the Doctrine of Equivalents. Applicants furthermore reserve their right to reintroduce subject matter deleted herein at a later time during the prosecution of this application or continuing applications.

Respectfully submitted,

By 
Edward W. Goodman, Reg. 28,613
Attorney
(914) 333-9611

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS
First Named Inventor/Applicant Name:	Andrei RADULESCU
Filer:	Michael E. Marion/Jeanne Rusciano
Attorney Docket Number:	NL040529

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
National Stage Fee	1631	1	300	300
Natl Stage Search Fee - Report provided	1642	1	400	400
National Stage Exam - all other cases	1633	1	200	200
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**900**

Electronic Acknowledgement Receipt

EFS ID:	1311760
Application Number:	11569083
International Application Number:	PCT/IB05/51580
Confirmation Number:	4172
Title of Invention:	INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS
First Named Inventor/Applicant Name:	Andrei RADULESCU
Customer Number:	24737
Filer:	Michael E. Marion/Jeanne Rusciano
Filer Authorized By:	Michael E. Marion
Attorney Docket Number:	NL040529
Receipt Date:	14-NOV-2006
Filing Date:	
Time Stamp:	12:26:43
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$900
RAM confirmation Number	1464
Deposit Account	141270
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	nl040529ADS.pdf	1089479	no	4
Warnings:					
Information:					
2	Oath or Declaration filed	nl040529dec.pdf	118870	no	2
Warnings:					
Information:					
3		NL040529PRELIM.PDF	226287	yes	8

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Claims	2	7
Applicant Arguments/Remarks Made in an Amendment	8	8

Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	8475	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1443111		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

Electronic Acknowledgement Receipt

EFS ID:	1311760
Application Number:	11569083
International Application Number:	PCT/IB05/51580
Confirmation Number:	4172
Title of Invention:	INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS
First Named Inventor/Applicant Name:	Andrei RADULESCU
Customer Number:	24737
Filer:	Michael E. Marion/Jeanne Rusciano
Filer Authorized By:	Michael E. Marion
Attorney Docket Number:	NL040529
Receipt Date:	14-NOV-2006
Filing Date:	
Time Stamp:	12:26:43
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	$900
RAM confirmation Number	1464
Deposit Account	141270
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	nl040529ADS.pdf	1089479	no	4
Warnings:					
Information:					
2	Oath or Declaration filed	nl040529dec.pdf	118870	no	2
Warnings:					
Information:					
3		NL040529PRELIM.PDF	226287	yes	8

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Claims	2	7
Applicant Arguments/Remarks Made in an Amendment	8	8

Warnings:	
Information:	
4	Fee Worksheet (PTO-875)	fee-info.pdf	8475	no	2
Warnings:					
Information:					
Total Files Size (in bytes):	1443111				

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 November 2005 (24.11.2005)

PCT

(10) International Publication Number
WO 2005/111823 A1

(51) International Patent Classification[7]: G06F 13/42

(21) International Application Number:
PCT/IB2005/051580

(22) International Filing Date: 13 May 2005 (13.05.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
04102189.0 18 May 2004 (18.05.2004) EP

(71) Applicant *(for all designated States except US)*: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

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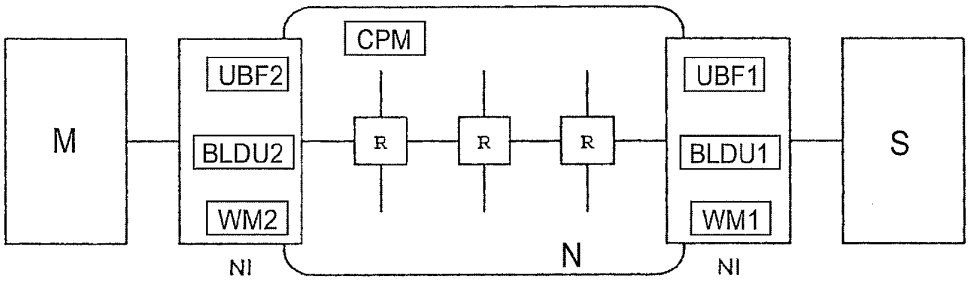
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(54) Title: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS



(57) Abstract: An integrated circuit comprising a plurality of processing modules (M, S) coupled by an interconnect means (N) is provided. A first processing module (M) communicates with a second processing module (S) based on transactions. A first wrapper means (WM1) associated to said second processing module (S) buffers data from said second processing module (S) to be transferred over said interconnect means until a first amount of data is buffered and then transfers said first amount of buffered data to said first processing module (M).

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INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGHT IN NETWORKS ON CHIPS

FIELD OF THE INVENTION

The invention relates to an integrated circuit having a plurality of processing modules and an interconnect means for coupling said plurality of processing, a method for buffering and a data processing system.

BACKGROUND OF THE INVENTION

Systems on silicon show a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions. This is enabled by the increasing density with which components can be integrated on an integrated circuit. At the same time the clock speed at which circuits are operated tends to increase too. The higher clock speed in combination with the increased density of components has reduced the area which can operate synchronously within the same clock domain. This has created the need for a modular approach. According to such an approach the processing system comprises a plurality of relatively independent, complex modules. In conventional processing systems the systems modules usually communicate to each other via a bus. As the number of modules increases however, this way of communication is no longer practical for the following reasons. On the one hand the large number of modules forms a too high bus load. On the other hand the bus forms a communication bottleneck as it enables only one device to send data to the bus.

A communication network forms an effective way to overcome these disadvantages. Networks on chip (NoC) have received considerable attention recently as a solution to the interconnect problem in highly-complex chips. The reason is twofold. First, NoCs help resolve the electrical problems in new deep-submicron technologies, as they structure and manage global wires. At the same time they share wires, lowering their number and increasing their utilization. NoCs can also be energy efficient and reliable and are scalable compared to buses. Second, NoCs also decouple computation from communication, which is essential in managing the design of billion-transistor chips. NoCs achieve this decoupling because they are traditionally designed using protocol stacks, which provide well-defined interfaces separating communication service usage from service implementation.

Using networks for on-chip communication when designing systems on chip (SoC), however, raises a number of new issues that must be taken into account. This is because, in contrast to existing on-chip interconnects (e.g., buses, switches, or point-to-point wires), where the communicating modules are directly connected, in a NoC the modules communicate remotely via network nodes. As a result, interconnect arbitration changes from centralized to distributed, and issues like out-of order transactions, higher latencies, and end-to-end flow control must be handled either by the intellectual property blocks (IP) or by the network.

Most of these topics have been already the subject of research in the field of local and wide area networks (computer networks) and as an interconnect for parallel machine interconnect networks. Both are very much related to on-chip networks, and many of the results in those fields are also applicable on chip. However, NoC's premises are different from off-chip networks, and, therefore, most of the network design choices must be reevaluated. On-chip networks have different properties (e.g., tighter link synchronization) and constraints (e.g., higher memory cost) leading to different design choices, which ultimately affect the network services.

Introducing networks as on-chip interconnects radically changes the communication when compared to direct interconnects, such as buses or switches. This is because of the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes. This is in contrast with the prevalent existing interconnects (i.e., buses) where modules are directly connected.

Modern on-chip communication protocols (e.g., Device Transaction Level DTL and AXI-Protocol) operate on a split and pipelined basis with transactions consisting of a request and a response, and the bus is released for use by others after a request issued by a master is accepted by a corresponding slave. Split pipelined communication protocols are used especially in multi-hop interconnects (e.g., networks on chip, or buses with bridges), allowing an efficient utilization of the interconnect. The efficiently of a split bus can be increased for cases where a response generation at the slave is time consuming. On a pipelined protocol, a master is allowed to have multiple outstanding requests (i.e., requests for which the response is pending or expected).

The above-mentioned protocols are designed to operate at a device level, as opposed to a system or interconnect level. In other words they are designed to be independent of the actual interconnect implementation (e.g., arbitration signals are not visible) allowing the reuse of intellectual property blocks IP and their earlier integration.

In particular, the above-mentioned on-chip communication protocols comprise four main groups of signals, namely commands (or address), write data, read data and write response. The command group consists of command, addresses and command flags like burst length and mask. The command and write data groups are driven by the initiator to the target. The read data and write response are driven by the target to the initiator following a command from an initiator. All four groups are independent of each other with some ordering constraints between them, e.g. a response cannot be issued before a command.

These on-chip communication protocols also implement the concept of buffering data which is well-known in the art of chip design. Typically, buffering is used to decouple different modules, wherein one module produces data and the other consumes the data. Without buffering, the producing module would be blocked by the consuming module until it is ready to accept its data. In order to avoid the blocking of the producing module, a buffer may be introduced, storing the data produced by the producing module and thus allowing the producer to continue its execution even when the consuming module is not ready. When the consuming module is ready to accept some or all buffered data, the data stored in the buffer is immediately supplied to the consuming module.

On the other hand modern on-chip communication protocols also use the buffering of write commands or data in order to improve the interconnect utilization. Accordingly, small write bursts are stored or accumulated in a buffer before they are sent over an interconnect. Instead of being transferred in short burst, the accumulated data will be transported in a long burst over the interconnect, which usually leads to an improved interconnect utilization. This may be implemented by buffering first write data W1 (i.e. the data is not transferred over the interconnect) which is then not transferred until for example a second write data W2 arrives in the buffer, such that they are transferred as one burst with an optimal length with regards to the interconnect utilization.

Therefore, data from a number of writes can be buffered and aggregated in one burst. In addition, parts of the data in write commands may be sent in separate bursts.

The reason for the implementation of this buffering technique in the above-mentioned on-chip communication protocols is that the intellectual property blocks IP in a system on-chip connected by an interconnect should be able to communicate "naturally", i.e. the word width and the burst sizes are configured such that they rather suit the device than the interconnect. For example, if an intellectual property block IP processes pixels, then these intellectual property blocks consume and produce pixels, while in the case that they

process video frames, they consume and produce video frames. By buffering the data, the data to be transmitted over the interconnect is forced to wait until a sufficient amount of data is gathered such that these data can be transferred at once in a burst.

The above-mentioned on-chip protocols have been designed mainly for buses with a small latency. In addition, these protocols have been designed based on the assumption that read operations are always urgent and should therefore be completed as soon as possible without unnecessary buffering. However, as systems grow larger and multi-hop interconnects like networks or buses with bridges, the latency grows as well. In these cases the communication granularity become coarser and the latency requirements become less strict.

In addition, these protocols comprise means to force some of the currently buffered data to be transferred although the optimal burst length has not been reached in order to prevent deadlock caused by buffering data indefinitely. The DTL communication protocol provides a flush signal forcing all data up to the current word to be transferred over the interconnect. The AXI protocol provide an unbuffered flag for write commands to force buffered data to be transferred.

It is therefore an object of the invention to provide an integrated circuit, a method for buffering as well as a data processing system with an improved interconnect utilization.

This object is solved by an integrated circuit according to claim 1, by a method for buffering according to claim 13 and by a data processing system according to claim 14.

Therefore, an integrated circuit comprising a plurality of processing modules coupled by an interconnect means is provided. A first processing module communicates with a second processing module based on transactions. A first wrapper means associated to said second processing module buffers data from said second processing module to be transferred over said interconnect means until a first amount of data is buffered and then transfers said first amount of buffered data to said first processing module.

Accordingly, data is buffered on the slave side until a sufficient large amount of data to be transferred over the interconnect in a single package is reached. Reducing the number of packets sent over the interconnect reduces the overhead of the communication as less packet headers are required. The data to be sent is buffered until a sufficient amount of data is gathered.

According to an aspect of the invention, a second wrapper means is associated to the first processing module for buffering data from said first processing module to be transferred over the interconnect means to said second processing module until a second amount of data is buffered and said second wrapper means then transfers said buffered data to said second processing module. Therefore, data is buffered on the master as well as on the slave side until a sufficient large amount of data to be transferred over the interconnect in a single package is reached.

According to a further aspect of the invention said first and second wrapper means are adapted to transfer the buffered data in response to a first and second unbuffer signal, or a particular combination of a group of signals, respectively (even if less than the first and second amount of data is buffered in said first and second wrapper means). By issuing the unbuffer signals an occurrence of a deadlock due to a processing waiting for the buffered data can be avoided.

According to a further aspect of the invention said first and second wrapper means are adapted to transfer the buffered data according to a first and second unbuffer flag, respectively (even if less than the first and second amount of data is buffered in said first and second wrapper means). Therefore, an alternative approach to flush buffered data is provided. As opposed to the signal, which is given for each transaction, the flag may be set for a longer time. In this way, the buffering can be switched on or off. The flag can be set/unset in any way, e.g., with a signal from the IP as part of a transaction, or via separate configuration transactions (either special flush transactions or a memory-mapped reads and writes). These transactions can be issued either from the same IP, or from a separate configuration module.

According to a preferred aspect of the invention at least one of said first and second wrapper means comprise a determination unit BLDU for determining the optimal first or second amount of data to be buffered in said first or second wrapper means before said data is transferred according to the communication properties of said communication between said first and second processing module. Accordingly, the packet size of the data transferred over the interconnect can be adapted according to the properties of the actual communication and thereby the utilization of the interconnect can be improved.

The invention also relates to a method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect means, wherein a first processing module communicated to a second processing module based on transactions, comprising the step of buffering data from said second processing

module to be transferred over the interconnect means until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered.

The invention further relates to a data processing system comprising an integrated circuit comprising a plurality of processing modules coupled by an interconnect means is provided. A first processing module communicates with a second processing module based on transactions. A second wrapper means associated to said second processing module buffers data from said second processing module to be transferred over said interconnect means until a first amount of data is buffered and then transfers said first amount of buffered data to said first processing module.

Accordingly, the buffering of data as described above can also be applied in a system comprising a plurality of integrated circuits.

The invention is based on the idea to buffer data until the buffered data is sufficiently large to be transferred optimally over an interconnect means in a packet. The larger a packet is, the smaller is the amount of packet headers and therefore the overhead is reduced and the interconnect is utilized more efficiently. The data is only transferred when sufficient data for an optimal packet size has been buffered even when data can be sent earlier. The data is only transferred from the buffer when the conditions for an optimal transfer are satisfied.

Further aspects of the invention are described in the dependent claims.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiment (s) described hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a schematic representation of a network on chip according to the first embodiment, and

Fig. 2 shows a schematic representation of a network on chip according to a second embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following embodiments relate to systems on chip, i.e. a plurality of modules on the same chip (including e.g. system in a package, multi-die modules) or on different chips, communicate with each other via some kind of interconnect. The interconnect is embodied as a network on chip NOC. The network on chip may include

wires, bus, time-division multiplexing, switches, and/or routers within a network. At the transport layer of said network, the communication between the modules may be performed over connections. A connection is considered as a set of channels, each having a set of connection properties, between a first module and at least one second module. For a connection between a first module and a single second module, the connection may comprises two channels, namely one from the first module to the second channel, i.e. the request channel, and a second from the second to the first module, i.e. the response channel. The request channel is reserved for data and messages from the first to the second, while the response channel is reserved for data and messages from the second to the first module. However, if the connection involves one first and N second modules, 2*N channels are provided. The connection properties may include ordering (data transport in order), flow control (a remote buffer is reserved for a connection, and a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data), throughput (a lower bound on throughput is guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data), transmission termination, transaction completion, data correctness, priority, or data delivery.

Fig. 1 shows a basic arrangement of a network on chip according to the invention. In particular, a master module M and a slave module S each with an associated network interface NI are depicted. Each module M, S is connected to a network N via its associated network interface NI, respectively. The network interfaces NI are used as interfaces between the master and slave modules M, S and the network N. The network interfaces NI are provided to manage the communication between the respective modules M, S and the network N, so that the modules can perform their dedicated operation without having to deal with the communication with the network or other modules. The network N may comprise a plurality of network routers R for routing data through the network from one network interface NI to another.

The modules as described in the following can be so-called intellectual property blocks IPs (computation elements, memories or a subsystem which may internally contain interconnect modules) that interact with network at said network interfaces NI. A network interface NI can be connected to one or more IP blocks. Similarly, an IP block can be connected to more than one network interfaces NI.

The network interfaces associated to the master M and the slave S each comprise a wrapper means WM2, WM1, respectively. The wrapper means WM2, WM1, are responsible for buffering any data sent from the master M and the slave S over the network

N. In particular, the two wrapper means WM1, WM2 buffer data coming from the master M or the slave S, respectively, until a certain amount of data is buffered. Thereafter, the buffered data is transferred over the network N, i.e. the interconnect, as a packet within a certain burst length. It should be noted that the wrapper means WM2, WM1 is associated to the master M as well as to the slave S allowing the request as well as the response data to be buffered and sent in respective burst lengths. As the response may differ from the request the burst lengths thereof may also differ. The selected burst length should be adopted to suit the network N in order to improve the network utilization.

Fig. 2 shows a schematic representation of a network on chip according to a second embodiment. In particular, the second embodiment substantially corresponds to the network on chip according to the first embodiment. Therefore, a first wrapper means WM1 is arranged in the network interface NI associated to the slave S and a second wrapper means WM2 is arranged in the network interface NI associated to the master M. As in the first embodiment, the wrapper means WM1, WM2 serve to buffer data to be sent over the network N until the conditions for an optimal transfer are satisfied. A first unbuffer-flag unit UBF1 and a second unbuffer-flag unit UBF2 are arranged in the network interface associated to the slave S and to the master M, respectively. The first and second unbuffer-flag units UBF1, UBF2 serve to store a first and second unbuffer flag. The first and second wrapper means WM1, WM2 are adapted to immediately transfer the buffered data when the first or second unbuffer-flag is set in the first or second unbuffer-flag unit UBF1, UBF2, respectively. By providing this possibility to flush the buffered data a deadlock caused by data being buffered can be prevented. In such case, all data being buffered are transferred as fast as possible without waiting for a packet size to suit the optimal burst length for the network N.

The flushing of the buffered data may also be achieved by a first or second unbuffer signal received by the first or second wrapper means WM1, WM2. Therefore, if the first or second wrapper means WM1, WM2 receives an unbuffer signal, the data currently buffered are transferred as fast as possible, i.e. without waiting for the optimal burst length to be acquired. Accordingly, the master M may initiate the flushing of requests and slave S initiates the flushing of responses.

As opposed to the unbuffer signals, which is given for each transaction, the unbuffer flag may be set for a longer time. In this way, the buffering can be switched on or off. The flag can be set/unset in any way, e.g., with a signal from the IP as part of a transaction, or via separate configuration transactions (either special flush transactions or a

memory-mapped reads and writes). These transactions can be issued either from the same IP, or from a separate configuration module.

In addition, a first and second determination means BLDU1, BLDU2 are arranged in the network interfaces NI associated to the slave S and the master M, respectively. The first and second determination units BLDU1, BLDU2 serve to determine the optimal burst length for transferring data over the network N according to the current communication or connection properties. The determination of the optimal burst length can be performed statically or dynamically, during the initial phases of the required processing or during predetermined time intervals. Alternatively, the optimal burst length may be determined dynamically (1) every time a connection is set up for transferring data over the network, (2) for every transaction, (3) whenever an IP switches to another connection, (4) for every packet, (5) when the state of the network on chip changes (e.g., reconfiguration, NoC load, buffer fillings, etc.). The determination of the optimal burst length may be performed based on information stored in the determination units BDLU 1, 2 or on information received from the network N or IP blocks. Accordingly, the network N may comprise a communication property means CPM for determining and possibly storing the communication or connection properties for a requested communication or connection. The CPM can be centralized, or distributed (e.g., in every NI).

Besides the optimal burst length determination, also the transmission moment may be determined in a similar way by the first and second determination means BLDU1, BLDU2. For a guaranteed throughput GT connection, data should wait for one of the slots reserved for its connection. Using a "flush"-like signal/flag may force the sending of the data in advance. Alternatively, for a best effort BE connection, a round robin arbitration across connections in the NI can be used. A "flush"-like signal may force a temporarily higher priority for a connection.

In the first and second embodiment the data, i.e. the buffered data, is send over the network in form of packets. The packets are preferably formed in the respective network interfaces NI and should be sufficiently large to be transferred in an optimal way with regard to the network N. As every packet comprises a packet header, the larger the packets, the smaller the number of required packet headers, which will consequently lead to a reduced overhead and an improved network utilization. The data is buffered until the buffered data reach an optimal packet size such that the buffered data can be transferred over the network. If the amount of buffered data has not yet reached the optimal packet size, none of the data is transferred over the network N even if transferring a smaller packet size is possible. The burst

size is associated to a bus or to the IP view on communication, while the packet length is only applicable when packetization takes place (not necessary for a bus). All of the burst size determination schemes mentioned in the previous paragraph also apply to the optimal packet size determination.

Preferably, according to the first and second embodiment the data is buffered in the network interface NI, i.e. the interconnect interface, such that the master M or the slave S, which may constitute intellectual property blocks are not involved in the actual communication or the communication protocol for communicating over the interconnect or the network.

In other words, buffering is achieved for requests as well as for responses, i.e. requests as well as responses are accumulated in a buffer on the master and on the slave side, respectively, before being transferred over the interconnect. The requests and responses are aggregated in bursts with a length optimal for the particular interconnect. As in the case of a request like a write, the buffering can be prevented with an unbuffered flag to the response part of the transaction. Hence, all responses or requests pending and including the current one are transferred as fast as possible without being buffered to form an optimal burst length for the interconnect.

According to a further embodiment, the master initiates the flushing of requests as well as responses, independently and/or at the same time. In such a case, the (AXI or DTL) command group should be extended to allow indication of the different kind of flushes (e.g., 2-bit flush signal in DTL). This indication for response flushing should be forwarded to the slave NI which will then act accordingly. The same applies when using flags.

According to a further embodiment the communication scheme of the network on chip is based on a message-passing communication scheme. Here, the message header of a message may contain a flush information, which will cause all the messages from the same connection that have been sent earlier to be flushed.

According to a further embodiment the communication scheme of the network on chip is a packet-based communication scheme, i.e. one message is sent in one or more packets, the flush information should be included in the packet header.

The above-mentioned scheme may be applied to transaction-based protocols like DTL and AXI. In particular, the scheme allows a wrapper to optimise the burst length for an interconnect not only for the request, but also for responses, within a transaction. Examples of requests are (acknowledged/ unacknowledged) write command a plus data, read

commands, or more complex commands such as test-and-set, semaphore commands (P, V). Examples of responses are read data, write acknowledgments, and return values from more complex commands. Intellectual property modules connected to the interconnect via the wrapper or interconnect interfaces can therefore be build independently of the interconnect, i.e. the reuse of these IP modules can be increased, as the knowledge of the interconnect characteristics lies only in the wrappers. As for the requests, this may introduce possible additional latency, however the overall system efficiency is increased.

In addition, by providing the wrapper means in the network interfaces associated to the master as well as to the slave, the network interfaces can be designed symmetrically which may also improve their reuse.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

Furthermore, any reference signs in the claims shall not be construed as limiting the scope of the claims.

CLAIMS:

1. Integrated circuit having a plurality of processing modules (M, S) being connected with an interconnect means (N), wherein a first processing module (M) communicates to a second processing module (S) using transactions, comprising:

- a first wrapper means (WM1) associated to said second processing module (S) for buffering data from said second processing module (S) to be transferred over the interconnect means (N) until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered.

2. Integrated circuit according to claim 1, further comprising:

- a second wrapper means (WM2) associated to said first processing module (M) for buffering data from said first processing module (M) to be transferred over the interconnect means (N) until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered.

3. Integrated circuit according to claim 1 or 2, wherein

- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data in response to a first and second unbuffer signal or a first and second combination of a group of signals, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

4. Integrated circuit according to claim 1 or 2, wherein

- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data according to a first and second unbuffer flag, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

5. Integrated circuit according to claim 1 or 2, wherein

- at least one of said first and second wrapper means (WM1, WM2) comprises a determination unit (BLDU1, BLDU2) for determining the optimal first or second amount of

data to be buffered according to communication properties of the communication between said first and second processing module (M, S).

6. Integrated circuit according to claim 1 or 2, wherein

- at least one of said first and second wrapper means (WM1, WM2) comprises a determination unit (BLDU1, BLDU2) for determining the optimal moment for sending the data in said first or second wrapper means (WM1, WM2) according to communication properties of the communication between said first and second processing module (M, S).

7. Integrated circuit according to claim 3, wherein

- said first unbuffer signal is initiated by said second processing module (S) and said second unbuffer signal is initiated by said first processing module (M).

8. Integrated circuit according to claim 4, wherein

- the setting of said first unbuffer flag is initiated by said second processing module (S) and the setting of said second unbuffer flag is initiated by said first processing module (M).

9. Integrated circuit according to claim 3 or 4, wherein

- said first processing module (M) is adapted to initiate said first and/or said second unbuffer signal.

10. Integrated circuit according to claim 4, wherein

- said first processing module (M) is adapted to initiate the setting of said first and/or second unbuffer flag.

11. Integrated circuit according to claim 1 or 2, wherein

- said first and second processing modules (M, S) communicate with each other using a message-passing communication scheme, wherein the messages contain message header,

- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

12. Integrated circuit according to claim 1 or 2, wherein

- said first and second processing modules (M, S) communicate with each other using a packet based communication scheme, wherein the packets contain packet header,
- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

13. Method for buffering data in an integrated circuit having a plurality of processing modules (M, S) being connected with an interconnect means (N), wherein a first processing module (M) communicates to a second processing module (S) using transactions, comprising the steps of:

- buffering data from said second processing module (S) to be transferred over the interconnect means (N) until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered.

14. Data processing system, comprising:

- a plurality of processing modules (M, S) being connected with an interconnect means (N), wherein a first processing module (M) communicates to a second processing module (S) using transactions, comprising:
- a first wrapper means (WM1) associated to said second processing module (S) for buffering data from said second processing module (S) to be transferred over the interconnect means (N) until a first amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered.

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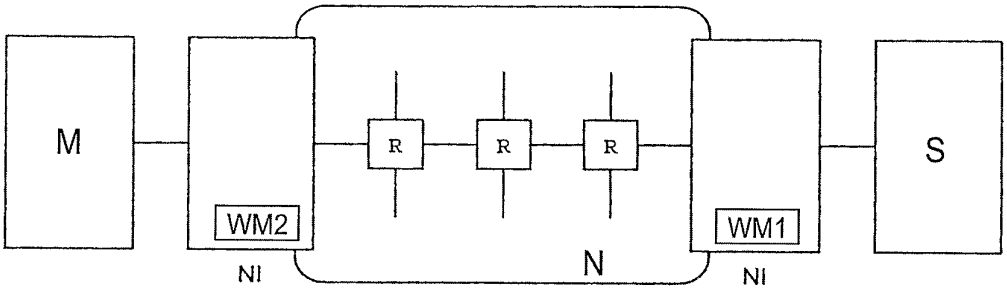


FIG.1

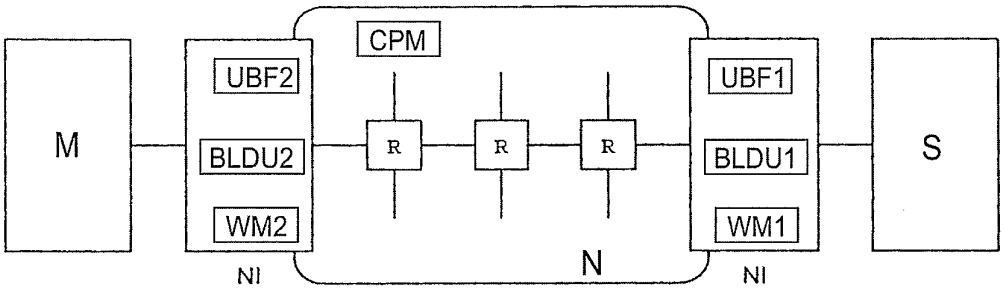


FIG.2

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Bescheinigung Certificate Attestation

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The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

04102189.0 ✓

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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R C van Dijk

Anmeldung Nr:
Application no.: 04102189.0
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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Integrated circuit and method for buffering

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Integrated circuit and method for buffering

FIELD OF THE INVENTION

The invention relates to an integrated circuit having a plurality of processing modules and an interconnect means for coupling said plurality of processing, a method for buffering and a data processing system.

BACKGROUND OF THE INVENTION

Systems on silicon show a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions. This is enabled by the increasing density with which components can be integrated on an integrated circuit. At the same time the clock speed at which circuits are operated tends to increase too. The higher clock speed in combination with the increased density of components has reduced the area which can operate synchronously within the same clock domain. This has created the need for a modular approach. According to such an approach the processing system comprises a plurality of relatively independent, complex modules. In conventional processing systems the systems modules usually communicate to each other via a bus. As the number of modules increases however, this way of communication is no longer practical for the following reasons. On the one hand the large number of modules forms a too high bus load. On the other hand the bus forms a communication bottleneck as it enables only one device to send data to the bus.

A communication network forms an effective way to overcome these disadvantages. Networks on chip (NoC) have received considerable attention recently as a solution to the interconnect problem in highly-complex chips. The reason is twofold. First, NoCs help resolve the electrical problems in new deep-submicron technologies, as they structure and manage global wires. At the same time they share wires, lowering their number and increasing their utilization. NoCs can also be energy efficient and reliable and are scalable compared to buses. Second, NoCs also decouple computation from communication, which is essential in managing the design of billion-transistor chips. NoCs achieve this decoupling because they are traditionally designed using protocol stacks, which provide well-defined interfaces separating communication service usage from service implementation.

Using networks for on-chip communication when designing systems on chip (SoC), however, raises a number of new issues that must be taken into account. This is because, in contrast to existing on-chip interconnects (e.g., buses, switches, or point-to-point wires), where the communicating modules are directly connected, in a NoC the modules communicate remotely via network nodes. As a result, interconnect arbitration changes from centralized to distributed, and issues like out-of order transactions, higher latencies, and end-to-end flow control must be handled either by the intellectual property blocks (IP) or by the network.

Most of these topics have been already the subject of research in the field of local and wide area networks (computer networks) and as an interconnect for parallel machine interconnect networks. Both are very much related to on-chip networks, and many of the results in those fields are also applicable on chip. However, NoC's premises are different from off-chip networks, and, therefore, most of the network design choices must be reevaluated. On-chip networks have different properties (e.g., tighter link synchronization) and constraints (e.g., higher memory cost) leading to different design choices, which ultimately affect the network services.

Introducing networks as on-chip interconnects radically changes the communication when compared to direct interconnects, such as buses or switches. This is because of the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes. This is in contrast with the prevalent existing interconnects (i.e., buses) where modules are directly connected.

Modern on-chip communication protocols (e.g., Device Transaction Level DTL and AXI-Protocol) operate on a split and pipelined basis with transactions consisting of a request and a response, and the bus is released for use by others after a request issued by a master is accepted by a corresponding slave. Split pipelined communication protocols are used especially in multi-hop interconnects (e.g., networks on chip, or buses with bridges), allowing an efficient utilization of the interconnect. The efficiently of a split bus can be increased for cases where a response generation at the slave is time consuming. On a pipelined protocol, a master is allowed to have multiple outstanding requests (i.e., requests for which the response is pending or expected).

The above-mentioned protocols are designed to operate at a device level, as opposed to a system or interconnect level. In other words they are designed to be independent of the actual interconnect implementation (e.g., arbitration signals are not visible) allowing the reuse of intellectual property blocks IP and their earlier integration.

In particular, the above-mentioned on-chip communication protocols comprise four main groups of signals, namely commands (or address), write data, read data and write response. The command group consists of command, addresses and command flags like burst length and mask. The command and write data groups are driven by the initiator to the target. The read data and write response are driven by the target to the initiator following a command from an initiator. All four groups are independent of each other with some ordering constraints between them, e.g. a response cannot be issued before a command.

These on-chip communication protocols also implement the concept of buffering data which is well-known in the art of chip design. Typically, buffering is used to decouple different modules, wherein one module produces data and the other consumes the data. Without buffering, the producing module would be blocked by the consuming module until it is ready to accept its data. In order to avoid the blocking of the producing module, a buffer may be introduced, storing the data produced by the producing module and thus allowing the producer to continue its execution even when the consuming module is not ready. When the consuming module is ready to accept some or all buffered data, the data stored in the buffer is immediately supplied to the consuming module.

On the other hand modern on-chip communication protocols also use the buffering of write commands or data in order to improve the interconnect utilization. Accordingly, small write bursts are stored or accumulated in a buffer before they are sent over an interconnect. Instead of being transferred in short burst, the accumulated data will be transported in a long burst over the interconnect, which usually leads to an improved interconnect utilization. This may be implemented by buffering first write data W1 (i.e. the data is not transferred over the interconnect) which is then not transferred until for example a second write data W2 arrives in the buffer, such that they are transferred as one burst with an optimal length with regards to the interconnect utilization.

Therefore, data from a number of writes can be buffered and aggregated in one burst. In addition, parts of the data in write commands may be sent in separate bursts.

The reason for the implementation of this buffering technique in the above-mentioned on-chip communication protocols is that the intellectual property blocks IP in a system on-chip connected by an interconnect should be able to communicate "naturally", i.e. the word width and the burst sizes are configured such that they rather suit the device than the interconnect. For example, if an intellectual property block IP processes pixels, then these intellectual property blocks consume and produce pixels, while in the case that they

process video frames, they consume and produce video frames. By buffering the data, the data to be transmitted over the interconnect is forced to wait until a sufficient amount of data is gathered such that these data can be transferred at once in a burst.

The above-mentioned on-chip protocols have been designed mainly for buses with a small latency. In addition, these protocols have been designed based on the assumption that read operations are always urgent and should therefore be completed as soon as possible without unnecessary buffering. However, as systems grow larger and multi-hop interconnects like networks or buses with bridges, the latency grows as well. In these cases the communication granularity become coarser and the latency requirements become less strict.

In addition, these protocols comprise means to force some of the currently buffered data to be transferred although the optimal burst length has not been reached in order to prevent deadlock caused by buffering data indefinitely. The DTL communication protocol provides a flush signal forcing all data up to the current word to be transferred over the interconnect. The AXI protocol provide an unbuffered flag for write commands to force buffered data to be transferred.

It is therefore an object of the invention to provide an integrated circuit, a method for buffering as well as a data processing system with an improved interconnect utilization.

This object is solved by an integrated circuit according to claim 1, by a method for buffering according to claim 13 and by a data processing system according to claim 14.

Therefore, an integrated circuit comprising a plurality of processing modules coupled by an interconnect means is provided. A first processing module communicates with a second processing module based on transactions. A first wrapper means associated to said second processing module buffers data from said second processing module to be transferred over said interconnect means until a first amount of data is buffered and then transfers said first amount of buffered data to said first processing module.

Accordingly, data is buffered on the slave side until a sufficient large amount of data to be transferred over the interconnect in a single package is reached. Reducing the number of packets sent over the interconnect reduces the overhead of the communication as less packet headers are required. The data to be sent is buffered until a sufficient amount of data is gathered.

According to an aspect of the invention, a second wrapper means is associated to the first processing module for buffering data from said first processing module to be transferred over the interconnect means to said second processing module until a second amount of data is buffered and said second wrapper means then transfers said buffered data to said second processing module. Therefore, data is buffered on the master as well as on the slave side until a sufficient large amount of data to be transferred over the interconnect in a single package is reached.

According to a further aspect of the invention said first and second wrapper means are adapted to transfer the buffered data in response to a first and second unbuffer signal, or a particular combination of a group of signals, respectively (even if less than the first and second amount of data is buffered in said first and second wrapper means). By issuing the unbuffer signals an occurrence of a deadlock due to a processing waiting for the buffered data can be avoided.

According to a further aspect of the invention said first and second wrapper means are adapted to transfer the buffered data according to a first and second unbuffer flag, respectively (even if less than the first and second amount of data is buffered in said first and second wrapper means). Therefore, an alternative approach to flush buffered data is provided. As opposed to the signal, which is given for each transaction, the flag may be set for a longer time. In this way, the buffering can be switched on or off. The flag can be set/unset in any way, e.g., with a signal from the IP as part of a transaction, or via separate configuration transactions (either special flush transactions or a memory-mapped reads and writes). These transactions can be issued either from the same IP, or from a separate configuration module.

According to a preferred aspect of the invention at least one of said first and second wrapper means comprise a determination unit BLDU for determining the optimal first or second amount of data to be buffered in said first or second wrapper means before said data is transferred according to the communication properties of said communication between said first and second processing module. Accordingly, the packet size of the data transferred over the interconnect can be adapted according to the properties of the actual communication and thereby the utilization of the interconnect can be improved.

The invention also relates to a method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect means, wherein a first processing module communicated to a second processing module based on transactions, comprising the step of buffering data from said second processing

module to be transferred over the interconnect means until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered.

The invention further relates to a data processing system comprising an integrated circuit comprising a plurality of processing modules coupled by an interconnect means is provided. A first processing module communicates with a second processing module based on transactions. A second wrapper means associated to said second processing module buffers data from said second processing module to be transferred over said interconnect means until a first amount of data is buffered and then transfers said first amount of buffered data to said first processing module.

Accordingly, the buffering of data as described above can also be applied in a system comprising a plurality of integrated circuits.

The invention is based on the idea to buffer data until the buffered data is sufficiently large to be transferred optimally over an interconnect means in a packet. The larger a packet is, the smaller is the amount of packet headers and therefore the overhead is reduced and the interconnect is utilized more efficiently. The data is only transferred when sufficient data for an optimal packet size has been buffered even when data can be sent earlier. The data is only transferred from the buffer when the conditions for an optimal transfer are satisfied.

Further aspects of the invention are described in the dependent claims.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiment (s) described hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a schematic representation of a network on chip according to the first embodiment, and

Fig. 2 shows a schematic representation of a network on chip according to a second embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following embodiments relate to systems on chip, i.e. a plurality of modules on the same chip (including e.g. system in a package, multi-die modules) or on different chips, communicate with each other via some kind of interconnect. The interconnect is embodied as a network on chip NOC. The network on chip may include

wires, bus, time-division multiplexing, switches, and/or routers within a network. At the transport layer of said network, the communication between the modules may be performed over connections. A connection is considered as a set of channels, each having a set of connection properties, between a first module and at least one second module. For a connection between a first module and a single second module, the connection may comprises two channels, namely one from the first module to the second channel, i.e. the request channel, and a second from the second to the first module, i.e. the response channel. The request channel is reserved for data and messages from the first to the second, while the response channel is reserved for data and messages from the second to the first module. However, if the connection involves one first and N second modules, 2*N channels are provided. The connection properties may include ordering (data transport in order), flow control (a remote buffer is reserved for a connection, and a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data), throughput (a lower bound on throughput is guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data), transmission termination, transaction completion, data correctness, priority, or data delivery.

Fig. 1 shows a basic arrangement of a network on chip according to the invention. In particular, a master module M and a slave module S each with an associated network interface NI are depicted. Each module M, S is connected to a network N via its associated network interface NI, respectively. The network interfaces NI are used as interfaces between the master and slave modules M, S and the network N. The network interfaces NI are provided to manage the communication between the respective modules M, S and the network N, so that the modules can perform their dedicated operation without having to deal with the communication with the network or other modules. The network N may comprise a plurality of network routers R for routing data through the network from one network interface NI to another.

The modules as described in the following can be so-called intellectual property blocks IPs (computation elements, memories or a subsystem which may internally contain interconnect modules) that interact with network at said network interfaces NI. A network interface NI can be connected to one or more IP blocks. Similarly, an IP block can be connected to more than one network interfaces NI.

The network interfaces associated to the master M and the slave S each comprise a wrapper means WM2, WM1, respectively. The wrapper means WM2, WM1, are responsible for buffering any data sent from the master M and the slave S over the network

N. In particular, the two wrapper means WM1, WM2 buffer data coming from the master M or the slave S, respectively, until a certain amount of data is buffered. Thereafter, the buffered data is transferred over the network N, i.e. the interconnect, as a packet within a certain burst length. It should be noted that the wrapper means WM2, WM1 is associated to the master M as well as to the slave S allowing the request as well as the response data to be buffered and sent in respective burst lengths. As the response may differ from the request the burst lengths thereof may also differ. The selected burst length should be adopted to suit the network N in order to improve the network utilization.

Fig. 2 shows a schematic representation of a network on chip according to a second embodiment. In particular, the second embodiment substantially corresponds to the network on chip according to the first embodiment. Therefore, a first wrapper means WM1 is arranged in the network interface NI associated to the slave S and a second wrapper means WM2 is arranged in the network interface NI associated to the master M. As in the first embodiment, the wrapper means WM1, WM2 serve to buffer data to be sent over the network N until the conditions for an optimal transfer are satisfied. A first unbuffer-flag unit UBF1 and a second unbuffer-flag unit UBF2 are arranged in the network interface associated to the slave S and to the master M, respectively. The first and second unbuffer-flag units UBF1, UBF2 serve to store a first and second unbuffer flag. The first and second wrapper means WM1, WM2 are adapted to immediately transfer the buffered data when the first or second unbuffer-flag is set in the first or second unbuffer-flag unit UBF1, UBF2, respectively. By providing this possibility to flush the buffered data a deadlock caused by data being buffered can be prevented. In such case, all data being buffered are transferred as fast as possible without waiting for a packet size to suit the optimal burst length for the network N.

The flushing of the buffered data may also be achieved by a first or second unbuffer signal received by the first or second wrapper means WM1, WM2. Therefore, if the first or second wrapper means WM1, WM2 receives an unbuffer signal, the data currently buffered are transferred as fast as possible, i.e. without waiting for the optimal burst length to be acquired. Accordingly, the master M may initiate the flushing of requests and slave S initiates the flushing of responses.

As opposed to the unbuffer signals, which is given for each transaction, the unbuffer flag may be set for a longer time. In this way, the buffering can be switched on or off. The flag can be set/unset in any way, e.g., with a signal from the IP as part of a transaction, or via separate configuration transactions (either special flush transactions or a

memory-mapped reads and writes). These transactions can be issued either from the same IP, or from a separate configuration module.

In addition, a first and second determination means BLDU1, BLDU2 are arranged in the network interfaces NI associated to the slave S and the master M, respectively. The first and second determination units BLDU1, BLDU2 serve to determine the optimal burst length for transferring data over the network N according to the current communication or connection properties. The determination of the optimal burst length can be performed statically or dynamically, during the initial phases of the required processing or during predetermined time intervals. Alternatively, the optimal burst length may be determined dynamically (1) every time a connection is set up for transferring data over the network, (2) for every transaction, (3) whenever an IP switches to another connection, (4) for every packet, (5) when the state of the network on chip changes (e.g., reconfiguration, NoC load, buffer fillings, etc.). The determination of the optimal burst length may be performed based on information stored in the determination units BDLU 1, 2 or on information received from the network N or IP blocks. Accordingly, the network N may comprise a communication property means CPM for determining and possibly storing the communication or connection properties for a requested communication or connection. The CPM can be centralized, or distributed (e.g., in every NI).

Besides the optimal burst length determination, also the transmission moment may be determined in a similar way by the first and second determination means BLDU1, BLDU2. For a guaranteed throughput GT connection, data should wait for one of the slots reserved for its connection. Using a "flush"-like signal/flag may force the sending of the data in advance. Alternatively, for a best effort BE connection, a round robin arbitration across connections in the NI can be used. A "flush"-like signal may force a temporarily higher priority for a connection.

In the first and second embodiment the data, i.e. the buffered data, is send over the network in form of packets. The packets are preferably formed in the respective network interfaces NI and should be sufficiently large to be transferred in an optimal way with regard to the network N. As every packet comprises a packet header, the larger the packets, the smaller the number of required packet headers, which will consequently lead to a reduced overhead and an improved network utilization. The data is buffered until the buffered data reach an optimal packet size such that the buffered data can be transferred over the network. If the amount of buffered data has not yet reached the optimal packet size, none of the data is transferred over the network N even if transferring a smaller packet size is possible. The burst

size is associated to a bus or to the IP view on communication, while the packet length is only applicable when packetization takes place (not necessary for a bus). All of the burst size determination schemes mentioned in the previous paragraph also apply to the optimal packet size determination.

Preferably, according to the first and second embodiment the data is buffered in the network interface NI, i.e. the interconnect interface, such that the master M or the slave S, which may constitute intellectual property blocks are not involved in the actual communication or the communication protocol for communicating over the interconnect or the network.

In other words, buffering is achieved for requests as well as for responses, i.e. requests as well as responses are accumulated in a buffer on the master and on the slave side, respectively, before being transferred over the interconnect. The requests and responses are aggregated in bursts with a length optimal for the particular interconnect. As in the case of a request like a write, the buffering can be prevented with an unbuffered flag to the response part of the transaction. Hence, all responses or requests pending and including the current one are transferred as fast as possible without being buffered to form an optimal burst length for the interconnect.

According to a further embodiment, the master initiates the flushing of requests as well as responses, independently and/or at the same time. In such a case, the (AXI or DTL) command group should be extended to allow indication of the different kind of flushes (e.g., 2-bit flush signal in DTL). This indication for response flushing should be forwarded to the slave NI which will then act accordingly. The same applies when using flags.

According to a further embodiment the communication scheme of the network on chip is based on a message-passing communication scheme. Here, the message header of a message may contain a flush information, which will cause all the messages from the same connection that have been sent earlier to be flushed.

According to a further embodiment the communication scheme of the network on chip is a packet-based communication scheme, i.e. one message is sent in one or more packets, the flush information should be included in the packet header.

The above-mentioned scheme may be applied to transaction-based protocols like DTL and AXI. In particular, the scheme allows a wrapper to optimise the burst length for an interconnect not only for the request, but also for responses, within a transaction. Examples of requests are (acknowledged/ unacknowledged) write command a plus data, read

commands, or more complex commands such as test-and-set, semaphore commands (P, V). Examples of responses are read data, write acknowledgments, and return values from more complex commands. Intellectual property modules connected to the interconnect via the wrapper or interconnect interfaces can therefore be build independently of the interconnect, i.e. the reuse of these IP modules can be increased, as the knowledge of the interconnect characteristics lies only in the wrappers. As for the requests, this may introduce possible additional latency, however the overall system efficiency is increased.

In addition, by providing the wrapper means in the network interfaces associated to the master as well as to the slave, the network interfaces can be designed symmetrically which may also improve their reuse.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

Furthermore, any reference signs in the claims shall not be construed as limiting the scope of the claims.

CLAIMS:

1. Integrated circuit having a plurality of processing modules (M, S) being connected with an interconnect means (N), wherein a first processing module (M) communicates to a second processing module (S) using transactions, comprising:

- a first wrapper means (WM1) associated to said second processing module (S) for buffering data from said second processing module (S) to be transferred over the interconnect means (N) until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered.

2. Integrated circuit according to claim 1, further comprising:

- a second wrapper means (WM2) associated to said first processing module (M) for buffering data from said first processing module (M) to be transferred over the interconnect means (N) until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered.

3. Integrated circuit according to claim 1 or 2, wherein

- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data in response to a first and second unbuffer signal or a first and second combination of a group of signals, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

4. Integrated circuit according to claim 1 or 2, wherein

- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data according to a first and second unbuffer flag, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

5. Integrated circuit according to claim 1 or 2, wherein

- at least one of said first and second wrapper means (WM1, WM2) comprises a determination unit (BLDU1, BLDU2) for determining the optimal first or second amount of

data to be buffered according to communication properties of the communication between said first and second processing module (M, S).

6. Integrated circuit according to claim 1 or 2, wherein

- at least one of said first and second wrapper means (WM1, WM2) comprises a determination unit (BLDU1, BLDU2) for determining the optimal moment for sending the data in said first or second wrapper means (WM1, WM2) according to communication properties of the communication between said first and second processing module (M, S).

7. Integrated circuit according to claim 3, wherein

- said first unbuffer signal is initiated by said second processing module (S) and said second unbuffer signal is initiated by said first processing module (M).

8. Integrated circuit according to claim 4, wherein

- the setting of said first unbuffer flag is initiated by said second processing module (S) and the setting of said second unbuffer flag is initiated by said first processing module (M).

9. Integrated circuit according to claim 3 or 4, wherein

- said first processing module (M) is adapted to initiate said first and/or said second unbuffer signal.

10. Integrated circuit according to claim 4, wherein

- said first processing module (M) is adapted to initiate the setting of said first and/or second unbuffer flag.

11. Integrated circuit according to claim 1 or 2, wherein

- said first and second processing modules (M, S) communicate with each other using a message-passing communication scheme, wherein the messages contain message header,

- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

12. Integrated circuit according to claim 1 or 2, wherein

- said first and second processing modules (M, S) communicate with each other using a packet based communication scheme, wherein the packets contain packet header,
- said first and second wrapper means (WM1, WM2) are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WM1, WM2).

13. Method for buffering data in an integrated circuit having a plurality of processing modules (M, S) being connected with an interconnect means (N), wherein a first processing module (M) communicates to a second processing module (S) using transactions, comprising the steps of:

- buffering data from said second processing module (S) to be transferred over the interconnect means (N) until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered.

14. Data processing system, comprising:

- a plurality of processing modules (M, S) being connected with an interconnect means (N), wherein a first processing module (M) communicates to a second processing module (S) using transactions, comprising:
- a first wrapper means (WM1) associated to said second processing module (S) for buffering data from said second processing module (S) to be transferred over the interconnect means (N) until a first amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered.

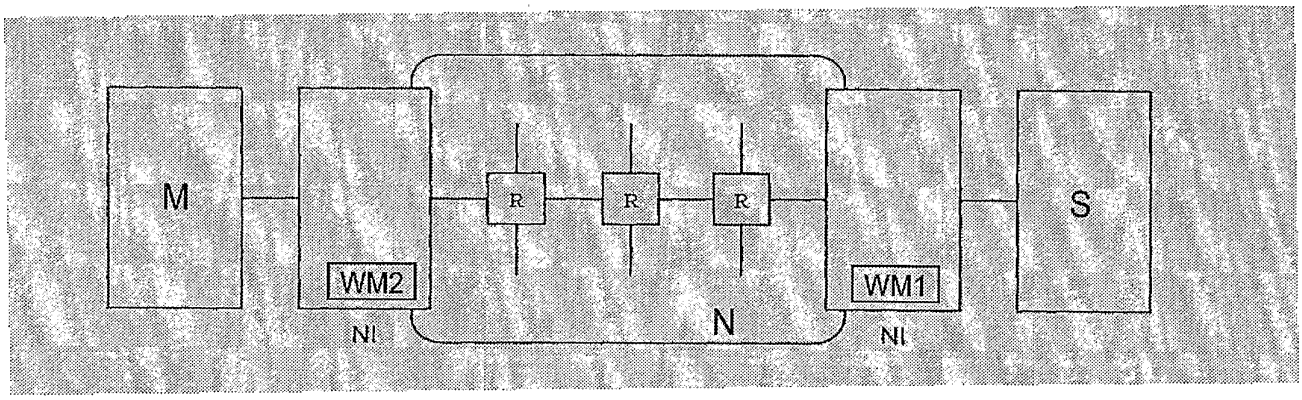


FIG.1

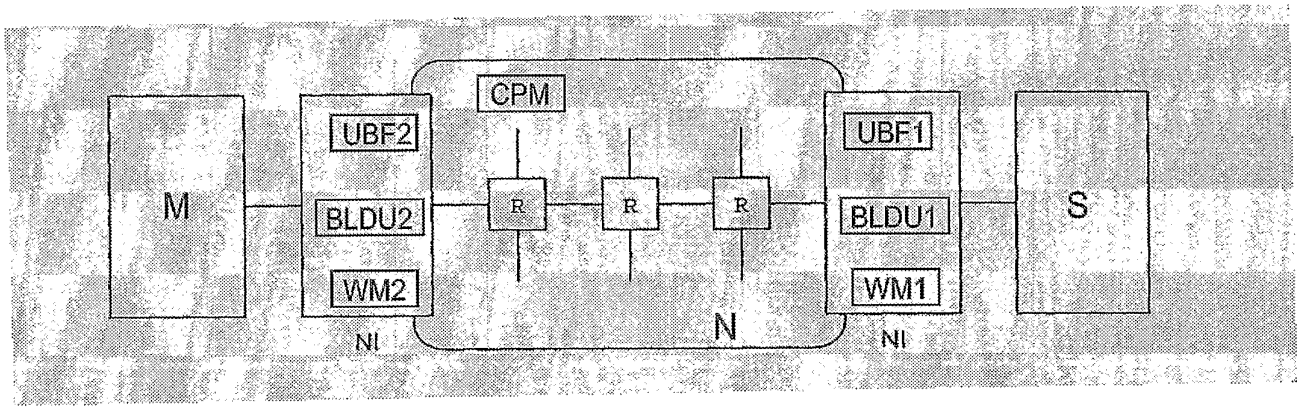


FIG.2

ABSTRACT:

An integrated circuit comprising a plurality of processing modules (M, S) coupled by an interconnect means (N) is provided. A first processing module (M) communicates with a second processing module (S) based on transactions. A first wrapper means (WM1) associated to said second processing module (S) buffers data from said second processing module (S) to be transferred over said interconnect means until a first amount of data is buffered and then transfers said first amount of buffered data to said first processing module (M).

Fig. 2

PCT/IB2005/051580



PCT REQUEST

Print Out (Original in Electronic Form)

VIII-2-1	**Declaration: Entitlement to apply for and be granted a patent** Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent (Rules 4.17(ii) and 51bis.1(a)(ii)), in a case where the declaration under Rule 4.17(iv) is not appropriate: Name (LAST, First)	in relation to this international application KONINKLIJKE PHILIPS ELECTRONICS N.V. is entitled to apply for and be granted a patent by virtue of the following:
VIII-2-1(ii)		KONINKLIJKE PHILIPS ELECTRONICS N.V. is entitled as employer of the inventor, RADULESCU, Andrei
VIII-2-1(ii)		KONINKLIJKE PHILIPS ELECTRONICS N.V. is entitled as employer of the inventor, GOOSSENS, Kees, G., W.
VIII-2-1(ix)	This declaration is made for the purposes of:	all designations except the designation of the United States of America

UNITED STATES NATIONAL STAGE WORKSHEET (DO/EO)

B.C., Patent Application Specialist, PCT /DO/EO/National Stage Division

Publication No. WO05/111823 Publication Date 11-24-05

Not Published: ____U.S. only ____Requested

Basic fee paid: $300 IPER fee paid: $200/____ ISA fee paid: $400/EP

U. S. Application No. - 11/569,083

International Application Number: PCT/IB05/51580 International Filing Date: 05-13-05

Application Filed by 30 Month: ✓ Yes ____No Language: ENG.

Copy in International Application: yes ✓ no____ Translation: yes____ no____ Defective: ___Yes

371 Filing Fees ✓ paid ____Insufficient Meet Article 33 Requirement: ____Yes ___No & why not____

Original claims: 1-14 Added Claims: ____Total Claims: 14 Chargeable 14 Independent 3 multiple N

Clms. Cancelled via Article 19 or 34____ &/or Pre-Amdt. ____Clms. added via Article 19 or 34 ____

Total Number of Drawing Sheets: 2 Foreign Text: ____

Oath/Declaration: yes ✓ no____: signed ✓ unsigned ___ defective___ Date Satisfied: 11-14-06

PCT/RO/101/Request Form Declaration: ____yes ____No ____ properly executed Date:____

Small Entity: ___Yes Small Entity Statement ____Assertion by filing fee paid ____ Large Entity: ✓

1st Submission: Biochemical Seq. Diskette: yes___ no____ entered & date ____ not entered & date ____

2nd Submission: Biochemical Seq. Diskette: yes___ no____ entered & date ____ not entered & date____

Biochemical Seq. Listing: yes __ no __ statement ___ yes ___ no other submission date(s): ____

Biochemical Diskette/Listing not needed: ____

Copy of ISR: ___with references without references ✓ Non-Establishment of ISR PCT/ISA/203 ____

Article 19 Amendment: ____entered ____not entered ____ Replaced by Article 34 Amendment ____

Copy of IPER: ____without Annexes: ____with Annexes: ____ Annexes entered ____Annexes not entered ____237

Reason Annexes have not been entered: ____

Preliminary Amendment(s): yes ✓ not entered____ & Why ____Other Amendment dates: ____

IDS: ___yes ___with references ___without references Other IDS Dates: ____

Request for Immediate Examination: yes____ no____, Other Early Processing Date: ____

Substitute Specification: yes____ Other Documents filed: ____

Assignment: yes ✓ Date filed: 11.14.06 Assignment for PG Pub: ___Yes Date filed:____

Power of Attorney ✓ Application Data Sheet ✓ Priority Document(s): yes ✓

Other Problems:____

Application Size: Spec. 11 Claims 3 Abstract 1 Drawings 2 Seq. List.____ Seq. RF___ Total (17)

Application Fees: owed/paid

___Declaration ___Claims ___Multiple ___Translation ___Extension ____Petition ____Application size____

Date of 35 USC Receipt of Request: 11-14-06

Date Completion USC 371 Requirements: 11

Notice of Missing Requirements: ____Response to Missing Requirements____

371 Formalities Letter: (Sequence) 922____922 Response ____ or (Fees Owed) 923____923-Repsonse ____

Notice of Defective Response: ____Defective Response Reply____

Notice of Acceptance: 06/21/07

Notice of Abandonment: ____Petition to Revive: ____ Petition 1.47: ____

PATENT APPLICATION FEE DETERMINATION RECORD

Effective December 8, 2004

Application or Docket Number: 11/569,083

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
U.S. NATIONAL STAGE FEES		
BASIC FEE	SMALL ENT. = $ 150	LARGE ENT. = $ 300
EXAMINATION FEE	Satisfies PCT Article 33(1)-(4) = $ 50 / $ 100	All other situations = $ 100 / $ 200
SEARCH FEE	U.S. is ISA = $ 50 / $ 100 ALL other countries = $ 200 / $ 400	ALL other situations = $ 250 / $ 500
FEE FOR EXTRA SPEC. PGS.	minus 100 =	/ 50 =
TOTAL CHARGEABLE CLAIMS	14 minus 20 =	*
INDEPENDENT CLAIMS	3 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT	☐	

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐	RATE	FEE	OR	OTHER THAN SMALL ENTITY	RATE	FEE
	BASIC FEE		OR		BASIC FEE	300
	EXAM. FEE				EXAM. FEE	200
	SEARCH FEE				SEARCH FEE	400
	X $ 125 =				X $ 250 =	
	X $ 25 =		OR		X $ 50 =	
	X $ 100 =		OR		X $ 200 =	
	+ $ 180 =		OR		+ $ 360 =	
	TOTAL		OR		TOTAL	900

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
14				
Total	* 14	Minus	** 20	= 0
Independent	* 3	Minus	*** 3	= 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM	☐			

SMALL ENTITY	RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY	RATE	ADDITIONAL FEE
	X $ 25 =		OR		X $ 50 =	
	X $ 100 =		OR		X $ 200 =	
	+ $ 180 =		OR		+ $ 360 =	
	TOTAL ADDIT. FEE		OR		TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM	☐			

RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
X $ 25 =		OR	X $ 50 =	
X $ 100 =		OR	X $ 200 =	
+ $ 180 =		OR	+ $ 360 =	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '20', enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '3', enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Barbara Campbell, PCT National Stage Division

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET (FOR USE WITH FORM PTO-875)	SERIAL NO. 11/569,083	FILING DATE 11-14-06
	APPLICANT(S)	

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1			1			
2				1		
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TOTAL IND.			3			
TOTAL DEP.			11			
TOTAL CLAIMS			14			

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
51						
52						
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100						
TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
11/569,083	11/14/2006	2816	900	NL 040529	14	3

CONFIRMATION NO. 4172

24737
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY10510

FILING RECEIPT

Date Mailed: 06/25/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Andrei Radulescu, Eindhoven, NETHERLANDS;
Kees Gerard Willem Goossens, Eindhoven, NETHERLANDS;

Assignment For Published Patent Application

KONINKLIJKE PHILIPS ELECTRONICS, N.V., Eindhoven, NL

Power of Attorney:
Jack Haken--26902
Edward Blocker--30245
Michael Marion--32266

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/IB05/51580 05/13/2005

Foreign Applications

EUROPEAN PATENT OFFICE (EPO) 04102189.0 05/18/2004

If Required, Foreign Filing License Granted: 06/21/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/569,083**

Projected Publication Date: 09/27/2007

Non-Publication Request: No

Early Publication Request: No

Title

Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips

Preliminary Class

327

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
11/569,083	Andrei Radulescu	NL 040529

INTERNATIONAL APPLICATION NO.	
PCT/IB05/51580	
I.A. FILING DATE	PRIORITY DATE
05/13/2005	05/18/2004

24737
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

CONFIRMATION NO. 4172

371 ACCEPTANCE LETTER

OC000000024488102

Date Mailed: 06/25/2007

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

11/14/2006	11/18/2006
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and (c)(4) REQUIREMENTS	DATE OF COMPLETION OF ALL 35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** *The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363).* Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Copy of the International Application filed on 11/14/2006
- Copy of the International Search Report filed on 11/14/2006
- Preliminary Amendments filed on 11/14/2006
- Oath or Declaration filed on 11/14/2006
- U.S. Basic National Fees filed on 11/14/2006
- Assignment filed on 11/14/2006
- Priority Documents filed on 11/14/2006
- Power of Attorney filed on 11/14/2006
- Specification filed on 11/14/2006
- Claims filed on 11/14/2006
- Abstracts filed on 11/14/2006

- Drawings filed on 11/14/2006

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

BARBARA A CAMPBELL
Telephone: (703) 308-9140 EXT 217

PART 3 - OFFICE COPY

FORM PCT/DO/EO/903 (371 Acceptance Notice)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/569,083	11/14/2006	Andrei Radulescu	NL 040529

CONFIRMATION NO. 4172

24737
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY10510

Title: Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips

Publication No. US-2007-0226407-A1
Publication Date: 09/27/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	NL 040529	4172

24737 7590 07/08/2009

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
ALSIP, MICHAEL	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
07/08/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/569,083	RADULESCU ET AL.	
	Examiner	Art Unit	
	MICHAEL ALSIP	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman et al. (US 4,228,496) and further in view of Barroso et al. (US 6,668,308).

4. Consider **claims 1, 13 and 14**, Katzman et al. discloses a method, data processing system and having a plurality of processing modules (M, S) being connected with an interconnect means (N), wherein a first processing module (M) communicates to a second processing module (S) using transactions (Fig. 2, first ¶ of the abstract), comprising: a first wrapper means (WMI) associated to said second processing module (S) for buffering data from said second processing module (S) to be transferred over the interconnect means (N) until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been

buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper means" is considered to by a buffer or queue like memory).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

5. Consider **claim 2** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose further comprising a second wrapper means (WM2) associated to said first processing module (M) for buffering data from said first processing module (M) to be transferred over the interconnect means (N) until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where each inter-processor control for each processor as an input and output buffer for sending and receiving data).

6. Consider **claim 3** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first and second wrapper means (WMI, WM2) are adapted to transfer the buffered data in response to a first and second unbuffer signal or a first and second combination of a group of signals, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WMI, WM2) (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task).

7. Consider **claim 4** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first and second wrapper means (WMI, WM2) are adapted to transfer the buffered data according to a first and second unbuffer flag, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WMI, WM2) (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed flags.).

8. Consider **claim 5** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein at least one of said first and second wrapper means (WMI, WM2) comprises a determination unit (BLDUI, BLDU2) for determining the optimal first or second amount of data to be buffered according to communication properties of the

communication between said first and second processing module (M, S) (Col. 7 lines 8-37).

9. Consider **claim 6** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein at least one of said first and second wrapper means (WMI, WM2) comprises a determination unit (BLDUI, BLDU2) for determining the optimal moment for sending the data in said first or second wrapper means (WMI, WM2) according to communication properties of the communication between said first and second processing module (M, S) (Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task of sending the data at the appropriate time.).

10. Consider **claim 7** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. disclose wherein said first unbuffer signal is initiated by said second processing module (S) and said second unbuffer signal is initiated by said first processing module (M) (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor).

11. Consider **claim 8** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. disclose wherein the setting of said first unbuffer flag is initiated by said second processing module (S) and the setting of said second unbuffer flag is initiated by said first processing module (M) (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

12. Consider **claim 9** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. disclose wherein said first processing module (M) is adapted to initiate said first and/or said second unbuffer signal (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor.).

13. Consider **claim 10** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. disclose wherein said first processing module (M) is adapted to initiate the

setting of said first and/or second unbuffer flag (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

14. Consider **claim 11** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first and second processing modules (M, S) communicate with each other using a message-passing communication scheme, wherein the messages contain message header, said first and second wrapper means (WMI, WM2) are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WMI, WM2) (Col. 31 lines 3-52, where the control packet is considered the head of the message and this identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor).

15. Consider **claim 12** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first and second processing modules (M, S) communicate with each other using a packet based communication scheme, wherein the packets contain packet header, said first and second wrapper means (WMI, WM2)

are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper means (WMI, WM2) (Katzman et al.: Col. 31 lines 3-52, where the control packet identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor and Barroso et al.: Col. 14 lines 36-45, discloses that data-less transactions are 128-bits long and that data packets have the same 128-bit header format, disclosing that both types have headers).

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The pertinent art is cited in the attached PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Michael Alsip
Examiner
Art Unit 2186

/Michael Alsip/
Examiner, Art Unit 2186

July 2, 2009

Notice of References Cited	Application/Control No. 11/569,083	Applicant(s)/Patent Under Reexamination RADULESCU ET AL.	
	Examiner MICHAEL ALSIP	Art Unit 2186	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,549,024	06-2009	Piry et al.	711/141
*	B	US-4,253,144	02-1981	Bellamy et al.	709/226
*	C	US-7,257,665	08-2007	Niell et al.	711/101
*	D	US-4,228,496	10-1980	Katzman et al.	710/100
*	E	US-6,668,308	12-2003	Barroso et al.	711/141
*	F	US-4,378,588	03-1983	Katzman et al.	710/57
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	Art Unit
	MICHAEL ALSIP	2186

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/02/2009								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	Art Unit
	MICHAEL ALSIP	2186

SEARCHED			
Class	Subclass	Date	Examiner
711	118	7/2/2009	MA
711	141	7/2/2009	MA
710	57	7/2/2009	MA
710	100	7/2/2009	MA

SEARCH NOTES		
Search Notes	Date	Examiner
inventor name and assignee search in eDAN and PALM	7/2/2009	MA
class/subclass and keyword search in EAST	7/2/2009	MA

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/MICHAEL ALSIP/ Examiner.Art Unit 2186	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 11:31
L3	145	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
L4	10	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
L5	245	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
L6	13	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
L7	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05

L8	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
L9	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
L10	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05

7/2/2009 1:06:22 PM
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BIB DATA SHEET

CONFIRMATION NO. 4172

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/569,083	11/14/2006 RULE	327	2186	NL 040529

APPLICANTS

Andrei Radulescu, Eindhoven, NETHERLANDS;
Kees Gerard Goossens, Eindhoven, NETHERLANDS;

**** CONTINUING DATA ***************************

This application is a 371 of PCT/IB05/51580 05/13/2005

**** FOREIGN APPLICATIONS ***************************

EUROPEAN PATENT OFFICE (EPO) 04102189.0 05/18/2004

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

06/21/2007

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☑ Yes ☐ No	☑ Yes ☐ No	/MICHAEL ALSIP/ Examiner's Signature	☐ Initials	NETHERLANDS	2	14	3

ADDRESS

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510
UNITED STATES

TITLE

Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips

FILING FEE RECEIVED		
900	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Atty. Docket: NL 040529
ANDREI RADULESCU ET AL.	Confirmation No. 4172
Serial No. 11/569,083	Group Art Unit: 2186
Filed: NOVEMBER 14, 2006	Examiner: ALSIP, M.

Title: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

Mail Stop Amendment
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action mailed on July 8, 2009, please amend the above-identified application and consider the remarks as follows:

IN THE ABSTRACT

Please delete the current Abstract in its entirety and substitute therefor the enclosed New Abstract.

NEW ABSTRACT

An integrated circuit includes a plurality of processing modules coupled by a network. A first processing module communicates with a second processing module based on transactions. A first wrapper means associated to the second processing module buffers data from the second processing module to be transferred over the network until a first amount of data is buffered and then transfers the first amount of buffered data to the first processing module.

IN THE SPECIFICATION

Please amend the specification as follows:

Delete the paragraph on page 4, between lines 20-22 of the specification.

Replace the paragraph spanning pages 9-10, between page 9, line 26, and page 10, line 4 of the specification with the following:

In the first and second embodiment the data, i.e. the buffered data, is ~~send~~ sent over the network in form of packets. The packets are preferably formed in the respective network interfaces NI and should be sufficiently large to be transferred in an optimal way with regard to the network N. As every packet comprises a packet header, the larger the packets, the smaller the number of required packet headers, which will consequently lead to a reduced overhead and an improved network utilization. The data is buffered until the buffered data reach an optimal packet size such that the buffered data can be transferred over the network. If the amount of buffered

data has not yet reached the optimal packet size, none of the data is transferred over the network N even if transferring a smaller packet size is possible. The burst size is associated to a bus or to the IP view on communication, while the packet length is only applicable when packetization takes place (not necessary for a bus). All of the burst size determination schemes mentioned in the previous paragraph also apply to the optimal packet size determination.

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) ~~Integrated~~ An integrated circuit ~~having~~ comprising:

a plurality of processing modules ~~(M, S)~~ being connected with an interconnect ~~means (N)~~, wherein a first processing module ~~(M)~~ communicates to a second processing module ~~(S)~~ using ~~transactions, comprising:~~ transactions; and

[[-]] a first wrapper ~~means (WM1)~~ associated to said second processing module ~~(S)~~ for buffering data from said second processing module ~~(S)~~ to be transferred over the interconnect ~~means (N)~~ until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered.

2.(Currently Amended) ~~Integrated~~ The integrated circuit according to claim 1, further comprising:

[[-]] a second wrapper ~~means (WM2)~~ associated to said first processing module ~~(M)~~ for buffering data from said first processing module ~~(M)~~ to be transferred over the interconnect ~~means (N)~~ until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered.

3.(Currently Amended) ~~Integrated~~ The integrated circuit according to claim 1, wherein

[[-]] said first wrapper and said second wrapper ~~means (WM1, WM2)~~ are adapted to transfer the buffered data in response to a first and second unbuffer signal or a first and second combination of a group of signals, respectively, even if less than said first and second amount of data is buffered in said first wrapper and said second wrapper ~~means (WM1, WM2)~~.

4.(Currently Amended) ~~Integrated~~ The integrated circuit

according to claim 1, wherein

[[-]] said first wrapper and said second wrapper ~~means (WM1, WM2)~~ are adapted to transfer the buffered data according to a first and second unbuffer flag, respectively, even if less than said first and second amount of data is buffered in said first wrapper and said second wrapper ~~means (WM1, WM2)~~.

5.(Currently Amended) ~~Integrated~~ The integrated circuit according to claim 1, wherein

[[-]] at least one of said first wrapper and said second wrapper ~~means (WM1, WM2)~~ comprises a determination unit ~~(BLDU1, BLDU2)~~ for determining the optimal first or second amount of data to be buffered according to communication properties of the communication between said first and second processing module ~~(M, S)~~.

6.(Currently Amended) ~~Integrated~~ The integrated circuit according to claim 1, wherein

[[-]] at least one of said first and second wrapper ~~means~~

~~(WM1, WM2)~~ comprises a determination unit ~~(BLDU1, BLDU2)~~ for determining the optimal moment for sending the data in said first or second wrapper ~~means (WM1, WM2)~~ according to communication properties of the communication between said first and second processing module ~~(M, S)~~.

7. (Currently Amended) ~~Integrated~~ The integrated circuit according to claim 3, wherein

[[-]] said first unbuffer signal is initiated by said second processing module ~~(S)~~ and said second unbuffer signal is initiated by said first processing module ~~(M)~~.

8. (Currently Amended) ~~Integrated~~ The integrated circuit according to claim 4, wherein

[[-]] the setting of said first unbuffer flag is initiated by said second processing module ~~(S)~~ and the setting of said second unbuffer flag is initiated by said first processing module ~~(M)~~.

9. (Currently Amended) ~~Integrated~~ The integrated circuit

according to claim 3, wherein

[[-]] said first processing module ~~(M)~~ is adapted to initiate said first and/or said second unbuffer signal.

10. (Currently Amended) ~~Integrated~~ The integrated circuit according to claim 4, wherein

[[-]] said first processing module ~~(M)~~ is adapted to initiate the setting of said first and/or second unbuffer flag.

11. (Currently Amended) ~~Integrated~~ The integrated circuit according to claim 1, wherein

[[-]] said first and second processing modules ~~(M, S)~~ communicate with each other using a message-passing communication scheme, wherein the messages contain message header, and wherein

[[-]] said first wrapper and said second wrapper ~~means (WM1, WM2)~~ are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first and second amount of data is buffered in said first wrapper and said second wrapper ~~means (WM1, WM2)~~.

12.(Currently Amended) ~~Integrated~~ The integrated circuit according to claim 1, wherein

[[-]] said first and second processing modules ~~(M, S)~~ communicate with each other using a packet based communication scheme, wherein the packets contain packet header, and wherein

[[-]] said first wrapper and said second wrapper ~~means (WM1, WM2)~~ are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper ~~means (WM1, WM2)~~.

13.(Currently Amended) ~~Method~~ A method for buffering data in an integrated circuit having a plurality of processing modules ~~(M, S)~~ being connected with an interconnect ~~means (N)~~, wherein a first processing module ~~(M)~~ communicates to a second processing module ~~(S)~~ using transactions, comprising the ~~steps~~ method comprising the acts of:

[[-]] buffering data from said second processing module ~~(S)~~

to be transferred over the interconnect ~~means (N)~~ until a first amount of data is ~~buffered, wherein~~ buffered; and

transferring the buffered data ~~are transferred~~ when said first amount of data has been buffered.

14. (Currently Amended) ~~Data~~ A data processing system, comprising:

[[-]] a plurality of processing modules ~~(M, S)~~ being connected with an interconnect ~~means (N)~~, wherein a first processing module ~~(M)~~ communicates to a second processing module ~~(S)~~ using ~~transactions, comprising:~~ transactions; and

[[-]] a first wrapper ~~means (WM1)~~ associated to said second processing module ~~(S)~~ for buffering data from said second processing module ~~(S)~~ to be transferred over the interconnect ~~means (N)~~ until a first amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered.

15. (New) An integrated circuit comprising:

a plurality of processing modules including a first processing module and a second processing module;

a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module; and

a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module;

wherein the first interconnect module includes a first memory for buffering first data from the first processing module until a first amount of data is buffered, and the second interconnect module includes a second memory for buffering second data from the second processing module until a second amount of data is buffered,

the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches a first amount, and the second interconnect

module transferring the second data to the first processing module when the second data buffered in the second memory reaches a second amount.

16. (New) The integrated circuit of claim 15, wherein the plurality of interconnect modules manages the communication connection freeing the plurality of processing modules to perform data processing.

17. (New) The integrated circuit of claim 15, wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first interconnect module has a first determination unit that determines the first burst length and the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection.

18.(New) The integrated circuit of claim 17, wherein the first burst length differs from the second burst length.

19.(New) The integrated circuit of claim 17, wherein the network comprises a communication property device that determines the properties of the network for a requested communication and provides the properties to the first determination unit and the second determination unit for determining the first burst length and the second burst length.

20.(New) The integrated circuit of claim 17, wherein the first interconnect module comprises a first communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second determination

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unit.

21.(New) The integrated circuit of claim 15, wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting reaching the first amount and the second amount.

22.(New) The integrated circuit of claim 21, wherein the first processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously.

23.(New) The integrated circuit of claim 21, wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory.

24.(New) The integrated circuit of claim 15, wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory.

REMARKS

This Amendment is being filed in response to the Office Action mailed July 8, 2009, which has been reviewed and carefully considered. Reconsideration and allowance of the present application in view of the remarks to follow are respectfully requested.

Claims 1-24 are pending in this application, where claims 15-24 have been currently added. Claims 1, 13, 14 and 15 are independent.

Applicants thank the Examiner for acknowledging the claim for priority and receipt of certified copies of all the priority documents.

By means of the present amendment, the current Abstract has been deleted and substituted with the enclosed New Abstract which better conforms to U.S. practice. Further, the specification has been amended to correct certain informalities and for better conformance with U.S. practice.

By means of the present amendment, claims 1-14 have been

amended for non-statutory reasons, such as for better form including beginning the independent claims with 'A', beginning the dependent claims with 'The' instead of 'A', and deleting reference designations typically used in European practice that are known to not limit the scope of the claims. Such amendments to claims 1-14 were not made in order to address issues of patentability and Applicants respectfully reserve all rights under the Doctrine of Equivalents.

In the Office Action, claims 1-14 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 4,228,496 (Katzman) in view of U.S. Patent No. 6,668,308 (Barroso). Applicants respectfully traverse and submit that claims 1-24 are patentable over Katzman and Barroso for at least the following reasons.

At the outset, it is pointed out that Katzman has 42 figures and 96 columns of text qualifying this patent as "complex". Therefore pursuant to 37 CFR 1.104, the Examiner must indicate how the reference is being applied. Further, since the reference is complex, Applicants will confine their remarks to those portions cited by the Examiner, except as otherwise indicated. Applicants

make no representation as to the contents of other portions of the references.

On page 2, line 1, FIGs 1 and 22, column 4, lines 47-67, and column 5, lines 24-61 of Katzman are cited to allegedly show that "wherein the buffered data are transferred when said first amount of data has been buffered," as recited in independent claim 1, and similarly recited in independent claims 13, 14 and 15. Applicants respectfully disagree and submit that FIG 1 merely shows "a multiprocessor system constructed in accordance with one embodiment of the present invention. FIG. 1 shows several processor modules 33 connected by two interprocessor buses 35 (an X bus and a Y bus) with each bus controlled by a bus controller 37. FIG. 1 also shows several dual-port device controllers 41 with each device controller connected to the input/output (I/O) buses 39 of two processor modules." (Katzman, column 10, line 66 to column 11, line 6) Further, "FIG. 22 is a block diagram showing the component parts of a data buffer 189 in the control part of a device controller 41. (Katzman, column 12, lines 12-14)

Further, column 4, lines 47-67 of Katzman recite that each

processor module interprocessor control for communications over the interprocessor buses. The interprocessor control includes fast buffers "which can be emptied and filled by the central processing unit without interfering with the interprocessor bus." (Katzman, column 4, lines 52-54) Column 4, lines 60-64 further recite that "[b]ecause the interprocessor bus operates asynchronously with each particular central processing unit, each inqueue and outqueue buffer is clocked either by the processor module or by the bus controller, but not by both simultaneously." Column 4, line 65 to column 5, line 1 further recite that "[e]ach inqueue buffer and outqueue buffer therefore has associated with it in the interprocessor control some logic that operates in synchronism with the bus clock and other logic that operates in synchronism with the central processing unit clock."

In addition, column 5, lines 24-61 of Katzman recite that the bus controller includes an individual select line, where select lines are used "in combination with a send command to let the sender processor module know the time frame for sending." (Katzman, column 5, lines 34-36) As recited on column 5, lines 49-

61, several data block transfers between different sender-receiver pairs of processor modules are interleaved on the interprocessor bus. Further, each processor module memory includes a separate buffer for each combination of a processor module and an interprocessor bus, and each memory includes a bus receive table for directing incoming data from an interprocessor bus to a specified location in a related buffer in the memory of a receiver processor module.

It is respectfully submitted that Katzman does not disclose or suggest the present invention as recited in independent claim 1, and similarly recited in independent claims 13, 14 and 15 which, amongst other patentable elements, recites (illustrative emphasis provided):

> wherein the buffered data are transferred **when said first amount of data has been buffered**.

Transferring the buffered data when the amount of data has been buffered is nowhere disclosed or suggested in Katzman. Barroso is cited to allegedly show other features and does not remedy the deficiencies in Katzman and Barroso.

Accordingly, it is respectfully submitted that independent

claims 1, 13, 14 and 15 are allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 4-12 and 16-24 should also be allowed at least based on their dependence from independent claims 1 and 15.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

By _____
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Attorney for Applicant(s)
October 5, 2009

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(914) 333-9643

Samsung Ex. 1004
Page 112

Electronic Patent Application Fee Transmittal

Application Number:	11569083
Filing Date:	14-Nov-2006
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Filer:	Michael E. Belk/Elissa DeLuccy
Attorney Docket Number:	NL 040529

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1615	4	52	208
Independent claims in excess of 3	1614	1	220	220
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**428**

Electronic Acknowledgement Receipt	
EFS ID:	6227789
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	NL 040529
Receipt Date:	08-OCT-2009
Filing Date:	14-NOV-2006
Time Stamp:	15:10:44
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$428
RAM confirmation Number	1391
Deposit Account	141270
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NL040529US1_Amd_2009_Oct_8.pdf	678102 dd7a09f24ecc4e928fecc5fdc47b38d695f38ed2	yes	24

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Abstract	2	3
Specification	4	5
Claims	6	17
Applicant Arguments/Remarks Made in an Amendment	18	24

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	31970 7e0f68f8986591eb2c0890dfc4ba7e2ffa4e56a3	no	2

Warnings:

Information:

Total Files Size (in bytes):	710072

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt	
EFS ID:	6227789
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	NL 040529
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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	NL 040529	4172

24737 7590 12/15/2009

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
ALSIP, MICHAEL	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
12/15/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/569,083	RADULESCU ET AL.	
	Examiner	Art Unit	
	MICHAEL ALSIP	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 21** is objected to because of the following informalities: In the final line of the claim the phrase “waiting reaching" is used. The Examiner is interpreting this to mean “waiting to reach”. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman et al. (US 4,228,496) and further in view of Barroso et al. (US 6,668,308).

4. Consider **claims 1, 13 and 14**, Katzman et al. discloses a method, data processing system and **integrated circuit comprising** a plurality of processing modules being connected with an interconnect, wherein a first processing module

communicates to a second processing module using transactions (Fig. 2, first ¶ of the abstract); and a first wrapper associated to said second processing module for buffering data from said second processing module to be transferred over the interconnect until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper means" is considered to by a buffer or queue like memory).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

5. Consider **claim 2** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose further comprising a second wrapper associated to said first processing module for buffering data from said first processing module to be transferred over the

interconnect until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where each inter-processor control for each processor as an input and output buffer for sending and receiving data).

6. Consider **claim 3** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first **wrapper** and **said** second wrapper are adapted to transfer the buffered data in response to a first and second unbuffer signal or a first and second combination of a group of signals, respectively, even if less than said first and second amount of data is buffered in said first **wrapper** and **said** second wrapper (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task).

7. Consider **claim 4** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first **wrapper** and **said** second wrapper are adapted to transfer the buffered data according to a first and second unbuffer flag, respectively, even if less than said first and second amount of data is buffered in said first **wrapper** and **said** second wrapper (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed flags.).

8. Consider **claim 5** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein at least one of said first **wrapper** and **said** second wrapper comprises a determination unit for determining the optimal first or second amount of data to be buffered according to communication properties of the communication between said first and second processing module (Col. 7 lines 8-37).

9. Consider **claim 6** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein at least one of said first and second wrapper comprises a determination unit for determining the optimal moment for sending the data in said first or second wrapper according to communication properties of the communication between said first and second processing module (Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task of sending the data at the appropriate time.).

10. Consider **claim 7** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. disclose wherein said first unbuffer signal is initiated by said second processing module and said second unbuffer signal is initiated by said first processing module (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted

signals are used by each processor to communicate and receive data packets for any other processor).

11. Consider **claim 8** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. disclose wherein the setting of said first unbuffer flag is initiated by said second processing module and the setting of said second unbuffer flag is initiated by said first processing module (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

12. Consider **claim 9** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. disclose wherein said first processing module is adapted to initiate said first and/or said second unbuffer signal (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor.).

13. Consider **claim 10** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. disclose wherein said first processing module is adapted to initiate the setting of said first and/or second unbuffer flag (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

14. Consider **claim 11** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first and second processing modules communicate with each other using a message-passing communication scheme, wherein the messages contain message header, **and wherein** said first **wrapper** and **said** second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first **wrapper** and **said** second amount of data is buffered in said first and second wrapper (Col. 31 lines 3-52, where the control packet is considered the head of the message and this identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor).

15. Consider **claim 12** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first and second processing modules communicate

with each other using a packet based communication scheme, wherein the packets contain packet header, **and wherein** said first **wrapper** and **said** second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first and second amount of data is buffered in said first and second wrapper (Katzman et al.: Col. 31 lines 3-52, where the control packet identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor and Barroso et al.: Col. 14 lines 36-45, discloses that data-less transactions are 128-bits long and that data packets have the same 128-bit header format, disclosing that both types have headers).

16. Consider **claim 15**, Katzman et al. discloses an integrated circuit comprising: a plurality of processing modules including a first processing module and a second processing module (Fig. 2, first ¶ of the abstract); a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module (Fig. 1, 19 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61); and a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module (fig. 1); wherein the first interconnect module includes a first memory for buffering first data from the first processing module until a first amount of data is buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61), and the second

interconnect module includes a second memory for buffering second data from the second processing module until a second amount of data is buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61), the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches a first amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches a second amount (Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

17. Consider **claim 16** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. disclose wherein the plurality of interconnect modules manages the

communication connection freeing the plurality of processing modules to perform data processing (col. 5 lines 13-22, Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32).

18. Consider **claim 17** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first interconnect module has a first determination unit that determines the first burst length and the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where there are variable burst lengths and the length is determined by various attributes including the network of buses providing the communication path).

19. Consider **claim 18** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the first burst length differs from the second burst length (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53).

20. Consider **claim 19** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the network comprises a communication property device that determines the properties of the network for a requested communication and

provides the properties to the first determination unit and the second determination unit for determining the first burst length and the second burst length (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where the burst time and length are dynamic and depend on many changing parameters which determine what these two parameters will be and circuitry is making these determinations).

21. Consider **claim 20** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the first interconnect module comprises a first communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second determination unit (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where the burst time and length are dynamic and depend on many changing parameters which determine what these two parameters will be and circuitry is making these determinations).

22. Consider **claim 21** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting reaching the first amount and the second amount (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and

Col. 27 lines 17-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed command.).

23. Consider **claim 22** as applied to **claim 21** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously (col. 4 lines 51-59, col. 6 lines 28-33).

24. Consider **claim 23** as applied to **claim 21** above, Katzman et al. in view of Barroso et al. discloses wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory (Col. 16 lines 17-21 and 39-51, Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where requests for services or data can be request by one processor to another which cases that data to be loaded into the output queue and sent to the requesting processor).

25. Consider **claim 24** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory (Col. 16 lines 17-29 and 39-51, Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27

lines 17-32, where the processor can send a message to send/ flush the data out of the out queue to another processor).

Response to Arguments

26. Applicant's arguments filed 10/08/2009 have been fully considered but they are not persuasive.

27. The Applicant first argues that Katzman qualifies as complex pursuant to 37 CFR 1.104 due to the number of figures and columns. Therefore stating that the Examiner must indicate how the reference is being applied and because of the complexity of the reference, only the cited portions will be used and that no representation of the rest of the reference is made. However the Examiner has found nothing in 37 CFR 1.104 that defines a reference as complex by the number of figures and columns, further 37 CFR 1.104 states that "When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable". The Examiner has clearly done this by citing specific figures and column/line locations of the Katzman reference for each claim and therefore has meet the requirements of 37 CFR 1.104. Also, whether the reference is complex or not, the Applicant is still responsible for reviewing the reference as a whole, not just sections cited by the Examiner.

28. The Applicant second argues that Katzman does not disclose the limitation: “wherein the buffered data are transferred when said first amount of data has been buffered”. Further stating that: "transferring the buffered data **when the amount** of data has been **buffered** is nowhere disclosed or suggested in Katzman. However the claim

language does not disclose how much data a first amount is, therefore a first amount can be any amount of data and Katzman discloses having outqueues which fill with data and then are sent out across the inter-processor bus, the outqueue can send up to fifteen words at a time and a first amount can be one to fifteen words (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 16 lines 17-29 and 39-51, Col. 18 lines 5-9, Col. 22-23 lines 24-32 and Col. 27 lines 17-32).

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Michael Alsip
Examiner
Art Unit 2186

/Michael Alsip/
Examiner, Art Unit 2186

December 9, 2009

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	Art Unit
	MICHAEL ALSIP	2186

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/02/2009	12/09/2009							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
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	20		✓							
	21		✓							
	22		✓							
	23		✓							

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	15075	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
L3	1	(koninklijke philips electronics).as. burst flush module buffer$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
L4	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L5	723	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L6	368	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L7	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L8	61	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

L9	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L10	43	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L11	1746	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L12	298	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L13	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L14	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L15	310	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L16	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

L17	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L18	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
L19	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
L20	104	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L21	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L22	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L23	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L24	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L25	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

L26	340	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L27	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L28	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L29	151	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L30	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L31	256	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L32	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L33	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

L34	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L35	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
L36	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S1	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 12:45
S2	700	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:48
S3	356	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:50
S4	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:58
S5	52	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:59

S6	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:04
S7	42	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:20
S8	1640	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S9	286	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S10	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:26
S11	11	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28
S12	298	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28
S13	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:29

S14	39	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:35
S15	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:36
S16	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:39
S17	104	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S18	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S19	182	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S20	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S21	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S22	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:17

S23	325	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:19
S24	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:20
S25	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 11:31
S26	145	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S27	10	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S28	245	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S29	13	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S30	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05

S31	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S32	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S33	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05

12/9/2009 3:26:59 PM
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	Art Unit
	MICHAEL ALSIP	2186

SEARCHED

Class	Subclass	Date	Examiner
711	118 limited w/ text	12/9/2009	MA
711	141 limited w/ text	12/9/2009	MA
710	57 limited w/ text	12/9/2009	MA
710	100 limited w/ text	12/9/2009	MA

SEARCH NOTES

Search Notes	Date	Examiner
inventor name and assignee search in eDAN and EAST	12/9/2009	MA
class/subclass and keyword search in EAST	12/9/2009	MA

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

/MICHAEL ALSIP/ Examiner.Art Unit 2186	

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2186

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Atty. Docket: NL 040529
ANDREI RADULESCU ET AL.	Confirmation No. 4172
Serial No. 11/569,083	Group Art Unit: 2186
Filed: NOVEMBER 14, 2006	Examiner: ALSIP, MICHAEL

Title: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

Mail Stop AF
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER §1.116

Sir:

In response to the Final Office Action mailed on December 15, 2009, please amend the above-identified application and consider the remarks as follows:

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) An integrated circuit comprising:

a plurality of processing modules being connected with an interconnect, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests; ~~and~~

a first wrapper associated to ~~said second processing module~~ the slave for buffering data from ~~said second processing module~~ the slave to be transferred over the interconnect to the master until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered, and wherein the first wrapper is connected between the slave and the interconnect; and

a second wrapper connected between the master and the interconnect for buffering data from the master to be transferred over the interconnect until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered, and wherein the second wrapper is connected between the master and the interconnect.

Claim 2 (Canceled)

3.(Currently Amended) The integrated circuit according to claim 1, wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to a first unbuffer signal and a second unbuffer signal ~~or a first and second combination of a group of signals~~, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

4.(Currently Amended) The integrated circuit according to claim 1, wherein said first wrapper and said second wrapper are adapted to transfer the buffered data according to a first unbuffer flag and a second unbuffer flag, respectively, even if less than

said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

5.(Currently Amended) The integrated circuit according to claim 1, wherein at least one of said first wrapper and said second wrapper comprises a determination unit for determining ~~the~~ an optimal first or second amount of data to be buffered according to communication properties of the communication between ~~said first and second processing module~~ the master and the slave.

6.(Currently Amended) The integrated circuit according to claim 1, wherein at least one of said first wrapper and said second wrapper comprises a determination unit for determining ~~the~~ an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between ~~said first and second processing module~~ the master and the slave.

7.(Currently Amended) The integrated circuit according to claim 3, wherein said first unbuffer signal is initiated by ~~said second processing module~~ the slave and said second unbuffer signal

is initiated by ~~said first processing module~~ the master.

8. (Currently Amended) The integrated circuit according to claim 4, wherein ~~the~~ setting of said first unbuffer flag is initiated by ~~said second processing module~~ the slave and ~~the~~ setting of said second unbuffer flag is initiated by ~~said first processing module~~ the master.

9. (Currently Amended) The integrated circuit according to claim 3, wherein said ~~first processing module~~ the master is adapted to initiate said first unbuffer signal ~~and/or~~ and said second unbuffer signal.

10. (Currently Amended) The integrated circuit according to claim 4, wherein ~~said first processing module~~ the master is adapted to initiate ~~the~~ setting of said first ~~and/or~~ and second unbuffer flag.

11. (Currently Amended) The integrated circuit according to claim 1, wherein ~~said first and second processing modules~~ the master and the slave communicate with each other using messages of

a message-passing communication scheme, wherein the messages contain a message header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

12. (Currently Amended) The integrated circuit according to claim 1, wherein ~~said first and second processing modules~~ the master and the slave communicate with each other using packets of a packet based communication scheme, wherein the packets contain a packet header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper.

13. (Currently Amended) A method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect through wrappers, wherein a first processing module communicates to a second processing module using

transactions, comprising the method comprising the acts of:

configuring the first processing module as a master the provides requests;

configuring the second processing module as a slave the provides responses to the requests;

connecting the master to a master wrapper of the wrappers;

connecting the master wrapper to the interconnect;

connecting the slave to a slave wrapper of the wrappers;

connecting the slave wrapper to the interconnect;

buffering by the slave wrapper data from ~~said second processing module~~ the slave to be transferred over the interconnect until a first amount of data is buffered slave wrapper data; ~~and~~

transferring the buffered data when said first amount of data has been buffered;

buffering by the master wrapper data from the master to be transferred over the interconnect until a second amount of data is buffered;

transferring the buffered data when said second amount of data has been buffered by the master wrapper data.

14.(Currently Amended) A data processing system, comprising:

a plurality of processing modules being connected with an interconnect, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests; and

a first wrapper associated to ~~said second processing module~~ the slave for buffering data from ~~said second processing module~~ the slave to be transferred over the interconnect until a first amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered, and wherein the first wrapper is connected between the slave and the interconnect; and

a second wrapper connected between the master and the interconnect for buffering data from the master to be transferred over the interconnect until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered, and wherein the second wrapper is connected between the master and the interconnect.

15. (Previously Presented) An integrated circuit comprising:

a plurality of processing modules including a first processing

module and a second processing module;

a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module; and

a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module;

wherein the first interconnect module includes a first memory for buffering first data from the first processing module until a first amount of data is buffered, and the second interconnect module includes a second memory for buffering second data from the second processing module until a second amount of data is buffered,

the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches a first amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches a second amount.

16.(Previously Presented) The integrated circuit of claim 15, wherein the plurality of interconnect modules manages the communication connection freeing the plurality of processing modules to perform data processing.

17.(Previously Presented) The integrated circuit of claim 15, wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first interconnect module has a first determination unit that determines the first burst length and the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection.

18.(Previously Presented) The integrated circuit of claim 17, wherein the first burst length differs from the second burst length.

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19.(Previously Presented) The integrated circuit of claim 17, wherein the network comprises a communication property device that determines the properties of the network for a requested communication and provides the properties to the first determination unit and the second determination unit for determining the first burst length and the second burst length.

20.(Previously Presented) The integrated circuit of claim 17, wherein the first interconnect module comprises a first communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second determination unit.

21.(Currently Amended) The integrated circuit of claim 15, wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data

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are sent without waiting ~~reaching~~ to reach the first amount and the second amount.

22. (Previously Presented) The integrated circuit of claim 21, wherein the first processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously.

23. (Previously Presented) The integrated circuit of claim 21, wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory.

24. (Previously Presented) The integrated circuit of claim 15, wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory.

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REMARKS

This Amendment is being filed in response to the Final Office Action mailed December 15, 2009, which has been reviewed and carefully considered. By means of the present amendment, independent claims 1, 13 and 14 have been amended for better form and to include features similar to that of independent claim 15. Accordingly no new issues have been introduced that require a new search, and thus entry of the present amendment is respectfully requested.

Claims 1 and 3-24 are pending in this application, where claim 2 has been currently canceled without prejudice. Claims 1, 13, 14 and 15 are independent.

In the Final Office Action, the Examiner objected to claim 21 for a certain informality. In response, claim 21 has been amended in accordance with the Examiner's suggestions. Accordingly, withdrawal of the objection to claim 21 is respectfully requested.

In Final the Office Action, claims 1-24 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 4,228,496 (Katzman) in view of U.S. Patent No. 6,668,308 (Barroso). Applicants respectfully traverse and submit that claims 1 and 3-24 are patentable over Katzman and Barroso for at least the following reasons.

Katzman is directed to a multiprocessor system, that includes separate processor modules 33 which are interconnected for parallel processing using two redundant interprocessor buses 35 dedicated exclusively to interprocessor communication. The buses 35 each includes a bus controller 37. As clearly shown in FIG 1, the bus controllers 37 are only connected to the buses 35, without any direct connection to the processor modules 33. Further, the processor modules 33 are directly connected to the buses 35 without any buffers between the processor modules 33 and the buses 35.

In stark contrast, the present invention as recited in independent claim 1, and similarly recited in independent claims 13, 14 and 15, amongst other patentable elements recites (illustrative emphasis provided):

> wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests; ...
> wherein the first wrapper is connected between the slave and the interconnect; and ...
> wherein the second wrapper is connected between the master and the interconnect.

Katzman does not even disclose or suggest any master slave relationship between the processor modules 33. Even, assuming arguendo, that somehow this feature is shown in Katzman, there is

still no disclosure or suggestion in Katzman of a wrapper (for buffering data) which is connected between the slave and the interconnect, or between the master and the interconnect, as recited in independent claims 1, 13, 14 and 15. Rather, FIG 1 of Katzman clearly shows that the processor modules 33 are directly connected to the buses 35 without any buffers therebetween, and the bus controller 37 is NOT between the processor modules 33 and the bus 35. Barroso is cited to allegedly show other features and does not remedy the deficiencies in Katzman and Barroso.

Accordingly, it is respectfully submitted that independent claims 1, 13, 14 and 15 are allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 3-12 and 16-24 should also be allowed at least based on their dependence from independent claims 1 and 15.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of

the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

By _____
Dicran Halajian, Reg. 39,703
Attorney for Applicant(s)
February 8, 2010

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Briarcliff Manor, NY 10510-8001
(914) 333-9643

Electronic Acknowledgement Receipt

EFS ID:	6989423
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	NL 040529
Receipt Date:	11-FEB-2010
Filing Date:	14-NOV-2006
Time Stamp:	10:06:10
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NL040529US1_116Amd_2010_Feb_11.pdf	566430 a37617fe370254cae4c2ab885e96df5cd44495ab	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment After Final	1	1
	Claims	2	12
	Applicant Arguments/Remarks Made in an Amendment	13	16
Warnings:			
Information:			
	Total Files Size (in bytes):	566430	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2186

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Atty. Docket: NL 040529
ANDREI RADULESCU ET AL.	Confirmation No. 4172
Serial No. 11/569,083	Group Art Unit: 2186
Filed: NOVEMBER 14, 2006	Examiner: ALSIP, MICHAEL

Title: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

Mail Stop AF
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER §1.116

Sir:

In response to the Final Office Action mailed on December 15, 2009, please amend the above-identified application and consider the remarks as follows:

DO NOT ENTER: /M.A./

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	NL 040529	4172

24737 7590 02/19/2010

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
ALSIP, MICHAEL	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
02/19/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 11/569,083	**Applicant(s)** RADULESCU ET AL.	
	Examiner MICHAEL ALSIP	**Art Unit** 2186	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 11 February 2010 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-24*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: The arguments pertain to the newly amended claim limitations, which have not been entered and therefore these arguments have not been addressed at this time.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Sheng-Jen Tsai/
Primary Examiner, Art Unit 2186

/Michael Alsip/
Examiner, Art Unit 2186

Continuation of 3. NOTE: The amendments made to the claim language are substantial and require further consideration and possible search on the part of the Examiner.

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	11569083	Filing Date	1006-11-14	Docket Number (if applicable)	NL040529US1	Art Unit	2186
First Named Inventor	Andrei Radulescu			Examiner Name	Michael Alsip		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☐ Enclosed

☐ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 141270

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Signature of Registered U.S. Patent Practitioner			
Signature	/Michael E. Belk/	Date (YYYY-MM-DD)	2010-03-08
Name	Michael E. Belk	Registration Number	33357

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	11569083
Filing Date:	14-Nov-2006
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Filer:	Michael E. Belk/Elissa DeLuccy
Attorney Docket Number:	NL040529US1

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt

EFS ID:	7156768
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	NL040529US1
Receipt Date:	08-MAR-2010
Filing Date:	14-NOV-2006
Time Stamp:	08:09:30
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810
RAM confirmation Number	7849
Deposit Account	141270
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

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Application Number	11569083
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First Named Inventor	Andrei Radulescu
Art Unit	2186
Examiner Name	Michael Alsip
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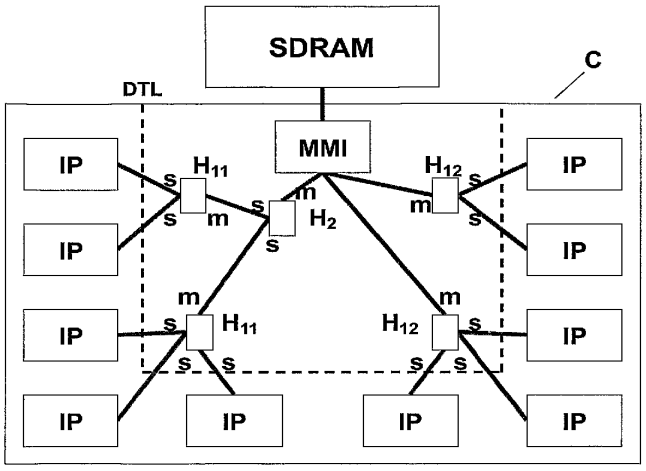
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[Continued on next page]

(54) Title: DATA PROCESSING SYSTEM



(57) Abstract: The disclosed data processing system comprises a memory means (SDRAM), a plurality of data processing means (IP) provided for accessing to said memory means (SDRAM), and a communication interface means coupled between said memory means (SDRAM) and said plurality of data processing means (IP), said communication interface means including a network of nodes (H 11, H 12, H2), each node comprising at least one slave port (s) for receiving a memory access request from a data processing means (IP) or from a previous node and at least one master port (m) for issuing a memory access request to a next node or to said memory means (SDRAM) in accordance with the memory access request received at said slave port (s), wherein said at least one slave port (s) is connected to a master port (m) of a previous node or to one of said data processing means (IP) and said at least one master port (m) is connected to a slave port (s) of a next node or to said memory means (SDRAM).

WO 2005/026964 A2

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Data processing system

FIELD OF THE INVENTION

The present invention relates to a data processing system comprising a memory means and a plurality of data processing means provided for accessing to said memory means.

BACKGROUND OF THE INVENTION

Such a system is usually called a multi processor system wherein the data processing means operate to some extent independently from each other and carry out certain processes. The plurality of data processing means have access to the memory means so that the memory means is shared by the plurality of data processing means. Usually, only a single common memory means is provided in such a data processing system, and the plurality of data processing means are provided on a single common chip, whereas the memory means resides outside such chip as an off-chip memory. As the internal details of said processing means are outside the scope of this invention, they will simply be referred to as intellectual property (IP) means.

As an example of such a shared-memory data processing system, a digital video platform (DVP) system in its basic form is shown in Figure 1. It comprises a plurality of data processing units IP which communicate via an off-chip memory SDRAM. The data processing units IP can be programmable devices like CPUs, application-specific hardware blocks, subsystems with a complex internal structure etc. Further provided in the system of Figure 1 is a device transaction level (DTL) interface DTL via which each data processing unit IP is interfaced to a central main memory (MMI) interface MMI which arbitrates the accesses to the off-chip memory SDRAM. All IP-to-IP communication is done via logical buffers (not shown) mapped in the off-chip memory SDRAM. Usually, one of the data processing units IP is a CPU (central processing unit) which manages the configuration of a task graph by programming the data processing units via a network of memory mapped configuration registers (not shown). A synchronization among the data processing units IP is also handled in a centralized way by this CPU which notifies the data processing units IP via the memory mapped input/output network whether full or empty buffers are available. The

data processing units IP notify the CPU via interrupt lines (not shown) whether these buffers have run empty or have been filled.

The mechanism used for synchronization results in that the buffers provided in the off-chip memory SDRAM must be rather large in order to keep the rate of the interrupts to the CPU low. For example, video processing units often synchronize at a coarse grain (e.g. a frame) even though from a functional perspective they could synchronize at a finer grain (e.g. a line).

Since such a data processing system comprises a shared memory architecture, there is a single address space which is accessible to all data processing means. This simplifies the programming model. Further, the common memory means helps to provide cost-effective system solutions.

However, such a data processing system in its basic form has a number of disadvantages which will become more eminent as technology progresses. Namely, as the number of data processing means increases, the number of connections to the memory interface increases resulting in a more complex memory interface. In particular, the arbitration among the different data processing means becomes more complex. Further, wire length may become a problem for the data processing means which are located far from the memory interface so that many long wires may cause wiring congestion as well as time delay and power consumption problems. A further critical disadvantage is that there is a potential bottleneck when bandwidth requirements increase further; the bandwidth to the (off-chip) memory means is restricted by certain aspects like signalling speed and pin count of the off-chip interconnect.

GB 2 233 480 A discloses a multi-processor data processing system wherein each processor has a local memory. The local memories together form the main memory of the system, and any processor can access any memory, whether it is local to that processor or remote. Each processor has an interface circuit which determines whether a memory access request relates to the local memory or to a remote memory, and routes the request to the appropriate memory, wherein remote requests are routed over a bus. Whenever a write access is made to the local memory, a dummy write request is routed over the bus to all the other processors. Each processor monitors all write requests on the bus, and if a copy of the location specified in the request is held in a local cache memory, such copy is invalidated so as to ensure cache consistency.

US 5,261,067 A discloses an apparatus and a method for ensuring data cache content integrity among parallel processors. Each processor has a data cache to store results

of intermediate calculations. The data cache of each processor is synchronized with each other through the use of synchronization intervals. During entry of a synchronization interval, modified data variables contained in an individual cache are written back to a shared memory. The unmodified data contained in a data cache is flushed from the memory. During exiting of a synchronization interval, data variables which were not modified since entry into the synchronization interval are also flushed. By retaining modified data cache values in the individual processors which computed the modified values, unnecessary access to shared memory is avoided.

US 6,253,290 B1 describes a multiprocessor system having a plurality of processor units each including a CPU and a local cache memory connected to the CPU. The CPUs have their shared bus terminals connected to a global shared bus, and local cache memories have their bus terminals connected to a global unshared bus. The global shared bus is connected to an external shared memory for storing shared information used in common by the CPUs, and the global unshared bus is connected to an external unshared memory for storing unshared information used by the CPUs.

US 6,282,708 B1 discloses a method for structuring a multi-instruction computer program as containing a plurality of basic blocks which each compose from internal instructions and external instructions organized in an internal directed acyclic graph. A guarding is executed on successor instructions which each collectively emanate from a respectively associated single predecessor instruction. A subset of joined instructions which converge onto a single join/target instruction are then unconditionally joined. This is accomplished by letting each respective instruction in the subset of joined instructions be executed under mutually non-related conditions, specifying all operations with respect to a jump instruction, specifying all operations which must have been executed previously and linking various basic blocks comprising subsets of successor instructions in a directed acyclic graph which allows parallel execution of any further subset of instructions contained therein.

SUMMARY OF THE INVENTION

An object of the present invention is to overcome the above mentioned drawbacks and to improve the data processing system so as to avoid a communication bottleneck between the data processing and the memory means even when the bandwidth requirements increase further, to decrease the number of connections to the memory interface, and to reduce the wire length.

In order to achieve the above and further objects, according to the present invention there is provided a data processing system comprising a memory means and a plurality of data processing means provided for accessing to said memory means, characterized by a communication interface means coupled between said memory means and said plurality of data processing means, said communication interface means including a network of nodes, each node comprising at least one slave port for receiving a memory access request from a data processing means or from a previous node and at least one master port for issueing a memory access request to a next node or to said memory means in accordance with the memory access request received at said slave port, wherein said at least one slave port is connected to a master port of a previous node or to one of said data processing means and said at least one master port is connected to a slave port of a next node or to said memory means.

Due to the construction according to the invention, the number of connections to the memory means is reduced. This is achieved by the provision of a specific physical organisation of a logically shared memory architecture wherein the communication interface means includes a network of a plurality of nodes having slave ports receiving memory access requests from the data processing means and at least one master port issuing a specific memory access request to the memory means. Typically, the number of master ports of a node is smaller than the number of slave ports of that node. As a result, the complexity of the memory interface is decreased since the number of clients connected thereto is reduced. Further, due to the interconnection of the communication interface means, the length of individual wires and, thus, the total length of wires are reduced so as to help avoiding wire congestion.

The communication interface means includes a network of a plurality of node means, wherein each node means comprises at least one slave port for receiving a memory access request and at least one master port for issuing a memory access request in accordance with the memory access request received at said slave port(s), wherein the number of said slave ports can be higher than the number of said master ports. So, the communication interface means according to the present invention includes a node structure for the connections between the data processing means and the memory means wherein multiple data processing means can be connected to a node means via its slave ports, whereas each node means has only one or a few master ports. Since the slave ports of a node means are uniform in that they offer the same services, it is transparent to the node means whether a slave port attaches a data processing means or another node means. A request for a memory

access issued by a data processing means is passed to one of the node means to which it is connected. An advantage of the concept of the invention is that it can be introduced in a step-wise manner. Namely, a first chip to adopt the concept of the invention could use a new node means for just a few data processing means; and in later chips, the number of node means may gradually rise, and the facilities of the communication interface means of the invention may be used for more and more communication between data processing means. In case a node means has multiple master ports, a single port is selected for forwarding, for example, in accordance with an address range discrimination.

In a first embodiment of the invention, each of the slave ports of said node means is connected to one of said plurality of data processing means and the master ports of said node means are coupled to said memory means. So, all the node means are provided in the same level, and the data processing means are coupled to the memory means via such single level of node means. The data processing means can issue memory access requests to an associated node means which forwards the request to the memory means.

In an alternative second embodiment, the network of node means is hierarchically structured having the data processing means as leaves and the node means as nodes.

The plurality of node means can be arranged in a directed acyclic graph structure. Each edge of the directed acyclic graph structure corresponds to an interconnect path which serves memory access requests. The edges are directed, and each edge connects a master port of one node means to a slave port of another node means. In case the memory means includes a plurality of memory sections, the acyclic graph structure can result in a set of master ports each providing a connection to a different memory section, in such a way that each data processing means can communicate to one or more memory section(s), thereby allowing multiple data processing means to access different memory sections concurrently, thereby reducing the bandwidth bottleneck. Furthermore, the acyclic graph structure might provide several different paths through the graph leading from one data processing means to one memory section. These different paths can be employed advantageously to further reduce communication bottlenecks or to avoid the use of faulty connections.

Further, in a preferred refinement of the above embodiment, the plurality of node means may be arranged in a tree structure so that one or more data processing mean(s) and/or previous node(s) are connected to a node means via its slave ports, but each node means has only one master port. This simplifies the forwarding process in the node means

and provides connectivity to a single memory section at the root of the node tree that can be accessed by all data processing means.

In this alternative second modification, preferably the plurality of node means include n groups of node means with $n \geq 2$, wherein each of the slave ports of the node means of a first group is connected to one of said plurality of data processing means, the master ports of the node means of the nth group are coupled to said memory means, and each of the slave ports of the node means of the nth group is connected to the master port of the node means of the $(n-1)^{th}$ group. So, the plurality of node means are divided into n groups, wherein each group defines a different level in the structure. If a node means receives a memory access request at one of its slave ports, the request is forwarded to a node means of a higher group or, if the node means is in the highest (i.e. n^{th}) group, to the memory means. With the respect thereto, it should be added that the node structure does not necessarily need to have a uniform depth. Some data processing means may be "close" to the memory means in that only one or two nodes separate them from the memory means, whereas (at the same time) other data processing means may be more "remote" from the memory means in that the memory access requests that they issue have to travel via a large number of nodes.

The above mentioned hierarchical structure of the node means is completely transparent to the data processing means so that no modifications of the data processing means are required.

Preferably, the node means are hubs.

In a further preferred embodiment of the invention, at least one local memory unit is attached to the communication interface, allowing such local memory unit to be selectively accessed to by a memory access request. So, a single address space is distributed over a global memory and such local memory unit(s). The advantage of this embodiment is that the data processing means may exchange data to each other via a local memory unit only instead of using the global memory, resulting in a further reduction of a potential bottleneck risk in the communication, by reducing memory access latency, reducing power consumption, and reducing the use of external memory bandwidth.

Preferably, at least one node means further comprises at least one memory port to which a local memory unit is connected. So, the node means checks whether or not the memory access request refers to the local memory unit(s) attached to such node means by comparing the address of the memory access request with the address ranges associated to the local memory unit(s) attached to such node means. If yes, the memory access is executed on the selected local memory unit. Otherwise, the node means forwards the memory access

request through one of its master ports either to a next node means where the check and "access or forward" is repeated if a local memory unit is also attached to such next node means, or to the memory means.

In a modification of the recently mentioned embodiment, the communication interface means includes a cache controller means for controlling the local memory unit(s) as a cache memory. In this case at least a part of the local memory unit is used to locally store a copy of data residing in other memories reachable via one of its master ports. So, memory access requests can be served locally for a wider address range for which caching behaviour is enabled.

Moreover, the communication interface means may include at least one synchronization means for streaming communication between data processing means. In particular, at least one node means includes said synchronization means for streaming communication between the data processing means directly or indirectly coupled to said node means.

In case a local memory unit is attached to the node means, the local memory unit should have a first-in/first-out (FIFO) function, and the synchronization means comprises a FIFO administration means for controlling said local memory unit(s). The synchronization services can be locally handled when the FIFO administration is locally stored, whereby multiple data processing means can communicate data via the local memory unit(s) attached to the node means; otherwise the synchronization request is forwarded to one of the master ports of the corresponding node means.

In a further preferred embodiment, the communication interface means is provided on a single chip. Moreover, at least a part of the plurality of data processing means may be additionally provided on said single chip.

The above described objects and other aspects of the present invention will be better understood by the following description and the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present invention are described with reference to the drawings in which

Fig. 1 shows a schematic basic block diagram of a DVP system in its basic form according to the prior art;

Fig. 2 shows a schematic basic block diagram of a DVP system including a hub structure according to a first preferred embodiment of the present invention;

Fig. 3 shows a schematic basic block diagram of a DVP system with a hub structure according to a second preferred embodiment of the present invention which further includes on-chip local memories; and

Fig. 4 shows a schematic basic block diagram of a DVP system including a hub structure according to a third preferred embodiment of the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 2 shows a digital video platform (DVP) system having a hub structure according to a first preferred embodiment of the present invention. Like the system shown in Figure 1, the system of Figure 2 comprises a plurality of data processing units IP, which may also be called intellectual property (IP) units, and a memory SDRAM. The data processing units IP can be programmable devices (CPUs), application-specific hardware blocks, subsystems with a complex internal structure etc. All data processing units comprise a device transaction level (DTL) interface. Further, there are provided a plurality of hubs H_{11}, H_{12}, H_2, wherein each hub comprises several slave ports s and one master port m. In the system of Figure 2, the hubs define a network of hubs comprising a first group of hubs H_{11} and H_{12} and a second group consisting of only one hub H_2. The first group of hubs H_{11} and H_{12} define a first level adjacent to the data processing units IP so that the hubs H_{11} and H_{12} of the first group are directly connected to the data processing units IP via its slave ports s. In the embodiment of Figure 2, each hub has only one master port m for connection to the next hub or the memory interface MMI. The hubs H_{11} of the first group are connected via its master ports m to the slave ports s of the hub H_2 of the second group which is connected via its master port m to the memory interface MMI whereas the hubs H_{12} of the first group are directly connected via its master ports m to the memory interface MMI. The memory interface MMI is coupled to the memory SDRAM.

In the embodiment of Figure 2, the network of hubs is organized as a directed acyclic graph (DAG) structure wherein the nodes of the DAG structure are defined by the hubs H_{11}, H_{12} and H_2, and each edge of the DAG structure corresponds to an interconnect path which serves memory access requests. The edges are directed. The DAG structure shown in Figure 2 is restricted to have a tree structure wherein each hub H_{12}, H_{11} and H_2 has one master port only. This simplifies the forwarding process in the hubs, as they do not need to select a master port for each memory request, for example by discriminating ranges on the requested address.

At the slave ports s of the hubs a memory access request is received which is forwarded by the master port m. The slave ports s of a hub are uniform in that they offer the same services. Therefore, it is transparent to the hub whether a slave port s is connected to a data processing unit IP or another hub.

It is noted that many modifications of the structure over the embodiment of Figure 2 are possible and that Figure 2 gives only one example. So, the network of hubs may include more than two levels. Further, the hubs H_{12} may be connected to a next hub higher in the structure. Moreover, a hub may have multiple master ports wherein a single master port is selected for forwarding, for example in accordance with an address range discrimination.

As further shown in Figure 2, the data processing units, the device transaction level DTL, the hubs H_{11}, H_{12} and H_2 and the memory interface MMI reside on a single chip C, whereas the memory SDRAM is provided outside the chip C.

Due to the hub structure shown in Figure 2, the number of clients of the memory interface MMI is reduced. Further, the length of individual wires and, thus, the total length of wires are reduced whereby wire congestion is avoided.

The hierarchical hub structure is completely transparent to the data processing units IP, and no modifications of the data processing units IP are required. Also it does not affect the way synchronization is performed; this may still be handled in a centralized way by means of a memory mapped input/output (not shown) and interrupts via a data processing unit including a CPU.

Figure 3 shows a second preferred embodiment of the present invention which differs from the first embodiment of Figure 2 in that an embedded local memory MEM is attached to each of the hubs. However, with respect thereto it should be noted that in an alternative embodiment local memories are provided for only some of the hubs. The local memories MEM are assigned private segments in the address space; wherein a single address space is provided which is distributed over the off-chip memory SDRAM and the multiple local memories MEM. The data processing units IP perform memory access requests in the usual address-based way, wherein an address can refer to the off-chip memory SDRAM or to an on-chip local memory MEM. All data processing units IP are able to access the off-chip memory SDRAM and a further on-chip local memory MEM attached to the memory interface MMI, but not all data processing units IP are able to access all on-chip local memories MEM attached to the hubs H_{11}, H_{12} and H_2. Namely, the data processing units IP can access only the local memories MEM attached to the hubs on the route to the memory interface MMI.

For the data processing units IP sharing a common hub, a buffered communication can be performed via the local memory MEM attached to that hub. A first-in/first-out (FIFO) buffer used for a communication between the data processing units is mapped to a memory segment of the local memory MEM attached to a common hub, preferably to the common hub H_{11} or H_{12} of the first group being the closest common hub. The data processing units IP are simply instructed to access the data in the address range in which such buffer has been allocated via their DTL interface, but are unaware of the physical location; this is transparent to the data processing units IP. The hubs check the addresses of the memory access requests performed by the data processing units IP and either perform an access to their local memory MEM, if the address is in the specified range, or forward the request up in the hierarchy. The buffers for the IP-to-IP communication can be allocated to the local memories MEM upon configuration, wherein the address range of the buffer is programmed in the hub to which the local memory MEM is attached.

The IP-to-IP communication which is mapped to a communication via an on-chip local memory MEM does not consume expensive bandwidth to the off-chip memory SDRAM. The hub structure should be chosen such that the data processing units IP which need to communicate frequently have a common hub for a communication via the local memory attached to such common hub. For example, video data processing units IP should be in the same sub-tree of the hub structure. Moreover, the total available memory bandwidth is increased significantly. In parallel to accesses to the off-chip memory SDRAM by some data processing units IP, accesses to the on-chip local memories may be performed by data processing units IP located in other (disjunct) sub-trees. Further, the communication via the on-chip local memories MEM is more power efficient and can more easily support higher bandwidth (wider interconnects and memory ports, higher clocks).

As explained above, the data processing units IP can simply access data via their DTL interface, irrespective of whether or not that data is located on-chip (local memory MEM) or off-chip (memory SDRAM). Hence, on-chip communication is transparent to the data processing units IP. This facilitates re-use of the data processing units IP in the proposed configuration.

Special attention should be paid to the synchronization among the data processing units IP. As already mentioned above, in the DVP system synchronization is performed by a data processing unit including a CPU, requiring low rate synchronization at a coarse data grain. This results in larger buffer sizes which can easily be accommodated in the off-chip SDRAM. For on-chip communication, however, smaller buffers should be used,

which requires synchronization at a finer data grain. For the functions performed by many data processing units, synchronization at a finer grain (e.g. line or macro block) is merely logical. However, using an interrupt-based scheme for synchronization at a finer grain would lead to a higher interrupt rate on the CPU.

One solution may be to dedicate more CPU power to synchronization or even to dedicate a special (light-weight) CPU to the synchronization task.

Another attractive solution is to add synchronization support to the hubs. In this case, each hub can perform the synchronization tasks which are related to the (FIFO-based) IP-to-IP communication via the local memory MEM attached to such hub; i.e., per first-in/first-out operation the availability of data and room is administered and signalled to the data processing units IP. As an effect, this supports continuous (autonomous) operation of the data processing units without CPU software intervention, at least as far as communication via local memories is involved.

It is proposed that the data processing units IP need to make abstract synchronization calls at their ports. The infrastructure decides how these synchronization calls are resolved, dependent on how the data processing unit IP is integrated in a system-on-chip. This would not be hardwired in a re-usable data processing unit. For example, if such a port maps to local communication via a local memory, the corresponding hub resolves the synchronization call locally or forwards it to the next higher hub. If the communication is done via the off-chip memory SDRAM, an interrupt may be generated. For the data processing unit IP this is hidden by an "abstract" interface (not shown) which is configured such that it offers a function to the data processing units IP to issue high level requests to the communication interface, but hides from the data processing units how such requests are implemented. When a buffer is provided in the local memory MEM attached to a hub, the port addresses for the synchronization are programmed in the hub together with the address range of the buffer at the configuration time, accordingly.

It is noted that in the scheme presented above the local memories MEM are used for buffered IP-to-IP communication in which no data needs to travel to the off-chip SDRAM at all. This is different from the use of the on-chip local memories as a cache for copying data from the off-chip SDRAM into an on-chip local memory MEM for repeated use.

However, the architecture of Figure 3 could be used to support caching as well, wherein two kinds of caching are distinguished: Transparent caching and IP controlled caching.

With transparent caching, the data processing units IP are not really aware of that data are copied to a local memory MEM, other than that it perceives a different latency in accessing the data. By means of a cache control function, data are copied from/to the off-chip memory SDRAM to/from an on-chip local memory MEM. Such cache control is implemented in a hub. Cache coherency must be resolved either by implementing a hardware cache coherency scheme or by adopting restrictions in the programming model.

With IP-controlled caching, a data processing unit IP itself copies data from the off-chip memory SDRAM to an on-chip local memory for repeated (fine-grain) use. The copies in the on-chip local memory MEM are in a different address range than the corresponding data in the off-chip memory SDRAM. With IP-controlled caching, the data processing units IP are responsible for the coherency. As an example of IP-controlled caching, it may be considered a three-dimensional graphics renderer which 'caches' texture data in an on-chip local memory MEM to perform fine grain accesses on it. This is done by copying the texture data to the address range of the local memory MEM attached to a hub and referring to addresses in that address range when performing the fine grain accesses. In such case, the cache control is performed by the data processing units IP themselves, and this kind of use is different from the transparent use of the on-chip local memory for IP-to-IP communication. Nevertheless, the architecture of Figure 3 supports this kind of use.

Figure 4 shows a third preferred embodiment which differs from the first embodiment of figure 2 in that in addition to a first off-chip memory SDRAM 1 and an associated first memory interface MMI 1 coupled thereto a second off-chip memory SDRAM 2 and an associated second memory interface MMI 2 coupled thereto are provided. Further, there are provided a plurality of hubs H_{11}, H_{12}, H_{21} and H_{22}, wherein the hubs H_{11} and H_{12} each comprises several slave ports s and two master ports m and the hubs H_{21} and H_{22} each comprises two slave ports s and one master port m. So, in the system of figure 4, the hubs define a network of hubs comprising a first group of hubs H_{11} and H_{12} and a second group consisting of hubs H_{21} and H_{22}. The first group of hubs H_{11} and H_{12} define a first level adjacent to the data processing units IP so that the hubs H_{11} and H_{12} of the first group are directly connected to the data processing units IP via its slave ports s. The second group of hubs H_{21} and H_{22} define a second level adjacent to the memory interfaces MMI 1 and MMI 2, wherein the hubs H_{21} and H_{22} each are connected via one of its slave ports to one of the master ports m of the hub H_{11} and further via the other one of its slave ports s to one of the master ports m of the hub H_{12}. Moreover, the hub H_{21} is connected via its master port m to

the first memory interface MMI 1, and the hub H_{22} is connected via its master port m to the second memory interface MMI 2.

So, in the third embodiment of figure 4, the network of hubs is organized as a DAG structure like in the first and second embodiments of figures 2 and 3, respectively, but the data processing units IP have optional access to two off-chip memories SDRAM 1 and SDRAM 2, whereas in the first and second embodiments of figures 2 and 3 there is only communication between a single off-chip memory SDRAM and the data processing units IP. Apart from that two off-chip memories SDRAM 1 and SDRAM 2 are connected to the network of hubs, the operation of the third embodiment of figure 4 is the same as that of the first embodiment of figure 2 so that reference is made to the description of figure 2. Further, in the third embodiment of figure 4 local memories and a synchronisation as described in conjunction with figure 3 may optionally be provided as well.

As described above, the third embodiment of figure 4 comprises two off-chip memories SDRAM 1 and SDRAM 2. However, more than two off-chip memories may be provided as well.

In the above description, it has been presented a next step in the evolution of a multi-processing data system like a DVP platform which allows the use of on-chip local memories MEM to avoid a communication bottleneck to the off-chip memory SDRAM. The use of the local memories MEM for IP-to-IP communication is largely transparent to the data processing units IP.

A further advantage of the above described architecture according to the present invention is that it can be introduced in a stepwise manner. A first chip to adopt the solution can use an on-chip local memory MEM and a new hub (e.g. H_{12}) for just a few data processing units IP which want to communicate via such local memory MEM. In later chips, the number of hubs with local memories may gradually rise, and the on-chip communication facilities may be used for more and more IP-to-IP communication.

Although the invention is described above with reference to examples shown in the attached drawings, it is apparent that the invention is not restricted to it but can vary in many ways within the scope disclosed in the attached claims.

CLAIMS:

1. A data processing system, comprising a memory means (SDRAM) and a plurality of data processing means (IP) provided for accessing to said memory means (SDRAM), characterized by a communication interface means coupled between said memory means (SDRAM) and said plurality of data processing means (IP), said communication interface means including a network of nodes (H_{11}, H_{12}, H_2), each node comprising at least one slave port (s) for receiving a memory access request from a data processing means (IP) or from a previous node and at least one master port (m) for issueing a memory access request to a next node or to said memory means (SDRAM) in accordance with the memory access request received at said slave port (s), wherein said at least one slave port (s) is connected to a master port (m) of a previous node or to one of said data processing means (IP) and said at least one master port (m) is connected to a slave port (s) of a next node or to said memory means (SDRAM).

2. The data processing system according to claim 1, characterized in that at each node means the number of said slave ports (s) is higher than the number of said master ports (m).

3. The data processing system according to claim 1 or 2, characterized in that said network of node means (H_{11}, H_{12}, H_2) is hierarchically structured.

4. The data processing system according to claim 3, characterized in that said plurality of node means (H_{11}, H_{12}, H_2) are arranged in a directed acyclic graph structure.

5. The data processing system according to claim 4, characterized in that said plurality of node means (H_{11}, H_{12}, H_2) are arranged in a tree structure.

6. The data processing system according to at least any one of the preceding claims, characterized in that said plurality of node means (H_{11}, H_{12}, H_2) include n groups of node means with $n \geq 2$, wherein each of the slave ports (s) of the node means (H_{11}) of a first

group is connected to one of said plurality of data processing means (IP), the master ports (m) of the node means (H_2) of the nth group are coupled to said memory means (SDRAM), and each of the slave ports (s) of the node means (H_2) of the nth group is connected to a master port (m) of the node means (H_{11}) of the $(n-1)^{th}$ group.

7. The data processing system according to at least any one of the preceding claims, characterized in that said node means (H_{11}, H_{12}, H_2) are hubs.

8. The data processing system according to at least any one of the preceding claims, characterized in that said communication interface means further includes at least one local memory unit (MEM) adapted to be selectively accessed to by a memory access request.

9. The data processing system according to claim 8, characterized in that at least one node means (H_{11}, H_{12}, H_2) further comprises at least one memory port (mp) to which a local memory unit (MEM) is connected.

10. The data processing system according to claim 8 or 9, characterized in that said communication interface means includes a cache controller means for controlling at least a section of the local memory unit(s) (MEM) as a cache memory.

11. The data processing system according to at least any one of the preceding claims, characterized in that said communication interface means further includes at least one synchronization means for streaming communication between data processing means (IP).

12. The data processing system according to claim 11, characterized in that at least one node means (H_{11}, H_{12}, H_2) includes said synchronization means for streaming communication between the data processing means (IP) directly or indirectly coupled to said node means.

13. The data processing system according to claim 8 as well as to claim 11 or 12, characterized in that the local memory unit(s) (MEM) is (are) configured to provide the storage means for a first-in/first-out function and said synchronization means comprises a first-in/first-out administration means for controlling said local memory unit(s) (MEM).

14. The data processing system according to at least any one of the preceding claims, characterized in that said communication interface means is provided on a single chip (C).

15. The data processing system according to claim 14, characterized in that at least a part of said plurality of data processing means (IP) is additionally provided on said single chip (C).

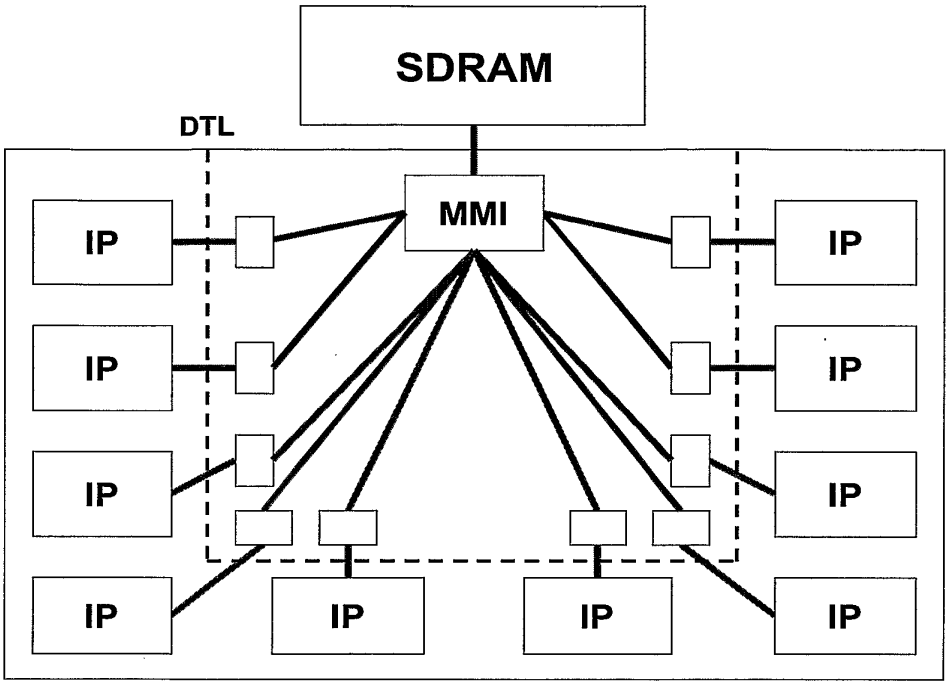


FIG.1

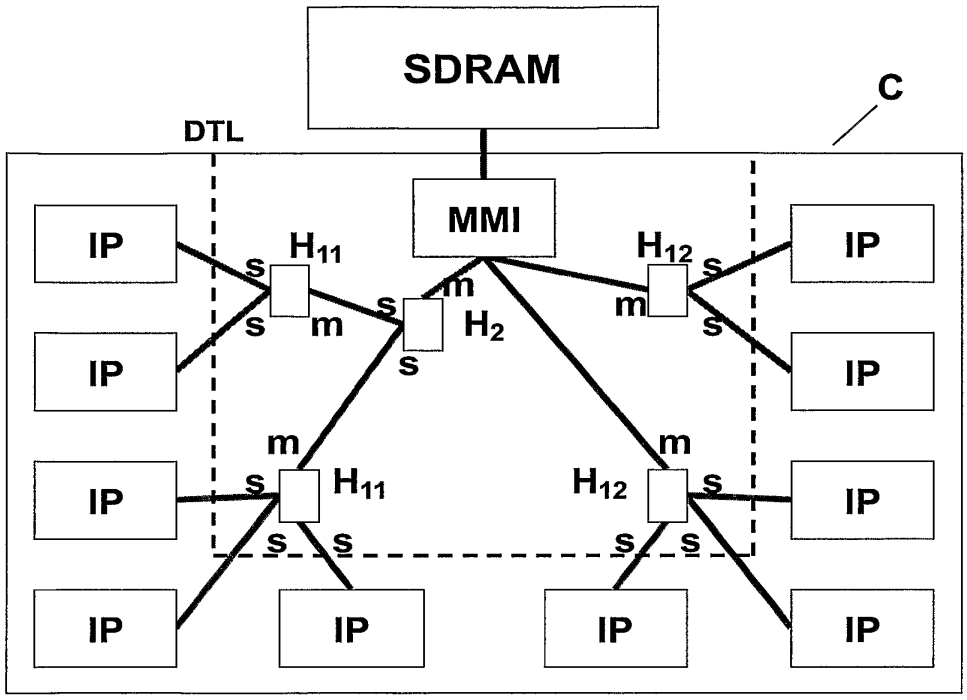


FIG.2

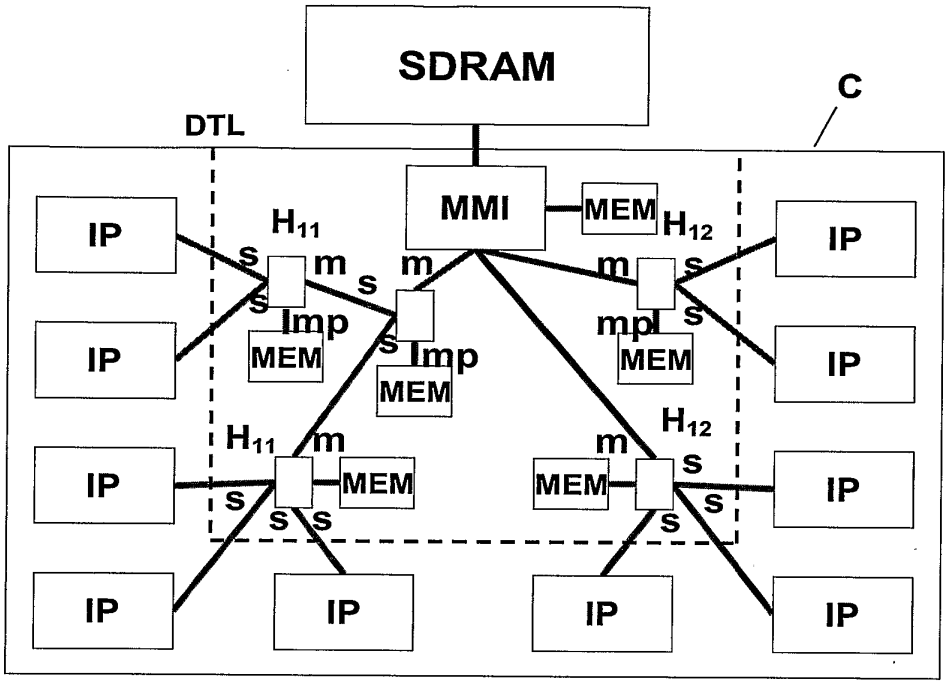


FIG.3

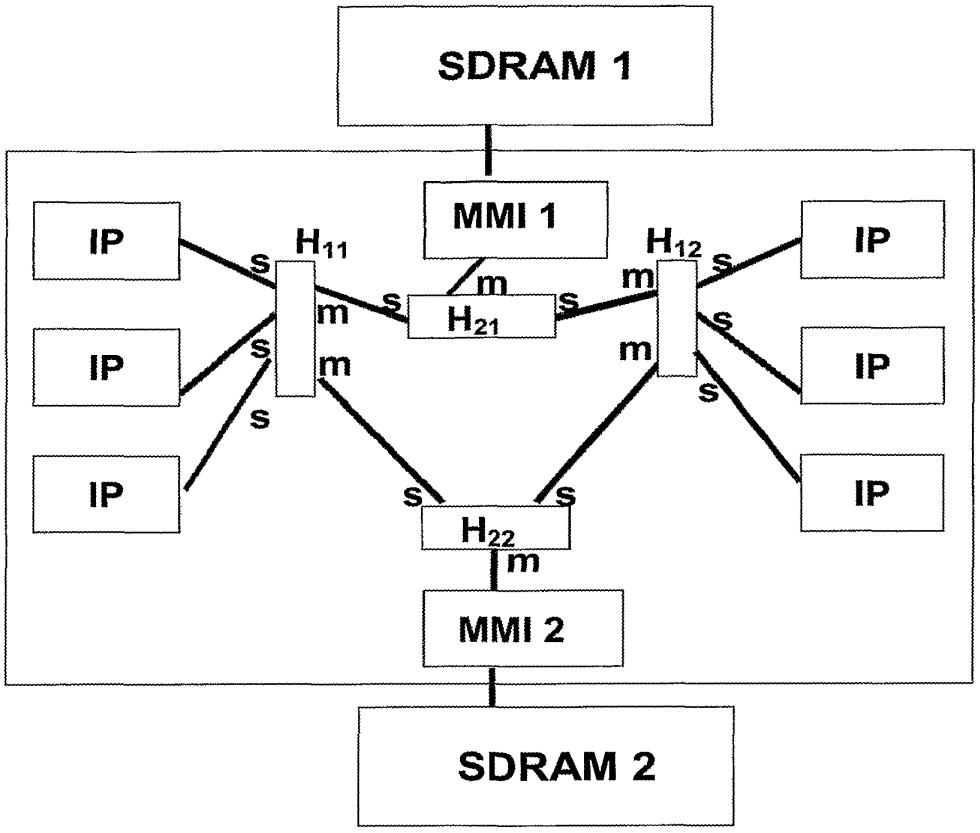


FIG.4

Electronic Acknowledgement Receipt

EFS ID:	7238599
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	NL040529US1
Receipt Date:	18-MAR-2010
Filing Date:	14-NOV-2006
Time Stamp:	15:53:05
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	NL040529US1_IDS.pdf	612175 68b414e2cb2c19f999b6653ead66d2a14be7585e	no	4

Warnings:

Information:

2	Foreign Reference	WO2005026964A2.pdf	998252 d028324e922dfbeab97bf09b84a00d4e1cc1896d	no	22
Warnings:					
Information:					
3	NPL Documents	AMBA_AXI_Protocol.pdf	787763 b57c6d566733551d6972cd78b78c9057f0cd74f6	no	29
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	NL040529US1	4172

24737 7590 03/22/2010

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EXAMINER	
ALSIP, MICHAEL	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
03/22/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/569,083	RADULESCU ET AL.	
	Examiner	Art Unit	
	MICHAEL ALSIP	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2010*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1, 3-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman et al. (US 4,228,496) and further in view of Barroso et al. (US 6,668,308).

4. Consider **claims 1 and 14**, Katzman et al. discloses data processing system and integrated circuit comprising a plurality of processing modules being connected with an interconnect, wherein a first processing module communicates to a second processing module using transactions (Fig. 2, first ¶ of the abstract); **wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests** (Col. 16 lines 17-51, this claim language states that the first processing module is a master and that its function is to provide requests to the second processing module, now called a slave, and the function

of the slave is to provide a response to the requests. Katzman et al. discloses this feature in the cited areas above, by disclosing that a process running on one processor module (master) may need to request the service of another process running on another processing unit (slave) and therefore the first processor will send a request to the second processor module and when the process on the second processor module has completed the request, it will return a response back to the first processor); a first wrapper associated to **the slave** for buffering data from said **the slave** to be transferred over the interconnect until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered, **and wherein the first wrapper is connected between the slave and the interconnect** (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected each of the other processor modules through an interconnect); **and a second wrapper connected between the master and the interconnect for buffering data from the master to be transferred over the interconnect until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered** (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where each inter-processor control for each processor as an input and output buffer for sending and receiving data)**, and wherein the second wrapper is connected between the master and the interconnect** (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term

"wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected each of the other processor modules through an interconnect).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

5. Consider **claim 13**, Katzman et al. discloses a method for buffering data having a plurality of processing modules being connected with an interconnect **through wrappers**, wherein a first processing module communicates to a second processing module using transactions (Fig. 1, 2 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, first ¶ of the abstract), comprising the method comprising the acts of: **configuring the first processing module as a master the provides requests; configuring the**

second processing module as a slave the provides responses to the requests (Col. 16 lines 17-51, this claim language states that the first processing module is a master and that its function is to provide requests to the second processing module, now called a slave, and the function of the slave is to provide a response to the requests. Katzman et al. discloses this feature in the cited areas above, by disclosing that a process running on one processor module (master) may need to request the service of another process running on another processing unit (slave) and therefore the first processor will send a request to the second processor module and when the process on the second processor module has completed the request, it will return a response back to the first processor); **connecting the master to a master wrapper of the wrappers; connecting the master wrapper to the interconnect; connecting the slave to a slave wrapper of the wrappers; connecting the slave wrapper to the interconnect** (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected each of the other processor modules through an interconnect); buffering by the slave wrapper data from **the slave** to be transferred over the interconnect until a first amount of data is buffered **slave wrapper data**; transferring the buffered data when said first amount of data has been buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for

transferring data between processor modules. This inter-processor control is part of every processor module and is connected each of the other processor modules through an interconnect); **buffering by the master wrapper data from the master to be transferred over the interconnect until a second amount of data is buffered; transferring the buffered data when said second amount of data has been buffered by the master wrapper data** (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where each inter-processor control for each processor as an input and output buffer for sending and receiving data).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

6. Consider **claim 3** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first wrapper and said second wrapper are adapted to

transfer the buffered data in response to a first **unbuffer signal** and **a** second unbuffer signal, respectively, even if less than said first **amount** and **said** second amount of data is buffered in said first wrapper and said second wrapper (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task).

7. Consider **claim 4** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first wrapper and said second wrapper are adapted to transfer the buffered data according to a first **unbuffer flag** and **a** second unbuffer flag, respectively, even if less than said first **amount** and **said** second amount of data is buffered in said first wrapper and said second wrapper (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed flags.).

8. Consider **claim 5** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein at least one of said first wrapper and said second wrapper comprises a determination unit for determining **an** optimal first or second amount of data to be buffered according to communication properties of the communication between **the master and the slave** (Col. 7 lines 8-37).

9. Consider **claim 6** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein at least one of said first **wrapper** and **said** second wrapper

comprises a determination unit for determining **an** optimal moment for sending the data in said first **wrapper** or **said** second wrapper according to communication properties of the communication between **the master and the slave** (Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task of sending the data at the appropriate time.).

10. Consider **claim 7** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. disclose wherein said first unbuffer signal is initiated by **the slave** and said second unbuffer signal is initiated by **the master** (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor).

11. Consider **claim 8** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. disclose wherein setting of said first unbuffer flag is initiated by **the slave** and setting of said second unbuffer flag is initiated by **the master** (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor

has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

12. Consider **claim 9** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. disclose wherein **the master** is adapted to initiate said first **unbuffer signal** and said second unbuffer signal (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor.).

13. Consider **claim 10** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. disclose wherein **the master** is adapted to initiate setting of said first **and** second unbuffer flag (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has a inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data

packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

14. Consider **claim 11** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein **the master and the slave** communicate with each other using **messages of** a message-passing communication scheme, wherein the messages contain **a** message header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first **amount** and said second amount of data is buffered in said first and second wrapper (Col. 31 lines 3-52, where the control packet is considered the head of the message and this identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor).

15. Consider **claim 12** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein **the master and the slave** communicate with each other using **packets of** a packet based communication scheme, wherein the packets contain **a** packet header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first **amount** and **said** second amount of data is buffered in said first and second wrapper (Katzman et al.: Col. 31 lines 3-52, where the control packet identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor and Barroso et al.: Col. 14 lines 36-45, discloses that data-less transactions are 128-bits

long and that data packets have the same 128-bit header format, disclosing that both types have headers).

16. Consider **claim 15**, Katzman et al. discloses an integrated circuit comprising: a plurality of processing modules including a first processing module and a second processing module (Fig. 2, first ¶ of the abstract); a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module (Fig. 1, 19 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61); and a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module (fig. 1); wherein the first interconnect module includes a first memory for buffering first data from the first processing module until a first amount of data is buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61), and the second interconnect module includes a second memory for buffering second data from the second processing module until a second amount of data is buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61), the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches a first amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches a second amount (Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

17. Consider **claim 16** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. disclose wherein the plurality of interconnect modules manages the communication connection freeing the plurality of processing modules to perform data processing (col. 5 lines 13-22, Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32).

18. Consider **claim 17** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first interconnect module has a first

determination unit that determines the first burst length and the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where there are variable burst lengths and the length is determined by various attributes including the network of buses providing the communication path).

19. Consider **claim 18** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the first burst length differs from the second burst length (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53).

20. Consider **claim 19** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the network comprises a communication property device that determines the properties of the network for a requested communication and provides the properties to the first determination unit and the second determination unit for determining the first burst length and the second burst length (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where the burst time and length are dynamic and depend on many changing parameters which determine what these two parameters will be and circuitry is making these determinations).

21. Consider **claim 20** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the first interconnect module comprises a first

communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second determination unit (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where the burst time and length are dynamic and depend on many changing parameters which determine what these two parameters will be and circuitry is making these determinations).

22. Consider **claim 21** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting reaching the first amount and the second amount (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed command.).

23. Consider **claim 22** as applied to **claim 21** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously (col. 4 lines 51-59, col. 6 lines 28-33).

24. Consider **claim 23** as applied to **claim 21** above, Katzman et al. in view of Barroso et al. discloses wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory (Col. 16 lines 17-21 and 39-51, Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where requests for services or data can be request by one processor to another which cases that data to be loaded into the output queue and sent to the requesting processor).

25. Consider **claim 24** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory (Col. 16 lines 17-29 and 39-51, Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where the processor can send a message to send/ flush the data out of the out queue to another processor).

Response to Arguments

26. Applicant's arguments filed 3/08/2010 have been fully considered but they are not persuasive. The arguments pertaining to the newly added claim limitations have been addressed in the appropriate claim rejections above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hetul Patel/
Primary Examiner, Art Unit 2186

/Michael Alsip/
Examiner, Art Unit 2186

March 16, 2010

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	**Art Unit**
	MICHAEL ALSIP	2186

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/02/2009	12/09/2009	03/16/2010						
	1	✓	✓	✓						
	2	✓	✓	-						
	3	✓	✓	✓						
	4	✓	✓	✓						
	5	✓	✓	✓						
	6	✓	✓	✓						
	7	✓	✓	✓						
	8	✓	✓	✓						
	9	✓	✓	✓						
	10	✓	✓	✓						
	11	✓	✓	✓						
	12	✓	✓	✓						
	13	✓	✓	✓						
	14	✓	✓	✓						
	15		✓	✓						
	16		✓	✓						
	17		✓	✓						
	18		✓	✓						
	19		✓	✓						
	20		✓	✓						
	21		✓	✓						
	22		✓	✓						
	23		✓	✓						
	24		✓	✓						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	Art Unit
	MICHAEL ALSIP	2186

SEARCHED			
Class	Subclass	Date	Examiner
711	118 limited w/ text	3/16/2010	MA
711	141 limited w/ text	3/16/2010	MA
710	57 limited w/ text	3/16/2010	MA
710	100 limited w/ text	3/16/2010	MA

SEARCH NOTES		
Search Notes	Date	Examiner
inventor name and assignee search in eDAN and EAST	3/16/2010	MA
class/subclass and keyword search in EAST	3/16/2010	MA

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/MICHAEL ALSIP/ Examiner.Art Unit 2186	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L2	737	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L3	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L4	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L5	63	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L6	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L7	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

L8	1794	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L9	299	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L10	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L11	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L12	312	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L13	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L14	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L15	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
L16	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59

L17	105	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L18	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L19	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L20	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L21	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L22	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L23	344	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L24	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

L25	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L26	154	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L27	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L28	264	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L29	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L30	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L31	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L32	60	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

L33	17	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L34	15892	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L35	1	(koninklijke philips electronics).as. burst flush module buffer$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L36	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L37	737	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L38	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L39	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L40	63	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

L41	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L42	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L43	1794	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L44	299	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L45	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L46	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L47	312	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L48	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

L49	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L50	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
L51	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
L52	105	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L53	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L54	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L55	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L56	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L57	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

L58	344	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L59	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L60	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L61	154	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L62	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L63	264	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L64	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L65	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

L66	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L67	60	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
L68	17	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S1	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 12:45
S2	700	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:48
S3	356	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:50
S4	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:58
S5	52	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:59

S6	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:04
S7	42	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:20
S8	1640	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S9	286	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S10	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:26
S11	11	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28
S12	298	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28
S13	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:29

S14	39	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:35
S15	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:36
S16	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:39
S17	104	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S18	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S19	182	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S20	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S21	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S22	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:17

S23	325	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:19
S24	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:20
S25	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 11:31
S26	145	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S27	10	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S28	245	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S29	13	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S30	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05

S31	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S32	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S33	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S35	15075	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
S36	1	(koninklijke philips electronics).as. burst flush module buffer$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
S37	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S38	723	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S39	368	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S40	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S41	61	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S42	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S43	43	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S44	1746	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S45	298	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S46	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S47	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S48	310	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S49	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S50	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S51	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
S52	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
S53	104	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S54	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S55	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S56	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S57	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S58	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S59	340	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S60	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S61	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S62	151	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S63	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S64	256	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S65	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S66	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S67	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S68	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S69	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Atty. Docket: NL040529US1
ANDREI RADULESCU ET AL.	Confirmation No. 4172
Serial No. 11/569,083	Group Art Unit: 2186
Filed: NOVEMBER 14, 2006	Examiner: ALSIP, MICHAEL

Title: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

Mail Stop Amendment
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Final Office Action mailed on March 22, 2010, please amend the above-identified application and consider the remarks as follows:

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) An integrated circuit comprising:

a plurality of processing modules being connected with an interconnect each having a memory, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests;

a first wrapper associated to the slave for buffering data from the slave to be transferred over the interconnect to the master until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered, and wherein the first wrapper is connected between the slave and the interconnect; and

a second wrapper connected between the master and the interconnect for buffering data from the master to be transferred over the interconnect until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data

has been buffered~~, and wherein the second wrapper is connected between the master and the interconnect~~.

Claim 2 (Canceled)

3.(Previously Presented) The integrated circuit according to claim 1, wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to a first unbuffer signal and a second unbuffer signal, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

4.(Previously Presented) The integrated circuit according to claim 1, wherein said first wrapper and said second wrapper are adapted to transfer the buffered data according to a first unbuffer flag and a second unbuffer flag, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

5.(Previously Presented) The integrated circuit according to claim 1, wherein at least one of said first wrapper and said second wrapper comprises a determination unit for determining an optimal first or second amount of data to be buffered according to

communication properties of the communication between the master and the slave.

6.(Previously Presented) The integrated circuit according to claim 1, wherein at least one of said first wrapper and said second wrapper comprises a determination unit for determining an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave.

7.(Previously Presented) The integrated circuit according to claim 3, wherein said first unbuffer signal is initiated by the slave and said second unbuffer signal is initiated by the master.

8.(Previously Presented) The integrated circuit according to claim 4, wherein setting of said first unbuffer flag is initiated by the slave and setting of said second unbuffer flag is initiated by the master.

9.(Previously Presented) The integrated circuit according to claim 3, wherein said the master is adapted to initiate said first unbuffer signal and said second unbuffer signal.

10.(Previously Presented) The integrated circuit according to claim 4, wherein the

master is adapted to initiate setting of said first and second unbuffer flag.

11.(Previously Presented) The integrated circuit according to claim 1, wherein the master and the slave communicate with each other using messages of a message-passing communication scheme, wherein the messages contain a message header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

12.(Previously Presented) The integrated circuit according to claim 1, wherein the master and the slave communicate with each other using packets of a packet based communication scheme, wherein the packets contain a packet header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper.

13.(Currently Amended) A method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect through wrappers, wherein a first processing module communicates to a second processing module using

transactions, comprising the method comprising the acts of:

configuring the first processing module having a first memory as a master the provides requests;

configuring the second processing module having a second memory as a slave the provides responses to the requests;

connecting the master to a master wrapper of the wrappers;

connecting the master wrapper to the interconnect so that the master wrapper is between the master and the interconnect;

connecting the slave to a slave wrapper of the wrappers;

connecting the slave wrapper to the interconnect so that the slave wrapper is between the slave and the interconnect;

buffering by the slave wrapper data from the slave to be transferred over the interconnect until a first amount of data is buffered slave wrapper data;

transferring the buffered data when said first amount of data has been buffered;

buffering by the master wrapper data from the master to be transferred over the interconnect until a second amount of data is buffered;

transferring the buffered data when said second amount of data has been buffered by the master wrapper data.

14.(Currently Amended) A data processing system, comprising:

a plurality of processing modules each having a memory and being connected with an interconnect, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests; and

a first wrapper associated to the slave for buffering data from the slave to be transferred over the interconnect until a first amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered, and wherein the first wrapper is connected between the slave and the interconnect; and

a second wrapper connected between the master and the interconnect for buffering data from the master to be transferred over the interconnect until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered~~, and wherein the second wrapper is connected between the master and the interconnect~~.

15.(Currently Amended) An integrated circuit comprising:

a plurality of processing modules including a first processing module having a first processing memory and a second processing module having a second processing memory;

a plurality of interconnect modules including a first interconnect module and a

second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module; and

a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module;

wherein the first interconnect module includes a first memory connected between the first processing module and the interconnect for buffering first data from the first processing module until a first amount of data is buffered, and the second interconnect module includes a second memory connected between the second processing module and the interconnect for buffering second data from the second processing module until a second amount of data is buffered,

the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches a first amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches a second amount.

16.(Previously Presented) The integrated circuit of claim 15, wherein the plurality of interconnect modules manages the communication connection freeing the plurality of processing modules to perform data processing.

17.(Previously Presented) The integrated circuit of claim 15, wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first interconnect module has a first determination unit that determines the first burst length and the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection.

18.(Previously Presented) The integrated circuit of claim 17, wherein the first burst length differs from the second burst length.

19.(Previously Presented) The integrated circuit of claim 17, wherein the network comprises a communication property device that determines the properties of the network for a requested communication and provides the properties to the first determination unit and the second determination unit for determining the first burst length and the second burst length.

20.(Previously Presented) The integrated circuit of claim 17, wherein the first

interconnect module comprises a first communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second determination unit.

21.(Previously Presented) The integrated circuit of claim 15, wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting to reach the first amount and the second amount.

22.(Previously Presented) The integrated circuit of claim 21, wherein the first processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously.

23.(Previously Presented) The integrated circuit of claim 21, wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory.

24.(Previously Presented) The integrated circuit of claim 15, wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory.

REMARKS

This Amendment is being filed in response to the Office Action mailed March 22, 2010, which has been reviewed and carefully considered. Reconsideration and allowance of the present application in view of the amendments made above and the remarks to follow are respectfully requested.

Claims 1 and 3-24 are pending in this application, where claim 2 has been currently canceled without prejudice. Claims 1, 13, 14 and 15 are independent.

In the Office Action, claims 1 and 3-24 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 4,228,496 (Katzman) in view of U.S. Patent No. 6,668,308 (Barroso). Applicants respectfully traverse and submit that claims 1 and 3-24 are patentable over Katzman and Barroso for at least the following reasons.

Katzman is directed to a multiprocessor system that includes separate processor modules 33 which are interconnected for parallel processing using two redundant interprocessor buses 35 dedicated exclusively to interprocessor communication. The buses 35 each includes a bus controller 37. As clearly shown in FIG 1, the processor modules 33 each have a memory 107 and are connected to two redundant interprocessor buses 35. No further memory, buffers or wrapper is shown in shown in FIG 1.

It is respectfully submitted that Katzman does not disclose or suggest the present invention as recited in independent claim 1, and similarly recited in independent claims 13, 14 and 15 which, amongst other patentable elements, recites (illustrative emphasis

provided):

> a plurality of processing modules being connected with an interconnect each having a memory, ... wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests;
>
> a first wrapper associated to the slave for buffering data from the slave to be transferred over the interconnect to the master until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered, and wherein the **first wrapper is connected between the slave and the interconnect**; and
>
> a **second wrapper connected between the master and the interconnect** for buffering data from the master to be transferred over the interconnect until a second amount of data is buffered, ...

Katzman does not even disclose or suggest any master-slave relationship between the processor modules 33. Even, assuming arguendo, that somehow this feature is shown in Katzman, there is still no disclosure or suggestion in Katzman of a **wrapper** (for buffering data) which is connected **between the slave and the interconnect, or between the master and the interconnect**, as recited in independent claims 1, 13, 14 and 15. Rather, FIG 1 of Katzman clearly shows that the processor modules 33 have a memory 107, and the processor modules 33 are directly connected to the buses 35 without any additional buffers. This dichotomy of a processor memory and master/slave wrapper for buffering data is recited in independent claims 1, 13, 14 and 15, and nowhere disclosed or suggested in Katzman. Barroso is cited to allegedly show other features and does not remedy the deficiencies in Katzman and Barroso.

Accordingly, it is respectfully submitted that independent claims 1, 13, 14 and 15 are allowable, and allowance thereof is respectfully requested. In addition, it is respectfully

submitted that claims 3-12 and 16-24 should also be allowed at least based on their dependence from independent claims 1 and 15.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

By _____
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Attorney for Applicant(s)
June 8, 2010

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Electronic Acknowledgement Receipt

EFS ID:	7864573
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
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Receipt Date:	22-JUN-2010
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Application Type:	U.S. National Stage under 35 USC 371

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Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NL040529US1_Amd_2010_June_22.pdf	479613 711f0fe936517a5050a8c9608cf5a8660d0a9910	yes	14

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	11
	Applicant Arguments/Remarks Made in an Amendment	12	14
Warnings:			
Information:			
	Total Files Size (in bytes):	479613	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/569,083	11/14/2006	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
AMENDMENT	06/22/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 23	Minus	** 20	= 3	X $ =		OR	X $52=	156
	Independent (37 CFR 1.16(h))	* 4	Minus	***3	= 1	X $ =		OR	X $220=	220
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	376

		(Column 1)		(Column 2)	(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DIANE JOHNSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	NL040529US1	4172

24737 7590 07/21/2010

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BRIARCLIFF MANOR, NY 10510

EXAMINER	
ALSIP, MICHAEL	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
07/21/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/569,083	RADULESCU ET AL.	
	Examiner	Art Unit	
	MICHAEL ALSIP	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/22/2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/18/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

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DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1, 3-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman et al. (US 4,228,496) and further in view of Barroso et al. (US 6,668,308).

4. Consider **claims 1 and 14**, Katzman et al. discloses data processing system and integrated circuit comprising a plurality of processing modules being connected with an interconnect **each having a memory**, wherein a first processing module communicates to a second processing module using transactions (Fig. 1 component 107, Fig. 2, first ¶ of the abstract, each processing module has a memory 107.); wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests (Col. 16 lines 17-51, this claim

language states that the first processing module is a master and that its function is to provide requests to the second processing module, now called a slave, and the function of the slave is to provide a response to the requests. Katzman et al. discloses this feature in the cited areas above, by disclosing that a process running on one processor module (master) may need to request the service of another process running on another processing unit (slave) and therefore the first processor will send a request to the second processor module and when the process on the second processor module has completed the request, it will return a response back to the first processor); a first wrapper associated to the slave for buffering data from said the slave to be transferred over the interconnect until a first amount of data is buffered, wherein the buffered data are transferred when said first amount of data has been buffered, and wherein the first wrapper is connected between the slave and the interconnect (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected each of the other processor modules through an interconnect); and a second wrapper connected between the master and the interconnect for buffering data from the master to be transferred over the interconnect until a second amount of data is buffered, wherein the buffered data are transferred when said second amount of data has been buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where each inter-processor control for each processor as an input and output buffer for sending and receiving data),

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

5. Consider **claim 13**, Katzman et al. discloses a method for buffering data having a plurality of processing modules being connected with an interconnect through wrappers, wherein a first processing module communicates to a second processing module using transactions (Fig. 1, 2 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, first ¶ of the abstract), comprising the method comprising the acts of: configuring the first processing module **having a first memory** as a master the provides requests; configuring the second processing module **having a second memory** as a slave the provides responses to the requests (fig. 1 component 107, Col. 16 lines 17-51, this claim language states that the first processing module is a master and that its function is to provide requests to the second processing module, now called a slave, and the function

of the slave is to provide a response to the requests. Katzman et al. discloses this feature in the cited areas above, by disclosing that a process running on one processor module (master) may need to request the service of another process running on another processing unit (slave) and therefore the first processor will send a request to the second processor module and when the process on the second processor module has completed the request, it will return a response back to the first processor. Also each processor module has a memory 107 associated with it.); connecting the master to a master wrapper of the wrappers; connecting the master wrapper to the interconnect **so that the master wrapper is between the master and the interconnect**; connecting the slave to a slave wrapper of the wrappers; connecting the slave wrapper to the interconnect **so that the slave wrapper is between the slave and the interconnect** (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules.); buffering by the slave wrapper data from the slave to be transferred over the interconnect until a first amount of data is buffered slave wrapper data; transferring the buffered data when said first amount of data has been buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected each of the other processor modules through an interconnect); buffering by

the master wrapper data from the master to be transferred over the interconnect until a second amount of data is buffered; transferring the buffered data when said second amount of data has been buffered by the master wrapper data (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where each inter-processor control for each processor as an input and output buffer for sending and receiving data).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

6. Consider **claim 3** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to a first unbuffer signal and a second unbuffer signal, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper (Col. 17 lines 32-64, Col. 22-

23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task).

7. Consider **claim 4** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein said first wrapper and said second wrapper are adapted to transfer the buffered data according to a first unbuffer flag and a second unbuffer flag, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed flags.).

8. Consider **claim 5** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein at least one of said first wrapper and said second wrapper comprises a determination unit for determining an optimal first or second amount of data to be buffered according to communication properties of the communication between the master and the slave (Col. 7 lines 8-37).

9. Consider **claim 6** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein at least one of said first wrapper and said second wrapper comprises a determination unit for determining an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave (Col. 17 lines 32-64, Col. 21 lines

57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task of sending the data at the appropriate time.).

10. Consider **claim 7** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. disclose wherein said first unbuffer signal is initiated by the slave and said second unbuffer signal is initiated by the master (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor).

11. Consider **claim 8** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. disclose wherein setting of said first unbuffer flag is initiated by the slave and setting of said second unbuffer flag is initiated by the master (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each

processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

12. Consider **claim 9** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. disclose wherein the master is adapted to initiate said first unbuffer signal and said second unbuffer signal (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor.).

13. Consider **claim 10** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. disclose wherein the master is adapted to initiate setting of said first and second unbuffer flag (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

14. Consider **claim 11** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein the master and the slave communicate with each other using messages of a message-passing communication scheme, wherein the messages contain a message header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper (Col. 31 lines 3-52, where the control packet is considered the head of the message and this identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor).

15. Consider **claim 12** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein the master and the slave communicate with each other using packets of a packet based communication scheme, wherein the packets contain a packet header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper (Katzman et al.: Col. 31 lines 3-52, where the control packet identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor and Barroso et al.: Col. 14 lines 36-45, discloses that data-less transactions are 128-bits long and that data packets have the same 128-bit header format, disclosing that both types have headers).

16. Consider **claim 15**, Katzman et al. discloses an integrated circuit comprising: a plurality of processing modules including a first processing module **having a first processing memory** and a second processing module **having a second processing memory** (Fig. 1 component 107, Fig. 2, first ¶ of the abstract); a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module (Fig. 1, 19 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61); and a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module (fig. 1); wherein the first interconnect module includes a first memory **connected between the first processing module and the interconnect** for buffering first data from the first processing module until a first amount of data is buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules.), and the second interconnect module includes a second memory **connected between the second processing module and the interconnect** for buffering second data from the second processing module until a second amount of data is buffered (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between

processor modules.), the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches a first amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches a second amount (Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

17. Consider **claim 16** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. disclose wherein the plurality of interconnect modules manages the communication connection freeing the plurality of processing modules to perform data

processing (col. 5 lines 13-22, Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32).

18. Consider **claim 17** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first interconnect module has a first determination unit that determines the first burst length and the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where there are variable burst lengths and the length is determined by various attributes including the network of buses providing the communication path).

19. Consider **claim 18** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the first burst length differs from the second burst length (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53).

20. Consider **claim 19** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the network comprises a communication property device that determines the properties of the network for a requested communication and provides the properties to the first determination unit and the second determination unit

for determining the first burst length and the second burst length (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where the burst time and length are dynamic and depend on many changing parameters which determine what these two parameters will be and circuitry is making these determinations).

21. Consider **claim 20** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the first interconnect module comprises a first communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second determination unit (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where the burst time and length are dynamic and depend on many changing parameters which determine what these two parameters will be and circuitry is making these determinations).

22. Consider **claim 21** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting reaching the first amount and the second amount (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where during the process of filling and sending a packet from the

out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed command.).

23. Consider **claim 22** as applied to **claim 21** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously (col. 4 lines 51-59, col. 6 lines 28-33).

24. Consider **claim 23** as applied to **claim 21** above, Katzman et al. in view of Barroso et al. discloses wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory (Col. 16 lines 17-21 and 39-51, Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where requests for services or data can be request by one processor to another which cases that data to be loaded into the output queue and sent to the requesting processor).

25. Consider **claim 24** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory (Col. 16 lines 17-29 and 39-51, Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where the processor can send a message to send/ flush the data out of the out queue to another processor).

Response to Arguments

26. Applicant's arguments filed 6/22/2010 have been fully considered but they are not persuasive.

27. The Applicant first argues that Katzman does not disclose a master-slave relationship, however as stated in the previous office action and reiterated in this action above, the claim language states that the first processing module is considered a master for the purposes of providing requests and that the second processing module is considered a slave for the purposes of providing responses to those requests. Katzman (Col. 16 lines 17-51) does not explicitly use the terms master and slave, but does disclose the claimed requirements as to what/how the first and second processing modules must interact with each other and therefore meets the claim language. The claim terms master and slave do not have any more specific requirements than those claimed of the first module providing requests and the second module providing responses to those requests, which Katzman discloses.

28. Secondly the Applicant argues that Katzman does not disclose the dichotomy of a processor memory and wrapper for buffering data as discloses in the independent claims, however as rejected above, Katzman discloses a, in fig. 1, a processor memory 107 that each processor module possess and, Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Katzman discloses that the inter-processor control has both inqueue and outqueue buffers for buffering data from/to the interconnect bus, therefore Katzman does teach having a processor memory and wrappers for buffering data as claimed.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael Alsip
Examiner
Art Unit 2186

/Mardochee Chery/
Primary Examiner, Art Unit 2188
July 19, 2010

/Michael Alsip/
Examiner, Art Unit 2186

July 12, 2010

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	**Art Unit**
	MICHAEL ALSIP	2186

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/02/2009	12/09/2009	03/16/2010	07/12/2010					
	1	✓	✓	✓	✓					
	2	✓	✓	-	-					
	3	✓	✓	✓	✓					
	4	✓	✓	✓	✓					
	5	✓	✓	✓	✓					
	6	✓	✓	✓	✓					
	7	✓	✓	✓	✓					
	8	✓	✓	✓	✓					
	9	✓	✓	✓	✓					
	10	✓	✓	✓	✓					
	11	✓	✓	✓	✓					
	12	✓	✓	✓	✓					
	13	✓	✓	✓	✓					
	14	✓	✓	✓	✓					
	15		✓	✓	✓					
	16		✓	✓	✓					
	17		✓	✓	✓					
	18		✓	✓	✓					
	19		✓	✓	✓					
	20		✓	✓	✓					
	21		✓	✓	✓					
	22		✓	✓	✓					
	23		✓	✓	✓					
	24		✓	✓	✓					

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	**Art Unit**
	MICHAEL ALSIP	2186

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
711	118 limited w/ text	7/12/2010	MA
711	141 limited w/ text	7/12/2010	MA
710	57 limited w/ text	7/12/2010	MA
710	100 limited w/ text	7/12/2010	MA

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
inventor name and assignee search in eDAN and EAST	7/12/2010	MA
class/subclass and keyword search in EAST	7/12/2010	MA

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

/MICHAEL ALSIP/ Examiner.Art Unit 2186	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
L2	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
L3	160	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
L4	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
L5	14	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
L6	14	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
L7	61	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10

L8	61	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
L9	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
L10	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:11
L11	46	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:11
L12	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:12
L13	5	US-6493776-$.DID. OR US-6397287-$.DID. OR US-6393500-$.DID. OR US-5987552-$.DID. OR US-6629253-$.DID.	US-PGPUB; USPAT; USOCR	AND	ON	2010/07/12 14:13
L14	2	"20030101307".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:14
L15	5	"2005026964".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:14

S1	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 12:45
S2	700	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:48
S3	356	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:50
S4	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:58
S5	52	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:59
S6	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:04
S7	42	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:20
S8	1640	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25

S9	286	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S10	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:26
S11	11	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28
S12	298	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28
S13	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:29
S14	39	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:35
S15	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:36
S16	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:39
S17	104	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44

S18	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S19	182	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S20	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S21	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S22	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:17
S23	325	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:19
S24	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:20
S25	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 11:31

S26	145	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S27	10	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S28	245	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S29	13	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S30	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S31	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S32	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S33	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05

S35	15075	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
S36	1	(koninklijke philips electronics).as. burst flush module buffer$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
S37	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S38	723	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S39	368	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S40	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S41	61	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S42	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S43	43	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S44	1746	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S45	298	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S46	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S47	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S48	310	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S49	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S50	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S51	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24

S52	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
S53	104	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S54	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S55	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S56	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S57	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S58	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S59	340	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S60	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S61	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S62	151	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S63	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S64	256	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S65	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S66	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S67	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S68	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S69	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S70	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S71	737	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S72	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S73	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S74	63	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S75	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S76	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S77	1794	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S78	299	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S79	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S80	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S81	312	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S82	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S83	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S84	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59

S85	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S86	105	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S87	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S88	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S89	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S90	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S91	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S92	344	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S93	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S94	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S95	154	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S96	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S97	264	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S98	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S99	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S100	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S101	60	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S102	17	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S103	15892	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S104	1	(koninklijke philips electronics).as. burst flush module buffer$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S105	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S106	737	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S107	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S108	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S109	63	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S110	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S111	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S112	1794	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S113	299	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S114	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S115	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S116	312	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S117	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S118	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S119	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S120	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S121	105	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S122	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S123	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S124	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S125	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S126	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S127	344	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S128	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S129	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S130	154	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S131	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S132	264	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S133	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S134	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S135	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S136	60	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S137	17	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

EAST Search History (Interference)

<This search history is empty>

7/12/2010 2:15:06 PM
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PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	11569083
Filing Date	2006-11-14
First Named Inventor	Andrei Radulescu
Art Unit	2186
Examiner Name	Michael Alsip
Attorney Docket Number	NL040529US1

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6493776	B1	2002-12-10	COURTRIGHT ET AL	
	2	6397287	B1	2002-05-28	BROWN ET AL	
	3	6393500	B1	2002-05-21	THEKKATH	
	4	5987552		1999-11-16	CHITTOR ET AL	
	5	6629253	B1	2003-09-30	WITTER ET AL	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20030101307	A1	2003-05-29	GEMELLI ET AL	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	11569083
	Filing Date	2006-11-14
	First Named Inventor	Andrei Radulescu
	Art Unit	2186
	Examiner Name	Michael Alsip
	Attorney Docket Number	NL040529US1

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2005026964	WO	A2	2005-03-24	VAN DER WOLF ET AL		☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	ARM, "AMBA AXI PROTOCOL V1.0 SPECIFICATION" XP002342105, pages 1011, August 24, 2005	☐

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EXAMINER SIGNATURE

Examiner Signature	/Michael Alsip/	Date Considered	07/12/2010

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2186

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Atty. Docket: NL040529US1
Andrei RADULESCU, et al.	Confirmation No. 4172
Serial No. 11/569,083	Group Art Unit: 2186
Filed: November 14, 2006	Examiner: ALSIP, Michael

Title: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

Mail Stop AF
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER §1.116

Sir:

In response to the Final Office Action mailed on July 21, 2010, please amend the above-identified application and consider the remarks as follows:

REMARKS

This Amendment is being filed in response to the Final Office Action mailed July 21, 2010, which has been reviewed and carefully considered.

By means of the present amendment, independent claims 1, 13, 14 and 15 have been amended for better clarity as well as including the features of claim 5 which has been canceled without prejudice. Accordingly no new issues have been introduced that require a new search, and thus entry of the present amendment is respectfully requested.

Claims 1, 3-4 and 6-24 are pending in this application, where claim 2 had been previously canceled without prejudice and claim 5 has been currently canceled without prejudice. Claims 1, 13, 14 and 15 are independent.

In the Final Office Action, claims 1 and 3-24 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 4,228,496 (Katzman) in view of U.S. Patent No. 6,668,308 (Barroso). Applicants respectfully traverse and submit that claims 1, 3-4 and 6-24 are patentable over Katzman and Barroso for at least the following reasons.

Katzman is directed to a multiprocessor system that includes separate processor modules 33, shown in FIG 1, which are interconnected for parallel processing using two redundant interprocessor buses 35 dedicated exclusively to interprocessor communication. The buses 35 each include a bus controller 37. As clearly shown in FIG 1, device controllers 41 are connected **between** input/output (I/O) buses 39 of the processor modules 33.

On page 7 of the Final Office Acton, in item 8 rejecting claim 5, it is alleged that column 7, lines 8-37 of Katzman discloses a determination unit for determining an optimal first or second amount of data to be buffered. This allegation is respectfully traversed. It is respectfully submitted that there is no disclosure or suggestion in column 7, lines 8-37 of Katzman of any a determination unit for determining an optimal first or second amount of data to be buffered. Rather, Katzman merely discloses in column 7, lines 8-19 (emphasis added):

> As noted above, each **buffer** is a stress responsive buffer and this provides two advantages.
>
> First of all, each buffer can be constructed to have an overall depth which is related to the type and number of devices to be serviced. Each device controller can therefore have a buffer size which is related to the kind of devices to be controlled.
>
> Secondly, the stress responsive buffer construction and mode of operation of the present invention allows the buffers to cooperate without communicating with each other. This in turn permits optimum efficient use of the bandwidth of the input/output channel.
>
> The stress placed on a particular buffer is determined by the degree of the full or empty condition of the buffer in combination with the direction of the transfer with respect to the processor module. Stress increases as the peripheral device accesses the buffer, and stress decreases as the input/output channel means access the buffer.

Further, Katzman merely discloses in column 7, lines 33-37 (emphasis added):

> The stress responsive **buffer** includes control logic for keeping track of the stress placed on the buffer. The control logic is effective to make reconnect requests to the input/output channel as the stress passes through a threshold depth of the buffer.

Assuming, arguendo, that the allegation that Katzman discloses a determination unit is correct, column 7, lines 8-37 of Katzman refers to buffers 189 (FIG 19) of I/O device

controller 41. As clearly shown in FIG 1 of Katzman, I/O device controllers 41 (that include the buffers 189 shown in FIG 19) are connected **between** input/output (I/O) buses 39 of the processor modules 33.

In stark contrast, the present invention as recited in independent claim 1, and similarly recited in independent claims 13, 14 and 15, amongst other patentable elements recites (illustrative emphasis provided):

> a first interface unit coupled to the slave and including a first wrapper for buffering data from the slave to be transferred over the interconnect to the master, the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and wherein the buffered data are transferred when said first optimal amount of data has been buffered by the first wrapper, and wherein the first interface unit including the first wrapper and the first determination unit is connected **between** the slave and the interconnect; and
>
> a second interface unit coupled to the master and including a second wrapper for buffering data from the master to be transferred over the interconnect, the second interface unit further including a second determination unit, wherein second first determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and wherein the buffered data are transferred when said second optimal amount of data has been buffered by the second wrapper, and wherein the second interface unit including the second wrapper and the second determination unit is connected **between** the master and the interconnect.

Interface units (or interconnect modules) that include determination units and are connected between the slave and an interconnect (or a network), and connected between the master and the interconnect/network, are nowhere disclosed or suggested in Katzman. Rather, as clearly shown in FIG 1, the Katzman I/O device controllers 41 that include the

buffers 189 (FIG 19) are connected **between** input/output (I/O) buses 39 of the processor modules 33. Barroso is cited to allegedly show other features and does not remedy the deficiencies in Katzman and Barroso.

Accordingly, it is respectfully submitted that independent claims 1, 13, 14 and 15 are allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 3-4, 6-12 and 16-24 should also be allowed at least based on their dependence from independent claims 1 and 15.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

By _____
Dicran Halajian, Reg. 39,703
Attorney for Applicant(s)
September 8, 2010

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P.O. Box 3001
Briarcliff Manor, NY 10510-8001
(914) 333-9643

Electronic Acknowledgement Receipt

EFS ID:	8382515
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	NL040529US1
Receipt Date:	09-SEP-2010
Filing Date:	14-NOV-2006
Time Stamp:	13:21:21
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NL040529US1_116Amd_2010_Sept_9.pdf	2157143 4fb7b6307d7283647e9e70ec063a140fc19918a4	yes	17

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment After Final	1	1
	Claims	2	12
	Applicant Arguments/Remarks Made in an Amendment	13	17
Warnings:			
Information:			
	Total Files Size (in bytes):	2157143	

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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD

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Application or Docket Number	Filing Date	☐ To be Mailed
11/569,083	11/14/2006	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	09/09/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 23	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/ANGELA WHITE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) An integrated circuit comprising:

a plurality of processing modules being connected with an interconnect and each of the plurality of processing modules having a memory, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests;

a first interface unit coupled to the slave and including a first wrapper ~~associated to the slave~~ for buffering data from the slave to be transferred over the interconnect to the master ~~until a first amount of data is buffered~~, the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and wherein the buffered data are transferred when said first optimal amount of data has been buffered by the first wrapper, and wherein the first interface unit including the first wrapper and the first

determination unit is connected between the slave and the interconnect; and

a second interface unit coupled to the master and including a second wrapper ~~connected between the master and the interconnect~~ for buffering data from the master to be transferred over the interconnect ~~until a second amount of data is buffered~~, the second interface unit further including a second determination unit, wherein second first determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and wherein the buffered data are transferred when said second optimal amount of data has been buffered by the second wrapper, and wherein the second interface unit including the second wrapper and the second determination unit is connected between the master and the interconnect.

Claim 2 (Canceled)

3.(Currently Amended) The integrated circuit according to claim 1, wherein the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer signal and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer signal, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to ~~a~~ the first unbuffer signal and ~~a~~ the second unbuffer signal, respectively, even if less than said first optimal amount and said second optimal amount of data is buffered in said first wrapper and said second wrapper.

4.(Currently Amended) The integrated circuit according to claim 1, wherein the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer flag and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer flag, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data according to ~~a~~ the first unbuffer flag and ~~a~~ the second unbuffer flag, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

Claim 5 (Canceled)

6.(Currently Amended) The integrated circuit according to claim 1, wherein at least one of ~~said first wrapper and said second wrapper comprises a~~ the first determination unit ~~for determining~~ and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave.

7.(Previously Presented) The integrated circuit according to claim 3, wherein said first unbuffer signal is initiated by the slave and said second unbuffer signal is initiated by the master.

8.(Previously Presented) The integrated circuit according to claim 4, wherein setting of said first unbuffer flag is initiated by the slave and setting of said second unbuffer flag is initiated by the master.

9.(Currently Amended) The integrated circuit according to claim 3, wherein ~~said~~ the master is adapted to initiate said first unbuffer signal and said second unbuffer signal.

10.(Previously Presented) The integrated circuit according to claim 4, wherein the master is adapted to initiate setting of said first and second unbuffer flag.

11.(Previously Presented) The integrated circuit according to claim 1, wherein the master and the slave communicate with each other using messages of a message-passing communication scheme, wherein the messages contain a message header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

12.(Previously Presented) The integrated circuit according to claim 1, wherein the

master and the slave communicate with each other using packets of a packet based communication scheme, wherein the packets contain a packet header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper.

13.(Currently Amended) A method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect through ~~wrappers~~ interface units, wherein a first processing module communicates to a second processing module using transactions, ~~comprising~~ the method comprising the acts of:

configuring the first processing module having a first memory as a master the provides requests;

configuring the second processing module having a second memory as a slave the provides responses to the requests;

connecting the master to a master ~~wrapper~~ interface unit of the ~~wrappers~~ interface units;

connecting the master ~~wrapper~~ interface unit to the interconnect so that the master ~~wrapper~~ interface unit is between the master and the interconnect;

connecting the slave to a slave ~~wrapper~~ interface unit of the ~~wrappers~~ interface units;

connecting the slave ~~wrapper~~ interface unit to the interconnect so that the slave ~~wrapper~~ interface unit is between the slave and the interconnect;

determining by a master determination unit of the master interface unit a first optimal amount of data to be buffered by a master wrapper of the master interface unit;

determining by a slave determination unit of the slave interface unit a second optimal amount of data to be buffered by a slave wrapper of the slave interface unit;

buffering by the slave wrapper of the slave ~~wrapper~~ interface unit data from the slave to be transferred over the interconnect until a first optimal amount of data is buffered ~~slave wrapper data~~;

transferring the buffered data from the slave wrapper to the master wrapper when said first optimal amount of data has been buffered by the slave wrapper;

buffering by the master wrapper of the master ~~wrapper~~ interface unit data from the master to be transferred over the interconnect until a second optimal amount of data is buffered by the master wrapper;

transferring the buffered data from the master wrapper to the slave wrapper when said second optimal amount of data has been buffered by the master wrapper ~~data~~.

14.(Currently Amended) A data processing system, comprising:

a plurality of processing modules each having a memory and being connected with an interconnect, wherein a first processing module communicates to a second processing

module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests; and

a first interface unit coupled to the slave and including a first wrapper ~~associated to the slave~~ for buffering data from the slave to be transferred over the interconnect ~~until a first amount of data is buffered~~, the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and wherein the buffered data are transferred when said ~~second~~ first optimal amount of data has been buffered by the first wrapper, and wherein the first interface unit including the first wrapper and the first determination unit is connected between the slave and the interconnect; and

a second interface unit coupled to the master and including a second wrapper ~~connected between the master and the interconnect~~ for buffering data from the master to be transferred over the interconnect ~~until a second amount of data is buffered~~, the second interface unit further including a second determination unit, wherein second first determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and wherein the buffered data are transferred when said second optimal amount of data has been buffered by the second wrapper, and wherein the second interface unit including the second wrapper and the second determination unit is connected between the master and the interconnect.

15.(Currently Amended) An integrated circuit comprising:

a plurality of processing modules including a first processing module having a first processing memory and a second processing module having a second processing memory;

a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module; and

a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module, wherein the first interconnect module is connected between the first processing module and the network, and wherein the second interconnect module is connected between the second processing module and the network;

wherein the first interconnect module includes a first memory ~~connected between the first processing module and the interconnect~~ for buffering first data from the first processing module ~~until a first amount of data is buffered~~, the first interconnect module further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory, and the second interconnect module includes a second memory ~~connected between the second~~

~~processing module and the interconnect~~ for buffering second data from the second processing module ~~until a second amount of data is buffered~~, the second interconnect module further including a second determination unit, wherein the second determination unit is configured to determine a second optimal amount of data to be buffered by the second memory,

the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches ~~a~~ the first optimal amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches ~~a~~ the second optimal amount.

16.(Previously Presented) The integrated circuit of claim 15, wherein the plurality of interconnect modules manages the communication connection freeing the plurality of processing modules to perform data processing.

17.(Previously Presented) The integrated circuit of claim 15, wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first interconnect module has a first determination unit that determines the first burst length and

the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection.

18.(Previously Presented) The integrated circuit of claim 17, wherein the first burst length differs from the second burst length.

19.(Previously Presented) The integrated circuit of claim 17, wherein the network comprises a communication property device that determines the properties of the network for a requested communication and provides the properties to the first determination unit and the second determination unit for determining the first burst length and the second burst length.

20.(Previously Presented) The integrated circuit of claim 17, wherein the first interconnect module comprises a first communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second determination unit.

21.(Previously Presented) The integrated circuit of claim 15, wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting to reach the first amount and the second amount.

22.(Previously Presented) The integrated circuit of claim 21, wherein the first processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously.

23.(Previously Presented) The integrated circuit of claim 21, wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory.

24.(Previously Presented) The integrated circuit of claim 15, wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	NL040529US1	4172

24737 7590 09/21/2010

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
ALSIP, MICHAEL	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
09/21/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No. 11/569,083	Applicant(s) RADULESCU ET AL.	
	Examiner MICHAEL ALSIP	Art Unit 2186	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 3 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,3,4 and 6-24*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: Since the amendments to the claim language have not been entered, the arguments pertaining to those newly amended limitations will not be addressed at this time.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Michael Alsip/
Examiner, Art Unit 2186

Continuation of 3. NOTE: The amendments to the independent claims change the scope of these claims and that of their dependent claims. Many dependent claims did not previously require the claim language of claim 5 and the amendments of the independent claims are more specific than previous claim 5 and thus require at least further consideration and possible search.

/Matt Kim/
SPE, AU2186

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	11569083	Filing Date	2006-11-14	Docket Number (if applicable)	NL040529US1	Art Unit	2186
First Named Inventor	Andrei Radulescu			Examiner Name	Michael Alsip		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☐ Enclosed

☐ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 141270

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Michael E. Belk/	Date (YYYY-MM-DD)	2010-10-19
Name	Michael E. Belk	Registration Number	33357

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	11569083
Filing Date:	14-Nov-2006
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Filer:	Michael E. Belk/Elissa DeLuccy
Attorney Docket Number:	NL040529US1

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**810**

Electronic Acknowledgement Receipt	
EFS ID:	8650988
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	NL040529US1
Receipt Date:	19-OCT-2010
Filing Date:	14-NOV-2006
Time Stamp:	10:35:32
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$810
RAM confirmation Number	7863
Deposit Account	141270
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	NL040529US1_RCE_2010_Oct_19.pdf	697410 367444e4a605aad071dafadbc6cb21f50f98e527	no	3
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30687 d5cdbf001c9850fd94c2d6dae212f4aa9edcd3ee	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	728097		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/569,083	11/14/2006	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	10/19/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 22	Minus	** 23	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Debra R. Wyatt/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	NL040529US1	4172

24737 7590 10/22/2010

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
ALSIP, MICHAEL	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
10/22/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/569,083	RADULESCU ET AL.	
	Examiner	Art Unit	
	MICHAEL ALSIP	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4 and 6-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 6-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

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DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1, 3-4 and 6-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman et al. (US 4,228,496) and further in view of Barroso et al. (US 6,668,308).

4. Consider **claims 1 and 14**, Katzman et al. discloses data processing system and integrated circuit comprising a plurality of processing modules being connected with an interconnect **and** each **of the plurality of processing modules** having a memory, wherein a first processing module communicates to a second processing module using transactions (Fig. 1 component 107, Fig. 2, first ¶ of the abstract, each processing module has a memory 107.); wherein the first processing module is a master for

providing requests and the second processing module is a slave for providing responses to the requests (Col. 16 lines 17-51, this claim language states that the first processing module is a master and that its function is to provide requests to the second processing module, now called a slave, and the function of the slave is to provide a response to the requests. Katzman et al. discloses this feature in the cited areas above, by disclosing that a process running on one processor module (master) may need to request the service of another process running on another processing unit (slave) and therefore the first processor will send a request to the second processor module and when the process on the second processor module has completed the request, it will return a response back to the first processor); **a first interface unit coupled to the slave and including** a first wrapper for buffering data from said the slave to be transferred over the interconnect to the master **the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and** wherein the buffered data are transferred when said first **optimal** amount of data has been buffered, **by the first wrapper** and wherein the **first interface unit including the** first wrapper **and the first determination unit** is connected between the slave and the interconnect (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, where the term "wrapper" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected to each of the

other processor modules through the interconnect. Each interprocessor control includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.); and **a second interface unit coupled to the master and including** a second wrapper for buffering data from the master to be transferred over the interconnect, **the second interface unit further including a second determination unit, wherein the second determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and** wherein the buffered data are transferred when said second **optimal** amount of data has been buffered **by the second wrapper and wherein the second interface unit including the second wrapper and the second determination unit is connected between the master and the interconnect** (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, where the term "wrapper" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Each interprocessor control includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit,

however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

5. Consider **claim 13**, Katzman et al. discloses a method for buffering data having a plurality of processing modules being connected with an interconnect through **interface units**, wherein a first processing module communicates to a second processing module using transactions (Fig. 1, 2 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, first ¶ of the abstract), the method comprising the acts of: configuring the first processing module having a first memory as a master the provides requests; configuring the second processing module having a second memory as a slave the provides responses to the requests (fig. 1 component 107, Col. 16 lines 17-51, this claim language states that the first processing module is a master and that its function is to provide requests to the second processing module, now called a slave, and the function of the slave is to provide a response to the requests. Katzman et al. discloses this feature in the cited areas above, by disclosing that a process running on one processor module (master)

may need to request the service of another process running on another processing unit (slave) and therefore the first processor will send a request to the second processor module and when the process on the second processor module has completed the request, it will return a response back to the first processor. Also each processor module has a memory 107 associated with it.); connecting the master to a master **interface unit** of the **interface units**; connecting the master **interface unit** to the interconnect so that the master **interface unit** is between the master and the interconnect; connecting the slave to a slave **interface unit** of the **interface units**; connecting the slave **wrapper** to the interconnect so that the slave **interface unit** is between the slave and the interconnect (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "interface unit" is considered the inter-processor control which contains inqueue and outqueue buffers for transferring data between processor modules.); **determining by a master determination unit of the master interface unit a first optimal amount of data to be buffered by a master wrapper of the master interface unit; determining by a slave determination unit of the slave interface unit a second optimal amount of data to be buffered by a slave wrapper of the slave interface unit** (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, where the term "wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Each interprocessor control

includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.)**;** buffering by **the slave wrapper of** the slave **the slave interface unit** data from the slave to be transferred over the interconnect until a first **optimal** amount of data is buffered; transferring the buffered data **from the slave wrapper to the master wrapper** when said first **optimal** amount of data has been buffered **by the slave wrapper** (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected each of the other processor modules through an interconnect. Each interprocessor control includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.); buffering by **the master wrapper of** the master **interface unit** data from the master to be transferred over the interconnect until a second **optimal** amount of data is buffered **by the master wrapper**; transferring the buffered data **from the master wrapper to the slave wrapper** when said second **optimal** amount of data has been buffered by the master wrapper (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where each inter-processor control for each processor as an input and output buffer for sending and receiving data).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit,

however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

6. Consider **claim 3** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein **the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer signal and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer signal**, said first wrapper and said second wrapper are adapted to transfer the buffered data in response to **the** first unbuffer signal and **the** second unbuffer signal, respectively, even if less than said first **optimal** amount and said second **optimal** amount of data is buffered in said first wrapper and said second wrapper (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task).

7. Consider **claim 4** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein **the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer flag and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer flag** said first wrapper and said second wrapper are adapted to transfer the buffered data according to **the** first unbuffer flag and **the** second unbuffer flag, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed flags.).

8. Consider **claim 6** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein at least one of **the first** determination unit **and the second determination unit is further configured to determine** an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave (Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task of sending the data at the appropriate time.).

9. Consider **claim 7** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. disclose wherein said first unbuffer signal is initiated by the slave and said second

unbuffer signal is initiated by the master (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor).

10. Consider **claim 8** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. disclose wherein setting of said first unbuffer flag is initiated by the slave and setting of said second unbuffer flag is initiated by the master (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

11. Consider **claim 9** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. disclose wherein the master is adapted to initiate said first unbuffer signal and said second unbuffer signal (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted

to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor.).

12. Consider **claim 10** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. disclose wherein the master is adapted to initiate setting of said first and second unbuffer flag (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

13. Consider **claim 11** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein the master and the slave communicate with each other using messages of a message-passing communication scheme, wherein the messages contain a message header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper (Col. 31 lines 3-52, where the control packet is considered the head of the message and this identifies the message and how

much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor).

14. Consider **claim 12** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein the master and the slave communicate with each other using packets of a packet based communication scheme, wherein the packets contain a packet header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper (Katzman et al.: Col. 31 lines 3-52, where the control packet identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor and Barroso et al.: Col. 14 lines 36-45, discloses that data-less transactions are 128-bits long and that data packets have the same 128-bit header format, disclosing that both types have headers).

15. Consider **claim 15**, Katzman et al. discloses an integrated circuit comprising: a plurality of processing modules including a first processing module having a first processing memory and a second processing module having a second processing memory (Fig. 1 component 107, Fig. 2, first ¶ of the abstract); a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module (Fig. 1, 19 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61); and a network for connecting the

first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module (fig. 1), **wherein the first interconnect module is connected between the first processing module and the network, and wherein the second interconnect module is connected between the second processing module and the network** (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, the inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Fig. 1 clearly discloses that the interprocessor control 55 of each processing module is between the it's own processing module and those of the other processing modules.); wherein the first interconnect module includes a first memory for buffering first data from the first processing module **the first interconnect module further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory** (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, where the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Each interprocessor control includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.), and the second interconnect module includes a second memory for

buffering second data from the second processing module, **the first interconnect module further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory** (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, where the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Each interprocessor control includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.), the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches **the** first **optimal** amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches **the** second **optimal** amount (Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of

Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

16. Consider **claim 16** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. disclose wherein the plurality of interconnect modules manages the communication connection freeing the plurality of processing modules to perform data processing (col. 5 lines 13-22, Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32).

17. Consider **claim 17** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first interconnect module has a first determination unit that determines the first burst length and the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where there are variable burst

lengths and the length is determined by various attributes including the network of buses providing the communication path).

18. Consider **claim 18** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the first burst length differs from the second burst length (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53).

19. Consider **claim 19** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the network comprises a communication property device that determines the properties of the network for a requested communication and provides the properties to the first determination unit and the second determination unit for determining the first burst length and the second burst length (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where the burst time and length are dynamic and depend on many changing parameters which determine what these two parameters will be and circuitry is making these determinations).

20. Consider **claim 20** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. discloses wherein the first interconnect module comprises a first communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second determination unit (fig. 19, 22 and

23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where the burst time and length are dynamic and depend on many changing parameters which determine what these two parameters will be and circuitry is making these determinations).

21. Consider **claim 21** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting reaching the first amount and the second amount (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed command.).

22. Consider **claim 22** as applied to **claim 21** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously (col. 4 lines 51-59, col. 6 lines 28-33).

23. Consider **claim 23** as applied to **claim 21** above, Katzman et al. in view of Barroso et al. discloses wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory (Col. 16 lines 17-21 and 39-51, Col. 17 lines 32-64, Col. 22-23 lines

24-32 and Col. 27 lines 17-32, where requests for services or data can be request by one processor to another which cases that data to be loaded into the output queue and sent to the requesting processor).

24. Consider **claim 24** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. discloses wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory (Col. 16 lines 17-29 and 39-51, Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where the processor can send a message to send/ flush the data out of the out queue to another processor).

Response to Arguments

25. Applicant's arguments filed 9/9/2010 have been fully considered but they are not persuasive.

26. The Applicant first argues that Katzman does not disclose a determination unit for determining an optimal first or second amount of data to be buffer, however as rejected above in the independent claims, Katzman: Col. 7 lines 8-37 and col. 18-19 lines 10-15, discloses optimizing efficient use of bandwidth in the system and that interprocessor controls 55 of fig. 1 uses input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered and the fill logic is considered part of the determination unit because it is determining when the buffer is full and ready to send data.

27. Secondly the Applicant argues that Katzman does not disclose that the interface units/interconnect modules are between the slave and the network and between the master and the network, however as stated in the rejections of the independent claims above, Katzman in fig. 1 illustrates that the interprocessor control 55, connected to its corresponding processing modules 105 and 107, is between its respective processing module and the network (X and Y buses), where the sending processing module is the master and the receiving one is the slave. Thus the interface units/interconnect modules are between the processing master/slave modules and the network.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael Alsip
Examiner
Art Unit 2186

/Michael Alsip/
Examiner, Art Unit 2186

October 20, 2010

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	**Art Unit**
	MICHAEL ALSIP	2186

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/02/2009	12/09/2009	03/16/2010	07/12/2010	10/20/2010				
	1	✓	✓	✓	✓	✓				
	2	✓	✓	-	-	-				
	3	✓	✓	✓	✓	✓				
	4	✓	✓	✓	✓	✓				
	5	✓	✓	✓	✓	-				
	6	✓	✓	✓	✓	✓				
	7	✓	✓	✓	✓	✓				
	8	✓	✓	✓	✓	✓				
	9	✓	✓	✓	✓	✓				
	10	✓	✓	✓	✓	✓				
	11	✓	✓	✓	✓	✓				
	12	✓	✓	✓	✓	✓				
	13	✓	✓	✓	✓	✓				
	14	✓	✓	✓	✓	✓				
	15		✓	✓	✓	✓				
	16		✓	✓	✓	✓				
	17		✓	✓	✓	✓				
	18		✓	✓	✓	✓				
	19		✓	✓	✓	✓				
	20		✓	✓	✓	✓				
	21		✓	✓	✓	✓				
	22		✓	✓	✓	✓				
	23		✓	✓	✓	✓				
	24		✓	✓	✓	✓				

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	Art Unit
	MICHAEL ALSIP	2186

SEARCHED

Class	Subclass	Date	Examiner
711	118 limited w/ text	10/20/2010	MA
711	141 limited w/ text	10/20/2010	MA
710	57 limited w/ text	10/20/2010	MA
710	100 limited w/ text	10/20/2010	MA

SEARCH NOTES

Search Notes	Date	Examiner
inventor name and assignee search in eDAN and EAST	10/20/2010	MA
class/subclass and keyword search in EAST	10/20/2010	MA

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

/MICHAEL ALSIP/ Examiner.Art Unit 2186	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L2	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L3	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L4	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L5	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L6	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L7	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42

L8	1930	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L9	312	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L10	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L11	16	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L12	327	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
L13	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L14	46	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L15	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
L16	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43

L17	106	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L18	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L19	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L20	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L21	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L22	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L23	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L24	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L25	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L26	168	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L27	12	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L28	290	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L29	18	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L30	14	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L31	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L32	64	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L33	18	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L34	17427	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L35	1	(koninklijke philips electronics).as. burst flush module buffer$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L36	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L37	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L38	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L39	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L40	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L41	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L42	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L43	1930	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L44	312	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L45	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L46	16	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L47	327	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L48	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L49	46	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L50	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
L51	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
L52	106	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L53	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L54	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L55	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L56	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L57	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L58	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L59	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L60	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L61	168	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L62	12	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L63	290	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L64	18	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L65	14	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L66	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L67	64	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L68	18	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L69	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L70	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L71	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L72	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L73	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L74	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L75	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L76	1930	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L77	312	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L78	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L79	16	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L80	327	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L81	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L82	46	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L83	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
L84	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
L85	106	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L86	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L87	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L88	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L89	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L90	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L91	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L92	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L93	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L94	168	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L95	12	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L96	290	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L97	18	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L98	14	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L99	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L100	64	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L101	18	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L102	17427	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L103	1	(koninklijke philips electronics).as. burst flush module buffer$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L104	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L105	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L106	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L107	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L108	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L109	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L110	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L111	1930	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L112	312	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L113	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L114	16	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L115	327	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L116	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L117	46	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L118	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
L119	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
L120	106	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L121	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L122	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L123	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L124	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L125	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L126	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L127	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L128	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L129	168	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L130	12	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L131	290	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L132	18	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L133	14	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L134	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L135	64	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L136	18	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L137	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L138	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L139	168	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L140	18	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L141	14	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L142	14	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L143	64	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L144	64	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L145	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L146	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L147	46	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

L148	16	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L149	5	US-6493776-$.DID. OR US-6397287-$.DID. OR US-6393500-$.DID. OR US-5987552-$.DID. OR US-6629253-$.DID.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
L150	2	"20030101307".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
L151	5	"2005026964".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S1	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 12:45
S2	700	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:48
S3	356	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:50
S4	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:58

S5	52	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:59
S6	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:04
S7	42	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:20
S8	1640	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S9	286	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S10	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:26
S11	11	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28
S12	298	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28

S13	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:29
S14	39	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:35
S15	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:36
S16	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:39
S17	104	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S18	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S19	182	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S20	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S21	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16

S22	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:17
S23	325	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:19
S24	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:20
S25	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 11:31
S26	145	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S27	10	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S28	245	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S29	13	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04

S30	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S31	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S32	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S33	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S35	15075	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
S36	1	(koninklijke philips electronics).as. burst flush module buffer$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
S37	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S38	723	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S39	368	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S40	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S41	61	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S42	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S43	43	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S44	1746	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S45	298	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S46	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S47	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S48	310	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S49	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S50	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S51	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
S52	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
S53	104	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S54	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S55	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S56	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S57	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S58	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S59	340	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S60	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S61	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S62	151	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S63	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S64	256	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S65	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S66	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S67	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S68	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S69	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S70	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S71	737	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S72	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S73	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S74	63	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S75	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S76	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S77	1794	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S78	299	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S79	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S80	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S81	312	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S82	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S83	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S84	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S85	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S86	105	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S87	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S88	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S89	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S90	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S91	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S92	344	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S93	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S94	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S95	154	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S96	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S97	264	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S98	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S99	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S100	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S101	60	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S102	17	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S103	15892	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S104	1	(koninklijke philips electronics).as. burst flush module buffer$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S105	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S106	737	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S107	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S108	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S109	63	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S110	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S111	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S112	1794	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S113	299	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S114	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S115	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S116	312	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S117	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S118	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S119	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S120	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S121	105	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S122	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S123	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S124	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S125	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S126	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S127	344	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S128	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S129	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S130	154	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S131	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S132	264	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S133	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S134	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S135	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S136	60	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S137	17	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S138	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S139	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S140	160	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S141	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S142	14	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S143	14	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S144	61	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S145	61	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10

S146	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S147	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:11
S148	46	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:11
S149	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:12
S150	5	US-6493776-$.DID. OR US-6397287-$.DID. OR US-6393500-$.DID. OR US-5987552-$.DID. OR US-6629253-$.DID.	US-PGPUB; USPAT; USOCR	AND	ON	2010/07/12 14:13
S151	2	"20030101307".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:14
S152	5	"2005026964".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:14

EAST Search History (Interference)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Atty. Docket: NL040529US1
Andrei RADULESCU, et al.	Confirmation No. 4172
Serial No. 11/569,083	Group Art Unit: 2186
Filed: November 14, 2006	Examiner: ALSIP, Michael

Title: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

Mail Stop Amendment
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action mailed on October 22, 2010, please amend the above-identified application and consider the remarks as follows:

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) An integrated circuit comprising:

a plurality of processing modules being connected with an interconnect and each of the plurality of processing modules having a memory, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests;

a first interface unit coupled to the slave and including a first wrapper for buffering data from the slave to be transferred over the interconnect to the master, the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and wherein the buffered data are transferred when said first optimal amount of data has been buffered by the first wrapper, and wherein the first interface unit including the first wrapper and the first determination unit is connected between the slave and the

interconnect; and

a second interface unit coupled to the master and including a second wrapper for buffering data from the master to be transferred over the interconnect, the second interface unit further including a second determination unit, wherein second ~~first~~ determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and wherein the buffered data are transferred when said second optimal amount of data has been buffered by the second wrapper, and wherein the second interface unit including the second wrapper and the second determination unit is connected between the master and the interconnect,

wherein a packet size of the data transferred over the interconnect is adapted according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the first determination unit and the second determination unit.

Claim 2 (Canceled)

3.(Previously Presented) The integrated circuit according to claim 1, wherein the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer signal and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer signal, and wherein said first wrapper and said second wrapper are adapted to

transfer the buffered data in response to the first unbuffer signal and the second unbuffer signal, respectively, even if less than said first optimal amount and said second optimal amount of data is buffered in said first wrapper and said second wrapper.

4.(Previously Presented) The integrated circuit according to claim 1, wherein the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer flag and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer flag, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data according to the first unbuffer flag and the second unbuffer flag, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

Claim 5 (Canceled)

6.(Currently Amended) The integrated circuit according to claim 1, wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data

producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.

7.(Previously Presented) The integrated circuit according to claim 3, wherein said first unbuffer signal is initiated by the slave and said second unbuffer signal is initiated by the master.

8.(Previously Presented) The integrated circuit according to claim 4, wherein setting of said first unbuffer flag is initiated by the slave and setting of said second unbuffer flag is initiated by the master.

9.(Previously Presented) The integrated circuit according to claim 3, wherein the master is adapted to initiate said first unbuffer signal and said second unbuffer signal.

10.(Previously Presented) The integrated circuit according to claim 4, wherein the master is adapted to initiate setting of said first and second unbuffer flag.

11.(Previously Presented) The integrated circuit according to claim 1, wherein the master and the slave communicate with each other using messages of a message-passing communication scheme, wherein the messages contain a message header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

12.(Previously Presented) The integrated circuit according to claim 1, wherein the master and the slave communicate with each other using packets of a packet based communication scheme, wherein the packets contain a packet header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper.

13.(Currently Amended) A method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect through interface units, wherein a first processing module communicates to a second processing module using transactions, the method comprising the acts of:

configuring the first processing module having a first memory as a master the

provides requests;

configuring the second processing module having a second memory as a slave the provides responses to the requests;

connecting the master to a master interface unit of the interface units;

connecting the master interface unit to the interconnect so that the master interface unit is between the master and the interconnect;

connecting the slave to a slave interface unit of the interface units;

connecting the slave interface unit to the interconnect so that the slave interface unit is between the slave and the interconnect;

determining by a master determination unit of the master interface unit a first optimal amount of data to be buffered by a master wrapper of the master interface unit;

determining by a slave determination unit of the slave interface unit a second optimal amount of data to be buffered by a slave wrapper of the slave interface unit;

buffering by the slave wrapper of the slave interface unit data from the slave to be transferred over the interconnect until a first optimal amount of data is buffered;

transferring the buffered data from the slave wrapper to the master wrapper when said first optimal amount of data has been buffered by the slave wrapper;

buffering by the master wrapper of the master interface unit data from the master to be transferred over the interconnect until a second optimal amount of data is buffered by the master wrapper;

transferring the buffered data from the master wrapper to the slave wrapper when said second optimal amount of data has been buffered by the master wrapper,

wherein a packet size of the data transferred over the interconnect is adapted according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the master determination unit and the slave determination unit.

14.(Currently Amended) A data processing system, comprising:

a plurality of processing modules each having a memory and being connected with an interconnect, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests; and

a first interface unit coupled to the slave and including a first wrapper for buffering data from the slave to be transferred over the interconnect, the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and wherein the buffered data are transferred when said first optimal amount of data has been buffered by the first wrapper, and wherein the first interface unit including the first wrapper and the first determination unit is connected between the slave and the interconnect; and

a second interface unit coupled to the master and including a second wrapper for buffering data from the master to be transferred over the interconnect, the second interface unit further including a second determination unit, wherein second first determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and wherein the buffered data are transferred when said second optimal amount of data has been buffered by the second wrapper, and wherein the second interface unit including the second wrapper and the second determination unit is connected between the master and the interconnect,

wherein a packet size of the data transferred over the interconnect is adapted according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the first determination unit and the second determination unit.

15.(Currently Amended) An integrated circuit comprising:

a plurality of processing modules including a first processing module having a first processing memory and a second processing module having a second processing memory;

a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second

interconnect module; and

a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module, wherein the first interconnect module is connected between the first processing module and the network, and wherein the second interconnect module is connected between the second processing module and the network;

wherein the first interconnect module includes a first memory for buffering first data from the first processing module, the first interconnect module further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory, and the second interconnect module includes a second memory for buffering second data from the second processing module, the second interconnect module further including a second determination unit, wherein the second determination unit is configured to determine a second optimal amount of data to be buffered by the second memory,

the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches the first optimal amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches the second optimal amount

wherein a packet size of the data transferred over the interconnect is adapted

according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the first determination unit and the second determination unit.

16.(Previously Presented) The integrated circuit of claim 15, wherein the plurality of interconnect modules manages the communication connection freeing the plurality of processing modules to perform data processing.

17.(Previously Presented) The integrated circuit of claim 15, wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first interconnect module has a first determination unit that determines the first burst length and the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection.

18.(Previously Presented) The integrated circuit of claim 17, wherein the first burst length differs from the second burst length.

19.(Previously Presented) The integrated circuit of claim 17, wherein the network comprises a communication property device that determines the properties of the network for a requested communication and provides the properties to the first determination unit and the second determination unit for determining the first burst length and the second burst length.

20.(Previously Presented) The integrated circuit of claim 17, wherein the first interconnect module comprises a first communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second determination unit.

21.(Previously Presented) The integrated circuit of claim 15, wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting to reach the first amount and the second amount.

22.(Previously Presented) The integrated circuit of claim 21, wherein the first

processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously.

23.(Previously Presented) The integrated circuit of claim 21, wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory.

24.(Previously Presented) The integrated circuit of claim 15, wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory.

REMARKS

This Amendment is being filed in response to the Office Action mailed October 22, 2010, which has been reviewed and carefully considered. Reconsideration and allowance of the present application in view of the amendments made above and the remarks to follow are respectfully requested.

Claims 1, 3-4 and 6-24 are pending in this application, where claims 1, 13, 14 and 15 are independent.

In the Office Action, claims 1, 3-4 and 6-24 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 4,228,496 (Katzman) in view of U.S. Patent No. 6,668,308 (Barroso). Applicants respectfully traverse and submit that claims 1, 3-4 and 6-24 are patentable over Katzman and Barroso for at least the following reasons.

Katzman is directed to a multiprocessor system that includes separate processor modules 33, shown in FIG 1, where buffers are "clocked either by the processor module or by the bus controller," for asynchronous operation of interprocessor buses and processor module operating at different clocks. (Katzman, column 4, lines 62-63; see also column 5, lines 1-5) For example, a "CPU 105 operates on a different clock from the interprocessor bus clock. During the filling of an outqueue or the emptying of an inqueue in the interprocessor control 55 by the CPU, the operation takes place at the CPU clock rate. However, transmission of packets over the interprocessor bus always takes place at the bus clock rate." (Katzman, column 17, lines 49-53)

Katzman further discloses on column 17, lines 54-64:

> It is an important feature of the present invention that the information transmitted over the interprocessor bus is transferred at high transmission rates without any required correspondence to the clock rates of the various CPUs 105. The information transfer rate over the interprocessor bus is also substantially faster than would be permitted by direct memory accesses into and out of the memory sections 107 at memory speed. This ensures that there is adequate bus bandwidth even when a large number of processor modules is connected in a multiprocessor system. (Emphasis added)

Buffers are used to accomplish faster transfer rates over the interprocessor bus. Buffers are filled until a count of 16. In particular, "[o]n the sixteenth occurrence of the store outqueue signal a transition from the FILL to the FULL state, as illustrated by the solid line arrow in FIG. 7, is allowed." (Katzman, column 22, lines 31-32) Further, Katzman discloses on column 27, lines 26-32:

> As the words are being read from memory, the address word is being incremented by one, and the count of the words to be sent is being decremented by one. **If the count reaches zero before fifteen words are read from memory, the remainder of the outqueue buffer is filled with zeros to pad out the data packet**. (Emphasis added)

That is, the output of the Katzman outqueue buffer is always the **same size** where, any "remainder of the outqueue buffer is filled with zeros to pad out the data packet," as specifically recited column 27, lines 30-31. (Emphasis added)

In stark contrast, the present invention as recited in independent claim 1, and similarly recited in independent claims 13, 14 and 15, amongst other patentable elements recites (illustrative emphasis provided):

> wherein a packet size of the data transferred over the interconnect is **adapted according to properties of actual communication** over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the first determination unit and the second determination unit.

A **determination unit** that determines packet size of transferred data, where the packet size of the data transferred over the interconnect is **adapted** according to properties of actual communication, is nowhere disclosed or suggested in Katzman. Rather, in Katzman, all the packet sizes that are transferred over a bus have the same size. While Katzman discloses on column 6, lines 28-33 that "[e]ach input/output channel is block multiplexed to handle several block transfers of data from several device controllers on an apparent simultaneous basis. This is accomplished by interleaving variable length bursts of data in transfers between the input/output channel and stress responsive buffers in the device controllers," such a disclosure is related to interleaving variable length bursts of data, where the interleaving variable length bursts of data is read out from the Katzman outqueue buffer at the **fixed packet size**. Barroso and Barroso are cited to allegedly show other features and do not remedy the deficiencies in Katzman.

Accordingly, it is respectfully submitted that independent claims 1, 13, 14 and 15 are allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 3-4, 6-12 and 16-24 should also be allowed at least based on their dependence from independent claims 1 and 15.

In addition, Applicants deny any statement, position or averment of the Examiner

that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

By _____

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January 11, 2011

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Electronic Acknowledgement Receipt

EFS ID:	9267414
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
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Application Type:	U.S. National Stage under 35 USC 371

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NL040529US1_amd_2011_Jan_20.pdf	636345 b36397a51c7be8088e556653eefb3ecb5d25be8b	yes	17

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	13
	Applicant Arguments/Remarks Made in an Amendment	14	17
Warnings:			
Information:			
	Total Files Size (in bytes):	636345	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/569,083	11/14/2006	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	01/20/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 22	Minus	** 24	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/LAWANDA MILTON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	NL040529US1	4172

24737 7590 02/24/2011

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EXAMINER	
ALSIP, MICHAEL	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
02/24/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/569,083	RADULESCU ET AL.	
	Examiner	Art Unit	
	MICHAEL ALSIP	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4 and 6-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 7-24* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. **Claims 1, 3-4 and 7-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Katzman et al. (US 4,228,496) and further in view of Barroso et al. (US 6,668,308) and Bahadiroglu (US 2002/0186660).

4. Consider **claims 1 and 14**, Katzman et al. discloses data processing system and integrated circuit comprising a plurality of processing modules being connected with an interconnect and each of the plurality of processing modules having a memory, wherein a first processing module communicates to a second processing module using transactions (Fig. 1 component 107, Fig. 2, first ¶ of the abstract, each processing module has a memory 107.); wherein the first processing module is a master for providing requests and the second processing module is a slave for providing

responses to the requests (Col. 16 lines 17-51, this claim language states that the first processing module is a master and that its function is to provide requests to the second processing module, now called a slave, and the function of the slave is to provide a response to the requests. Katzman et al. discloses this feature in the cited areas above, by disclosing that a process running on one processor module (master) may need to request the service of another process running on another processing unit (slave) and therefore the first processor will send a request to the second processor module and when the process on the second processor module has completed the request, it will return a response back to the first processor); a first interface unit coupled to the slave and including a first wrapper for buffering data from said the slave to be transferred over the interconnect to the master the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and wherein the buffered data are transferred when said first optimal amount of data has been buffered, by the first wrapper and wherein the first interface unit including the first wrapper and the first determination unit is connected between the slave and the interconnect (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, where the term "wrapper" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Each interprocessor control includes input and output queues and include

fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.); and a second interface unit coupled to the master and including a second wrapper for buffering data from the master to be transferred over the interconnect, the second interface unit further including a second determination unit, wherein the second determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and wherein the buffered data are transferred when said second optimal amount of data has been buffered by the second wrapper and wherein the second interface unit including the second wrapper and the second determination unit is connected between the master and the interconnect (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, where the term "wrapper" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Each interprocessor control includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

As for the new limitation: "**wherein a packet size of the data transferred over the interconnect is adapted according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the first determination unit and the second determination unit.**", Katzman et al. teaches in Col. 27 lines 17-32 that variable amounts of actual user data can be sent across the network, but instead of sending variable sized packets, the packets are just padded with zeros, however Bahadiroglu discloses that actual communication properties can be used to optimize the packet size and inter-packet interval for transmission of those packets and therefore meets the new claim requirements (pg. 1 ¶ [0001] and pg. 7 ¶'s [0047]-[0048]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have adaptable sized packets based upon communication properties in the system of Katzman et al., because Bahadiroglu discloses that doing so enhances and optimizes data transmission rates (pg. 1 ¶ [0001] and pg. 7 ¶'s [0047]-[0048]).

5. Consider **claim 13**, Katzman et al. discloses a method for buffering data having a plurality of processing modules being connected with an interconnect through interface units, wherein a first processing module communicates to a second processing module using transactions (Fig. 1, 2 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, first ¶ of the abstract), the method comprising the acts of: configuring the first processing module having a first memory as a master the provides requests; configuring the second processing module having a second memory as a slave the provides responses to the requests (fig. 1 component 107, Col. 16 lines 17-51, this claim language states that the first processing module is a master and that its function is to provide requests to the second processing module, now called a slave, and the function of the slave is to provide a response to the requests. Katzman et al. discloses this feature in the cited areas above, by disclosing that a process running on one processor module (master) may need to request the service of another process running on another processing unit (slave) and therefore the first processor will send a request to the second processor module and when the process on the second processor module has completed the request, it will return a response back to the first processor. Also each processor module has a memory 107 associated with it.); connecting the master to a master interface unit of the interface units; connecting the master interface unit to the interconnect so that the master interface unit is between the master and the interconnect; connecting the slave to a slave interface unit of the interface units; connecting the slave wrapper to the interconnect so that the slave interface unit is between the slave and the interconnect (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5

lines 24-61, where the term "interface unit" is considered the inter-processor control which contains inqueue and outqueue buffers for transferring data between processor modules.); determining by a master determination unit of the master interface unit a first optimal amount of data to be buffered by a master wrapper of the master interface unit; determining by a slave determination unit of the slave interface unit a second optimal amount of data to be buffered by a slave wrapper of the slave interface unit (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, where the term "wrapper means" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Each interprocessor control includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.); buffering by the slave wrapper of the slave the slave interface unit data from the slave to be transferred over the interconnect until a first optimal amount of data is buffered; transferring the buffered data from the slave wrapper to the master wrapper when said first optimal amount of data has been buffered by the slave wrapper (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where the term "wrapper" is considered to be a buffer or queue like memory and the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected each of the other processor

modules through an interconnect. Each interprocessor control includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.); buffering by the master wrapper of the master interface unit data from the master to be transferred over the interconnect until a second optimal amount of data is buffered by the master wrapper; transferring the buffered data from the master wrapper to the slave wrapper when said second optimal amount of data has been buffered by the master wrapper (Fig. 1 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, where each inter-processor control for each processor as an input and output buffer for sending and receiving data).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex, processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

As for the new limitation: "**wherein a packet size of the data transferred over the interconnect is adapted according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the master determination unit and the slave determination unit.**", Katzman et al. teaches in Col. 27 lines 17-32 that variable amounts of actual user data can be sent across the network, but instead of sending variable sized packets, the packets are just padded with zeros, however Bahadiroglu discloses that actual communication properties can be used to optimize the packet size and inter-packet interval for transmission of those packets and therefore meets the new claim requirements (pg. 1 ¶ [0001] and pg. 7 ¶'s [0047]-[0048]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have adaptable sized packets based upon communication properties in the system of Katzman et al., because Bahadiroglu discloses that doing so enhances and optimizes data transmission rates (pg. 1 ¶ [0001] and pg. 7 ¶'s [0047]-[0048]).

6. Consider **claim 3** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. disclose wherein the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer signal and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer signal, said first wrapper and said second wrapper are adapted to transfer the buffered data in response to the first unbuffer signal and the second unbuffer signal, respectively, even if less than said first optimal amount and said second optimal amount of data is buffered in said first wrapper and said second wrapper (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines

26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task).

7. Consider **claim 4** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. and Bahadiroglu disclose wherein the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer flag and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer flag said first wrapper and said second wrapper are adapted to transfer the buffered data according to the first unbuffer flag and **the** second unbuffer flag, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed flags.).

8. Consider **claim 7** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. and Bahadiroglu disclose wherein said first unbuffer signal is initiated by the slave and said second unbuffer signal is initiated by the master (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the

buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor).

9. Consider **claim 8** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. and Bahadiroglu disclose wherein setting of said first unbuffer flag is initiated by the slave and setting of said second unbuffer flag is initiated by the master (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

10. Consider **claim 9** as applied to **claim 3** above, Katzman et al. in view of Barroso et al. and Bahadiroglu disclose wherein the master is adapted to initiate said first unbuffer signal and said second unbuffer signal (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor.).

11. Consider **claim 10** as applied to **claim 4** above, Katzman et al. in view of Barroso et al. and Bahadiroglu disclose wherein the master is adapted to initiate setting of said first and second unbuffer flag (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 26-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state changes occur and signals are asserted to accomplish the task. Each processor has an inter-processor control for communicating between each other, which contains the buffers and control logic, therefore the states and asserted signals are used by each processor to communicate and receive data packets for any other processor. Where the state logic is considered to be equivalent to the claimed flags.).

12. Consider **claim 11** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. and Bahadiroglu disclose wherein the master and the slave communicate with each other using messages of a message-passing communication scheme, wherein the messages contain a message header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper (Col. 31 lines 3-52, where the control packet is considered the head of the message and this identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor).

13. Consider **claim 12** as applied to **claim 1** above, Katzman et al. in view of Barroso et al. and Bahadiroglu disclose wherein the master and the slave communicate

with each other using packets of a packet based communication scheme, wherein the packets contain a packet header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper (Katzman et al.: Col. 31 lines 3-52, where the control packet identifies the message and how much data is to be received, therefore indicating how much data is to be transferred into the buffer of the receiving processor and Barroso et al.: Col. 14 lines 36-45, discloses that data-less transactions are 128-bits long and that data packets have the same 128-bit header format, disclosing that both types have headers).

14. Consider **claim 15**, Katzman et al. discloses an integrated circuit comprising: a plurality of processing modules including a first processing module having a first processing memory and a second processing module having a second processing memory (Fig. 1 component 107, Fig. 2, first ¶ of the abstract); a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module (Fig. 1, 19 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61); and a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module (fig. 1), wherein the first interconnect module is connected between the first processing module and the network, and wherein the second interconnect

module is connected between the second processing module and the network (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, the inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Fig. 1 clearly discloses that the interprocessor control 55 of each processing module is between the it's own processing module and those of the other processing modules.); wherein the first interconnect module includes a first memory for buffering first data from the first processing module the first interconnect module further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, where the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Each interprocessor control includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.), and the second interconnect module includes a second memory for buffering second data from the second processing module, the first interconnect module further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory (Fig. 1-2, 4-5 and 22, Col. 4 lines 47-67 and Col. 5 lines 24-61, Col. 7 lines 8-37 and col. 18-19 lines 10-15, where

the inter-processor control contains inqueue and outqueue buffers for transferring data between processor modules. This inter-processor control is part of every processor module and is connected to each of the other processor modules through the interconnect. Each interprocessor control includes input and output queues and include fill logic in order to fill the queue buffers with sixteen, sixteen bits words and this number of words is considered the optimal amount of data to be buffered.), the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches the first optimal amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches the second optimal amount (Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32).

Katzman et al. does not explicitly state that have the plurality of processing modules, interconnect and buffer memories all reside on a single integrated circuit, however Barroso et al. does teach this feature (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the multiple processors, buffer memory and interconnection means of Katzman et al. on one integrated chip as disclosed in Barroso et al., because Barroso et al. teaches that multi-processor chips (CMP) use shorter wires as opposed to costly and slow long wires that can adversely affect cycle time and also that integration on a single-chip of a plurality of processor cores outperforms next-generation, more complex,

processors by about 2.3 to 2.9 times on important loads (fig. 1, abstract, Col. 1 lines 36-43, Col. 2 lines 18-24, Col. 4 lines 3-7 and lines 56-67).

As for the new limitation: "**wherein a packet size of the data transferred over the interconnect is adapted according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the first determination unit and the second determination unit.**", Katzman et al. teaches in Col. 27 lines 17-32 that variable amounts of actual user data can be sent across the network, but instead of sending variable sized packets, the packets are just padded with zeros, however Bahadiroglu discloses that actual communication properties can be used to optimize the packet size and inter-packet interval for transmission of those packets and therefore meets the new claim requirements (pg. 1 ¶ [0001] and pg. 7 ¶'s [0047]-[0048]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have adaptable sized packets based upon communication properties in the system of Katzman et al., because Bahadiroglu discloses that doing so enhances and optimizes data transmission rates (pg. 1 ¶ [0001] and pg. 7 ¶'s [0047]-[0048]).

15. Consider **claim 16** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. disclose wherein the plurality of interconnect modules manages the communication connection freeing the plurality of processing modules to perform data processing (col. 5 lines 13-22, Col. 17 lines 32-64, Col. 21 lines 57-67, Col. 22-23 lines 24-32 and Col. 27 lines 26-32).

16. Consider **claim 17** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. and Bahadiroglu discloses wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first interconnect module has a first determination unit that determines the first burst length and the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where there are variable burst lengths and the length is determined by various attributes including the network of buses providing the communication path).

17. Consider **claim 18** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. and Bahadiroglu discloses wherein the first burst length differs from the second burst length (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53).

18. Consider **claim 19** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. and Bahadiroglu discloses wherein the network comprises a communication property device that determines the properties of the network for a requested communication and provides the properties to the first determination unit and the second determination unit for determining the first burst length and the second burst length (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col.

44 lines 48-53 and col. 45 lines 45-53, where the burst time and length are dynamic and depend on many changing parameters which determine what these two parameters will be and circuitry is making these determinations).

19. Consider **claim 20** as applied to **claim 17** above, Katzman et al. in view of Barroso et al. and Bahadiroglu discloses wherein the first interconnect module comprises a first communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second determination unit (fig. 19, 22 and 23, col. 6 lines 28-33, col. 7 lines 47-56, Col. 31 lines 3-52, col. 44 lines 48-53 and col. 45 lines 45-53, where the burst time and length are dynamic and depend on many changing parameters which determine what these two parameters will be and circuitry is making these determinations).

20. Consider **claim 21** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. and Bahadiroglu discloses wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting reaching the first amount and the second amount (Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where during the process of filling and sending a packet from the out queue buffer to the requesting processor module, many state

changes occur and signals are asserted to accomplish the task. Where the state logic is considered to be equivalent to the claimed command.).

21. Consider **claim 22** as applied to **claim 21** above, Katzman et al. in view of Barroso et al. and Bahadiroglu discloses wherein the first processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously (col. 4 lines 51-59, col. 6 lines 28-33).

22. Consider **claim 23** as applied to **claim 21** above, Katzman et al. in view of Barroso et al. and Bahadiroglu discloses wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory (Col. 16 lines 17-21 and 39-51, Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where requests for services or data can be request by one processor to another which cases that data to be loaded into the output queue and sent to the requesting processor).

23. Consider **claim 24** as applied to **claim 15** above, Katzman et al. in view of Barroso et al. and Bahadiroglu discloses wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory (Col. 16 lines 17-29 and 39-51, Col. 17 lines 32-64, Col. 22-23 lines 24-32 and Col. 27 lines 17-32, where the processor can send a message to send/ flush the data out of the out queue to another processor).

Allowable Subject Matter

24. **Claim 6** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

25. The following is a statement of reasons for the indication of allowable subject matter: The Examiner is unable to find in the prior art a disclosure of a system that determines the optimal time to send data over a communication line using all of the listed conditions/requirements.

Response to Arguments

26. Applicant's arguments with respect to the newly introduced claim limitations have been considered but are moot in view of the new ground(s) of rejection/indication of allowable subject matter.

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Thursday 9:00AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shane M Thomas/
Primary Examiner, Art Unit 2186

Michael Alsip
Examiner
Art Unit 2186

/Michael Alsip/

Examiner, Art Unit 2186

February 17, 2011

Notice of References Cited	Application/Control No. 11/569,083	Applicant(s)/Patent Under Reexamination RADULESCU ET AL.	
	Examiner MICHAEL ALSIP	Art Unit 2186	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0186660	12-2002	Bahadiroglu, Murat I.	370/248
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	**Art Unit**
	MICHAEL ALSIP	2186

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
711	118 limited w/ text	2/17/2011	MA
711	141 limited w/ text	2/17/2011	MA
710	57 limited w/ text	2/17/2011	MA
710	100 limited w/ text	2/17/2011	MA

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
inventor name and assignee search in eDAN and EAST	2/17/2011	MA
class/subclass and keyword search in EAST	2/17/2011	MA

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

/MICHAEL ALSIP/ Examiner.Art Unit 2186	

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11569083	RADULESCU ET AL.
	Examiner	**Art Unit**
	MICHAEL ALSIP	2186

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/02/2009	12/09/2009	03/16/2010	07/12/2010	10/20/2010	02/17/2011			
	1	✓	✓	✓	✓	✓	✓			
	2	✓	✓	-	-	-	-			
	3	✓	✓	✓	✓	✓	✓			
	4	✓	✓	✓	✓	✓	✓			
	5	✓	✓	✓	✓	-	-			
	6	✓	✓	✓	✓	✓	O			
	7	✓	✓	✓	✓	✓	✓			
	8	✓	✓	✓	✓	✓	✓			
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	11	✓	✓	✓	✓	✓	✓			
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	19		✓	✓	✓	✓	✓			
	20		✓	✓	✓	✓	✓			
	21		✓	✓	✓	✓	✓			
	22		✓	✓	✓	✓	✓			
	23		✓	✓	✓	✓	✓			
	24		✓	✓	✓	✓	✓			

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 12:45
S2	700	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:48
S3	356	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:50
S4	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:58
S5	52	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:59
S6	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:04
S7	42	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:20

S8	1640	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S9	286	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S10	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:26
S11	11	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28
S12	298	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28
S13	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:29
S14	39	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:35
S15	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:36
S16	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:39

S17	104	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S18	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S19	182	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S20	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S21	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S22	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:17
S23	325	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:19
S24	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:20

S25	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 11:31
S26	145	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S27	10	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S28	245	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S29	13	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S30	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S31	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S32	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05

S33	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S35	15075	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
S36	1	(koninklijke philips electronics).as. burst flush module buffer$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
S37	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S38	723	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S39	368	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S40	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S41	61	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S42	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S43	43	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S44	1746	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S45	298	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S46	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S47	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S48	310	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S49	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S50	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S51	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
S52	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
S53	104	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S54	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S55	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S56	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S57	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S58	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S59	340	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S60	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S61	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S62	151	"711/118".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S63	11	"711/118".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S64	256	"711/141".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S65	16	"711/141".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S66	13	"710/57".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S67	2	"710/57".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S68	58	"710/100".ccls. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S69	16	"710/100".ccls. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S70	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S71	737	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S72	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S73	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S74	63	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S75	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S76	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S77	1794	"711".clas. (multi $processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S78	299	"711".clas. (multi $processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S79	2	"711".clas. (multi $processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S80	13	"711".clas. (multi $processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S81	312	"711".clas. (multi $processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S82	8	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S83	45	"711".clas. (multi $processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S84	2	("20040039880" | "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S85	10	("20010047439" | "20030070059" | "4831517" | "5388074" | "5706491" | "5819254" | "6078983" | "6269436" | "6532531" | "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S86	105	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S87	1	"711".clas. (multi $processor) (integrated near circuit) (queue or buffer) interprocessor near shar$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S88	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S89	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S90	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S91	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59