

S92	344	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S93	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S94	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S95	154	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S96	11	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S97	264	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S98	16	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S99	13	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S100	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S101	60	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S102	17	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S103	15892	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S104	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S105	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S106	737	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S107	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S108	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S109	63	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S110	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S111	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S112	1794	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S113	299	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S114	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S115	13	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S116	312	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S117	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S118	45	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S119	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S120	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S121	105	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S122	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S123	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S124	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S125	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S126	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S127	344	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S128	12	"711".cls.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S129	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S130	154	"711/118".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S131	11	"711/118".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S132	264	"711/141".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S133	16	"711/141".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S134	13	"710/57".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S135	2	"710/57".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S136	60	"710/100".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S137	17	"710/100".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S138	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S139	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S140	160	"711/118".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10

S141	16	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S142	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S143	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S144	61	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S145	61	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S146	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S147	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:11
S148	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:11

S149	13	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:12
S150	5	US-6493776-\$.DID. OR US-6397287-\$.DID. OR US-6393500-\$.DID. OR US-5987552-\$.DID. OR US-6629253-\$.DID.	US-PGPUB; USPAT; USOCR	AND	ON	2010/07/12 14:13
S151	2	"20030101307".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:14
S152	5	"2005026964".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:14
S153	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S154	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S155	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S156	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42

S157	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S158	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S159	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S160	1930	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S161	312	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S162	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S163	16	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S164	327	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42

S165	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S166	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S167	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S168	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S169	106	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S170	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S171	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S172	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S173	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S174	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S175	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S176	12	"711".cls.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S177	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S178	168	"711/118".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S179	12	"711/118".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S180	290	"711/141".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S181	18	"711/141".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S182	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S183	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S184	64	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S185	18	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S186	17427	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S187	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S188	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S189	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S190	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S191	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S192	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S193	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S194	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S195	1930	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S196	312	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S197	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S198	16	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S199	327	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S200	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S201	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S202	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S203	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S204	106	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S205	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S206	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S207	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S208	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S209	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S210	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S211	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S212	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S213	168	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S214	12	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S215	290	"711/141".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S216	18	"711/141".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S217	14	"710/57".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S218	2	"710/57".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S219	64	"710/100".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S220	18	"710/100".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S221	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S222	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S223	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S224	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S225	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S226	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S227	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S228	1930	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S229	312	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S230	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S231	16	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S232	327	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S233	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S234	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S235	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S236	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S237	106	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S238	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S239	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S240	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S241	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S242	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S243	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S244	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S245	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S246	168	"711/118".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S247	12	"711/118".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S248	290	"711/141".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S249	18	"711/141".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S250	14	"710/57".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S251	2	"710/57".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S252	64	"710/100".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S253	18	"710/100".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S254	17427	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S255	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S256	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S257	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S258	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S259	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S260	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S261	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S262	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S263	1930	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S264	312	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S265	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S266	16	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S267	327	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S268	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S269	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S270	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S271	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S272	106	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S273	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S274	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S275	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S276	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S277	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S278	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S279	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S280	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S281	168	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S282	12	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S283	290	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S284	18	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S285	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S286	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S287	64	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S288	18	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S289	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S290	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S291	168	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S292	18	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S293	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S294	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S295	64	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S296	64	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S297	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S298	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S299	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S300	16	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S301	5	US-6493776-\$.DID. OR US-6397287-\$.DID. OR US-6393500-\$.DID. OR US-5987552-\$.DID. OR US-6629253-\$.DID.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S302	2	"20030101307".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S303	5	"2005026964".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S304	1522	(packet adj size) near3 (adapt\$4 or adjust\$4 or variab\$4 or varying or varies)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/02/17 14:13

S305	70	"711".clas. (packet adj size) near3 (adapt\$4 or adjust\$4 or variab\$4 or varying or varies)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/02/17 14:13
S306	902	(packet adj size) near (adapt\$4 or adjust\$4 or variab\$4 or varying or varies)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/02/17 14:22
S307	593	(packet adj size) near (adapt\$4 or adjust\$4 or variab\$4 or varying or varies) processors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/02/17 14:23
S308	3	(packet adj size) near (adapt\$4 or adjust\$4 or variab\$4 or varying or varies) communication near properties	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/02/17 14:23

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**RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2186**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket: NL040529US1

Andrei RADULESCU, et al.

Confirmation No. 4172

Serial No. 11/569,083

Group Art Unit: 2186

Filed: November 14, 2006

Examiner: ALSIP, Michael

Title: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE
BURST LENGTH IN NETWORKS ON CHIPS

Mail Stop AF
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER §1.116

Sir:

In response to the Final Office Action mailed on February 24, 2011, please amend
the above-identified application and consider the remarks as follows:

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) An integrated circuit comprising:

a plurality of processing modules being connected with an interconnect and each of the plurality of processing modules having a memory, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests;

a first interface unit coupled to the slave and including a first wrapper for buffering data from the slave to be transferred over the interconnect to the master, the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and wherein the buffered data are transferred when said first optimal amount of data has been buffered by the first wrapper, and wherein the first interface unit including the first wrapper and the first determination unit is connected between the slave and the

interconnect; and

a second interface unit coupled to the master and including a second wrapper for buffering data from the master to be transferred over the interconnect, the second interface unit further including a second determination unit, wherein second determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and wherein the buffered data are transferred when said second optimal amount of data has been buffered by the second wrapper, and wherein the second interface unit including the second wrapper and the second determination unit is connected between the master and the interconnect,

~~wherein a packet size of the data transferred over the interconnect is adapted according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the first determination unit and the second determination unit~~ wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed,

latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.

Claim 2 (Canceled)

3.(Previously Presented) The integrated circuit according to claim 1, wherein the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer signal and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer signal, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to the first unbuffer signal and the second unbuffer signal, respectively, even if less than said first optimal amount and said second optimal amount of data is buffered in said first wrapper and said second wrapper.

4.(Previously Presented) The integrated circuit according to claim 1, wherein the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer flag and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer flag, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data according to the first unbuffer flag and the second unbuffer flag, respectively, even if less than said first amount and said second amount of data is buffered in said first

wrapper and said second wrapper.

Claims 5-6 (Canceled)

7.(Previously Presented) The integrated circuit according to claim 3, wherein said first unbuffer signal is initiated by the slave and said second unbuffer signal is initiated by the master.

8.(Previously Presented) The integrated circuit according to claim 4, wherein setting of said first unbuffer flag is initiated by the slave and setting of said second unbuffer flag is initiated by the master.

9.(Previously Presented) The integrated circuit according to claim 3, wherein the master is adapted to initiate said first unbuffer signal and said second unbuffer signal.

10.(Previously Presented) The integrated circuit according to claim 4, wherein the master is adapted to initiate setting of said first and second unbuffer flag.

11.(Previously Presented) The integrated circuit according to claim 1, wherein the master and the slave communicate with each other using messages of a message-passing

communication scheme, wherein the messages contain a message header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.

12.(Previously Presented) The integrated circuit according to claim 1, wherein the master and the slave communicate with each other using packets of a packet based communication scheme, wherein the packets contain a packet header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper.

13.(Currently Amended) A method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect through interface units, wherein a first processing module communicates to a second processing module using transactions, the method comprising the acts of:

configuring the first processing module having a first memory as a master the provides requests;

configuring the second processing module having a second memory as a slave the

provides responses to the requests;

connecting the master to a master interface unit of the interface units;

connecting the master interface unit to the interconnect so that the master interface unit is between the master and the interconnect;

connecting the slave to a slave interface unit of the interface units;

connecting the slave interface unit to the interconnect so that the slave interface unit is between the slave and the interconnect;

determining by a master determination unit of the master interface unit a first optimal amount of data to be buffered by a master wrapper of the master interface unit;

determining by a slave determination unit of the slave interface unit a second optimal amount of data to be buffered by a slave wrapper of the slave interface unit;

buffering by the slave wrapper of the slave interface unit data from the slave to be transferred over the interconnect until a first optimal amount of data is buffered;

transferring the buffered data from the slave wrapper to the master wrapper when said first optimal amount of data has been buffered by the slave wrapper;

buffering by the master wrapper of the master interface unit data from the master to be transferred over the interconnect until a second optimal amount of data is buffered by the master wrapper;

transferring the buffered data from the master wrapper to the slave wrapper when said second optimal amount of data has been buffered by the master wrapper,

~~wherein a packet size of the data transferred over the interconnect is adapted according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the master determination unit and the slave determination unit~~ wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.

14.(Currently Amended) A data processing system, comprising:

a plurality of processing modules each having a memory and being connected with an interconnect, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the

requests; and

a first interface unit coupled to the slave and including a first wrapper for buffering data from the slave to be transferred over the interconnect, the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and wherein the buffered data are transferred when said first optimal amount of data has been buffered by the first wrapper, and wherein the first interface unit including the first wrapper and the first determination unit is connected between the slave and the interconnect; and

a second interface unit coupled to the master and including a second wrapper for buffering data from the master to be transferred over the interconnect, the second interface unit further including a second determination unit, wherein second first determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and wherein the buffered data are transferred when said second optimal amount of data has been buffered by the second wrapper, and wherein the second interface unit including the second wrapper and the second determination unit is connected between the master and the interconnect,

~~wherein a packet size of the data transferred over the interconnect is adapted according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the first determination unit and the second determination unit~~ wherein at least one of the first

determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.

15.(Currently Amended) An integrated circuit comprising:

a plurality of processing modules including a first processing module having a first processing memory and a second processing module having a second processing memory;

a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module; and

a network for connecting the first interconnect module to the second interconnect

module in order to provide a communication connection between the first processing module and the second processing module, wherein the first interconnect module is connected between the first processing module and the network, and wherein the second interconnect module is connected between the second processing module and the network;

wherein the first interconnect module includes a first memory for buffering first data from the first processing module, the first interconnect module further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory, and the second interconnect module includes a second memory for buffering second data from the second processing module, the second interconnect module further including a second determination unit, wherein the second determination unit is configured to determine a second optimal amount of data to be buffered by the second memory,

the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches the first optimal amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches the second optimal amount

~~wherein a packet size of the data transferred over the interconnect is adapted according to properties of actual communication over the interconnect among the plurality of processing modules, the packet size being determined by at least one of the first~~

determination unit and the second determination unit wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.

16.(Previously Presented) The integrated circuit of claim 15, wherein the plurality of interconnect modules manages the communication connection freeing the plurality of processing modules to perform data processing.

17.(Previously Presented) The integrated circuit of claim 15, wherein the first interconnect module transfers the first data over the network as a first packet having a first burst length, and the second interconnect module transfers the second data over the network as a second packet having a second burst length; and wherein the first

interconnect module has a first determination unit that determines the first burst length and the second interconnect module has a second determination unit that determines the second burst length in accordance with properties of selected buses of the network that provide the communication connection.

18.(Previously Presented) The integrated circuit of claim 17, wherein the first burst length differs from the second burst length.

19.(Previously Presented) The integrated circuit of claim 17, wherein the network comprises a communication property device that determines the properties of the network for a requested communication and provides the properties to the first determination unit and the second determination unit for determining the first burst length and the second burst length.

20.(Previously Presented) The integrated circuit of claim 17, wherein the first interconnect module comprises a first communication property device that determines the properties of the network for a requested communication for selection of the first burst length by the first determination unit, and the second interconnect module comprises a second communication property device that determines the properties of the network for the requested communication for selection of the second burst length by the second

determination unit.

21.(Previously Presented) The integrated circuit of claim 15, wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting to reach the first amount and the second amount.

22.(Previously Presented) The integrated circuit of claim 21, wherein the first processing module provides the first flushing command and the second flushing command at least one of independently and simultaneously.

23.(Previously Presented) The integrated circuit of claim 21, wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory.

24.(Previously Presented) The integrated circuit of claim 15, wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory.

REMARKS

This Amendment is being filed in response to the Final Office Action mailed February 24, 2011, which has been reviewed and carefully considered. By means of the present amendment, independent claims 1, 13, 14 and 15 have been amended to include the features of canceled claim 6. Accordingly, no new issues requiring a new search have been introduced and entry of the present amendment is respectfully requested. Reconsideration and allowance of the present application in view of the amendments made above and the remarks to follow are respectfully requested.

Claims 1, 3-4 and 7-24 are pending in this application, where claims 1, 13, 14 and 15 are independent.

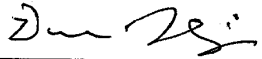
In the Final Office Action, the Examiner indicated that claim 6 would be allowable if rewritten in independent form. Applicants gratefully acknowledge the indication that claim 6 contains patentable subject matter. By means of the present amendment, independent claims 1, 13, 14 and 15 have been amended to include the features of allowable claim 6 which has been canceled without prejudice, without including certain features that are believed to be not necessary for patentability.

Accordingly, it is respectfully submitted that independent claims 1, 13, 14 and 15 are allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 3-4, 7-12 and 16-24 should also be allowed at least based on their dependence from independent claims 1 and 15.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

By 
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March 30, 2011

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Briarcliff Manor, NY 10510-8001
(914) 333-9643

Electronic Acknowledgement Receipt	
EFS ID:	9946394
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	Integrated Circuit And Method For Buffering To Optimize Burst Length In Networks On Chips
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Patti DeMichele
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	NL040529US1
Receipt Date:	25-APR-2011
Filing Date:	14-NOV-2006
Time Stamp:	13:40:24
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NL040529US1_116AMD_2011A pr25.pdf	616547 bf0bb3ede9e9c31efb1694b9e3f6b8b325474747	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment After Final	1	1
	Claims	2	14
	Applicant Arguments/Remarks Made in an Amendment	15	16
Warnings:			
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/569,083		Filing Date 11/14/2006		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300			
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =			X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL		300		
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	04/25/2011	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 21	Minus	** 24	= 0	X \$ =		OR	X \$2=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X \$ =		OR	X \$220=	0
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/TAMMY MCBETH BROWN/

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24737 7590 05/11/2011
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P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER

ALSIP, MICHAEL

ART UNIT

PAPER NUMBER

2186

DATE MAILED: 05/11/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	NL040529US1	4172

TITLE OF INVENTION: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	08/11/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/569,083	11/14/2006	Andrei Radulescu	NL040529US1	4172
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TITLE OF INVENTION: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	08/11/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
ALSIP, MICHAEL	2186	711-118000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____ (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE _____ (B) RESIDENCE: (CITY and STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted: ☐ Issue Fee ☐ Publication Fee (No small entity discount permitted) ☐ Advance Order - # of Copies _____	4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above) ☐ A check is enclosed. ☐ Payment by credit card. Form PTO-2038 is attached. ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).
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5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____
 Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	NL040529US1	4172

24737 7590 05/11/2011
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
ALSIP, MICHAEL	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/11/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 527 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 527 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DETAILED ACTION

Allowable Subject Matter

1. **Claims 1, 3-4 and 7-24** are allowed.
2. The following is an examiner's statement of reasons for allowance: The Applicant has incorporated the subject matter of now cancelled **claim 6**, previously indicated as allowable in the final office action dated 2/24/2011, into each independent claim and therefore the case is now in condition for allowance. As stated in the previous office action, the claim language of now cancelled claim 6, describes a process/function of determining an optimal moment for sending data in said first or second wrapper according to: "communication properties of the communication between the master and slave" and then further claims that "the communication properties" include the claimed extensive list of properties. The prior art found alone or in combination does not teach or suggest that the communication properties of the communication between the master and slave used to determine the optimal moment for sending data, incorporate the claimed list of communication properties to make that determination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-

1182. The examiner can normally be reached on Monday through Thursday 9:00AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael Alsip
Examiner
Art Unit 2186

/Michael Alsip/
Examiner, Art Unit 2186

May 5, 2011

**RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2186**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket: NL040529US1

Andrei RADULESCU, et al.

Confirmation No. 4172

Serial No. 11/569,083

Group Art Unit: 2186

Filed: November 14, 2006

Examiner: ALSIP, Michael

Title: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE
BURST LENGTH IN NETWORKS ON CHIPS

Mail Stop AF
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER §1.116

Sir:

In response to the Final Office Action mailed on February 24, 2011, please amend
the above-identified application and consider the remarks as follows:

OK TO ENTER: /M.A./

<i>Search Notes</i> 	Application/Control No. 11569083	Applicant(s)/Patent Under Reexamination RADULESCU ET AL.
	Examiner MICHAEL ALSIP	Art Unit 2186

SEARCHED			
Class	Subclass	Date	Examiner
711	118 limited w/ text	5/5/2011	MA
711	141 limited w/ text	5/5/2011	MA
710	57 limited w/ text	5/5/2011	MA
710	100 limited w/ text	5/5/2011	MA

SEARCH NOTES		
Search Notes	Date	Examiner
inventor name and assignee search in eDAN and EAST	5/5/2011	MA
class/subclass and keyword search in EAST	5/5/2011	MA
internet search using same keywords as in the EAST search	5/5/2011	MA

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	see attached EAST interference search	5/5/2011	MA

/MICHAEL ALSIP/ Examiner.Art Unit 2186	
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Issue Classification 	Application/Control No. 11569083	Applicant(s)/Patent Under Reexamination RADULESCU ET AL.
	Examiner MICHAEL ALSIP	Art Unit 2186

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
711		118				G	0	6	F	12 / 00 (2006.0)								
CROSS REFERENCE(S)						G	0	6	F	13 / 00 (2006.0)								
						G	0	6	F	13 / 28 (2006.0)								
						G	0	6	F	3 / 00 (2006.0)								
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					G	0	6	F	5 / 00 (2006.0)								
711	141																	
710	57	100																

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	14	17												
	2	15	18												
2	3	16	19												
3	4	17	20												
	5	18	21												
	6	19	22												
4	7	20	23												
5	8	21	24												
6	9														
7	10														
8	11														
9	12														
10	13														
11	14														
12	15														
13	16														

		Total Claims Allowed:	
		21	
(Assistant Examiner) /MICHAEL ALSIP/ Examiner, Art Unit 2186	(Date) 05/06/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L2	771	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L3	392	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L4	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L5	74	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L6	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L7	45	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L8	2065	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L9	319	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L10	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L11	17	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L12	334	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L13	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L14	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L15	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L16	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02

L17	109	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L18	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L19	201	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L20	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L21	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L22	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L23	365	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L24	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L25	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L26	180	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L27	13	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L28	305	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L29	19	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L30	16	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L31	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L32	65	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L33	19	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L34	18758	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L35	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L36	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L37	771	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L38	392	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L39	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L40	74	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L41	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L42	45	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L43	2065	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L44	319	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L45	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L46	17	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L47	334	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L48	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L49	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L50	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L51	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L52	109	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L53	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L54	201	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L55	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L56	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L57	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L58	365	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L59	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L60	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L61	180	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L62	13	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L63	305	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L64	19	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L65	16	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L66	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L67	65	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L68	19	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L69	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L70	771	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L71	392	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L72	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L73	74	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L74	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L75	45	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L76	2065	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L77	319	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L78	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L79	17	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L80	334	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L81	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L82	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L83	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L84	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L85	109	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L86	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L87	201	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L88	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L89	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L90	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L91	365	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L92	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L93	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L94	180	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L95	13	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L96	305	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L97	19	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L98	16	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L99	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L100	65	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L101	19	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L102	18758	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L103	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L104	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L105	771	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L106	392	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L107	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L108	74	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L109	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L110	45	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L111	2065	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L112	319	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L113	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L114	17	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L115	334	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L116	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L117	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L118	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L119	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L120	109	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L121	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L122	201	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L123	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L124	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L125	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L126	365	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L127	12	"711".cls.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L128	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L129	180	"711/118".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L130	13	"711/118".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L131	305	"711/141".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L132	19	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L133	16	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L134	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L135	65	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L136	19	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L137	392	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L138	45	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L139	180	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L140	19	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L141	16	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L142	16	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L143	65	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L144	65	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L145	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L146	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L147	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L148	17	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L149	5	US-6493776-\$.DID. OR US-6397287-\$.DID. OR US-6393500-\$.DID. OR US-5987552-\$.DID. OR US-6629253-\$.DID.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L150	2	"20030101307".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L151	5	"2005026964".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L152	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L153	771	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L154	392	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L155	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L156	74	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L157	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L158	45	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L159	2065	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L160	319	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L161	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L162	17	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L163	334	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L164	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L165	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L166	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L167	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L168	109	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L169	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L170	201	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L171	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L172	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L173	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L174	365	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L175	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L176	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L177	180	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L178	13	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L179	305	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L180	19	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L181	16	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L182	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L183	65	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L184	19	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L185	18758	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L186	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L187	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L188	771	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L189	392	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L190	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L191	74	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L192	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L193	45	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L194	2065	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L195	319	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L196	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L197	17	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L198	334	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L199	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L200	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L201	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L202	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L203	109	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L204	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L205	201	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L206	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L207	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L208	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L209	365	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L210	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L211	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L212	180	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L213	13	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L214	305	"711/141".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L215	19	"711/141".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L216	16	"710/57".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L217	2	"710/57".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L218	65	"710/100".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L219	19	"710/100".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L220	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L221	771	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L222	392	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L223	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L224	74	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L225	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L226	45	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L227	2065	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L228	319	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L229	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L230	17	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L231	334	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L232	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L233	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L234	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L235	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L236	109	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L237	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L238	201	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L239	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L240	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L241	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L242	365	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L243	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L244	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L245	180	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L246	13	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L247	305	"711/141".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L248	19	"711/141".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L249	16	"710/57".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L250	2	"710/57".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L251	65	"710/100".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L252	19	"710/100".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L253	18758	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L254	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L255	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L256	771	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L257	392	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L258	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L259	74	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L260	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L261	45	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L262	2065	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L263	319	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L264	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L265	17	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L266	334	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L267	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L268	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L269	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L270	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L271	109	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L272	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L273	201	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L274	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L275	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L276	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L277	365	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L278	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L279	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L280	180	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L281	13	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L282	305	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L283	19	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L284	16	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L285	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L286	65	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L287	19	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L288	392	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L289	45	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L290	180	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L291	19	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L292	16	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L293	16	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L294	65	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L295	65	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L296	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L297	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L298	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L299	17	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L300	5	US-6493776-\$.DID. OR US-6397287-\$.DID. OR US-6393500-\$.DID. OR US-5987552-\$.DID. OR US-6629253-\$.DID.	US-PGPUB; USPAT; USOCR	AND	ON	2011/05/05 14:02
L301	2	"20030101307".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L302	5	"2005026964".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L303	1561	(packet adj size) near3 (adapt\$4 or adjust\$4 or variab\$4 or varying or varies)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02

L304	71	"711".clas. (packet adj size) near3 (adapt\$4 or adjust\$4 or variab\$4 or varying or varies)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L305	924	(packet adj size) near (adapt\$4 or adjust\$4 or variab\$4 or varying or varies)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L306	611	(packet adj size) near (adapt\$4 or adjust\$4 or variab\$4 or varying or varies) processors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
L307	3	(packet adj size) near (adapt\$4 or adjust\$4 or variab\$4 or varying or varies) communication near properties	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/05/05 14:02
S1	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 12:45
S2	700	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:48
S3	356	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:50
S4	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:58

S5	52	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 13:59
S6	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:04
S7	42	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:20
S8	1640	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S9	286	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:25
S10	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:26
S11	11	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28
S12	298	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:28

S13	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:29
S14	39	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:35
S15	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:36
S16	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/06/30 14:39
S17	104	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S18	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/06/30 14:44
S19	182	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S20	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16
S21	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:16

S22	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:17
S23	325	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:19
S24	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/01 12:20
S25	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 11:31
S26	145	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S27	10	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S28	245	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04
S29	13	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:04

S30	13	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S31	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S32	58	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S33	16	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/07/02 13:05
S35	15075	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
S36	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:23
S37	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S38	723	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S39	368	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S40	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S41	61	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S42	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S43	43	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S44	1746	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S45	298	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S46	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S47	13	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S48	310	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S49	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S50	45	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S51	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
S52	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2009/12/09 15:24
S53	104	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S54	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S55	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S56	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S57	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S58	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S59	340	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S60	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S61	2	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S62	151	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S63	11	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24

S64	256	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S65	16	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S66	13	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S67	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S68	58	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S69	16	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2009/12/09 15:24
S70	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S71	737	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S72	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S73	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S74	63	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S75	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S76	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S77	1794	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S78	299	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S79	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S80	13	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S81	312	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S82	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S83	45	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S84	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S85	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S86	105	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S87	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S88	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S89	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S90	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S91	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S92	344	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S93	12	"711".cls.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S94	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S95	154	"711/118".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S96	11	"711/118".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S97	264	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S98	16	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S99	13	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S100	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S101	60	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S102	17	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S103	15892	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S104	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S105	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S106	737	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S107	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S108	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S109	63	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S110	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S111	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S112	1794	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S113	299	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S114	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S115	13	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S116	312	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S117	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S118	45	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S119	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S120	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/03/16 13:59
S121	105	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S122	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S123	194	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S124	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S125	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S126	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S127	344	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S128	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S129	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S130	154	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S131	11	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S132	264	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S133	16	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S134	13	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S135	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S136	60	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59
S137	17	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/03/16 13:59

S138	377	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S139	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S140	160	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S141	16	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S142	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S143	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S144	61	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S145	61	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10

S146	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:10
S147	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:11
S148	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:11
S149	13	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:12
S150	5	US-6493776-\$.DID. OR US-6397287-\$.DID. OR US-6393500-\$.DID. OR US-5987552-\$.DID. OR US-6629253-\$.DID.	US-PGPUB; USPAT; USOCR	AND	ON	2010/07/12 14:13
S151	2	"20030101307".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:14
S152	5	"2005026964".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/07/12 14:14
S153	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42

S154	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S155	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S156	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S157	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S158	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S159	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S160	1930	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S161	312	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42

S162	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S163	16	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S164	327	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:42
S165	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S166	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S167	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S168	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S169	106	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S170	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S171	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S172	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S173	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S174	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S175	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S176	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S177	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S178	168	"711/118".cls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S179	12	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S180	290	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S181	18	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S182	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S183	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S184	64	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S185	18	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S186	17427	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S187	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S188	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S189	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S190	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S191	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S192	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S193	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S194	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S195	1930	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S196	312	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S197	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S198	16	"711".clas. (multi \$processor) ((request near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S199	327	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S200	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S201	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S202	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S203	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43

S204	106	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S205	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S206	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S207	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S208	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S209	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S210	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S211	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S212	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S213	168	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S214	12	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S215	290	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S216	18	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S217	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S218	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S219	64	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S220	18	"710/100".cls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S221	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S222	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S223	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S224	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S225	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S226	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S227	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S228	1930	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S229	312	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S230	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S231	16	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S232	327	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S233	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S234	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S235	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S236	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43

S237	106	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S238	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S239	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S240	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S241	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S242	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S243	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S244	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S245	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S246	168	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S247	12	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S248	290	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S249	18	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S250	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S251	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S252	64	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S253	18	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S254	17427	(koninklijke philips electronics).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S255	1	(koninklijke philips electronics).as. burst flush module buffer\$3 wrapper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S256	2	"6397287".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S257	753	"711".clas. master slave buffer flag signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S258	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S259	1	"711".clas. master slave buffer unbuffer (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S260	68	"711".clas. master slave buffer (noc or soc) (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S261	4	"711".clas. ((master slave) near processor) buffer (noc or soc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S262	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S263	1930	"711".clas. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S264	312	"711".clas. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S265	2	"711".clas. (multi \$processor) ((request receive) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S266	16	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S267	327	"711".clas. (multi \$processor) (queue or buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S268	8	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S269	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S270	2	("20040039880" "20050160235").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S271	10	("20010047439" "20030070059" "4831517" "5388074" "5706491" "5819254" "6078983" "6269436" "6532531" "6640231").PN.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43
S272	106	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S273	1	"711".clas. (multi \$processor) (integrated near circuit) (queue or buffer) interprocessor near shar\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S274	198	multiprocessor near integrated near circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S275	0	(multiprocessor near integrated near circuit) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S276	2	(multiprocessor near integrated near circuit) with (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S277	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S278	354	(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S279	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S280	3	"4378588".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S281	168	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S282	12	"711/118".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S283	290	"711/141".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S284	18	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S285	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S286	2	"710/57".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S287	64	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S288	18	"710/100".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S289	381	"711".clas. master slave buffer flag signal (integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S290	44	"711".clas. ((master slave) near processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S291	168	"711/118".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S292	18	"711/141".ccls. (multi \$processor) (buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S293	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43

S294	14	"710/57".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S295	64	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S296	64	"710/100".ccls. (multi \$processor) buffer (integrated near circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S297	12	"711".clas.(cmp or sop) near (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S298	5	(multiprocessor near integrated near circuit) same (benefits or advantages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S299	46	"711".clas. (multi \$processor) near (integrated near circuit) (queue or buffer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S300	16	"711".clas. (multi \$processor) ((request) near buffer) (integrated near circuit) (master slave)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S301	5	US-6493776-\$.DID. OR US-6397287-\$.DID. OR US-6393500-\$.DID. OR US-5987552-\$.DID. OR US-6629253-\$.DID.	US-PGPUB; USPAT; USOCR	AND	ON	2010/10/20 14:43

S302	2	"20030101307".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S303	5	"2005026964".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2010/10/20 14:43
S304	1522	(packet adj size) near3 (adapt\$4 or adjust\$4 or variab\$4 or varying or varies)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/02/17 14:13
S305	70	"711".clas. (packet adj size) near3 (adapt\$4 or adjust\$4 or variab\$4 or varying or varies)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/02/17 14:13
S306	902	(packet adj size) near (adapt\$4 or adjust\$4 or variab\$4 or varying or varies)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/02/17 14:22
S307	593	(packet adj size) near (adapt\$4 or adjust\$4 or variab\$4 or varying or varies) processors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/02/17 14:23
S308	3	(packet adj size) near (adapt\$4 or adjust\$4 or variab\$4 or varying or varies) communication near properties	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/02/17 14:23

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L308	6114	wrapper.clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:10
L309	12	wrapper.clm. (master slave).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:11

L310	3	wrapper.clm. (master slave).clm. flow.clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:11
L311	0	wrapper.clm. (master slave).clm. flow.clm. throughput.clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:11
L312	6	(master slave).clm. flow.clm. throughput.clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:11
L313	1	(master slave).clm. flow.clm. throughput.clm. latency.clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:11
L314	0	(master slave).clm. flow.clm. throughput.clm. latency.clm. lossiness.clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:12
L315	2	flow.clm. throughput.clm. latency.clm. lossiness.clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:12
L316	1	flow.clm. throughput.clm. latency.clm. lossiness.clm. priority.clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:12
L317	2	module.clm. interconnect.clm. buffer \$3.clm. amount.clm. wrapper.clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:18
L318	2	module.clm. interconnect.clm. buffer \$3.clm. amount.clm. master.clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/05/05 14:20

5/ 5/ 2011 2:20:33 PM

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Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL **(Submitted Only via EFS-Web)**

Application Number	11569083	Filing Date	2006-11-14	Docket Number (if applicable)	2004P01041WOUS	Art Unit	2186
First Named Inventor	Andrei Radulescu			Examiner Name	Michael Alsip		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☐ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No. 141270

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

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Signature of Registered U.S. Patent Practitioner			
Signature	/Michael E. Belk/	Date (YYYY-MM-DD)	2011-08-04
Name	Michael E. Belk	Registration Number	33357

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11569083	
	Filing Date		2006-11-14	
	First Named Inventor	Andrei Radulescu		
	Art Unit	2186		
	Examiner Name	Michael Alsip		
	Attorney Docket Number	2004P01041WOUS		

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	3	2002084289	JP	A	2002-03-22	HASEGAWA ET AL		☐

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	Filing Date		2006-11-14	
	First Named Inventor	Andrei Radulescu		
	Art Unit	2186		
	Examiner Name	Michael Alsip		
	Attorney Docket Number	2004P01041WOUS		

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	11569083
Filing Date	2006-11-14
First Named Inventor	Andrei Radulescu
Art Unit	2186
Examiner Name	Michael Alsip
Attorney Docket Number	2004P01041WOUS

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

- ☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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- ☐ See attached certification statement.
- ☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.
- ☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Michael E. Belk/	Date (YYYY-MM-DD)	2011-08-04
Name/Print	Michael E. Belk	Registration Number	33,357

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

FRAME TRANSMISSION CIRCUIT

Publication number: JP7123118 (A)

Publication date: 1995-05-12

Inventor(s): GOTO JUNICHI +

Applicant(s): FUJI XEROX CO LTD +

Classification:

- international: **H04L12/40; H04L13/08; H04L29/02; H04L12/40; H04L13/08; H04L29/02;** (IPC1-7): H04L12/40; H04L13/08; H04L29/02

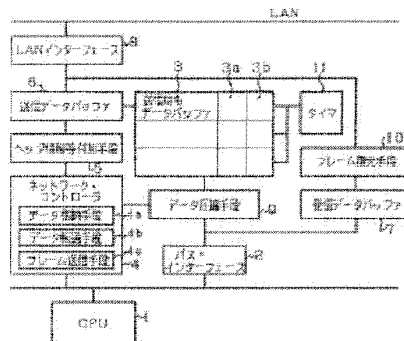
- European:

Application number: JP19930285807 19931021

Priority number(s): JP19930285807 19931021

Abstract of JP 7123118 (A)

PURPOSE: To improve the transmission efficiency of the whole of a system by reducing the number of frames sent to LAN. **CONSTITUTION:** A transmission queue data buffer 3 has plural individual buffers which have the capacity corresponding to the length of the data area of a maximum frame allowed on LAN. Until individual buffers are full, packets whose transmission is requested by a CPU 1 are compressed, multiplexed, and stored there by transmission destinations. When individual buffers are filled up with data in the middle of data storage, compressed and multiplexed data stored in individual buffers before is transferred to a transmission data buffer 6. The transmission destination address, the transmission source address, the frame type, and the frame check sequence are added before and after data transferred to the transmission data buffer 6 by a header information adding means 5 to form a frame, and it is transmitted to LAN by a frame transmission means.



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(19)日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11)特許出願公開番号

特開平7-123118

(43)公開日 平成7年(1995)5月12日

(51)Int.Cl. ⁸	識別記号	庁内整理番号	F I	技術表示箇所
H 0 4 L 13/08 12/40 29/02		9371-5K		
		7341-5K	H 0 4 L 11/ 00	3 2 0
		9371-5K	13/ 00	3 0 1 Z
			審査請求 未請求	請求項の数 2 F D (全 9 頁)

(21)出願番号 特願平5-285807

(22)出願日 平成5年(1993)10月21日

(71)出願人 000005496

富士ゼロックス株式会社

東京都港区赤坂三丁目3番5号

(72)発明者 後藤 淳一

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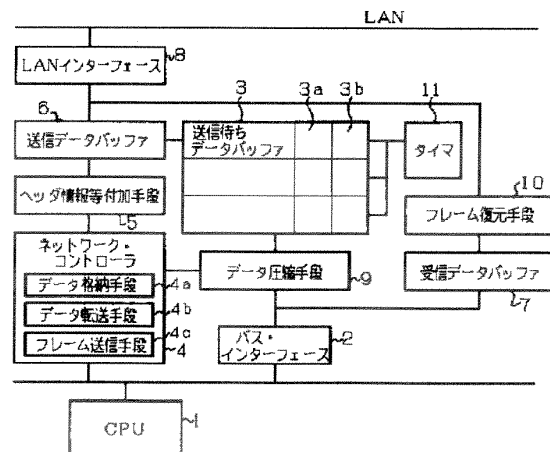
(74)代理人 弁理士 本庄 富雄

(54)【発明の名称】 フレーム送信回路

(57)【要約】

【目的】 LAN上へ送出するフレーム数を減少させることにより、全体の伝送効率を向上させること。

【構成】 送信待ちデータバッファ3は、LAN上で許容される最大フレームのデータ領域の長さに相当する容量の複数の個別バッファを持っている。それらの個別バッファには、それが満杯になるまで、CPU1から送信要求のあったパケットを送信先別に圧縮・多重化して格納する。データ格納中に個別バッファが満杯になったときは、それ以前に該個別バッファに格納されていた圧縮・多重化データを送信データバッファ6へ転送する。そして、送信データバッファ6へ転送されたデータの前後に、ヘッダ情報付加手段5により、送信先アドレス、発信元アドレス、フレーム・タイプ及びフレーム・チェック・シーケンスを付加してフレームを形成した後、フレーム送信手段によりLANに送信する。



【特許請求の範囲】

【請求項1】 LAN上で許容される最大フレームを格納可能な容量を有する送信データバッファと、LAN上で許容される最大フレームのデータ領域のサイズと等しい容量を有する複数の送信待ちデータバッファと、送信要求のあったデータを送信先別に前記送信待ちデータバッファに順次格納するデータ格納手段と、データの格納中に前記送信待ちデータバッファが満杯になったとき、該データの格納以前に該送信待ちデータバッファに格納されていたデータを前記送信データバッファへ転送するデータ転送手段と、前記送信データバッファへ転送されたデータに送信先アドレス、発信元アドレス、フレーム・タイプ及びフレーム・チェック・シーケンスを付加してフレームを形成するヘッダ情報等付加手段と、前記送信データバッファ中で形成されたフレームをLANに送信するフレーム送信手段とを具えたことを特徴とするフレーム送信回路。

【請求項2】 前記送信待ちデータバッファに格納するデータを圧縮するデータ圧縮手段を具えたことを特徴とする請求項1記載のフレーム送信回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、計算機からLAN（ローカル・エリア・ネットワーク）に対してフレームを送信するフレーム送信回路に関するものである。

【0002】

【従来の技術】LANでは、通信の最小単位をフレームと呼び、それによって物理的なメディア・アクセスを管理している。LAN上の計算機からLANに対してデータを送信する場合は、計算機中のフレーム送信回路でフレームを組み立ててからLANに送出する。

【0003】図8は、従来のフレーム送信回路の一例を示すブロック図である。図8において、1はCPU（中央処理装置）、2はバス・インターフェース、3は送信待ちデータバッファ、4はネットワーク・コントローラ、5はヘッダ情報等付加手段、6は送信データバッファ、7は受信データバッファ、8はLANインターフェースである。

【0004】CPU1がLAN上の端末に対してデータを送信する場合、バス・インターフェース2を介して、一旦、送信待ちデータバッファ3に送信データを送って保持させ、その後、それを送信データバッファ6に転送する。一方、CPU1は、ネットワーク・コントローラ4を介して送信先アドレス、フレームタイプをヘッダ情報等付加手段5に送る。そして、それらを受け取ったヘッダ情報等付加手段5は、送信データバッファ6中の送信データの前後に、送信先アドレス、発信元アドレス、フレームタイプ及びフレーム・チェック・シーケンスを

付加して、フレームを形成する。その後、フレームをLANインターフェース8を介してLANに送出する。従来のフレーム送信回路では、このようにして、CPU1から送信要求のあったデータを、要求毎に1つのフレームを形成してLANに送出するようにしていた。

【0005】なお、フレーム送信回路に関連する従来の文献としては、例えば、特開平4-207336号公報がある。

【0006】

【発明が解決しようとする課題】（問題点）しかしながら、前記従来の技術には、LAN上でのデータの全体的な伝送効率が低くなってしまいう問題点があった。

【0007】（問題点の説明）LANの規格上、1個のフレームで送信できるデータ量には上限があり、各フレーム毎にその上限までデータを送ることができるが、従来のフレーム送信回路では、1個のフレームの送信データ量がその上限値に比してごく少量であっても、CPU1からの送信要求毎に1個のフレームを形成してLANに送出するようにしていた。そのため、全体的に送信するフレームの数が増えて、フレーム自体に含まれるヘッダ情報等、本来送信すべきデータ以外の情報が多くなったり、フレームを送出するためのオーバーヘッド分が多くなったりして、全体的な伝送効率が低くなる結果となっていた。本発明は、そのような問題点を解決することを課題とするものである。

【0008】

【課題を解決するための手段】前記課題を解決するため、本発明のフレーム送信回路では、LAN上で許容される最大フレームを格納可能な容量を有する送信データバッファと、LAN上で許容される最大フレームのデータ領域のサイズと等しい容量を有する複数の送信待ちデータバッファと、送信要求のあったデータを送信先別に前記送信待ちデータバッファに順次格納するデータ格納手段と、データの格納中に前記送信待ちデータバッファが満杯になったとき、該データの格納以前に該送信待ちデータバッファに格納されていたデータを前記送信データバッファへ転送するデータ転送手段と、前記送信データバッファへ転送されたデータに送信先アドレス、発信元アドレス、フレーム・タイプ及びフレーム・チェック・シーケンスを付加してフレームを形成するヘッダ情報等付加手段と、前記送信データバッファ中で形成されたフレームをLANに送信するフレーム送信手段とを具えることとした。また、上記フレーム送信回路において、前記送信待ちデータバッファに格納するデータを圧縮するデータ圧縮手段を具えることとした。

【0009】

【作 用】データの送信要求があったとき、データ格納手段により、送信要求のあったデータを送信先別に送信待ちデータバッファに順次格納する。データの格納中に送信待ちデータバッファが満杯になったときは、該デ

ータの格納以前に該送信待ちデータバッファに格納されていたデータを、データ転送手段により前記送信データバッファへ転送する。ヘッダ情報等付加手段は、送信データバッファへ転送されたデータに、送信先アドレス、発信元アドレス、フレーム・タイプ及びフレーム・チェック・シーケンスを付加してフレームを形成する。そして、フレーム送信手段により、該フレームをLANに送信する。そのようにして、送信要求のあったデータは、各送信待ちデータバッファ内で送信先別に多重化され、それを送信データバッファに転送して1つのフレームにしてLANに送信するため、LAN上へ送出するフレーム数を減少させることができる。そのため、フレーム自体に含まれる本来送信すべきデータ以外の情報や、フレーム送出のためのオーバーヘッド分を減少させ、全体の伝送効率を向上させることができる。また、送信要求のあったデータを、データ圧縮手段により圧縮してから前記送信待ちデータバッファに格納する。そのため、1フレーム当たりにも多重化するデータ数を増やすことができる上、LAN上を流れるデータの冗長度を減らし、1フレーム当たりの伝送できる総データ量を増加させ、さらに伝送効率を向上させることができる。

【0010】

【実施例】以下、本発明の実施例を図面に基いて詳細に説明する。図1は、本発明の一実施例を示すブロック図である。符号は、図8のものに対応し、3aはアドレス・レジスタ、3bはタイム・レジスタ、4aはデータ格納手段、4bはデータ転送手段、4cはフレーム送信手段、9はデータ圧縮手段、10はフレーム復元手段、11はタイマである。

【0011】本発明における送信待ちデータバッファ3は複数設けられ、各送信待ちデータバッファ3は、LAN上で許容される最大フレームのデータ領域のサイズと等しい容量（例えば、1500バイト）を有するリング・バッファより成る。また、この実施例では、データ圧縮手段9を設け、例えば、ランレングス方式のような、可逆符号化方式で、かつ辞書の送信を必要としない圧縮方式により、CPU1から送信要求のあったデータを逐次圧縮してから送信待ちデータバッファ3に格納するようにしている。そしてまた、上記各送信待ちデータバッファ3には、それぞれに対応して、送信先アドレスを保持するアドレス・レジスタ3aと、現在送信待ちデータバッファ3に格納されているデータの内の最先のデータを格納した時刻をタイマ11から取得して保持するタイム・レジスタ3bとを具えている。

【0012】CPU1から送信要求のあったデータは、ネットワーク・コントローラ4のデータ格納手段4aにより、送信先別に振り分けられて、送信待ちデータバッファ3に格納され、該当する送信待ちデータバッファ3にデータを格納しようとしたとき、既に該送信先の前のデータが格納されている場合には、その後に順次追加す

る形で多重化して格納する。また、送信待ちデータバッファ3のデータは、ネットワーク・コントローラ4のデータ転送手段4bにより送信データバッファ6に転送した後、フレーム送信手段4cによりLANへ送信する。

【0013】一方、フレーム復元手段10は、受信したフレームより送信先アドレス、フレーム・チェック・シーケンス等を取り出して、自局宛のものかどうか、不正なフレームかどうかなどの判定を行った後、取り込むべきものと判断されたフレームのデータについて、データ伸長と多重化の解除を行う。

【0014】次に、送信データバッファ6からLANに送信するフレームのフレーム構成について説明する。図2は、LANに送信するフレームのフレーム構成を示す図である。このフレームは、データリンク層におけるフレームであり、圧縮、多重化データを非圧縮の送信先アドレス、発信元アドレス、フレームタイプ及びフレーム・チェック・シーケンスで挟んだ構成になっている。また、上記圧縮、多重化データには、データリンク層の上位層であるネットワーク層でのヘッダ、送信先アドレス、発信元アドレス及びデータを持った1つ以上のネットワーク層パケットが圧縮、多重化された形で収容されている。このようなフレームを受信した側では、圧縮、多重化データを伸長すると、ネットワーク層パケットのヘッダ領域には、ヘッダ領域からデータまでのバイト長が保持されているので、パケットがいくつか連なった状態で受信データバッファに格納されても、それを個々のパケットに分割して処理することが可能である。

【0015】次に、本発明の基本的な動作をフローチャートを使って説明する。図3は、本発明によるパケット送信処理手順の一例を示すフローチャートである。

ステップ1…CPU1は、送信先アドレス、送信データ量をネットワーク・コントローラ4のデータ格納手段4aに通知する。

ステップ2…データ格納手段4aは、通知された送信先アドレスと、各送信待ちデータバッファ3に対応するアドレス・レジスタ3aに格納されているアドレスとを比較する。

ステップ3…同一のアドレスがあったか否かを判別する。

ステップ4…あったら、CPU1よりの送信データをデータ圧縮手段9で圧縮した後、アドレス・レジスタ3aのアドレスが同一であった送信待ちデータバッファ3に格納する。

【0016】ステップ5…データを格納中のバッファが満杯になったか否かを判別する。

ステップ6…満杯になったら、データの格納を中断し、該データの格納を開始する以前に当該送信待ちデータバッファ3に格納されていたデータを、データ転送手段4bにより送信データバッファ6に転送した後、フレーム送信手段4cによりLANへの送信を行う。

ステップ7…中断していたデータの格納をバッファの先頭より再開する。

ステップ8…該データの格納が終了した時のタイマ11の値をタイム・レジスタ3bに書込む。

【0017】ステップ9…ステップ3で同一のアドレスがなかったら、空いている送信待ちデータバッファ3に対応するアドレス・レジスタ3aに送信先アドレスを書込む。

ステップ10…CPU1よりの送信データをデータ圧縮手段9で圧縮した後、上記の空いている送信待ちデータバッファ3に格納する。

ステップ11…データを格納中の送信待ちデータバッファ3が満杯になったか否かを判別する。

ステップ12…満杯になったら、データの格納を中断し、該データの格納を開始する以前に当該送信待ちデータバッファ3に格納されていたデータを、データ転送手段4bにより送信データバッファ6に転送した後、フレーム送信手段4cによりLANへの送信を行う。

ステップ13…中断していたデータの格納をバッファの先頭より再開する。

ステップ14…該データの格納が終了した時のタイマ11の値をタイム・レジスタ3bに書込む。

【0018】図4は、送信待ちデータバッファのタイマアウト監視処理を示すフローチャートである。この処理は、タイマ11の値がインクリメントされる度毎に実行される。

ステップ1…送信待ちデータバッファ3の内の1つを指定するための変数Nに1を代入し、変数Mにタイマ11の現在の値を代入する。

ステップ2…N番目の送信待ちデータバッファ3に対応するタイム・レジスタに書き込まれている値をTR

(N)で表すとき、変数KにM-TR(N)を代入する。すなわち、Kの値は、当該タイム・レジスタに書き込まれている値の書き込み後の経過時間に対応する。

ステップ3…Kが所定値Th以上になったか否かを判別する。

ステップ4…なったとき、当該送信待ちデータバッファ3内に格納されているデータを、データ転送手段4bにより送信データバッファ6に転送した後、フレーム送信手段4cによりLANへの送信を行う。

ステップ5…当該送信待ちデータバッファ3に対応するアドレス・レジスタ3aの値AR(N)及びタイム・レジスタ3bの値TR(N)をクリアする。

ステップ6…変数Nに1を加える。

ステップ7…変数Nが送信待ちデータバッファ3の送信待ちデータバッファ3の数を超えたか否かを判別する。

【0019】次に、他の計算機からフレームを受信した場合の処理手順を示すフローチャートである。

ステップ1…受信を開始する。

ステップ2…受信フレームより送信先アドレスを取得する。

ステップ3…取得したアドレスが自局のアドレスと一致しているか否かを判別する。

ステップ4…一致していれば、受信フレームより発信元アドレスとフレームタイプを取り出してネットワーク・コントローラ4内に保持する。

【0020】ステップ5…受信フレームより、圧縮、多重化されたデータ部分を取り出してフレーム復元手段10で伸長した後、受信データバッファ7の現在の先頭番地より、発信元アドレス、フレームタイプ及びデータ長を格納するための領域をあけた後から格納する。その際、格納を行いながら格納済のバイト数をカウントし、格納終了後にカウント結果をネットワーク・コントローラ4内に保持する。

ステップ6…ステップ4、5でネットワーク・コントローラ4内に保持しておいた発信元アドレス、フレームタイプ及びバイト数を、受信データバッファ7の上記領域に格納する。

20 ステップ7…受信データバッファ7の現在の先頭番地を示すポインタを格納した受信データの末端の番地の次の番地に移動させる。

ステップ8…ステップ3で自局のアドレスと一致しなかったとき、受信動作を中断する。

【0021】次に、CPU1から図7に示すようなパケット送信要求があった場合を例にして、本実施例の動作を具体的に説明する。図7のP₁～P₁₀は、送信要求のあったパケットを示し、その上段は送信先アドレスを示し、下段はデータ長をバイト数で示している。このようなパケット送信要求があった場合、送信待ちデータバッファ3には、以下のようにデータが格納されていく。なお、図7下の「LANへの送信」の欄は、フレーム送信回路からLANへ送信されるフレームの送信先アドレス及び送信のタイミングを示している。

【0022】図6は、送信待ちデータバッファの状態を示す図である。まず、図7にP₁で示す、アドレス“000010”へ46バイトのパケット送信要求があったとき、どの送信待ちデータバッファ3も空であるので、図6

40 (イ)に示すように、新たに1つの送信待ちデータバッファ3が割り当てられ、データ圧縮手段9で圧縮したデータp₁が、その先頭から格納される。そして、該送信待ちデータバッファ3に対応するアドレス・レジスタ3aにアドレス“000010”が書き込まれ、タイム・レジスタ3bにその時のタイマ11の値“20”が書き込まれる。なお、アドレス及びタイマ11の値は、全て16進表示で表示している。

【0023】次に、図7にP₂で示す、アドレス“000022”へ46バイトのパケット送信要求があったとき、送信待ちデータバッファ3はまだ2つ空いているので、図6

50 (ロ)に示すように、新たに送信待ちデータバッファ3

が割り当てられ、データ圧縮手段 9 で圧縮したデータ p_2 が、その先頭から格納される。そして、該送信待ちデータバッファ 3 に対応するアドレス・レジスタ 3 a にアドレス "000022" が書き込まれ、タイム・レジスタ 3 b にその時のタイム 11 の値 "2 A" が書き込まれる。

【0024】次に、図 7 に P_3 で示す、アドレス "000102" へ 120 バイトのパケット送信要求があったとき、図 6 (ハ) に示すように、アドレス "000102" は新規であるため新たに送信待ちデータバッファ 3 が割り当てられ、圧縮されたデータ p_3 がその先頭から格納される。それ 10 に続いて、図 7 に P_4 、 P_5 で示す、アドレス "000010" へ 800 バイト及び 1000 バイトのパケット送信要求があったとき、アドレス "000010" は既に送信待ちデータバッファ 3 が割り当てられているため、データ p_1 の後にパケット P_4 、 P_5 の圧縮データ p_4 、 p_5 が多重化される。その際、パケット P_1 、 P_4 、 P_5 の合計バイト数は 1846 バイトになるが、送信待ちデータバッファ 3 に格納する前に圧縮しているので、バッファはまだ満杯にはならない。また、この時、アドレス "000010" に 20 割り当てられている送信待ちデータバッファ 3 に対応するタイム・レジスタ 3 b は書き換ええない。

【0025】次に、図 7 に P_6 で示す、アドレス "002004" へ 1000 バイトのパケット送信要求があったとき、既に送信待ちデータバッファ 3 は全て割り当て済であるので、そのままでは送信待ちデータバッファ 3 に格納できない。そこで、図 6 (ニ) に示すように、最もタイム・レジスタ 3 b の値が古いアドレス "000010" へのデータが送信データバッファ 6 に移され、それによって空いた 30 バッファにパケット P_6 の圧縮データ p_6 が格納される。また、その時、アドレス・レジスタ 3 a、タイム・レジスタ 3 b の値も更新される。

【0026】次に、図 7 に P_7 、 P_8 で示す、アドレス "000022" へ 1000 バイト及び 150 バイトのパケット送信要求があったとき、このアドレス "000022" は既に送信待ちデータバッファ 3 が割り当てられているため、図 6 (ホ) に示すように、データ p_2 の後にパケット P_7 、 P_8 の圧縮データ p_7 、 p_8 が多重化される。また、この時、アドレス "000022" に割り当てられている送信待ちデータバッファ 3 に対応するタイム・レジスタ 3 b は書き換ええない。

【0027】次に、図 7 に P_9 で示す、アドレス "000022" へ 600 バイトのパケット送信要求があったとき、このアドレス "000022" は既に送信待ちデータバッファ 3 が割り当てられているため、パケット P_9 の圧縮データ p_9 は、データ p_8 の後に格納されていくが、その最中に 40 バッファ容量限界である 1500 バイトに達してしまう。そのため、以前に蓄積されたデータ p_2 、 p_7 、 p_8 を一旦送信データバッファ 6 に転送した後、残りのデータの格納を該送信待ちデータバッファ 3 の先頭より再開する。その場合、アドレス "000022" 用の送信待ちデー

タバッファ 3 の先頭を示すポインタは、図 6 (ヘ) の A で示す位置となる。また、タイム・レジスタ 3 b は、データ p_9 を格納後、タイム 11 の現在値 "70" に更新される。

【0028】ここで、次の送信要求がくる前に、ネットワーク・コントローラ 4 が、アドレス "000102" に割り当てられている送信待ちデータバッファ 3 に格納されているデータがタイムアウトに達していることを発見したものとする。その時、ネットワーク・コントローラ 4 は、データ転送手段 4 b により、図 6 (ト) に示すように、アドレス "000102" に割り当てられている送信待ちデータ 50 バッファ 3 に格納されているデータを送信データバッファ 6 に転送すると共に、アドレス・レジスタ 3 a 及びタイム・レジスタ 3 b をクリアする。

【0029】次に、図 7 に P_{10} で示す、アドレス "000022" へ 46 バイトのパケット送信要求があったとき、このアドレス "000022" は既に送信待ちデータバッファ 3 が割り当てられているため、図 6 (チ) に示すように、パケット P_{10} の圧縮データ p_{10} は、データ p_9 の後に格納される。

【0030】

【発明の効果】以上述べた如く、本発明のフレーム送信回路によれば、送信要求のあったデータは、各送信待ちデータバッファ内で送信先別に多重化され、それを送信データバッファに転送して 1 つのフレームにして LAN に送信するため、LAN 上へ送出するフレーム数を減少させることができる。そのため、フレーム自体に含まれる本来送信すべきデータ以外の情報や、フレーム送出のためのオーバーヘッド分を減少させ、全体の伝送効率を向上させることができる。また、送信要求のあったデータを、データ圧縮手段により圧縮してから前記送信待ちデータバッファに格納する。そのため、1 フレーム当たり 40 に多重化するデータ数を増やすことができる上、LAN 上を流れるデータの冗長度を減らし、1 フレーム当たりの伝送できる総データ量を増加させ、さらに伝送効率を向上させることができる。

【図面の簡単な説明】

【図 1】 本発明の一実施例を示すブロック図

【図 2】 LAN に送信するフレームのフレーム構成を示す図

【図 3】 本発明によるパケット送信処理手順の一例を示すフローチャート

【図 4】 送信待ちデータバッファのタイムアウト監視処理を示すフローチャート

【図 5】 フレーム復元手段における処理手順を示すフローチャート

【図 6】 送信待ちデータバッファの状態を示す図

【図 7】 パケット送信要求とネットワークへの送信の関係を示す図

【図 8】 従来のフレーム送信回路の一例を示すブロッ

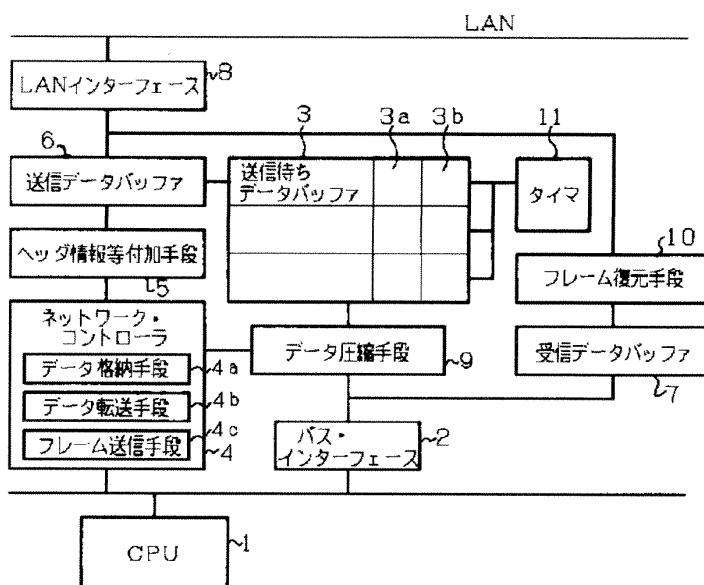
ク図

【符号の説明】

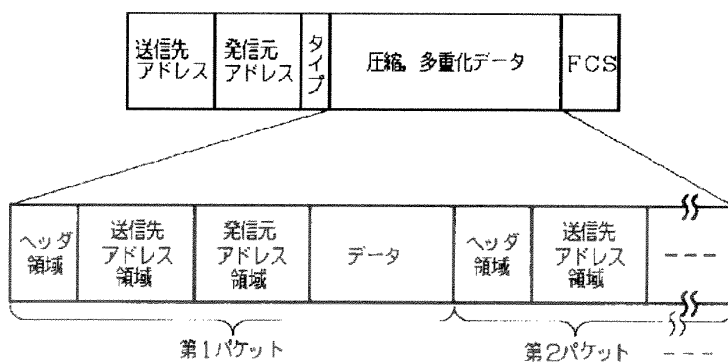
1…CPU、2…バスインターフェース、3…送信待ちデータバッファ、3a…アドレス・レジスタ、3b…タイム・レジスタ、4…ネットワーク・コントローラ、4*

* a…データ格納手段、4b…データ転送手段、4c…フレーム送信手段、5…ヘッダ情報等付加手段、6…送信データバッファ、7…受信データバッファ、8…LANインターフェース、9…データ圧縮手段、10…フレーム復元手段、11…タイマ

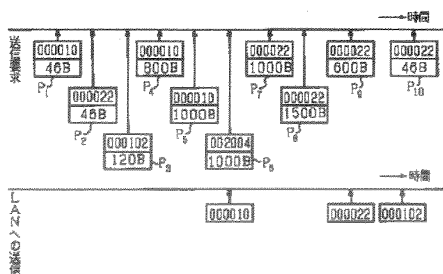
【図1】



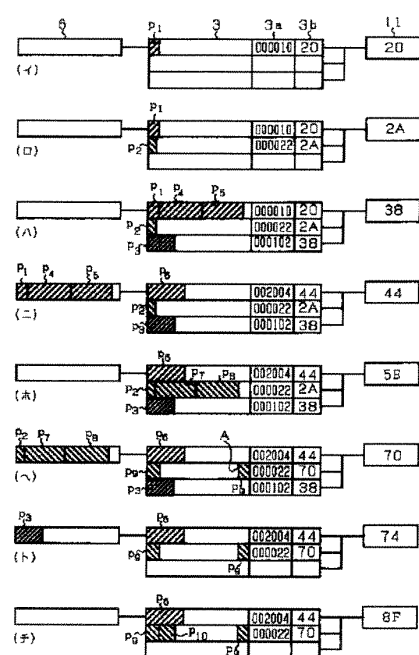
【図2】



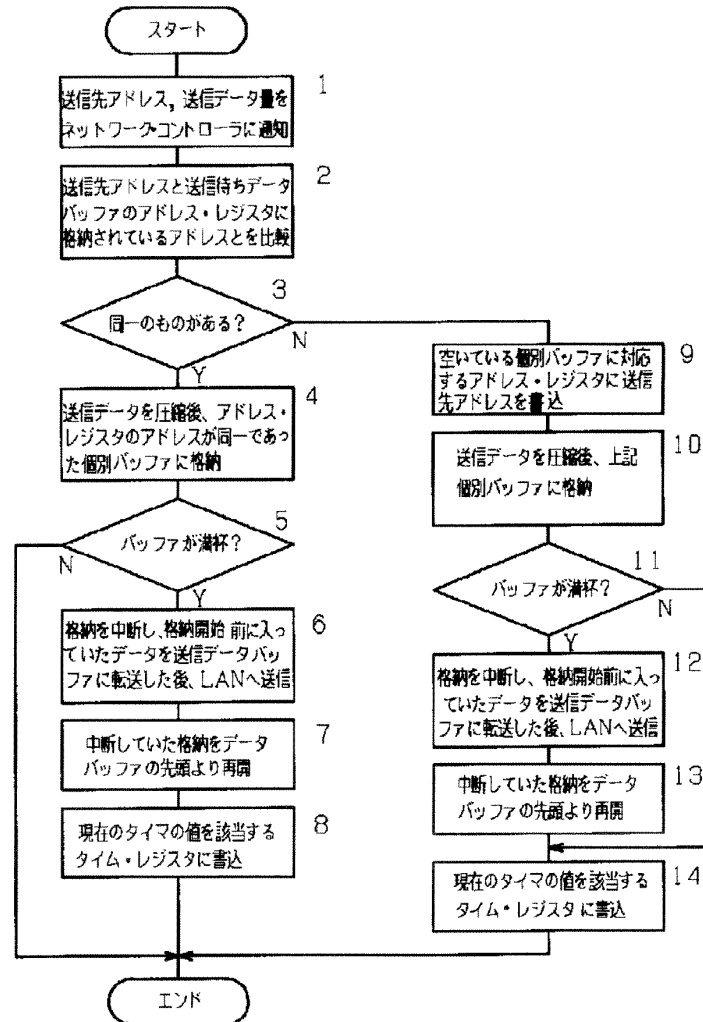
【図7】



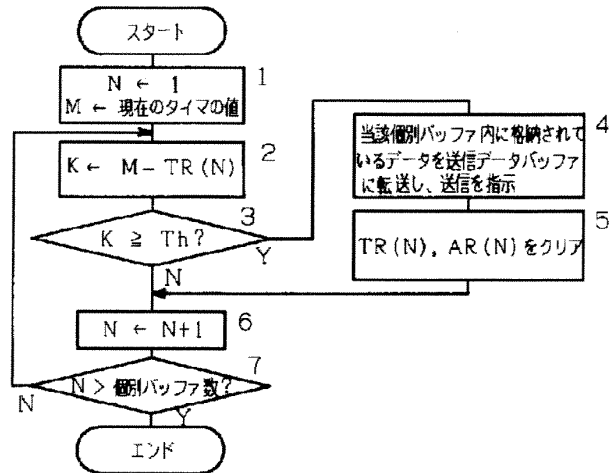
【図6】



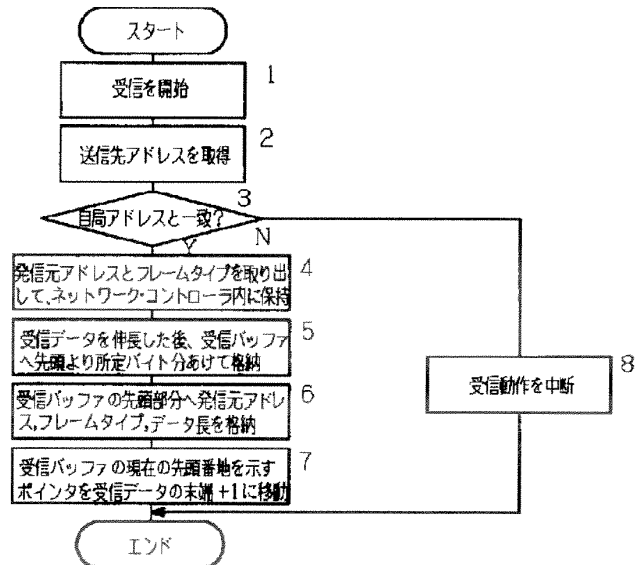
【図3】



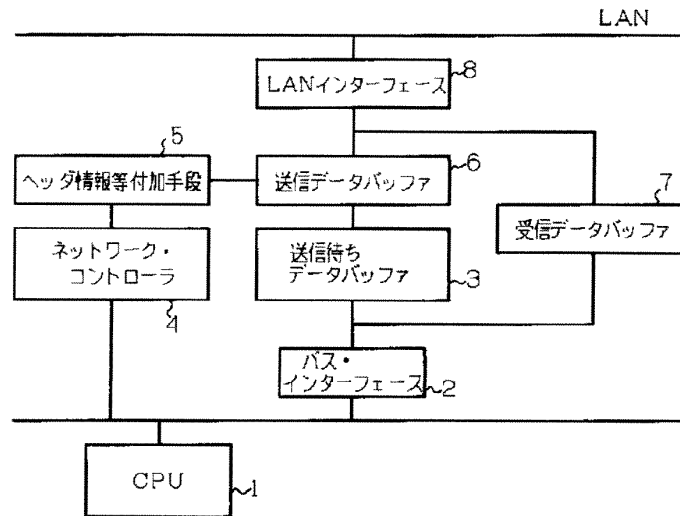
【図 4】



【図 5】



【図 8】



RADIOTELEPHONY SYSTEM

Publication number: JP2000209652 (A)

Publication date: 2000-07-28

Inventor(s): FUKUSHIMA TAKASHI; NARASAKI HIROSHI; TAKAHASHI EIJI; TAMURA NAOKI +

Applicant(s): KOBE STEEL LTD +

Classification:

- international: H04B7/26; H04J3/00; H04J3/04; H04Q7/38; H04B7/26; H04J3/00; H04J3/04; H04Q7/38; (IPC1-7): H04B7/26; H04J3/00; H04J3/04; H04Q7/38

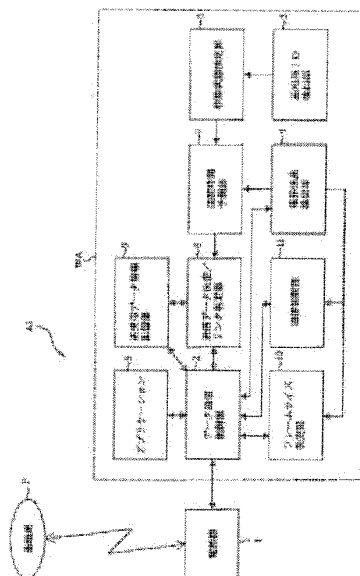
- European:

Application number: JP19990008863 19990118

Priority number(s): JP19990008863 19990118

Abstract of JP 2000209652 (A)

PROBLEM TO BE SOLVED: To obtain a radiotelephony system that flexibly copes with different communication states so as to attain efficient data transmission at all times by solving a problem of a fixed frame size in a conventional system where a too small frame size for usual communication causes much waste in an excellent communication state and a too large frame size for re-transmission on the occurrence of channel interruption causes waste in the communication efficiency. **SOLUTION:** A frame size decision section 10 sets the frame size of transmission data to an optional size (a smaller frame size when the electric field strength is low and a larger frame size when the electric field strength is high) at transmission start and during transmission on the basis of an electric field strength detected by an electric field strength detection section 4. Furthermore, a communication interruption section 11 positively interrupts connection when the electric field strength reaches a prescribed threshold or below.



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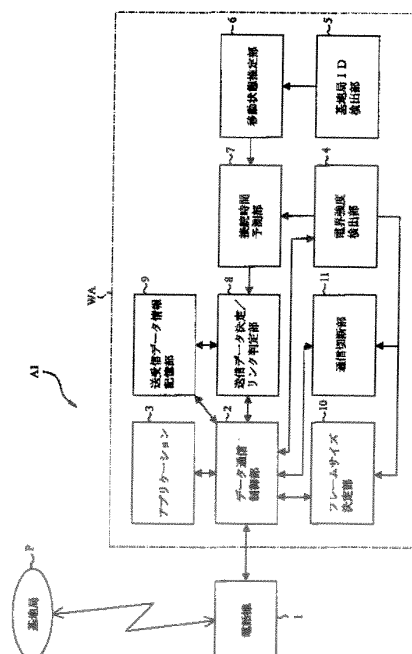
最終頁に続く

(54) 【発明の名称】 無線電話装置

(57) 【要約】 (修正有)

【課題】 フレームサイズが固定されていたため、通信状態が良い場合にはフレームサイズが小さすぎて無駄が多く、悪化して回線が切断された場合には再送するフレームのサイズが大きいために通信効率に無駄が生じる。

【解決手段】 フレームサイズ決定部10により、電界強度検出部4で検出された電界強度に基づいて、送信開始時及び送信中に送信データのフレームサイズを、任意の大きさ（電界強度が低い場合には小さく、高い場合には大きく）設定する。更に、通信切断部11により、上記電界強度が所定の閾値以下になった場合には接続を積極的に切断する。



【特許請求の範囲】

【請求項 1】 基地局を介して無線によりデータ通信を行う無線電話装置において、データ通信の状況に応じて、送信データのフレームサイズを任意の大きさに設定するフレームサイズ設定手段を具備してなることを特徴とする無線電話装置。

【請求項 2】 基地局を介して無線によりデータ通信を行う無線電話装置において、データ通信の状況が所定のレベル以下になった場合に上記基地局との接続を積極的に切断する通信切断手段を具備してなることを特徴とする無線電話装置。

【請求項 3】 基地局を介して無線によりデータ通信を行う無線電話装置において、データ通信の状況に応じて、送信データのフレームサイズを任意の大きさに設定するフレームサイズ設定手段と、データ通信の状況が所定のレベル以下になった場合に上記基地局との接続を積極的に切断する通信切断手段を具備してなることを特徴とする無線電話装置。

【請求項 4】 上記フレームサイズ設定手段でフレームサイズが設定された送信データの送信途中で通信が切断された場合に、後の再送信の機会に上記切断時に送信中であつたフレームの最初から送信を再開するレジューム手段を具備する請求項 1 又は 3 記載の無線電話装置。

【請求項 5】 上記通信切断手段によって送信データの送信途中で通信が切断された場合に、後の再送信の機会に上記送信データの未送信部分を送信するレジューム手段を具備する請求項 2 又は 3 記載の無線電話装置。

【請求項 6】 上記データ通信の状況が、上記基地局から受信した制御信号の電界強度に基づいて判断される請求項 1～5 のいずれかに記載の無線電話装置。

【請求項 7】 上記データ通信の状況が、一定時間内に送信されるデータ量に基づいて判断される請求項 1～5 のいずれかに記載の無線電話装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、基地局を介して無線によりデータ通信を行う無線電話装置に係り、例えば簡易型携帯電話（PHS）等を用いてデータの送受信を行う無線電話装置に関するものである。

【0002】

【従来の技術】デジタル携帯電話（PDC）、簡易型携帯電話（PHS）などの無線電話や携帯型情報端末（例えばミニノート型パソコン）等の急激な普及により、出先や移動中の電車の中などでデータ通信を行う、いわゆるモバイル通信が盛んに行われるようになってきた。しかしながら、PHS等の無線電話を用いたデータ通信は、有線によるデータ通信と比べて通信品質が不安定であり、移動による環境条件の変化に伴って通信品質が大きく変化したり、或いは通信ができたりできなかったりといった様々な状態に遷移するという欠点があり、

有線によるデータ通信ほど容易ではない。このような特徴を有する無線電話を用いたデータ通信において、従来は、例えばデータ送信の開始時にその時の電波強度に応じた転送速度を設定し、固定されたフレームサイズで送信を開始すると共に、上記送信速度、フレームサイズは送信終了まで一定に保たれていた。また、データ送信が終了するまでは、電波状態が悪化したとしても自然に回線が切断されるまでは上記転送速度、フレームサイズでデータ送信が継続されていた。尚、データ送信中に電波状態が悪化して回線が自然切断された場合には、例えば次の回線接続時に、上記切断時に送信中であつたフレームから送信を再開する、いわゆるレジューム機能により、通信の無駄をできるだけ抑える工夫がなされていた。

【0003】

【発明が解決しようとする課題】ところで、上述したように、無線電話によるデータ通信では電波強度が一定の値で安定していることは稀であり、絶えず変化する。そのため、上記従来のデータ送信方法では、例えばデータ送信の開始時に強かった電波強度がその後に悪化したような場合には、高い転送速度のままで送信エラーが増加して転送効率が悪くなってもその状態で通信が継続されるため、コスト高となってしまうという問題点があつた。また、通信状態の変化に関わらずフレームサイズが常に一定であるため、通信状態が良い場合にはフレームサイズが小さすぎて無駄が多く、通信状態が悪化して回線が自然切断された場合にはレジューム機能を用いて再送するフレームのサイズが大きいために無駄が発生するなど、上記フレームサイズをどのように設定しても結局無駄が発生してしまうという問題点もあつた。本発明は上記事情に鑑みてなされたものであり、通信状況に柔軟に対応することによって常に効率の良いデータ送信が可能な無線電話装置を提供することを目的とする。

【0004】

【課題を解決するための手段】上記目的を達成するために第 1 の発明は、基地局を介して無線によりデータ通信を行う無線電話装置において、データ通信の状況に応じて、送信データのフレームサイズを任意の大きさに設定するフレームサイズ設定手段を具備してなることを特徴とする無線電話装置として構成されている。また、第 2 の発明は、基地局を介して無線によりデータ通信を行う無線電話装置において、データ通信の状況が所定のレベル以下になった場合に上記基地局との接続を積極的に切断する通信切断手段を具備してなることを特徴とする無線電話装置として構成されている。更に、第 3 の発明は、上記第 1、第 2 の発明を同時に具備するもので、基地局を介して無線によりデータ通信を行う無線電話装置において、データ通信の状況に応じて、送信データのフレームサイズを任意の大きさに設定するフレームサイズ設定手段と、データ通信の状況が所定のレベル以下にな

った場合に上記基地局との接続を積極的に切断する通信切断手段を具備してなることを特徴とする無線電話装置として構成されている。上記第1、第3の発明における上記フレームサイズ設定手段は、送信データの送信途中で通信が切断された場合に、後の再送信の機会に上記切断時に送信中であったフレームの最初から送信を再開するレジューム手段を具備する場合に特に有効に作用する。また、上記第2、第3の発明における上記通信切断手段についても、転送途中で接続を切断しても後の再送信の機会に上記送信データの未送信部分から送信される

【0005】

【作用】上記第1、第3の発明によれば、基地局から受信した制御信号の電界強度や一定時間内に送信されるデータ量等に基づいて判断されるデータ通信の状況に基づいて、送信データのフレームサイズが任意の大きさ、即ち通信状況が悪い場合には小さく、良い場合には大きく設定される。これにより、通信状況が良い場合には無駄のない効率的な送信ができ、通信状況が悪くなって回線が切断されたとしても例えばレジューム機能によって再送が必要なフレームが小さいため、いずれにしても効率的で無駄のないデータ通信が可能となる。また、上記第2、第3の発明によれば、上記データ通信の状況が所定のレベル以下になった場合にはたとえそのまま通信を継続することが可能であっても上記基地局との接続が積極的に切断され、後に状況が改善されてから通信が再開される。これにより、非効率的なデータ通信を無理に続けることによる無駄を最小限に抑えることができる。

【0006】

【発明の実施の形態】以下、添付図面を参照して、本発明の実施の形態及び実施例につき説明し、本発明の理解に供する。尚、以下の実施の形態及び実施例は、本発明を具体化した一例であって、本発明の技術的範囲を限定する性格のものではない。ここに、図1は本発明の実施の形態に係る無線電話装置A1の概略構成を示すブロック図、図2は上記無線電話装置A1による通信制御処理手順の一例を示すフローチャート（前半）、図3は上記無線電話装置A1による通信制御処理手順の一例を示すフローチャート（後半）、図4は基地局IDの変化周期に基づく移動状態推定テーブルと、電界強度の平均、分散に基づく接続時間予測テーブル、及びその対応関係の一例を示す図、図5は電界強度の平均、分散に基づく接続時間予測テーブルの一例を示す図、図6は図5に示す接続時間予測テーブルを用いた二値判別による接続時間判別方法の説明図、図7は送受信データ情報の一例を示す図、図8は納期までの残余時間によって変化するコス

ト閾値の設定例、図9は電波強度とフレームサイズとの対応を設定したテーブルの一例、図10は実施例に係る無線電話装置A2の概略構成を示すブロック図、図11は上記無線電話装置A2による通信制御処理手順の一例を示すフローチャート、図12は電界強度の平均、分散に基づく移動状態推定テーブルと、電界強度の平均、分散に基づく接続時間予測テーブル、及びその対応関係の一例を示す図、図13は基地局IDの変化周期に基づく接続時間予測テーブルの一例を示す図、図14はニューラルネットワークを用いた接続時間予測の説明図である。本実施の形態では、上記第3の発明の一実施例について説明する。

【0007】本実施の形態に係る無線電話装置A1は、図1に示す如く、基地局Pを介して無線通信を行うPHS等の電話機1と、該電話機1に接続されたワイヤレスエージェント部WAとで構成されている。更に、上記ワイヤレスエージェント部WAは、データ通信制御部2（レジューム手段の一例）、アプリケーション3、電界強度検出部4、基地局ID検出部5、移動状態推定部6、接続時間予測部7、送信データ決定／リンク判定部8、送受信データ情報記憶部9、フレームサイズ決定部10（フレームサイズ設定手段に相当）、及び通信切断部11（通信切断手段に相当）で構成されている。上記ワイヤレスエージェント部WAは、例えば、上記構成各部の処理手順を記述したプログラムが搭載されたミニノート型パソコン等の携帯情報機器であり、上記電話機1とは例えばPCカード等のインターフェイスを介して接続される。尚、上記ワイヤレスエージェント部WAの一部若しくは全てを上記電話機1に内蔵してもよく、逆に上記ワイヤレスエージェント部WAを構成する携帯情報機器内に電話機1の機能を内蔵してもよい。

【0008】上記電話機1は、従来からの一般的な通信機能の他に、上記ワイヤレスエージェント部WAからの問い合わせに対し、上記基地局Pから受信した制御信号の電界強度や、上記制御信号中に含まれる上記基地局のID情報を返答する機能を有している。上記データ通信制御部2は、上記電話機1との間のデータのやり取りをはじめ、上記ワイヤレスエージェント部WAによるデータ通信を集中的に制御する。また、あるデータの送信中に通信が切断された場合には、そのデータの再送信時に上記切断時に送信中であったフレームから送信を再開するレジューム機能を有している。上記アプリケーション3は、例えば電子メールプログラムなど、通信を伴う処理を行うアプリケーションプログラムであり、上記データ通信制御部2に対して任意のデータの送信要求を出力する。上記電界強度検出部4は、上記データ通信制御部2を介して上記電話機1に対して上記電界強度の要求信号を出力し、その返答として出力される上記電界強度を受け取って所定時間分蓄積する。上記基地局ID検出部5は、上記データ通信制御部2を介して上記電話機1に

対して上記基地局IDの要求信号を出力し、その返答として出力される上記基地局IDを受け取って所定時間分蓄積する。上記移動状態推定部6は、上記基地局ID検出部5から上記基地局IDを受け取って蓄積し、これに基づいて当該無線電話装置A1の移動速度を推定する。上記接続時間予測部7は、上記電界強度検出部4から上記電界強度の情報を受け取り、これと上記移動状態推定部6で推定された移動速度とに基づいて、今基地局Pとの間で接続を行った場合にその接続が継続できる時間

(接続時間という)を予測する。上記送受信データ情報記憶部9には、上記アプリケーション3から上記データ通信制御部2に対して出力された送信要求に基づく送信データ情報と、他の端末との間での送受信データ交換

(後述する)によって受信した受信データ情報とが、図7に示すような送受信データ情報として記憶される。上記送信データ決定/リンク判定部8は、上記接続時間予測部7で予測された接続時間に基づいて、上記送受信データ情報記憶部9に記憶されている1又は複数の送信データの送信順序を決定すると共に、その待ち行列の先頭のデータを送信するための発呼を行うか否かを判断し、その結果を上記データ通信制御部2に出力する。上記フレームサイズ決定部10は、データの送信開始前、及びデータ送信中に、上記電界強度検出部4で検出される電*

*界強度に基づいてフレームサイズを決定し、上記データ通信制御部2に指示する。上記通信切断部11は、データ送信中に上記電界強度検出部4で検出される電界強度等に基づいてこのままデータ送信を続けるべきか否かを判定し、続けるべきではないと判断した場合には現在の通信を積極的に切断する。

【0009】続いて、以上のような構成を有する無線電話装置A1による通信制御処理の手順を、図2及び図3に示すフローチャートに従って説明する。尚、アプリケーション3からデータ通信制御部2に対して既に複数のデータの送信要求が出され、それら送信データの情報が上記送受信データ情報記憶部9内に、図7に示すような形で登録されているものとする。まず、基地局ID検出部5と電界強度検出部4は、電話機1からそれぞれ基地局IDと電界強度の情報を逐次受け取り、蓄積する(ステップS1)。上記基地局IDと上記電界強度とが所定時間分(例えば、基地局IDで60秒間、電界強度で10秒間程度)継続して蓄積されると、続いて、移動状態推定部6により、上記基地局ID検出部5に蓄積された所定時間分の基地局IDの変化周期 ω_i (i は現在時刻)が例えば次式により計算される(ステップS2→S3)。

【数1】

$$\text{変化周期: } \omega_i = T / (\sum_{k=i-N+1}^i \delta_k) \\ \text{IF}(\sum_{k=i-N+1}^i \delta_k = 0) \text{ THEN } \omega_i = \infty$$

ただし T = 一定時間

N = 一定時間のデータ個数

δ_k = 時刻 k における基地局ID変化有無(変化有=1、変化無=0)

そして、得られた変化周期と、予め用意された基地局IDの変化周期と移動速度の対応テーブルとを用いて、現在の移動速度が推定される(ステップS4)。 T を60(秒)としたときの上記対応テーブルの一例を図4(上図)に示す。同テーブルに示すように、基地局IDの変化周期が短いほど、即ち短い周期で次々と相手の基地局が切り替わるほど、移動速度が速いと推定できる。また、上記ステップS3、S4と並行して、接続時間予測部7により、上記電界強度検出部4に蓄積された所定時間分の電界強度の平均 m_i と分散 σ_i (i は現在時刻)とが次式により計算される(ステップS5)。

【数2】

$$\text{平均: } m_i = (\sum_{k=i-N+1}^i E_k) / N \\ \text{分散: } \sigma_i = (\sum_{k=i-N+1}^i (E_k - m_i)^2) / (N-1)$$

ただし N = 一定時間のデータ個数

E_k = 時刻 k における電界強度データ

続いて、上記接続時間予測部7において、上記移動状態推定部6で推定された移動速度に基づいて接続時間予測用のテーブルが選択され(ステップS6)、このテーブルと上記算出された電界強度の平均、分散とに基づいて

接続時間が予測される(ステップS7)。

【0010】上記移動速度毎に用意された上記各テーブルは、例えば図5に示すように、電界強度の平均、分散の2軸グラフであり、この2次元空間が、{接続時間0秒、10秒、20秒、30秒}の4領域に分けられており、上記電界強度の平均、分散と接続時間とを対応付けるものとなっている。このように、接続時間予測に電界強度の平均と分散を用いるのは、例えば平均が同じでも分散が小さい方が通信状態が安定していると考えられ、両者を考慮することによってより正確な接続時間予測が可能となるからである。また、電界強度の平均と分散が同じであっても、移動速度が異なれば予測される接続時間も異なると考えられるため、上記のように移動速度毎に異なるテーブルを用いることによって更に正確な接続時間予測が可能となる。ここで、図5に示すような接続時間予測用テーブルを用いた接続時間の判別方法の具体例として、二値判別による方法を簡単に説明する。まず、図5に示す3本の判別曲線のうち、0秒の領域と10秒の領域とを分ける曲線を取り出し、その曲線上に判別点をとる(図6参照)。そして、上記判別点を所定の方向に移動させながら、測定値(電界強度の平均、分

散)が次の条件を満たしているか否かを判定する。

測定値の平均 $\geq$ 判別点の示す平均

且つ

測定値の分散 $\leq$ 判別点の示す分散

上記判別点が上記曲線上のいずれかの位置において上記条件を満たせば、上記測定値は上記曲線の右側の領域

(ここでは10秒以上の領域)にあると判定できる。逆に、上記判別点が上記曲線上の全ての位置において上記条件を満たさなければ、上記測定値は上記曲線の右側の領域(ここでは10秒未満の領域)にあると判定できる。以上の処理を、上記測定値が存在する領域を特定できるまで上記各判別曲線について順次行い、その領域の属する接続時間を予測接続時間とする。

【0011】以上のような処理により接続時間が予測されると、続いて送信データ決定/リンク判定部8により、上記接続時間予測部7で予測された接続時間に基づいて送信待ち状態にあるデータの送信順序を決定する(ステップS8)。これにより、次に送信を行うデータが決定される。ここで、上記ステップS8での送信順序の決定方法の一例を説明する。まず、上記送受信データ情報記憶部9内に記憶された送受信データ情報には、例えば図7に示すように、各送受信データ毎に、各送受信データの送受信相手の端末ID、データID(相手先端末毎)、データサイズ、転送済データ数、送受信データの別、優先度、送信完了期限(以下、納期という)迄の残余時間等が設定されている。尚、送信データ情報は、上記アプリケーション3から上記データ通信制御部2に対して出力された送信要求に基づいて設定される。一方、受信データ情報は、他の端末と接続された際に必要に応じて、若しくは所定時間毎にデータ交換することによって受信される。尚、本実施の形態はデータ送信について説明するため、受信データやその受信手順等についての説明は省略する。更に、上記送信データ情報より、各送信データの送信に要する時間は、上記データサイズから転送済データ数を引いた未送信データサイズを通信速度で割ることによって求められる。尚、通信環境により通信速度は既知であるとする。

【0012】各送信データの送信順序の決定は、例えば次のような考え方に基づいて行うことができる。

(1) 納期に対して重点を置く場合には、納期までの残余時間が小さい順に送信順序を決定する。

(2) 納期の管理を必要としない場合には、少しでも数多くのデータを送信するため、各送信データの送信に要する時間の短い順に(即ち未送信データサイズの小さい順に)送信順序を決定する。

(3) 上記(1)、(2)を両立させたい場合、即ち納期に対して重点を置きつつ、少しでも数多くのデータを送信したい場合には、次のようにして送信順序を決定する。

①まずデータ送信に要する時間が短い順に各送信データ

を並べる。

②納期までの残余時間に対して所定の閾値を設けておき、上記残余時間がこの閾値を下回ったデータを待ち行列の先頭に移動させる。

(4) 上記接続時間予測部7で予測された接続時間を有効に利用する場合には、次のようにして送信順序を決定する。尚、この方法は、レジューム機能がない場合には特に有効である。

①上記接続時間予測部7で予測された接続時間内で送信が完了できる(即ち、送信に要する時間が上記接続時間よりも小さい)データのうち、最大サイズのデータを待ち行列の先頭とする。

②上記接続時間の残余時間(上記接続時間から上記先頭のデータの送信に要する時間を引いた時間)で送信可能な1又は複数のデータを選択する。

③以下、これを繰り返す。

④納期までの残余時間に対して所定の閾値を設けておき、上記残余時間がこの閾値を下回ったデータを待ち行列の先頭に移動させる。尚、図7に示すように各送信データにその他の優先度が付与されているような場合には、適宜その優先度を加味することも可能である。例えば、上記(2)、(3)の場合であれば、まず優先度の高い順に各送信データを並べ、優先度の同じ送信データが複数存在する場合には送信に要する時間の短い順に並べるようにしてもよい。以上のような方法により、その時点で最も適当な送信データが選択されるため、無駄のない効率的なデータ送信が可能となる。

【0013】以上のような方法で次の送信データが決定されると、続いて上記送信データ決定/リンク判定部8により、上記送信データを送信するための発呼を行うか否かが判断され、その結果が上記データ通信制御部2に出力される(ステップS9)。ここで、上記発呼を行うか否かの判断手順の具体例を示す。

1) 理想的な条件でのファイル送信時間 T_{ideal} (sec) を次式により求める。

$$T_{ideal} = (\text{未送信データサイズ(bit)}) / (\text{通信速度(bit/sec)})$$

2) 上記接続時間予測部7で得られた予測接続時間を T_{pred} とする。

3) コスト C_i を次式により求める。

$$C_i = T_{ideal} / T_{pred}$$

ここで、上記コスト C_i は送信完了までに必要な接続回数に相当し、再接続が多いほど上記コスト C_i は大きくなる。尚、ここでは1回の接続確立にあたって通信以外の内部処理に必要な時間をコストとして考慮している。

4) 現時点でのコスト C_i が予め設定された閾値よりも小さければ発呼を行う。尚、上記閾値は、図8に示すように納期までの残余時間によって変化するように設定することもできる。また、上記判断手順に、更に過去の通信履歴を考慮することも可能である。この場合には以下

のような手順となる。

5) 前回の通信における実績コスト C_2 を次式により求める。

$$C_2 = T_{\text{ideal}} / (\text{実際の接続時間(sec)})$$

6) 実績コスト C_2 を時間とともに減衰させる次のような関数を定義する。

$$C(t) = C_2 \exp(Mt)$$

但し、 M : 減衰パラメータ、 t : 前回の回線切断時刻からの経過時間

7) 上記3) で求めたコスト C_1 と上記 $C(t)$ とに基づいて、次のような合成コスト C_{total} を求める。

$$C_{\text{total}} = \text{Max} \{ C_1, C(t) \}$$

8) 上記 C_{total} を用いて、上記4) と同様の要領で発呼するか否かを判断する。

【0014】以上説明したような判断手順により、発呼不可と判断されれば上記ステップS1以下の処理が繰り返される。一方、上記ステップS9において発呼可と判断されれば、上記フレームサイズ決定部10において、上記電界強度検出部4で検出された現在の電界強度に基づいて、上記送信データの送信に用いるフレームサイズが決定される(ステップS10)。上記フレームサイズの決定には、例えば図9に示すようなテーブルが用いられる。即ち、上記フレームサイズは、電界強度が大きければ小さく、電界強度が小さければ大きく設定される。これは、電界強度が大きければなるべく大きなフレームサイズとで効率よく送信すると共に、上記電界強度の低下に応じてフレームサイズを小さくすることで、送信途中で通信が切断された場合の再送データをなるべく少なくして無駄を最小限に抑えるためである。なお、これは、あるデータの送信中に通信が切断された場合に、そのデータの再送信時に上記切断時に送信中であったフレームから送信を再開するレジューム機能を有する場合に特に有効である。上記フレームサイズ決定部10においてフレームサイズが決定されると、上記データ通信制御部2により、送信対象として選択された送信データの送信相手先端末(上記送受信データ情報記憶部9に記憶された送受信データ情報が参照される)に対する発呼処理が自動的に行われる(ステップS11)。このように、上記送受信データ情報として相手先端末を認識するための情報が各送信データ毎に設定されているため、複数端末に対するデータ送信(及び複数端末からのデータ受信)を、例えば送信順序等を調整することなく容易に行うことが可能である。

【0015】上記ステップS11の発呼処理によって送信相手先端末との回線が接続されると、上記相手先端末との間で今から送信する送信データに関する送信データ情報の交換と内容の一致確認が行われ(ステップS12)、上記ステップS10で設定されたフレームサイズでデータ送信が開始される(ステップS13)。データ送信が開始されると、上記フレームサイズ決定部10

は、上記電界強度検出部4で検出される現在の電界強度と図9に示すテーブルとを用いてフレームサイズの変更が必要か否かを常に監視し(ステップS14)、適宜フレームサイズを変更する(ステップS15)。一方、上記通信切断部11では、上記電界強度検出部4で検出される現在の電界強度を監視し、所定の閾値との比較によって通信を継続すべきか否かを判断する(ステップS16)と共に、このまま通信を継続するとコスト等の面で無駄が多いと判断される場合には、現在の通信を積極的に切断する(ステップS17)。送信効率の悪い状態でデータの送信を継続すると、通信エラーの増加によって実質的な送信速度は低下するため、コスト高となって無駄が多いからである。上記通信切断部11によって(或いは通信状態の低下によって自然に)通信が切断されると、上記ステップS1に戻って処理が繰り返される。このとき、送信途中で送信が中断された上記送信データについては、送信データ情報(図7)における送信済データ数が更新された上で、その他の送信待ちデータと同様に送信待ち行列に加えられる。即ち、上記ステップS8における送信データの選択に際しては、送信途中で中断された送信データについてもその他の送信待ちデータと同様に取り扱われる。従って、送信途中で通信が切断された場合でも、次に回線が接続された際にはその続きから送信が開始されるとは限らない。これにより、例えば回線が頻繁に切断されるような電波状況で大きなサイズの送信データが長時間にわたってレジュームを繰り返しながら送信されている場合などには、送信が完了する前であっても送信完了期限が迫ってきた他の送信データを優先させるような制御が可能であり、効率的なデータ送信が可能となる。上記ステップS14、S15、S16の処理は、通信が途中で切断されない限り、送信中のデータの送信が終了するまで繰り返される(ステップS18)。そして、送信中のデータの送信が終了すると、送信待ちデータが存在するか否かが判断される(ステップS19)。送信待ちデータが存在する場合には上記ステップS1以降の処理が繰り返され、送信待ちデータが存在しない場合には一旦処理は終了し、アプリケーション3から新たな送信要求があるまで待機状態となる。

【0016】以上説明したように、本実施の形態に係る無線電話装置A1では、基地局から受信した制御信号の電界強度に基づいて、送信データのフレームサイズが任意の大きさ、即ち通信状況が悪い場合には小さく、良い場合には大きく設定される。これにより、通信状況が良い場合には無駄のない効率的な送信ができ、通信状況が悪くなって回線が切断されたとしても例えばレジューム機能によって再送が必要なフレームが小さいため、いずれにしても効率的で無駄のないデータ通信が可能となる。また、上記電界強度が所定の閾値を下回った場合には、たとえそのまま通信を継続することが可能であって

も上記基地局との接続が積極的に切断され、後に状況が改善されてから通信が再開される。これにより、非効率的なデータ通信を無理に続けることによる無駄を最小限に抑えることができる。また、複数の送信データの中から、その時の予測接続時間に対して最も効率的となる送信データが選択される。また、送信途中で通信が切断された送信データの未送信部分も、他の送信待ちデータと同様に待ち行列に加えられる。従って、通信状態が不安定な無線電話においても無駄のない効率的なデータ送信が可能となる。また、送信を開始する際には、その送信データの送信データ情報内の送信相手先端末が参照され、それに基づいて発呼処理が行われる。従って、例えば複数の送信相手先に対する送信データを、その送信順序に関わらず正しく送信することが可能となる。

【0017】

【実施例】上記実施の形態では、ステップS14におけるフレームサイズ決定部10によるフレームサイズ変更の判断、及びステップS16における通信切断部11による通信切断の判断を、電界強度に基づいて行うようにしたが、例えば、一定時間内に送信されるデータ量に基づいて判断することもできる。例えば上記ステップS16においては、一定時間内に送信されるデータ量が所定の閾値を下回ったときに通信継続不可と判断することも可能である。勿論、上記電界強度に基づく判断と併用してもよい。また、上記実施の形態において、フレームサイズ決定部10と通信切断部11とは必ずしも同時に具備されている必要はない。何れか一方のみを具備する場合（第1、及び第2の発明に相当）でも通信の効率改善効果は十分に期待できる。

【0018】また、上記実施の形態では、基地局IDを用いて移動状態（移動速度）推定を行い、更に推定された移動速度と電界強度の平均、分散とを用いて接続時間予測を行い、これに基づいて自動発呼処理を行う例を説明したが、これについては以下のような変形例が考えられる。

【0019】〔移動状態推定を省略〕移動状態推定を経ることなく、図4の下図に示す接続時間予測テーブルをただ1つ用いて接続時間予測を行うこともできる。この場合、図1に示す構成図では基地局ID検出部5と移動状態推定部6とが省略され、図2に示すフローチャートではステップS3～S6が省略される。勿論、この例の場合には移動状態が考慮されないため、上記実施の形態の例に比べると接続時間予測の精度は多少なりとも低下することに注意しなければならない。

【0020】〔電界強度の平均と分散を用いた移動状態推定〕上記移動状態推定部6による移動状態（移動速度）推定を、電界強度検出部4で検出された電界強度に基づいて行うこともできる。この場合の無線電話装置A2の構成例を図10に、自動発呼処理のフローチャートを図11に示す。本無線電話装置A2の自動発呼手順

（図11）において、図2に示す手順と異なるのは、ステップS3aにおいて電界強度の平均と分散（ステップS5における平均と分散よりも長い区間（例えば60秒間）での値）を求め、ステップS4aで上記電界強度の平均と分散に基づいて移動速度を推定する部分のみである。ここで、ステップS4aにおける移動速度の推定は、例えば図12の上図に示すような移動速度推定テーブルを用いて行われる。この移動速度推定テーブルは、長区間平均と長区間分散の2軸グラフであり、この2次元空間が、〔静止、低速移動、中速移動、高速移動〕の4領域に分けられており、上記電界強度の平均、分散と移動速度とを対応付けるものとなっている。上記移動速度推定テーブルを用いて移動速度が推定されると、その移動速度に基づいて接続時間予測用のテーブルが選択され（ステップS6）、このテーブルと上記算出された電界強度の平均、分散とに基づいて接続時間が予測される（ステップS7）が、これ以降は既に説明した図2に示す手順と同様である。

【0021】〔基地局IDの変化周期を用いた接続時間予測〕上記実施の形態、及び各実施例では、接続時間予測部7による接続時間予測に電界強度の平均と分散とを用いた例を示したが、これら全ての例において接続時間予測に基地局IDの変化周期を用いることもできる。即ち、図2、図11のステップS5において基地局IDの変化周期を算出すると共に、ステップS6、S7において用いられる接続時間予測用テーブルとして、図5に示すようなテーブルに代えて、例えば図13に示すような、基地局IDの変化周期と接続時間とを対応付けるテーブルを用いるようにしてもよい。

【0022】以上説明した実施の形態及び実施例に関し、更に次のような変形例も考えられる。まず、移動状態推定においては、上述したような基地局IDの変化周期等を用いる代わりに、加速度センサやGPS等の各種センサを用いることも可能である。例えば、上記加速度センサを用いる場合には、加速度センサから出力される加速度値を一定時間蓄積し、積分することによってその区間の移動速度が推定できる。またGPSを用いる場合には、GPSから出力される位置情報を一定時間蓄積し、その間に移動した距離を求めることでその区間の移動速度が推定できる。また、電界強度に関する所定の統計量の例として、平均と分散を用いた例を示したが、上記統計量としてはこれらに限られるものではない。例えば、分散に代えて標準偏差を用いても同様の結果が得られることは言うまでもない。

【0023】また、電界強度の統計量（例えば平均と分散）を用いた接続時間予測、若しくは移動状態推定においては、上述したようなテーブル（図5、図12）を用いる方法以外に、例えば上記統計量を入力層とし、接続時間（若しくは移動状態）を出力層とするニューラルネットワークを用いる方法（図14参照）なども考えられ

る。例えば、図14において、電界強度の平均が25.7、分散が7.6であったとすると、入力ベクトルXは例えば次のようになる。

$X = (0, 0, 0, 0, 0, 0, 0, 0, 1, \dots, 0, 1, 0, 0, \dots)$

そして、上記入力ベクトルXに対して例えば出力ベクトルYが、

$Y = (0, 1, 0, 0)$

として得られたとすると、接続時間予測値は10秒となる。

【0024】

【発明の効果】以上説明したように、第1の発明は、基地局を介して無線によりデータ通信を行う無線電話装置において、データ通信の状況に応じて、送信データのフレームサイズを任意の大きさに設定するフレームサイズ設定手段を具備してなることを特徴とする無線電話装置として構成されているため、上記フレームサイズは例えば通信状況が悪い場合には小さく、良い場合には大きく設定される。従って通信状況が良い場合には無駄のない効率的な送信ができ、通信状況が悪くなって回線が切断されたとしても例えばレジューム機能によって再送が必要なフレームが小さいため、いずれにしても効率的で無駄のないデータ通信が可能となる。また、第2の発明は、基地局を介して無線によりデータ通信を行う無線電話装置において、データ通信の状況が所定のレベル以下になった場合に上記基地局との接続を積極的に切断する通信切断手段を具備してなることを特徴とする無線電話装置として構成されているため、上記データ通信の状況が所定のレベル以下になった場合にはたとえそのまま通信を継続することが可能であっても上記基地局との接続が積極的に切断され、後に状況が改善されてから通信が再開される。これにより、非効率的なデータ通信を無理に続けることによる無駄を最小限に抑えることができる。また、第3の発明は、上記第1、第2の発明を同時に具備するもので、上記第1、第2の発明による効果を共に得ることができる。

【図面の簡単な説明】

【図1】 本発明の実施の形態に係る無線電話装置A1の概略構成を示すブロック図。

【図2】 上記無線電話装置A1による通信制御処理手*40

【図7】

端末ID	データID	データサイズ	転送済データ数	送受信	優先度	納期までの 残余時間
000	1	10,000	0	送	2	1,000
000	2	5,000	3,000	受	4	800
111	1	1,000	0	送	5	100

* 順の一例を示すフローチャート（前半）。

【図3】 上記無線電話装置A1による通信制御処理手順の一例を示すフローチャート（後半）。

【図4】 基地局IDの変化周期に基づく移動状態推定テーブルと、電界強度の平均、分散に基づく接続時間予測テーブル、及びその対応関係の一例を示す図。

【図5】 電界強度の平均、分散に基づく接続時間予測テーブルの一例を示す図。

【図6】 図5に示す接続時間予測テーブルを用いた二値判別による接続時間判別方法の説明図。

【図7】 送受信データ情報の一例を示す図。

【図8】 納期までの残余時間によって変化するコスト閾値の設定例。

【図9】 電波強度とフレームサイズとの対応を設定したテーブルの一例。

【図10】 実施例に係る無線電話装置A2の概略構成を示すブロック図。

【図11】 上記無線電話装置A2による通信制御処理手順の一例を示すフローチャート。

【図12】 電界強度の平均、分散に基づく移動状態推定テーブルと、電界強度の平均、分散に基づく接続時間予測テーブル、及びその対応関係の一例を示す図。

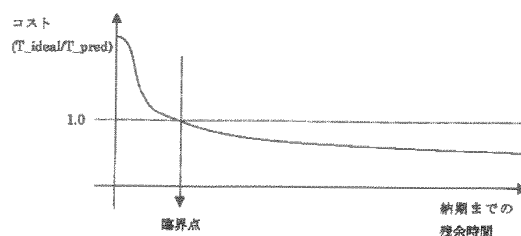
【図13】 基地局IDの変化周期に基づく接続時間予測テーブルの一例を示す図。

【図14】 ニューラルネットワークを用いた接続時間予測の説明図。

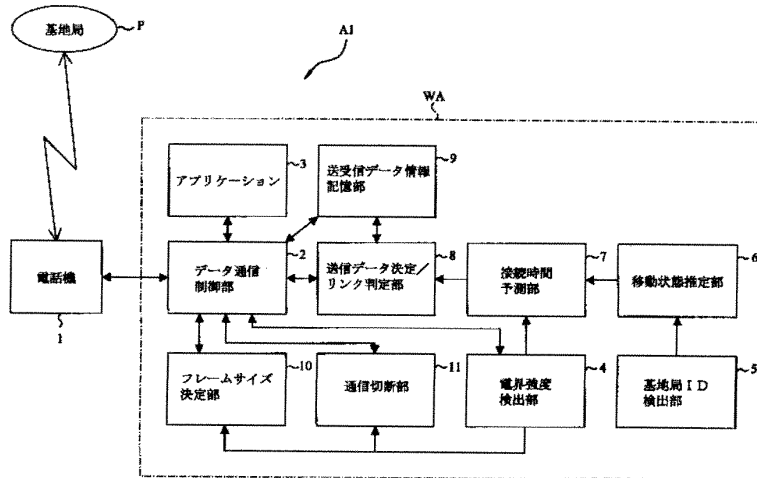
【符号の説明】

- 1…電話機
- 2…データ通信制御部（レジューム手段の一例）
- 3…アプリケーション
- 4…電界強度検出部
- 5…基地局ID検出部
- 6, 6a…移動状態推定部
- 7…接続時間予測部
- 8…送信データ決定／リンク判定部
- 9…送受信データ情報記憶部
- 10…フレームサイズ決定部（フレームサイズ設定手段）
- 11…通信切断部（通信切断手段）

【図8】



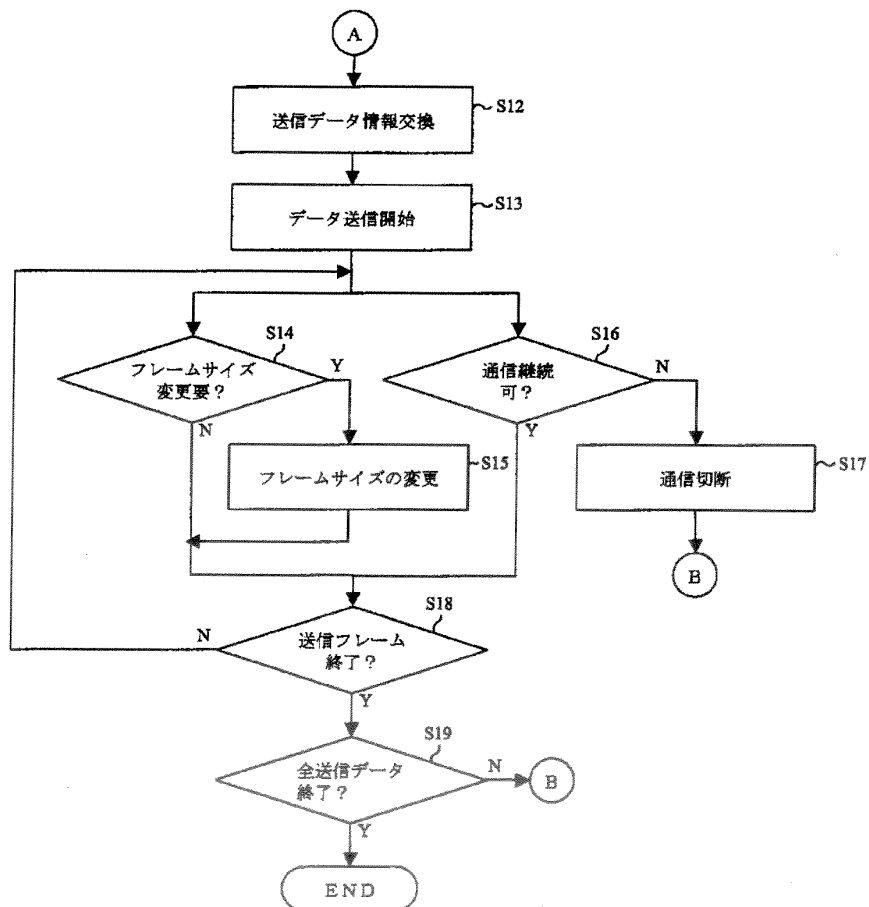
【図1】



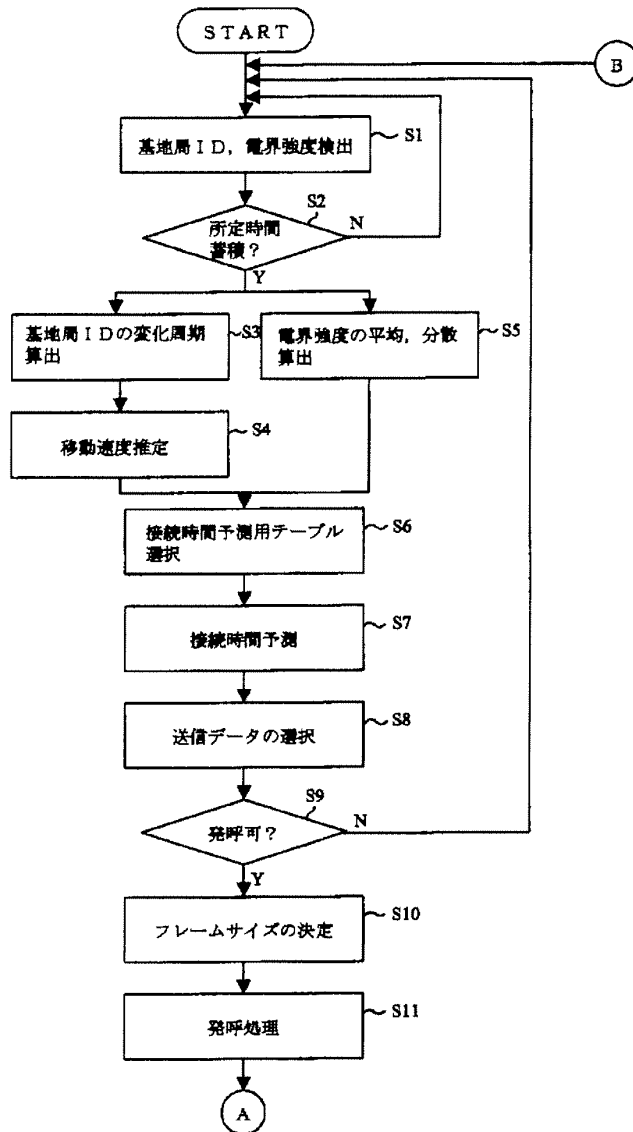
【図9】

電波強度	フレームサイズ
～ 10	256
11～20	512
21～30	1024
31～	2048

【図3】



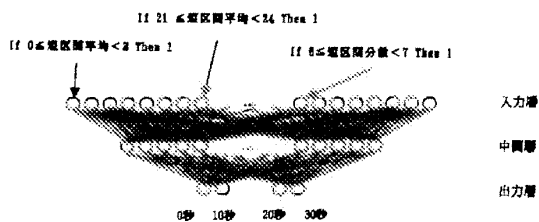
【図2】



【図13】

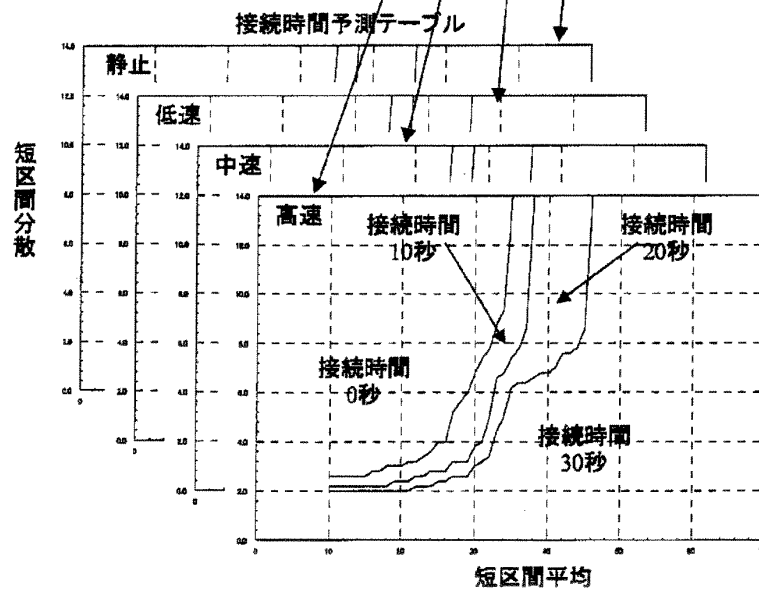
変化周期 [sec.]	接続時間予測
0~5	接続時間 0秒
6~15	接続時間 10秒
16~∞	接続時間 ∞秒

【図14】

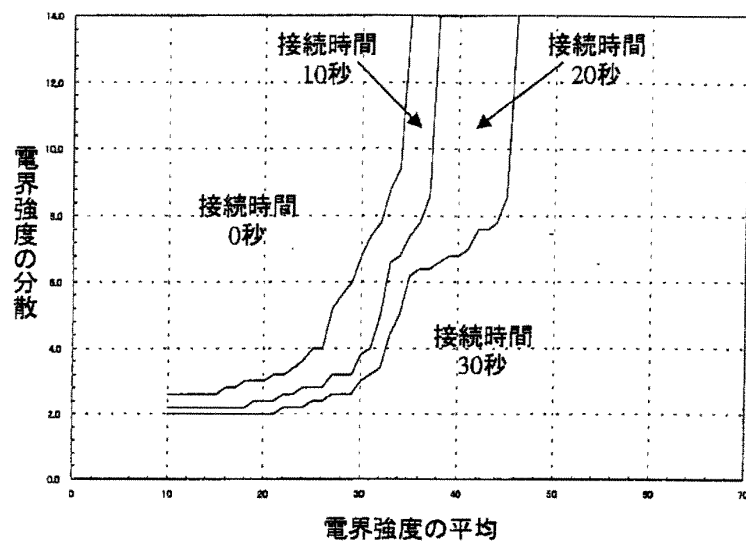


【図4】

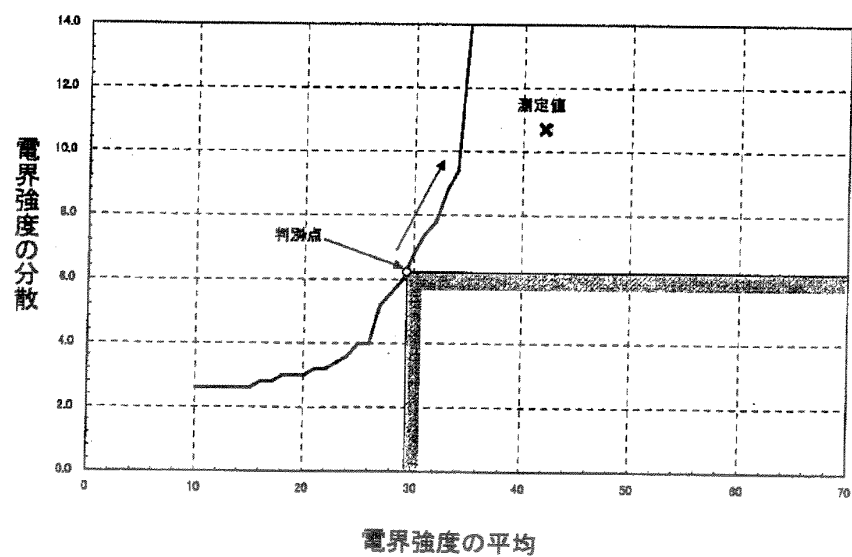
変化周期 [sec.]	移動速度 (状態推定)
0~15	高速移動 (電車)
16~30	中速移動 (車両)
31~60	低速移動 (歩行)
61~∞	静止



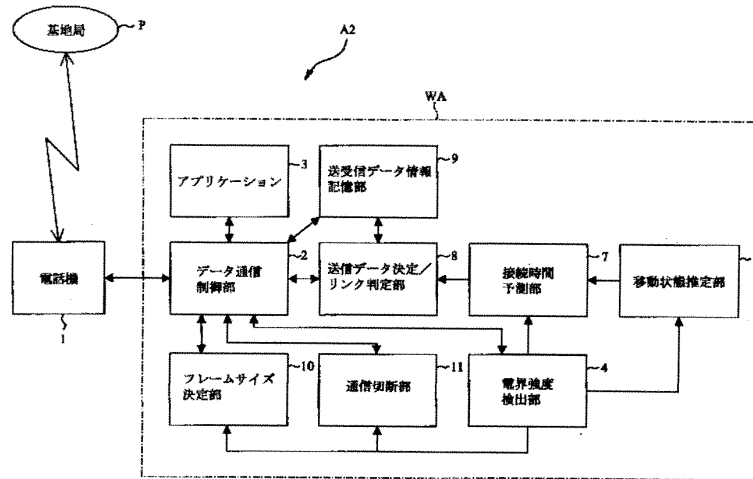
【図5】



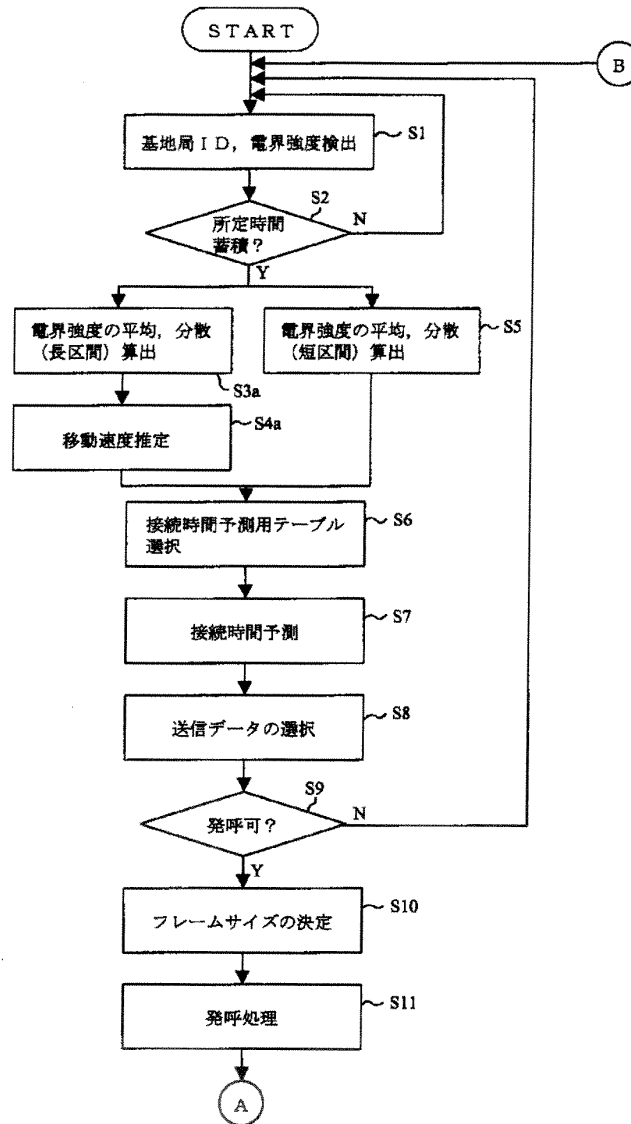
【図6】



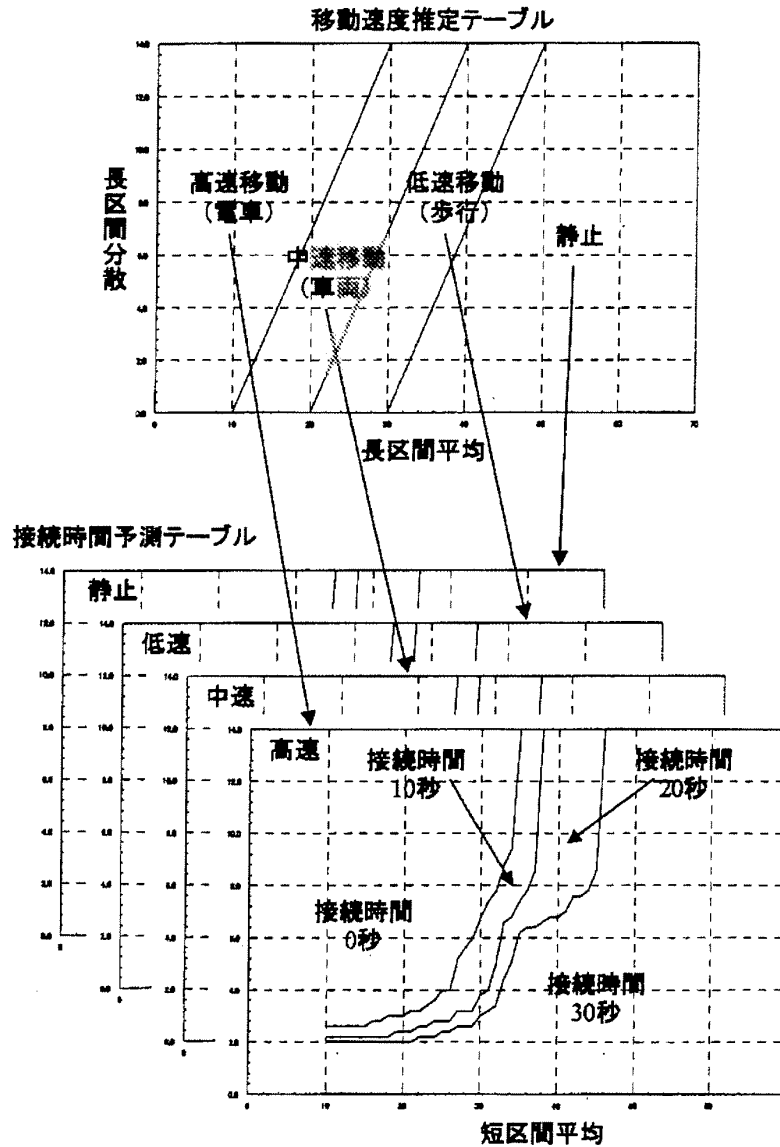
【図10】



【図11】



【図12】



フロントページの続き

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HH23

TCP COMMUNICATION METHOD

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+

Applicant(s): KDDI CORP +

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- European:

Application number: JP20000271666 20000907

Priority number(s): JP20000271666 20000907

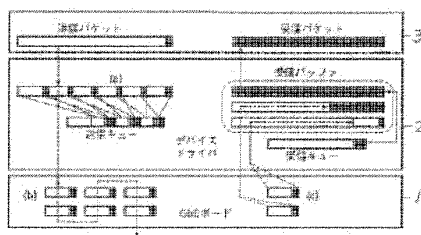
Also published as:

JP4041646 (B2)

Abstract of **JP 2002084289 (A)**

PROBLEM TO BE SOLVED: To attain efficient TCP (Transmission Control Protocol) communication where a terminal can process packets with a larger size without revising the smaller size of packets of about 1,500 bytes or so widely used for a network.
SOLUTION: A CPU on a communication board 1 is utilized so as to disassemble/assemble packets at a TCP level thereby attaining the TCP communication at a high-speed.

送受信の源先



Data supplied from the *espacenet* database — Worldwide

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(12) 公開特許公報 (A)

(11) 特許出願公開番号
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	12/56	11/20	1 0 2 F 5 K 0 3 3
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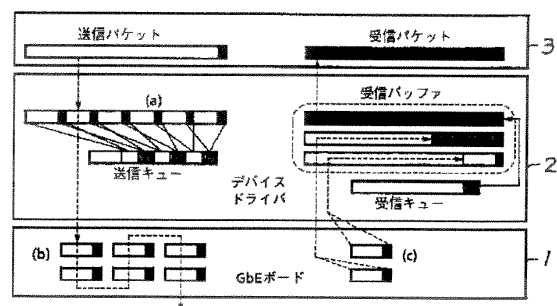
(54) 【発明の名称】 T C P 通信方法

(57) 【要約】

【課題】 ネットワークで広く用いられている例えば1
5 0 0 バイト程度の小さなパケットサイズを変更すること
なく、端末において大きなパケットサイズによる効率的な
T C P 通信を可能にする。

【解決手段】 通信ボード1上のC P Uを利用してT C
P レベルでパケットの分割及び組立を行うことによりT
C P 通信を高速化する。

送受信の流れ



【特許請求の範囲】

【請求項1】 端末本体に搭載される通信ボード上のCPU（以下、オンボードCPUと呼ぶ）を利用してTCPレベルでパケットの分割及び組立を行うことによりTCP通信を高速化することを特徴とするTCP通信方法。

【請求項2】 請求項1において、前記端末本体のTCPモジュールから送信された1つのデータセグメントを前記通信ボード上で適切なTCP/IPヘッダを持つ複数のデータセグメントに分割してネットワークへ出力し、前記ネットワークから入力された複数のデータセグメントを前記通信ボード上で1つのデータセグメントに組み立てた後、前記TCPモジュールに通知することを特徴とするTCP通信方法。

【請求項3】 請求項2において、分割前のデータセグメントに対するACKパケットの増加、並びに、組立前のデータセグメントに対するACKパケットの減少を前記通信ボード上で調整し、これらACKパケットの増減がTCPの輻輳制御や再送処理等の制御手順へ及ぼす影響を防ぐことを特徴とするTCP通信方法。

【請求項4】 請求項3において、送受信シーケンス番号及びACK番号をTCPコネクション毎に保持するコネクションテーブルを前記通信ボード上に用意し、前記コネクションテーブルを参照して前記ACKパケットの増減を調整することを特徴とするTCP通信方法。

【請求項5】 請求項2において、通信経路上のネットワークを含む全てのリンクにおけるMTUサイズ（以下、パスMTUと呼ぶ）と、ネットワークに対するMTUサイズ（以下、ネットMTUと呼ぶ）を比較し、パスMTU $\geq$ ネットMTUである場合はネットMTUに基づいて前記データセグメントの分割を行い、パスMTU<ネットMTUである場合はパスMTUに基づいて前記データセグメントの分割を行うことを特徴とするTCP通信方法。

【請求項6】 請求項5において、宛先IPアドレス毎にパスMTU情報を参照して、前記パスMTUに基づくデータセグメントの分割を行うことを特徴とするTCP通信方法。

【請求項7】 請求項1において、UDPのようにメッセージ境界を保つ必要があるプロトコルのパケットに対してはIPレベルでパケットの分割及び組立を行うことを特徴とするTCP通信方法。

【請求項8】 TCPを処理するTCPモジュール及びIPを処理するIPモジュールを有する端末本体と、CPU及びメモリを有し、ネットワーク及び前記ホストに接続される通信ボードと、該通信ボードの前記CPU（オンボードCPU）上で動作するファームウェアと、前記端末本体が有するCPU（以下、ホストCPUと呼ぶ）で動作する、前記通信ボード用のデバイスドライバとによりTCP通信を行うこと、前記ファームウェア

は、TCPコネクションの確立を監視し、該TCPコネクションの確立手順を利用することより、前記端末本体が前記ネットワーク上のパケットサイズよりも大きなパケットサイズを利用することを可能にする第1機能と、前記通信ボードへ前記端末本体から分割されてDMA転送されたTCPセグメントに適切なTCPヘッダを付加し、前記通信ボードから前記ネットワークへ転送する第2機能と、前記ネットワークから前記通信ボードが受信したパケットをTCPコネクション毎にまとめて1つのパケットとして前記端末本体へ通知する第3機能を提供すること、前記デバイスドライバは、前記端末本体から前記通信ボードへ渡されるべきパケットを、メモリコピーを行うことなく、前記通信ボードでのTCPヘッダの付加を考慮して分割し、通信ボードの前記メモリにDMA転送する機能を提供することを特徴とするTCP通信方法。

【請求項9】 請求項8において、前記ファームウェアは、前記第1、第2及び第3機能により生じる前記端末本体から前記通信ボードへのACKパケットの減少、並びに、前記ネットワークから前記通信ボードへのACKパケットの増加を防ぐ第4機能を提供することを特徴とするTCP通信方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】 本発明はTCP通信を高速化する技術に関する。

【0002】

【従来の技術】 通常のイーサネット（登録商標）では、IPの最大パケット長(Maximum Transfer Unit size:以下、MTUサイズと呼ぶ)は1500バイトであり、TCPの最大ユーザデータ長(Maximum Segment Size:以下、MSSと呼ぶ)はMTUサイズからIP及びTCPのヘッダ領域を除いた1460バイトである。

【0003】 このように通常のイーサネットでは、TCPの最大ユーザデータ長MSSが小さいために、パケット単位で行われるTCPやIPのプロトコル処理、並びに、ホスト端末と通信ボード間のデータ転送処理がホスト端末に対して大きなオーバーヘッドとなり、この処理オーバーヘッドがTCP通信の高速化を妨げている。

【0004】 これらの処理オーバーヘッドを減らすためには、より大きなMSSを用いることが望まれる。

【0005】 一方、近年、ギガビットイーサネット（Gigabit Ethernet（登録商標）：以下、GbEと呼ぶ）の普及に伴い、ホスト端末においてもギガビットクラスの広い帯域を利用可能になっている。しかし、GbEで標準的に用いられているMTUサイズは通常のイーサネットと同じ1500バイトであるため、現状のホスト端末ではやはり、パケット単位で行われるプロトコル処理、並びに、ホスト端末と通信ボード間のデータ転送処理が大きなオーバーヘッドとなる。

【0006】その解決策として、フレーム長を独自に長く拡張したイーサネットフレーム（以下、ジャンボフレームと呼ぶ）を用いてMTUサイズを拡大する方法が提案されている（例えば、MTUサイズ：8800バイト、MSS：8760バイト）。しかし、この方法には下記に示す問題点がある。

(1) 原則として、サブネットを構成するホスト端末、並びに、スイッチやルータ等のネットワーク機器全てが、ジャンボフレームをサポートする必要がある。このため、ジャンボフレームをサポートしない既存のホスト端

末とは同一のサブネットを構成できない。
(2) 通信経路上の、広域網を含む全てのリンクにおけるMTUサイズ（以下、パスMTUサイズと呼ぶ）が例えば8800バイト以上と大きい必要がある。そうでない場合は、ルータでのIPパケットの分割（IPフラグメンテーション）や、ホスト端末でのパスMTUサイズに応じたパケットサイズの調整（最大セグメントサイズの交換、パスMTUディスカバリー(path MTU discovery)) が起きるため、大きなサイズのパケットで通信することは不可能である。

【0007】

【発明が解決しようとする課題】本発明の課題は、パスMTUサイズよりも大きなMTUサイズをホスト端末に提供することができるTCP通信方法を提供することである。

【0008】

【課題を解決するための手段】請求項1に係る発明は上記課題を解決するTCP通信方法であり、端末本体に搭載される通信ボード上のCPU（オンボードCPU）を利用してTCPレベルでパケットの分割及び組立を行うことを特徴とする。請求項2に係る発明は、請求項1において、前記端末本体のTCPモジュールから送信された1つのデータセグメントを前記通信ボード上で適切なTCP/IPヘッダを持つ複数のデータセグメントに分割してネットワークへ出力し、前記ネットワークから入力された複数のデータセグメントを前記通信ボード上で1つのデータセグメントに組み立てた後、前記TCPモジュールに通知することを特徴とするTCP通信方法である。

【0009】請求項3に係る発明は、請求項2において、分割前のデータセグメントに対するACKパケットの増加、並びに、組立前のデータセグメントに対するACKパケットの減少を前記通信ボード上で調整し、これらACKパケットの増減がTCPの輻輳制御や再送処理等の制御手順へ及ぼす影響を防ぐことを特徴とするTCP通信方法である。請求項4に係る発明は、請求項3において、送受信シーケンス番号及びACK番号をTCPコネクション毎に保持するコネクションテーブルを前記通信ボード上に用意し、前記コネクションテーブルを参照して前記ACKパケットの増減を調整することを特徴

とするTCP通信方法である。

【0010】請求項5に係る発明は、請求項2において、通信経路上のネットワークを含む全てのリンクにおけるMTUサイズ（以下、パスMTUと呼ぶ）と、ネットワークに対するMTUサイズ（以下、ネットMTUと呼ぶ）を比較し、パスMTU $\geq$ ネットMTUである場合はネットMTUに基づいて前記データセグメントの分割を行い、パスMTU $<$ ネットMTUである場合はパスMTUに基づいて前記データセグメントの分割を行うことを特徴とするTCP通信方法である。請求項6に係る発明は、請求項5において、宛先IPアドレス毎にパスMTU情報を参照して、前記パスMTUに基づくデータセグメントの分割を行うことを特徴とするTCP通信方法である。

【0011】請求項7に係る発明は、請求項1において、UDPのようにメッセージ境界を保つ必要があるプロトコルのパケットに対してはIPレベルでパケットの分割及び組立を行うことを特徴とするTCP通信方法である。

【0012】請求項8に係る発明は上記課題を解決する他のTCP通信方法であり、TCPを処理するTCPモジュール及びIPを処理するIPモジュールを有する端末本体と、CPU及びメモリを有し、ネットワーク及び前記ホストに接続される通信ボードと、該通信ボードのCPU（オンボードCPU）上で動作するファームウェアと、前記端末本体が有するCPU（ホストCPU）で動作する、前記通信ボード用のデバイスドライバとによりTCP通信を行うこと、前記ファームウェアは、TCPコネクションの確立を監視し、該TCPコネクションの確立手順を利用することより、前記端末本体が前記ネットワーク上のパケットサイズよりも大きなパケットサイズを利用することを可能にする第1機能と、前記通信ボードへ前記端末本体から分割されてDMA転送されたTCPセグメントに適切なTCPヘッダを付加し、前記通信ボードから前記ネットワークへ転送する第2機能と、前記ネットワークから前記通信ボードが受信したパケットをTCPコネクション毎にまとめて1つのパケットとして前記端末本体へ通知する第3機能を提供すること、前記デバイスドライバは、前記端末本体から前記通信ボードへ渡されるべきパケットを、メモリコピーを行うことなく、前記通信ボードでのTCPヘッダの付加を考慮して分割し、通信ボードの前記メモリにDMA転送する機能を提供することを特徴とする。請求項8に係る発明は、請求項8において、前記ファームウェアは、前記第1、第2及び第3機能により生じる前記端末本体から前記通信ボードへのACKパケットの減少、並びに、前記ネットワークから前記通信ボードへのACKパケットの増加を防ぐ第4機能を提供することを特徴とするTCP通信方法である。

【0013】

【発明の実施の形態】図面を参照して、本発明の実施形態例に係るTCP通信方法を説明する。

【0014】[発明の基本] 本方法では、通信ボード上のCPU（オンボードCPU）を利用してパケットの分割及び組立を行うことにより、ネットワークに対しては標準のイーサネットと同じMTUサイズを使用しつつ、端末本体のTCPやIP等のプロトコルモジュールにおいて大きなパケットの利用を可能とする。このため、通信ボード用のデバイスドライバでは、端末本体のIPモジュールに対して、ネットワークに対するMTUサイズ（以下、ネットMTUと呼ぶ）とは独立した、大きなMTUサイズ（以下、ホストMTUと呼ぶ）を提供する。

【0015】TCPでは、コネクション確立時に交換するMSSを越えるセグメントを送信してはならない。一方、MSSの値はMTUサイズに依存するため、大きなMTUサイズを持たない既存の端末では、大きなセグメントを使用することが不可能である。そこで、既存端末とのTCP通信においても、本方法を適用できるように、パケット分割・組立をIPではなくTCPレベルで行う。即ち、端末本体のTCPモジュールから送信された1つのDT（データセグメント）を、通信ボード上で、それぞれ適切なTCP/IPヘッダを持つ複数のDTに分割してネットワークへ出力する。また、ネットワークから入力された複数のDTを、通信ボード上で1つのDTに組み立てた上で、端末本体のTCPモジュールへ通知する。一方、UDP（ユーザデータグラムプロトコル）のようなメッセージ境界を保つ必要があるプロトコルに対しては、通信ボード上でIPレベルのパケット分割・組立（IPフラグメンテーションとリアセンブリ）を行う高速化を図る。

【0016】上記の処理により、TCP通信においては、端末本体のTCPモジュールで処理される1つのDTは、ネットワーク上で転送される複数のDTに対応することになる。このため、既存の端末との通信を想定した場合、分割前のDTに対するACK（確認応答）の数は多くなり、逆に、組立前のDTに対するACKの数は少なくなることが予想される。一方、TCPのslow start（スロースタート）手順やcongestion avoidance（コンジェスチョンアボイダンス）手順、あるいは、fast recovery（ファーストリカバリ）手順において参照される輻輳ウインドウ(cwnd)はACK受信により更新される。また、fast retransmit（ファーストリトランスミット）手順では受信したACKを調べてパケット紛失を検出する。これらのため、通信ボード上でACKの数並びにその内容を調整し、これらの制御手順への影響を抑える。

【0017】ACK調整を行うために、通信ボード上で個々のTCPコネクション毎に、送受信シーケンス番号やACK番号を登録し参照する。そこで、これらの情報（TCPコネクション毎の送受信シーケンス番号やAC

K番号)を保持するためのコネクションテーブルを通信ボード上に用意する。また、パスMTU<ネットMTUである場合は、パケット分割は、ネットMTUではなくパスMTUに基づいて行う。このため、パスMTU<ネットMTUである場合は、宛先IPアドレス毎にパスMTU情報を参照できるようにする。

【0018】端末の収容先としては、基本的には1500バイトのMTUサイズを持つ標準のイーサネットセグメントを想定しているが、これより大きなMTUサイズを持つイーサネットセグメントへ収容した場合も動作可能である。

【0019】[全体構成] 図1に本例に係るTCP通信方法の全体構成を示す。図1において、1は通信ボード、2はデバイスドライバ、3はTCP/IPモジュールである。通信ボード1はオンボードCPUを有する市販のPCIバス用GbEボード（例えば、Alteon Websystems ACEnic（アルテオン・ウェブシステムズ社のエスニック））には用い、本発明実現のため、GbEボードのオンボードCPU（図示省略）上で動作する高速データ通信ソフトウェア（ファームウェア）を改修してある。また、GbEボードに搭載されたPCI/GbEコントロール用ASIC中には、2つのRISC-CPU（MIPS R4000 相当）が組み込まれており、端末本体（図示省略）からダウンロードされたファームウェアによって、送信パケットと受信パケットに対して付加的な処理を行うことができるようにしてある。デバイスドライバ2は端末本体と通信ボード1との間のデータ転送を制御するための通信ボード1用デバイスドライバであり、端末本体が有するCPU（ホストCPU：図示省略）で動作する。デバイスドライバ2には、本発明実現のため、GbEボード用デバイスドライバを改修して用いている。TCP/IPモジュール3はTCPを処理するTCPモジュール及びIPを処理するIPモジュールであり、端末本体に備えられている。その他、端末本体はメモリ等を備え、ジャンボフレームをサポートしている。端末本体にはUNIX（登録商標）コンピュータを用いている。

【0020】ファームウェアはデバイスドライバ2と協調してTCPレベルのパケット分割・組立機能を提供し、TCPを用いた通信に対して効率的なホストバスインターフェースを提供する。デバイスドライバ2は端末本体のOS（例えばUNIX）のカーネルの一部として実装され、カーネル内に予め用意されているIP等のプロトコルモジュールと協調して動作する。また、端末本体は、ファームウェア並びにデバイスドライバ2に実装した機能に対する各種パラメータの設定並びに統計情報の取得を行うための制御用ソフトウェアを有する。これはユーザプロセスである。

【0021】[ファームウェアとデバイスドライバ] 上記の機能を実現するため、通信ボードのファームウェア

並びに端末本体のデバイスドライバ2では、以下の処理(1)～(5)を行う。

【0022】(1) デバイスドライバ2からIPモジュールに対し、1500バイト以上のMTUサイズを通知する。通知するMTUサイズは制御プログラムにより可能とし、例えば最大で36000バイトとする。デフォルト値は8800バイトとする。このMTUサイズはホストMTUである。

【0023】(2) ファームウェアでは、TCPコネクションの確立を監視して、必要に応じて、対応するTCPコネクションテーブルを作成する。このテーブルの最大数はデフォルトで16とするが、コンパイルオプションにより変更可能としている。TCPレベルのパケット分割・組立機能は、このTCPコネクションテーブルが作成されているコネクションに対してのみ適用する。

【0024】(3) TCPではコネクション確立時に交換するSYNパケット並びにSYN+ACKパケットを用いてMSSを互いに交換するため、ファームウェアで必要に応じてこれを書き換え、TCPモジュールに大きなMSSを通知する。

【0025】(4) 上位プロトコルモジュールから渡されたパケットを、送信側ファームウェアにより、制御用ソフトウェアにより指定されたMTUサイズでネットワークに出力できるようにする。このMTUサイズはボードMTUである。このために、付加するヘッダを含む送信パケットを連続したオンボードメモリ(通信ボード1)上に置く。そこで、デバイスドライバ2において以下の手順(a)、(b)を用いることにより、デバイスドライバ2自身並びに通信ボード1上において不要なデータコピーを行うことなく、分割した各パケットに対して通信ボード1上で容易にヘッダを付加できるようにする。

(a) デバイスドライバ2では、分割する各パケット毎にDMA(Direct Memory Access)転送要求を設定する。この際、先頭パケット以外は、DMA転送を開始するアドレスをヘッダ領域分、前にずらす(図1の(a)参照)。パケット本体のコピーは行わない。

(b) ファームウェアでは、先頭パケットのヘッダ情報を基に各パケットのヘッダを作成し、各パケットの先頭部分を上書きして送信する(図1の(b)参照)。

【0026】(5) 受信側のファームウェアでは、ネットワークから受信したパケットをできる限り大きなパケットサイズでデバイスドライバに通知するために、以下に示す方針(a)～(e)に従って組み立てる。

(a) 受信したフレームがTCPセグメントであり、且つ、対応するコネクションテーブルが存在する場合は、原則として、端末本体に対して受信通知のための割り込みをかけず、端末本体へのDMA転送のみを行い、次のフレームの受信を待つ。

(b) 次の受信フレームが、受信済み(但し、端末本体には未通知)のTCPセグメントに連続するTCPセグ

メントである場合は、受信フレームからTCP/IPヘッダ等を取り除いて、1つのTCPセグメントに結合されるようにDMA転送する。結合されたTCPセグメントに対するTCP/IPヘッダの書き換えも同時に行う。

(c) セグメント紛失等により連続するTCPセグメントを受信しなかった場合や、上記の結合処理によってホストMTUを超えたTCPセグメントとなる場合等、パケット組立が不可能である場合は、これ以前に受信した未通知のフレームのみを端末本体へ通知する。以降は、セグメント紛失から回復するまで、該当するコネクションに属するセグメントの組立は行わない。

(d) セグメント紛失を検出した場合($rx_next \neq rx_max$)は、シーケンス番号(SEQ番号)を持つセグメントのグループ rx_gle と rx_max を保持する。このグループが受信ホストから送達確認(ACK, $no \geq rx_max - rex$)されるか、このグループまでのセグメントを再度、紛失なく連続して受信した場合に、セグメント紛失が回復したと見なす。

(e) 一定の待ち時間($deliver_timeout$)経過後は、受信したフレームを端末本体へ通知する。

【0027】[TCP-ACK補償機能] TCPレベルのパケット分割を行うことにより、TCPモジュールから渡された1つのTCPセグメントに対して、複数のACKパケットが返ることが予想される。このため、下記の問題(1)～(2)が予想される。

(1) ACK処理負荷が削減されない。

(2) スロースタート(slow start)時の輻輳ウィンドウの急増など、TCP輻輳制御との不整合が発生する。

【0028】一方、パケット組立を行う端末のTCPモジュールでは、大きなパケットサイズでプロトコル処理を行うため、十分にACKパケットを送信できない可能性があり、これによりTCPの輻輳制御や再送制御に悪影響を与える恐れがあるという問題がある。

【0029】これらの問題を解決するために、以下の要領(a)～(b)により端末本体に通知するTCP-ACK(ユーザデータを含まない)を削減し、また、ネットワーク側へ送出するTCP-ACKを増加させることとする。

【0030】(a) TCP-ACKの削減(送信側)

(i) TCPコネクションテーブルにACK番号、並びに、送信TCPセグメントのSEQ番号を記録する。記録するSEQ番号は必要に応じて上書きする。

(ii) 保持しているTCPセグメントのSEQ番号を送達確認する場合、または、 $2 \times \text{host_mss} - \text{n_mss}$ を超えるTCPパケットを新規に送達確認する場合、または、最もSEQ番号の大きい送信済みパケットをACKする場合(A

CK. no == snd_max) に、ACKを端末本体に通知する。

(iii) DUPACK (重複ACK: ACK. noとACK. win (ウインドウサイズ) が前回と同じACK) では、ホスト側MSS/ボード側MSSで与えられる個数のDUPACK受信毎に端末本体へ通知する。

【0031】(b) TCP-ACKの増加(受信側)

(i) TCPセグメントが連続して2セグメント受信した場合は、通信ボード1でACKを作成し送信する。但し、原則として、3セグメント目を受信後に2セグメント分のACKをする。

(ii) 3セグメント目が受信されない場合は、deliver_timer 発火後、端末本体への通知と同時にack_timerを起動させる。ack_timer発火までに端末本体からのACK受信もしくはネットワークからのDT受信がなければ、ACKを作成し送信する。

(iii) パケット紛失時は、前述のようにDT受信毎にそのままホストに通知させ、適切にDUPACKを発生させる。

【0032】従って、TCP通信に対する動作手順は以下のように定まる。

【0033】〔動作手順その1: コネクション確立とパスMTU設定〕図2にTCPコネクション確立に伴う処理フローを示す。TCPでは、コネクション確立時に相手から通知されたMSSと自分のMSSとを比較し、いずれも小さい方のMSSを使用する。このため、通信ボード1とそのデバイスドライバ2では、コネクション確立時に以下の処理(1)～(2)を行い、端末本体のTCPモジュールで使用するMSSを大きく保つと同時に、相手端末に対しては、ネットMTU(netMTU)またはパスMTU(pathMTU)に基づくMSSを通知する。更に、必要であればパケット分割に用いるパスMTUの設定も行う。

【0034】(1) 図2において、TCPモジュールからのSYN(+ACK)を受信した場合(ステップS1)、それに含まれるMSS(図2のSYN(+ACK). MSS)を、同じIPアドレス宛のパスMTUがあればこれに基づくMSSに、無い場合はネットMTUに基づくMSSに更新し、相手端末に送信する(ステップS2、S5)。受信がSYNであれば、同時にコネクションテーブルも作成する(ステップS3、S4)。

【0035】(2) ネットワークからのSYN(+ACK)を受信した場合(ステップS6)、それに含まれるMSS(図2のSYN(+ACK). MSS)と、同じIPアドレス宛のパスMTUがあればこれに基づくMSS(図2のnmss)と、無い場合はネットMTUに基づくMSS(図2のnmss)と比較する(ステップS7、S8)。前者が小さい場合は、nmssの更新、並びに、パスMTUの登録あるいは更新を行う(ステップS9)。次に、ホストMTUに基づくMSSを超えないようにnmss

を整数倍した値を、SYN(+ACK)のMSSとしてTCPジュールに通知する(ステップS10、S13)。また、受信がSYNであれば、コネクションテーブルを作成する(ステップS11、S12)。

【0036】図3にコネクション確立時の通信シーケンス例を示す。ここでは、双方の端末で、ホストMTUを9000バイト程度として、ネットMTUに1500または9000バイトを使用した4種類の組み合わせa～dに対するシーケンスを示している。

【0037】図3より、いずれの組み合わせの場合も、ネットワーク側のMSSは小さい方のネットMTUに基づく適切な値(a～cでは1460バイト、dでは8960バイト)が設定され、端末側のMSSもネットワーク側のMSSの整数倍(a～cでは8760バイト、dでは8960バイト)となるように調整されていることが判る。なお、dでは、双方の端末のネットMTUが9000バイトであるため、端末間に9000バイトより小さいMTUサイズを持つ経路が存在しなければ、パケット分割は行われない。

【0038】一方、a～dの全ての場合で、より小さいパスMTUが通信経路中に存在する可能性もある。これは、データ転送中にICMPunreachable が返送されることで検出できる。通信ボード1ではICMPunreachable に含まれる新しいパスMTUの登録。更新を行い、分割に用いるパケットサイズを調整する。

【0039】〔動作手順その2: データ転送時の手順〕図4に、本方法をサポートする端末間におけるデータ転送開始直後の通信シーケンスを示す。以下、図4に沿ってデータ転送時の動作手順(1)～(5)を説明する。

【0040】(1) 送信側のTCP並びにIPモジュールは、動作手順その1により提供される大きなMSS(8760バイト:以降、ホストMSSと呼ぶ)並びにMTUサイズを利用してプロトコル処理を行い、DT送信を通信ボード1に要求する(図4中、(a)参照)。

【0041】(2) 送信側の通信ボード1では、DTを動作手順その1により決定したMSS(1460バイト:以降、ネットMSSと呼ぶ)に適合するように分割し、各々に適切なTCP/IPヘッダを付加した上で送信する(図4中、(b)参照)。

【0042】(3) 受信側の通信ボード1では、DTが正しく連続受信されている間は、原則としてネットワークから受信したDTを即座にTCPモジュールへは通知せず、可能な限り大きなDTに組み立てる。DT通知は以下のどちらかの条件(a)(b)を満たした時点で行う。

(a) DTの長さ>ホストMTU-ネットMTU(図4中、(c)参照)。

(b) 先頭DTの受信後一定時間が経過(図4中、(d)参照)。

【0043】(4) 一般的なTCPの実装では、2つのD

Tを正しく受信する毎に、対応するACK番号を持つACKを1つ返す。DT送信側が本方法をサポートしていない場合も同様の間隔でACKが返るように、以下の要領(a)(b)に従い受信側の通信ボード1でACKを補填する。この際、TCPモジュールからのACKと重複することを避けるようにしている。

(a) 新たに2つのDTを送達確認可能である場合、次のDT受信時にACKを送信する(図4中、(e)参照)。但し、2つのDT毎にACKを返すために、最後に受信したDTはACKの対象に含めない。

(b) 上記(3)によるDT通知時点で、新たに2つのDTをACKできる場合はACKタイマを設定する(図4中、(f)~(h)参照)。このタイマは次のDTの受信(図4中、(f)参照)、もしくは、TCPモジュールからのACK応答(図4中、(g)参照)によりキャンセルされる。タイマが満了した場合は、通信ボード1からACKを送信する(図4中、(h)参照)。

【0044】また、TCPモジュールからのACKについては、最後に送信したACKよりも新しい情報(ACK番号、winsize)を含んでいれば送信側に転送する。この際、通信ボード1でより進んだACK番号を既に送信側に通知している場合は、これに合わせてACK番号とウィンドウサイズ(winsize)を決定する(図4中、(i)参照)。

【0045】(5) 一方、DT送信側の通信ボード1には上記(4)により2つのDT送信毎に1つのACKが戻る。TCPモジュールにおいても、cwndを適切に更新するために、分割前の2つのDTに対して1つのACKが通知されることが望ましい。また、silly window syndrome(シリウインドウシンドローム)を避けるためには、ホストMSS以上の受信ウィンドウを通知すべきである。逆に、Nagle algorithm(ナグルアルゴリズム)、keep alive(キープアライブ)、window probe(ウィンドウプローブ)等の手順では、受信したACKを必ず通知すべきである。そこで通信ボード1では、下記(a)(b)(c)いずれかの処理は見込まれる場合のみ、ACKを通知する。

(a) ホストMTUの2倍ーネットMTU以上のDTを送信確認する(図4中、(j)参照)。

(b) 干す炉MTU以上の受信ウィンドウが付与される(図4中、(k)参照)。

(c) 送達確認待ちのDTがなくなるか、既がない(図4中、(l)参照)。

なお、ACK番号またはwinsizeのいずれかに、TCPモジュールにまだ通知すべきでない小さな更新がある場合は、これらを調整した上で通知する(図4中、(k)参照)。

【0046】[動作手順その3:誤り回復時の手順] 図5に、DT紛失に伴う再送手順を含む通信シーケンス例を示す。紛失DTに回復手順は、双方の端末のTCPに

よりエンド・エンドで提供される。以下、図5に従って、TCPの誤り回復手順を考慮した方法の動作手順(1)~(6)を説明する。

【0047】(1) DT(29201:30661)の紛失を検出すると、通信ボード1は既に受信組立済みのDT(26281:29201)を即座にTCPモジュールへ通知する(図5中、(a)参照)。

以降、通信ボード1では、TCPモジュールの誤り回復手順の完了を確認するまで、受信したDTの組立は行わない(図5中、(b)参照)。

【0048】(2) 受信側通信ボード1では、TCPモジュールにおける誤り回復手順の完了を検出するために、DT紛失の検出後、最大のシーケンス番号を持つ連続した受信済みDTのグループをリスト[rx_gle, rx_max]形式で保存する。

【0049】図5の例では、DT紛失を検出した直後の受信済みDTグループは[30661, 32121]であり、再送DTの受信直前は[30661, 43801]となる。通信ボード1はrx_gleまでの紛失DTを受信することで、紛失部分がなくなり、rx_maxまで連続して受信した状態となる。

TCPモジュールから、rx_maxまで送達確認するACKが返されれば、TCPモジュールの誤り回復手順が完了したと見なす。また、rx_maxまでの全てのDTが再度連続して受信された場合も同様である。

【0050】(3) TCPモジュールから、紛失DTの送信を要求するACK(a29201, w37961)が渡されると、通信ボード1はこれを送信側に転送する。以降も、DT通知毎に返送されるduplicate ACKについては、そのまま送信側に転送する。(図5中、(c)参照)。

【0051】(4) 送信側の通信ボード1において検出したduplicate ACK(a29291, w62615)は、fast retransmitの開始前後で以下(a)(b)のように処理を変える。

(a) fast retransmitを素早く開始させるために、TCPモジュールに同一のACKを既に通知済みか同化検査し、通知済みであれば1つのACKを、そうでなければ2つのACKをTCPモジュールに通知する。更に、2つのduplicate ACKについては、受信次第TCPモジュールに通知する(図5中、(e)参照)。

(b) その後は、fast recovery手順でのcwndの急激な増加を避けるために、ホストMTU/ネットMTU(比の値)個に1つの割合で、duplicate ACKが通知されるようにする。但し、fast retransmit開始のために先に通知した4つのACKを考慮して、次の(5番目)のACK通知だけは、前のACKから数えてホストMTUの4倍/ネットMTU(比の値)-3なる個数のduplicate ACKを受信した時点で行う。

【0052】(5) TCPモジュールは、duplicate ACKを受信すると、DT(29201:37961)を再送する。通信ボード1は、これをネットMSSに基づき分割し、先頭のDT(29201:30661)だけを送信する(図5中、

(f) 参照)。

【0053】(6) 受信側の通信ボード1では、再送DT (29201:30661) の受信により、紛失部分がなくなり受信済みDTグループ[30661,43801]まで連続して受信した状態となる。そこで通信ボード1では、rx_max = 43801をrx_max_recに記録し、再送DTをTCPモジュールに通知する。そして、TCPモジュールから返送されるACK(a43801,w35040)により、誤り回復の完了を確認する。これにより、以降の受信DT(45261:46721-51101:52561)は組立可能となる(図5中、(g)参

照)。一方、ACKが戻る前に受信したDT(43801:45261)は、誤り回復完了を検出する前であるため、受信後すぐにTCPモジュールへ通知されている(図5中、

(h)参照)。本DTはrx_max_recに連続するため、ACK(a43801,w35050)が戻った時点で、TCPモジュールにより正常に連続受信されることが保証される。

【0054】[動作手順その4:コネクション終了時の手順] 図6に、コネクション終了時の通信シーケンス例を示す。本方法では、コネクション終了に伴う状態遷移を簡素化するために、TCPモジュールからのコネクション終了要求(FIN)並びにその送達確認のみを監視する。TCPモジュールからのFINが送達確認された時点で、そのコネクションに対しては、通信ボード1に新たなパケット送信要求が来ないことが保証されるため、該当するコネクションテーブルを削除することができる。以下、図6を例に、コネクション終了時の手順(1)~(3)を説明する。

【0055】(1) 通信ボード1では、TCPモジュールからFINフラグを有効にしたDTを渡されると、これがネットMSS以上のユーザデータを含むDTである場合、これを通信ボード1で分割する。その際、FINフラグは分割後の最後のDTのみ有効にする(図6中、(a)参照)。

【0056】(2) 一方、ネットワークから受信したFINセグメントについては、通信ボード1上で、通常のDTと同様、可能であれば前のDTに連結する。そして、直ぐに、TCPモジュールへ通知する(図6中、(b)参照)。

【0057】(3) ネットワークからFINに対するACKを受信すると、通信ボード1はこれをTCPモジュールへ通知し、コネクションテーブルを削除する(図6中、(c)参照)。以降は、通信ボード1はTCP通信に介在せず、受信データをそのままTCPモジュールへ通知する(図6中、(d)参照)。

【0058】上述のように、通信ボード1のオンボードCPUを利用して、TCPまで考慮したパケット分割と組立を行うことにより、端末に大きなMTUサイズを提供するから、例えば標準のイーサネットと同じMTUサイズ(1500バイト)をネットワーク上で用いること

ができる。つまり、ネットワークでは広く使用されている小さなパケットサイズを用いつつ、ホスト内では大きなパケットサイズで効率良くTCPのプロトコル処理を行うことができる。このため、本方法をサポートする端末のプロトコルモジュールでは、大きなMTUサイズをサポートしない既存の端末やネットワーク機器と接続した場合でも、大きなパケットで処理を行うことが可能となる。

【0059】また、パケットの分割・組立により、端末本体のTCPモジュールにおける1つのデータセグメント(DT)が、ネットワーク上における複数のデータセグメント(DT)に対応するので、本方法をサポートする端末が既存端末と通信した場合は、双方の端末が送受信するACK(確認応答)の数が変動するので、TCPの輻輳制御や再送処理に影響が現れる可能性があるが、ACK数の増減を調整することによりこの影響を抑制することができる。

【0060】つまり、TCPレベルのパケット分解・組立を行うと、通信ボード1が端末本体ホストから受信するACKパケットが、通信ボード1が通信相手へ送信すべきACKパケットよりも減少し、反対に、通信ボード1が端末本体へ通知すべきACKパケットよりも、通信ボード1が通信相手から受信するACKパケットが増加する。このようなACKパケット数の不一致はTCP輻輳制御機能等に副作用を与えるが、ACKパケット増減を補償することにより、TCP輻輳制御機能等に与える副作用を防ぐことができる。

【0061】更に、TCP以外のパケット、例えばUDPパケットについては、通信ボード1上でIPフラグメンテーション(IP分割)並びにそのデフラグメンテーション(IP組立)を行うことにより、送信端末と受信端末におけるプロトコル処理の負荷が削減可能である。

【0062】また、端末本体と通信ボード1間でのTCPレベルのパケット分解・組立には、メモリコピーを行わず、DMA転送を行うことにより処理時間を短縮することができる。

【0063】互いに通信する端末間の一方が上述の機能をサポートすることにより、他方の端末及びネットワーク機器がジャンボフレームをサポートしない場合でも、相互接続性を保証することができる。

【0064】また、上述の機能を双方の端末がともにサポートしていれば、ネットワーク機器がジャンボフレームをサポートしない場合でも、全てジャンボフレームを適用した場合と同様に、各端末上でTCP、IP、デバイスドライバ等の処理オーバーヘッドを削減することが可能である。

【0065】

【発明の効果】本発明によれば、ネットワークで広く用いられている例えば1500バイト程度の小さなパケッ

トサイズを変更することなく、端末において大きなパケットサイズによる効率的なTCP通信が可能となる。また、パケットの分解・組立に伴うACKパケットの増大・不足を補償することで、TCP輻輳制御等との不整合を防止することができ、ネットワークに対して従来と同様の輻輳制御等を提供することが可能となる。このような効果を持つ本発明は、FPGA等の（プログラマブル）ロジックによる実装を通じた通信装置への適用等が可能である。

【図面の簡単な説明】

【図1】本発明の実施形態例に係るTCP通信方法の全体構成を示す図。

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* 【図2】コネクション確立時の処理フローを示す図。

【図3】コネクション確立時の通信シーケンス例を示す図。

【図4】データ転送時の通信シーケンス例を示す図。

【図5】再送時の通信シーケンス例を示す図。

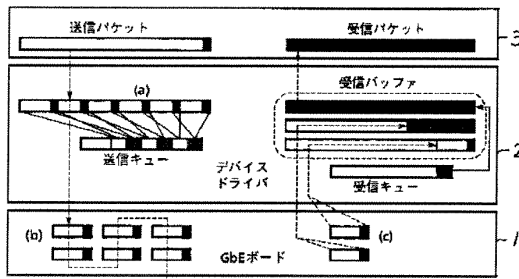
【図6】コネクション終了時の通信シーケンス例を示す図。

【符号の説明】

- 1 通信ボード
- 2 デバイスドライバ
- 3 TCP/IPモジュール

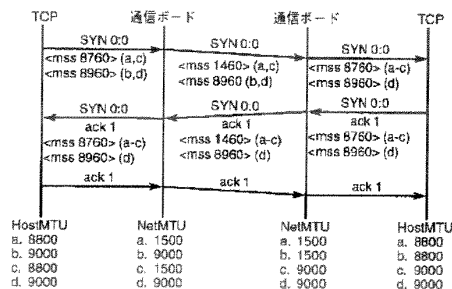
【図1】

送受信の流れ



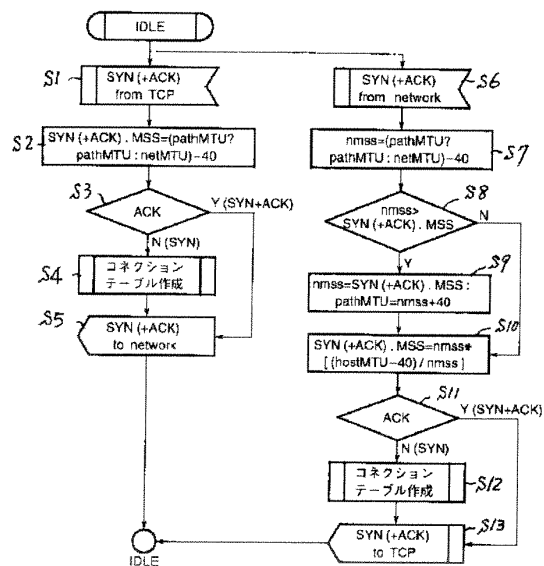
【図3】

コネクション確立時の通信シーケンス例



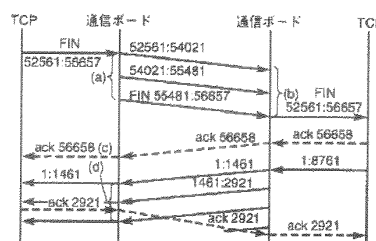
【図2】

コネクション確立時の処理フロー



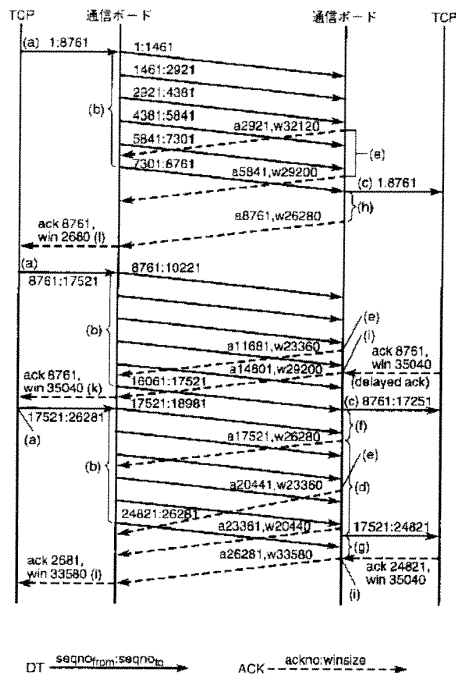
【図6】

コネクション終了時の通信シーケンス例



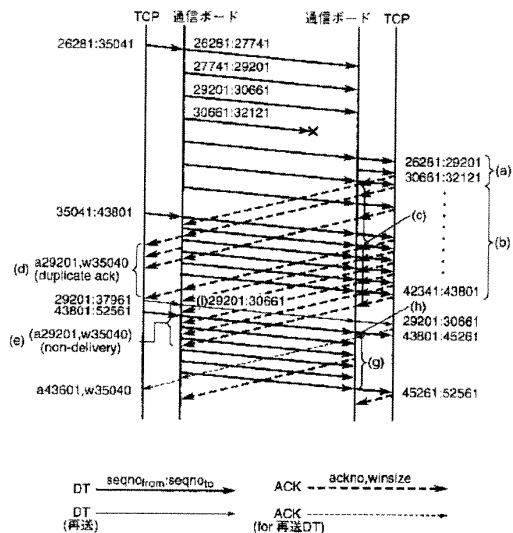
【图 4】

データ転送時の通信シーケンス例



【图5】

再送時の通信シーケンス例



フロントページの続き

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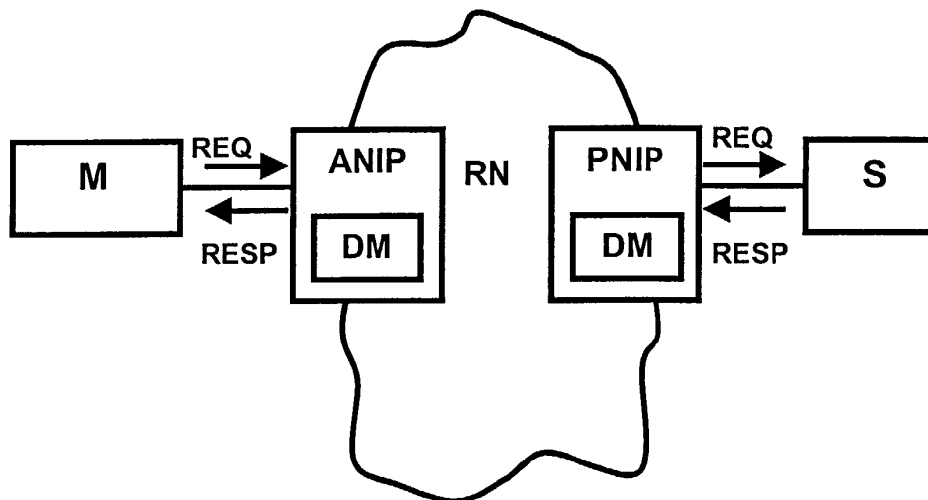
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(54) Title: INTEGRATED CIRCUIT AND METHOD FOR EXCHANGING DATA



(57) Abstract: An integrated circuit comprising a plurality of processing modules M, S and a network N; RN arranged for providing at least one connection between a first and at least one second module M, S is provided. Said connection supports transactions comprising outgoing messages from the first module to the second modules and return messages from the second modules to the first module. Said integrated circuit comprises at least one dropping means DM for dropping data exchanged by said first and second module M, S. Accordingly, an alternative scheme for transaction completion is provided, where full and immediate transaction completion is merely applied for certain cases. The invention is based on the idea to allow the dropping of data in certain cases.

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Integrated circuit and method for exchanging data

FIELD OF THE INVENTION

The invention relates to an integrated circuit having a plurality of processing modules and a network arranged for providing connections between processing modules and a method for exchanging messages in such an integrated circuit.

5

BACKGROUND OF THE INVENTION

Systems on silicon show a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions. This is enabled by the increasing density with which components can be integrated on an integrated circuit. At the same time the clock speed at which circuits are operated tends to increase too. The higher clock speed in combination with the increased density of components has reduced the area which can operate synchronously within the same clock domain. This has created the need for a modular approach. According to such an approach the processing system comprises a plurality of relatively independent, complex modules. In conventional processing systems the systems modules usually communicate to each other via a bus. As the number of modules increases however, this way of communication is no longer practical for the following reasons. On the one hand the large number of modules forms a too high bus load. On the other hand the bus forms a communication bottleneck as it enables only one device to send data to the bus. A communication network forms an effective way to overcome these disadvantages.

Networks on chip (NoC) have received considerable attention recently as a solution to the interconnect problem in highly-complex chips. The reason is twofold. First, NoCs help resolve the electrical problems in new deep-submicron technologies, as they structure and manage global wires. At the same time they share wires, lowering their number and increasing their utilization. NoCs can also be energy efficient and reliable and are scalable compared to buses. Second, NoCs also decouple computation from communication, which is essential in managing the design of billion-transistor chips. NoCs achieve this decoupling because they are traditionally designed using protocol stacks, which provide well-defined interfaces separating communication service usage from service implementation.

Using networks for on-chip communication when designing systems on chip (SoC), however, raises a number of new issues that must be taken into account. This is because, in contrast to existing on-chip interconnects (e.g., buses, switches, or point-to-point wires), where the communicating modules are directly connected, in a NoC the modules
5 communicate remotely via network nodes. As a result, interconnect arbitration changes from centralized to distributed, and issues like out-of order transactions, higher latencies, and end-to-end flow control must be handled either by the intellectual property block (IP) or by the network.

Most of these topics have been already the subject of research in the field of
10 local and wide area networks (computer networks) and as an interconnect for parallel machine interconnect networks. Both are very much related to on-chip networks, and many of the results in those fields are also applicable on chip. However, NoC's premises are different from off-chip networks, and, therefore, most of the network design choices must be reevaluated. On-chip networks have different properties (e.g., tighter link synchronization)
15 and constraints (e.g., higher memory cost) leading to different design choices, which ultimately affect the network services.

NoCs differ from off-chip networks mainly in their constraints and synchronization. Typically, resource constraints are tighter on chip than off chip. Storage (i.e., memory) and computation resources are relatively more expensive, whereas the number
20 of point-to-point links is larger on chip than off chip. Storage is expensive, because general-purpose on-chip memory, such as RAMs, occupy a large area. Having the memory distributed in the network components in relatively small sizes is even worse, as the overhead area in the memory then becomes dominant.

For on-chip networks computation too comes at a relatively high cost
25 compared to off-chip networks. An off-chip network interface usually contains a dedicated processor to implement the protocol stack up to network layer or even higher, to relieve the host processor from the communication processing. Including a dedicated processor in a network interface is not feasible on chip, as the size of the network interface will become comparable to or larger than the IP to be connected to the network. Moreover, running the
30 protocol stack on the IP itself may also be not feasible, because often these IPs have one dedicated function only, and do not have the capabilities to run a network protocol stack.

The number of wires and pins to connect network components is an order of magnitude larger on chip than off chip. If they are not used massively for other purposes than

NoC communication, they allow wide point-to-point interconnects (e.g., 300-bit links). This is not possible off-chip, where links are relatively narrower: 8-16 bits.

On-chip wires are also relatively shorter than off chip allowing a much tighter synchronization than off chip. This allows a reduction in the buffer space in the routers
5 because the communication can be done at a smaller granularity. In the current semiconductor technologies, wires are also fast and reliable, which allows simpler link-layer protocols (e.g., no need for error correction, or retransmission). This also compensates for the lack of memory and computational resources.

Reliable communication: A consequence of the tight on-chip resource
10 constraints is that the network components (i.e., routers and network interfaces) must be fairly simple to minimize computation and memory requirements. Luckily, on-chip wires provide a reliable communication medium, which can help to avoid the considerable overhead incurred by off-chip networks for providing reliable communication. Data integrity can be provided at low cost at the data link layer.

15 Deadlock: Computer network topologies have generally an irregular (possibly dynamic) structure, which can introduce buffer cycles. Deadlock can also be avoided, for example, by introducing constraints either in the topology or routing. Fat-tree topologies have already been considered for NoCs, where deadlock is avoided by bouncing back packets in the network in case of buffer overflow. Tile-based approaches to system design use mesh or
20 torus network topologies, where deadlock can be avoided using, for example, a turn-model routing algorithm. Deadlock is mainly caused by cycles in the buffers. To avoid deadlock, routing must be cycle-free, because of its lower cost in achieving reliable communication. A second cause of deadlock are atomic chains of transactions. The reason is that while a module is locked, the queues storing transactions may get filled with transactions outside the
25 atomic transaction chain, blocking the access of the transaction in the chain to reach the locked module. If atomic transaction chains must be implemented (to be compatible with processors allowing this, such as MIPS), the network nodes should be able to filter the transactions in the atomic chain.

Network flow control and buffering strategy: Network flow control and
30 buffering strategy have a direct impact on the memory utilization in the network. Wormhole routing requires only a flit buffer (per queue) in the router, whereas store-and-forward and virtual-cut-through routing require at least the buffer space to accommodate a packet. Consequently, on chip, wormhole routing may be preferred over virtual-cut-through or store-and-forward routing. Similarly, input queuing may be a lower memory-cost alternative to

virtual-output-queuing or output-queuing buffering strategies, because it has fewer queues. Dedicated (lower cost) FIFO memory structures also enable on-chip usage of virtual-cut-through routing or virtual output queuing for a better performance. However, using virtual-cut-through routing and virtual output queuing at the same time is still too costly.

5 Time-related guarantees: Off-chip networks typically use packet switching and offer best-effort services. Contention can occur at each network node, making latency guarantees very hard to offer. Throughput guarantees can still be offered using schemes such as rate-based switching or deadline-based packet switching, but with high buffering costs. An alternative to provide such time-related guarantees is to use time-division multiple access
10 (TDMA) circuits, where every circuit is dedicated to a network connection. Circuits provide guarantees at a relatively low memory and computation cost. Network resource utilization is increased when the network architecture allows any left-over guaranteed bandwidth to be used by best-effort communication.

 Introducing networks as on-chip interconnects radically changes the
15 communication when compared to direct interconnects, such as buses or switches. This is because of the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes. This is in contrast with the prevalent existing interconnects (i.e., buses) where modules are directly connected. The implications of this change reside in the arbitration (which must change from centralized to distributed), and
20 in the communication properties (e.g., ordering, or flow control).

 An outline the differences of NoCs and buses will be given below. We refer mainly to buses as direct interconnects, because currently they are the most used on-chip interconnect. Most of the bus characteristics also hold for other direct interconnects (e.g., switches). Multilevel buses are a hybrid between buses and NoCs. For our purposes,
25 depending on the functionality of the bridges, multilevel buses either behave like simple buses or like NoCs. The programming model of a bus typically consists of load and store operations which are implemented as a sequence of primitive bus transactions. Bus interfaces typically have dedicated groups of wires for command, address, write data, and read data. A bus is a resource shared by multiple IPs. Therefore, before using it, IPs must go
30 through an arbitration phase, where they request access to the bus, and block until the bus is granted to them.

 A bus transaction involves a request and possibly a response. Modules issuing requests are called masters, and those serving requests are called slaves. If there is a single arbitration for a pair of request-response, the bus is called non-split. In this case, the bus

remains allocated to the master of the transaction until the response is delivered, even when this takes a long time. Alternatively, in a split bus, the bus is released after the request to allow transactions from different masters to be initiated. However, a new arbitration must be performed for the response such that the slave can access the bus.

5 For both split and non-split buses, both communication parties have direct and immediate access to the status of the transaction. In contrast, network transactions are one-way transfers from an output buffer at the source to an input buffer at the destination that causes some action at the destination, the occurrence of which is not visible at the source. The effects of a network transaction are observable only through additional transactions. A request-response type of operation is still possible, but requires at least two distinct network transactions. Thus, a bus-like transaction in a NoC will essentially be a split transaction.

10 In addition, in a network at each layer in the protocol stack, control information must be supplied together with the data (e.g., packet type, network address, or packet size). This control information is organized as an envelope around the data. That is, first a header is sent, followed by the actual data (payload), followed possibly by a trailer. Multiple such envelopes may be provided for the same data, each carrying the corresponding control information for each layer in the network protocol stack.

Buffering and Flow Control: Buffering data of a master (output buffering) is used both for buses and NoCs to decouple computation from communication. However, for 20 NoCs output buffering is also needed to marshal data, which consists of (a) (optionally) splitting the outgoing data in smaller packets which are transported by the network, and (b) adding control information for the network around the data (packet header). To avoid output buffer overflow the master must not initiate transactions that generate more data than the currently available space. Similarly to output buffering, input buffering is also used to 25 decouple computation from communication. In a NoC, input buffering is also required to unmarshal data.

In addition, flow control for input buffers differs for buses and NoCs. For buses, the source and destination are directly linked, and, destination can therefore signal directly to a source that it cannot accept data. This information can even be available to the 30 arbiter, such that the bus is not granted to a transaction trying to write to a full buffer.

In a NoC, however, the destination of a transaction cannot signal directly to a source that its input buffer is full. Consequently, transactions to a destination can be started, possibly from multiple sources, after the destination's input buffer has filled up. If an input buffer is full, additional incoming transitions are not accepted, and stored in the network.

However, this approach can easily lead to network congestion, back pressure and deadlock, as the data could be eventually stored all the way to the sources, blocking the links in between.

When a master needs to send data to a slave, the master can not be stopped directly by the slave when its buffer space is full. In order to avoid a buffer overflow there must be some kind of agreement between the master and the slave in which the slave reserves buffer space for that master and keeps the master informed of the available buffer space, i.e. when more buffer space has been consumed. This scheme will however generate extra traffic in the network and may lead to a non-efficient network resource utilization, e.g. because of a pessimistic buffer allocation.

To avoid input buffer overflow connections can be used, together with end-to-end flow control. At connection set up between a master and one or more slaves, buffer space is allocated at the network interfaces of the slaves, and the network interface of the master is assigned credits reflecting the amount of buffer space at the slaves. The master can only send data when it has enough credits for the destination slave(s). The slaves grant credits to the master when they consume data.

End-to-end flow control is implemented between a master and a slave to ensure that no data is dropped in the connection between the modules. The data arrive in the requested order and in time, therefore no contention or "traffic jam" will occur in the network. However, end-to-end flow control is expensive to implement.

SUMMARY OF THE INVENTION

It is an object of the invention to provide an integrated circuit and a method for exchanging messages in an integrated circuit which ensures transaction completion at lower cost.

This object is achieved by an integrated circuit according to claim 1 and a method for exchanging messages according to claim 9.

Therefore, an integrated circuit comprising a plurality of processing modules M, S and a network N; RN arranged for providing at least one connection between a first and at least one second module M, S is provided. Said connection supports transactions comprising outgoing messages from the first module to the second modules and return messages from the second modules to the first module. Said integrated circuit comprises at least one dropping means DM for dropping data exchanged by said first and second modules M, S.

Accordingly, an alternative scheme for transaction completion is provided, where full and immediate transaction completion is merely applied for certain cases.

The invention is based on the idea to allow the dropping of data in certain cases.

5 According to an aspect of the invention, an integrated circuit comprising at least one interface means ANIP, PNIP for managing the interface between a module M, S and the network N, RN is provided, wherein said interface means ANIP, PNIP comprises a first dropping means DM for dropping data. The dropping of data and therefore the transaction completion can be controlled by the interface means.

10 According to a further aspect of the invention, an integrated circuit is provided with a network N, RN comprised of a plurality of network routers for forwarding data without dropping data, i.e. only the interface means are allowed to drop data.

 According to still a further aspect of the invention, said dropping means DM are adapted to create an error message if data is dropped. Therefore, a source of said data is
15 informed of the dropping of the data, so that it can re-send said data later on, which will be part of another transaction.

 According to a further aspect of the invention said dropping means DM are adapted to send said error message to a first dropping means DM. Hence, error messages are send to the dropping means in the interface means.

20 According to still a further aspect of the invention, said dropping means DM are adapted to send said error message to said first module M. The error messages are directly send to the first module.

 According to a further aspect of the invention, said interface means ANIP, PNIP is adapted to store received error messages. It is therefore possible for the interface
25 means to keep track of the completion of transactions.

 According to a further aspect of the invention, an interface means ANIP associated to the first module M is adapted not to drop error messages.

 The invention also relates to a method for exchanging messages in an integrated circuit comprising a plurality of modules. The messages between the modules are
30 being exchanged over connections via a network., wherein data exchanged by said first and second module M, S can be dropped.

 The invention also relates to a method for exchanging messages in an integrated circuit comprising a plurality of modules as described above.

 Further aspects of the invention are described in the dependent claims.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiment(s) described hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

- 5 Fig. 1 shows a System on chip according to a first embodiment, and
 Fig. 2 shows a System on chip according to a second embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

- The following embodiments relate to systems on chip, i.e. a plurality of
10 modules on the same chip communicate with each other via some kind of interconnect. The
 interconnect is embodied as a network on chip NOC. The network on chip may include
 wires, bus, time-division multiplexing, switch, and/or routers within a network. At the
 transport layer of said network, the communication between the modules are performed over
 connections. A connection is considered as a set of channels, each having a set of connection
15 properties, between a first module and at least one second module. For a connection between
 a first module and a single second module, the connection comprises two channel, namely
 one from the first module to the second channel, i.e. the request channel, and a second from
 the second to the first module, i.e. the response channel. The request channel is reserved for
 data and messages from the first to the second, while the response channel is reserved for
20 data and messages from the second to the first module. However, if the connection involves
 one first and N second modules, $2*N$ channels are provided. The connection properties may
 include ordering (data transport in order), flow control (a remote buffer is reserved for a
 connection, and a data producer will be allowed to send data only when it is guaranteed that
 space is available for the produced data), throughput (a lower bound on throughput is
25 guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data),
 transmission termination, transaction completion, data correctness, or data delivery.

- Fig. 1 shows a System on chip according to a first embodiment. The system
 comprises a master module M, a slave modules S. Although just one slave module is shown
 in Fig. 1, the system may comprise a plurality of slave modules. Each module is connected to
30 a network N via a network interface NI, respectively. The network interfaces NI are used as
 interfaces between the master and slave module M, S and the network N. The network
 interfaces NI are provided to manage the communication of the respective modules and the
 network N, so that the modules can perform their dedicated operation without having to deal

with the communication with the network or other modules. Each network interfaces comprises a buffer for buffering data and messages.

The communication according to this embodiment is transaction based. These transactions consist of a request and possibly a response. Typically, a request is initiated by the master M (a), send to the slave S via the two network interfaces NI and the network N (b). The slave S may respond (c) and a response is send back to the master M (d). However, some transactions may exist, where no response from the slave S is necessary. In such a case the transaction is completed when it has been executed by the slave S. A transaction with a response is completed when the response has been delivered to the master M. Therefore, the master can only detect the completion of the transaction if it receives a response. As long as a flow control is implemented in the network, the deliverance of the request as well as the response are guaranteed and therefore transaction completeness is guaranteed. However, if no end-to-end flow control is implemented both the request and the response may be dropped and hence no transaction completion is guaranteed.

Fig. 2 shows a system on chip according to a second embodiment. The system comprises two modules, namely a master M and a slave S module, a router network RN, and two network interfaces ANIP, PNIP between the modules and the router network RN. The network interfaces provide two network interface ports NIP (one request and one response port) through which the modules communicate with the router network RN or other modules via the router network RN. The network interface associated to the master module M is called the active network interface ports ANIP and the network interface associated to the slave module S is called the passive network interface ports PNIP. The communication between the master module M and the slave module s is based on request-response transactions, where the master M initiates a transaction by placing a request, possibly with some data or required connection properties. The request REQ is delivered to the slave S via the active network interface port ANIP, the network RN and the passive network interface port PNIP. The request is executed by the slave module S and data is returned as a response RESP if necessary or required. This response RESP may include data and/or acknowledgement for the master M.

Here, it is assumed, that the network N, RN, i.e. the routers, do not drop data. The active network interface ANIP as well as the passive network interface PNIP comprise a dropping manager DM, respectively. These dropping managers DM are responsible for the dropping of data or messages, i.e. only the network interfaces are able to drop data or messages. In particular, requests can only be dropped by the active network interface ports

ANIP, while responses can only be dropped by the passive network interface ports PNIP. Possible scenarios include: (a) the oldest message is dropped (milk policy), or (b) the newest message is dropped (wine policy).

A transaction can be composed from the following messages:

- 5 - A command message (CMD) is sent by the ANIP, and describes the action to be executed at the slave connected to the PNIP. Examples of commands are read, write, test and set, and flush. Commands are the only messages that are compulsory in a transaction. For NIPs that allow only a single command with no parameters (e.g., fixed-size address-less write), we assume the command message still exists, even if it is implicit (i.e., not explicitly
10 sent by the IP).
- An out data message (OUTDATA) is sent by the ANIP following a command that requires data to be executed (e.g., write, multicast, and test-and-set).
- A return data message (RETDATA) is sent by a PNIP as a consequence of a transaction execution that produces data (e.g., read, and test-and-set).
- 15 - A completion acknowledgment message (RETSTAT) is an optional message which is returned by PNIP when a command has been completed. It may signal either a successful completion or an error. For transactions including both RETDATA and RETSTAT the two messages can be combined in a single message for efficiency. However, conceptually, they exist both: RETSTAT to signal the presence of data or an error, and
20 RETDATA to carry the data.

Messages composing a transaction are divided in outgoing messages, namely CMD and OUTDATA, and response messages, namely RETDATA, RETSTAT. Within a transaction, CMD precedes all other messages, and RETDATA precedes RETSTAT if present. These rules apply both between master and ANIP, and PNIP and slave.

- 25 A transaction without a response (e.g. a posted write) is said to be complete when it has been executed by the slave. As there is no response message to the master, no guarantee regarding transaction completion can be given. A transaction with a response (e.g. an acknowledged write) is said to be complete when a RETSTAT message is received from the ANIP. Recall that when data is received as a response (RETDATA), a RETSTAT
30 (possibly implicit) is also received to validate the data. The transaction may either be executed successfully, in which case a success RETSTAT is returned, fail in its execution at the slave, and then an execution error RETSTAT is returned, or fail because of buffer overflow in a connection with no flow control, and then it reports an overflow error. We

assume that when a slave accepts a CMD requesting a response, the slave S always generates the response.

The dropping manager DM may drop data in case of buffer overflow. All of CMD, OUTDATA, and RETDATA may be dropped. To guarantee transaction completion, RETSTAT is not allowed to be dropped. Consequently, in the ANIPs enough buffer space must be provided to accommodate RETSTAT messages for all outstanding transactions. This is enforced by bounding the number of outstanding transactions.

For the case of several slaves S in the above system, return message or response messages could be combined as follows. If each of write transaction (initiated by the master M) has been successfully executed by all slaves S, all will return RETSTAT=RETOK messages, which can be combined by the ANIP in a single message to be delivered to the master.

If the write transaction has been successfully executed only by some slaves, there will be a mix of RETSTATs (RETOK and RETERROR). They can either be combined into:

- a) a single RETSTAT=RETERERROR, to specify that an error occurred, or
- b) a single RETSTAT, but a larger one, more descriptive, encoding where there have been errors.

All RETSTATs can be bundled together in a single RETSTAT for the master, or <slave identifiers,error code> pairs can be bundled to form a single RETSTAT for the master.

If the connection has no flow control, messages can be dropped by the dropping managers DM, resulting also in RETSTAT=RETLOST messages. Again, combinations as those above can be made.

The master module M should always receive a response to a transaction. This is achieved by the dropping managers DM. If the dropping manager DM in the passive network interface ports PNIP drops data or messages possibly because of a buffer overflow, it always returns a FAIL/ERROR message to the ANIP. This return status (RETSTAT) message will never be dropped by the dropping manager of the active network interface ports ANIP because the ANIP that initiated the transaction will reserve space for return messages of every transaction that it initiates. This combination of reserving space and generating an error message whenever a message is dropped is a way to introduce flow control. Preferably, the RETSTAT message is generated by the interface of the slave module, although alternatively it could be generated at the intermediary network nodes too.

By implementing the above dropping scheme, transaction completion is guaranteed, i.e. it is always known whether an initiated transaction:

- a) was delivered and executed successfully at the slave (RETSTAT=OK produced by the slave),
- 5 b) was never delivered at the slave (RETSTAT=REQLOST produced by the PNIP and returned to the ANIP),
- c) was delivered at the slave, but not successfully executed (RETSTAT=ERROR produced by the slave), or
- d) was delivered and executed successfully at the slave but the response message
- 10 was dropped (RETSTAT=RETLOST produced by the ANIP and delivered to the master M).

This is achieved by either not dropping messages (flow-controlled connection), in this case RETSTAT is either OK or ERROR, or by allowing messages to be dropped (on a connection without flow control), but generating a RETSTAT (REQLOST or RETLOST) whenever the message is dropped, or a RETOK or RETERROR as usual when

15 the message is not dropped.

It is essential however, never to drop RETSTATs, because this completes the transaction. This is realized in that a buffer for the RETSTAT is located at the master's ANIP. The latter reserves space for RETSTATs when initiating transactions, and bounds the number of outstanding transactions (for finite sized RETSTAT buffers).

20 The flow control on the outgoing and return connections is in principle independent. Thus, for outgoing flow control & return flow control, the RETSTAT message is according to a) or c) above. In case of outgoing flow control & no return flow control, the RETSTAT message is a) or c) or d) above. In case of no outgoing flow control & return flow control, the RETSTAT message is a) or b) or c) above.

25 For the above system, connections can be classified as follows:

- A simple connection is a connection between one ANIP and one PNIP.
- A narrowcast connection is a connection between one ANIP and one or more PNIPs, in which each transaction that the ANIP initiates is executed by exactly one PNIP. An example of the narrowcast connection, where the ANIP performs transactions on an address space which is mapped on two memory modules. Depending on the transaction
- 30 address, a transaction is executed on only one of these two memories.
- A multicast connection is a connection between one ANIP and one or more PNIPs, in which the sent messages are duplicated and each PNIP receives a copy of those messages. In a multicast connection no return messages are currently allowed, because of the

large traffic they generate (i.e., one response per destination). It could also increase the complexity in the ANIP because individual responses from PNIPs must be merged into a single response for the ANIP. This requires buffer space and/or additional computation for the merging itself.

5 Connecting properties that can be configured for a connection are as follows: guaranteed message integrity, guaranteed transaction completion, various transaction orderings, guaranteed throughput, bounded latency and jitter, and connection flow control.

 The modules as described in Fig. 1 and 2 can be so-called intellectual property blocks IPs (computation elements or memories, but not interconnection elements) that
10 interact with network at said network interfaces NI. NIs provide NI ports NIP through which the communication services are accessed. A NI can have several NIPs to which one or more IPs can be connected. Similarly, an IP can be connected to more than one NI and NIP.

 The communication over the network is performed by the network interfaces on connections, i.e. the master and the slave module are invisible to the network. Connections
15 are introduced to describe and identify communication with different properties, such as guaranteed throughput, bounded latency and jitter, ordered delivery, or flow control. The connections according to the embodiments of the invention must be first created or established with the desired properties before being used. This may result in resource
20 reservations inside the network (e.g., buffer space, or percentage of the link usage per time unit). If the requested resources are not available, the network RN will refuse the request. After usage, connections are closed, which leads to freeing the resources occupied by that connection.

 At both ANIP and PNIPs, outgoing messages belonging to different transactions on the same connection are allowed to be interleaved. For example, two write
25 commands can be issued, and only afterwards their data. If the order of OUTDATA messages differs from the order of CMD messages, transaction identifiers must be introduced to associate OUTDATAs with their corresponding CMD.

 Outgoing messages can be delivered by the PNIPs to the slaves (see b) as follows:

- 30 - Unordered, which imposes no order on the delivery of the outgoing messages of different transactions at the PNIPs.
- Ordered locally, where transactions must be delivered to each PNIP in the order they were sent (a), but no order is imposed across PNIPs. Locally-ordered delivery of

the outgoing messages can be provided either by an ordered data transportation, or by reordering outgoing messages at the PNIP.

- Ordered globally, where transactions must be delivered in the order they were sent, across all PNIPs of the connection. Globally-ordered delivery of the outgoing part of transactions require a costly synchronization mechanism.

Transaction response messages can be delivered by the slaves to the PNIPs (c) as Ordered, when RETDATA and RETSTAT messages are returned in the same order as the CMDs were delivered to the slave (b), or as Unordered, otherwise. When responses are unordered, there has to be a mechanism to identify the transaction to which a response belongs. This is usually done using tags attached to messages for transaction identifications (similar to tags in VCI).

Response messages can be delivered by the ANIP to the master (see d) as follows:

- Unordered, which imposes no order on the delivery of responses. Here, also, tags must be used to associate responses with their corresponding CMDs.

- Ordered locally, where RETDATA and RETSTAT messages of transactions for a single slave are delivered in the order the original CMDs were presented by the master to the ANIP. Note that there is no ordering imposed for transactions to different slaves within the same connection.

- Globally ordered, where all responses in a connection are delivered to the master in the same order as the original CMDs. When transactions are pipelined on a connection, then globally-ordered delivery of responses requires reordering at the ANIP.

All $3 \times 2 \times 3 = 18$ combinations between the above orderings are possible. Out of these, the following two are defined. An unordered connection is a connection in which no ordering is assumed in any part of the transactions. As a result, the responses must be tagged to be able identify to which transaction they belong. Implementing unordered connections has low cost, however, they may be harder to use, and introduce the overhead of tagging.

In an alternative embodiment, the dropping means as described above may be implemented in some of the routers of the network, so that these routers are allowed to drop data. However, in such a case they must follow the above scheme and in particular create the above error messages.

In another alternative embodiment of the invention, the transaction completion can be implemented in systems which are not connection based, as such a system is equivalent to a system with a single connection

It should be noted that the above-mentioned embodiments illustrate rather than
5 limit the invention, and that those skilled in the art will be able to design many alternative
embodiments without departing from the scope of the appended claims. In the claims, any
reference signs placed between parentheses shall not be construed as limiting the claim. The
word "comprising" does not exclude the presence of elements or steps other than those listed
in a claim. The word "a" or "an" preceding an element does not exclude the presence of a
10 plurality of such elements. In the device claim enumerating several means, several of these
means can be embodied by one and the same item of hardware. The mere fact that certain
measures are recited in mutually different dependent claims does not indicate that a
combination of these measures cannot be used to advantage.

Furthermore, any reference signs in the claims shall not be construed as
15 limiting the scope of the claims.

CLAIMS:

1. Integrated circuit comprising a plurality of processing modules (M, S) and a network (N; RN) arranged for providing at least one connection between a first and at least one second module (M, S),
wherein said connection supports transactions comprising outgoing messages
5 from the first module to the second modules and return messages from the second modules to the first module, the integrated circuit comprising at least one dropping means (DM) for dropping data exchanged by said first and second module (M, S).
2. Integrated circuit according to claim 1, further comprising:
10 at least one interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN),
wherein said interface means (ANIP, PNIP) comprises a first dropping means (DM) for dropping data.
- 15 3. Integrated circuit according to claim 2, wherein
said network (N, RN) comprises a plurality of network routers for forwarding data without dropping data.
4. Integrated circuit according to claim 2 or 3, wherein
20 said dropping means (DM) are adapted to create an error message if data is dropped.
5. Integrated circuit according to claim 4, wherein
said dropping means (DM) are adapted to send said error message to a first
25 dropping means (DM).
6. Integrated circuit according to claim 4, wherein
said dropping means (DM) are adapted to send said error message to said first module (M).

7. Integrated circuit according to claim 5 or 6, wherein
said interface means (ANIP, PNIP) is adapted to store received error
messages.
- 5 8. Integrated circuit according to claim 7, wherein
an interface means (ANIP) associated to the first module (M) is adapted not to
drop error messages.
- 10 9. Method for exchanging messages in an integrated circuit comprising a
plurality of modules, the messages between the modules being exchanged over connections
via a network,
wherein said connection supports transactions comprising outgoing messages
from the first module to the second module and return messages from the second module to
15 the first module, wherein data exchanged by said first and second module (M, S) can be
dropped.

1/1

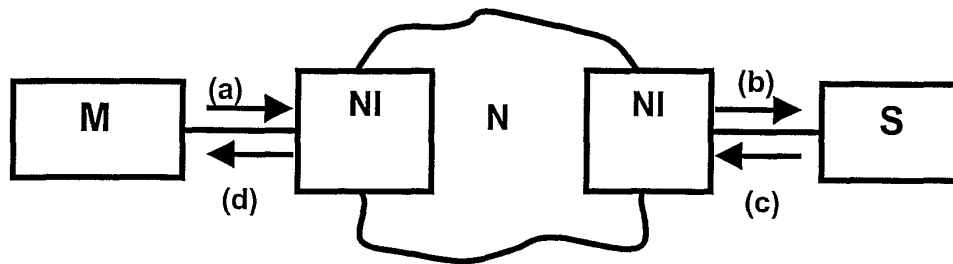


FIG.1

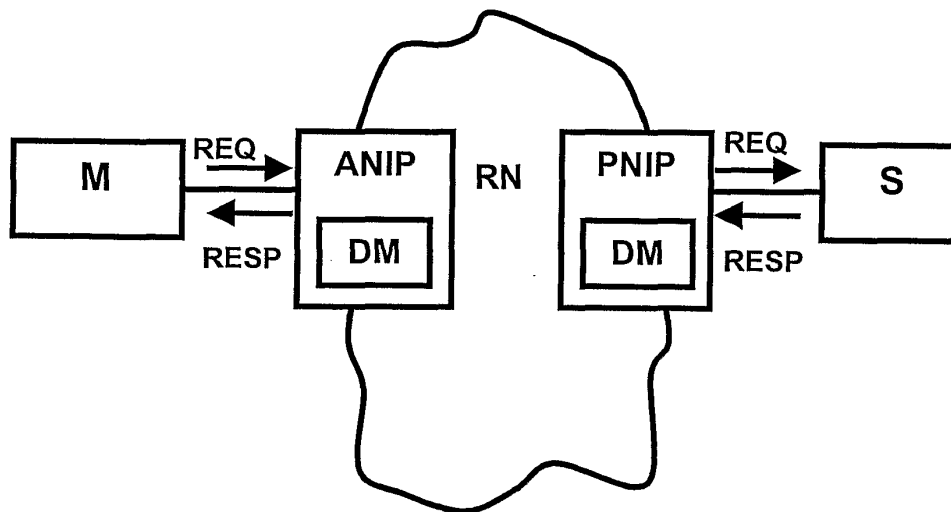


FIG.2

Electronic Patent Application Fee Transmittal				
Application Number:		11569083		
Filing Date:		14-Nov-2006		
Title of Invention:		INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS		
First Named Inventor/Applicant Name:		Andrei Radulescu		
Filer:		Michael E. Belk/Elissa DeLuccy		
Attorney Docket Number:		NL040529US1		
Filed as Large Entity				
U.S. National Stage under 35 USC 371 Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	1801	1	810	810
Total in USD (\$)				810

Electronic Acknowledgement Receipt	
EFS ID:	10664215
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	NL040529US1
Receipt Date:	04-AUG-2011
Filing Date:	14-NOV-2006
Time Stamp:	10:06:22
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$810
RAM confirmation Number	9092
Deposit Account	141270
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. 1.492 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

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Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	2004P01041WOUS_RCE.pdf	697429	no	3
			53c41f2bbba72ce571656d168e0cd51cf2f2df3		
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2004P01041WOUS_IDS.pdf	612102	no	4
			712be245d3be1fb8040985057ffe2b29f4c81c8f		
Warnings:					
Information:					
3	Foreign Reference	JP7123118A.pdf	1152433	no	10
			5bc40c6ce880956b80c95a4899b0b7f93803fe4c		
Warnings:					
Information:					
4	Foreign Reference	JP2000209652A.pdf	2059881	no	16
			dcc1c7d115050ab6a4f36318a15759b1f0a008f1		
Warnings:					
Information:					
5	Foreign Reference	JP2002084289A.pdf	1738324	no	11
			05d428825c28d881894702571a522bd32d0c6ad4		
Warnings:					
Information:					
6	Foreign Reference	WO2004034173A2.pdf	1091716	no	20
			e1517cb8f3d770d914d953e33fc02184f4e35968		
Warnings:					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	30864	no	2
			9f7898601e1247a23b2d627d06eebd47ca8c1e37		
Warnings:					
Information:					
Total Files Size (in bytes):			7382749		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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NOTICE OF ALLOWANCE AND FEE(S) DUE

24737 7590 08/26/2011
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER

ALSIP, MICHAEL

ART UNIT

PAPER NUMBER

2186

DATE MAILED: 08/26/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	2004P01041WOUS	4172

TITLE OF INVENTION: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/28/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24737 7590 08/26/2011

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/569,083	11/14/2006	Andrei Radulescu	2004P01041WOUS	4172
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TITLE OF INVENTION: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/28/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
ALSIP, MICHAEL	2186	711-118000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	11/14/2006	Andrei Radulescu	2004P01041WOUS	4172
24737	7590	08/26/2011	EXAMINER	
PHILIPS INTELLECTUAL PROPERTY & STANDARDS			ALSIP, MICHAEL	
P.O. BOX 3001			ART UNIT	
BRIARCLIFF MANOR, NY 10510			PAPER NUMBER	

2186

DATE MAILED: 08/26/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 527 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 527 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	11/569,083	RADULESCU ET AL.	
	Examiner	Art Unit	
	MICHAEL ALSIP	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the IDS filed 8/4/2011.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1,3,4 and 7-24.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of the:

1. ☒ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.

(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>8/4/2011</u> 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date ____. 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
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/Michael Alsip/ Primary Examiner, Art Unit 2186	
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DETAILED ACTION

Allowable Subject Matter

1. **Claims 1, 3-4 and 7-24** are allowed.
2. The IDS filed on 8/4/2011 has been considered by the Examiner.
3. The following is an examiner's statement of reasons for allowance, which is the same reasoning as given in the allowance dated 5/11/2011 due to the references submitted in the IDS not teaching the previously allowed subject matter. The Applicant has incorporated the subject matter of now cancelled **claim 6**, previously indicated as allowable in the final office action dated 2/24/2011, into each independent claim and therefore the case is now in condition for allowance. As stated in the previous office action dated 2/24/2011, the claim language of now cancelled **claim 6**, describes a process/function of determining an optimal moment for sending data in said first or second wrapper according to: "communication properties of the communication between the master and slave" and then further claims that "the communication properties" include the claimed extensive list of properties. The prior art found alone or in combination does not teach or suggest that the communication properties of the communication between the master and slave used to determine the optimal moment for sending data, incorporate the claimed list of communication properties to make that determination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

Application/Control Number: **Error! Unknown document property name.**

Page 3

Art Unit: **Error! Unknown document property name.**

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ALSIP whose telephone number is (571)270-1182. The examiner can normally be reached on Monday through Thursday 9:00AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael Alsip
Examiner
Art Unit 2186

/Michael Alsip/
Examiner, Art Unit 2186

Application/Control Number: **Error! Unknown document property name.**

Page 4

Art Unit: **Error! Unknown document property name.**

August 23, 2011

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11569083	
	Filing Date		2006-11-14	
	First Named Inventor	Andrei Radulescu		
	Art Unit	2186		
	Examiner Name	Michael Alsip		
	Attorney Docket Number	2004P01041WOUS		

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	7769893	B2	2010-03-03	GOOSSENS	ALSO PUBLISHED AS WO2004034173A2		
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1							
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1	2004034173	WO	A2	2004-04-22	RADULESCU ET AL	ALSO PUBLISHED AS US7769893	☐
	2	200209652	JP	A	2000-07-28	FUKUSHIMA ET AL		☐
	3	2002084289	JP	A	2002-03-22	HASEGAWA ET AL		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11569083	
	Filing Date		2006-11-14	
	First Named Inventor	Andrei Radulescu		
	Art Unit	2186		
	Examiner Name	Michael Alsip		
	Attorney Docket Number	2004P01041WOUS		

	4	7123118A	JP	A	1995-05-12	GOTO		☐
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If you wish to add additional Foreign Patent Document citation information please click the Add button **Add**

NON-PATENT LITERATURE DOCUMENTS							Remove
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
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EXAMINER SIGNATURE			
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Examiner Signature	/Michael Alsip/	Date Considered	08/23/2011
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Issue Classification 	Application/Control No. 11569083	Applicant(s)/Patent Under Reexamination RADULESCU ET AL.
	Examiner MICHAEL ALSIP	Art Unit 2186

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
711		118				G	0	6	F	12 / 00								
CROSS REFERENCE(S)						G	0	6	F	13 / 00								
						G	0	6	F	13 / 28								
						G	0	6	F	3 / 00								
711	141					G	0	6	F	5 / 00								
710	57	100																

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	14	17												
	2	15	18												
2	3	16	19												
3	4	17	20												
	5	18	21												
	6	19	22												
4	7	20	23												
5	8	21	24												
6	9														
7	10														
8	11														
9	12														
10	13														
11	14														
12	15														
13	16														

		Total Claims Allowed:	
		21	
(Assistant Examiner) /MICHAEL ALSIP/ Examiner, Art Unit 2186	(Date) 05/06/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

<i>Search Notes</i> 	Application/Control No. 11569083	Applicant(s)/Patent Under Reexamination RADULESCU ET AL.
	Examiner MICHAEL ALSIP	Art Unit 2186

SEARCHED			
Class	Subclass	Date	Examiner
711	118 limited w/ text	5/5/2011	MA
711	141 limited w/ text	5/5/2011	MA
710	57 limited w/ text	5/5/2011	MA
710	100 limited w/ text	5/5/2011	MA

SEARCH NOTES		
Search Notes	Date	Examiner
inventor name and assignee search in eDAN and EAST	5/5/2011	MA
class/subclass and keyword search in EAST	5/5/2011	MA
internet search using same keywords as in the EAST search	5/5/2011	MA

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	see attached EAST interference search	5/5/2011	MA

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

24737 7590 08/26/2011
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/569,083	11/14/2006	Andrei Radulescu	2004P01041WOUS	4172
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TITLE OF INVENTION: INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/28/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
ALSIP, MICHAEL	2186	711-118000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____ (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE **Koninklijke Philips Electronics N.V.** (B) RESIDENCE: (CITY and STATE OR COUNTRY) **Eindhoven, The Netherlands**

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted: ☒ Issue Fee ☒ Publication Fee (No small entity discount permitted) ☐ Advance Order - # of Copies _____	4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above) ☐ A check is enclosed. ☐ Payment by credit card. Form PTO-2038 is attached. ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number <u>14-1270</u> . (enclose an extra copy of this form).
---	--

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Michael E. Belk/ Date November 28, 2011
Typed or printed name Michael E. Belk Registration No. 33,357

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		11569083		
Filing Date:		14-Nov-2006		
Title of Invention:		INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS		
First Named Inventor/Applicant Name:		Andrei Radulescu		
Filer:		Michael E. Belk/Elissa DeLuccy		
Attorney Docket Number:		2004P01041WOUS		
Filed as Large Entity				
U.S. National Stage under 35 USC 371 Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2040

Electronic Acknowledgement Receipt	
EFS ID:	11487038
Application Number:	11569083
International Application Number:	
Confirmation Number:	4172
Title of Invention:	INTEGRATED CIRCUIT AND METHOD FOR BUFFERING TO OPTIMIZE BURST LENGTH IN NETWORKS ON CHIPS
First Named Inventor/Applicant Name:	Andrei Radulescu
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	2004P01041WOUS
Receipt Date:	28-NOV-2011
Filing Date:	14-NOV-2006
Time Stamp:	14:10:29
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$2040
RAM confirmation Number	435
Deposit Account	141270
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2004P01041WOUS_Issue_Fee.pdf	113093 e59d38baa23d703eaa0a79c9f285c2a6d8c21385	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32422 6a13bfbbea2f662eaf69e01f731aba7549232f4f	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			145515		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/569,083	12/27/2011	8086800	2004P01041WOUS	4172

24737 7590 12/07/2011
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 632 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Andrei Radulescu, Eindhoven, NETHERLANDS;
Kees Gerard Goossens, Eindhoven, NETHERLANDS;