UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETWORK SYSTEM TECHNOLOGIES, LLC, Plaintiff, v. TEXAS INSTRUMENTS INCORPORATED; FORD MOTOR COMPANY, Defendants.	Civil Action No. 2:22-CV-00482-RWS **JURY TRIAL DEMANDED**

OPENING CLAIM CONSTRUCTION BRIEF
BY PLAINTIFF NETWORK SYSTEM TECHNOLOGIES, LLC

TABLES OF CONTENTS

TABLES OF CONTENTS ii
TABLE OF EXHIBITS iii
TABLE OF AUTHORITIES iv
I. Introduction 1
II. Technical Background 1
A. Background on Network-on-Chip Technology 1
B. Overview of the Asserted Patents 3
III. Legal Standard 5
A. Plain and Ordinary 5
B. Means-Plus-Function 6
C. Definiteness 6
IV. Level of Ordinary Skill in the Art 7
V. Disputed Terms 8
A. "Network" 8
B. "Interconnect Means" 9
C. "Integrated Circuit" 10
D. "Interface Means" 12
E. "Dropping Means" 15
F. "Communication Manager" 18
G. "Resource Manager" 21
H. "Multicast" 24
I. "Narrowcast" 25
J. "Data Communication" 26
K. "Optimal Moment" 27
L. "Optimal Amount" 29
VI. Conclusion 30

TABLE OF EXHIBITS

Ex. No.	Exhibit
1	U.S. Patent No. 7,366,818
2	U.S. Patent No. 7,373,449
3	U.S. Patent No. 7,594,052
4	U.S. Patent No. 7,769,893
5	U.S. Patent No. 8,072,893
6	U.S. Patent No. 8,086,800
7	2023-08-17 – Declaration of Dr. Erik Chmelar re Claim Construction
8	American Heritage College Dictionary (4th ed. 2000)

TABLE OF AUTHORITIES

Page(s)

Cases

Apex Inc. v. Raritan Computer, Inc.,
325 F.3d 1364 (Fed. Cir. 2003).....6, 14, 17

Avid Tech., Inc. v. Harmonic, Inc.,
812 F.3d 1040 (Fed. Cir. 2016).....6, 23

Bitmicro LLC v. Kioxia America, Inc., et al.,
Case 6:22-cv-00331 (W.D. Texas Feb. 16, 2023) 28, 30

Budde v. Harley-Davidson, Inc.,
250 F.3d 1369 (Fed. Cir. 2001).....6

Halliburton Energy Servs., Inc. v. M-I LLC,
514 F.3d 1244 (Fed. Cir. 2008).....7

Interval Licensing LLC v. AOL, Inc.,
766 F.3d 1364 (Fed. Cir. 2014).....7

Linear Tech. Corp. v. Impala Linear Corp.,
379 F.3d 1311 (Fed. Cir. 2004).....14, 17

Massachusetts Institute of Technology v. Shire Pharmaceuticals, Inc.,
839 F.3d 1111 (Fed. Cir. 2016).....23

Medrad, Inc. v. MRI Devices Corp.,
401 F.3d 1313 (Fed. Cir. 2005).....5

MIT v. Abacus Software,
462 F.3d 1344 (Fed. Cir. 2006).....14, 17

Nautilus, Inc. v. Biosig Instruments, Inc.,
572 U.S. 898 (2014).....6

O2 Micro, Ltd. v. Beyond Innovation Tech. Co.,
521 F. 3d 1351 (Fed. Cir. 2008).....9, 10, 11

Phillips v. AWH Corp.,
415 F.3d 1303 (Fed. Cir. 2005).....5

Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.,
711 F.3d 1348 (Fed. Cir. 2013).....14, 17

Skky, Inc. v. MindGeek s.a.r.l.,
859 F.3d 1014 (Fed. Cir 2017).....6, 13, 16, 20

Thorner v. Sony Computer Entertainment America LLC,
669 F.3d 1362 (Fed. Cir. 2012).....5, 6, 23

Vitronics Corp. v. Conceptronic, Inc.,
90 F.3d 1576 (Fed. Cir. 1996).....5

Statutes

35 U.S.C. § 112 ¶ 6 ..... *passim*

35 U.S.C. § 282.....7

I. Introduction

Pursuant to P.R. 4-5 and this Court's Docket Control Order (Dkt. 49), Plaintiff Network System Technologies, LLC ("NST") respectfully submits its opening claim construction brief regarding U.S. Patent Nos. 7,366,818 ("'818 Patent"), 7,373,449 ("'449 Patent"), 7,594,052 ("'052 Patent"), 7,769,893 ("'9893 Patent"), 8,072,893 ("'2893 Patent"), and 8,086,800 ("'800 Patent") (collectively, "Asserted Patents" attached hereto as Exhibits 1–6). The Parties have requested that the Court construe 12 claim terms, each of which are addressed below.

II. Technical Background

A. Background on Network-on-Chip Technology

System-on-chip ("SoC") technology is widely used in consumer electronics and computing devices, including smartphones, laptops, and embedded systems such as vehicle infotainment and advanced driver assistance systems. Dkt. 1 ¶ 92. As the adoption of SoCs in electronic devices grew over time, and as microchip manufacturing technology advanced, more processing cores and other circuitry modules were incorporated into SoCs. *Id.* ¶ 93. In early SoC designs, these circuitry modules were directly connected, first by point-to-point interconnects, and later by shared buses, both of which resulted in large SoCs with poor interconnect efficiency. *Id.*; *see also* Declaration of Dr. Erik Chmelar ("Chmelar Decl." attached hereto as Exhibit 7), ¶¶ 29-31. Though more efficient than point-to-point interconnects, buses suffered from a critical limitation insofar as only one module can send data to the bus at a time and the others must wait their turn. '818 Patent at 1:33-34. Thus, as the number of circuitry modules increased, buses became a bottleneck limiting the number of circuitry modules that could be practicably interconnected—and therefore, limited the potential power and capability of SoCs. *Id*.

To eliminate this bottleneck, the inventors of the Asserted Patents at Philips Semiconductor developed advanced network-on-chip ("NoC") technologies. An NoC is a substantially different

interconnection paradigm for on-chip communication that leverages certain aspects of traditional computer networks, such as network interfaces for connecting modules to an on-chip network, packetized data for breaking messages up into smaller units for transmission by the on-chip network, and routers for switching of data packets along various routes. Chmelar Decl. ¶¶ 32, 57-59. In an NoC, a message transmitted from one module to another may be divided into smaller packets by a network interface and those packets may travel across the NoC using different routes determined by the routers in the NoC. *Id.* ¶ 58. Each interconnection between routers may be called a "hop," such that the NoC is a "multi-hop" interconnection between modules separated by routers, or network nodes. *Id.* ¶¶ 32, 57-60. Accordingly, an NoC is an "indirect" interconnection between modules. *Id.* ¶¶ 181, 189. This is distinctly different from a shared bus, where data transmitted from one module to another always takes the same route, and is therefore a "direct" interconnection between modules.

Besides overcoming the bottleneck of shared buses, NoCs have other advantages over prior, direct, interconnections. Because NoCs can utilize interconnects more efficiently than shared buses, fewer interconnects are required. *Id.* ¶¶ 32-36, 65. This reduces the area and power consumption of the on-chip interconnects of an SoC compared to shared buses. *Id.* ¶¶ 59, 65. Additionally, by moving the communications logic of a circuitry module to a dedicated network interface that connects the module to the NoC, the modules can be simpler and more modular, which enables even higher levels of integration at lower design costs. *Id.* ¶¶ 59, 65.

Although NoCs leverage certain aspects of traditional computer networks, the on-chip environment of NoCs introduces several constraints and challenges not present in the off-chip environment. '818 Patent at 1:62-2:6. For example, there is substantially less memory and computational resources in the on-chip environment that can be dedicated to network processing.

Id. at 2:44-50, 3:7-22, 3:31- 35. The Asserted Patents address these challenges.

B. Overview of the Asserted Patents

The Asserted Patents generally relate to integrated circuits having a plurality of circuitry modules that are communicatively interconnected via NoCs.

Multiple of the Asserted Patents disclose systems for Quality of Service ("QoS"), called "connection properties" in the Patents, which are mechanisms to prioritize and manage communication between different circuitry modules. Chmelar Decl. ¶¶ 38-39. QoS allows for the allocation of network resources according to the specific requirements of different applications or tasks, ensuring, for example, that critical communications get higher priority while lower-priority communications do not unnecessarily consume resources. *Id.* ¶¶ 38-39. Examples of QoS include minimum throughput or bandwidth, maximum latency, and priority. *Id.* ¶¶ 38-39. The '449 and '052 Patents concern aspects of QoS.

The '449 Patent discloses an NoC that interconnects modules by communication channels, with each channel having QoS properties, such as bandwidth and latency guarantees, that can be configured independently. '449 Patent at Abstract, 7:15-30, 11:20-22, 16:1-5. For example, a request channel can guarantee a bandwidth of 1 mega-bit-per-second, and a return channel can guarantee bandwidth of 25 mega-bits-per-second. *Id.* at 9:51-59. Such independently configurable QoS guarantees enable more efficient utilization of the resources of the NoC because the guarantees on each channel can be efficiently adapted to their actual requirements. *Id.* at Abstract, 7:26-31.

The '052 Patent discloses NoC network interfaces configured to map communications to communication channels based on a desired QoS requested for the communication. '052 Patent at Abstract, 1:6-10, 3:6-34, 3:45-51, 4:7-18, 8:7-9, 8:63-65. This mapping ensures that high-priority communications requiring certain QoS guarantees are appropriately mapped within the network,

resulting in the most efficient use of network resources. *Id.* at 7:63-67. Moreover, performing such mapping within the network interfaces, as opposed to within the modules, frees the modules to focus on their dedicated operations. *Id.* at 3:30-34, 5:16-21.

The Asserted Patents disclose NoC network interfaces that manage certain inter-module communication tasks, such as packetizing data at the sending module and the depacketizing data at the receiving module, translating between different communication protocols used by the modules, and dropping data in certain cases. The ’9893 and ’818 Patents concern aspects of network interfaces.

The ’9893 Patent discloses an NoC network interface configured to translate between different address formats used by the modules. ’9893 Patent at Abstract, 3:43-63. This address translation allows various types of modules to be integrated regardless of the communication protocols used by the modules. *Id.* at 1:45-48. This can simplify modules and reduce SoC design time and costs. *Id.* at 1:42-48.

The ’818 Patent discloses NoC network interfaces configured to drop data in certain cases. ’818 Patent at 5:35-36. One example where data may be dropped is when the buffer at the receiving module is full and thus no more data may be received at that module. *Id.* at 4:40-55.

Finally, multiple of the Asserted Patents disclose NoC buffers to increase network efficiency and resolve synchronization issues between fast and slow communication channels. The ’2893 and ’800 Patents concern aspects of data storage and buffering.

The ’2893 Patent discloses how to synchronize slow communication channels with faster channels. ’2893 Patent at 1:34-2:33. Instead of simply slowing down the faster channels, data storage elements are added to the slow channels to delay their communications by an amount that causes each data package transmitted on the slow channels to be received in a next data-package

cycle instead of the current data-package cycle. *Id.* at 1:65-2:14, 2:26-33, 2:47-3:17, 3:49-53.

The '800 Patent discloses an NoC network interface that has buffers to store data until an optimal amount of data is available for transmission on the network. '800 Patent at 4:18-28, 4:50-57. Rather than inefficiently transmitting data in small packages as it is generated by the circuitry modules, the buffers aggregate data until an optimal amount of data is ready to be transmitted over the network, increasing overall network utilization and efficiency. *Id.* at 3:1-3, 7:44-46.

III. Legal Standard

A. Plain and Ordinary

The "words of a claim" are understood according to their plain and ordinary meaning in the context of the surrounding claim limitations, the specification, and the prosecution history. *Thorner v. Sony Computer Entertainment America LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

The "words of a claim" are not given their plain meaning only when the patentee "acts as his own lexicographer" or "disavows the full scope of a claim term either in the specification or during prosecution." *Thorner*, 669 F.3d at 1365. As the Federal Circuit cautions, "we must look at the ordinary meaning in the context of the written description and the prosecution history," since importing limitations is one of the "cardinal sins of patent law." *Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1320 (Fed. Cir. 2005). Accordingly, a "claim construction that does not encompass a disclosed embodiment is rarely, if ever, correct." *Medrad*, 401 F.3d at 1320.

The standard for lexicography is exacting. *Thorner*, 669 F.3d at 1365-67. "To act as its own lexicographer, a patentee must clearly set forth a definition of the disputed claim term other than its plain and ordinary meaning," and occurs only when the patentee explicitly discloses that a term "means" a particular definition or "is defined." *Id*. The "standard for disavowal of claim

scope is similarly exacting." *Id*. The intrinsic evidence must provide "expressions of manifest exclusion or restriction," clarifying that the invention does not include a particular feature. *Id*. "Where the alleged disavowal is ambiguous," courts do not apply the doctrine of prosecution history disclaimer. *Avid Tech., Inc. v. Harmonic, Inc.*, 812 F.3d 1040, 1045 (Fed. Cir. 2016).

B. Means-Plus-Function

"In determining whether a claim term invokes § 112, ¶ 6, the essential inquiry is not merely the presence or absence of the word 'means' but whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Skky, Inc. v. MindGeek s.a.r.l.*, 859 F.3d 1014, 1019 (Fed. Cir 2017) (internal quotations and citations omitted). While the word "means" triggers a presumption that § 112, ¶ 6 applies, this can be rebutted by a preponderance of the evidence when "consider[ing] the limitations as a whole" according to the "understanding of one of ordinary skill in the art." *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1374 (Fed. Cir. 2003) (internal quotations, citations, and modifications omitted). "[W]hen a claim uses the term 'means,' the focus is on whether the claim term recites no function corresponding to the means or recites sufficient structure or material for performing that function." *Id*. at 1372 (internal quotations omitted). To further "hold that a claim containing a means-plus-function limitation lacks a disclosure of structure" "requires [an additional] finding, by clear and convincing evidence, that the specification lacks disclosure of structure sufficient to be understood by one skilled in the art as being adequate to perform the recited function." *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1376-77 (Fed. Cir. 2001).

C. Definiteness

Definiteness is evaluated from the perspective of someone "skilled in the relevant art." *Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 909 (2014). "[T]he certainty which the law requires in patents is not greater than is reasonable, having regard to their subject-matter." *Id*.

at 910 (quoting *Minerals Separation, Ltd. v. Hyde*, 242 U.S. 261, 270 (1916)). Terms of degree are not "inherently indefinite," and "absolute or mathematical precision is not required." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 (Fed. Cir. 2014).

Indefiniteness requires an accused infringer to show "by clear and convincing evidence that a skilled artisan could not discern the boundaries of the claim based on the claim language, the specification, and the prosecution history, as well as her knowledge of the relevant art area." *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1249-50 (Fed. Cir. 2008); 35 U.S.C. § 282.

IV. Level of Ordinary Skill in the Art

NST's expert, Dr. Chmelar, opines that a person of ordinary skill in the art ("POSITA") at the time of the invention of the Asserted Patents is an individual having at least: a Bachelor of Science (or equivalent) degree in electrical engineering, computer engineering, or a related field, and 2-3 years of work experience in very large-scale integrated ("VLSI") systems, such as application-specific integrated circuits ("ASICs"), application-specific standard parts ("ASSPs"), system-on-chip ("SoC"), or field-programmable gate arrays ("FPGAs"), and has an understanding of on-chip interconnection networks. Chmelar Decl. ¶ 26.

Defendants' expert, Dr. Thornton, posits an even higher skill level: at least either a Master's degree in Electrical Engineering, or related field, as well as at least three years of work experience in the field of SoC design, or a Bachelor's degree in Electrical Engineering, or related field, as well as at least five years of work experience in the field of SoC design.

Neither expert has opined whether this discrepancy would have an impact on their conclusions as to the constructions of the various terms. It is noteworthy, however, that Dr. Chmelar opines that the Asserted Patents would not be indefinite to a POSITA having a skill level lower than that posited by Dr. Thornton, so it is reasonable to conclude that Dr. Chmelar's

definiteness conclusions would remain the same for Dr. Thornton's higher-skilled POSITA.

V. Disputed Terms

A. "Network"

Term	NST's Construction	Defendants' Construction
"network" '818 Patent: claims 1, 2 '449 Patent: claims 10-12, 14 '9893 Patent: claims 4, 11 '2893 Patent: claims 1, 10	"multi-hop interconnection between modules separated by one or more network nodes"	Plain and ordinary meaning

NST's proposed construction of "network" as a "multi-hop interconnection between modules separated by one or more network nodes" reflects what a POSITA would have understood this term to mean as used in the Asserted Patents. *See* Chmelar Decl. ¶¶ 50-52. This construction is based on intrinsic evidence in the Asserted Patents, which explain, "[i]ntroducing networks as on-chip interconnects **radically changes the communication** when compared to direct interconnects, such as buses or switches. **This is because of the multi-hop nature of a network**, where communication modules are not directly connected, but **separated by one or more network nodes**." *See, e.g.*, '818 Patent at 3:36-41; *see also* '449 Patent at 3:47-52; '052 Patent at 2:32-37; '9893 Patent at 2:46-51; '800 Patent at 2:3-8. Defendants' proposal fails to account for the multi-hop nature of the network.

Moreover, Defendants' proposal is unworkable because the term "network" lacked a consistent plain and ordinary meaning at the time of the inventions. At that time, the concept of an on-chip "network" was still emerging from the intersection of computer networking and microchip design. Chmelar Decl. ¶ 53. This is reflected in an authoritative IEEE dictionary of the time, which includes differing definitions for the term "network." *See* Chmelar Decl. ¶ 56 (*comparing* "An arrangement of components, or nodes, and interconnecting branches" (microchip-design

perspective) *with* "A network is any set of devices or subsystems connected by links joining (directly or indirectly) a set of terminal nodes" (computer networking perspective)). Not surprisingly, the Asserted Patents explicitly distinguish between the differing definitions of a "network" as used in the asserted inventions from traditional computer networking or traditional microchip design concepts. *Id.* ¶ 59; '818 Patent at 1:67-2:16; *see also* '449 Patent at 1:66-2:15; '052 Patent at 1:64-2:12; '9893 Patent at 1:65-2:11; '800 Patent at 1:64-2:2. These distinctions were not trivial to the inventions, and are key to the Parties' invalidity disputes. Thus, NST's plain and ordinary meaning construction should be adopted. *O2 Micro, Ltd. v. Beyond Innovation Tech. Co.,* 521 F. 3d 1351, 1361 (Fed. Cir. 2008) ("[W]hen a term has more than one 'ordinary' meaning or when reliance on a term's 'ordinary' meaning does not resolve the parties' dispute.").

B. "Interconnect Means"

Term	NST's Construction	Defendants' Construction
"interconnect means" '052 Patent: claim 6	"multi-hop interconnection between modules separated by one or more network nodes."	Plain and ordinary meaning. Not subject to Section 112 ¶ 6.

Intrinsic evidence shows that a POSITA would have understood the term "interconnect means" to describe a "multi-hop interconnection between modules separated by one or more network nodes" as a "network" (*i.e.*, an indirect interconnection) rather than a shared bus (*i.e.*, a ***direct interconnection***). *See* Chmelar Decl. ¶¶ 175-177.

For instance, the '052 Patent ascribes the exact same functionalities to an "interconnect means (N)" as it does to a "network N," which was addressed in the previous section. *See* Chmelar Decl. ¶¶ 182-187 (citing '052 Patent at Abstract, Fig. 1, Fig. 4, 1:7-8, 3:18-22, 3:51-54, 4:1-4, 5:24-31). Furthermore, the '052 Patent discloses that the "interconnect means (N) is provided . . . for enabling a connection based communication having a set of connection properties." *See*

Chmelar Decl. ¶ 188 (citing '052 Patent at Abstract; *see also* 3:15-18, 3:51-54, 4:1-4). To this end, the Patent lists a number of properties for the "connection," including "1) data integrity, 2) transaction ordering, 3) transaction completion, 4) connection flow control, and 5) connection throughput, latency, and jitter." *Id.* ¶¶ 188-189 (citing '052 Patent at 4:50-5:5, 6:13-19). A POSITA would understand a connection with these properties to be a known attribute of an example of the "network" disclosed in the Asserted Patents. *Id.* ¶ 189. In this context, a POSITA would understand "interconnection means" to describe a "network" comprising indirect interconnections between modules, not a direct interconnection between modules as typically found in a bus architecture. *Id.* Thus, a POSITA would understand that the "network N" and the "interconnect means (N)" to be the same thing. *Id.*

Defendants' argument for a plain and ordinary meaning construction fails because, like "network," the term "interconnect means" lacked consistent meaning at the time of the inventions. *See* Chmelar Decl. ¶¶ 178-181. Moreover, adopting a plain and ordinary meaning would fail to resolve key invalidity disputes regarding whether the terms "network" and "interconnect means" should be constrained by their usage in the Asserted Patents or should encompass additional concepts like bus architectures and off-chip communications. Thus, a plain and ordinary meaning is inappropriate. *O2 Micro, Ltd.,* 521 F. 3d at 1361 (Fed. Cir. 2008).

C. "Integrated Circuit"

Term	NST's Construction	Defendants' Construction
"integrated circuit" '818 Patent: claims 1-3, 5-7 '449 Patent: claim 10 '052 Patent: claim 6 '9893 Patent: claim 4 '2893 Patent: claims 1, 10 '800 Patent: claim 12	"interconnected circuitry on a chip"	Plain and ordinary meaning

Intrinsic evidence supports NST's construction of an "integrated circuit" as "interconnected circuitry on a chip." The Asserted Patents disclose embodiments concerning circuitry "on a chip" (*i.e.*, network-on-chip) rather than "off-chip," explaining the many ways in which "NoC's [(network-on-chip's)] premises are different from off-chip networks," including "their constraints and synchronization," such that "most of the network design choices must be reevaluated." Chmelar Decl. ¶¶ 64-65; '818 Patent at 1:67-2:43;'449 Patent at 1:66-2:42; '052 Patent at 1:64-2:12; '9893 Patent at 1:65-2:36; '800 Patent at 1:64-2:2. For instance, the Asserted Patents disclose a "system-on-chip" or a "system on silicon" where most or all components are integrated on an interconnected circuit, including memories, processors, high-speed I/O interfaces, and dedicated application-specific logic. Chmelar Decl. ¶¶ 67-68; '818 Patent at 1:51-53; '449 Patent at 1:15-35, 1:50-52; '052 Patent at 1:14-32, 1:48-50; '9893 Patent at 1:14-34, 1:49-51; '2893 Patent at 1:8-13; '800 Patent at 1:14-32, 1:48-50.

NST's construction of an "integrated circuit" as an "interconnected circuitry on a chip" is also supported by extrinsic evidence, including IEEE technical dictionaries that define an "integrated circuit" as "[a] combination of ***interconnected circuit*** elements [(*i.e.*, 'interconnected circuitry')] inseparably associated ***on or within a continuous substrate*** [(*i.e.*, 'on a chip')]." Chmelar Decl. ¶ 69 (citing Exs. H, I and G thereto).

Defendants' plain and ordinary meaning argument fails to recognize that the Asserted Patents only disclose an "integrated circuit" that can be interconnected *on-chip*. Instead, Defendants' construction would actually introduce the new concept that an "integrated circuit" can be *off-chip*, which is not disclosed by the Asserted Patents and would expand the Parties' invalidity disputes. Thus, Defendants' position is inappropriate. *O2 Micro,* 521 F. 3d at 1361.

D. "Interface Means"

Term	NST's Construction	Defendants' Construction
"interface means" / "interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN) wherein said interface means (ANIP, PNIP) comprises a first dropping means (DM) for dropping data, and wherein the dropping of data and therefore the transaction completion can be controlled by the interfaces means" '818 Patent: claims 1, 6, 7	**For "interface means":** "interface circuit that connects a module to a network" **For "interface means (ANIP, PNIP) for managing the interface…":** NST incorporates its definitions for the terms "interface means," "network," and "dropping means." The remaining parts of this term should be afforded their plain and ordinary meanings. **If the Court holds §112, ¶ 6 applies:** NST disagrees that this term is governed by §112, ¶ 6. Nonetheless, if the Court holds otherwise, NST proposes the following construction: **Function**: *Claim 1*: "manage the interface between a module and the network, and control the dropping of data and therefore the transaction completion"; *Claim 6*: the function according to claim 1 and "store received error messages"; *Claim 7*: the function according to claim 1 and "not drop error messages" **Structure**: "circuit"	Subject to § 112 ¶ 6. **Function**: *Claim 1*: "managing the interface between a module (M, S) and a network (N, RN) and controlling dropping of data and transaction completion"; *Claim 6*: "storing received error messages"; *Claim 7*: "not dropping error messages" **Structure**: With respect to claim 1, "structure for dropping means and buffer to accommodate a return status message for outstanding transactions, as disclosed in the '818 Patent at 8:40-45, 9:1-2, and 9:11-36." Otherwise, indefinite.

NST's construction of an "interface means" as an "interface circuit that connects a module to a network" reflects what a POSITA would have understood this term to mean as used by the

’818 Patent. For instance, the ’818 Patent discloses “**an integrated circuit comprising at least one interface means** ANIP [(active network interface port)], PNIP [(passive network interface port)] . . . is provided . . . .” ’818 Patent at 5:37-40 (emphasis added). And an “integrated circuit” is understood by a POSITA as a “combination of interconnected circuit elements.” Chmelar Decl. ¶ 75. If the ’818 Patent discloses an “interface means” comprised in an “integrated circuit,” then it logically follows that the “interface means” must be a “circuit element” of the “integrated circuit.” *Id.* That an “interface means ANIP, PNIP is **adapted to store** received error messages” supports NST’s construction because **storage** cannot be achieved without **storage circuitry** (*e.g.,* latches, flip-flops, registers, memory cells, etc.). *Id.* (citing ’818 Patent at 5:64-66) (emphases added). Additionally, the ’818 Patent discloses that the “interface means” connects “modules and the router network.” *Id.* ¶ 76 (quoting ’818 Patent at 7:23-27; *see also id.* at Fig 2, 7:27-31

Defendants’ position that “interface means” is part of a larger phrase that should be construed as a means plus function term under 35 U.S.C. § 112 ¶ 6 is unfounded, and is undermined by Defendants’ inconsistent treatment of “interconnect means,” which though contains the word “means” was not proposed by Defendants to be governed by 112 ¶ 6. Moreover, the presumption that the word “means” subjects a claim term to interpretation under 112 ¶ 6 is rebutted where phrase describes structure. *Skky*, 859 F.3d at 1020 (finding “‘wireless device means’ does not invoke 112 ¶ 6 because its clause recites sufficient structure”). Similar to how the “wireless device” in “wireless device means” was sufficient structure, and how the “interconnect” in “interconnect means” was sufficiently structural according to Defendants’ ready, the “interface” in the subject phrase “interface means” describes sufficient structure and 112 ¶ 6 does not apply.

Nevertheless, if 35 U.S.C. § 112 ¶ 6 does apply, the correct functions and structures would be as follows:

Claim	Function	Structure
Claim 1	"manage the interface between a module and the network, and control the dropping of data and therefore the transaction completion."	"circuit"
Claim 6	Function According to Claim 1 + to "store received error messages."	"circuit"
Claim 7	Function According to Claim 1 + to "not drop error messages."	"circuit"

Chmelar Decl. ¶¶ 95-100. These functions are supported by the specification, which discloses "an integrated circuit comprising at least one interface means ANIP, PNIP **for managing the interface between a module M, S and the network N, RN**." '818 Patent at 5:37-40 (emphasis added); *see also id.* at 5:64-67, 5:37-44. The claims themselves also recite these functions, including claim 1's recitation: "at least one interface means … **for managing the interface between a module … and the network** … **wherein the dropping of data and therefore the transaction completion can be controlled by** the interface means," '818 Patent at claim 1 (emphasis added); *see also* claim 6 ("said interface means (ANIP, PNIP) is adapted to store received error messages"); claim 7 ("an interface means (ANIP) associated to the first module (M) is adapted not to drop error messages.").

Second, the '818 Patent discloses the structure of the "interface means" to be a "circuit," which the Federal Circuit has repeatedly found to be a term that sufficiently connotes structure. *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348, 1364 (Fed. Cir. 2013); *MIT v. Abacus Software,* 462 F.3d 1344, 1355 (Fed. Cir. 2006); *Linear Tech. Corp. v. Impala Linear Corp.,* 379 F.3d 1311, 1320-21 (Fed. Cir. 2004) (holding that the term "circuit" is not a means-plus-function limitation when the patent provides "a recitation of the respective circuit's operation in sufficient detail to suggest structure to persons of ordinary skill in the art"); *Apex Inc. v. Raritan Computer, Inc.,* 325 F.3d 1364, 1373 (Fed. Cir. 2003) ("[T]he term 'circuit' with an appropriate identifier such as 'interface,' 'programming' and 'logic,' certainly identifies some structural meaning to one of ordinary skill in the art."). For example, the '818 Patent discloses that "[a]ccording to an aspect of the invention, **an integrated circuit** comprising

at least one interface means ANIP [(active network interface port)], PNIP [(passive network interface port)] . . . is provided . . . ." '818 Patent at 5:37-40 (emphasis added); *see also* Chmelar Decl. ¶ 99. Likewise, according to authoritative extrinsic sources of the time, an "integrated circuit" is "[a] combination of interconnected circuit elements inseparably associated on or within a continuous substrate." *Id.* (citing Exs. I and G thereto). Therefore, an interface means comprised in an integrated circuit must be a circuit element of the integrated circuit. *Id.*

E. "Dropping Means"

Term	NST's Construction	Defendants' Construction
"dropping means" / "one dropping means (DM) for dropping data exchanged by said first and second module (M, S) / a first dropping means (DM) / said dropping means (DM)" '818 Patent: claims 1, 3, 5	**For "dropping means":** "circuit configured to drop messages" **For "one dropping means (DM) for dropping data exchanged by …":** NST incorporates its definition for the term "dropping means." The remaining parts of this term should be afforded their plain and ordinary meanings. **If the Court holds §112, ¶ 6 applies:** NST disagrees that this term is governed by §112, ¶ 6. Nonetheless, if the Court holds otherwise, NST proposes the following construction: **Function**: *Claim 1*: "drop data exchanged by said first and second module"; *Claim 3*: function according to claim 1 and "create an error message if data is dropped"; *Claim 5*: function according to claim 1 and "send said error message	Subject to § 112 ¶ 6. **Function**: *Claim 1*: "dropping data exchanged by first and second module (M, S)"; *Claim 3*: "creating error messages"; *Claim 5*: "sending error messages" **Structure**: With respect to claim 1, "buffer that implements a 'milk' policy (drops oldest data) or a 'wine' policy (drops newest data) when the buffer overflows, as disclosed in the '818 Patent at 7:51-56; 8:38-39, 8:64-66." Otherwise, indefinite. With respect to claims 3 and 5, "structure for claim 1 with additional structure disclosed in the '818 Patent at 9:2-10." Otherwise, indefinite.

Term	NST's Construction	Defendants' Construction
	to said first module" **Structure**: "circuit"	

NST's construction of "dropping means"[1] as an "circuit configured to drop messages" reflects what a POSITA would have understood the term to mean as used in the Asserted Patents. For instance, the '818 Patent's specification explicitly discloses that "[s]aid **integrated circuit comprises** at least **one dropping means.**" Chmelar Decl. ¶ 105 (citing '818 Patent at Abstract (emphases added); *see also id.* at 5:27-28, 5:37-41 ("integrated circuit comprising at least one interface means" that "comprises a first dropping means."). Likewise, authoritative technical dictionaries of the time further support this construction by defining an "integrated circuit" as "[a] combination of **interconnected circuit elements** inseparably associated on or within a continuous substrate." *Id.* (citing Exs. I and G thereto). Therefore, a dropping means comprised in an integrated circuit must be a circuit element of the integrated circuit. *Id.*

Defendants' argument that "dropping means" should be construed as part of a larger phrase under 35 U.S.C. § 112 ¶ 6 is unfounded, and is undermined by Defendants' inconsistent treatment of "interconnect means," which though contains the word "means" was not proposed by Defendants to be governed by 112 ¶ 6. Moreover, the presumption that the word "means" subjects a claim term to interpretation under 112 ¶ 6 is rebutted where phrase describes structure. *Skky*, 859 F.3d 1014 at 1020 (finding "'wireless device means' does not invoke 112 ¶ 6 because its clause recites sufficient structure"). Here, the claim language expressly describes an "**integrated circuit** comprising at least one dropping means." '818 Patent at Claim 1. Thus, because sufficient

[1] The '818 Patent uses the terms "dropping means" and "dropping manager" interchangeably. '818 Patent at 7:48-50.

structure, *i.e.*, the intergrated circuit, is disclosed, 112 ¶ 6 does not apply.

Nevertheless, if § 112 ¶ 6 does apply, Defendant's position is incorrect. Instead, the correct functions and structures are identified as follows:

Claim	Function	Structure
Claim 1	"drop data exchanged by said first and second module."	"circuit"
Claim 3	Claim 1's Function ***plus*** to "create an error message if data is dropped."	"circuit"
Claim 5	Claim 1's Function ***plus*** to "send said error message to said first module."	"circuit"

Chmelar Decl. ¶¶ 125-130. First, claim 1 of the '818 Patent recites the function "dropping data exchanged by said first and second module (M, S)" for the "dropping means (DM)." Chmelar Decl. ¶ 126 citing '818 Patent at Claim 1. The specification also discloses the function "a first dropping means DM **for dropping data**." *Id.* (citing '818 Patent at 5:37-42 (emphasis added). Claims 3 and 5 incorporate this same function, while adding the limitations in NST's proposal above. *Id.* ¶ 127 (citing '818 Patent at claim 3 ("said **dropping means** (DM) are **adapted to create an error message if data is dropped**") *and* claim 5 ("said **dropping means** (DM) are adapted to **send said error message to said first module**."). These additional limitations are also disclosed in the specification. *Id.* (citing '818 Patent at 5:50-54 (claim 3) *and* 5:60-63 (claim 5)).

Second, the '818 Patent discloses the corresponding structure as a "circuit," which the Federal Circuit has held is a term that connotes adequate structure. *See Power Integrations*; *MIT*; *Linear Tech.*; *Apex*, *supra*; *see also* Chmelar Decl. ¶ 129 (citing '818 Patent at Abstract ("[s]aid integrated circuit comprises at least one dropping means."), 5:27-28).

That a "circuit" is the corresponding structure is also supported by authoritative extrinsic sources in publication at the time of the inventions, which define an "integrated circuit" as "[a] combination of interconnected circuit elements inseparably associated on or within a continuous substrate." *Id.* ¶ 129 (*citing* Exs. I and G thereto). By this definition, a "dropping means"

comprised in an integrated circuit, as is disclosed by the Asserted Patents, must be a "circuit element" of an "integrated circuit." *Id.*

F. "Communication Manager"

Term	NST's Construction	Defendants' Construction
"communication manager" '449 Patent: claim 10	"circuit that manages communication between modules" **<u>If the Court holds §112, ¶ 6 applies:</u>** NST disagrees that this term is governed by §112, ¶ 6. Nonetheless, if the Court holds otherwise, NST proposes the following construction: **Function**: "forward a request for a connection to a resource manager" **Structure**: "circuit"	Subject to § 112 ¶ 6. **Function**: receiving a request for a connection from a first module, forwarding the request to a resource manager, and receiving the availability of the target connection from the resource manager **Structure**: Indefinite

NST's construction of a "communication manager" as a "circuit that manages communication between modules" reflects what a POSITA would have understood this term to mean as used in the Asserted Patents. First, intrinsic evidence supports this construction, since the '449 Patent discloses that the "communication manager" is comprised in "a system on chip," which is an "integrated circuit." *See supra* Section V.C; *see also* Chmelar Decl. ¶ 159 (citing '449 Patent at 9:66-10:3); *see id.* ¶ 64 (explaining that a "system on chip" is an "integrated circuit"). Indeed, the '449 Patent expressly discloses that "**said integrated circuit comprises** at least one **communication managing means**."[2] *Id.* (citing '449 Patent at 7:35-38 (emphases added)).

Authoritative technical dictionaries of the time also support this construction by defining

[2] The '449 Patent uses the terms "communication manager" and "communication managing means" interchangeably. Chmelar Decl. ¶ 159.

an "integrated circuit" as "[a] combination of **interconnected circuit elements** inseparably associated on or within a continuous substrate." Chmelar Decl. ¶ 160 (*citing* Exs. I and G thereto). In other words, since the '449 Patent discloses a "communication manager" comprised in an integrated circuit, it logically follows that the "communication manager" must be a "circuit element" of said "integrated circuit." This is further supported by the '449 Patent's disclosure of the "communication manager" as being arranged in a "network," a "router network," or a "network interface means," which are themselves comprised in an "integrated circuit." Chmelar Decl. ¶ 161 (citing '449 Patent at 9:66-10:6; Abstract ("An integrated circuit comprising a plurality of processing modules (M; I; S; T) and a network (N; RN) arranged for providing at least one connection between a first and at least one second module is provided"), 1:7-11 ("The invention relates to an integrated circuit having a plurality of processing modules and a network arranged for providing connections between processing modules and a method for exchanging messages in such an integrated circuit."), 7:15-18 ("Therefore, an[] integrated circuit comprising a plurality of processing modules M; I; S; T and a network N; RN arranged for providing at least one connection between a first and at least one second module is provided."); 8:7-11 ("According to still a further aspect of the invention, said integrated circuit comprises at least one network interface means N1, associated to each of said modules, for managing the communication between said modules and said network N."); 9:17-21 ("FIG. 2 shows a system on chip according to a second embodiment. The system comprises two modules, namely an initiator I and a target T, a router network RN, and two network interfaces ANIP, PNIP between the modules and the router network RN.").

Defendants' position that "communication manager" is part of a larger phrase that must be construed under 35 U.S.C. § 112 ¶ 6 is unfounded, and is undermined by their reasoning in their proposed constructions for "dropping means" and "communication manager." Chmelar Decl. ¶

174. Namely, Defendants' contend that "dropping means" should be construed under § 112 ¶ 6, means-plus-function, where the corresponding structure is "dropping **manager**" that drops oldest data (milk policy) or newest data (wine policy) when a buffer overflows." *Id.* Defendants appear to suggest that the term "manager" is inherently structural, especially because the rest of their proposed structure is an action performed by the dropping manager, *i.e.*, it drops oldest or newest data. *Id.* Applying this logic, the "manager" in the "communication manager" should have sufficient structure to not trigger § 112 ¶ 6. *Skky*, 859 F.3d 1014 at 1020

Nevertheless, if § 112 ¶ 6 were to apply, Defendant's proposal that this term is indefinite is incorrect. Rather, the function and structure for claim 10 would be as follows:

Claim	Function	Structure
Claim 10	"forward a request for a connection to a resource manager"	"circuit"

Chmelar Decl. ¶¶ 165-173. First, this function is recited in claim 10 as a communication manager for "**forwarding the request to a resource manager**." Chmelar Decl. ¶ 166 (emphasis added). The specification also discloses this function as "[t]he communication manager CM **request[s] a connection with a set of properties between two modules from the resource manager RM, after receiving the request REQ** from the active network interface ports ANIP," and that the "the resource manager RM . . . **responds to the communication manager CM which connection is available**." *Id.* (citing '449 Patent at 10:19-46) (emphases added).

Additionally, intrinsic evidence supports a "circuit" as the corresponding structure by disclosing that "**said integrated circuit** comprises at least one **communication managing means** CM for managing the communication between different modules." Chmelar Decl. ¶ 169 (citing '449 Patent at 7:35-38 (emphases added), 9:66-10:3). Moreover, the '449 Patent also discloses that the "communication manager" is arranged in either a network, a router network, or a network interface means, all of which are comprised in an "integrated circuit." *Id.* ¶ 171; '449 Patent at

9:66-10; *see also id.*, 1:7-11, 7:15-18, 8:7-11, 9:17-21, Abstract ("An integrated circuit comprising a plurality of processing modules (M; I; S; T) and a network (N; RN) arranged for providing at least one connection between a first and at least one second module is provided.").

As with other terms, technical dictionaries also support that conclusion that a "circuit" is the corresponding structure for this term by defining an "integrated circuit" as "[a] combination of interconnected circuit elements inseparably associated on or within a continuous substrate." And because a "communication manager" is comprised in an integrated circuit must, the "communication manager" must be a "circuit element" of said integrated circuit. *Id.* ¶ 170 (citing Exs. I and G). Under this definition, since the "communication manager" is comprised in either the network, a router network, or the network interface means, which are integrated circuits, the "communication manager" must also be a "circuit."

G. "Resource Manager"

Term	NST's Construction	Defendants' Construction
"resource manager determining whether a target connection with the desired connection properties is available" '449 Patent: claims 10, 14, 15	"resource manager" means "circuit that manages network resources." The remaining parts of this term should be afforded their plain and ordinary meanings.	"resource manager determining whether a target connection with the desired connection properties is available, where the resource manager is not an arbiter that selects the output based on input priorities"

NST's construction reflects what a POSITA would have understood this term to mean as used in the '449 Patent, namely, that "resource manager" means a "circuit that manages network resources" and that the rest of this term has a plain and ordinary meaning.

For one, the '449 Patent repeatedly discloses that the "resource manager" is part of a "circuit." *See* Chmelar Decl. ¶ 135 (citing '449 Patent at 9:66-10:3 ("FIG. 3 shows a system on chip [that] comprises a communication manager CM and a resource manager RM."); 7:35-39

("**said integrated circuit comprises . . . at least one resource managing means** RM for managing the resources of the network N.") (emphasis added)).[3] The '449 Patent also discloses that the "resource manager" is arranged in a network or a network interface means, which are both comprised in integrated circuits. *Id.* ¶ 137 (citing '449 Patent at Abstract). This circuit "manages network resources," consistent with NST's construction. *Id.* ¶ 140 (quoting '449 Patent at 7:38-39 ("at least one resource managing means RM for managing the resources of the network"); *see also id.* ¶¶ 141-144.

The rest of this term should be afforded its plain and ordinary meaning. The independent claims and the specification disclose a resource manager "for managing the resources of the network." Chmelar Decl. ¶ 148 (quoting and describing multiple examples from the '449 Patent of management functions of the resource manager that relate to "determining whether a target connection with the desired connection properties is available") (citing '449 Patent at 10:19-46; 10:34-40; 10:41-44).

As with the other terms, NST's construction is also supported by technical dictionaries of the time, which defined an "integrated circuit" as "[a] combination of **interconnected circuit elements** inseparably associated on or within a continuous substrate." Chmelar Decl. ¶ 138 (citing Ex. I (emphasis added); *see also id.* at Ex. G). Again, if a network, a router network, or a network interface means is comprised in an integrated circuit, a "resource manager" comprised in a network, router network, or network interface means must also be a "circuit."

Defendants' proposed construction is inappropriate as it seeks to add language to the claim term (*i.e.*, "where the resource manager is not an arbiter that selects the output based on input

[3] The '449 Patent uses the terms "resource manager" and "resource managing means" interchangeably. Chmelar Decl. ¶ 135.

priorities") that is not supported by the specification or prosecution history.

NST's expert, Dr. Chmelar, reviewed and analyzed the prosecution passages that Defendants rely upon for their construction and concluded that there is nothing in the prosecution history that concerns whether "the resource manager is not an arbiter that selects the output based on input priorities." *Id.* ¶¶ 150-154.

Though the Applicant amended claim 10 of the '449 Patent to add limitations concerning features of the resource manager: 1) receiving a request from the communication manager comprising desired connection properties associated with the sets of communication channels; 2) determining whether a target connection with the desired connection properties is available; and 3) responding with the availability of the target connection to the communication manager, *see id.* ¶ 151, and distinguished the cited Emerson reference based on the fact that Emerson's arbiter does not have those features, *see id.* ¶ 150, the Applicant made no clear and unmistakable concession that the resource manager "is not an arbiter that selects the output based on input priorities." *See id.* ¶ 153. Indeed, the Examiner explained in the reason for allowance that the claim was allowable over the prior art (including Emerson) because it "do[es] not teach wherein the resource manager determines whether the at least one connection with the communication channels is available based on the connection properties being available"—which is a limitation already expressly included in claim 10. *Id.* ¶ 152 (quoting prosecution history).

Thus, because there was no "exacting" disavowal of claim scope, it is improper to read in the limitation that Defendants propose. *Thorner*, 669 F.3d at 1365–67 ("The standard for disavowal of claim scope is … exacting."); *Avid Tech.*, 812 F.3d at 1045 ("Where the alleged disavowal is ambiguous," courts do not apply the doctrine of prosecution history disclaimer); *Massachusetts Institute of Technology v. Shire Pharmaceuticals, Inc.*, 839 F.3d 1111, 1119 (Fed.

Cir. 2016) (prosecution history disclaimer must be "clear and unmistakable" such that where disavowal is ambiguous or amenable to multiple interpretations, prosecution history disclaimer does not attach).

H. "Multicast"

Term	NST's Construction	Defendants' Construction
"multicast" '9893 Patent: claims 7, 10	"between one and each of a selected group of others collectively"	"a connection in which the messages are duplicated, sent to each receiving module, executed by each receiving module, but no return messages are allowed"

NST's proposed construction of "multicast" reflects what a POSITA would have understood the term to mean as used in the Asserted Patents. For instance, the specification of the '9893 Patent discloses that "[a] **multicast** connection is a connection between one ANIP and one or more PNIPs, in which the sent messages are duplicated and each PNIP receives a copy of those messages." Chmelar Decl. ¶ 195; '9893 Patent at 5:58-67 (emphasis added).

Additionally, technical dictionaries of the time support this construction by defining "multicast" as "[a] transmission mode in which a single message is sent to multiple network destinations, (i.e., one-to-many)." Chmelar Decl. ¶ 197 (citing Ex. G thereto); *see also id.* (citing Exs. K and L thereto). A POSITA *would not* understand this definition of "multicast" to restrict a select group of modules from providing a response. The ability to provide a response has no bearing on whether the connection is multicast or not. Chmelar Decl. ¶ 198. In some embodiments, a selected group may provide a response whereas in others they may not. *Id.*

Defendants' construction seeks to add the restriction that "**no** return messages are allowed," which is undermined by the specification's disclosure of circumstances under which return messages are expected. *See, e.g.*, Chmelar Decl. ¶ 196 (citing '9893 Patent at 7:42-43 ("However, since **a multicast connection expects a response form [sic] each slave**, the PNIPs must include

empty responses") (emphasis added)). Thus, Defendants' construction must be rejected.

I. "Narrowcast"

Term	NST's Construction	Defendants' Construction
"narrowcast" '9893 Patent: claims 7, 10	"between one and each of a selected group of others individually"	"a connection in which the messages are duplicated, sent to each receiving module, but executed by exactly one receiving module"

NST's construction of "narrowcast" as "between one and each of a selected group of others individually" reflects what a POSITA would have understood this term to mean as used in the Asserted Patents. Intrinsic evidence supports the distinction between a "narrowcast" connection as involving communication between a master and a group of slaves on an individual basis, whereas a "multicast" connection involves communication to a group of slaves collectively. Chmelar Decl. ¶ 203 (citing '9893 Patent at 4:58-60, 6:1-8 ("A narrowcast connection is a connection between one ANIP and one or more PNIPs, in which each transaction that the ANIP initiates is executed by exactly one PNIP.").

The implementations in the '9893 Patent also support NST's construction. For instance, the '9893 Patent discloses a narrowcast connection wherein "the target slave of the transaction is identified and the **transaction request is only sent to that particular slave**" such that "the request will only be visible to the target slave **and not to all of the slaves in the network**." Chmelar Decl. ¶ 205 (citing '9893 Patent at 5:49-52 (emphases added)); *see also id.* ¶ 206 (citing '9893 Patent at 7:9-13 ("**According to the address the master module M** or its active network interface port

ANIP **selects an appropriate simple connection**.”)[4] (emphases added)).[5]

J. “Data Communication”

Term	NST’s Construction	Defendants’ Construction
“data communication introducing a delay of M*N cycles” ’2893 Patent: claim 1	“data storage elements introducing a delay of M*N cycles”	Indefinite

NST’s proposed construction of “data communication” draws on language disclosed in the ’2893 Patent, to illustrate that the language in the claim is an obvious typographical error that would have immediately been understood by a POSITA to mean “data storage elements introducing a delay of M*N cycles.” Chmelar Decl. ¶¶ 213-214.

Claim 1 of the ’2893 Patent recites:

> An integrated circuit comprising: . . . **a data communication network comprising** . . . M*N **data storage elements**, M being a positive integer, the data communication **introducing a delay of M*N cycles** on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold.

’2893 Patent at Claim 1 (emphases added). Dr. Chmelar reviewed this language and noted that though Claim 1 recites M*N *data storage elements*, it then states that the *data communication* introduces a delay of M*N cycles. Chmelar Decl. ¶ 214. Based on this, Dr. Chmelar concluded that a POSITA would readily understand this to be a typographical error, where, on the one hand,

---

[4] A simple connection is “a connection between a first module and a single second module (*i.e.*, simple connection), . . .” Chmelar Decl. ¶ 203 (citing ’9893 Patent at 4:58-60).

[5] In fact, since a “narrowcast” connection shares many of the characteristics of a “multicast” connection, the ’9893 Patent discloses that “the functionality of a narrowcast connection can also be achieved using simple or multicast connections” by “using several simple connections to each slave module S.” *Id.* ¶ 206 (citing ’9893 Patent at 7:5-53).

"M*N data storage elements" are introduced, but on the other hand, "the *data communication*"—instead of "the *data storage elements*"—is introducing a delay of M*N cycles. *Id.*

Confirming Dr. Chmelar's conclusion, the '2893 Patent includes five independent claims, each of which describe M*N data storage elements, and each of which describe a delay of M*N cycles. However, every independent claim other than claim 1 describes *the data storage elements* introducing a delay of M*N cycles. *Id.* ¶ 215 (quoting '2893 Patent at Claim 4, Claim 7, Claim 10, Claim 11).

Further confirming Dr. Chmelar's opinion, the specification discloses "data **storage elements**"—not "the data communication"—as "introducing a delay a delay of M*N cycles." *Id.* ¶ 217 (citing '2893 Patent at Abstract, 2:12-13, 3:49-51, 5:55-56, 9:63-64). Likewise, "data **storage elements**"—not "the data communication"—are disclosed as the type of data storage circuitry that a POSITA would expect. *Id.* ¶ 217 (citing '2893 Patent at 6:24-26) (emphasis added).

K. "Optimal Moment"

Term	NST's Construction	Defendants' Construction
"an optimal moment for sending the data" '800 Patent: claim 12	Plain and ordinary meaning	Indefinite

The "optimal moment" term relates to sending data between a master and a slave. Claim 12 of the '800 Patent recites:

> at least one of the first determination unit and the second determination unit is further **configured to determine an optimal moment for sending the data** in said first wrapper or said second wrapper **according to communication properties of the communication between the master and the slave**.

'800 Patent at 12:16-21 (emphases added). The "optimal moment" term requires no construction beyond its plain and ordinary meaning. Defendants' position that this term is indefinite under §

112 is incorrect, as the term is readily understandable to a POSITA in light of the intrinsic and extrinsic evidence.

As Dr. Chmelar opines, a POSITA would understand "optimal moment" to relate to the "transmission moment" (*i.e.*, when transmission occurs) whereas the "transmission" would refer to the "data to be transmitted." Chmelar Decl. ¶ 221 (citing '800 Patent at 3:14, 7:4-6).

The specification further confirms that a POSITA would understand "transmission moment" to sufficiently disclose the "optimal moment." For example, the specification discloses:

> . . . the **transmission moment may be determined in a similar way** by the first and second determination means BLDU1, BLDU2. **For a guaranteed throughput GT connection, data should wait for one of the slots reserved for its connection.** Using a "flush"-like signal/flag may force the sending of the data in advance. Alternatively, **for a best effort BE connection, a round robin arbitration across connections in the NI can be used.**

'800 Patent at 7:4-14 (emphases added). Throughput is a communication property that encompasses guaranteed throughput (GT) as a lower bound whereas best effort (BE) does not. Chmelar Decl. ¶ 222. Further, as recited in claim 12, throughput is one of the connection properties that is used to determine the "optimal moment" for transmitting data. *See id.*; *see also* '800 Patent at 12:16-32 ("wherein the communication properties include . . . throughput where a lower bound on throughput is guaranteed"). Since the transmission moment is determined based on the same connection properties as the "optimal moment," a POSITA would understand an "optimal moment" to be the "transmission moment" (*i.e.*, the moment in which data transmitted), where the moment is based on the recited connection properties, including at least throughput. Chmelar Decl. ¶ 223. Accordingly, a POSITA would understand the term "optimal moment" to not be indefinite and should be afforded its plain and ordinary meaning.

Case law supports a plain and ordinary meaning construction for this term. *See, e.g.*, *Bitmicro LLC v. Kioxia America, Inc., et al.*, Case 6:22-cv-00331 (W.D. Texas Feb. 16, 2023)

(affording "optimal" a plain and ordinary meaning). A dictionary definition of "optimal" is "[m]ost favorable or desirable; optimum" and "optimum," which further means "[t]he point at which the condition, degree, or amount of something is the most favorable." Ex. 8. A plain and ordinary meaning is appropriate because claim 12 recites that the optimal moment is determined under a particular set of circumstances (*i.e.*, "according to communication properties"). Accordingly, extrinsic evidence supports a plain and ordinary meaning construction.

L. "Optimal Amount"

Term	NST's Construction	Defendants' Construction
"optimal amount of data to be buffered" '800 Patent: claim 12	Plain and ordinary meaning	Indefinite

Similarly, intrinsic evidence also confirms that "optimal amount" should be afforded its plain and ordinary meaning. Indeed, as Dr. Chmelar observes, multiple passages of the specification confirm that the '800 Patent discloses an invention for improving—indeed, for optimizing—interconnect utilization in a network, where the improvement is achieved by buffering data until conditions for an optimal transfer are satisfied. Chmelar Decl. ¶ 227 (citing '800 Patent at 3:35-37, 4:18-28, 4:49-57, 6:15-17,6:22-30, 6:31-36, 7:23-28, 7:44-51). From these passages, Dr. Chmelar concludes: (1) buffering of data improves and/or optimizes interconnect utilization; (2) the optimal amount of data to be buffered can be based on communication properties of a communication and (3) the optimal amount of data to be buffered can be specific to a particular interconnect. *Id.* ¶ 228. As Dr. Chmelar concludes, the "optimal amount of data" is not a fixed quantifier but based on certain conditions such as communication properties and/or interconnect characteristics. *Id.* Thus, a POSITA would understand that a "first optimal amount of data to be buffered" equates to the amount of data that is optimal under certain conditions. *Id.*

Affording this term its plain and ordinary meaning is also supported by case law, wherein the term "optimal" has been afforded its plain and ordinary meaning. *See, e.g.*, *Bitmicro LLC v. Kioxia America, Inc., et al.*, Case 6:22-cv-00331 (W.D. Texas Feb. 16, 2023). A POSITA would understand that the '800 Patent uses the term "optimal amount" in its plain and ordinary sense, *i.e.*, optimal amount of data to be buffered based on certain conditions, which is supported by dictionary definitions of the time that define "optimal" as the "[m]ost favorable or desirable; optimum" and "optimum," which further means "[t]he point at which the condition, degree, or amount of something is the most favorable." Ex. 8.

Defendants' position that "optimal amount" is indefinite is undermined by the '800 Patent's disclosure of when and how optimal transfer conditions are satisfied. Chmelar Decl. ¶ 227; *see also* '800 Patent at 4:18-28; 4:49-57; 6:15-17; 6:22-30; 6:31-36; 7:23-28; 7:44-51. The '800 Patent relates to optimizing interconnect utilization in a network, *id*. ¶ 227, by buffering data until optimal transfer conditions are satisfied. *Id.* (citing '800 Patent at 4:49-57) ("buffer data until the buffered data is sufficiently large to be transferred optimally over an interconnect means in a packet."); *see also id.* ("[t]he larger a packet is, the smaller is the amount of packet headers and therefore the overhead is reduced and the interconnect is utilized more efficiently."). The data are only transferred when sufficient data have been buffered to provide the optimal packet size. *Id.* Thus, a POSITA would not consider this term to be indefinite. *Id*. ¶ 227.

VI. <u>Conclusion</u>

For the foregoing reasons, Plaintiff respectfully requests that the Court adopts its proposed claim construction positions.

Date: September 27, 2023

Respectfully submitted,

/s/ Daniel S. Stringfield w/ permission William E. Davis, III

William E. Davis, III
Texas Bar No. 24047416
Ty Wilson
DAVIS FIRM PC
213 N. Fredonia Street, Suite 230
Longview, TX 75601
903-230-9090
bdavis@davisfirm.com
twilson@davisfirm.com

Daniel S. Stringfield (lead counsel)
NIXON PEABODY LLP
70 West Madison St., Suite 5200
Chicago, IL 60602
312-977-4130
dstringfield@nixonpeabody.com
nst@nixonpeabody.com

Erica J. Van Loon
Vincent C. Capati
NIXON PEABODY LLP
300 S. Grand Avenue, Suite 4100
Los Angeles, CA 90071
213-629-6000
evanloon@nixonpeabody.com
vcapati@nixonpeabody.com

David R. Kocan
NIXON PEABODY LLP
One Embarcadero Center, 32nd Floor
San Francisco, CA 94111
415-984-8282
dkocan@nixonpeabody.com

Attorneys for Plaintiff
Network System Technologies, LLC

CERTIFICATE OF SERVICE

I hereby certify that all counsel of record are being served on September 27, 2023 with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3).

/s/ William E. Davis, III