

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner

v.

NETWORK SYSTEM TECHNOLOGIES, LLC,
Patent Owner

U.S. PATENT NO. 8,086,800

Case IPR2024-00339

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	BACKGROUND OF THE '800 PATENT	1
A.	Claims.....	2
B.	Overview of the '800 Patent.....	2
C.	Prosecution History of the '800 Patent	3
III.	IDENTIFICATION AND BASIS OF CHALLENGE	3
IV.	OVERVIEW OF THE ASSERTED PRIOR ART	5
A.	Rădulescu	5
B.	Bahadiroglu	6
C.	Petersen.....	6
D.	Rădulescu-WO	7
V.	LEVEL OF ORDINARY SKILL IN THE ART	8
VI.	CLAIM CONSTRUCTION.....	8
VII.	THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	9
A.	Ground 1: Claims 1, 2, 4, 6, 8–12, 13, and 18–21 Are Rendered Obvious by Rădulescu in view of Bahadiroglu.....	9
1.	Motivation to Combine Rădulescu and Bahadiroglu.....	9
2.	Claim 12.....	13
3.	Claim 13	35
4.	Claim 18.....	36
5.	Claim 19.....	37
6.	Claim 20	38

Petition for *Inter Partes* Review of U.S. Patent No. 8,086,800

7.	Claim 21	39
8.	Claim 10	39
9.	Claim 1	41
10.	Claim 2	42
11.	Claim 4	43
12.	Claim 6	43
13.	Claim 8	44
14.	Claim 9	45
15.	Claim 11	46
B.	Ground 2: Claims 1, 2, 4, 6, 8–12, 13, and 18–21 Are Rendered Obvious by Rădulescu in view of Petersen	47
1.	Motivation to Combine Rădulescu and Petersen	47
2.	Claim 12	50
3.	Claim 13	56
4.	Claim 18	56
5.	Claim 19	56
6.	Claim 20	56
7.	Claim 21	56
8.	Claim 10	56
9.	Claim 1	58
10.	Claim 2	58
11.	Claim 4	58
12.	Claim 6	59

13.	Claim 8.....	59
14.	Claim 9.....	59
15.	Claim 11	59
C.	Ground 3: Claims 1, 2, 4, 6, 8–12, 13, and 18–21 Are Rendered Obvious by Rădulescu in view of Bahadiroglu and Rădulescu- WO	60
1.	Motivation to Combine Rădulescu, Bahadiroglu, and Rădulescu-WO	60
2.	Claim 12.....	61
3.	Claim 13.....	64
4.	Claim 18.....	64
5.	Claim 19.....	64
6.	Claim 20.....	64
7.	Claim 21	65
8.	Claim 10.....	65
9.	Claim 1	66
10.	Claim 2.....	67
11.	Claim 4.....	67
12.	Claim 6.....	67
13.	Claim 8.....	67
14.	Claim 9.....	67
15.	Claim 11	68
D.	Ground 4: Claims 1, 2, 4, 6, 8–12, 13, and 18–21 Are Rendered Obvious by Rădulescu in view of Petersen and Rădulescu-WO	68

1.	Motivation to Combine Rădulescu, Petersen, and Rădulescu-WO	68
2.	Claim 12	69
3.	Claim 13	70
4.	Claim 18	70
5.	Claim 19	70
6.	Claim 20	70
7.	Claim 21	70
8.	Claim 10	70
9.	Claim 1	72
10.	Claim 2	72
11.	Claim 4	72
12.	Claim 6	72
13.	Claim 8	72
14.	Claim 9	73
15.	Claim 11	73
E.	Secondary Considerations of Non-Obviousness	73
VIII.	PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION.....	74
A.	Discretionary Denial Under 35 U.S.C. § 325(d) is Not Warranted	74
B.	Discretionary Denial Under 35 U.S.C. § 314(a) is Not Warranted	76
IX.	MANDATORY NOTICES	77
A.	Real Party-In-Interest	77

B.	Related Matters.....	78
C.	Counsel Information.....	78
D.	Service Information.....	79
X.	PAYMENT OF FEES	79
XI.	CERTIFICATION.....	79
XII.	CONCLUSION	79
	Claims Listing Appendix.....	81

TABLE OF AUTHORITIES

	Page(s)
 Cases	
<i>Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH</i> , IPR2019-01469, Paper 6 (P.T.A.B. Feb. 13, 2020).....	74
<i>Apple Inc. v. Fintiv, Inc.</i> , IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020).....	76, 77
<i>Becton, Dickinson, & Co. v. B. Braun Melsungen AG</i> , IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017)	74
<i>Bowtech Inc. v. MCP IP, LLC</i> , IPR2019-00383, Paper 14 (P.T.A.B. Aug. 6, 2019).....	75
<i>CommScope Techs. LLC v. Dali Wireless, Inc.</i> , IPR2022-01242, Paper 23 (Feb. 27, 2023)	77
<i>Fasteners for Retail, Inc. v. RTC Indus., Inc.</i> , IPR2019-00994, Paper 9 (P.T.A.B. Nov. 5, 2019).....	74
<i>Hulu, LLC v. Sound Innovations, LLC</i> , IPR2018-01039, Paper 29 (P.T.A.B. Dec. 20, 2019)	4
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005) (<i>en banc</i>)	8
<i>Sotera Wireless, Inc. v. Masimo Corp.</i> , IPR2020-01019, Paper 12 (P.T.A.B. Dec. 1, 2020)	76
<i>Thryv, Inc v. Click-To-Call Techs., LP</i> , 140 S. Ct. 1367 (2020).....	77
<i>Wyers v. Master Lock Co.</i> , 616 F.3d 1231 (Fed. Cir. 2010)	73
 Statutes	
35 U.S.C.	
§ 102.....	3
§ 102(a)	3, 4

§ 102(b).....	3, 4
§ 102(e)	4
§ 103.....	3, 5
§ 112.....	22
§ 112(6).....	23
§ 311(b).....	4
§ 314(a)	76
§ 315(e)(1)	79
§ 325(d).....	74
§ 371.....	2

Other Authorities

37 C.F.R.

§ 42.10(b).....	79
§ 42.15(a)(1)	79
§ 42.100(b).....	8

LIST OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 8,086,800 (“the ’800 Patent”)
1002	Declaration of Todd Mowry in Support of Petition for <i>Inter Partes</i> Review of U.S. Patent No. 8,086,800
1003	Curriculum Vitae for Todd Mowry
1004	Prosecution History of U.S. Patent No. 8,086,800
1005	Andrei Rădulescu <i>et al.</i> , <i>An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration</i> , 2 PROC. DESIGN, AUTOMATION AND TEST IN EUR. CONF. & EXHIBITION 878 (2004) (“Rădulescu”)
1006	U.S. Patent Application Publication No. 2002/0186660 to Murat I. Bahadiroglu <i>et al.</i> (“Bahadiroglu”)
1007	U.S. Patent No. 5,434,872 to Brian Petersen <i>et al.</i> (“Petersen”)
1008	International Patent Publication No. WO 2004/034176 A2 to Rădulescu <i>et al.</i> (“Rădulescu-WO”)
1009	Axel Jantsch and Hannu Tenhunen, <i>Networks on Chip</i> (2003)
1010	Kees Goossens <i>et al.</i> , <i>Chapter 4: Guaranteeing the Quality of Services in Networks on Chip</i> , NETWORKS ON CHIP, at 61–82 (2003)
1011	Defs.’ Joint Opening Claim Construction Br., <i>Network Sys. Techs., LLC v. Qualcomm Inc.</i> , No. 1:22-cv-1331, Dkt. 77 (E.D. Tex. Oct. 12, 2023)
1012	Amit Goel & William R. Lee, <i>Formal Verification of an IBM CoreConnect™ Processor Local Bus Arbiter Core</i> , PROCEEDINGS OF THE 37TH ANNUAL DESIGN AUTOMATION CONFERENCE 196–200 (2000)
1013	Luca Benini & Giovanni De Micheli, <i>Networks on Chips: A New SoC Paradigm</i> , 35 COMPUTER 70–78 (2002)
1014	Erik Jan Marinissen, <i>Wrapper Design for Embedded Core Test</i> , IEEE INT’L TEST CONFERENCE (ITC) 1–10 (2000)

1015	Terry Tao Ye <i>et al.</i> , <i>Packetization and Routing Analysis of On-Chip Multiprocessor Networks</i> , J. SYS. ARCHITECTURE, Vol. 50, Issues 2-3, pp 81-104 (2004)
1016	Zhonghai Lu <i>et al.</i> , Network-on-Chip Assembler Language, RETRIEVED FROM INSTITUTE OF MICROELECTRONICS AND INFORMATION TECHNOLOGY, ROYAL INSTITUTE OF TECHNOLOGY (KTH) (2003); available at https://people.kth.se/~zhonghai/Archive/NoC-AL-V01.pdf
1017	Declaration of Gordon MacPherson
1018	David E. Culler <i>et al.</i> , <i>Parallel Computer Architecture</i> (1998)
1019	John Heinlein <i>et al.</i> , <i>Coherent Block Data Transfer in the FLASH Multiprocessor</i> , IEEE PROCEEDINGS 11TH INT’L PARALLEL PROCESSING SYMPOSIUM, Genva, Switzerland, pp. 18-27 (1997)
1020	Pl.’s Opening Claim Construction Br., <i>Network Sys. Techs., LLC v. Tex. Instruments Inc.</i> , No. 2:22-cv-00482-RWS, Dkt. 98 (E.D. Tex. Sept. 27, 2023)
1021	Pl.’s Responsive Claim Construction Br., <i>Network Sys. Techs., LLC v. Qualcomm Inc.</i> , No. 1:22-cv-1331-DAE, Dkt. 81 (W.D. Tex. Nov. 16, 2023)
1022	Wael Badawy, <i>System on Chip: The Challenge and Opportunities</i> , SYSTEM ON CHIP FOR REAL-TIME APPLICATIONS, 3–16 (2003)
1023	Ahmed Amine Jerraya & Wayne Wolf, <i>Multiprocessor Systems-on-Chips</i> (2005)
1024	Ann Marie Rincorn <i>et al.</i> , <i>The Changing Landscape of System-on-a-Chip Design</i> , IEEE 1999 CUSTOM INTEGRATED CIRCUITS CONF. 83–90 (1999)
1025	Shashi Kumar <i>et al.</i> , <i>A Network on Chip Architecture and Design Methodology</i> , PROCEEDINGS OF THE IEEE COMPUTER SOC’Y ANN. SYMPOSIUM ON VLSI (ISVLSI’02) (2002)
1026	Luca Benini & Giovanni De Micheli, <i>Chapter 16: Energy-Efficient System-Level Design</i> , POWER AWARE DESIGN METHODOLOGIES 473–516 (2002)
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1030	John Heinlein <i>et al.</i> , <i>Integration of Message Passing and Shared Memory in the Stanford FLASH Multiprocessor</i> , ACM SIGOPS OPERATING SYSTEMS REVIEW, Vol. 28, Issue 5, pp 38–50 (1994)
1031	Hugo De Man, <i>System-on-Chip Design: Impact on Education and Research</i> , IEEE DESIGN & TEST OF COMPUTERS, Vol. 16, No. 3, pp. 11-19, (July-Sept. 1999)
1032	William J. Dally <i>et al.</i> , <i>Route Packets, Not Wires: On-Chip Interconnection Networks</i> , PROCEEDINGS OF THE 38TH DESIGN AUTOMATION CONF. (IEEE Cat. No.01CH37232), Las Vegas, NV, USA, 2001, pp. 684-689 (2001)
1033	Andrei Rădulescu <i>et al.</i> , <i>Communication Services for Networks on Chip</i> . SIGNAL PROCESSING AND COMMUNICATIONS (2000)
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1035	Ahmed Hemani <i>et al.</i> , <i>Network on Chip: An Architecture for Billion Transistor Era</i> (2001)
1036	Daniel Wiklund <i>et al.</i> , <i>Design of a System-on-Chip Switched Network and Its Design Support</i> , IEEE 2002 INT’L CONF. ON COMMC’NS, CIRCUITS & SYS. & WEST SINO EXPOSITIONS, Chengdu, China, pp. 1279-1283 Vol.2 (2002)

Samsung Electronics Co., Ltd. (“Petitioner”) respectfully requests *inter partes* review of claims 1, 2, 4, 6, 8–12, 13, and 18–21 (“Challenged Claims”) of U.S. Patent No. 8,086,800 (the “’800 Patent”) (Ex-1001).

I. INTRODUCTION

The ’800 Patent is directed to an integrated circuit having processing modules and a network in which data is buffered until it reaches an optimal amount and transmitted over the network at an optimal moment determined based on communication properties.

But the claimed invention is unpatentable because such integrated circuits would have been obvious. Network on chip (“NoC”) structures connecting processing modules, buffering an optimal amount of data in a network interface, and transmitting data over a network at an optimal moment based on network conditions or communication properties were all known. Skilled artisans would have been motivated to combine these known network-related concepts and reasonably expected that combination to succeed. That is illustrated by the prior art grounds relied upon in this Petition, none of which was considered by the Examiner during prosecution of the ’800 Patent.

II. BACKGROUND OF THE ’800 PATENT

The ’800 Patent issued on December 27, 2011, from U.S. Application No. 11/569,083 (Ex-1004, “the ’083 Application”), which was filed on Nov. 14, 2006.

The '083 Application is a national stage application (under 35 U.S.C. § 371) of PCT/IB2005/051580, which was filed on May 13, 2005. The '800 Patent claims priority to EP Application No. 04102189, which was filed on May 18, 2004.

A. Claims

The '800 Patent has 21 claims. Claims 1, 2, 4, 6, 8–12, 13, and 18–21 are challenged here, four of which are independent.

B. Overview of the '800 Patent

The '800 Patent states it is “an object of the invention to provide an integrated circuit” and “a method for buffering” data in that circuit. Ex-1001 at 3:35–37, 4:29–36. The integrated circuit includes “a plurality of processing modules” called “intellectual property blocks” (or “IPs”) that communicate with one another via “a network on chip NOC.” *Id.*, 3:38–41, 5:10–11, 5:51–55. Network interfaces “NI” connect master and slave IP modules and manage communication between them. *Id.*, 5:39–47, 5:55–57.

The '800 Patent states that data from the IP blocks are buffered in the network interfaces “until the conditions for an optimal transfer are satisfied.” *Id.*, 5:58–64, 6:15–17; *see id.*, 7:23–25. Data is transferred over the network interconnect “as a packet within a certain burst length” that is “adopted to suit the network N in order to improve the network utilization.” *Id.*, 5:64–66, 6:4–6. The '800 Patent states this

is implemented using “determination units” in the network interfaces, which are also used to determine “the transmission moment.” *Id.*, 6:47-53, 7:4–6; *see id.*, 7:7–14.

C. Prosecution History of the ’800 Patent

The ’083 application was originally filed with fourteen claims directed to an integrated circuit, method of buffering data, and data processing system. Ex-1004 at 8–13, 66. Throughout prosecution, the claims were repeatedly rejected as obvious over the prior art, *id.*, 73–82, 119–34, 204–18, 258–74, 330–49, 410–29, leading some claims to be cancelled, others to be repeatedly narrowed through amendment, and others to be added. *Id.*, 94–105, 147–57, 240–50, 308–19, 391–402, 475–87. After six rounds of rejections and narrowing amendments, the claims were allowed. *Id.*, 497, 652.

III. IDENTIFICATION AND BASIS OF CHALLENGE

Petitioner’s challenge is based on the following prior art:

- **Rădulescu** – Andrei Rădulescu *et al.*, *An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration* (Ex-1005), published no later than February 20, 2004, is prior art under 35 U.S.C. §§ 102(a) and (b).¹

¹ Cites to 35 U.S.C. §§ 102 and 103 are to the pre-AIA version applicable here.

- **Bahadiroglu** – U.S. Patent Application Publication No. 2002/0186660 to Bahadiroglu *et al.* (Ex-1006), filed June 12, 2001 and published December 12, 2002, is prior art under 35 U.S.C. §§ 102(a), (b), and (e).
- **Petersen** – U.S. Patent No. 5,434,872 to Petersen *et al.* (Ex-1007), filed July 1992 and issued July 18, 1995, is prior art under 35 U.S.C. §§ 102(a), (b), and (e).
- **Rădulescu-WO** – International Patent Publication No. WO 2004/034176 to Rădulescu *et al.* (Ex-1008), filed October 7, 2003 and published April 22, 2004, is prior art under 35 U.S.C. §§ 102(a), (b), and (e).

Rădulescu is a printed publication pursuant to 35 U.S.C. § 311(b) because it was published and publicly available before the '800 Patent's priority date. Ex-1005; *Hulu, LLC v. Sound Innovations, LLC*, IPR2018-01039, Paper 29 at 17-19 (P.T.A.B. Dec. 20, 2019) (precedential). Supporting documentation and testimonial evidence further demonstrate that it is a printed publication that was publicly available before the '800 Patent's priority date. Ex. 1017; *Hulu*, Paper 29 at 12-14, 17-21.

Petitioner requests IPR and cancellation of the Challenged Claims on the following grounds:

Ground	Basis	Challenged Claim(s)	Reference(s)
1	§ 103	1, 2, 4, 6, 8–12, 13, 18–21	Rădulescu, Bahadiroglu
2	§ 103	1, 2, 4, 6, 8–12, 13, 18–21	Rădulescu, Petersen

Ground	Basis	Challenged Claim(s)	Reference(s)
3	§ 103	1, 2, 4, 6, 8–12, 13, 18–21	Rădulescu, Bahadiroglu, Rădulescu-WO
4	§ 103	1, 2, 4, 6, 8–12, 13, 18–21	Rădulescu, Petersen, Rădulescu-WO

Section VII details the statutory grounds for unpatentability of the Challenged Claims. Additional evidence is provided in the accompanying Declaration of Dr. Todd Mowry (Ex-1002) and other supporting exhibits.

IV. OVERVIEW OF THE ASSERTED PRIOR ART

A. Rădulescu

Rădulescu discloses “a network interface for an on-chip network”—the *Æthereal* NoC—that “is intended for systems on chip (SoC).” Ex-1005 at 1. Communication over the NoC “is performed using a transaction-based protocol, where master IP modules issue request messages ... that are executed by the addressed slave modules, which may respond with a response message” *Id.*, figs. 8–9. Rădulescu discloses that data messages are buffered until “the amount of sendable data” satisfies “a configurable threshold,” at which point a “scheduler” determines the data can be transmitted over a router network. *Id.*, 3–4, fig. 2. This mechanism is intended “[t]o optimize the NoC utilization.” *Id.*, 4. Rădulescu’s NoC is depicted in Figure 8. Ex-1002 ¶52.

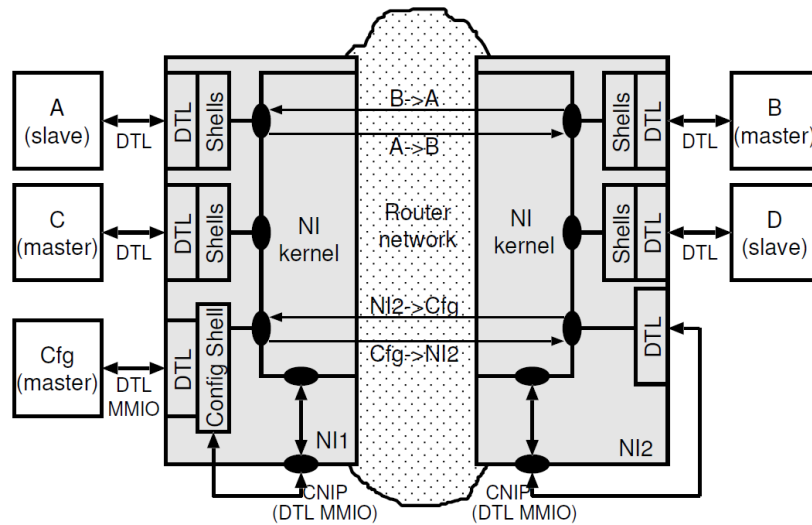


Figure 8. NI configuration

B. Bahadiroglu

Bahadiroglu discloses “[a]n adaptive packet mechanism and method for optimizing data packet transmission through a network connection between a sending node and a receiving node” based on real-time network conditions. Ex-1006 at Abstract; [0047]–[0048]. Bahadiroglu describes measuring connection properties and network conditions, and determining “an optimum packet size and an optimum inter-packet interval for transmission of packet data between the sending node and the receiving node” of a network. *Id.*, [0048]; Ex-1002 ¶53.

C. Petersen

Petersen discloses “an architecture for a network interface controller” that “optimize[s] performance” of a host by using “a dedicated transmit buffer.” Ex-1007 at 2:14–16, 2:31–34, 2:56–61. It describes comparing “the amount of data” in the buffer to a “threshold value” to determine when a sufficient amount of data is present

in the buffer to transmit it over the network. *Id.*, 2:16–31, 2:49–53, 4:61–5:13; *see id.*, Abstract. Petersen’s “threshold value” is “dynamically programmable” based on “status information”—such as “indications of underrun conditions”—to optimize the threshold value and thus “optimize performance” of the host. *Id.*, 2:31–34, 4:40–47, 4:56–60; Ex-1002 ¶54.

D. Rădulescu-WO

Rădulescu-WO discloses “an integrated circuit comprising a plurality of processing modules,” including “a network arranged for providing connections between [master and slave] processing modules.” Ex-1008 at Abstract, 1:1–3, 12:5–10. Those connections have a set of “properties” that may be used to efficiently adapt the connections to their requirements. *Id.*, 9:10–21, 11:5–22. An example of Rădulescu-WO’s integrated circuit is depicted in Figure 3. Ex-1002 ¶55.

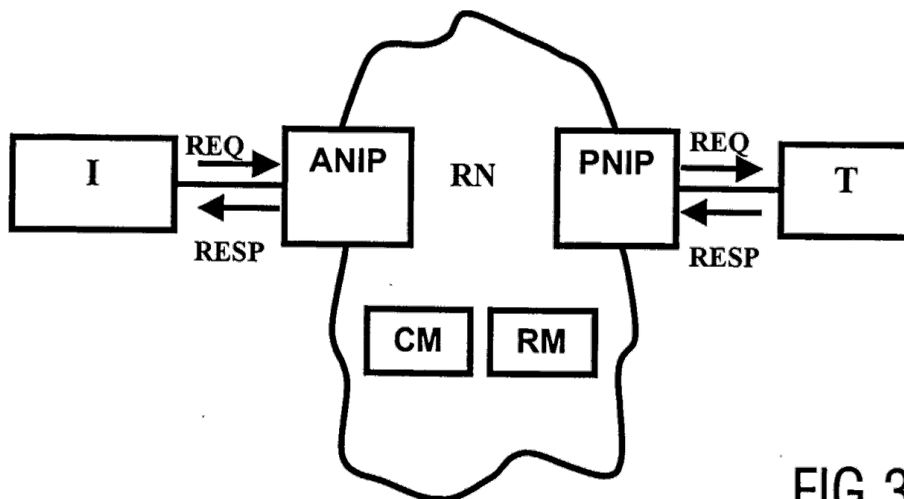


FIG.3

V. LEVEL OF ORDINARY SKILL IN THE ART

As described by Dr. Mowry, a person of ordinary skill in the art (“POSITA”) at the time of the alleged invention would have had at least a Bachelor’s degree in computer science, electrical engineering, computer engineering, or an equivalent technical degree, and two or more years of experience with system-on-chip, interconnect, or networking technologies. Ex-1002 ¶¶48–50. Additional education would compensate for less experience, and vice-versa. *Id.*

The result would be the same under the level of ordinary skill in the art that PO has proposed in related district court proceedings: “a Bachelor of Science (or equivalent) degree in electrical engineering, computer engineering, or a related field, and 2-3 years of work experience in very large-scale integrated (‘VLSI’) systems, such as application-specific integrated circuits (‘ASICs’), application-specific standard parts (‘ASSPs’), system-on-chip (‘SoC’), or field-programmable gate arrays (‘FPGAs’), and has an understanding of on-chip interconnection networks.” Ex-1021 at 13; Ex-1002 ¶51.

VI. CLAIM CONSTRUCTION

Claims in an IPR are construed under the claim construction principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*); 37 C.F.R. § 42.100(b). For the purposes of this proceeding only, Petitioner does not believe any claim terms need to be construed to resolve the prior art issues presented in this

Petition. Petitioner reserves the right to identify terms for construction in litigation concerning the '800 Patent, and to respond to any constructions that PO submits.

VII. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: Claims 1, 2, 4, 6, 8–12, 13, and 18–21 Are Rendered Obvious by Rădulescu in view of Bahadiroglu

1. Motivation to Combine Rădulescu and Bahadiroglu

A POSITA would have been motivated to combine the teachings of Rădulescu with those of Bahadiroglu in order to create a NoC with improved performance and efficiency. Ex-1002 ¶¶56–63.

Rădulescu discloses “a network interface for an on-chip network,” which supports data communication between “IP modules.” Ex-1005 at 1. Rădulescu discloses a method of “optimiz[ing] the NoC utilization” using a “configurable threshold mechanism” to determine when the “amount of sendable data” queued in the network interface is sufficiently large. Ex-1005 at 4. This mechanism produces longer packets that use the NoC more efficiently. *Id.*; Ex-1002 ¶58. Although Rădulescu does not expressly specify how its configurable threshold mechanism is implemented, a POSITA would have understood that this threshold could be set either with a fixed value (*e.g.*, programmed into a register) or with an adjustable value that changes at runtime based on conditions in the NoC. Ex-1002 ¶58.

Indeed, Bahadiroglu discloses an example of a runtime-adjustable implementation for a threshold mechanism. Ex-1002 ¶59. Bahadiroglu is directed to

the same goal of optimizing network utilization, and a POSITA would have been motivated to combine Rădulescu's disclosures with Bahadiroglu's disclosures regarding a runtime-adjustable implementation to obtain the benefits of Bahadiroglu's known solution to network optimization. *Id.* In particular, a POSITA would have looked to Bahadiroglu's disclosure of "an adaptive packet mechanism" as a means of setting the configurable threshold described by Rădulescu and scheduling packet transmissions. Ex-1002 ¶¶59–60. Bahadiroglu describes that this mechanism "periodically determine[s]" the "current network conditions" and uses those conditions to "adjust[] the transmitted packet size ... in real time to that optimum for the current network and connection bandwidth" and/or other network properties. Ex-1006, [0048], [0071]. Bahadiroglu's mechanism also determines the most optimal timing for the transmission of those packets, *i.e.*, the "inter-packet interval." *Id.* Bahadiroglu describes determining the optimal packet size and transmission timing based on various communication properties, including "the amount and type of data to be transmitted" and "network conditions" that include latency, jitter, available bandwidth, and traffic conditions. *See id.*, [0048], [0071], [0107], [0111]–[0114].

A POSITA would have understood that using Bahadiroglu's mechanism would improve the performance and efficiency of Rădulescu's NoC by adjusting both the packet size and transmission timing based on real-time network conditions,

providing the most optimal usage of the NoC. Ex-1002 ¶60. A POSITA would have recognized that doing so would enable larger packets to be sent when network conditions allow, reducing the number of packet headers that must be sent and allowing more data to travel over the NoC. *Id.* Real-time adaptation would also prevent the transmission of packets that are too large for the current network conditions, which could otherwise result in buffers overflowing and packets being dropped, necessitating wasteful retransmissions. *Id.* Similarly, optimizing the packet transmission timing based on current network conditions would maximize usage of the network bandwidth and manage traffic, increasing the likelihood of successful transmissions. *Id.* Indeed, Bahadiroglu itself explains that “efficient bandwidth and traffic management is essential to obtain full advantage of the bandwidth and capacity of a network.” Ex-1006 at [0011]; *see id.*, [0013]–[0014]. Moreover, Rădulescu’s NoC is contemplated “for highly complex chips,” Ex-1005 at 1, and Bahadiroglu’s mechanism is offered as a solution to the “extreme[] difficult[y]” of “determin[ing] the optimum operating parameters” in highly complex networks. Ex-1006 at [0033]. For those reasons, a skilled artisan would have been motivated to combine Rădulescu’s and Bahadiroglu’s teachings to arrive at the claimed invention.

A POSITA would have further reasonably expected this combination to succeed. They would have understood that combining Rădulescu and Bahadiroglu merely combines prior art elements according to known methods to yield predictable

results. Ex-1002 ¶¶61–63. Moreover, both Rădulescu and Bahadiroglu occupy the same field of optimizing data communication in a network. *Id.* As such, a POSITA would have reasonably expected that use of Bahadiroglu’s known technique for optimizing data communication in a network through its adaptive packet mechanism would improve Rădulescu’s NoC in the same way. *Id.* It would require nothing more than routine implementation details to combine Bahadiroglu’s mechanism with Rădulescu’s NoC, and Bahadiroglu provides an extensive disclosure of such implementation details throughout its specification. *Id.* A POSITA would also have understood that Bahadiroglu’s disclosure is applicable to networks on chip, including because Bahadiroglu’s adaptive packet mechanism disclosure would optimize rather than exhaust the resources in Rădulescu’s NoC while simultaneously maximizing bandwidth, capacity, and traffic management efficiencies through Rădulescu’s NoC at minimal resource cost. *Id.* For example, Bahadiroglu describes an implementation that combines known analyzers to achieve a system that is relatively efficient, requires relatively little processing resources, and is relatively fast, which is optimal for on-chip services. *Id.* A POSITA would have understood that combining Rădulescu and Bahadiroglu effectively balances NoC optimization with implementation cost and complexity. *Id.*

2. Claim 12

For ease of presentation, the analysis of the Challenged Claims begins with claim 12, and then addresses the other challenged claims. Rădulescu in view of Bahadiroglu teaches all the limitations of claim 12 and thus would have rendered it obvious. Ex-1002 ¶¶56, 64–105.

a. Claim 12[pre]: “An integrated circuit comprising”

To the extent the preamble is limiting, Rădulescu discloses an integrated circuit. Ex-1002 ¶¶66–69. Rădulescu “present[s] a network interface for an on-chip network” (*i.e.*, a NoC) and states that its network interface “is intended for systems on chip (SoC).” Ex-1005 at 1. A POSITA would have understood that SoCs are integrated circuits, and that Rădulescu’s “on chip network” and the components that interface therewith are implemented on the same integrated circuit. Ex-1002 ¶¶33–38, 67–68. Indeed, the ’800 Patent describes its alleged invention in the context of SoCs and discloses “a network on chip” as an embodiment of the alleged invention. Ex-1001 at 1:14–58, 4:66–5:11, 5:36–37, 6:7–8, figs. 1–2.

b. Claim 12[a]: “a plurality of processing modules including a first processing module having a first processing memory and a second processing module having a second processing memory”

Rădulescu discloses this limitation. Ex-1002 ¶¶70–74. Rădulescu discloses a plurality of processing modules called “IP modules,” including “master IP modules” and “slave modules.” Ex-1005 at 1; *see id.* at 2, 5, fig. 9. Rădulescu’s Figure 8

depicts such modules, including “B (master)” (*i.e.*, first processing module) and “A (slave)” (*i.e.*, second processing module), annotated in red below.

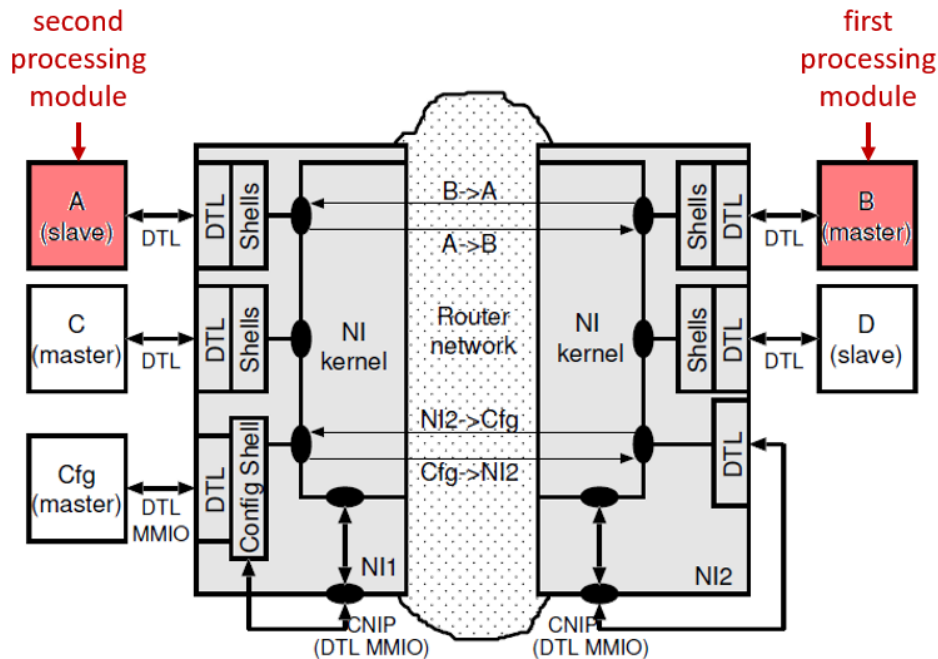


Figure 8. NI configuration

Id., fig. 8 (annotated).

A POSITA would have also understood that the “IP modules” are processing modules having processing memory. Ex-1002 ¶¶71–74; Ex-1005 at 1–4 (describing “IP modules”). For example, Rădulescu describes that these modules perform “computation,” execute commands, and read and write data. *Id.*, 1–2. A POSITA would have understood that these functions involve processing and that the IP modules would require local processing memory, such as a cache, to perform these functions. Ex-1002 ¶71. To the extent PO argues that Rădulescu does not explicitly disclose such processing memory, IP modules that perform processing and include

processing memory were well-known, and a POSITA would have found it obvious to include such modules in a system like the one described by Rădulescu. Ex-1002 ¶72 (citing Ex-1008 at 12:13–15 (describing “intellectual property blocks IPs (computation elements, memories or a subsystem ...)”), 6:7–9 (describing modules with “a memory, or a register”); Ex-1025 at 3–4 (describing “processor and DSP cores provided with caches as well as local memories”), Fig. 3; Ex-1016 at 14 (“microprocessors usually have local caches,” “each node has its own local portion of the global main memory”), Fig. 2.5; Ex-1026 at 5–6 (describing a CPU core with registers, local caches, and scratch-pad RAM), 8–9 (describing audio and video cores comprising processors, local caches, and local memory)).

Rădulescu’s disclosure of processing modules having processing memory is at least commensurate with the disclosure in the ’800 Patent, which describes that “the first processing module is a master” and “the second processing module is a slave,” and states “[t]he modules ... can be so-called intellectual property blocks IPs (computation elements, memories or a subsystem which may internally contain interconnect modules)” Ex-1001 at 5:51–55, 8:48–51, 10:67–11:3; *see id.*, 5:37–39 (disclosing “a master module M and a slave module S”), 7:35–40 (stating “the master M or the slave S ... may constitute intellectual property blocks”), 5:58–6:6, 6:37–38. Therefore, in Rădulescu, each master IP module (including master B) is a first processing module having first processing memory and each slave IP module

(including slave A) is a second processing module having second processing memory. Ex-1002 ¶¶70–74.

- c. **Claim 12[b]: “a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module”**

Rădulescu discloses this limitation. Ex-1002 ¶¶75–76. Rădulescu explains that its NoC includes a plurality of “network interface[s] (NI)” that facilitate transaction-based communication between the processing modules and the network. Ex-1005 at 1–4. Rădulescu’s Figure 8, annotated below, depicts a network interface NI2 (*i.e.*, first interconnect module) connected to the “B (master)” IP module (*i.e.*, first processing module) and a network interface NI1 (*i.e.*, second interconnect module) connected to the “A (slave)” IP module (*i.e.*, second processing module). *Id.*, 5.

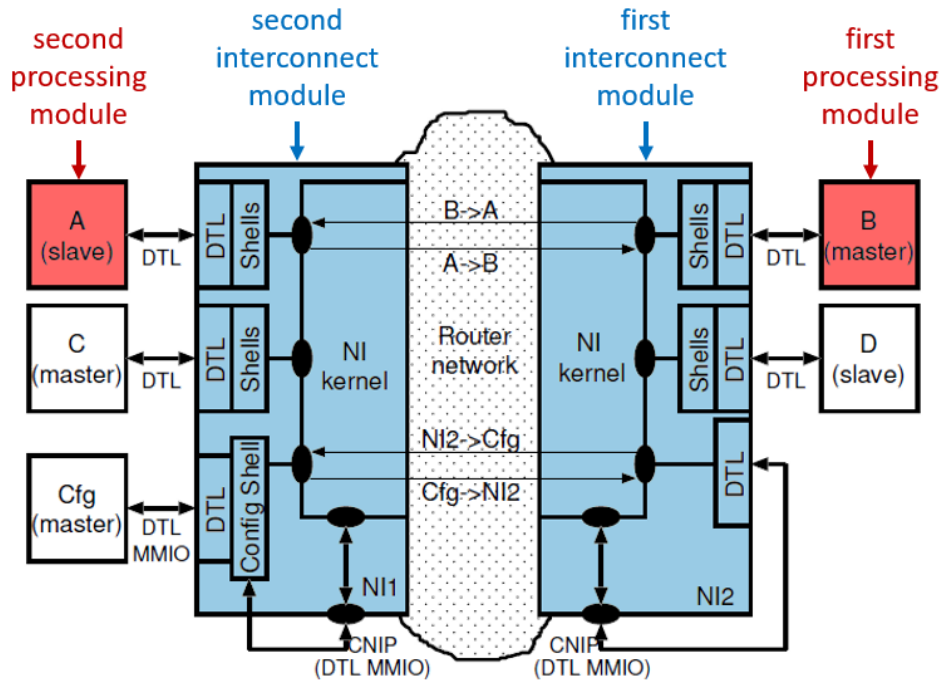


Figure 8. NI configuration

Id., fig. 8 (annotated); *see id.*, figs. 1–6. Rădulescu’s network interfaces match the interconnect modules disclosed in the ’800 Patent. *See, e.g.*, Ex-1001 at 5:36–50 (disclosing that each “master module M” and “slave module S” is “connected to a network” via “associated network interface[s] NI”), 6:7–30 (similar), figs. 1–2.

- d. **Claim 12[c]: “a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module, wherein the first interconnect module is connected between the first processing module and the network, and wherein the second interconnect module is connected between the second processing module and the network”**

Rădulescu discloses this limitation. Ex-1002 ¶¶77–79. Rădulescu describes that its NoC comprises a network of routers for connecting network interfaces to

provide a connection for transaction-based communications between master and slave IP modules. *Id.* ¶¶77–78; Ex-1005 at 1, 3–5. For example, Rădulescu states “[n]etworks are composed of routers, which transport the data from one place to another, and network interfaces (NI), which implement the interface to the IP modules.” Ex-1005 at 1. Rădulescu further states that the network interfaces include components used to facilitate communication between “the IP modules” through the router network. *Id.*, 3, 6. Rădulescu also describes and depicts connections between processing modules that permit communication of requests and responses between those modules over the network using channels connecting the NI interconnect modules. *Id.*, 5, fig. 9. Rădulescu states these “[c]onnections can be opened and closed at any time.” *Id.*, 2.

In Figure 8 of Rădulescu, the network is illustrated as “router network” (shown in green), which connects the first interconnect module NI2 to the second interconnect module NI1 in order to provide a communication connection between the first processing module master B and the second processing module slave A (*e.g.*, depicting “B -> A” and “A -> B” over the “router network,” as shown in the red box). *Id.*, 5.

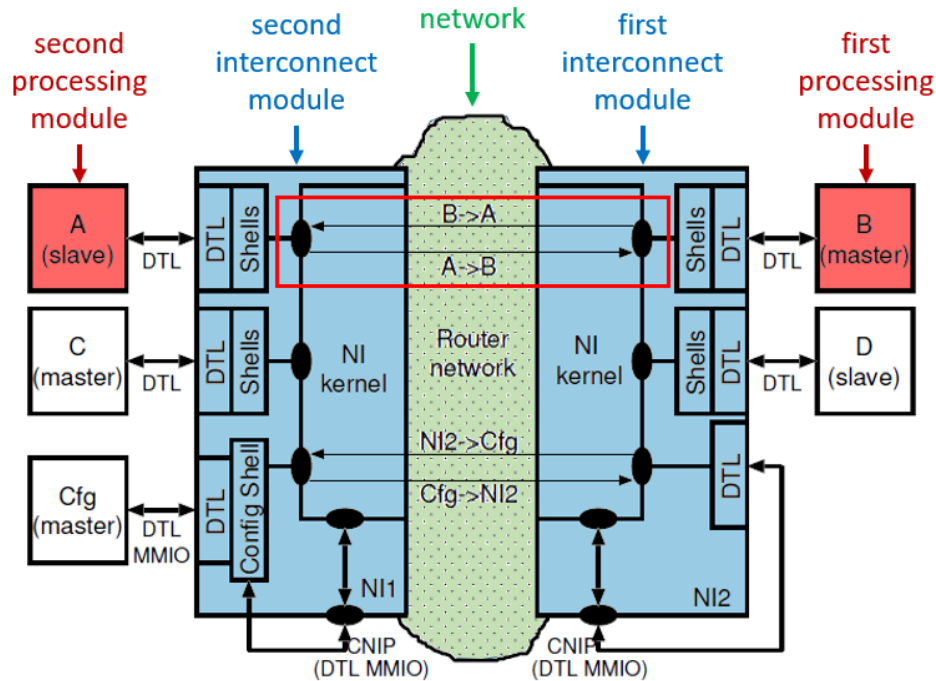


Figure 8. NI configuration

Id., fig. 8 (annotated). As shown in Rădulescu’s Figure 8, the first interconnect module NI2 is connected between the first processing module master B and the network, and the second interconnect module NI1 is connected between the second processing module slave A and the network. *Id.* This configuration matches the configuration of the alleged invention depicted in the ’800 Patent’s figures. *See* Ex-1001 at figs. 1–2; *see id.*, 5:47–50 (disclosing a network of “routers” for routing data “from one network interface NI to another”).

To the extent PO advocates a construction of “network” here as “a multi-hop interconnection between modules separated by one or more network nodes” (Ex.-1020 at 13), a POSITA would have understood that Rădulescu discloses such a network as its routers are “network nodes” and that the need for a packet to traverse

one or more of such routers from its source to its destination means it includes a “multi-hop interconnection between modules separated by one or more network nodes.” Ex-1002 ¶79; *see* Ex-1006 at [0073] (node may be router). Indeed, PO has argued in parallel district court litigation that NoCs like Rădulescu’s meet this construction. *See* Ex-1021 at 8 (“Each interconnection between routers may be called a ‘hop,’ such that the NoC is a ‘multi-hop’ interconnection between modules separated by routers, or network nodes.”).

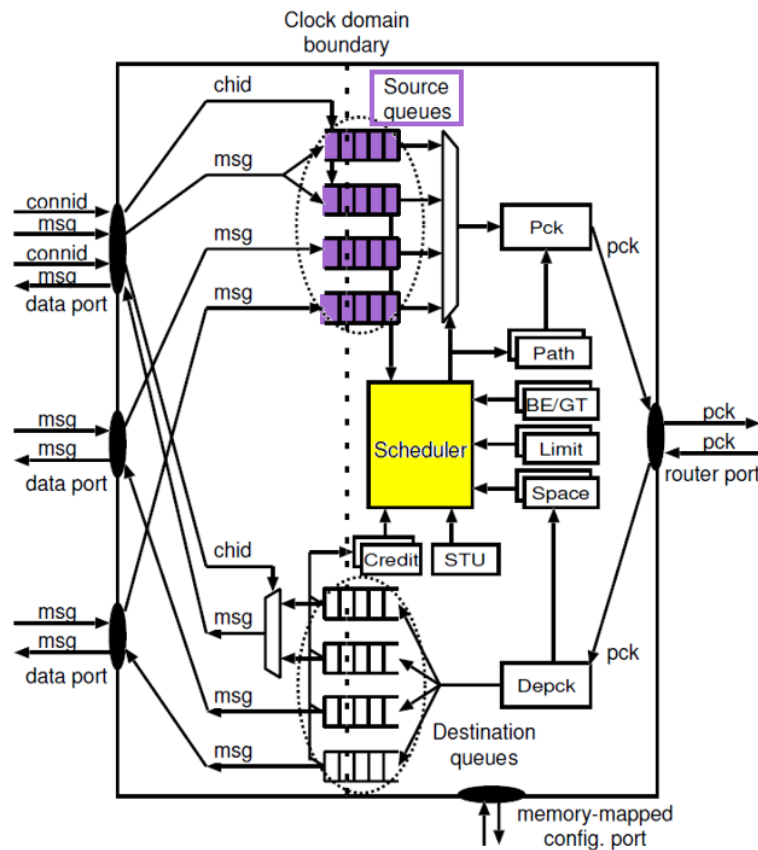
- e. **Claim 12[d]: “[i] wherein the first interconnect module includes a first memory for buffering first data from the first processing module, [ii] the first interconnect module further including a first determination unit, [iii] wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory, [iv] and the second interconnect module includes a second memory for buffering second data from the second processing module, [v] the second interconnect module further including a second determination unit, [vi] wherein the second determination unit is configured to determine a second optimal amount of data to be buffered by the second memory”**

Rădulescu in view of Bahadiroglu renders this limitation obvious. Ex-1002 ¶¶80–90.

- a. Subelements [i] and [iv]

Rădulescu discloses that each of its network interfaces NI2 and NI1 (*i.e.*, the first and second interconnect modules) include memory. *Id.* In particular, the NI kernels in each of these network interfaces comprise “message queues,” including

“source queue[s], for messages going to the NoC.” Ex-1005 at 3. Rădulescu explains that these “queues are implemented using custom-made *hardware fifos*” (*id.*, 3, 5), which a POSITA would have understood constitute memory. Ex-1002 ¶¶80–81; *see also* Ex-1005 at 5 (describing “hardware fifos” of the queues as an alternative to “RAMs,” or “random access memories”). Indeed, Rădulescu explains that “memory [is] allocated for the queues.” Ex-1005 at 1. Rădulescu illustrates the memory of each NI kernel (which is a component of each NI) in Figure 2, as annotated in purple below. *Id.*, 3.



Id., fig. 2 (annotated).

Radulescu further discloses that the source queues in the NI kernels of the interconnect modules (*i.e.*, the first and second memory) buffer data from their associated IP blocks (*i.e.*, the first and second processing modules). Ex-1002 ¶82. As Rădulescu explains, “[t]he NI kernel ... receives and provides messages, which contain the data provided by the IP modules.” Ex-1005 at 3. Rădulescu further describes that the source queues “buffer” sendable data received from the IP modules. *See id.*, at 4 (describing a flush mechanism to prevent “data being buffered indefinitely” in the source queues).

b. Subelements [ii] and [v]

Rădulescu discloses that each of its network interfaces NI2 and NI1 (*i.e.*, the first and second interconnect modules) includes a scheduler configured to determine an amount of data to be buffered. Ex-1002 ¶¶83–85. One such scheduler is depicted in Figure 2 (annotated in yellow above). Ex-1005 at Fig. 2. The scheduler in NI2 (*i.e.*, first determination unit) and the scheduler in NI1 (*i.e.*, second determination unit) are “determination units,” at least as that term has been interpreted by PO,²

² While parties in parallel district court litigation have taken the position that “determination unit” is a means-plus-function term, PO contends that this term is “[n]ot subject to § 112 ¶ 6.” Ex-1021 at 44. If the Board finds it is governed by §

because they are “circuit[s] that make[] determinations based on stored or received information.” Ex-1021 at 44. In particular, Rădulescu’s schedulers use “a configurable threshold mechanism” to determine whether the amount of sendable data in a source queue is above a stored or received threshold value. Ex-1005 at 4. Rădulescu describes that the schedulers select a channel for transmission, and “skip[] a channel as long as the sendable data is below the threshold.” *Id.*; *see also id.* (describing “a scheduler to select connections from which messages are consumed, based e.g., on their filling”); *id.* (stating “the scheduler selects a BE channel with data and remote space ... based on the queue filling”); Ex-1002 ¶84. Rădulescu further explains that “a queue becomes eligible for scheduling when ... the amount of sendable data are above a first threshold.” *Id.* Thus, the threshold indicates the amount of data to be buffered in the source queue. Ex-1002 ¶¶83–85. Moreover, a POSITA would have understood that Rădulescu’s schedulers are “circuits” at least because Rădulescu’s network interface “is intended for systems on chip (SoC)” and is operationalized “by implementing the protocol stack in hardware.” Ex-1005 at 1; *see also id.* at 2 (“In the Æthereal NoC, we optimize the performance and minimize

112(6), PO contends its structure is “circuit,” *id.*, which is disclosed by Rădulescu’s scheduler.

the cost of the protocol stack by implementing it in hardware, rather than in software.”); Ex-1002 ¶85.

c. Subelements [iii] and [vi]

Rădulescu describes that the threshold mechanism in its schedulers “optimize[s] the NoC utilization” because “it is preferable to send longer packets.” Ex-1005 at 4. A POSITA would have known one way to optimize the NoC’s utilization, consistent with Radulescu’s disclosure, was to optimize the packet size, and thus the optimal amount of data to be buffered. *See* VII.A.1; Ex-1002 ¶¶39, 86. This is consistent with the ’800 Patent, which states that “packets ... should be sufficiently large to be transferred in an optimal way with regard to the network N.” Ex-1001 at 7:15–28.

To the extent PO argues that Rădulescu does not explicitly disclose that the “threshold” used by the schedulers reflects the “optimal amount of data to be buffered,” a POSITA would have found this element obvious in view of Bahadiroglu, which discloses a determination unit configured to determine an optimal amount of data to be buffered in a network interface memory.³ Ex-1002

³ While Petitioner believes the claimed “optimal amount of data” is indefinite because the scope of what is “optimal” is subjective, PO disagrees and has represented in litigation that this term would have been understood to “equate[] to

¶¶87–90. Specifically, Bahadiroglu discloses “optimizing data packet transmission through a network connection” based on “[c]urrent network conditions in the connection.” Ex-1006 at Abstract, [0047]–[0048]. Bahadiroglu explains that its mechanism “determine[s] an *optimum packet size* ... for transmission of packet data between the sending node and the receiving node.” *Id.*; *see also, e.g., id.*, Abstract, [0048], [0051]–[0052], [0054], [0077]–[0078], [0107], [0109], [0113], [0120]–[0121], [0127]–[0128], [0133], [0152]–[0153], [0163], [0164]. Bahadiroglu further explains that the optimum packet size reflects the packet size that uses “the maximum available bandwidth of the connection most efficiently under current network latency, jitter and traffic conditions” in order to “adjust[] the transmitted packet size ... in real time to that *optimum* for the current network and connection bandwidth.” *Id.*, [0071]; *see also id.*, [0047]–[0048]. Bahadiroglu also contemplates “updating the optimum packet size” in the nodes based on current network conditions, *id.*, claim 11; *see id.*, [0052], which a POSITA would have understood

the amount of data that is optimal under certain conditions.” Ex-1020 at 34. Whatever the scope of “optimal amount of data,” it is clearly disclosed by Bahadiroglu, which expressly describes determining the “*optimum* packet size,” as discussed further below.

supports determination of both first and second optimal amounts of data as network conditions change. Ex-1002 ¶¶87–89.

A POSITA would have understood that Bahadiroglu’s “optimum packet size” is an optimal amount of data to be buffered, because the packet size determines the amount of data that must be buffered in the network interface memory before the data can be transmitted across the network. Ex-1002 ¶88. As Bahadiroglu explains, data that is passed to network interfaces for transmission is “packetize[d]” into packets “of the size designated by the Optimum Packet Size.” Ex-1006 at [0120]; *see id.*, at [0079] (“Packet Transfer Engines (PTE) 20T ... will ... communicate ‘payload’ Data Packets 16C of the optimum packet size”), [0121] (“The Packet Transfer Engine (PTE) 20TS will form the Data 22D into Data Packets 16C of the size designated by Optimum Packet Size 36S....”), [0126], fig. 6A. A POSITA would have understood that a set of data must be buffered to be sent as a packet. Ex-1002 ¶¶87–89. Indeed, the ’800 Patent equates the amount of data to be buffered with the “optimal packet size.” *See* Ex-1001 at 6:49–65, 7:14–34.

For the reasons discussed above, a POSITA would have looked to Bahadiroglu’s disclosures regarding an adaptive packet mechanism to configure Rădulescu’s threshold, and would have had a reasonable expectation of success in doing so. *See* VII.A.1; Ex-1002 ¶90. A POSITA would have been motivated to apply Bahadiroglu to both of Rădulescu’s network interfaces at least because they are

symmetrical and equally benefit from Bahadiroglu's adaptive packet mechanism.

Id. ¶¶80(n.1), 90.

- f. **Claim 12[e]: “the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches the first optimal amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches the second optimal amount”**

Rădulescu in view of Bahadiroglu renders this limitation obvious. Ex-1002 ¶¶91–93. As discussed above with respect to claim element 12[d], Rădulescu describes “optimiz[ing] the NoC utilization” by transmitting data buffered in the source queues (*i.e.*, first and second memories) of each of its network interfaces NI2 and NI1 (*i.e.*, the first and second interconnect modules) to the destination queues of the other network interface, and then to a target IP block (*i.e.*, from the first processing module to the second and from the second processing module to the first), when the amount of buffered data is above “a configurable threshold.” Ex-1005 at 4; *see id.*, fig. 8 (showing data flowing through Rădulescu's NoC from slave A to master B, and vice versa). As further discussed, Bahadiroglu discloses “determin[ing] an optimum packet size ... for transmission of packet data” between the sending and receiving nodes, and sending data packets of the “optimum packet size” over a network. Ex-1006 at [0048]; *see id.*, at Abstract, [0078], [0113], [0119]–

[0121]. Thus, the combination of Rădulescu and Bahadiroglu renders this limitation obvious. Ex-1002 ¶¶91–93.

- g. Claim 12[f]: “wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave”**

Rădulescu discloses this limitation and Rădulescu in view of Bahadiroglu renders this limitation obvious, at least as it has been interpreted by PO. Ex-1002 ¶¶94–98. Rădulescu discloses that its schedulers (*i.e.*, first and second determination units) are configured to determine the moment at which data in the source queues is transmitted based on communication properties of the communication between “B (master)” module and “A (slave)” module. Ex-1005 at 3–4; Ex-1002 ¶94. For example, Rădulescu describes that the schedulers determine the moment of transmission for data with “time guarantees (GT)” based on whether “the current slot is reserved for a GT channel”—reflecting the “throughput” property as well as (indirectly) the “latency” property—and “there is space in the channel’s destination buffer”—reflecting the “flow control” property. Ex-1005 at 3; Ex-1002 ¶94. As another example, if those prior conditions are not satisfied, Rădulescu states that its schedulers transmit data on a best effort (“BE”) channel when there is “data and remote space using some arbitration scheme: e.g., round-robin, weighted round-

robin, or based on the queue filling,” reflecting at least the flow control property. *Id.*, 3–4. These disclosures are consistent with the word “scheduler” itself, which implies that it determines the moment for sending data. Ex-1002 ¶94. Citing to similar disclosure, PO has argued that each of these transmission moments is an optimal moment ⁴ for sending data according to communication properties of the communication between the master B and the slave A. *See* Ex-1020 at 33 (citing Ex-1001 at 7:4–13); Ex-1002 ¶95.

Rădulescu further discloses that the data for which the scheduler is configured to determine an optimal moment for sending is sent from “the source queues” of NI2 and NI1 (*i.e.*, the first memory and second memory, respectively), Ex-1005 at 3; *See* VII.A.2.e, which are “said first wrapper” and “said second wrapper” under PO’s interpretation that these terms refer to the previously recited “first memory” and “second memory,” respectively. Ex-1021 at 50; Ex-1002 ¶96.

⁴ While Petitioner believes the claimed “optimal moment” is indefinite because the scope of what is “optimal” is subjective, PO disagrees and has represented in litigation that this term would have been understood “to be the ‘transmission moment’ (*i.e.*, the moment in which data [is] transmitted), where the moment is based on the recited connection properties, including at least throughput.” Ex-1020 at 33.

In addition, Rădulescu in view of Bahadiroglu renders this limitation obvious. Ex-1002 ¶¶97–98. In addition to determining an optimal packet size, Bahadiroglu describes using its adaptive packet mechanism to determine an optimal moment for sending packetized data based on network conditions or communication properties. *Id.* For example, Bahadiroglu describes that its adaptive packet mechanism “optimiz[es] data packet transmission through a connection” by using “current network conditions in the connection” to “determine ... an optimum inter-packet interval for transmission of packet data” between the sending and receiving nodes. Ex-1006 at [0047]–[0048]; *see id.*, Abstract, [0048], [0067], [0071], [0077], [0120], [0126], [0152], [0154], [0160], [0164]. Bahadiroglu further describes determining “the optimum inter-packet interval” based on “the amount and type of data to be transmitted” and “network conditions” that include latency, jitter, available bandwidth, and traffic conditions. *See id.*, [0048], [0071], [0106]–[0107], [0111]–[0114].

A POSITA would have understood that a determination of the “optimum inter-packet interval,” as described by Bahadiroglu, is a determination of the “optimal moment for sending the data.” Ex-1002 ¶97. As Bahadiroglu explains, the “inter-packet interval” is “the interval between packets that are transmitted consecutively through the connection,” or the amount of time between packet transmissions. Ex-1006, [0068], [0107]; *see id.*, [0069] (describing “inter-packet

delay of 10 msec” and “inter-packet delay of 20 ms”). Determining the optimal amount of time between packet transmissions thus determines the optimal moment for sending the data of each subsequent packet. Ex-1002 ¶97.

For the reasons discussed above, a POSITA would have found it obvious and been motivated to combine Rădulescu’s disclosure of schedulers that determine when to transmit data buffered in network interface source queues with Bahadiroglu’s disclosure of an adaptive packet mechanism that determines the optimum inter-packet interval based on various network conditions, and would had a reasonable expectation of success in doing so. *See* VII.A.1; Ex-1002 ¶98. Thus, a POSITA would have understood that this combination of Rădulescu and Bahadiroglu teaches that the determination units in either or both of Rădulescu’s NI1 and NI2 interconnect modules are configured to determine an optimal moment (*i.e.*, based on the “Optimum Inter-Packet Interval” as disclosed in Bahadiroglu) for sending the data according to communication properties of the communication between Rădulescu’s master B and its slave A. Ex-1002 ¶¶94–98.

- h. Claim 12[g]: “wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery”**

Rădulescu discloses this limitation and Rădulescu in view of Bahadiroglu renders this limitation obvious, at least as it has been interpreted by PO. Ex-1002 ¶¶99–105. Rădulescu discloses that many of the listed communication properties are used in the operation of its NoC. Ex-1005 at 1, 6. These include ordering of data transport, flow control, throughput, latency, data delivery, transmission termination, and transaction completion. For example, Rădulescu describes that “[s]upport for real-time communication is achieved by providing throughput, latency, and jitter *guarantees.*” *Id.*, 2; *see id.*, 1 (disclosing a “guarantee[.]” on the “lower bounds on throughput” and “upper bounds on latency”), 6. Regarding flow control, Rădulescu describes that “[e]nd-to-end flow control ensures that no data is sent unless there is

enough space in the destination buffer to accommodate it.” *Id.*, 3; *see also id.*, 6.⁵ Rădulescu also describes ordering of data transport. *Id.*, 2 (describing “order or unordered message delivery”), 4 (describing “[i]n-order delivery” of data), 6 (stating the NoC offers “transaction ordering”). With respect to data delivery, transmission termination, and transaction completion, Rădulescu further describes “guaranteed message delivery or not” and data transmission “with or without timing guarantees.” *Id.*, 2. As discussed above, a POSITA would have understood that Rădulescu’s schedulers consider these communication properties in determining when to transmit data buffered in the source queues of Rădulescu’s NI2 and NI1. *See* VII.A.2.g; Ex-1002 ¶¶100–101.

In addition, Bahadiroglu describes determining the “optimum inter-packet interval” (*i.e.*, optimal moment) based on many of the same “communication properties,” which Bahadiroglu calls “Network Conditions.” Ex-1006 at Abstract, [0001], [0047]–[0048], [0071]. For example, Bahadiroglu describes making this determination based on information relating to bandwidth (*i.e.*, throughput), jitter, latency, “two way delay time,” “number of packets out of sequence,” and “number

⁵ Rădulescu’s disclosure of the “flow control” property is consistent with both the definition of that property in the claims and the construction proposed by PO in parallel district court litigation. Ex-1011 at 13.

of packets lost.” *Id.*, Abstract, [0048], [0049]–[0051], [0065], [0129]–[0132]; *see also id.*, fig. 6A (listing network conditions). Bahadiroglu further describes that factors related to lossiness, data correctness, and data delivery, “such as packet error, packet loss, packet dropping, or packet retransmission [*sic*] rates[,] ... may be used to refine the results.” *Id.*, [0066]. In addition, Bahadiroglu describes considerations related to flow control. *Id.*, [0013], [0093]–[0094], [0102]–[0103]; Ex-1002 ¶102.

Rădulescu and Bahadiroglu—each independently and in combination—disclose determining the moment of transmission based on one or more of the claimed “communication properties.”⁶ Ex-1002 ¶¶103–104. To the extent PO argues that any of the claimed communication properties are not explicitly disclosed by Rădulescu or Bahadiroglu, such properties were well-known to a POSITA, and it would have been obvious to consider such properties in scheduling transmissions. *Id.* ¶¶103–105 (citing Ex-1008 at 11:17–22 (listing all of the claimed communication properties), Abstract, 9:5–7, 9:18–23, 16:32–34). Indeed, Bahadiroglu expressly recognizes “that Network Conditions 42 directly or indirectly represent a significant number of network variables,” Ex-1006 at [0153], and that Bahadiroglu’s adaptive packet mechanism may take into account “some or all of [the] Network Conditions

⁶ PO has represented in parallel litigation that the determination unit need not use all of the listed properties in making its determination. Ex-1021 at 41–44.

42.” *Id.*, [0155]. A POSITA would have been motivated to use all these network conditions in combination with Rădulescu and Bahadiroglu to further optimize data communication over Rădulescu’s NoC with a reasonable expectation of success. Ex-1002 ¶105. For example, a POSITA would have understood that doing so would maximize efforts to control bandwidth, capacity, and traffic management over Rădulescu’s NoC by accounting for the maximum number of possible factors bearing on effective communication between IP modules. *Id.* Accounting for these network conditions minimizes the potential for conflicts among traditional network efficiency indicators and traffic management levers that would otherwise degrade the transmission of data (*i.e.*, by balancing all potential factors rather than maximizing some factors at the expense of others). *Id.*

3. Claim 13⁷

Claim 12 is obvious as discussed above. *See* VII.A.2. In addition, Rădulescu discloses the limitation of claim 13 as it explains that its network interfaces—including NI2 and NI1 (*i.e.*, the interconnect modules)—manage communication over the NoC. *See, e.g.*, Ex-1005 at 2 (“Packetization is performed by the NI, and is thus transparent to the IP modules.”), 3 (“The network interface (NI) ...

⁷ Petitioner has attached an appendix containing the language for all Challenged Claims, broken down by element as referenced in this Petition.

implement[s] the connections”), 3–4 (describing a “scheduler” that offloads a communication burden from the IP modules), 5 (“NI2 can be configured to set up a channel from B to A”). Communication is thus “decoupled” from computation performed by the processing modules. *Id.*, Abstract (“Our network interface decouples computation from communication”), 1 (identifying NI as “a key ingredient” in “decoupling” computation and communication), 2; Ex-1008 at 1:25–26 (“NoCs also decouple computation from communication”); Ex-1002 ¶106. This is the same as what the ’800 Patent discloses, including using the NoC to “decouple computation from communication” such that the network interfaces taken on the communication burden while the IP modules focus on computational tasks and employing “determination units” in the network interfaces to improve network utilization by again (and among other things) taking communication burdens off the IP modules. Ex-1001 at 1:42–47, 6:7–30.

4. Claim 18

Claim 12 is obvious as discussed above. *See* VII.A.2. Additionally, Rădulescu renders obvious the limitation of claim 18. Rădulescu discloses using “a *flush* signal for each channel ... to temporarily override the threshold” for buffering data in the source queue to prevent indefinite data buffering. Ex-1005 at 4. A POSITA would have understood that this signal is a first flushing command provided by the master IP module (*i.e.*, first processing module) to flush buffered data in the master source

queue (*i.e.*, first data in the first memory) so that it is sent before the threshold is reached (*i.e.*, without waiting to reach the first amount). Ex-1002 ¶107; *see also* Ex-1005 at 2 (stating master IP modules “initiate transactions by issuing requests,” which includes “commands”); *id.* at 4 (discussing “high” “flush signal” to “bypass[]” threshold for source queue); Ex-1001 at 6:25–27 (flush signal prevents “deadlock”).

Rădulescu further discloses providing another “flush signal to force credits to be sent even when they are below their threshold” to “prevent possible starvation” by allowing source-queue data to be transferred, where the “credits are sent to the producer of data” to indicate space availability at the interconnect’s other side. Ex-1005 at 3–4. A POSITA would have understood this signal is a second flushing command used to flush buffered data in the slave source queue (*i.e.*, second data in the second memory) comprising “piggybacked” credits, which are sent before the threshold is reached (*i.e.*, without waiting to reach the second amount), and that this second flushing command is also provided by the master IP module (*i.e.*, first processing module) to indicate space availability at the second interconnect module for the data flushed by the first flushing command. Ex-1002 ¶108; Ex-1005 at 3–4.

5. Claim 19

Claim 18 is obvious. *See* VII.A.4. Rădulescu also renders obvious the limitation of claim 19 because a POSITA would have understood the master IP module facing a situation where data is not transmitting would employ multiple,

simultaneous options to address the possible causes. Ex-1002 ¶109. These simultaneous options would include (1) a flush command to the master source queue, forcing transfer of buffered data from the first memory before the threshold is reached, and (2) a flush command to slave source queue, to obtain sufficient flushed credits piggybacked in the header of the second data packets to show space availability at the interconnect's slave-side for the flushed first data. *Id.*; Ex-1005 at 3–4.

6. Claim 20

Claim 18 is obvious. *See* VII.A.4. Rădulescu also renders obvious the limitation of claim 20 because the second “flush signal ... force[s] credits to be sent even when they are below their threshold,” where the “credits are piggybacked on packets” of data to allow “a queue [to] become[] eligible for scheduling” the sending of data. Ex-1005 at 4; *see id.* at 3 (“piggyback[ing] credits” in data packet headers). Rădulescu thus discloses the second flushing command includes an indication to flush data in NI1's source queue (*i.e.*, second memory) so that “credits are sent to the producer of data” to indicate space availability at NI1 for flushed first data from the first memory. Ex-1002 ¶110. A POSITA would have further understood that, because this flushing process stems from simultaneous commands issued at the master IP module, Rădulescu teaches NI2 forwards the second flushing command to

NI1 for flushing the second data from the second memory (*i.e.*, from the slave NI1 source queue). *Id.*

7. Claim 21

Claim 12 is obvious. *See* VII.A.2. Additionally, Rădulescu renders obvious the limitation of claim 21. Rădulescu teaches its first processing module sends a flush signal to flush first data buffered in the first memory. *See* VII.A.4. Rădulescu states this flush signal is provided “for each channel” with “a bit in the message header” to cause “all the words in the queue at the time of flushing” that “have not been sent” to be flushed. Ex-1005 at 4, fig. 2. A POSITA would have understood the buffered first data from the first memory caused to be flushed constitutes all messages from a same connection that have been sent earlier because this buffered data awaiting transfer came from the master IP module. Ex-1002 ¶111.

8. Claim 10

Rădulescu in view of Bahadiroglu teaches all the limitations of claim 10 and thus would have rendered the claim obvious. Ex-1002 ¶¶112–127.

a. Claim 10[pre]

To the extent the preamble is limiting, Rădulescu discloses a method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect through interface units, wherein a first processing module communicates to a second processing module using transactions. Ex-1002 ¶113; *See* § VII.A.2.a–VII.A.2.d.

b. Claim 10[a]

See VII.A.2.b.

c. Claim 10[b]

See VII.A.2.b.

d. Claim 10[c]

See VII.A.2.c.

e. Claim 10[d]

See VII.A.2.d.

f. Claim 10[e]

See VII.A.2.c.

g. Claim 10[f]

See VII.A.2.d.

h. Claim 10[g]

See VII.A.2.e. A POSITA would have understood that source and destination queues in Rădulescu’s NI2 master interface unit collectively constitute a master wrapper. Ex-1005 at 3–4, figs. 2, 8; *see also* Ex-1001 at 5:60–65 (stating “[t]he wrapper means” buffers data); Ex-1002 ¶120.

i. Claim 10[h]

See VII.A.2.e. A POSITA would have understood that source and destination queues in Rădulescu’s NI1 slave interface unit collectively constitute a slave

wrapper. Ex-1005 at 3–4, figs. 2, 8; *see also* Ex-1001 at 5:60–65 (stating “[t]he wrapper means” buffers data); Ex-1002 ¶121.

j. Claim 10[i]

See VII.A.2.e.

k. Claim 10[j]

See VII.A.2.f.

l. Claim 10[k]

See VII.A.2.e.

m. Claim 10[l]

See VII.A.2.f.

n. Claim 10[m]

See VII.A.2.g.

o. Claim 10[n]

See VII.A.2.h.

9. Claim 1

Rădulescu in view of Bahadiroglu teaches all the limitations of claim 1 and thus would have rendered the claim obvious. Ex-1002 ¶¶128–133.

a. Claim 1[pre]

See VII.A.2.a.

b. Claim 1[a]

See VII.A.8.a–VII.A.8.c.

c. Claim 1[b]

See VII.A.8.f–VII.A.8.g, VII.A.8.i–VII.A.8.k.

d. Claim 1[c]

See VII.A.8.d–VII.A.8.e, VII.A.8.h, VII.A.8.l–VII.A.8.m.

e. Claim 1[d]

See VII.A.8.n–VII.A.8.o.

10. Claim 2

Claim 1 is obvious as discussed above. *See* VII.A.9. Additionally, Rădulescu renders obvious the limitation of claim 2. Rădulescu states that the network interface units NI1 and NI2 each include an NI kernel, which “receive[] and provide[] messages ... contain[ing] the data provided by the IP modules.” Ex-1005 at 3, figs. 2, 8. Those messages—originating at the IP modules—include “a *flush* signal for each channel (and a bit in the message header) to temporarily override the threshold” for sending buffered data from the source queues before the threshold amount of sendable data is met, as well as another “flush signal to force credits to be sent [from the other side of the interconnect] even when they are below their threshold” to show space is available for data. *Id.* at 4; *see id.* (noting “credits are piggybacked on packets” of data); Ex-1002 ¶¶134–135.

In view of the combined teachings of the proposed combination, a POSITA would have understood that the bypassed thresholds are the optimal amounts of first and second data. Ex-1002 ¶¶134–135. A POSITA would have thus understood that

the slave network interface's NI kernel is a first unbuffer-flag unit for providing a first unbuffer signal (*e.g.*, either the flush signal to send data from the first wrapper in the slave NI1 or, alternatively, the flush signal to send data piggybacking credits from the first wrapper in the slave network interface) and the master network interface's NI kernel is a second unbuffer-flag unit for providing a second unbuffer signal (*e.g.*, the flush signal to send data from the second wrapper in the master NI2). *Id.*; *see* VII.A.6. A POSITA would have further understood that, in the proposed combination, buffered data is transferred from the first wrapper and second wrapper in response to these unbuffer signals when less than the first amount or second amount of data (*i.e.*, optimal amounts that are less than the threshold values) are present in the wrappers. Ex-1002 ¶¶134–135; *see* Ex. 1005 at 4 (explaining flush signals cause thresholds to be bypassed before those thresholds are satisfied).

11. Claim 4

Claim 2 is obvious as discussed above. *See* VII.A.10. Additionally, Rădulescu renders obvious the limitation of claim 4 because its disclosure teaches the unbuffer signals are initiated by the IP modules in the symmetrical NoC. *Id.*; Ex-1002 ¶136.

12. Claim 6

Claim 2 is obvious as discussed above. *See* VII.A.10. Additionally, Rădulescu renders obvious the limitation of claim 6 because a POSITA would have understood

based on Rădulescu's disclosure that the master IP module initiates the flush signals (*i.e.*, the first and second unbuffer signals). *See* VII.A.4; Ex-1002 ¶137.

13. Claim 8

Claim 1 is obvious as discussed above. *See* VII.A.9. Additionally, Rădulescu renders obvious the limitation of claim 8. Rădulescu discloses that communication over its NoC “is performed using a transaction-based protocol, where master IP modules issue *request messages* ... that are executed by the addressed slave modules, which may respond with a *response message*,” Ex-1005 at 1; *see id.* at 2, fig. 9, which a POSITA would have understood is a message-passing communication scheme. Ex-1002 ¶138. Rădulescu discloses the request and response messages contain a message header. *See id.*; Ex-1005 at fig. 7; *id.* at 4 (referring to “message header” of flush signal from IP module); *id.* at 3 (referring to “header of the packets of the data” transmitted over NoC).

Further, a POSITA would have understood that the first and second wrappers are adapted to transfer buffered data in response to information in the message header even if the amount of buffered data is below the threshold first and second amounts because Rădulescu associates the flush signal with “a bit in the message header” that causes the threshold to be “temporarily overrid[den].” Ex-1005 at 4; Ex-1002 ¶139.

14. Claim 9

Claim 1 is obvious as discussed above. *See* VII.A.9. Additionally, Rădulescu renders obvious the limitation of claim 9. Rădulescu states that its request and response messages communicated between the master and slave IP modules “are transported by means of *packets*,” Ex-1005 at 2; *see id.* at 3 (referring to “packet-based communication of the NoC” and “packetiz[ing] messages”), 4 (referring to “number of bits in the packet header”), which a POSITA would have understood is a packet-based communication scheme. Ex-1002 ¶140. Rădulescu further discloses these data packets comprise “[a] packet header.” Ex. 1005 at 3. Moreover, Rădulescu discloses that a “flush signal ... force[s] credits to be sent even when they are below their threshold,” where the “credits are piggybacked on packets” and are limited to “the given number of bits in the packet header.” *Id.* at 4. Because those credits of the first data in the first wrapper triggered to be transferred by Rădulescu’s flush signals will indicate space at the slave-side of the interconnect and thereby allow the second data flushed from the second wrapper to be transferred across the interconnect, a POSITA would have understood that the first and second wrappers are adapted to transfer buffered data in response to information in the packet header even if the amount of buffered data is below the threshold first and second amounts. Ex-1005 at 3–4; Ex-1002 ¶140; *see* VII.A.13.

15. Claim 11

Rădulescu in view of Bahadiroglu teaches all the limitations of claim 11 and thus would have rendered the claim obvious. Ex-1002 ¶¶141–146.

a. Claim 11[pre]

To the extent the preamble is limiting, Rădulescu teaches a data processing system, as it explains that the processing modules of the SoC execute commands and perform computation. *E.g.*, Ex-1005, Abstract, 1 (“master IP modules issue request messages . . . that are executed by the addressed slave modules, which may respond with a response message”), 2 (“the communication services of the Æthereal NoC are defined to meet the following goals: (a) decouple *computation (IP modules)* from communication (NoC)...”), 3-5 (describing “video pixel processing”); Ex-1002 ¶142.

b. Claim 11[a]

See VII.A.9.b.

c. Claim 11[b]

See VII.A.9.c.

d. Claim 11[c]

See VII.A.9.d.

e. Claim 11[d]

See VII.A.9.e.

B. Ground 2: Claims 1, 2, 4, 6, 8–12, 13, and 18–21 Are Rendered Obvious by Rădulescu in view of Petersen

1. Motivation to Combine Rădulescu and Petersen

A POSITA would have been motivated to combine the teachings of Rădulescu with those of Petersen to create a NoC with improved performance and efficiency. Ex-1002 ¶¶39, 147–153.

As discussed above, Rădulescu discloses “optimiz[ing] the NoC utilization” using a “configurable threshold mechanism” to determine when the “amount of sendable data” queued in the network interface is sufficiently large. *See* VII.A.1. As further discussed, although Rădulescu does not expressly specify how its configurable threshold mechanism is implemented, a POSITA would have understood that Rădulescu’s configurable threshold could be set either with a fixed value (*e.g.*, programmed into a register) or with an adjustable value that changes at runtime based on conditions in the NoC. *Id.*

Indeed, Petersen discloses an example of a runtime-adjustable implementation for a threshold mechanism. Ex-1002 ¶150. Petersen is directed to the same goal of optimizing network utilization, and a POSITA would have been motivated to combine Rădulescu’s disclosures with Petersen’s disclosures regarding a runtime-adjustable implementation to obtain the benefits of Petersen’s known solution to network optimization. Ex-1002 ¶¶150–151. In particular, a POSITA would have looked to Petersen’s disclosure of a “dynamically programmable” threshold as a

means of setting the configurable threshold described by Rădulescu and scheduling packet transmissions. *Id.* Like Rădulescu, Petersen describes using a configurable “threshold” to determine whether there is a sufficient amount of data buffered in a network interface before transmitting that data in order to “optimize performance.” *See, e.g.,* Ex-1007 at Abstract. Petersen further describes that this threshold is dynamically programmed based on network conditions, such as “system latencies or bandwidth limitations,” to avoid “underrun” conditions and “unnecessary delays.” *Id.*, 4:40–60, 29:39–46.

A POSITA would have understood that using Petersen’s mechanism would improve the performance and efficiency of Rădulescu’s NoC by adjusting both the packet size and transmission timing based on real-time network conditions, providing the most optimal usage of the NoC. Ex-1002 ¶151. A POSITA would have recognized that doing so would enable larger packets to be sent when network conditions allow, reducing the number of packet headers that must be sent and allowing more data to travel over the NoC. *Id.* Real-time adaptation would also prevent the transmission of packets that are too large for the current network conditions, which could otherwise result in buffers overflowing and packets being dropped, necessitating wasteful retransmissions. Similarly, optimizing the packet transmission timing based on current network conditions would maximize usage of the network bandwidth and manage traffic, increasing the likelihood of successful

transmissions. Moreover, Petersen’s disclosure of the benefits of utilizing a transmit buffer system, “while maintaining the communications throughput available from the simpler FIFO based systems,” would have provided a POSITA with a further motivation to combine the teachings of Rădulescu and Petersen. *Compare* Ex-1005 at 3, 5 (disclosing use of FIFO buffers), *with* Ex-1007 at 1:47–63, 2:7–10 (balancing benefits of transmit and FIFO buffers). A POSITA would have further recognized that Petersen, like Rădulescu, strives to decouple the host from communication. *See* Ex-1007 at 1:65–67 (“[T]he prior art systems which use transmit data buffers require the host or sending system to manage the transmit data buffer.”); Ex-1002 ¶151. For those reasons, a POSITA would have been motivated to combine Rădulescu’s and Petersen’s teachings to arrive at the claimed invention. *Id.*

A POSITA would have further reasonably expected this combination to succeed. They would have understood that combining Rădulescu and Petersen merely combines prior art elements according to known methods to yield predictable results. *Id.* ¶¶152–153. Moreover, both Rădulescu and Petersen occupy the same field of optimizing data communication in a network. *Id.* As such, a POSITA would have reasonably expected that use of Petersen’s known technique for optimizing data communication in a network through its dynamically programmable threshold would improve Rădulescu’s NoC in the same way. *Id.* It would require nothing more than routine implementation details to combine Petersen’s mechanism with Rădulescu’s

NoC, and Petersen provides an extensive disclosure of such implementation details throughout its specification. *Id.* A POSITA would also have understood that Petersen's disclosure is applicable to networks on chip, including because Petersen's dynamically programmable threshold mechanism disclosure would optimize rather than exhaust the resources in Rădulescu's NoC while simultaneously maximizing bandwidth, capacity, and traffic management efficiencies through Rădulescu's NoC at minimal resource cost. *Id.*

2. Claim 12

Rădulescu in view of Petersen teaches all the limitations of claim 12, Ex-1002 ¶¶154–168, and thus would have rendered that claim obvious.

a. Claim 12[pre]

See VII.A.2.a.

b. Claim 12[a]

See VII.A.2.b.

c. Claim 12[b]

See VII.A.2.c.

d. Claim 12[c]

See VII.A.2.d.

e. Claim 12[d]

Rădulescu in view of Petersen renders this limitation obvious. Ex-1002 ¶¶159–163.

a. Subelements [i] and [iv]

As discussed in Ground 1, Rădulescu discloses this subelement.
See VII.A.2.e.

b. Subelements [ii] and [v]

As discussed in Ground 1, Rădulescu discloses this subelement.
See VII.A.2.e.

c. Subelements [iii] and [vi]

As discussed in Ground 1, Rădulescu discloses this subelement.
See VII.A.2.e. To the extent PO argues that Rădulescu does not explicitly disclose that the “threshold” used by the schedulers reflects the “optimal amount of data to be buffered,” a POSITA would have found this element obvious in view of Petersen, which discloses a determination unit configured to determine an optimal amount of data to be buffered in a network interface memory.⁸ Ex-1002 ¶¶160–163.

In particular, Petersen discloses a network interface system for transmitting data from a “transmit buffer” only after a “threshold determination indicates that a sufficient portion of the [data] frame is resident in the transmit buffer.” Ex-1007 at

⁸ Whatever the scope of “optimal amount of data,” it is clearly disclosed by Petersen, which expressly describes “*optimizing* the threshold value” used to determine the amount of data to be buffered, as discussed further below.

2:14–27, *see also id.*, 4:13–17 (“The early transmit logic 6A makes a threshold determination for a given frame being transferred from the host 1 into the adapter memory 9.... When the threshold is met, then the adapter 6 begins transmitting the frame across the network.”), Abstract, 4:40–45, 4:64–5:5, 5:56–61, 31:16–28, figs. 1–2. Petersen explains that this “threshold determination” is based on comparing “the amount of data of a frame which is downloaded by the host to the transmit buffer” to a “threshold value” housed in a “threshold store,” wherein the threshold value “may be set by the host system to *optimize* performance” *Id.*, 2:31–34, 4:40–45; *see also id.*, 4:46–47 (“The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30.”), Abstract, 2:27–31, 5:5–13, 21:14–16, 21:31–34, 23:20–27, 24:48–52, 24:59–64, 25:3–18, 29:39–57, 31:16–28, fig. 12. For example, Petersen states that “status information” supplied to the host system that “includes indications of underrun conditions” allows “the host to optimize the value” of the threshold. *Id.*, 4:56–60; *see also id.*, 29:39–57, 31:34–37, 32:48–55.

A POSITA would have understood that Petersen’s optimal “threshold value” represents an optimal amount of data to be buffered, because the threshold determines the amount of data that must be buffered in the network interface memory before the data can be transmitted across the network. Ex-1002 ¶162. As Petersen explains, “packets or frames of data” are transmitted “across a communications

network” only after “the amount of data” in the transmit buffer satisfies the “threshold value,” which constitutes the optimal amount of data. Ex-1007 at 1:17–21, 2:18–27; *see also* 4:40–45 (stating the “threshold value ... indicates an amount of data of a frame that must be resident in the frame buffer 34 before transmission of that frame may be initiated”), 4:68–5:3 (“When the threshold amount of data is resident in the buffer 34, then the transmit logic 39 is instructed to begin transmission of the frame.”), Abstract. Moreover, given Petersen’s technique of optimizing the threshold value based on current conditions in the system, *id.*, 4:56–60; *see also id.*, 29:39–57, 31:34–37, 32:48–55, a POSITA would have understood that Petersen teaches determination of both first and second optimal amounts of data as conditions change. Ex-1002 ¶162.

For the reasons discussed above, a POSITA would have looked to Petersen’s disclosures regarding a dynamically programmable threshold to configure Rădulescu’s threshold, and would have had a reasonable expectation of success in doing so. *See* VII.B.1; Ex-1002 ¶¶160–163. A POSITA would have been motivated to apply Petersen to both of Rădulescu’s network interfaces at least because they are symmetrical and would equally benefit from Petersen’s dynamically programmable threshold. *Id.*

f. Claim 12[e]

Rădulescu in view of Petersen renders this limitation obvious. Ex-1002 ¶164. As discussed above with respect to claim element 12[d], Rădulescu describes transmitting data buffered in the source queues (*i.e.*, first and second memories) of each of its network interfaces NI2 and NI1 (*i.e.*, the first and second interconnect modules) to the destination queues of the other network interface, and then to a target IP block (*i.e.*, from the first processing module to the second and from the second processing module to the first), when the amount of buffered data is above “a configurable threshold.” Ex-1005 at 4; *see also id.*, fig. 8 (showing data flows through Rădulescu’s NoC from slave A to master B, and vice versa). As further discussed, Petersen discloses transmitting data over a network when “the threshold amount of data is resident in the buffer.” *See* Ex-1007 at 2:18–34, 4:68–5:3; *see also id.*, at Abstract, 2:52–53, 4:11–17, 4:30–45, 4:56–60, 5:3–13, 21:14–16, 21:31–34, 24:59–25:18, 29:39–40, 31:16–33, figs. 1–2, 12.

g. Claim 12[f]

Rădulescu discloses this limitation, at least as it has been interpreted by PO. Ex-1002 ¶¶165–166; *see* VII.A.2.g. Petersen also describes determining an optimal threshold value, which dictates when buffered data is transmitted, based on communication properties such as “system latencies or bandwidth limitations,” to avoid “underrun” conditions and “unnecessary delays.” Ex-1007, 4:40–60, 29:39–

46. Latency and bandwidth (*i.e.*, throughput) are both among the claimed communication properties.

For the reasons discussed above, a POSITA would have looked to Petersen’s disclosures regarding dynamically programmable threshold to configure Rădulescu’s threshold, and would have had a reasonable expectation of success in doing so. *See* VII.B.1; Ex-1002 ¶¶165–166.

h. Claim 12[g]

Rădulescu in view of Petersen renders this limitation obvious. Ex-1002 ¶¶167–168. As discussed above, Rădulescu discloses that many of the listed communication properties are used in the operation of its NoC. *See* VII.A.2.h. Moreover, a POSITA would have understood that Rădulescu’s scheduler considers these communication properties in determining when to transmit data buffered in the source queues of Rădulescu’s NI1 and NI2. *Id.* Petersen likewise describes determining when to transmit data based on the listed communication properties, including latency and throughput. *See* VII.B.2.g.

Rădulescu and Petersen—each independently and in combination—disclose determining the moment of transmission based on one or more of the claimed “communication properties.” Ex-1002 ¶168. As explained in Ground 1, to the extent PO argues that any of the claimed communication properties are not explicitly disclosed by Rădulescu or Petersen, such properties were well-known to a POSITA,

and it would have been obvious to consider such properties in scheduling transmissions. *See* VII.A.2.h.

3. Claim 13

Claim 12 is obvious as discussed above. *See* VII.B.2. In addition, Rădulescu discloses the limitation of claim 13 for the reasons described in Ground 1. *See* VII.A.3; Ex-1002 ¶169.

4. Claim 18

See VII.B.2, VII.A.4; Ex-1002 ¶170.

5. Claim 19

See VII.B.4, VII.A.5; Ex-1002 ¶171.

6. Claim 20

See VII.B.4, VII.A.6; Ex-1002 ¶172.

7. Claim 21

See VII.B.2, VII.A.7; Ex-1002 ¶173.

8. Claim 10

Rădulescu in view of Petersen teaches all the limitations of claim 10, Ex-1002 ¶¶174–189, and thus would have rendered that claim obvious.

a. Claim 10[pre]

See VII.A.8.a.

b. Claim 10[a]

See VII.A.8.b.

c. Claim 10[b]

See VII.A.8.c.

d. Claim 10[c]

See VII.A.8.d.

e. Claim 10[d]

See VII.A.8.e.

f. Claim 10[e]

See VII.A.8.f.

g. Claim 10[f]

See VII.A.8.g.

h. Claim 10[g]

See§ VII.B.2.e, VII.A.8.h.

i. Claim 10[h]

See§ VII.B.2.e, VII.A.8.i.

j. Claim 10[i]

See VII.B.2.e.

k. Claim 10[j]

See VII.B.2.f.

l. Claim 10[k]

See VII.B.2.e.

m. Claim 10[l]

See VII.B.2.f.

n. Claim 10[m]

See VII.B.2.g.

o. Claim 10[n]

See VII.B.2.h.

9. Claim 1

Rădulescu in view of Petersen teaches all the limitations of claim 1 and thus would have rendered the claim obvious. Ex-1002 ¶¶190–195.

a. Claim 1[pre]

See VII.B.2.a.

b. Claim 1[a]

See VII.B.8.a–VII.B.8.c.

c. Claim 1[b]

See VII.B.8.f–VII.B.8.g, VII.B.8.i–VII.B.8.k.

d. Claim 1[c]

See VII.B.8.d–VII.B.8.e, VII.B.8.h, VII.B.8.l–VII.B.8.m.

e. Claim 1[d]

See VII.B.8.n–VII.B.8.o.

10. Claim 2

See VII.B.9, VII.A.10; Ex-1002 ¶196.

11. Claim 4

See VII.B.10, VII.A.11; Ex-1002 ¶197.

12. Claim 6

See VII.B.10, VII.A.12; Ex-1002 ¶198.

13. Claim 8

See VII.B.9, VII.A.13; Ex-1002 ¶199.

14. Claim 9

See VII.B.9, VII.A.14; Ex-1002 ¶200.

15. Claim 11

Rădulescu in view of Petersen teaches all the limitations of claim 11 and thus would have rendered the claim obvious. Ex-1002 ¶¶201–206.

a. Claim 11[pre]

See VII.A.15.a.

b. Claim 11[a]

See VII.B.9.b.

c. Claim 11[b]

See VII.B.9.c.

d. Claim 11[c]

See VII.B.9.d.

e. Claim 11[d]

See VII.B.9.e.

C. Ground 3: Claims 1, 2, 4, 6, 8–12, 13, and 18–21 Are Rendered Obvious by Rădulescu in view of Bahadiroglu and Rădulescu-WO

1. Motivation to Combine Rădulescu, Bahadiroglu, and Rădulescu-WO

A POSITA would have been motivated to combine Rădulescu and Bahadiroglu for the reasons described in Ground 1. *See* VII.A.1. In addition, a POSITA would have been motivated to combine Rădulescu and Rădulescu-WO because they have common authors—Andrei Rădulescu and Kees Goossens—and pertain to the very same network on chip technology. *Compare* Ex-1008 at Cover with Ex-1005 at 1; Ex-1002 ¶¶207–208. Like Rădulescu, Rădulescu-WO discloses an integrated circuit—embodied as an SoC comprising an NoC—which supports data communication between “processing modules,” over “connections,” which each have “a set of connection properties.” Ex-1008 at Abstract, 9:5–15, 9:18–21, 11:5–11, 11:17–22. A POSITA would have also sought out known network conditions or communication properties that may be used to optimize communications over an NoC, found Rădulescu-WO’s disclosure of such communication properties, and been further motivated to combine Rădulescu-WO with Rădulescu. Ex-1002 ¶208. While they address the same subject matter, Rădulescu-WO discloses additional implementation details pertaining to certain features of Rădulescu’s NoC and a POSITA would have been motivated to consider the two references together to have the benefit of these additional details. *Id.* Because

they pertain to the same NoC and were written by common authors, a POSITA would also have reasonably expected this combination to succeed. *Id.*

2. Claim 12

Rădulescu in view of Bahadiroglu and Rădulescu-WO teaches all the limitations of claim 12, Ex-1002 ¶¶209–220, and thus would have rendered that claim obvious.

a. Claim 12[preamble]

See VII.A.2.a.

b. Claim 12[a]

As discussed in Ground 1, Rădulescu discloses this limitation and/or renders it obvious. *See* VII.A.2.b. To the extent PO argues that processing modules having processing memory are not disclosed or rendered obvious by Rădulescu, however, such processing modules would have been obvious in view of Rădulescu-WO. Ex-1002 ¶211. Rădulescu-WO discloses “a plurality of processing modules”—also described as “intellectual property blocks IPs”—including “masters” and “slaves.” Ex-1008 at Abstract, 1:1, 2:7, 12:13–15; *see also id.* 9:10–12, 11:5–6, 11:23–24, 11:31–33, 13:1–2, 13:6, 14:28–31, 25:1–9. Two such processing modules—“initiator module I” and “target module T”—are shown in red below.

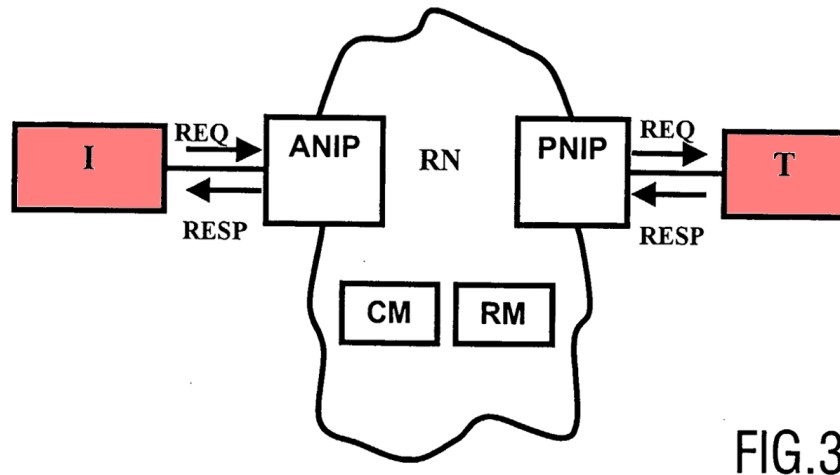


FIG.3

Id., fig. 3 (annotated); *see also id.*, Abstract, 12:5–1, figs. 1–2.

A POSITA would have understood that Rădulescu-WO’s processing modules, including the masters and slaves, are processing modules having processing memory. Ex-1002 ¶¶212–213. Rădulescu-WO states “[t]he modules ... can be so-called intellectual property blocks IPs (computation elements, memories or a subsystem which may internally contain interconnect modules).” Ex-1008 at 12:13–15; *see also id.*, 6:7–9, 22:23–23:1. This disclosure is identical to the ’800 Patent’s disclosure of processing modules: “[t]he modules ... can be so-called intellectual property blocks IPs (computation elements, memories or a subsystem which may internally contain interconnect modules).” Ex-1001 at 5:51–55, 8:48–51, 10:67–11:3; *see also* § VII.A.2.b. Additionally, Rădulescu-WO describes that the modules have within them “a memory, or a register.” Ex-1008 at 6:7–9.

c. Claim 12[b]

See VII.A.2.c.

d. Claim 12[c]

See VII.A.2.d.

e. Claim 12[d]

See VII.A.2.e.

f. Claim 12[e]

See VII.A.2.f.

g. Claim 12[f]

See VII.A.2.g.

h. Claim 12[g]

As discussed in Ground 1, Rădulescu in view of Bahadiroglu renders this limitation obvious. *See* VII.A.2.h. To the extent PO argues that the full list of claimed communication properties is not disclosed or rendered obvious by Rădulescu in view of Bahadiroglu, however, it is obvious in view of Rădulescu-WO. Ex-1002 ¶¶219–220. Rădulescu-WO discloses all the listed communication properties and their use in the operation of its NoC. Ex-1008 at Abstract, 9:5–7, 9:18–23, 11:5–22, 16:32–34. It explains that “communication between the modules are performed over connections” that are made up of “channels” having “connection properties,” which can be configured to maximize efficient use of NoC resources. *Id.*, 11:8–11; *see id.*, Abstract, 9:5–7, 9:18–23, 12:19–22, 14:9–13, 15:17–18, 16:32–34. Rădulescu-WO states:

“[t]he connection properties may include ordering (data transport in order), flow control (a remote buffer is reserved for a connection, and a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data), throughput (a lower bound on throughput is guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data), transmission termination, transaction completion, data correctness, priority, or data delivery.”

Id., 11:17–22; *see also id.*, 16:32–34. This is exactly the same list of connection properties disclosed and claimed in the ’800 Patent. *See* Ex-1001 at 5:27–35, claim 12. Rădulescu-WO describes many of these properties and their operation in detail. *See id.*, 3:9–4:22, 5:21–9:2.

As explained above in Ground 1, a POSITA would have found it obvious to consider the connection properties listed in Rădulescu-WO in determining the “optimum inter-packet interval” to further optimize data communication with a reasonable expectation of success. Ex-1002 ¶¶219–220; VII.A.2.h.

3. Claim 13

See VII.C.2, VII.A.3; Ex-1002 ¶221.

4. Claim 18

See VII.C.2, VII.A.4; Ex-1002 ¶222.

5. Claim 19

See VII.C.4, VII.A.5; Ex-1002 ¶223.

6. Claim 20

See VII.C.4, VII.A.6; Ex-1002 ¶224.

7. Claim 21

See VII.C.2, VII.A.7; Ex-1002 ¶225.

8. Claim 10

Rădulescu in view of Rădulescu-WO and Bahadiroglu teaches all the limitations of claim 10, Ex-1002 ¶¶226–241, and thus would have rendered that claim obvious.

a. Claim 10[pre]

See VII.A.8.a.

b. Claim 10[a]

See VII.A.8.b, VII.C.2.b.

c. Claim 10[b]

See VII.A.8.c, VII.C.2.b.

d. Claim 10[c]

See VII.A.8.d.

e. Claim 10[d]

See VII.A.8.e.

f. Claim 10[e]

See VII.A.8.f.

g. Claim 10[f]

See VII.A.8.g.

h. Claim 10[g]

See VII.A.8.h.

i. Claim 10[h]

See VII.A.8.i.

j. Claim 10[i]

See VII.A.8.j.

k. Claim 10[j]

See VII.A.8.k.

l. Claim 10[k]

See VII.A.8.l.

m. Claim 10[l]

See VII.A.8.m.

n. Claim 10[m]

See VII.A.8.n.

o. Claim 10[n]

See VII.A.8.o, VII.C.2.h.

9. Claim 1

Rădulescu in view of Rădulescu-WO and Bahadiroglu teaches all the limitations of claim 1 and thus would have rendered the claim obvious. Ex-1002 ¶¶242–247.

a. Claim 1[pre]

See VII.C.2.a.

b. Claim 1[a]

See VII.C.8.a–VII.C.8.c.

c. Claim 1[b]

See VII.C.8.f–VII.C.8.g, VII.C.8.i–VII.C.8.k.

d. Claim 1[c]

See VII.C.8.d–VII.C.8.e, VII.C.8.h, VII.C.8.l–VII.C.8.m.

e. Claim 1[d]

See VII.C.8.n–VII.C.8.o.

10. Claim 2

See VII.C.9, VII.A.10; Ex-1002 ¶248.

11. Claim 4

See VII.C.10, VII.A.11; Ex-1002 ¶249.

12. Claim 6

See VII.C.10, VII.A.12; Ex-1002 ¶250.

13. Claim 8

See VII.C.9, VII.A.13; Ex-1002 ¶251.

14. Claim 9

See VII.C.9, VII.A.14; Ex-1002 ¶252.

15. Claim 11

Rădulescu in view of Rădulescu-WO and Bahadiroglu teaches all the limitations of claim 11 and thus would have rendered the claim obvious. Ex-1002 ¶¶253–258.

a. Claim 11[pre]

See VII.A.15.a.

b. Claim 11[a]

See VII.C.9.b.

c. Claim 11[b]

See VII.C.9.c.

d. Claim 11[c]

See VII.C.9.d.

e. Claim 11[d]

See VII.C.9.e.

D. Ground 4: Claims 1, 2, 4, 6, 8–12, 13, and 18–21 Are Rendered Obvious by Rădulescu in view of Petersen and Rădulescu-WO

1. Motivation to Combine Rădulescu, Petersen, and Rădulescu-WO

A POSITA would have been motivated to combine Rădulescu and Petersen for the reasons described in Ground 2. *See* VII.B.1. In addition, a POSITA would have been motivated to combine Rădulescu and Rădulescu-WO for the reasons described in Ground 3. *See* VII.C.1. A POSITA would have further reasonably

expected these combinations to succeed for the same reasons discussed above. *See* Ex-1002 ¶¶259–260.

2. Claim 12

Rădulescu in view of Petersen and Rădulescu-WO teaches all the limitations of claim 12 and thus would have rendered that claim obvious. Ex-1002 ¶¶261–269.

a. Claim 12[pre]

See VII.B.2.a.

b. Claim 12[a]

See VII.B.2.b, VII.C.2.b.

c. Claim 12[b]

See VII.B.2.c.

d. Claim 12[c]

See VII.C.2.d.

e. Claim 12[d]

See VII.B.2.e.

f. Claim 12[e]

See VII.B.2.f.

g. Claim 12[f]

See VII.B.2.g.

h. Claim 12[g]

See VII.B.2.h, VII.C.2.h.

3. Claim 13

See VII.D.2, VII.A.3; Ex-1002 ¶270.

4. Claim 18

See VII.D.2, VII.A.4; Ex-1002 ¶271.

5. Claim 19

See VII.D.4, VII.A.5; Ex-1002 ¶272.

6. Claim 20

See VII.D.4, VII.A.6; Ex-1002 ¶273.

7. Claim 21

See VII.D.2, VII.A.7; Ex-1002 ¶274.

8. Claim 10

Rădulescu in view of Petersen and Rădulescu-WO teaches all the limitations of claim 10 and thus would have rendered it obvious. Ex-1002 ¶¶275–290.

a. Claim 10[pre]

See VII.B.8.a.

b. Claim 10[a]

See VII.B.8.b, VII.C.8.b.

c. Claim 10[b]

See VII.B.8.c, VII.C.8.b.

d. Claim 10[c]

See VII.B.8.d.

e. Claim 10[d]

See VII.B.8.e.

f. Claim 10[e]

See VII.B.8.f.

g. Claim 10[f]

See VII.B.8.g.

h. Claim 10[g]

See VII.B.8.h.

i. Claim 10[h]

See VII.B.8.i.

j. Claim 10[i]

See VII.B.8.j.

k. Claim 10[j]

See VII.B.8.k.

l. Claim 10[k]

See VII.B.8.l.

m. Claim 10[l]

See VII.B.8.m.

n. Claim 10[m]

See VII.B.8.n.

o. Claim 10[n]

See VII.B.8.o, VII.C.2.h.

9. Claim 1

Rădulescu in view of Petersen and Rădulescu-WO teaches all the limitations of claim 1 and thus would have rendered the claim obvious. Ex-1002 ¶¶291–296.

a. Claim 1[pre]

See VII.D.2.a.

b. Claim 1[a]

See VII.D.8.a–VII.D.8.c.

c. Claim 1[b]

See VII.D.8.f–VII.D.8.g, VII.D.8.i–VII.D.8.k.

d. Claim 1[c]

See VII.D.8.d–VII.D.8.e, VII.D.8.h, VII.D.8.l–VII.D.8.m.

e. Claim 1[d]

See VII.D.8.n–VII.D.8.o.

10. Claim 2

See VII.D.9, VII.A.10; Ex-1002 ¶297.

11. Claim 4

See VII.D.10, VII.A.11; Ex-1002 ¶298.

12. Claim 6

See VII.D.10, VII.A.12; Ex-1002 ¶299.

13. Claim 8

See VII.D.9, VII.A.13; Ex-1002 ¶300.

14. Claim 9

See VII.D.9, VII.A.14; Ex-1002 ¶301.

15. Claim 11

Rădulescu in view of Rădulescu-WO and Petersen teaches all the limitations of claim 11 and thus would have rendered the claim obvious. Ex-1002 ¶¶302–307.

a. Claim 11[pre]

See VII.A.15.a.

b. Claim 11[a]

See VII.D.9.b.

c. Claim 11[b]

See VII.D.9.c.

d. Claim 11[c]

See VII.D.9.d.

e. Claim 11[d]

See VII.D.9.e.

E. Secondary Considerations of Non-Obviousness

Petitioner is unaware of any evidence of secondary considerations that would support a finding of non-obviousness, and Petitioner does not believe PO will be able to identify any. Even if secondary considerations did exist, they cannot overcome the strong obviousness case shown in this Petition. *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1246 (Fed. Cir. 2010). Should PO attempt to meet its burden to

show secondary considerations, Petitioner reserves the right to respond to any such assertions during this proceeding. Ex-1002 ¶308.

VIII. PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION

The Board should institute review of the Challenged Claims.

A. Discretionary Denial Under 35 U.S.C. § 325(d) is Not Warranted

All six Becton Dickinson factors weigh in favor of institution. *Becton, Dickinson, & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017); *see Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020). The Board has consistently “held that a reference that ‘was neither applied against the claims nor discussed by the Examiner’ does not weigh in favor of exercising [] discretion under § 325(d).” *Fasteners for Retail, Inc. v. RTC Indus., Inc.*, IPR2019-00994, Paper 9 at 7-11 (P.T.A.B. Nov. 5, 2019). Here, all but one of the prior art references are not cited on the face of the ’800 Patent. Although Bahadiroglu was cited by the Examiner during prosecution, the arguments presented herein are not the same or substantially the same as those considered during prosecution. None of the grounds in this Petition were evaluated during prosecution. Although the Examiner allowed the claims over the combined teachings of Bahadiroglu, U.S. Patent No. 4,228,496, and U.S. Patent No. 6,668,308, the Examiner concluded “[t]he prior art found alone or in combination does not teach or suggest that the communication properties ... used to

determine the optimal moment for sending data, incorporate the claimed list of communication properties to make that determination.” Ex-1004 at 498; *see id.* at 411–32. The prior art combinations presented in this Petition, however, ***do*** disclose or teach those claimed communication properties. The Examiner improperly concluded the Challenged Claims were not obvious because the Examiner did not have the opportunity to consider the asserted prior art combinations presented herein. *Bowtech Inc. v. MCP IP, LLC*, IPR2019-00383, Paper 14 at 5 (P.T.A.B. Aug. 6, 2019).

Further, although WO2004/034173 to Rădulescu *et al.* was submitted to the Patent Office for consideration, Ex-1004 at 582, this reference was not submitted until months ***after*** the Examiner had allowed the Challenged Claims. To the extent this late submission was even considered, it was error for the Examiner not to discover that this reference (similar to the Rădulescu-WO reference in Grounds 3 and 4 of this Petition) includes the exact disclosure of claimed communication properties that the Examiner found was missing from the prior art combinations used for the claim rejection before allowance. Ex-1004 at 632 (8:20–26), 653, 498. Moreover, the applicants had no basis for the late disclosure in 2011 of their own reference bearing their names that published in 2004, more than a year before the application for the ’800 Patent was even filed.

B. Discretionary Denial Under 35 U.S.C. § 314(a) is Not Warranted

Evaluation of the factors under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential) and the clarifications made by the Director of the United States Patent and Trademark Office favors institution. *See* USPTO Memorandum, Interim Procedure for Discretionary Denials in AIA Post Grant Proceedings with Parallel District Court Litigation, 2 (June 21, 2022) (“Director’s Memo”).

To avoid overlap with parallel district court proceedings, and consistent with *Sotera Wireless*, Petitioner hereby stipulates that, “if the PTAB institutes *inter partes* review, ‘Petitioner will not pursue in [*Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00481 (E.D. Tex.) (“the Samsung district court case”)] the specific grounds [asserted in this petition], or ... any other ground ... that was raised or could have been reasonably raised in an IPR.” *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 13-14 (P.T.A.B. Dec. 1, 2020) (precedential as to § II.A).

Moreover, other relevant factors also weigh against discretionary denial under § 314(a). First, thirteen of the fourteen claims challenged herein—claims 1, 2, 4, 6, 8–11, 13, and 18–21—are not at issue in the Samsung district court case. As such, there is only limited overlap between issues raised in the petition and in the parallel proceeding. Second, it is still relatively early in the Samsung district court case. No

claim construction opinions have been issued, no depositions have been taken, and no expert reports have been submitted. Further, although the trial date in the Samsung district court case, currently scheduled for October 28, 2024, will likely pre-date the Board’s final written decision, the trial date is not set in stone and could easily change.

Additionally, as demonstrated in Section VII, the Petition presents “compelling” arguments for unpatentability of the Challenged Claims based on the same features and functionality described in the specification of the ’800 Patent. *See* Director’s Memo at 4–5 (“the PTAB will not deny institution based on *Fintiv* if there is compelling evidence of unpatentability”); *CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 3-5 (Feb. 27, 2023) (precedential) (evidence is compelling when it is “highly likely that the petitioner would prevail with respect to at least one challenged claim”). Thus, institution is consistent with the significant public interest against “leaving bad patents enforceable.” *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

IX. MANDATORY NOTICES

A. Real Party-In-Interest

Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC are the real parties-in-interest.

B. Related Matters

The '800 Patent is the subject of multiple parallel proceedings in the Eastern District of Texas and Western District of Texas, *Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00481 (E.D. Tex.); *Network System Technologies, LLC v. Texas Instruments Inc.*, No. 2:22-cv-00482 (E.D. Tex.); *Network System Technologies, LLC v. Lenovo Group Ltd.*, No. 2:23-cv-00167 (E.D. Tex.); *Network System Technologies, LLC v. Ford Motor Co.*, No. 2:23-cv-00440 (E.D. Tex.); *Network System Technologies, LLC v. Qualcomm Inc. et al.*, No. 1:22-cv-01331 (W.D. Tex.); *Network System Technologies, LLC v. OnePlus Technology (Shenzhen) Co., Ltd.* 2:23-cv-00520 (E.D. Tex.). These actions may affect, or be affected by, decisions in this proceeding. Nothing herein should be taken as an endorsement of NST's positions in the co-pending litigations.

C. Counsel Information

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D. Service Information

Samsung concurrently submits a Power of Attorney, 37 C.F.R. § 42.10(b), and consents to electronic service directed to the following email address: Samsung_NST_IPR@kirkland.com.

X. PAYMENT OF FEES

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. § 42.15(a)(1) any additional fees that may be due in connection with this Petition to Deposit Account No. 506092.

XI. CERTIFICATION

Petitioner certifies, pursuant to Rule 42.104(a), that the '800 Patent is available for IPR and Petitioner is not barred or estopped from requesting an IPR of the Challenged Claims on the grounds identified in this Petition. Petitioner certifies: (1) Petitioner is not the owner of the '800 Patent; (2) Petitioner (or any real party-in-interest) has not filed a civil action challenging the validity of any claim of the '800 Patent; (3) this Petition is being filed within one year of service of a complaint against Petitioner asserting the '800 Patent; (4) estoppel provisions of 35 U.S.C. § 315(e)(1) do not prohibit this IPR; and (5) this Petition is filed after the '800 Patent was granted.

XII. CONCLUSION

Petitioner requests institution of an IPR and cancellation of the Challenged Claims.

Dated: December 15, 2023

Respectfully submitted,

/s/ F. Christopher Mizzo

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Claims Listing Appendix

U.S. Patent No. 8,086,800

Challenged Claims 1, 2, 4, 6, 8–12, and 18–21

Reference	Claim Limitation
Independent Claim 1	
[1.pre]	An integrated circuit comprising:
[1.a]	a plurality of processing modules being connected with an interconnect and each of the plurality of processing modules having a memory, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests;
[1.b]	a first interface unit coupled to the slave and including a first wrapper for buffering data from the slave to be transferred over the interconnect to the master, the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and wherein the buffered data are transferred when said first optimal amount of data has been buffered by the first wrapper, and wherein the first interface unit including the first wrapper and the first determination unit is connected between the slave and the interconnect; and
[1.c]	a second interface unit coupled to the master and including a second wrapper for buffering data from the master to be transferred over the interconnect, the second interface unit further including a second determination unit, wherein second determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and wherein the buffered data are transferred when said second optimal amount of data has been buffered by the second wrapper, and wherein the second interface unit including the second wrapper and the second determination unit is connected between the master and the interconnect,

[1.d]	wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.
Dependent Claim 2	
[2]	The integrated circuit according to claim 1, wherein the first interface unit includes a first unbuffer-flag unit for providing a first unbuffer signal and the second interface unit includes a second unbuffer-flag unit for providing a second unbuffer signal, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to the first unbuffer signal and the second unbuffer signal, respectively, even if less than said first optimal amount and said second optimal amount of data is buffered in said first wrapper and said second wrapper.
Dependent Claim 4	
[4]	The integrated circuit according to claim 2, wherein said first unbuffer signal is initiated by the slave and said second unbuffer signal is initiated by the master.
Dependent Claim 6	
[6]	The integrated circuit according to claim 2, wherein the master is adapted to initiate said first unbuffer signal and said second unbuffer signal.

Dependent Claim 8	
[8]	The integrated circuit according to claim 1, wherein the master and the slave communicate with each other using messages of a message-passing communication scheme, wherein the messages contain a message header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said message header, respectively, even if less than said first amount and said second amount of data is buffered in said first wrapper and said second wrapper.
Dependent Claim 9	
[9]	The integrated circuit according to claim 1, wherein the master and the slave communicate with each other using packets of a packet based communication scheme, wherein the packets contain a packet header, and wherein said first wrapper and said second wrapper are adapted to transfer the buffered data in response to information in said packet header, respectively, even if less than said first amount and said second amount of data is buffered in said first and second wrapper.
Independent Claim 10	
[10.pre]	A method for buffering data in an integrated circuit having a plurality of processing modules being connected with an interconnect through interface units, wherein a first processing module communicates to a second processing module using transactions, the method comprising the acts of:
[10.a]	configuring the first processing module having a first memory as a master the provides requests;
[10.b]	configuring the second processing module having a second memory as a slave the provides responses to the requests;
[10.c]	connecting the master to a master interface unit of the interface units;

[10.d]	connecting the master interface unit to the interconnect so that the master interface unit is between the master and the interconnect;
[10.e]	connecting the slave to a slave interface unit of the interface units;
[10.f]	connecting the slave interface unit to the interconnect so that the slave interface unit is between the slave and the interconnect;
[10.g]	determining by a master determination unit of the master interface unit a first optimal amount of data to be buffered by a master wrapper of the master interface unit;
[10.h]	determining by a slave determination unit of the slave interface unit a second optimal amount of data to be buffered by a slave wrapper of the slave interface unit;
[10.i]	buffering by the slave wrapper of the slave interface unit data from the slave to be transferred over the interconnect until a first optimal amount of data is buffered;
[10.j]	transferring the buffered data from the master wrapper to the slave wrapper when said second optimal amount of data has been buffered by the master wrapper,
[10.k]	buffering by the master wrapper of the master interface unit data from the master to be transferred over the interconnect until a second optimal amount of data is buffered by the master wrapper;
[10.l]	transferring the buffered data from the master wrapper to the slave wrapper when said second optimal amount of data has been buffered by the master wrapper,
[10.m]	wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave,
[10.n]	wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced

	data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.
Independent Claim 11	
[11.pre]	A data processing system, comprising:
[11.a]	a plurality of processing modules each having a memory and being connected with an interconnect, wherein a first processing module communicates to a second processing module using transactions, wherein the first processing module is a master for providing requests and the second processing module is a slave for providing responses to the requests; and
[11.b]	a first interface unit coupled to the slave and including a first wrapper for buffering data from the slave to be transferred over the interconnect, the first interface unit further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first wrapper, and wherein the buffered data are transferred when said first optimal amount of data has been buffered by the first wrapper, and wherein the first interface unit including the first wrapper and the first determination unit is connected between the slave and the interconnect; and
[11.c]	a second interface unit coupled to the master and including a second wrapper for buffering data from the master to be transferred over the interconnect, the second interface unit further including a second determination unit, wherein second first determination unit is configured to determine a second optimal amount of data to be buffered by the second wrapper, and wherein the buffered data are transferred when said second optimal amount of data has been buffered by the second wrapper, and wherein the second interface unit including the second wrapper and the second determination unit is connected between the master and the interconnect,
[11.d]	wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal

	moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.
Independent Claim 12	
[12.pre]	An integrated circuit comprising:
[12.a]	a plurality of processing modules including a first processing module having a first processing memory and a second processing module having a second processing memory;
[12.b]	a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module; and
[12.c]	a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module, wherein the first interconnect module is connected between the first processing module and the network, and wherein the second interconnect module is connected between the second processing module and the network;
[12.d]	[i] wherein the first interconnect module includes a first memory for buffering first data from the first processing module, [ii] the first interconnect module further including a first determination unit, [iii] wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory, [iv] and the second interconnect module includes a

	second memory for buffering second data from the second processing module, [v] the second interconnect module further including a second determination unit, [vi] wherein the second determination unit is configured to determine a second optimal amount of data to be buffered by the second memory,
[12.e]	the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches the first optimal amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches the second optimal amount
[12.f]	wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave,
[12.g]	wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.
Dependent Claim 18	
[18]	The integrated circuit of claim 12, wherein the first processing module provides a first flushing command to flush the first memory and a second flushing command to flush the second memory so that the first data and the second data are sent without waiting to reach the first amount and the second amount.
Dependent Claim 19	
[19]	The integrated circuit of claim 18, wherein the first processing module provides the first flushing command and the second

	flushing command at least one of independently and simultaneously.
Dependent Claim 20	
[20]	The integrated circuit of claim 18, wherein the second flushing command includes an indication to flush the second memory so that the first interconnect module forwards the second flushing command to the second interconnect module for flushing the second data from the second memory.
Dependent Claim 21	
[21]	The integrated circuit of claim 12, wherein the first processing module includes flush information in a header of a message to cause all messages from a same connection that have been sent earlier to be flushed from at least one of the first memory and the second memory.

CERTIFICATE OF COMPLIANCE

This Petition complies with the type-volume limitations as mandated in 37 C.F.R. § 42.24, totaling 13,985 words. Counsel has relied upon the word count feature providing by Microsoft Word.

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CERTIFICATE OF SERVICE

I hereby certify that, on December 18, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,086,800 and supporting exhibits and appendix to be served via express mail on the Patent Owner at the following correspondence address of record as listed on the USPTO Patent Center:

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A courtesy copy was also served by electronic mail on the Patent Owner's designated lead counsel for service for the related matter: *Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00481 (E.D. Tex.).

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