IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETWORK SYSTEM TECHNOLOGIES, LLC,

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG AUSTIN SEMICONDUCTOR, LLC, SAMSUNG SEMICONDUCTOR, INC.,

Defendants.

Civil Action No. 2:22-CV-00481-JRG

JURY TRIAL DEMANDED

PLAINTIFF NETWORK SYSTEM TECHNOLOGIES, LLC'S
OPENING CLAIM CONSTRUCTION BRIEF

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2	U.S. Patent No. 7,373,449
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I. Introduction

Pursuant to P.R. 4-5 and this Court's Docket Control Order (Dkt. 59), Plaintiff Network System Technologies, LLC ("NST") hereby submits its opening claim construction brief regarding U.S. Patent Nos. 7,366,818 ("'818 Patent"), 7,373,449 ("'449 Patent"), 7,594,052 ("'052 Patent"), 7,769,893 ("'9893 Patent"), 8,072,893 ("'2893 Patent"), and 8,086,800 ("'800 Patent") (collectively, "Asserted Patents" attached hereto as Exhibits 1-6). The Parties have requested that the Court construe eleven claim terms, each of which are addressed below.

II. Technical Background

A. Background on Network-on-Chip Technology

System-on-chip ("SoC") technology is widely used in consumer electronics and computing devices, including smartphones, laptops, and embedded systems such as vehicle infotainment and advanced driver assistance systems. Dkt. 1 ¶ 144. As the adoption of SoCs in electronic devices grew over time, and as microchip manufacturing technology advanced, more processing cores and other circuitry modules were incorporated into SoCs. *Id.* ¶ 145. In early SoC designs, these circuitry modules were directly connected, first by point-to-point interconnects, and later by shared buses, both of which resulted in large SoCs with poor interconnect efficiency. *Id.*; *see also* Declaration of Dr. Erik Chmelar ("Chmelar Decl." attached hereto as Exhibit 7), ¶¶ 29-31. Though more efficient than point-to-point interconnects, buses suffered from a critical limitation insofar as only one module can send data to the bus at a time and the others must wait their turn. '818 Patent at 1:33-34. Thus, as the number of circuitry modules increased, buses became a bottleneck limiting the number of circuitry modules that could be practicably interconnected—and therefore, limited the potential power and capability of SoCs. Chmelar Decl. ¶ 31.

To eliminate this bottleneck, the inventors of the Asserted Patents at Philips Semiconductor developed advanced network-on-chip ("NoC") technologies. An NoC is a substantially different

interconnection paradigm for on-chip communication that leverages certain aspects of traditional computer networks, such as network interfaces for connecting modules to an on-chip network, packetized data for breaking messages up into smaller units for transmission by the on-chip network, and routers for switching of data packets along various routes. Chmelar Decl. ¶ 32. In an NoC, a message transmitted from one module to another may be divided into smaller packets by a network interface and those packets may travel across the NoC using different routes determined by the routers in the NoC. *Id.* ¶¶ 32-34, 39. Each interconnection between routers may be called a "hop," such that the NoC is a "multi-hop" interconnection between modules separated by routers, or network nodes. *Id.* ¶¶ 32. Accordingly, an NoC is an "indirect" interconnection between modules. *Id.* ¶¶ 139, 147. This is distinctly different from a shared bus, where data transmitted from one module to another always takes the same route, and is therefore a "direct" interconnection between modules. *Id.* ¶¶ 29, 32.

Besides overcoming the bottleneck of shared buses, NoCs have other advantages over prior direct interconnections. Because NoCs can utilize interconnects more efficiently than shared buses, fewer interconnects are required. *Id.* ¶¶ 32-36. This reduces the area and power consumption of the on-chip interconnects of an SoC compared to shared buses. *Id.* ¶¶ 31, 101, 123. Additionally, by moving the communications logic of a circuitry module to a dedicated network interface that connects the module to the NoC, the modules can be simpler and more modular, which enables even higher levels of integration at lower design costs. *Id.*

Although NoCs leverage certain aspects of traditional computer networks, the on-chip environment of NoCs introduces several constraints and challenges not present in the off-chip environment. '818 Patent at 1:62-2:6. For example, there is substantially less memory and computational resources in the on-chip environment that can be dedicated to network processing.

Id. at 2:44-50, 3:7-22, 3:31-35. The Asserted Patents address these challenges.

B. Overview of the Asserted Patents

The Asserted Patents generally relate to integrated circuits having a plurality of circuitry modules that are communicatively interconnected via NoCs. The Asserted Patents disclose systems for Quality of Service ("QoS"), called "connection properties" in the Patents, which are mechanisms to prioritize and manage communication between different circuitry modules. Chmelar Decl. ¶¶ 38-39. QoS allows for the allocation of network resources according to the specific requirements of different applications or tasks, ensuring, for example, that critical communications get higher priority while lower-priority communications do not unnecessarily consume resources. *Id.* Examples of QoS include minimum throughput or bandwidth, maximum latency, and priority. *Id.* The '449 and '052 Patents relate to various aspects of QoS.

The '449 Patent discloses a NoC that interconnects modules by communication channels, with each channel having QoS properties, such as bandwidth and latency guarantees, that can be configured independently. '449 Patent at Abstract, 7:15-30, 11:20-22, 16:1-5. For example, a request channel can guarantee a bandwidth of 1 mega-bit-per-second, and a return channel a bandwidth of 25 mega-bits-per-second. *Id.* at 9:51-59. Such independently configurable QoS guarantees enable more efficient utilization of the resources of the NoC because the guarantees on each channel can be efficiently adapted to their actual requirements. *Id.* at Abstract, 7:26-31.

The '052 Patent discloses NoC network interfaces configured to map communications to communication channels based on a desired QoS requested for the communication. '052 Patent at Abstract, 1:6-10, 3:6-34, 3:45-51, 4:7-18, 8:7-9, 8:63-65. This mapping ensures that high-priority communications requiring certain QoS guarantees are appropriately mapped within the network, resulting in the most efficient use of network resources. *Id.* at 7:63-67. Moreover, performing such mapping within the network interfaces, as opposed to within the modules, frees the modules to

focus on their dedicated operations. *Id.* at 3:30-34, 5:16-21.

The Asserted Patents disclose NoC network interfaces that manage certain inter-module communication tasks, such as packetizing data at the sending module and the depacketizing data at the receiving module, translating between different communication protocols used by the modules, and dropping data in certain cases. The '9893 and '818 Patents concern aspects of network interfaces. First, the '9893 Patent discloses a NoC network interface configured to translate between different address formats used by the modules. '9893 Patent at Abstract, 3:43-63. This address translation allows various types of modules to be integrated regardless of the communication protocols used by the modules. *Id.* at 1:45-48. This can simplify modules and reduce SoC design time and costs. *Id.* at 1:42-48. Second, the '818 Patent discloses NoC network interfaces configured to drop data in certain cases. '818 Patent at 5:35-36. One example where data may be dropped is when the buffer at the receiving module is full and thus no more data may be received at that module. *Id.* at 4:40-55.

Finally, multiple of the Asserted Patents disclose NoC buffers to increase network efficiency and resolve synchronization issues between fast and slow communication channels. The '2893 and '800 Patents concern aspects of data storage and buffering. First, the '2893 Patent discloses how to synchronize slow communication channels with faster channels. '2893 Patent at 1:34-2:33. Instead of simply slowing down the faster channels, data storage elements are added to the slow channels to delay their communications by an amount that causes each data package transmitted on the slow channels to be received in a next data-package cycle instead of the current data-package cycle. *Id.* at 1:65-2:14, 2:26-33, 2:47-3:17, 3:49-53. Second, the '800 Patent discloses a NoC network interface that has buffers to store data until an optimal amount of data is available for transmission on the network. '800 Patent at 4:18-28, 4:50-57. Rather than

inefficiently transmitting data in small packages as it is generated by the circuitry modules, the buffers aggregate data until an optimal amount of data is ready to be transmitted over the network, increasing overall network utilization and efficiency. *Id.* at 3:1-3, 7:44-46.

III. Legal Standard

A. Plain and Ordinary Meaning

The "words of a claim" are understood according to their plain and ordinary meaning in the context of the surrounding claim limitations, the specification, and the prosecution history. *Thorner v. Sony Computer Entertainment America LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

The "words of a claim" are not given their plain meaning only when the patentee "acts as his own lexicographer" or "disavows the full scope of a claim term either in the specification or during prosecution." *Thorner*, 669 F.3d at 1365. As the Federal Circuit cautions, "we must look at the ordinary meaning in the context of the written description and the prosecution history," since importing limitations is one of the "cardinal sins of patent law." *Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1320 (Fed. Cir. 2005). Accordingly, a "claim construction that does not encompass a disclosed embodiment is rarely, if ever, correct." *Medrad*, 401 F.3d at 1320.

The standard for lexicography is exacting. *Thorner*, 669 F.3d at 1365-67. "To act as its own lexicographer, a patentee must clearly set forth a definition of the disputed claim term other than its plain and ordinary meaning," and occurs only when the patentee explicitly discloses that a term "means" a particular definition or "is defined." *Id*. The "standard for disavowal of claim scope is similarly exacting." *Id*. The intrinsic evidence must provide "expressions of manifest exclusion or restriction," clarifying that the invention does not include a particular feature. *Id*. "Where the alleged disavowal is ambiguous," courts do not apply the doctrine of prosecution

history disclaimer. *Avid Tech., Inc. v. Harmonic, Inc.*, 812 F.3d 1040, 1045 (Fed. Cir. 2016).

B. Means-Plus-Function

"In determining whether a claim term invokes § 112, ¶ 6, the essential inquiry is not merely the presence or absence of the word 'means' but whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Skky, Inc. v. MindGeek s.a.r.l.*, 859 F.3d 1014, 1019 (Fed. Cir 2017) (internal quotations and citations omitted). When a claim term lacks the words "means," there is a presumption that § 112, ¶ 6 does not apply. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015). While the word "means" triggers a presumption that § 112, ¶ 6 applies, this can be rebutted by a preponderance of the evidence when "consider[ing] the limitations as a whole" according to the "understanding of one of ordinary skill in the art." *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1374 (Fed. Cir. 2003) (internal quotations, citations, and modifications omitted). "[W]hen a claim uses the term 'means,' the focus is on whether the claim term recites no function corresponding to the means or recites sufficient structure or material for performing that function." *Id*. at 1372 (internal quotations omitted). To further "hold that a claim containing a means-plus-function limitation lacks a disclosure of structure" "requires [an additional] finding, by clear and convincing evidence, that the specification lacks disclosure of structure sufficient to be understood by one skilled in the art as being adequate to perform the recited function." *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1376-77 (Fed. Cir. 2001).

C. Definiteness

Definiteness is evaluated from the perspective of someone "skilled in the relevant art." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 909 (2014). "[T]he certainty which the law requires in patents is not greater than is reasonable, having regard to their subject-matter." *Id*. at 910 (quoting *Minerals Separation, Ltd. v. Hyde*, 242 U.S. 261, 270 (1916)). Terms of degree

are not "inherently indefinite," and "absolute or mathematical precision is not required." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 (Fed. Cir. 2014). Indefiniteness requires an accused infringer to show "by clear and convincing evidence that a skilled artisan could not discern the boundaries of the claim based on the claim language, the specification, and the prosecution history, as well as her knowledge of the relevant art area." *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1249-50 (Fed. Cir. 2008); 35 U.S.C. § 282.

IV. Level of Ordinary Skill in the Art

NST's expert, Dr. Chmelar, opines that a person of ordinary skill in the art ("POSITA") at the time of the invention of the Asserted Patents is an individual having at least: a Bachelor of Science (or equivalent) degree in electrical engineering, computer engineering, or a related field, and 2-3 years of work experience in very large-scale integrated ("VLSI") systems, such as application-specific integrated circuits ("ASICs"), application-specific standard parts ("ASSPs"), system-on-chip ("SoC"), or field-programmable gate arrays ("FPGAs"), and has an understanding of on-chip interconnection networks. Chmelar Decl. ¶ 26.

Defendants' expert, Dr. Madisetti, posits a similar skill level: at least a Bachelor's degree in computer science, electrical engineering, computer engineering, or an equivalent technical degree, and two or more years of experience with system-on-chip, interconnect, or networking technologies. Neither expert has opined whether this discrepancy would have an impact on their conclusions as to the constructions of the various terms.

V. Claim Construction Order in *Network System Technologies v. Texas Instruments*

On January 3, 2024, Judge Schroeder issued a Claim Construction Order that addresses several of the terms the parties propose for construction here. *Network System Technologies, LLC v. Texas Instruments, Inc.*, No. 2:22-CV-00482-RWS, Dkt. 150 (E.D. Tex. Jan. 3, 2024), the "TI Order," attached hereto as Ex. 8. NST agrees with the TI Order in many respects, and respectfully

disagrees with others. NST will note its agreement or disagreement as applicable herein.

VI. Disputed Terms

A. "Interconnect Means"

Term	NST's Construction	Defendants' Construction
"interconnect means" '052 Patent: claim 6	"multi-hop interconnection between modules separated by one or more network nodes."	Plain and ordinary meaning. Not subject to § 112, ¶ 6.

Intrinsic evidence shows that a POSITA would have understood the term "interconnect means" to describe a "multi-hop interconnection between modules separated by one or more network nodes" as a "network" (*i.e.*, an *indirect* interconnection) rather than a shared bus (*i.e.*, a *direct* interconnection). *See* Chmelar Decl. ¶¶ 133-35.

The TI Order adopts the same construction as NST proposes here: **"multi-hop interconnection between modules separated by one or more network nodes."** Ex. 8 at 51 (emphasis original). NST agrees with the TI Order's construction and adopts the Order's rationale for reaching such construction. *See id.* at 47-51. As the TI Order found, and as NST's expert observes, the term "network" and "interconnect means" are used interchangeably in the related patents. *Id.* at 48-49; Chmelar Decl. ¶¶ 140-45 (citing '052 Patent at Abstract, Fig. 1, Fig. 4, 1:7-8, 3:18-22, 3:51-54, 4:1-4, 5:24-31).

Here, the parties have stipulated that "network" means "multi-hop interconnection between modules separated by one or more network nodes." *See* Dkt. 91, Appendix 1. Thus, following the TI Order, and Dr. Chmelar's, logic, the term "interconnect means" should likewise be construed as "multi-hop interconnection between modules separated by one or more network nodes."

The TI Order expressly rejected the same "plain and ordinary meaning" construction that Defendants advocate here as inconsistent with the intrinsic record. Ex. 8 at 51. Additionally, insofar as there is a dispute between the parties as to whether "interconnect means" should

encompass additional concepts like bus architectures and off-chip communications, a plain and ordinary meaning construction is inappropriate. *O2 Micro, Ltd.,* 521 F. 3d at 1361 (Fed. Cir. 2008).

B. "Dropping Means"

Term	NST's Construction	Defendants' Construction
"dropping means (DM) for dropping data exchanged by said first and second module (M, S)" '818 Patent: claims 1, 3, 5	**Not subject to § 112, ¶ 6:** "dropping means": "circuit configured to drop data." The remaining language should be afforded its plain and ordinary meaning. **If the Court holds § 112, ¶ 6 applies:** **Function**: *Claim 1*: "drop data exchanged by said first and second module"; *Claim 3*: function according to claim 1 and "create an error message if data is dropped"; *Claim 5*: function according to claim 3 and "send said error message to said first module" **Structure**: "circuit"	Subject to § 112, ¶ 6. **Function**: *Claim 1*: "dropping data exchanged by first and second module (M, S)"; *Claim 3*: "create an error message if data is dropped"; *Claim 5*: "send said error message to said first module" **Structure**: portion of the circuit configured to implement the scheme disclosed in the '818 Patent at 7:45–56, 8:38–40, 8:64–9:10. Otherwise, indefinite.

NST's construction of "dropping means"[1] as a "circuit configured to drop data" reflects a POSITA's understanding of the term as recited in the Asserted Patents. Chmelar Decl. ¶¶ 52-62.

Defendants' position that "dropping means" is part of a larger phrase that should be construed as a means plus function term under 35 U.S.C. § 112, ¶ 6 is incorrect, and is undermined by Defendants' inconsistent treatment of "interconnect means," which though contains the word "means" was not proposed by Defendants to be governed by § 112, ¶ 6. *See* § VI.A., *supra*.

Notably, by including the language "portion of the circuit," Defendants' proposed

[1] The '818 Patent uses the terms "dropping means" and "dropping manager" interchangeably. '818 Patent at 7:48-50.

construction not only acknowledges that the '818 Patent discloses a "circuit," but also concedes that a "circuit" is sufficiently structural.[2] Thus, in light of: 1) Defendants' inconsistent treatment of "means" terms; 2) Defendants' concession that a "circuit" is structural, and 3) the vast body of Federal Circuit precedent holding that a "circuit" is sufficiently structural, the § 112, ¶ 6 presumption is rebutted and NST's construction (the *only* non-§ 112, ¶ 6 construction before the Court) should be adopted. *See Skky*, 859 F.3d at 1020 (finding "'wireless device means' does not invoke § 112, ¶ 6 because its clause recites sufficient structure"); *see also Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 711 F.3d 1348, 1364 (Fed. Cir. 2013) ("We have previously held on several occasions that the term 'circuit' connotes structure."); *MIT v. Abacus Software,* 462 F.3d 1344, 1355 (Fed. Cir. 2006) ("[T]he term 'circuit,' combined with a description of the function of the circuit, connoted sufficient structure to one of ordinary skill in the art to avoid 112 P6 treatment."); *Linear Tech. Corp. v. Impala Linear Corp.,* 379 F.3d 1311, 1320-21 (Fed. Cir. 2004) (holding that the term "circuit" is not a means-plus-function limitation when the patent provides "a recitation of the respective circuit's operation in sufficient detail to suggest structure to persons of ordinary skill in the art"); *Apex Inc. v. Raritan Computer, Inc.,* 325 F.3d 1364, 1373 (Fed. Cir. 2003) ("[T]he term 'circuit' with an appropriate identifier such as 'interface,' 'programming' and 'logic,' certainly identifies some structural meaning to one of ordinary skill in the art.").

[2] The conclusion that the "dropping means" is a structural "circuit" is inescapable. The '818 Patent discloses "[s]aid **integrated circuit comprises** at least **one dropping means.**" Chmelar Decl. ¶ 53 (citing '818 Patent at Abstract (emphasis added)); *see also* '818 Patent at 5:27-28, 5:37-41 ("integrated circuit comprising at least one interface means" that "comprises a first dropping means."). The parties stipulated that an "integrated circuit" means "interconnected circuitry on a chip" which is consistent with a POSITA's understanding of the term. Dkt. 91, Appendix 1; Chmelar Decl. ¶ 53. Since the '818 Patent discloses a "dropping means" comprised in an "integrated circuit," then it logically follows that the "dropping means" must be a circuit element of the "integrated circuit" and is therefore likewise structural. *Id.*

If, however, the Court determines that § 112, ¶ 6 applies, the parties do not materially differ on the applicable functions. The dispute is therefore centered on whether the structure is a "circuit" (NST's position) or whether the structure is a "portion of the circuit configured to implement the scheme disclosed in the '818 Patent at 7:45–56, 8:38–40, 8:64–9:10" (Defendants' position).

Defendants' construction is the same as the TI Order's construction, which NST respectfully submits is incorrect. Though Defendants' definition of the structure correctly references the structural "circuit" (consistent with NST's construction), it additionally includes a requirement that such circuit "implement the scheme disclosed in the '818 Patent at 7:45–56, 8:38–40, 8:64–9:10," thereby inserting additional *functional* limitations contained in these specification passages (e.g., describing "possible" scenarios where data "may" or "can" be dropped). However, § 112, ¶ 6 "does not permit limitation of a means-plus-function claim by adopting a function different from that explicitly recited in the claim" and a construction—such as Defendants'—that "incorporate[es] unrecited functional limitations into the claims" is erroneous. *Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999).

Therefore, if § 112, ¶ 6 applies, the correct structure is one that does not incorporate additional functional limits, such as NST's proposal: "circuit." Or, partially adopting the TI Order's construction, a permissible construction is "portion of the circuit configured to drop data."

C. "Interface Means"

Term	NST's Construction	Defendants' Construction
"interface means" / "interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN)	**Not subject to § 112, ¶ 6:** "interface means": "interface circuit that connects a module to a network" "interface means (ANIP, PNIP) for managing the interface…": NST incorporates its definitions for the terms	Subject to § 112, ¶ 6. **Function**: *Claim 1*: "managing the interface between a module (M, S) and a network (N, RN) and controlling dropping of data and transaction completion";

Term	NST's Construction	Defendants' Construction
wherein said interface means (ANIP, PNIP) comprises a first dropping means (DM) for dropping data, and wherein the dropping of data and therefore the transaction completion can be controlled by the interfaces means" '818 Patent: claims 1, 6, 7	"interface means" and "dropping means," and the agreed upon definition for the term "network." The remaining language should be afforded its plain and ordinary meaning. **If the Court holds § 112, ¶ 6 applies:** **Function**: *Claim 1*: "manage the interface between a module and the network, and control the dropping of data and therefore the transaction completion"; *Claim 6*: the function according to claim 1 and "store received error messages"; *Claim 7*: the function according to claim 1 and "not drop error messages" **Structure**: "circuit"	*Claim 6*: "store received error messages"; *Claim 7*: "not drop error messages" **Structure**: portion of the circuit configured to implement the scheme disclosed in the '818 patent at 7:57-8:63, 9:10-49 and the structure of the claimed dropping means. Otherwise, indefinite.

NST's construction of "interface means" as an "interface circuit that connects a module to a network" reflects what a POSITA would have understood this term to mean as used by the '818 Patent. Chmelar Decl. ¶¶ 71-74.

Identically to Defendants' construction of "dropping means," addressed above, their construction of "interface means" includes the language "portion of the circuit," thereby acknowledging that the "circuit" of the '818 Patent is sufficiently structural.[3] Thus, as with "dropping means," and in light of: 1) Defendants' inconsistent treatment of "means" terms; 2)

[3] As with "dropping means," the '818 Patent discloses the "interface means" comprised in an "integrated circuit" and the parties stipulated that an "integrated circuit" means "interconnected circuitry on a chip." It therefore logically follows that the "interface means" must be a circuit element of the "integrated circuit." That an "interface means ANIP, PNIP is **adapted to store** received error messages" supports NST's construction because **storage** cannot be achieved without **storage circuitry** (*e.g.,* latches, flip-flops, registers, memory cells, etc.). *Id.* (citing '818 Patent at 5:64-66) (emphases added). Additionally, the '818 Patent discloses that the "interface means" connects "modules and the router network." *Id.* ¶ 73 (quoting '818 Patent at 7:23-27); *see also id.* at Fig. 2, 7:27-31.

Defendants' concession that "circuit" is structural, and 3) the Federal Circuit precedent cited above holding that a "circuit" is sufficiently structural, the § 112, ¶ 6 presumption is rebutted and NST's construction (again, the *only* non-§ 112, ¶ 6 construction before the Court) should be adopted. *See Skky*, 859 F.3d at 1020 (finding "'wireless device means' does not invoke § 112, ¶ 6 because its clause recites sufficient structure").

If § 112, ¶ 6 applies, the parties do not materially differ on the applicable functions and the crux of the dispute is whether the structure is a "circuit" (NST's position) or whether the structure is a "portion of the circuit configured to implement the scheme disclosed in the '818 patent at 7:57-8:63, 9:10-49 and the structure of the claimed dropping means" (Defendants' position).

Defendants' construction is similar to the TI Order's construction (which, like "dropping means," NST respectfully submits is incorrect), but appends the additional language "and the structure of the claimed dropping means." As with "dropping means," though Defendants' definition of the structure correctly references the structural "circuit" (consistent with NST's construction), by additionally inserting a requirement that such circuit "implement the scheme disclosed in the '818 patent at 7:57-8:63, 9:10-49," the construction incorrectly and impermissibly inserts additional *functional* limitations embodied in these specification passages (e.g., describing "examples" of commands and "optional" messages sent by the network interfaces). Such a construction is erroneous. *Micro Chem.*, 194 F.3d at 1258.

Therefore, as with "dropping means," if § 112, ¶ 6 applies, the correct structure is one that does not incorporate additional functional limits, such as NST's proposal: "circuit." Or, partially adopting the TI Order's construction, a permissible construction is "portion of the circuit configured to connect modules to the network."

D. "Communication Manager"

Term	NST's Construction	Defendants' Construction
"communication manager [(CM) for managing the communication between different modules" '449 Patent: claims 2, 6, 10	**Not subject to § 112, ¶ 6:** "communication manager": "circuit that manages communication between modules." The remaining language should be afforded its plain and ordinary meaning. **If the Court holds § 112, ¶ 6 applies:** **Function**: "forward a request for a connection to a resource manager" **Structure**: "circuit"	Subject to § 112, ¶ 6 **Function**: forwarding a request to a resource manager. **Structure**: portion of the circuit configured to implement the scheme disclosed in the '449 Patent at 10:19-24, 10:41-54. Otherwise, indefinite.

NST's construction of a "communication manager" as a "circuit that manages communication between modules" reflects what a POSITA would have understood this term to mean as used in the Asserted Patents. First, intrinsic evidence supports this construction, since the '449 Patent discloses that the "communication manager" is comprised in "a system on chip," which is an "integrated circuit." *See* Chmelar Decl. ¶¶ 100, 102-04 (citing '449 Patent at 9:66-10:3). Indeed, the '449 Patent expressly discloses that "**said integrated circuit comprises** at least one **communication managing means**."[4] *Id*. ¶ 103 (citing '449 Patent at 7:35-38 (emphases added)).

The parties' stipulation as to the meaning of "integrated circuit" also supports NST's proposed construction by defining an "integrated circuit" as "interconnected circuitry on a chip." Dkt. 91, Appendix 1; Chmelar Decl. ¶¶ 100, 104 (*citing* Exs. I and G thereto). In other words, since the '449 Patent discloses a "communication manager" comprised in an integrated circuit, it

[4] The '449 Patent uses the terms "communication manager" and "communication managing means" interchangeably. Chmelar Decl. ¶ 159.

logically follows that the "communication manager" must be "circuitry" of said "integrated circuit." This is further supported by the '449 Patent's disclosure of the "communication manager" as being arranged in a "network," a "router network," or a "network interface means," which are themselves undisputedly structural elements comprised in the "integrated circuit." Chmelar Decl. ¶ 105 (citing '449 Patent at 9:66-10:6; Abstract, 1:7-11, 7:15-18, 8:7-11, 9:17-21).

Defendants' position that "communication manager" is part of a larger phrase that must be construed under 35 U.S.C. § 112, ¶ 6 fails for several reasons. First, Defendants cannot rebut the presumption that § 112, ¶ 6 does not apply because a POSITA having reviewed the intrinsic evidence would understand "communication manager" as having a "sufficiently definite meaning as the name for structure." *Williamson*, 792 F.3d at 1349. The "communication manager" is consistently described throughout the claims and specification as a constituent of an "integrated circuit," which the parties agree means "interconnected circuitry on a chip." *See* '449 Patent at Claim 10; *see also* Chmelar Decl. ¶¶ 100, 104. An "integrated circuit" is physical hardware, and so too are the constituent circuitry elements that make up the integrated circuit, including the "communication manager." *Id.* ¶ 108.

Second, by not proposing "resource manager" for construction, Defendants tacitly concede that it is sufficiently structural and therefore not subject to § 112, ¶ 6. The '449 Patent discloses the structure of the "resource manager" and "communication manager" in parallel. Chmelar Decl. ¶¶ 102, 105. Since both are described as structural circuits, Defendants' inconsistent treatment of these terms is unwarranted, and their assertion that "communication manager" is subject to § 112, ¶ 6 must be rejected.

Third, identically to Defendants' constructions of "dropping means" and "interface means," addressed above, their construction of "communication manager" includes the language

"portion of the circuit," thereby acknowledging that the "circuit" of the '449 Patent, like the "circuit" of the '818 Patent, is sufficiently structural.

Nevertheless, if § 112, ¶ 6 were to apply, the parties' competing proposals for the function are similar. Thus, as with "dropping means" and "interface means," addressed above, the crux of the dispute is whether the structure is a "circuit" (NST's position) or whether the structure is a "portion of the circuit configured to implement the scheme disclosed in the '449 Patent at 10:19-24, 10:41-54" (Defendants' position).

Defendants' construction is the same as the TI Order's construction, which NST respectfully submits is incorrect. As with "dropping means," though Defendants' definition of the structure correctly references the structural "circuit" (consistent with NST's construction), by additionally inserting a requirement that such circuit "implement the scheme disclosed in the '449 Patent at 10:19-24, 10:41-54," the construction incorrectly and impermissibly inserts additional *functional* limitations embodied in these specification passages (e.g., describing possible scenarios where the communication manager refuses a connection and sends an error message). Such a construction is erroneous. *Micro Chem.*, 194 F.3d at 1258.

Therefore, as with "dropping means" and "interface means," if § 112, ¶ 6 applies, the correct structure is one that does not incorporate additional functional limits, such as NST's proposal: "circuit." Or, partially adopting the TI Order's construction, a permissible construction is "portion of the circuit configured to manage communication between modules."

E. "Mapping Means"

Term	NST's Construction	Defendants' Construction
"mapping means (A) for mapping the requested at least one communication	**<u>Not subject to § 112, ¶ 6:</u>** "mapping means": "circuit configured to map a requested communication service to	Subject to § 112, ¶ 6 **Function**: "mapping the requested at least one

Term	NST's Construction	Defendants' Construction
service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification." '052 Patent: claims 1, 2, 7	a connection." NST incorporates the agreed upon definition for the term "connection properties" and the remaining language should be afforded its plain and ordinary meaning. **<u>If the Court holds § 112, ¶ 6 applies:</u>** **Function**: "mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification" **Structure**: "circuit"	communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification." **Structure**: adapter unit/shell comprising a sequentializing unit and a desequentializing unit as disclosed in the '052 Patent at 5:58–6:3, 6:30–7:14, Figs. 1, 2A and 2B. Otherwise, indefinite.

NST's construction reflects what a POSITA would have understood this term to mean as used in the '052 Patent; namely, that a "mapping means" is a "circuit configured to map a requested communication service to a connection," and the remaining language should be afforded its plain and ordinary meaning. For instance, the '052 Patent's specification discloses an "**[i]integrated circuit,** comprising: … **a mapping means** (A)…" Chmelar Decl. ¶ 121 (citing '052 patent at 9:25-41) (emphasis added). Likewise, the Parties' stipulation as to the meaning of "integrated circuit" as "**interconnected circuitry on a chip**" further supports NST's proposed construction because a mapping means comprised in an integrated circuit must be circuitry of the integrated circuit. *Id.*

Defendants' argument that "mapping means" should be construed as part of a larger phrase under 35 U.S.C. § 112, ¶ 6 is incorrect, and is undermined by Defendants' inconsistent treatment of "interconnect means," which though contains the word "means" was not proposed by Defendants to be governed by § 112, ¶ 6. *See* § VI.A., *supra*. As discussed above, the presumption that the word "means" subjects a claim term to interpretation under § 112, ¶ 6 is rebutted where

the phrase describes structure. *Skky*, 859 F.3d at 1020 (finding "'wireless device means' does not invoke § 112, ¶ 6 because its clause recites sufficient structure"). Here, the claim language expressly describes sufficient structure by reciting that the "mapping means" is part of an "integrated circuit." '052 Patent at Claim 1 (an "integrated circuit comprising … a mapping means."). Moreover, the "network interface," which Defendants do not assert to be non-structural and subject to § 112, ¶ 6, is disclosed in one embodiment as "compris[ing] a mapping means for mapping the requested at least one communication service." '052 Patent at 3:23-24. Construing "mapping means" to be non-structural and subject to § 112, ¶ 6—where there is no dispute that network interface is a known structure—is irreconcilable to the patent's disclosure that the network interface hardware may comprise the "mapping means." Thus, because sufficient structure, *i.e.*, the integrated circuit and constituents thereof, is disclosed, § 112, ¶ 6 does not apply.

Nevertheless, if § 112, ¶ 6 does apply, Defendants' proposed construction is incorrect. The Parties agree on the function of the "mapping means," but disagree as to its structure. As Dr. Chmelar explains, Defendants' proposed structure unreasonably narrows the scope of the "mapping means." Chmelar Decl. ¶ 130-32. The intrinsic evidence assigns various structures that can perform the agreed upon function of the claimed "mapping means," including an "adapter unit A" ('052 Patent at 5:10, 5:12, 5:58, 5:61, 6:34, 6:37, and 6:41) and "shell A" ('052 Patent at 6:46, 6:41-42 ("these adapter units A may also be considered as shells …"). Chmelar Decl. ¶ 130. A POSITA would not understand the intrinsic evidence to limit the structure of the "mapping means" to "a sequentializing unit and a desequentializing unit," as Defendants suggest. *Id.*

Defendants' construction additionally suffers from the same infirmity as its constructions of "dropping means," "interface means" and "communication manager," addressed above, insofar as its construction of "mapping means" similarly seeks to incorporate specification passages,

thereby inserting additional *functional* limitations contained in these specification passages (e.g., describing "packetization/depacketization," "schedules," and "implement the connections"). However, as explained above, this is impermissible and erroneous. *See Micro Chem.*, *supra*.

A POSITA would readily understand that a "circuit" performs the function of the "mapping means." *Id.* ¶ 131. In particular, a POSITA would understand that mapping is performed using well-known structures such as mapping logic, *i.e.*, digital logic circuitry, gates, or look-up tables, *i.e.*, memory circuitry. *Id.* Moreover, asserted claim 1 requires the mapping means to map "the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification." '052 Patent at claim 1. While the mapping may involve sequentializing and desequentializing, by "a sequentializing unit and a desequentializing unit," a POSITA would recognize that the mapping means is not so limited. Chmelar Decl. ¶ 131.

Accordingly, if the Court construes "mapping means" under § 112, ¶ 6, the Court should reject Defendants' overly narrow construction and adopt NST's proposed construction.

F. "arranging … the first and second information comprising said issued message as a single address"

Term	NST's Construction	Defendants' Construction
"arranging … the first and second information comprising said issued message as a single address" '9893 Patent: claim 4	"arranging … the first and second information comprised in said issued message as a single address"	Indefinite.

The question here is whether the "first information" and "second information" is "**comprised in**" the "issued message" (i.e., the "message" has the "first" and "second" information within it) or whether the "first information" and "second information" is "**comprising**" the "issued

message" (i.e., "message" is within the "first" and "second" information), which is how step (b) of claim 4 is written. From the specification and surrounding claim language, which makes clear that the "message issued by an addressing module M **comprises**: first information…and second information," a POSITA would understand that "the first and second information" is "**comprised in** said issued message." Chmelar Decl. ¶ 153-55; '9893 Patent at claim 4.

Indeed, claim 4 recites that "a message issued by an addressing module M **comprises**: first information … and second information." Chmelar Decl. ¶ 153; '9893 Patent at claim 4. The specification confirms this understanding. Chmelar Decl. ¶ 154; '9893 Patent at 3:16-22 ("the message **comprises** first information indicative for the location of the addressed module(s) within the network. The message may further **include** second information indicative for a particular location within the module, such as memory, or a register address"); *see also id.* 3:46-49; 4:19-23.

Defendants' suggestion that this term is indefinite defies the intrinsic evidence and POSITA's understanding of the term. Chmelar Decl. ¶ 155. In contrast, NST's construction appropriately affords the true meaning to a term containing an obvious "clerical or typographical mistake," which is "clearly evident from the specification, drawings, and prosecution history." *Superior Fireplace Co. v. Majestic Prods. Co.*, 270 F.3d 1358, 1376 (Fed. Cir. 2001). The claim and specification consistently disclose that the message "comprises" the first information and the second information. '9893 Patent, Claim 4, 3:16-22; Chmelar Decl. ¶¶ 153-55. "[C]laims must be construed so as to be consistent with the specification, of which they are a part." *Merck & Co. v. Teva Pharms. USA, Inc.*, 347 F.3d 1367, 1371 (Fed. Cir. 2003) ("[a] fundamental rule of claim construction is that terms in a patent document are construed with the meaning with which they are presented in the patent document."). NST's construction corrects a clear typographical error in the claims to allow the term to be construed consistent with its usage in the specification.

For these reasons, the Court should adopt NST's construction.

G. "each data package comprising N data elements"

Term	NST's Construction	Defendants' Construction
"each data package comprising N data elements" '2893 Patent: claims 1, 10	"data package": "fixed-size arrangement of data." "data elements": "groups of data." The remaining language should be afforded its plain and ordinary meaning.	"every data package communicated by the network stations has a fixed size of N data elements"

NST's construction reflects what a POSITA would have understood this term to mean as used in the '2893 Patent. The main dispute between the Parties is over Defendants' inclusion of the word "every" in their proposed construction of the term. NST's position is that a "fixed-size arrangement" of "N data elements" refers to the fact that the number of data elements in a given data package must remain fixed (*i.e.,* constant) throughout the course of each communication. While the number of data elements can vary between one data package and the next, the number for any given data package cannot fluctuate (*i.e.*, must remain "fixed"). *See* Chmelar Decl. ¶ 167. Conversely, Defendants' introduction of the word "every" requires that all (*i.e.*, "every") data packages ever communicated across an integrated circuit to contain the same exact number of data elements. By doing so, Defendants seek to inject a limitation that is not supported by the claims or the specification. Chmelar Decl. ¶¶ 168, 173. In other words, Defendants' construction reads: "[each and] every data package [ever] communicated by the network stations [must have the same] fixed size of N data elements." This overly narrow construction is in direct contravention to the teachings of the '2893 Patent.

NST's construction also best reflects the language actually used in the claims and the specification itself. For instance, Defendants seek to substitute the word "each" for "every" in the claims. However, the word "every" is never used to describe "data package comprising N data

elements" anywhere in the '2893 Patent. Instead, the claims and the specification repeatedly disclose "***each*** data package." '2893 Patent at Abstract, 2:3, 3:40, and 4:52. Put simply, Defendants' construction would profoundly alter the meaning of the disputed term from "***each*** data package ***individually***" to "***all possible*** data packages ***collectively***." Chmelar Decl. ¶¶ 171-73. This must be rejected.

As for the rest of NST's construction, Defendants do not appear to dispute NST's proposal that the data elements be construed as "groups of data." For instance, a person of ordinary skill would understand Figure 3 to show that data elements are grouped into respective data packages. Chmelar Decl. ¶ 167, 171-73. This grouping is also shown in other figures, including Figure 4 below, where the individual data elements "h," "d0," and "d1" in each row are grouped together in separate data packages. '2893 Patent at 7:58-61 ("a data package consisting of data elements h, d0 and d1"). Consistent with this interpretation, the specification further discloses that data elements are "sent" together as part of a "data package." *See, e.g.*, '2893 Patent at 7:58-61 ("a data package consisting of data elements h, d0 and d1 is sent from data router 120 to data router 140."). A person of ordinary skill would understand this to mean that individual "data elements" are grouped together and sent as a "data package." Chmelar Decl. ¶ 173.

For these reasons, the Court should adopt NST's construction.

H. "Determination Unit"

Term	NST's Construction	Defendants' Construction
"determination unit" '800 Patent: claim 12	**<u>Not subject to § 112, ¶ 6:</u>** "circuit that makes determinations based on stored or received information" **<u>If the Court holds § 112, ¶ 6 applies:</u>**	Subject to § 112, ¶ 6. **Function**: "determine a first/second amount of data to be buffered by the first/second memory" and for at least one of the first determination unit and the

Term	NST's Construction	Defendants' Construction
	Function: "determine an optimal amount of data to be buffered" and "determine an optimal moment for sending the data" **Structure**: "circuit"	second determination unit "determine an optimal moment for sending data." **Structure**: Indefinite.

NST's construction of "determination unit" as a "circuit that makes determinations based on stored or received information" reflects what a POSITA would have understood the term to mean as used in the '800 Patent. Chmelar Decl. ¶ 193. The '800 Patent expressly discloses a machine: "systems on chip, i.e., a plurality of modules on the same chip (including e.g. system in a package, multi-die modules) or on different chips, communicate with each other via some kind of interconnect. The interconnect is embodied as a network on chip NOC." '800 Patent at 5:7-11. Moreover, the '800 Patent is also directed to hardware circuitry; nowhere does the Asserted Patent disclose or claim intangible software or firmware. Chmelar Decl. ¶ 198. This is consistent with the Parties' agreed construction of "integrated circuit" as "interconnected circuitry on a chip" which is recited in the disputed claim's preamble. Dkt. 91, Appendix 1; '800 Patent at Claim 12.

This is also consistent with the '800 Patent's disclosure of "[t]he determination of the optimal burst length may be performed based on information ***stored in*** the determination units BDLU [sic] 1, 2 or on information received from the network N or IP blocks," '800 Patent at 6:62-65, since information ***can be stored only in*** storage circuitry, such as latches, flip-flops, registers, or memory cells. Chmelar Decl. ¶ 199. In another embodiment, the "determination units" (BLDU) are physically located, or "arranged[,] in the network interfaces NI associated to the slave S and master M, respectively." *Id.* ¶ 197 (quoting '800 Patent at 6:47-53); '800 Patent at Fig. 2. Because the determination unit is housed within the network interfaces NI, "data is [therefore] buffered in the network interface NI, i.e. the interconnect surface, such that the master M or slave S, which

may constitute intellectual property block [that] are not involved in the actual communication or the communication protocol for communicating over the interconnect or network." *Id*. at 7:34-40. Further still, in another embodiment, the "wrapper means comprise a determination unit BLDU for determining the optimal first or second amount of data to be buffered." *Id*. at 4:18-24. Again, information cannot be buffered except with storage *circuitry*, which, as discussed previously, the Federal Circuit has held is inherently structural. *See* § VI.B., *supra* (collecting cases).

In further alternative embodiments, the "determination unit" itself may be the network interface or wrapper, as applicable. '800 Patent at 8:34-36 ("In the device claim enumerating several means, several of these means can be embodied by one and the same item of ***hardware***"). Notably, Defendants do not dispute that such network interface NI is not subject to § 112, ¶ 6. Construing "determination unit" to be non-structural and subject to § 112, ¶ 6 where there is no dispute that network interface NI is a known structure is irreconcilable to the patent's disclosure that the determination unit and the network interface NI may be embodied by the same hardware.

For these reasons, Defendants cannot overcome the presumption against subjecting "determination unit" to § 112, ¶ 6. Nevertheless, if § 112, ¶ 6 were to apply, Defendants' proposal is incorrect. NST and Defendants proposed similar functions for the "determination unit." Yet, Defendants contend that the "determination unit" is indefinite because it allegedly lacks structure. Defendants' proposed construction is in direct contravention of a POSITA's understanding of the term and the intrinsic evidence. Chmelar Decl. ¶ 193-200.

As discussed above, a POSITA having reviewed the intrinsic evidence would recognize that the "determination unit" is a circuit within the integrated circuit. *Id.* ¶¶ 195-200 (citing '800 Patent at 11:44-12:5; 4:18-24). This is especially true because the '800 Patent refers to the "determination unit" as an "item of hardware." *Id.* ¶ 198 (quoting '800 Patent at 8:34-36). A

POSITA would similarly recognize that the network interface may include the determination unit. *Id.* ¶ 197 (citing '800 Patent at 6:47-53). Notably, Defendants concede that the network interface is structural. Because the determination unit is included in the network interface, which both parties agree is structural, the determination unit is also structural. Thus, Defendants' contention that the "determination unit" is indefinite must be rejected.

I. "Optimal Amount"

Term	NST's Construction	Defendants' Construction
"optimal amount of data to be buffered" '800 Patent: claim 12	Plain and ordinary meaning	Indefinite

The "optimal amount" term relates to buffering, or storing, an amount of data that is optimal to send given the physical configuration of the network and the rules, or constraints, placed on the transmission by the communication properties. '800 Patent at 6:47-53; Chmelar Decl. ¶ 179.

Indeed, the '800 Patent makes clear that its overarching goal is to improve utilization of the network by "buffer[ing] data until the buffered data is sufficiently large to be transferred optimally…in a packet" because "the larger a packet is …overhead is reduced and the interconnect is utilized more efficiently." '800 Patent at 4:49-57; *see also id.* at 3:35-37, 4:18-28.

The "optimal amount" term requires no construction beyond its plain and ordinary meaning. Defendants' position that this term is indefinite under § 112 is incorrect, as the term is readily understandable to a POSITA in light of the intrinsic and extrinsic evidence.

Indeed, as Dr. Chmelar observes, multiple passages of the specification confirm that the '800 Patent discloses an invention for improving—indeed, for optimizing—interconnect utilization in a network, where the improvement is achieved by buffering data until conditions for an optimal transfer are satisfied. Chmelar Decl. ¶ 178 (citing '800 Patent at 3:35-37, 4:18-28, 4:49-

57, 6:15-17,6:22-30, 6:31-36, 7:23-28, 7:44-51). From these passages, Dr. Chmelar concludes: (1) buffering of data improves and/or optimizes interconnect utilization; (2) the optimal amount of data to be buffered can be based on communication properties of a communication and (3) the optimal amount of data to be buffered can be specific to a particular interconnect. *Id.* ¶ 179. As Dr. Chmelar concludes, the "optimal amount of data" is not a fixed quantifier but based on certain conditions such as communication properties and/or interconnect (i.e., network) characteristics. *Id.* Thus, a POSITA would understand that a "first optimal amount of data to be buffered" equates to the amount of data that is optimal under certain conditions. *Id.*

Affording this term its plain and ordinary meaning is also supported by case law, wherein the term "optimal" has been afforded its plain and ordinary meaning. *See, e.g.*, *Bitmicro LLC v. Kioxia America, Inc., et al.*, Case 6:22-cv-00331 (W.D. Texas Feb. 16, 2023). A POSITA would understand that the '800 Patent uses the term "optimal amount" in its plain and ordinary sense, *i.e.*, optimal amount of data to be buffered based on certain conditions, which is supported by dictionary definitions at the time of the invention which define "optimal" as the "[m]ost favorable or desirable; optimum" and "optimum," which further means "[t]he point at which the condition, degree, or amount of something is the most favorable." Ex. 9.

The TI Order found "optimal amount" to be indefinite, a finding which NST respectfully submits is incorrect. The TI Order's holding of indefiniteness rests upon the finding that the "optimal amount of data to be buffered" is purely subjective. Ex. 8 at 52. This finding, however, is based on a misapprehension of the role of the chip designer. The TI Order mistakenly assumed that the chip designer, using his or her subjective opinion, would determine the "optimal amount." *Id.* at 54. This is not so. The chip designer determines the physical layout of the network, the communication properties to be applied, and, if multiple communication properties are to be

applied, the priority and interaction amongst such properties. Chmelar Decl. ¶¶ 179-182. But the chip designer **does not** determine the "optimal amount of data to be buffered" (which may potentially render the term subjective and indefinite); instead, the hardware "determination unit" of the "integrated circuit" determines the "optimal amount" based on the physical layout and communication properties. *Id.* (citing '800 Patent at 6:47-53). This is a machine-made decision with a result that is objectively determinable and, therefore, definite.

The '800 Patent lists latency, which is a measure of delay, as a connection property. '800 Patent at 5:27-35. Using this example, if the connection properties impose a latency constraint of a maximum of one-tenth of a millisecond, then the "optimal amount" is the most data that can be transmitted in under one-tenth of a millisecond given the physical characteristics of the network (e.g., data path width, etc.). *See* Chmelar Decl. ¶ 181. This amount is objective and definite.

Thus, Defendants' position (and the TI Order's conclusion) that "optimal amount" is indefinite is undermined by the '800 Patent's disclosure of when and how optimal transfer conditions are satisfied. Chmelar Decl. ¶ 178; *see also* '800 Patent at 4:18-28; 4:49-57; 6:15-17; 6:22-30; 6:31-36; 7:23-28; 7:44-51. Thus, a POSITA would not consider this term to be indefinite. *Id*. ¶ 183.

J. "Optimal Moment"

Term	NST's Construction	Defendants' Construction
"optimal moment for sending the data" '800 Patent: claim 12	Plain and ordinary meaning	Indefinite

The "optimal moment" term relates to the moment the "optimal amount" of data (addressed above) is transmitted. A POSITA would understand "optimal moment" to relate to the "transmission moment" (*i.e.*, when transmission occurs) whereas the "transmission" would refer

to the "data to be transmitted." Chmelar Decl. ¶ 187 (citing '800 Patent at 3:14, 7:4-6).

The specification further confirms that a POSITA would understand "transmission moment" to sufficiently disclose the "optimal moment." For example, the specification discloses:

> . . . the **transmission moment may be determined in a similar way** by the first and second determination means BLDU1, BLDU2. **For a guaranteed throughput GT connection, data should wait for one of the slots reserved for its connection.** Using a "flush"-like signal/flag may force the sending of the data in advance. Alternatively, **for a best effort BE connection, a round robin arbitration across connections in the NI can be used.**

'800 Patent at 7:4-14 (emphases added). Throughput is a communication property that encompasses guaranteed throughput (GT) as a lower bound whereas best effort (BE) does not. Chmelar Decl. ¶ 188. Further, as recited in claim 12, throughput is one of the connection properties that is used to determine the "optimal moment" for transmitting data. *See id*.; *see also* '800 Patent at 12:16-32 ("wherein the communication properties include . . . throughput where a lower bound on throughput is guaranteed"). Since the transmission moment is determined based on the same connection properties as the "optimal moment," a POSITA would understand an "optimal moment" to be the "transmission moment" (*i.e*., the moment in which data transmitted), where the moment is based on the recited connection properties, including at least throughput. Chmelar Decl. ¶ 189. The cited passage discloses that, in the example of a guaranteed throughput communication property, the "optimal moment" is when "one of the slots reserved" is available to accommodate the "optimal amount" of data. Chmelar Decl. ¶ 187 (citing '800 Patent at 7:4-14). This moment is definite and determinable. Accordingly, a POSITA would understand the term "optimal moment" to not be indefinite and should be afforded its plain and ordinary meaning.

As with "optimal amount," the TI Order concluded that "optimal moment" is indefinite because it is "purely subjective." Again, NST respectfully submits that this conclusion was incorrect because it rests on a misapprehension of the respective roles of the chip *designer* and the

chip itself. Just as the "optimal amount" is determined by the determination unit of the chip based on the physical layout of the network and the communication properties, so too is the "optimal moment." *See* Chmelar Decl. ¶¶ 179-182, 189. The designer merely determines what the physical layout and communication properties are; the chip determines the optimal amount and optimal moment.

K. "said first wrapper" / "said second wrapper"

Term	NST's Construction	Defendants' Construction
"said first wrapper" / "said second wrapper" '800 Patent: claim 12	"said first memory" / "said second memory"	Indefinite

A POSITA would understand that the claim and specification equate the "[first/second] wrapper" to the "[first/second] memory." Chmelar Decl. ¶ 210. Specifically, claim 12 recites "a first memory for buffering first data … a second memory for buffering second data … wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper." Chmelar Decl. ¶ 210 (quoting '800 Patent, claim 12). A POSITA would recognize that the first/second memory are the only claim elements that buffer the first/second data, respectively. *Id.* Thus, a POSITA would recognize from the claim language alone that the first wrapper refers to the first memory and that the second wrapper refers to the second memory. *Id.*

The intrinsic evidence further supports this understanding. In particular, the specification refers to the wrapper as the component that buffers data. Chmelar Decl. ¶ 210 (citing '800 Patent at 3:41-43; 3:54-56; 4:1-2; 4:7-8; 4:18-22; 4:41-43; 5:60-64; 6:4-14; 6:31-38). With the understanding that the wrapper buffers data, coupled with claim 12 reciting that the memory

buffers data, a POSITA would readily understand that the wrapper and memory are used interchangeably. *Id.* Thus, a POSITA would understand that "said [first/second] wrapper" in claim 12 means "said [first/second] memory."

Defendants effectively concede that the Court should adopt NST's proposed construction by separately arguing that "said [first/second] wrapper" means "said first/second memory" in their proposed function for "determination unit." *See* § VI.H, *supra*. Defendants cannot credibly suggest that it is unclear whether "said [first/second] wrapper" is meant to refer back to the previously recited "[first/second] memory." Moreover, because the "[first/second] wrapper" unit is included in the network interface, which both parties agree is structural, the "[first/second] wrapper" is also structural. Thus, Defendants' contention that the ""said [first/second] wrapper" " is indefinite must be rejected and the Court should adopt NST's construction.

VII. Conclusion

For the foregoing reasons, Plaintiff respectfully requests that the Court adopts its proposed claim construction positions.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that all counsel of record are being served on February 20, 2024 with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3).

/s/ William E. Davis, III
William E. Davis, III