IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

NETWORK SYSTEM TECHNOLOGIES, LLC,	)	
	)	
Plaintiff,	)	
	)	
v.	)	Civil Action No. 1:22-cv-1331
	)	
QUALCOMM INCORPORATED;	)	**JURY TRIAL DEMANDED**
QUALCOMM TECHNOLOGIES, INC.;	)	
ARTERIS, INC.,	)	
	)	
Defendants.	)	
	)	

QUALCOMM INCORPORATED, QUALCOMM TECHNOLOGIES, INC., AND ARTERIS, INC.'S SUPPLEMENTAL INVALIDITY CONTENTIONS

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I. INTRODUCTION

Qualcomm Incorporated and Qualcomm Technologies, Inc. (collectively "Qualcomm") and Arteris, Inc. ("Arteris") (collectively with Qualcomm, "Defendants") hereby provide to Plaintiff Network System Technologies, LLC ("NST" or "Plaintiff") supplemental Invalidity Contentions concerning U.S. Patent Nos. 7,366,818 (the "'818 patent"); 7,373,449 (the "'449 patent"); 7,594,052 (the "'052 patent"); 7,769,893 (the "'9893 patent"); 8,072,893 (the "'2893 patent"); and 8,086,800 (the "'800 patent") (collectively, "the Asserted Patents"). Through these supplemental invalidity contentions, Defendants do not withdraw any of the invalidity contentions included in their initial contentions and instead merely add positions that Defendants identified after they served their initial contentions. Defendants are serving the following exhibits with these supplemental contentions.

Chart	Reference	Filing Date	Date of Issue or Publication	Citation	Patent
B-13S	K. Goossens, et al., *Networks on Silicon: Combining Best-Effort and Guaranteed Services*		Aug. 7, 2002	Goossens2002	U.S. Pat. No. 7,373,449
B-14S	K. Goossens, et al., *Guaranteeing the Quality of Services in Networks on Chip*		Jan. 31, 2003	Goossens2003	U.S. Pat. No. 7,373,449
B-15S	U.S. 5,461,611	June 7, 1994	Oct. 24, 1995	Drake	U.S. Pat. No. 7,373,449
B-16S				Combination References	U.S. Pat. No. 7,373,449
C-1S	U.S. 7,165,094	Mar. 9, 2001	Jan. 16, 2007	Weber	U.S. Pat. No. 7,594,052
C-1S	U.S. Pub. No. 2002/0129173	Mar. 9, 2001	Sept. 12, 2002	Weber	U.S. Pat. No. 7,594,052

C-18S	A. Radulescu, et al., *An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared Memory Abstraction, and Flexible Network Configuration*		Feb. 16, 2004	2004 Radulescu	U.S. Pat. No. 7,594,052
C-20S	Open Core Protocol Specification, Release 1.0, OCP-IP Association (2001)		2001	OCP	U.S. Pat. No. 7,594,052
C-21S				Combination Reference	U.S. Pat. No. 7,594,052
E-2S	U.S. 6,081,844	Jan. 26, 1998	Jun. 27, 2000	Nowatzyk	U.S. Pat. No. 8,072,893
E-5S	D. Bertozzi *et al*., *Xpipes: A Network-on-Chip Architecture for Gigascale Systems-on-Chips*		Sep, 3, 2004	Xpipes	U.S. Pat. No. 8,072,893
E-13S	Axel Jantsch and Hannu Tenhunen, *Networks on Chip*		January 2003	Jantsch	U.S. Pat. No. 8,072,893
E-16S	Soha Hassoun, et al., *Optimal Buffered Routing Path Constructions for Single and Multiple Clock Domain Systems*		Nov. 2002	Hassoun	U.S. Pat. No. 8,072,893
E-17S	John Dielissen, et al., *Concepts and Implementation of the Philips Network-on-Chip*		Nov. 2003	Dielissen	U.S. Pat. No. 8,072,893
E-18S	Jose Duato, et al., *Interconnection Networks an Engineering Approach*		1997	Duato	U.S. Pat. No. 8,072,893
E-19S	Andrei Radulescu, et al., *An Efficient On-Chip NI Offering*		Jan. 2005	Radulescu 2005	U.S. Pat. No. 8,072,893

	Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration				
E-20S	Pasquale Cocchini, *Concurrent Flip-Flop and Repeater Insertion for High Performance Integrated Circuits*		Nov. 2002	Cocchini	U.S. Pat. No. 8,072,893
E-21S	U.S. 6,029,220	Oct. 8, 1992	Feb. 22, 2000	Iwamura	U.S. Pat. No. 8,072,893
E-22S				Combination Reference	U.S. Pat. No. 8,072,893
F-1S	U.S. 5,434,872	July 28, 1992	July 18, 1995	Petersen	U.S. Pat. No. 8,086,800
F-2S	WIPO Pub. No. 2004/034176	Oct. 7, 2003	Apr. 22, 2004	Radulescu II	U.S. Pat. No. 8,086,800
F-19S	Andrei Radulescu, et al, *An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration*		Feb. 2004	Radulescu III	U.S. Pat. No. 8,086,800
F-20S	U.S. Pat. App. No. 2002/0186660	Jun. 12, 2001	Dec. 12, 2002	Bahadiroglu	U.S. Pat. No. 8,086,800
F-21S	U.S. Pat. No. 6,769,030	Feb. 7, 2000	July. 27, 2004	Bournas	U.S. Pat. No. 8,086,800
F-22S	U.S. Pat. No. 7,355,971	Oct. 22, 2001	Apr. 8, 2008	Jason	U.S. Pat. No. 8,086,800
F-23S				Combination Reference	U.S. Pat. No. 8,086,800

Defendants do not withdraw any of the exhibits included with their initial invalidity contentions and intend to rely on those exhibits as well as the exhibits served herewith. Defendants counsel hereby certifies that they undertook reasonable efforts to prepare their initial invalidity contentions and the amendments provided herein are based on material (e.g. references, understanding of references, expert opinions, understandings of NST's claim construction positions, and/or updated caselaw) that Defendants identified after the preliminary invalidity contentions were served.

These Invalidity Contentions address the following asserted claims, which were identified by Plaintiff in its May 26, 2023 Disclosures of Asserted Claims and Infringement Contentions, and its disclosure on August 18, 2023 which substituted claim 10 of the 800 patent with claim 12 of the 800 patent, (collectively "Infringement Contentions") (with independent claims identified in **bold**):

No.	Asserted Patent	Asserted Claims (Qualcomm)	Asserted Claims (Arteris)
1	7,366,818	**1**-3 and 5-7	**1**-3 and 5-7
2	7,373,449	**10**-16	**10**-16
3	7,594,052	**6**	**6**
4	7,769,893	**4**-11	**4**-11
5	8,072,893	**10**	**10**
6	8,086,800	**12**	**12**

Defendants contend that each of the claims asserted by Plaintiff is invalid under at least one or more of 35 U.S.C. §§ 101, 102, 103, and 112. Defendants hereby incorporate by reference in their entirety invalidity contentions (including any supplementations) served in related litigations, including contentions served in *Network System Technologies, LLC v. Texas*

Instruments Inc. et al., No. 2:22-cv-00482 (E.D. Tex.) and *Network System Technologies, LLC v. Samsung Electronics Co. Ltd.* et al., No. 2:22-cv-00481 (E.D. Tex.).

II. RESERVATION OF RIGHTS

Defendants' invalidity contentions are based on their current knowledge of the Asserted Patents, the prior art, Plaintiff's infringement contentions, and upon information presently and reasonably available to Defendants. This litigation is in the early stages, and Defendants' investigation of the prior art is ongoing. Consistent with the Federal Rules of Civil Procedure, Defendants reserve the right to supplement, amend, modify, revise, or correct any aspect of their invalidity contentions and to provide additional information as such information becomes available through discovery or otherwise. No aspect of Defendants' invalidity contentions shall be deemed to be an admission that their invalidity contentions are complete. In particular, Defendants reserve the right to supplement their invalidity contentions as discovery continues and after any further claim construction by the Court. In addition, Defendants also reserve the right to supplement their invalidity contentions should Plaintiff subsequently attempt to amend its Infringement Contentions in any way, or to otherwise modify its infringement allegations against Defendants or seek to establish an earlier date of invention (while reserving all rights to challenge any attempt by Plaintiff to do so).

Defendants further reserve the right to supplement their invalidity contentions with information subsequently provided by Plaintiff concerning its infringement contentions. Plaintiff's Infringement Contentions fail to identify specifically for many of the asserted claim limitations the allegedly infringing structures and acts in the accused products and methods. Examples of deficiencies in Plaintiff's infringement contentions are identified in the letters Qualcomm sent to Plaintiff on June 22, 2023 and August 30, 2023, and the letter Arteris sent to

Plaintiff on July 28, 2023. Plaintiff's failure to identify specifically infringing structures and acts prevents Defendants from searching for, locating, presenting, and relying on prior art having all or some of such structures and acts, thus effectively denying Defendants the opportunity to rely on the fundamental principle that whatever infringes a claim if later in time anticipates the claim if earlier in time, and further denying Defendants the opportunity to conduct other invalidity analytical methods.

Moreover, Defendants reserve the right to revise their ultimate contentions concerning the invalidity of the claims of the Asserted Patents based upon the Court's construction of the claims of the Asserted Patents, any findings as to the priority dates of the Asserted Claims, and/or positions that Plaintiff, Defendants, or any expert witness may take concerning claim interpretation, infringement, and/or invalidity issues.

Prior art not included in this disclosure, whether known or not known to Defendants, may become relevant. In particular, Defendants are currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the Asserted Claims are not disclosed in the prior art identified by Defendants. To the extent that Plaintiff contends that limitations of the asserted claims are not disclosed in the prior art identified by Defendants, Defendants reserve the right to identify other references that would have made the addition of the allegedly missing limitation to the disclosed device or method obvious or show that the allegedly missing limitation would have been known or readily apparent to one of ordinary skill in the art at the time of the alleged invention in light of the disclosure of the prior art at issue. Defendants reserve the right to rely on any reference found in the prosecution histories of the applications leading to the asserted patents or otherwise identified in connection with this litigation. Further, Defendants reserve the right to rely on any reference or item sought or to be sought from third parties that is solely within those

third parties' possession, custody, or control, and has not yet been produced during discovery. Defendants may issue subpoenas to third parties believed to have knowledge, documentation and/or corroborating evidence concerning some of the prior art listed herein and/or additional prior art. These third parties include, but are not limited to, the authors, employers of authors, inventors, assignees, or former or current employee of assignees, of the references identified or the Asserted Patents, and of other parties accused of infringing the asserted patents in this or related litigation matters. Defendants reserve the right to supplement these contentions in light of any newly discovered information produced by these or other companies from which Defendants may seek discovery.

Much of the art identified in the attached exhibits reflects common knowledge and the state of the art before the filing date of the asserted patents. In many instances where a particular contention calls for combining references, any one of a number of references can be combined. The inclusion of certain exemplary combinations of prior art references does not exclude other combinations based upon the claim charts attached hereto. Moreover, Defendants reserve the right to rely on the general knowledge of a person of skill in the art to demonstrate that any claim element would have been obvious.

Each of the Asserted Claims of the Asserted Patents is anticipated by and/or obvious in view of one or more of the items of prior art identified herein alone or in combination with other prior art references. Defendants' claim charts in Exhibits A–F cite to or reference particular teachings and disclosures of the prior art as applied to features of the Asserted Claims, but persons having ordinary skill in the art generally may view an item of prior art in the context of other publications, literature, products, and understanding. As such, the cited portions are only examples, and Defendants reserve the right to rely on uncited portions of the prior-art references

and on other publications and expert testimony as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that the prior art discloses a claim limitation. Defendants further reserve the right to rely on uncited portions of the prior-art references, other publications, and testimony to establish reasons for combining certain cited references that render the Asserted Claims obvious. The references discussed in the claim charts in Exhibits A–F may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame.

Defendants intend to rely on admissions concerning the scope of the prior art relevant to the Asserted Patents found in, *inter alia*: the Asserted Patents and related patents and/or patent applications; the patent prosecution histories for the Asserted Patents and related patents and/or patent applications (including all prior art cited therein); any deposition testimony of the named inventors of the Asserted Patents and related patents and/or patent applications in this matter or any other matter; evidence and testimony relating to the level of ordinary skill in the art; evidence from prior litigation, administrative proceedings, and correspondence involving the Asserted Patents and related patents; and the papers filed and any evidence submitted by Plaintiff in connection with this matter or the related matters involving the Asserted Patents.

To the extent that these Invalidity Contentions rely on or otherwise embody particular constructions of terms or phrases in the Asserted Claims, Defendants are not proposing or adopting any such constructions as proper constructions of those terms or phrases at this time. For purposes of these Invalidity Contentions, Defendants may adopt alternative claim construction positions and broadly interpret each term or phrase. Certain of these contentions may be based on claim constructions that appear to underlie Plaintiff's infringement contentions or claim construction positions in this or in earlier cases. Defendants, however, do not concede

that Plaintiff's apparent constructions are proper, and expressly reserve the right to contest any such constructions. In addition, to the extent that these Invalidity Contentions suggest or imply a particular order in which the steps of method claims are performed, Defendants do not necessarily propose that the method claims must be limited to such order, although Defendants reserve the right to propose such an order.

Moreover, Defendants do not admit that any accused product, method, or service infringes any of the asserted claims. Nothing stated herein shall be treated as an admission, acknowledgement, acquiescence, or suggestion regarding the scope of any of the asserted claims or that any accused technology meets any limitations of the claims. Nothing stated herein shall be construed as an admission or a waiver of any particular construction of any claim term. Moreover, use of terms herein from the Asserted Patents should not be understood to mean that such terms as used in the Asserted Patents, or claims, thereof are definite, enabled, or supported by adequate written description in accordance with 35 U.S.C. §§ 112(1), (2), (6). Likewise, use of terms herein from the Asserted Patents should not be understood to suggest or imply a common, usual, ordinary, customary, plain, or accepted meaning in the art for any such term.

Defendants Invalidity Contentions are made in a variety of alternatives and do not represent Defendants' agreement or view as to the meaning, definiteness, written description support for, or enablement of any claim contained therein. Given that the Court has not yet made any claim construction ruling in this action, Defendants' Invalidity Contentions are made in a variety of alternatives, and are not intended to necessarily be consistent with each other and/or Defendants' other contentions in this action, and should not be otherwise construed. Defendants' contentions herein are not, and should in no way be seen as, admissions or adoptions as to any particular claim scope or construction, or as any admission that any particular claim element is

met in any particular way. Defendants object to any attempt to imply claim constructions from any identification of potential prior art. Additionally, Defendants' Invalidity Contentions may use Plaintiff's improper assertions of infringement and improper applications of the claims to understand Plaintiff's view of the scope of the asserted claims. Defendants do not agree with Plaintiff's application of the claims and deny infringement. Further, to the extent an accused product or feature comprises or arises from prior art, Defendants contend, without admitting purported infringement, that the asserted patents are anticipated and/or made obvious in light of that prior art and Plaintiff's own Infringement Contentions.

In those instances where Defendants assert that the claims are invalid under 35 U.S.C. § 112 (e.g., no written description, not enabled, and/or indefinite), Defendants have applied the prior art in part in accordance with Defendants' assumptions that Plaintiff: (1) contends those claims are definite, (2) finds written description support for those claims, and (3) contends that those claims are enabled. However, Defendants' prior art invalidity contentions do not necessarily represent Defendants' agreement or view as to the meaning, definiteness, written description support for, or enablement of any claim contained therein. In fact, Defendants note numerous grounds for invalidity on such bases below.

Defendants have, in the attached appendices, identified examples of where the subject matter recited in the preambles of the asserted claims may be found in various prior art references, without regard to whether the preambles are properly considered to be limitations of the asserted claims. Defendants reserve the right to argue that any of the preambles are or are not limiting during the claim construction proceedings in this case.

Defendants' Invalidity Contentions are based at least in part on the claimed priority dates that appear on the faces of the Asserted Patents and may also address any claims by Plaintiff to

have sworn behind such dates. Defendants reserve the right to challenge Plaintiff's claimed priority dates for the Asserted Patents, based on the faces of the Asserted Patents or sworn behind or otherwise, as discovery continues and after any further claim construction by the Court, including based on Plaintiff's proposed (or implicit) claim construction positions or other facts learned during discovery.

Discovery is ongoing, and Defendants reserve the right to assert invalidity under 35 U.S.C. §§ 101 and 102(a)-(g) to the extent that discovery or further investigation yield additional information forming the basis for such claims. Defendants reserve the right to assert that any Asserted Patent is invalid under 35 U.S.C. §§ 102(f) and 116 in the event Defendants obtain evidence that one or more of the named inventors should not have been named as an inventor, or that one or more persons who should have been named as an inventor was not named. In either event, Defendants will supplement their contentions to address the misjoinder and/or non-joinder of inventors by, *inter alia*, identifying the persons who should not have been named inventors (or who should have been named) and describing the relevant facts and circumstances.

Defendants have provided disclosures and related documents pertaining only to the Asserted Claims as identified by Plaintiff in its Infringement Contentions. Defendants reserve the right to modify, amend, or supplement these Invalidity Contentions to show the invalidity of any additional claims that the Court may allow Plaintiff to later assert. Defendants further reserve the right to supplement its document production should it later find additional, responsive documents.

III. PRIORITY AND CONCEPTION DATES FOR THE ASSERTED CLAIMS

Defendants provide the following response to the priority dates Plaintiff suggest applies to the patents-in-suit in Plaintiff's infringement contentions. Defendants note that under 35

U.S.C. § 102(b), a patent is invalid over any invention that is patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States, irrespective of its priority date. Therefore, Plaintiff's claim for an earlier priority date may not be relevant to the prior art status of certain references.

A. U.S. Patent No. 7,366,818

In its Infringement Contentions, NST asserts that the Asserted Claims of the '818 patent are entitled to claim priority from EP02079196, filed on October 8, 2002. Defendants dispute that the Asserted Claims of the '818 patent are entitled to claim priority from EP02079196 because, among other things, EP02079196 does not disclose any structure for at least the claimed "dropping means (DM) for dropping data" and "wherein said interface means (ANIP, PNIP) comprises a first dropping means (DM) for dropping data" or the claimed interface means or the claimed interface means that comprises a dropping means. For example, EP02079196 does not describe any structure that performs the function of "dropping data exchanged by said first and second module (M, S)." As such, the Asserted Claims of the '818 patent are entitled to a priority date no earlier than July 4, 2003, when the PCT application was filed.[1]

B. U.S. Patent No. 7,373,449

In its Infringement Contentions, NST asserts that the Asserted Claims of the '449 patent are entitled to claim priority from EP02079196, filed on October 8, 2002. Defendants dispute that the Asserted Claims of the '449 patent are entitled to claim priority from EP020791196 because, among other things, EP020791196 does not disclose the claimed "connection manager"

[1] Defendants reserve the right to argue that the Asserted Claims of the '818 patent are invalid under 35 U.S.C. § 112, as discussed in Section VI.

or the claimed "resource manager." As such, the Asserted Claims of the '449 patent are entitled to a priority date no earlier than October 7, 2003, when the PCT application was filed.[2]

C. U.S. Patent No. 7,594,052

In its Infringement Contentions, NST asserts that the Asserted Claims of the '052 patent are entitled to claim priority from EP04101095, filed on March 17, 2004. NST has provided no evidence to support its contentions that the Asserted Claims are entitled to claim priority back to this date, and Defendants therefore reserve the right to argue that a later priority date is appropriate based on any findings as to the priority date of the Asserted Claims by the Court, information learned through discovery, or otherwise. Should NST fail to establish that any Asserted Claim is entitled to the above priority date or should NST improperly later assert a different invention or priority date, Defendants reserve the right to add additional prior art references to these Invalidity Contentions.

D. U.S. Patent No. 7,769,893

In its Infringement Contentions, NST asserts that the Asserted Claims of the '9893 patent are entitled to priority from EP02079196, filed on October 8, 2002. Defendants dispute that the Asserted Claims of the '9893 patent are entitled to claim priority from EP02079196 because, among other things, EP02079196 does not disclose at least the claimed "first information indicative of a location of an addressed message receiving module S within the network [that] is comprised of (1) a connection identifier identifying two or more message receiving modules S and (2) an identifier of a passive network interface means associated with the addressed message

[2] Defendants reserve the right to argue that the Asserted Claims of the '449 patent are invalid under 35 U.S.C. § 112, as discussed in Section VI.

receiving module S" or "address translation unit." As such, the Asserted Claims of the '9893 patent are entitled to a priority date no earlier than July 4, 2003, when the PCT application was filed.[3]

E. U.S. Patent No. 8,072,893

In its Infringement Contentions, NST asserts that the Asserted Claims of the '2893 patent are entitled to claim priority from EP05103232, filed on April 21, 2005. NST has provided no evidence to support its contentions that the Asserted Claims are entitled to claim priority back to this date, and Defendants therefore reserve the right to argue that a later priority date is appropriate based on any findings as to the priority date of the Asserted Claims by the Court, information learned through discovery, or otherwise. Should NST fail to establish that any Asserted Claim is entitled to the above priority date or should NST improperly later assert a different invention or priority date, Defendants reserve the right to add additional prior art references to these Invalidity Contentions.[4]

F. U.S. Patent No. 8,086,800

In its infringement contentions, NST asserts that the Asserted Claims of the '800 patent and are entitled to claim priority from EP04102189, filed on May 18, 2004. NST has provided no evidence to support its contentions that the Asserted Claims are entitled to claim priority back to this date, and Defendants therefore reserve the right to argue that a later priority date is appropriate based on any findings as to the priority date of the Asserted Claims by the Court, information learned through discovery, or otherwise. Should NST fail to establish that any

[3] Defendants reserve the right to argue that the Asserted Claims of the '449 patent are invalid under 35 U.S.C. § 112, as discussed in Section VI.
[4] Defendants reserve the right to argue that the Asserted Claims of the '2893 patent are invalid under 35 U.S.C. § 112, as discussed in Section VI.

Asserted Claim is entitled to the above priority date or should NST improperly later assert a different invention or priority date, Defendants reserve the right to add additional prior art references to these Invalidity Contentions.

IV. STATE OF THE ART

This section describes the general state of the art surrounding the claimed inventions at the time of the alleged invention and identifies a number of prior art references providing additional background, detail, and context, on which Defendants may rely. Defendants set forth additional description and summary of the state of the art for each of the Asserted Patents in the Sections regarding the Disclosures of the Asserted Patents below. Defendants also intend to rely on each of the prior art references discussed below and in exhibits to these invalidity contentions for purposes of demonstrating the state of the art for the Asserted Patents. Defendants also reserve the right to rely on the discussions of the state of the art and prior art in each of the Asserted Patents and their file histories including explanations of the state of the art and the correspondence of prior art references with the claims of the Asserted Patents. Defendants further expressly reserve the right to supplement their summary of the state of the art, including for example, by information from any of the authors or named inventors on any of the prior art references, by personnel familiar with systems based on any of the prior art, or by technical experts retained on behalf of any party.

Since the middle of the 1990s, System-on-chip (SoC) designs have provided integrated solutions to challenging design problems in the telecommunication, multimedia, and consumer electronics domains. The progress in these fields has been made possible by the circuit designers' ability to integrate complex designs with a broad array of functionality on a single integrated chip under tight time-to-market constraints. A major goal of SoC design is to provide

correct and reliable operation of interacting components on a single chip. Success of the SoC designs depended upon using appropriate design and process methodologies, as well as ability to interconnect existing components, including processors, controllers, and memories, reliably. Before the alleged conception of the alleged inventions described and claimed in the Asserted Patent, numerous researchers from the field of design of integrated circuits had recognized the potential benefits and solved the challenges of interconnecting components on a SoC using a network by leveraging known techniques from the field of computer networking and from the field of multiprocessor computers based on the principles of networking and multiprocessor design. Selected publications disclosing the above trends are listed below:

- L. Benini and G. De Micheli, *Networks on Chips: A New SoC Paradigm*, IEEE 2002 ("Benini")
- S. Kumar et al., *A Network on Chip Architecture and Design Methodology*, 2001 ("Kumar")
- W. Dally and B. Towles, *Route Packets, Not Wires: On-Chip Interconnection Networks*, June 2001 ("Dally")
- P. Guerrier & A. Greiner, *A Generic Architecture for On-Chip Packet-Switched Interconnections*, 2000 ("Guerrier")
- K. Goossens et al., *Networks on Silicon: Combining Best-Effort and Guaranteed Services*, 2002 ("2002 Goossens")
- D. Wingard & Kurosawa, *Integration Architecture for System-on-a-Chip Design*, 1998 ("Wingard & Kurosawa")

For example, in a paper entitled *Networks on Chips: A New SoC Paradigm*, Benini & De Micheli recommended borrowing techniques from the field of networking: "Network engineers have

already gained experience with using stochastic techniques and models for large-scale designs. We propose borrowing models, techniques, and tools from the network design field and applying them to SoC design." Benini at 71. The authors further noted that "[o]n-chip networks relate closely to interconnection networks for high-performance parallel computers with multiple processors, in which each processor is an individual chip. Like multiprocessor interconnection networks, nodes are physically close to each other and have high link reliability. Further, developers have traditionally designed multiprocessor interconnections under stringent bandwidth and latency constraints to support effective parallelization. Similar constraints will drive micronetwork design." *Id.* at 72. Notably, mere integration or reduction in size of a device is not patentable. *Pacifica Technica Corp. v. United States*, 11 Cl. Ct. 393, 414 (1986) ("It is well established that merely changing the size of a device is not an invention."), *aff'd in part, vacated on other grounds*, 835 F.2d 871 (Fed. Cir. 1987); *cf. Tex. Instruments v. U.S. Int'l Trade Comm'n*, 805 F. 2d 1558, 1570 (Fed. Cir. 1986) ("A mere change in size [of electronic components] due to improved miniaturization by technological advance does not in itself save the accused devices from infringement[.]").

Similarly, in a paper entitled *A Network on Chip Architecture and Design Methodology* regarding architecture and design of a network on a chip, S. Kumar et al. noted that their platform leveraged the techniques of networking: "We propose a packet switched platform for single chip systems which scales well to an arbitrary number of processor like resources. The platform, which we call Network-on-Chip (NOC), includes both the architecture and the design methodology." Kumar at Abstract. When summarizing related work and the industry trends, the author noted that the designer of SoCs was relying upon networking principles: "Many architectural templates have been proposed for hardware platforms for future SoCs. There is a

general emphasis on providing efficient and standardized communication infrastructure for connecting multiple resources on the chip [11, 8, 9]. There is a trend to adapt layered approach of OSI reference model towards on Chip communication [12, 10, 13].” Kumar at 2.

In a paper entitled *A Generic Architecture for On-Chip Packet-Switched Interconnections*, P. Guerrier and A. Grenier noted the origins of their research in networking and parallel computing domains: “This paper presents an architectural study of a scalable system-level interconnection template. . . We present an alternative interconnection in the form of switching networks. This technology originates in parallel computing, but is also well suited for heterogeneous communication between embedded processors and addresses many of the deep submicron integration issues.” Guerrier at Abstract.

In their paper entitled *Route Packets, Not Wires: On-Chip Interconnection Networks*, advocating a new paradigm for On-Chip interconnection networks, W. Dally & B. Towles noted that “[u]sing a network to replace global wiring has advantages of structure, performance, and modularity.” Dally at 684.

Finally, one of the inventors of several of the Asserted Patents noted that their design borrowed principles from the networking domain. A paper, entitled *Networks on Silicon: Combining Best-Effort and Guaranteed Services* and authored by K. Goossens et al., proposed a design based on packet switching and circuit switching techniques. Their design which embodied the alleged inventions of the Asserted Patent was referred to as the ÆTHEREAL NOS (network on silicon). At the time of the publication of the paper, the authors noted that the ÆTHEREAL NOS “intends to support both guaranteed and best-efforts services. . . We use a combination of circuit and packet switching, in the spirit of ATM [1].” 2002 Goossens at 425. The authors

specifically referenced the *ATM User-Network Interface Specification* that was published by the ATM Forum in 1994.

Mirroring the above, the background sections of the Asserted Patent mention that the inventors rely upon the principles from the domain of computer networks.

Certain networking concepts were well known at the time of the purported invention. For example, it was known for networks to implement Quality of Service (QoS) guarantees. *See, e.g.*, Andrew Campbell, et al., *A Quality of Service Architecture*, ACM SIGCOMM Computer Communication Review, Volume 24 Issue 2 (April 1994) ("Campbell") at 6; Andrew S. Tanenbaum, *Computer Networks*, 3d Edition (1996) ("Tanenbaum") at 481-83. Various QoS parameters exist, such as connection establishment delay, connection establishment failure, throughput, transit delay, residual error ratio, protection, priority, and resilience. Tanenbaum at 482-83. "The QoS parameters are specified by the transport user when a connection is requested. Both the desired and minimum acceptable values can be given. In some cases, upon seeing the QoS parameters, the transport payer may immediately realize that some of them are unachievable…." Tanenbaum at 483. Further, various network designs and topologies were well known in the art. For example, J. Duato et al., *Interconnection Networks an Engineering Approach*, 1997 ("Duato") taught, among other things, various switching techniques, including circuit switching and packet switching. Duato at 40-60.

V. INVALIDITY UNDER 35 U.S.C. §§ 102 AND 103

Defendants contend that each Asserted Claim of the Asserted Patents is invalid as anticipated by the prior art under various subsections of 35 U.S.C. § 102[5] and/or as obvious in

[5] Based on Plaintiff's contentions of the priority dates of the Asserted Claims, Defendants apply pre-AIA subsections 102(a), 102(b), 102(e), and 102(g), and post-AIA subsections 102(a)(1) and 102(a)(2), but to the extent other versions (*e.g.*, pre- or post-AIA) regarding invalidity for

view of the prior art under 35 U.S.C. § 103. The charts attached to these invalidity contentions as Exhibits A–F set forth how prior art identified by Defendants anticipates either expressly or inherently, and/or renders obvious either alone or in combination with knowledge of a person of ordinary skill in the art and/or additional prior art references, each asserted claim. In addition, Defendants incorporate by reference invalidity contentions served in related litigations, including contentions served in *Network System Technologies, LLC v. Texas Instruments Inc. et al.*, No. 2:22-cv-00482 (E.D. Tex.) and *Network System Technologies, LLC v. Samsung Electronics Co. Ltd. et al.*, No. 2:22-cv-00481 (E.D. Tex.). Defendants reserve the right to rely on any information included in any such prior contentions not yet produced by Plaintiff. For invalidity pursuant to 35 U.S.C. §§ 102, 103, the parties' agreed upon scheduling recommendations solely require Defendants to provide "a chart setting forth where in the prior art references each element of the asserted claim(s) are found." In this document and the attached Exhibits, Defendants provide far more information, including information related to exemplary combinations of references and motivations to combine those references. Defendants provide this exemplary additional information solely for illustrative purposes. By setting forth this information, Defendants are not suggesting those are the only combinations that they may rely on to prove the claims of the patents-in-suit are invalid, nor are they attempting to identify all the motivations a POSA may have had to combine or modify these references in a way that would render the claimed invention obvious.

In the charts, Defendants cite various relevant portions of the identified prior art references, but other portions may contain additional or different support for a particular claim

anticipation or obviousness apply, Defendants' invalidity contentions and analysis apply just the same.

limitation, and thus may additionally anticipate, either expressly or inherently, and/or render obvious, one or more of the asserted claims. Persons of ordinary skill in the art at the time of the filing of the asserted patents knew to read references as a whole, and in the context of other publications and literature and the general knowledge in the field.

For each Asserted Patent, the Exhibits also contain an omnibus reference chart identifying each reference that teaches a given limitation. Defendants reserve the right to combine each anticipating reference and/or obviousness combination disclosed herein with one or more references as disclosed in the omnibus chart. Specifically, if any anticipating reference or obviousness combination identified in these contentions is alleged or found to lack sufficient disclosure to anticipate or render obvious an element or limitation recited in an asserted claim, further disclosure supporting the obviousness of that element or limitation is identified in the omnibus chart. Defendants also reserve the right to rely on the omnibus chart and the multiplicity of prior art disclosures of the same element or limitation as evidence that the limitation was well-known and obvious to a person of ordinary skill in the art.

Defendants also reserve the right to rely on other references disclosed or incorporated by reference in these Invalidity Contentions, in prior art references identified or charted in these contentions, in the Asserted Patents, any patents or applications related to the Asserted Patents, in the file history of the Asserted Patents or any related patents or applications, in any related litigation, and in the attached Exhibits.

Defendants further expect to rely on any products that Plaintiff accuses of infringing the patents-in-suit in its infringement contentions, including for example MSM6000, MSM6025, MSM6050, MSM6100, MSM6150, MSM6275, MSM6280, MSM6500, MSM6550, MSM6800, and MSM7500 which were designed and produced before the earliest priority dates of the

patents-in-suit, that show that the alleged invention was (1) known or used by others in this country, (2) described in a printed publication in this or a foreign country, (3) was not invented by the named inventors of the patents-in-suit, or (4) previously invented by another. For this purpose only, Defendants hereby incorporate Plaintiff's infringement claim charts which Plaintiff alleges establish how these products meet each of the limitations of the asserted claims of the patents-in-suit. Documents providing evidence that these products are prior art pursuant to pre-AIA 35 U.S.C. 102 and showing how these products worked are being contemporaneously produced as QNST_0000001 – QNST_0229277, and source code providing this evidence is being produced pursuant to the Protective Order.

Defendants also reserve the right to rely on all of the prior art cited and all grounds disclosed during the prosecution of each of the Asserted Patents, their family members, or foreign counterparts, either during initial prosecution or during subsequent post grant proceedings, and all arguments made by Patentee during such proceedings.

Defendants' claim charts may disclose multiple theories of invalidity in a single chart. Each chart directed to an anticipatory product/system may also describe that the product/system alone, in light of the knowledge and skill in the art, or in light of one or more other prior art references, rendering each Asserted Claim obvious.

Where Defendants cite to a particular figure in a prior art reference, the citation should be understood to encompass the caption and description of the figure as well as any text relating to the figure in addition to the figure itself. Conversely, where a cited portion of text refers to a figure, the citation should be understood to include the figure as well. Furthermore, while Defendants have generally identified at least one citation per limitation present in a reference or

combination, every disclosure of the same or similar limitation in the same reference or combination is not necessarily identified. To focus the issues, Defendants cite particularly pertinent portions of identified references, even where a reference or combination may contain additional support for a particular claim element. Thus, Defendants may rely on uncited portions of the prior art references for additional support or context, such as for elucidating how a POSITA would understand the cited portions of the reference disclose a particular element, in view of what the prior art reference discloses as a whole. Defendants may rely upon other prior art identified in future supplements, corroborating references, documentation, source code, products, and testimony, including materials obtained through further investigation and third-party discovery of the prior art identified herein, that demonstrates the invalidating functionality identified in these Invalidity Contentions or that show the state of the art in the relevant time period (irrespective of whether such references themselves qualify as prior art to the Asserted Patent), and expert testimony to provide context to or aid in understanding the cited portions of the identified prior art. Similarly, where there are multiple references relating to a single prior art product or system, Defendants may cite only to a single reference for a particular limitation, even though other references may also contain similar teachings. Thus, Defendants may rely on uncited references relating to a particular prior art document or system for additional support for a particular element. Any prior art disclosed as anticipating a limitation also renders that limitation obvious.

Additionally, persons of ordinary skill in the art at the time of the alleged inventions generally read a prior art reference as a whole and in the context of other publications and literature. Numerous prior art references, including those identified herein and in the attached exhibits, reflect common knowledge and the state, scope, and content of the prior art before the

priority date of the Asserted Claims of the Asserted Patents. Defendants may rely on uncited portions of the prior art references and on other publications and expert testimony to provide context and as aids to understanding and interpreting the portions that are cited.

In general, a claimed invention is invalid due to obviousness "if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art." 35 U.S.C. § 103; *Graham v. John Deere Co.*, 383 U.S. 1, 13-14 (1966). The ultimate determination of whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: "(1) the scope and content of the prior art; (2) the differences between the prior art and the claims; (3) the level of ordinary skill in the art at the time of invention; and (4) objective evidence of nonobviousness." *Miles Labs., Inc. v. Shandon, Inc.*, 997 F.2d 870, 877 (Fed. Cir. 1993); *see Graham*, 383 U.S. at 17-18.

To the extent that any claim limitation is not anticipated pursuant to 35 U.S.C. § 102, Defendants contend that any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged inventions, in view of the state of the art and knowledge of those skilled in the art under 35 U.S.C. § 103. Each Asserted Claim would have been obvious in view of each reference cited in the attached Exhibits either alone or combined with the knowledge that was possessed by one of ordinary skill in the art. Additionally, each Asserted Claim would have been obvious to one of ordinary skill in the art in view of the combination of any one of the prior art references identified in the attached Exhibits with one or more of the other references identified or discussed in the same Exhibits. Defendants reserve the right to illustrate the knowledge of one of ordinary skill in the art using

any of the prior art references identified throughout these Invalidity Contentions, expert testimony, learned treatises, and/or testimony of prior art fact witnesses.

Statements made by the Applicants in the specification and/or during prosecution of the Asserted Patents and any related patents/applications, such as in the "Background of the Invention" section that describes the related art known to the Applicants, are admissions that can be relied upon for both anticipation and obviousness determinations, regardless of whether the admitted prior art would otherwise qualify as prior art under the statutory categories set forth in 35 U.S.C. § 102. *See* MPEP §§ 2129 and 608.01(c). To the extent Plaintiff contends that the Asserted Claims are not invalid as anticipated by and/or obvious in view of the prior art under 35 U.S.C. §§ 102 and 103, Defendants reserve the right to rely on Applicants' "Admitted Prior Art" to demonstrate the invalidity of the Asserted Claims.

Under *KSR Int'l v. Teleflex Co.*, a motivation to combine prior art references is not necessarily required to show obviousness under 35 U.S.C. § 103. 550 U.S. 398 (2007). Nonetheless, one of ordinary skill in the art at the time of the invention would have been motivated and had a reasonable expectation of success to make one or more combinations of the prior art references cited in Exhibits A-F. In particular, those of ordinary skill in the art at the time of the alleged inventions of the Asserted Patents would have been motivated to modify or combine the prior art references because, for example: (a) the references in general deal with the same or related subject matter; (b) one of ordinary skill in the art would have been motivated by the problem that the inventor was attempting to solve, or with other problems that would have been faced in reaching a solution, and would have looked to references that concerned similar issues or taught how to overcome the problems faced; (c) the combinations were obvious to try and would have operated in their known and expected way; (d) the combinations were within the

technical skill and understanding of a person of ordinary skill in the art; (e) the combinations would have been motivated by the developments in technology; and (f) the combinations reflect various design choices that would have been known to one of ordinary skill in the art and within that person's technical capability to implement (i.e., technically feasible).

The various motivations described above provide a basis for combining or modifying references, as detailed below, to render each of the Asserted Claims obvious. In addition, the Court can consider the inferences and creative steps a person of ordinary skill in the art would employ in making such combinations. *See KSR*, 127 S. Ct. at 1741 ("a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ").

Additional motivations to combine references may be found in the discussion of the state of the art, above, and in the discussion of invalidity with respect to each Asserted Patent, below. If, and to the extent, Plaintiff challenges the correspondence of the references in the Exhibits with respect to particular limitations of the Asserted Claims of the Asserted Patents, Defendants reserve the right to supplement these Invalidity Contentions to identify additional combinations, motivations to modify, or explanations for particular references with additional particularity.

Additionally, Defendants believe that certain non-parties and current or former employees thereof may have possession of relevant information and/or documents constituting prior art to the Asserted Patents, including parties in related litigations. Defendants are continuing the investigation into these and other companies and their products. Defendants reserve the right to supplement these Invalidity Contentions to identify additional references, combinations, motivations to modify, or explanations for particular references based on any information and/or documents provided by the former employees and/or successors-in-interests of companies or individuals who may possess relevant information and/or documents

constituting prior art to the Asserted Patents. The concepts disclosed and claimed in each of the Asserted Patents are not new, and had been disclosed, used, offered for sale, sold, and practiced by others prior to the claimed priority date of the patents. The prior art identified herein and in the Exhibits, individually or in combination, invalidates the Asserted Claims under 35 U.S.C. §§ 102 (a), (b), (e), (g) and §103. Because discovery is ongoing, Defendants expect to gather additional information about the identified prior art, and other prior art, through third-party discovery or other discovery, and will thus amend and supplement these Invalidity Contentions once they obtain that discovery and have meaningful and reasonable time to analyze it. As described in more detail below, claims of the Asserted Patents are also invalid under 35 U.S.C. §§ 101 and 112.

Moreover, Defendants reserve the right to rely on inventor admissions concerning the scope of the prior art relevant to the Asserted Patents found in, *inter alia*, the prosecution histories of the Asserted Patents or related patents and/or patent applications, any testimony or declarations of the named inventors concerning the Asserted Patents or related patents, and any papers or evidence submitted by Plaintiff in connection with this litigation, any other pending or future litigation brought by Plaintiff involving the Asserted Patents or related patents, or *inter partes* review proceedings involving the Asserted Patents or related patents. Defendants also may establish what was known to a person having ordinary skill in the art through references discussed above in connection with the state of the art and treatises, published industry standards, other publications, products, and/or testimony.

A. Disclosures For U.S. Patent No. 7,366,818

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits A-1 to A-16 demonstrate where each limitation of the claims is found, either expressly or inherently in the larger context of the passage, or rendered obvious by, certain of the references listed below, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a) Prior Art Patents, Patent Publications, and Non-Patent Publications to the Asserted Claims of the '818 patent.

Chart	Reference	Filing Date	Date of Issue or Publication	Citation	Claims
A-1	U.S. 7,039,750	July 23, 2001	May 2, 2006	Regula	Anticipated: 1–3, 5–7 Obvious: 1–3, 5–7
A-2	U.S. 6,490,630	May 8, 1998	Dec. 3, 2002	Poon	Obvious: 1–2
A-3	R. Bhoedjang et al., *User-Level Network Interface Protocols*		Nov. 1998	Bhoedjang	Obvious: 1–3, 5–7
A-4	U.S. 6,885,638	Jun. 13, 2002	April 26, 2005	Xu	Obvious: 1–3, 5–7
A-5	K. Goossens, et al., *Networks on Silicon: Combining Best-Effort and Guaranteed Services*		March 2002	2002 Goossens	Obvious: 1–2
A-6	U.S. 7,200,137	July 29, 2002	Apr. 3, 2007	Dorr	Obvious: 1–3, 5–7
A-7	H. Tezuka, et al., *PM: An Operating System Coordinated High Performance Communication Library*		December 1997	Tezuka	Obvious: 1–3, 5–7
A-8	CoreConnect		1999	CoreConnect	Anticipated: 1–3, 5–7

					Obvious: 1–3, 5–7
A-9	Timothy Callahan et al., *NIFDY: A Low Overhead, High Throughput Network Interface*		1995	Callahan	Obvious: 1–3, 5–7
A-10	Shubhendu S. Mukherjee et al., *A Survey of User-Level Network Interfaces for System Area Networks*		1997	Mukherjee	Obvious: 1–3, 5–7
A-11	Jae H. Kim et al., *Compressionless Routing: A Framework for Adaptive and Fault-Tolerant Routing*		1997	Kim	Obvious: 1–3, 5–7
A-12	U.S. 6,480,489	Mar. 1, 1999	Nov. 12, 2002	Muller	Obvious: 1–3, 5–7
A-13	U.S. Pat. Pub. No. 2001/0042147	Dec. 5, 2000	Nov. 15, 2001	Adams	Anticipated: 1–3, 5–7 Obvious: 1–3, 5–7
A-14	Andrew S. Tanenbaum, *Computer Networks, Third Edition*		1996	Tanenbaum	Obvious: 1–3, 5–7
A-15	William J. Dally, et al., *Router Packets, Not Wires: On-Chip Interconnection Networks*		June 2001	Dally	Obvious: 1-3, 5-7
A-16	Erland Nilsson, *Design and Implementation of a hot-potato Switch in a Network on Chip*		June 17, 2002	Nilsson	Anticipated: 1–2 Obvious: 1–2

b) Prior Art Systems/Services To The Asserted Claims of the ’818 patent.

Defendants further identify the commercial embodiments of the inventions described in Exhibits A-1 to A-16, to the extent those systems or services were on sale or in public use before the priority date of the ’818 patent. Moreover, on information and belief, IBM and other

companies sold, offered for sale, and/or publicly used products incorporating IBM's CoreConnect architecture ("CoreConnect") that constitutes prior art to the '818 patent. Chart A-8 demonstrates where each limitation of the claims is found in the CoreConnect architecture.

2. Obviousness Combinations

A person having ordinary skill in the art would have been motivated to modify or combine the references described in attached Exhibits A-1 to A-16 with knowledge of a person of ordinary skill in the art and/or as listed below, or further as shown in the exemplary omnibus reference chart A-17, and for the reasons described below.

Reference	In Combination With	Claims
Regula	AAPA	1–3, 5–7
	Xu	1–3, 5–7
	Muller	1–3, 5–7
	Kim	1–3, 5–7
	Tanenbaum	1–3, 5–7
	Dally	1-3, 5-7
Poon	AAPA	1–2
	Regula	1–3, 5–7
	2002 Goossens	1–2
	Nilsson	1–2
	Dorr	1–3, 5–7
	Xu	1–3, 5–7
	Bhoedjang	1–3, 5–7
	Tezuka	1–3, 5–7
	Muller	1–3, 5–7
	Kim	1–3, 5–7
	Mukherjee	1–3, 5–7
	Adams	1–3, 5–7
	Callahan	1–3, 5–7
	Tanenbaum	1–3, 5–7
	Dally	1-3, 5-7
	AAPA/Dally and Bhoedjang	1–3, 5–7
	AAPA/Dally and Tezuka	1–3, 5–7
	AAPA/Dally and Xu	1–3, 5–7
	AAPA/Dally and Bhoedjang and Xu	1–3, 5–7
	AAPA/Dally and Muller	1–3, 5–7
	AAPA/Dally and Bhoedjang and Muller	1–3, 5–7
	AAPA/Dally and Tezuka and Muller	1–3, 5–7
	2002 Goossens and Tezuka	1–3, 5–7
	2002 Goossens and Xu	1–3, 5–7

	2002 Goossens and Bhoedjang and Xu	1–3, 5–7
	2002 Goossens and Tezuka and Xu	1–3, 5–7
	2002 Goossens and Muller	1–3, 5–7
	2002 Goossens and Bhoedjang and Muller	1–3, 5–7
	2002 Goossens and Tezuka and Muller	1–3, 5–7
	Dorr and Xu	1–3, 5–7
	Dorr and Bhoedjang and Xu	1–3, 5–7
	Dorr and Tezuka and Xu	1–3, 5–7
	Dorr and Muller	1–3, 5–7
	Dorr and Bhoedjang and Muller	1–3, 5–7
	Dorr and Tezuka and Muller	1–3, 5–7
Bhoedjang	AAPA	1–3, 5–7
	Regula	1–3, 5–7
	2002 Goossens	1–3, 5–7
	Nilsson	1–3, 5–7
	Adams	1–3, 5–7
	Xu	1–3, 5–7
	Muller	1–3, 5–7
	Dally	1-3, 5-7
	AAPA/Dally and Xu	1–3, 5–7
	2002 Goossens and Xu	1–3, 5–7
	Regula and Xu	1–3, 5–7
	Dorr and Xu	1–3, 5–7
	AAPA/Dally and Muller	1–3, 5–7
	2002 Goossens and Muller	1–3, 5–7
	Regula and Muller	1–3, 5–7
	Dorr and Muller	1–3, 5–7
Tezuka	AAPA	1–3, 5–7
	Regula	1–3, 5–7
	2002 Goossens	1–3, 5–7
	Nilsson	1–3, 5–7
	Xu	1–3, 5–7
	Muller	1–3, 5–7
	Dally	1-3, 5-7
	AAPA/Dally and Xu	1–3, 5–7
	2002 Goossens and Xu	1–3, 5–7
	Regula and Xu	1–3, 5–7
	Adams and Xu	1–3, 5–7
	AAPA/Dally and Muller	1–3, 5–7
	2002 Goossens and Muller	1–3, 5–7
	Regula and Muller	1–3, 5–7
	Adams and Muller	1–3, 5–7
Dorr	AAPA	1–3, 5–7
	Xu	1–3, 5–7
	Bhoedjang	1–3, 5–7
	Tezuka	1–3, 5–7
	Muller	1–3, 5–7

	Kim	1–3, 5–7
	Mukherjee	1–3, 5–7
	Callahan	1–3, 5–7
	Tanenbaum	1–3, 5–7
	Dally	1-3, 5-7
CoreConnect	AAPA	1–3, 5–7
	Regula	1–3, 5–7
	2002 Goossens	1–3, 5–7
	Nilsson	1–3, 5–7
	Adams	1–3, 5–7
	Xu	1–3, 5–7
	Bhoedjang	1–3, 5–7
	Tezuka	1–3, 5–7
	Muller	1–3, 5–7
	Kim	1–3, 5–7
	Mukherjee	1–3, 5–7
	Callahan	1–3, 5–7
	Tanenbaum	1–3, 5–7
	Dally	1-3, 5-7
Adams	AAPA	1–3, 5–7
	Xu	1–3, 5–7
	Muller	1–3, 5–7
	Kim	1–3, 5–7
	Tanenbaum	1–3, 5–7
	Dally	1-3, 5-7
2002 Goossens	Bhoedjang	1–3, 5–7
	Tezuka	1–3, 5–7
	Poon	1–3, 5–7
	Dally	1–3, 5–7
	Bhoedjang and Xu	1–3, 5–7
	Bhoedjang and Muller	1–3, 5–7
	Poon and Xu	1–3, 5–7
	Poon and Muller	1–3, 5–7
	Tezuka and Xu	1–3, 5–7
	Tezuka and Muller	1–3, 5–7
Nilsson	Bhoedjang	1–3, 5–7
	Tezuka	1–3, 5–7
	Xu	1–3, 5–7
	Muller	1–3, 5–7
	Poon	1–3, 5–7
	Dally	1–3, 5–7
	Dorr	1–3, 5–7
	Mukherjee	1–3, 5–7
	Bhoedjang and Xu	1–3, 5–7
	Bhoedjang and Muller	1–3, 5–7
	Poon and Xu	1–3, 5–7
	Poon and Muller	1–3, 5–7

	Tezuka and Xu Tezuka and Muller	1–3, 5–7 1–3, 5–7

A person having ordinary skill in the art at the time of filing of the ’818 patent would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them. It would have been obvious to a person of ordinary skill in the art at the time of the alleged invention to combine a reference with one or more of the other references for the following reasons:

- Combining the prior art limitations according to known methods would have yielded predictable results.
- Simple substitution of one known limitation for another would have yielded predictable results.
- Use of known technique to improve similar devices in the same way would have been obvious.
- Applying a known technique to a known device ready for improvement would have yielded predictable results.
- References disclosing these concepts teach the beneficial utility of them, including as cited in the claim charts submitted herewith.

In addition, a person of ordinary skill in the art would have been motivated to make the combinations based on the general industry trends and other considerations discussed in connection with the state of the art. For example, as explained above in Section IV that describes the state of the art prior to the alleged dates of alleged inventions in the Asserted Patents, the industry was moving towards using system-on-chips (SoCs). Mirroring the general trend of higher integration with time (e.g., Moore’s Law), SoCs were integrating greater number of

modules all on one chip. A person of skill in the art was aware of the need for interconnection networks to connect the modules on a single chip as well as traditionally connected modules on different chips. As further explained in Section IV, researchers were advocating the need to adopt principles and techniques from computer networking domains in the context of SoCs. A person of ordinary skill in the art would have been aware of such trends and suggestions to incorporate techniques from closely-related domains to address and overcome challenges in the SoC arena.

A person of ordinary skill in the art at the time of the alleged invention would have combined the references because each generally relates to similar technology. *See, e.g.*, Poon at Abstract, FIG. 1; Regula at Abstract, FIG. 1; Bhoedjang at 53; Tezuka at Abstract; Dorr at title, 3:56-67; Xu at 3:10-28, 3:65-4:8; Callahan at 230; Mukherjee at 1; Kim at 229; Muller at 1:48-52; Adams at [0002], [0011], [0012]; Tanenbaum at Title, 16; Nilsson at 9-10; ’818 patent at 1:16-5:13. A person of skill in the art also would have been motivated to combine references in order to obtain the benefits of one prior art device, system or method in another device, system or method. Moreover, to the extent the ’818 patent identifies any known need for improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, it would also have been obvious to a person of ordinary skill in the art to combine all the combinations listed above with the Applicant Admitted Prior Art (“AAPA”) of the ’818 patent. The ’818 patent admits that systems on silicon and networks on chip are prior art, and that there were known motivations to use a NoC instead of a bus. *See, e.g.*, ’818 patent at 1:16-50. For example, the ‘818 patent indicates that it was known that a NoC “resolve[s] the

electrical problems in new deep-submicron technologies, as they structure and manager global wires" and a NoC "share[s] wires, lowering their number and increasing their utilization". *Id. at* 1:39-44. The '818 patent also admits that it was known that NoCs are "energy efficient and reliable and are scalable compared to buses". *Id.* at 1:43-44. The '818 patent further admits that it was known that NoCs "decouple computation from communication, which is essential in managing the design of billion-transistor chips." *Id.* at 1:44-46. The '818 patent also admits that off-chip network technology is related and applicable to on-chip networks. *See, e.g.*, '818 patent at 1:62-67. In addition, the '818 patent admits that networks on chip are "reliable" and do not inadvertently drop packets. *See, e.g.*, '818 patent at 2:35–52. The '818 patent also admits that "transactions" comprising requests and responses were known in the art. *See, e.g.*, '818 patent at 3:63–4:17. To the extent the '818 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, the AAPA of the '818 patent would have provided additional motivation to combine the identified references according to the combinations listed above.

For example, Poon teaches a computer network having a plurality of nodes and an interconnect for connecting the plurality of nodes. *See, e.g.*, Poon at 4:16-25. In particular, Poon teaches that the nodes in the computer network can include a network interface that drops unreliable messages. *See, e.g.*, Poon at 6:25-39. It would have been obvious to combine Poon with Regula, 2002 Goossens, Nilsson, Dorr, or Adams, each of which teaches systems for communication in which plural components communicate using an on chip network. *See, e.g.*, Regula at 2:9-10; 4:8-9; 2002 Goossens at 423, 425; Nilsson at 9-10; Dorr at title, 3:56-67;

Adams at [0002], [0011], [0012]. A POSITA would have been motivated to make such a combination in order to make networks interconnecting the various components smaller, more reliable, and more efficient. On chip networks require less energy to transfer data between components and are highly reliable. *See* '818 patent at 1:37-50. In addition, it would have obvious to combine Poon and Regula, 2002 Goossens, Nilsson, or Dorr with Bhoedjang or Tezuka, both of which teach a network interface that drops a packet if buffer space is unavailable at the receiver, and further describe utilizing an ACK/NACK protocol that indicates the status of transmitted packets. *See, e.g.*, Bhoedjang at 55–56, 59; Tezuka at Abstract, 4-6. It would also have been obvious to combine the above references with Xu or Muller. Xu teaches network elements can include a selective packet dropping circuit. *See, e.g.,* Xu at 3:65-4:8. Muller teaches a system for randomly dropping a packet with intelligence that prevents certain types of packets from being dropped. Muller at 105:25-27, 105:65-66, 106:12-17. A POSITA would have been motivated to make such a combination in order to avoid dropping packets that would result in additional congestion in the network. The methods taught by Xu and Muller would yield predictable results and improve the performance in the same way.

As another example, Bhoedjang teaches a network interface protocol. *See, e.g.*, Bhoedjang at 53. In particular, Bhoedjang teaches a network interface that drops a packet if buffer space is unavailable at the receiver, and further describes utilizing an ACK/NACK protocol that indicates the status of transmitted packets. *See, e.g.*, Bhoedjang at 55–56, 59. It would have been obvious to combine Bhoedjang with Regula, 2002 Goossens, Nilsson, Dorr, or Adams, each of which teaches systems for communication in which plural components communicate using an on chip network. *See, e.g.*, Regula at 2:9-10; 4:8-9; 2002 Goossens at 423, 425; Nilsson at 9-10; Dorr at title, 3:56-67; Adams at [0002], [0011], [0012]. A POSITA would

have been motivated to make such a combination in order to make networks interconnecting the various components smaller, more reliable, and more efficient. On chip networks require less energy to transfer data between components and are highly reliable. *See* '818 patent at 1:37-50. It would also have been obvious to combine the above references with Xu or Muller. Xu teaches network elements can include a selective packet dropping circuit. *See, e.g.,* Xu at 3:65-4:8. Muller teaches a system for randomly dropping a packet with intelligence that prevents certain types of packets from being dropped. Muller at 105:25-27, 105:65-66, 106:12-17. A POSITA would have been motivated to make such a combination in order to avoid dropping packets that would result in additional congestion in the network. The methods taught by Xu and Muller would yield predictable results and improve the performance in the same way.

As another example, Tezuka teaches a network interface that drops a packet if buffer space is unavailable at the receiver, and further describes utilizing an ACK/NACK protocol that indicates the status of transmitted packets. *See, e.g.*, Tezuka at *Abstract*, 4-6. It would have been obvious to combine Tezuka with Regula, 2002 Goossens, Nilsson, Dorr, or Adams, each of which teaches systems for communication in which plural components communicate using an on chip network. *See, e.g.*, Regula at 2:9-10; 4:8-9; 2002 Goossens at 423, 425; Nilsson at 9-10; Dorr at title, 3:56-67; Adams at [0002], [0011], [0012]. A POSITA would have been motivated to make such a combination in order to make networks interconnecting the various components smaller, more reliable, and more efficient. On chip networks require less energy to transfer data between components and are highly reliable. *See* '818 patent at 1:37-50. It would also have been obvious to combine the above references with Xu or Muller. *See, e.g.,* Xu at 3:65-4:8. Muller teaches a system for randomly dropping a packet with intelligence that prevents certain types of packets from being dropped. Muller at 105:25-27, 105:65-66, 106:12-17. A POSITA would have

been motivated to make such a combination in order to avoid dropping packets that would result in additional congestion in the network. The methods taught by Xu and Muller would yield predictable results and improve the performance in the same way.

As another example, Regula teaches a system for communication on chip and further describes dropping data in the event of a stall or timeout at a receiver station. Regula at Abstract, 10:17–31. It would have obvious to combine Regula with Bhoedjang or Tezuka, both of which teach a network interface that drops a packet if buffer space is unavailable at the receiver, and further describe utilizing an ACK/NACK protocol that indicates the status of transmitted packets. *See, e.g.*, Bhoedjang at 55–56, 59; Tezuka at *Abstract*, 4-6. A POSITA would have been motivated to make such a combination in order to deal with congestion in the network. Congestion occurs when a network element is inundated with packets that it cannot handle. One known method for dealing with congestion is to drop or discard packets that are beyond the capability of the networking element (commonly referred to as load shedding). *See* Tanenbaum at 390. The use of such a method would yield predictable results and improve performance in the same way. It would also have been obvious to combine the above references with Xu or Muller. Xu teaches network elements can include a selective packet dropping circuit. *See, e.g.,* Xu at 3:65-4:8. Muller teaches a system for randomly dropping a packet with intelligence that prevents certain types of packets from being dropped. Muller at 105:25-27, 105:65-66, 106:12-17. A POSITA would have been motivated to make such a combination in order to avoid dropping packets that would result in additional congestion in the network. The methods taught by Xu and Muller would yield predictable results and improve the performance in the same way.

As another example, Adams teaches an on-chip interconnect architecture a system on chip and further describes removing a grant of the interconnect to an initiator in the event of a

timeout. Adams at [0011]-[0012], [0064]. It would have obvious to combine Adams with Bhoedjang or Tezuka, both of which teach a network interface that drop packets, and further describe utilizing an ACK/NACK protocol that indicates the status of transmitted packets. *See, e.g.*, Bhoedjang at 55–56, 59; Tezuka at *Abstract*, 4-6. A POSITA would have been motivated to make such a combination in order to deal with congestion in the network. Congestion occurs when a network element is inundated with packets that it cannot handle. One known method for dealing with congestion is to drop or discard packets that are beyond the capability of the networking element (commonly referred to as load shedding). *See* Tanenbaum at 390. The use of such a method would yield predictable results and improve performance in the same way. It would also have been obvious to combine the above references with Xu or Muller. Xu teaches network elements can include a selective packet dropping circuit. *See, e.g.,* Xu at 3:65-4:8. Muller teaches a system for randomly dropping a packet with intelligence that prevents certain types of packets from being dropped. Muller at 105:25-27, 105:65-66, 106:12-17. A POSITA would have been motivated to make such a combination in order to avoid dropping packets that would result in additional congestion in the network. The methods taught by Xu and Muller would yield predictable results and improve the performance in the same way.

As another example, 2002 Goossen teaches a network on silicon that implements communications between IP cores within a chip. 2002 Goossens at 1. It would have been obvious to combine 2002 Goossens with Bhoedjang, Tezuka, or Poon, which teach a network interfaces that drop packets. Bhoedjang at 55–56, 59; Tezuka at *Abstract*, 4-6; Poon at 6:25-39. A POSITA would have been motivated to make such a combination in order to deal with congestion in the network. Congestion occurs when a network element is inundated with packets that it cannot handle. One known method for dealing with congestion is to drop or discard

packets that are beyond the capability of the networking element (commonly referred to as load shedding). *See* Tanenbaum at 390. The use of such a method would yield predictable results and improve performance in the same way. Additionally, Bhoedjang and Tezuka further describe utilizing an ACK/NACK protocol that indicates the status of transmitted packets. *See, e.g.*, Bhoedjang at 55–56, 59; Tezuka at *Abstract*, 4-6. It would also have been obvious to combine the above references with Xu or Muller. Xu teaches network elements can include a selective packet dropping circuit. *See, e.g.,* Xu at 3:65-4:8. Muller teaches a system for randomly dropping a packet with intelligence that prevents certain types of packets from being dropped. Muller at 105:25-27, 105:65-66, 106:12-17. A POSITA would have been motivated to make such a combination in order to avoid dropping packets that would result in additional congestion in the network. The methods taught by Xu and Muller would yield predictable results and improve the performance in the same way.

As yet another example, Nilsson teaches a network on chip that implements communications between IP elements within a system on chip. Nilsson at 9-10. It would have been obvious to combine Nilsson with Bhoedjang, Tezuka, or Poon, which teach a network interfaces that drop packets. Bhoedjang at 55–56, 59; Tezuka at *Abstract*, 4-6; Poon at 6:25-39. A POSITA would have been motivated to make such a combination in order to deal with congestion in the network. Congestion occurs when a network element is inundated with packets that it cannot handle. One known method for dealing with congestion is to drop or discard packets that are beyond the capability of the networking element (commonly referred to as load shedding). *See* Tanenbaum at 390. The use of such a method would yield predictable results and improve performance in the same way. Additionally, Bhoedjang and Tezuka further describe utilizing an ACK/NACK protocol that indicates the status of transmitted packets. *See, e.g.*,

Bhoedjang at 55–56, 59; Tezuka at *Abstract*, 4-6. It would also have been obvious to combine the above references with Xu or Muller. Xu teaches network elements can include a selective packet dropping circuit. *See, e.g.,* Xu at 3:65-4:8. Muller teaches a system for randomly dropping a packet with intelligence that prevents certain types of packets from being dropped. Muller at 105:25-27, 105:65-66, 106:12-17. A POSITA would have been motivated to make such a combination in order to avoid dropping packets that would result in additional congestion in the network. The methods taught by Xu and Muller would yield predictable results and improve the performance in the same way.

It would have been obvious to combine Dorr with one of the following: Xu, Bhoedjang, Tezuka, and Muller. Like Dorr, Bhoedjang teaches a network interface protocol. *See, e.g.*, Bhoedjang at 53. In particular, Bhoedjang teaches that the network interface drops a packet if the host buffer is not available. *See, e.g.*, Bhoedjang at pp. 55. Tezuka teaches a network interface unit that drops packets when the buffers at the interface overflow and discloses an ACK/NACK protocol. *See, e.g.,* Tezuka at *Abstract*, 4-6. Xu teaches a wireless communication system having a wireless unit and one or more network elements. *See, e.g.,* Xu at 3:10-28. In particular, Xu teaches that the network elements can include a selective packet dropping circuit. *See, e.g.,* Xu at 3:65-4:8. Muller teaches a network interface that drops packets when a network interface is already storing a maximum number of packets. Muller at 105:21-33. A POSITA would have been motivated to make such a combination in order to deal with congestion in the network. Congestion occurs when a network element is inundated with packets that it cannot handle. One known method for dealing with congestion is to drop or discard packets that are beyond the capability of the networking element (commonly referred to as load shedding). *See* Tanenbaum

at 390. The use of such a method would yield predictable results and improve performance in the same way.

It would also have been obvious to modify any of the references to replace any of their interconnects with a NoC based on the AAPA or Dally. In particular, the AAPA admits that NoCs were known and that there were known motivations to use a NoC for an interconnect in place of a bus. *See,* '818 patent at 1:16-50. Dally also indicates that networks on chip are generally preferable to a bus because they have higher bandwidth and support multiple concurrent communications. *See,* Dally at pp. 1.

It would also have been obvious to modify any of the references to combine discrete components together into a single integrated circuit ("IC") in the form of a system-on-chip ("SoC"). In particular, the text entitled *Modern VLSI Design: System-on-Chip Design, Third Edition* by Wayne Wolf explains that at the time of the patent, it was known that integrating discrete components onto an integrated circuit allowed designers "to build systems with many more transistors, allowing much more computing power to be applied to solving a problem." W. Wolf, *Modern VLSI Design: System-on-Chip Design, Third Edition*, Prentice Hall 2002 ("Wolf") at 1. Wolf teaches that integrated circuits are "much easier to design and manufacture and are more reliable than discrete systems," and that the small sizes of integrated circuits "leads to advantages in speed and power consumption, since smaller components have smaller parasitic resistances, capacitances, and inductances." *Id.* at 2. Wolf further explains, "Communication within a chip can occur hundreds of times faster than communication between chips on a printed circuit board" because on-chip circuits are smaller, and "smaller components and wires have smaller parasitic capacitances to slow down the signal." *Id.* Wolf notes that the small size of a device is "often an advantage in itself," and that replacing discrete components with a single chip

reduces power consumption, which has ripple effects on the rest of the system. *Id*. at 3. For example, with reduced power consumption, a smaller and cheaper power supply can be used. *Id*. Lower power consumption means less heat, so a fan may no longer be necessary. *Id*. Finally, Wolf explains that reducing the number of components, power supply requirements, and so on will "inevitably reduce system cost." *Id*. Indeed, as Wolf explains, many motivations exist to combine discrete components together to form a single IC.

The Applicant's Admitted Prior Art (AAPA) in the '818 patent also confirms that SoCs were previously known, and that it was known to combine discrete components together into a single IC in the form of an SoC, and thus the AAPA in the patent confirms it would have been obvious to modify any of the references to combine discrete components together into a single IC in the form of a SoC. Specifically, the Applicant for the '818 patent explained that the alleged invention arose out of "a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions" in ICs and by "the increasing density with which components can be integrated on an integrated circuit." '818 patent at 1:16-20.

The combinations of references provided are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendants may rely on such combination(s) in this litigation. In particular, Defendants are currently unaware of Plaintiff's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendants are also unaware of the extent, if any, to which Plaintiff may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendants as anticipatory, and the extent to which Plaintiff will contend that elements not disclosed in the asserted patent specifications would have

been known to persons of skill in the art. And Defendants do not yet know how the Court will construe terms in the asserted claims. Defendants are also continuing its investigation of the universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Plaintiff may also be in possession of prior art that Defendants may receive as discovery progresses in this case. Defendants reserve the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

B. Disclosures For U.S. Patent No. 7,373,449

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits B-1 to B-15 demonstrate where each limitation of the claims is found in, either expressly or inherently in the larger context of the passage, or rendered obvious by, certain of the references listed below, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a) Prior Art Patents, Patent Publications, and Non-Patent Publications to the Asserted Claims of the '449 patent.

Chart	Reference	Filing Date	Date of Issue or Publication	Citation	Claims
B-1	U.S. 7,200,137	July 29, 2002	Apr. 3, 2007	Dorr	Anticipated: 10-16 Obvious: 10-16
B-2	U.S. Pub. No. 2002/0129173	Mar. 9, 2001	Sept. 12, 2002	Weber	Anticipated: 10-16 Obvious: 10-16

B-3	S. Tan, et al., *QoS-based Connection Set-up in ATM Networks*		Sept. 5, 2000	Tan 2000	Obvious: 10-16
B-4	A. Campbell, et al., *A Quality of Service Architecture*		1994	Campbell QoS	Obvious: 10-16
B-5	CoreConnect		1999	CoreConnect	Anticipated: 10-16 Obvious: 10-16
B-6	Edwin Rijpkema, et al., *A Router Architecture for Networks on Silicon*		Oct. 2, 2001	Rijpkema	Anticipated: 10-16 Obvious: 10-16
B-7	Andrew S. Tanenbaum, *Computer Networks,* Third Edition		1996	Tanenbaum	Obvious: 10-16
B-8	U.S. 7,373,449	Oct. 7, 2003	May 13, 2008	AAPA	Obvious: 10-16
B-9	U.S. Pub. No. 2001/0042147	Dec. 5, 2000	Nov. 15, 2001	Adams	Anticipated: 10-16 Obvious: 10-16
B-10	U.S. Pub. No. 2004/0103230	Nov. 25, 2002	May 27, 2004	Emerson	Anticipated: 10-16 Obvious: 10-16
B-11	U.S. Pub. No. 2002/0129173	Mar. 9, 2001	Sept. 12, 2002	Weber-Alternative	Obvious: 10-16
B-12	William J. Dally, et al., *Router Packets, Not Wires: On-Chip Interconnection Networks*		June 2001	Dally	Obvious: 10-16
B-13S	K. Goossens, et al., *Networks on Silicon: Combining Best-Effort*		Aug. 7, 2002	Goossens2002	Obvious: 10-16

	and Guaranteed Services				
B-14S	K. Goossens, et al., *Guaranteeing the Quality of Services in Networks on Chip*		Jan. 31, 2003	Goossens2003	Obvious: 10-16
B-15S	U.S. 5,461,661	June 7, 1994	Oct. 24, 1995	Drake	Obvious: 10-16

b) Prior Art Systems/Services To The Asserted Claims of the '449 patent.

Defendants further identify the commercial embodiments of the inventions described in Exhibits B-1 to B-15, to the extent those systems or services were on sale or in public use before the priority date of the '449 patent. Moreover, on information and belief, IBM and other companies sold, offered for sale, and/or publicly used products incorporating IBM's CoreConnect architecture ("CoreConnect") that constitutes prior art to the '449 patent. Chart B-5 demonstrates where each limitation of the claims is found in the CoreConnect architecture.

2. Obviousness Combinations

A person having ordinary skill in the art would have been motivated to modify or combine the references described in attached Exhibits B-1 to B-15 with knowledge of a person of ordinary skill in the art and/or as listed below, or further as shown in the exemplary omnibus reference chart B-16, and for the reasons described below.

Reference	In Combination With	Claims
Dorr	AAPA	10-16
	Weber	10-16
	Tan 2000	10-16
	Campbell QoS	10-16
	Dally	10-16
	Drake	10-16
	AAPA/Dally and Tan 2000	10-16
	AAPA/Dally and Campbell QoS	10-16
	AAPA/Dally and Drake	10-16
	Weber and Tan 2000	10-16
	Weber and Campbell QoS	10-16

	Weber and Drake	10-16
	AAPA/Dally and Weber and Tan 2000	10-16
	AAPA/Dally and Weber and Campbell QoS	10-16
	AAPA/Dally and Weber and Drake	10-16
Weber	AAPA	10-16
	Dorr	10-16
	Tan 2000	10-16
	Campbell QoS	10-16
	Dally	10-16
	Drake	10-16
	AAPA/Dally and Tan 2000	10-16
	AAPA/Dally and Campbell QoS	10-16
	AAPA/Dally and Drake	10-16
	Dorr and Campbell QoS	10-16
	Dorr and Tan 2000	10-16
	Dorr and Drake	10-16
	AAPA/Dally and Dorr and Tan 2000	10-16
	AAPA/Dally and Dorr and Campbell QoS	10-16
	AAPA/Dally and Dorr and Drake	10-16
Tan 2000	AAPA	10-16
	Dorr	10-16
	Weber	10-16
	AAPA and Dorr	10-16
	AAPA and Weber	10-16
Campbell QoS	AAPA	10-16
	Dorr	10-16
	Weber	10-16
	AAPA and Dorr	10-16
	AAPA and Weber	10-16
CoreConnect	AAPA	10-16
	Dorr	10-16
	Weber	10-16
	Tan 2000	10-16
	Campbell QoS	10-16
	Dally	10-16
	Drake	10-16
Rijpkema	Dorr	10-16
	Tan 2000	10-16
	Tan 2000 + AAPA	10-16
	Tanenbaum	10-16
	Tanenbaum + AAPA	10-16
	Drake	10-16
	Drake + AAPA	10-16
Tanenbaum	AAPA	10-16
Adams	Dorr	10-16
	Tanenbaum	10-16
	Tanenbaum + AAPA/Dally	10-16
	Drake	10-16

	Drake + AAPA/Dally	10-16
Emerson	Dorr Tanenbaum Tanenbaum + AAPA/Dally Drake Drake + AAPA/Dally	10-16 10-16 10-16 10-16 10-16
Weber-Alternative	AAPA Dorr Tan 200 Campbell QoS Weber Dally Drake AAPA/Dally and Tan 2000 AAPA/Dally and Campbell QoS AAPA/Dally and Drake Dorr and Campbell QoS Dorr and Tan 2000 Dorr and Drake AAPA/Dally and Dor and Tan 2000 AAPA/Dally and Dorr and Campbell QoS	10-16 10-16 10-16 10-16 10-16 10-16 10-16 10-16 10-16 10-16 10-16 10-16 10-16 10-16 10-16
Goossens2002	Dorr Tan 2000 Tan 2000 + AAPA Tanenbaum Tanenbaum + AAPA Drake Drake + AAPA	10-16 10-16 10-16 10-16 10-16 10-16 10-16
Goossens2003	Dorr Tan 2000 Tan 2000 + AAPA Tanenbaum Tanenbaum + AAPA Drake Drake + AAPA	10-16 10-16 10-16 10-16 10-16 10-16 10-16
Drake	AAPA	10-16

A person having ordinary skill in the art at the time of filing of the ’449 patent would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them. It would have been obvious to a person of ordinary skill in the art at the time of the alleged invention to combine a reference with one or more of the other references for the following reasons:

- Combining the prior art limitations according to known methods would have yielded predictable results.
- Simple substitution of one known limitation for another would have yielded predictable results.
- Use of known technique to improve similar devices in the same way would have been obvious.
- Applying a known technique to a known device ready for improvement would have yielded predictable results.
- References disclosing these concepts teach the beneficial utility of them, including as cited in the claim charts submitted herewith.

In addition, a person of ordinary skill in the art would have been motivated to make the combinations based on the general industry trends and other considerations discussed in connection with the state of the art. For example, as explained above in Section IV that describes the state of the art prior to the alleged dates of alleged inventions in the Asserted Patents, the industry was moving towards using system-on-chips (SoCs). Mirroring the general trend of higher integration with time (e.g., Moore's Law), the SoCs were integrating greater number of modules all on one chip. A person of skill in the art was aware of the need for interconnection networks to connect the modules on a single chip as well as they traditionally connected modules on different chips. As further explained in Section IV, researchers were advocating the need to adopt principles and techniques from computer networking domains in the context of SoCs. A person of ordinary skill in the art would have been aware of such trends and suggestions to incorporate techniques from closely-related domains to address and overcome challenges in the SoC arena.

A person of ordinary skill in the art at the time of the alleged invention would have combined the references because each generally relates to similar technology (*See* e.g., Dorr at Abstract, FIG. 1; Weber at para. [0041], FIG. 14; Tan 2000 at Abstract; Campbell QoS at pp. 7; Rijpkema at Title; Tanenbaum at pp. 1-2; Adams at Abstract; Emerson at Abstract; Goossens2002 at Abstract; Goossens2003 at Abstract; Drake at Abstract). A person of skill in the art also would have been motivated to combine references in order to obtain the benefits of one prior art device, system or method in another device, system or method. Moreover, to the extent the ’449 patent identifies any known need for improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, it would also have been obvious to a person of ordinary skill in the art to combine all the combinations listed above with the Applicant Admitted Prior Art (“AAPA”) of the ’449 patent. The ’449 patent admits that systems on silicon and networks on chip are prior art, and that there were known motivations to use a NoC instead of a bus. *See, e.g.*, ’449 patent at 1:15-49. For example, the ‘449 patent indicates that it was known that a NoC “resolve[s] the electrical problems in new deep-submicron technologies, as they structure and manager global wires” and a NoC “share[s] wires, lowering their number and increasing their utilization”. *Id. at* 1:38-42. The ’449 patent also admits that it was known that NoCs are “energy efficient and reliable and are scalable compared to buses”. *Id.* at 1:42-43. The ‘449 patent further admits that it was known that NoCs “decouple computation from communication, which is essential in managing the design of billion-transistor chips.” *Id.* at 43-46. The ’449 patent also admits that off-chip network technology is related and applicable to on-chip networks. *See, e.g.*, ’449 patent

at 1:61-66. The ’449 patent also admits that “transactions” comprising requests and responses were known in the art. *See, e.g.*, ’449 patent at 4:7–28; *see also id*. at 15:63–65, 18:1–6. Furthermore, the ’449 patent admits that prior art protocols “allow transactions to be performed on connections.” *See, e.g.*, ’449 patent at 4:29–44; *see also id*. at 9:59–61, 18:6–12. To the extent the ’449 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, the AAPA of the ’449 patent would have provided additional motivation to combine according to the combinations listed above.

For example, Dorr teaches an on-chip communication system including an on-chip network. *See, e.g.*, Dorr at 3:56-67. In particular, Dorr teaches that the on-chip communication system includes requests from an interface controller to a fabric arbiter that manages resources of the network. *See, e.g.*, Dorr at 6:59-7:28. It would have been obvious to combine Dorr with Weber, which describes a communication system in an integrated circuit and further describes independent data channels. *See, e.g.*, Weber at 4:43–5:8, 15:38-49, 16:10–21. In addition, it would have obvious to combine Dorr or Dorr and Weber with Tan 2000 or Campbell QoS, both of which disclose networks that implement connections using connection managers and resource managers. *See, e.g.*, Campbell QoS at 12, 14–15, 17–18; Tan 2000 at 115–118.

For example, Weber-Alternative teaches an on-chip system utilizing data flows. *See, e.g.*, Weber at FIG. 14, 15:38-64. It would have been obvious to combine Weber-Alternative with Dorr, which describes an on-chip communication system that includes requests from an interface controller to a fabric arbiter that manages resources of the network. *See, e.g.*, Dorr at 6:59-7:28.

In addition, it would have obvious to combine Weber-Alternative or Weber-Alternative and Dorr with Tan 2000 or Campbell QoS, both of which disclose networks that implement connections using connection managers and resource managers. *See, e.g.*, Campbell QoS at 12, 14–15, 17–18; Tan 2000 at 115–118. It would also have been obvious to combine the connections used in Weber with the communication system described in Weber-Alternative and/or Dorr and/or Tan 2000 or Campbell QoS in order to implement the connections of Weber in that communication system. Weber-Alternative relates to an embodiment in which a communication system communicatively coupling function blocks includes multiple communications sub-systems. *See* Weber at FIG. 14. It would have been obvious to implement the connections of Weber in the communications system of Weber-Alternative in order to implement global connection identification. *See* Weber at para. 48. In fact, Weber indicates that request and responses can be tagged in order to allow quality of service guarantees to be given. *Id.* at para. 98.

As another example, it would have been obvious to combine CoreConnect with either Campbell QoS or with Weber. CoreConnect discloses a high-performance and multi-tiered interconnect that can be employed to connect modules in an SoC. Campbell QoS teaches a communication system including a network. *See, e.g.*, Campbell QoS at pp. 7. Weber teaches an on-chip system having one or more functional blocks and one or more communication subsystems for connecting the functional blocks. *See, e.g.*, Weber at FIG. 14, 15:38-49. To the extent the ’449 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

As another example, it would have been obvious to combine Rijpkema and Dorr in order to implement the requests and associated resource management of Dorr for the arbitration within the NoC of Rijpkema. Rijpkema indicates that arbitration is used with its best efforts channels but does not describe some details about how the arbitration is implemented. *See* Rijpkema at pp. 7, col. 2. It would have been obvious to look to other on-chip interconnects, like Dorr, to implement the arbitration in Rijpkema.

As another example, it would have been obvious to combine Rijpkema and Tan 2000, Campbell QoS, or Tanenbaum in order to implement the connections of Tan 2000, Campbell QoS, or Tanenbaum in the NoC of Rijpkema. Rijpkema describes that interconnection networks can be either connection-oriented or connectionless and that the system of Rijpkema uses a connection-oriented service for its guaranteed throughput traffic. *See* Rijpkema at pp. 2, col. 2. Tan 2000 describes details about systems and methods that use connections. *See* Tan 2000 at Abstract. Campbell QoS describes connection-oriented transport in a computer network. Campbell QoS at pp. 12. Tanenbaum describes details about connection-oriented systems. *See* Tanenbaum at pp. 39-40. It would have obvious to use the connection-oriented systems and processes of Tan 2000 or Tanenbaum in the connection-oriented service of Rijpkema. It would also have been obvious to combine AAPA with Rijpkema and Tan 2000 or Tanenbaum. AAPA indicates that computer networking concepts like those implemented in Tan 200 and Tanenbaum are "very much related" and "applicable" to on-chip interconnects like Rijpkema. '449 patent at 1:61-66.

As another example, Tanenbaum describes connection-oriented systems for computer networks. *See* Tanenbaum at pp. 39-40. It would also have been obvious to combine AAPA with Tanenbaum in order to implement the connection-oriented systems of Tanenbaum in an on-chip

network. AAPA indicates that computer networking concepts like those implemented in Tanenbaum are “very much related” and “applicable” to on-chip interconnects. ’449 patent at 1:61-66.

As another example, Drake describes ensuring quality of service for transmission requests in computer networks. *See* Drake at Abstract. It would also have been obvious to combine AAPA with Drake in order to implement the quality of service mechanisms of Drake in an on-chip network. AAPA indicates that computer networking concepts like those implemented in Drake are “very much related” and “applicable” to on-chip interconnects. ’449 patent at 1:61-66.

As another example, it would have been obvious to combine Adams and Dorr in order to implement the requests and associated resource management of Dorr for the arbitration in the system of Adams. Adams indicates that arbitration is used and that different arbitration schemes can be used. *See* Adams at para. 54-56. It would have been obvious to look to other on-chip interconnects, like Dorr, to implement the arbitration in Adams.

As another example, it would have been obvious to combine Emerson and Dorr in order to implement the requests and associated resource management of Dorr for the arbitration in the system of Emerson. Adams indicates that arbitration is used and that different arbitration schemes can be used. *See* Emerson at para. 25-26. It would have been obvious to look to other on-chip interconnects, like Dorr, to implement the arbitration in Emerson.

As another example, it would have been obvious to combine Goossens2002 and Drake for at least the reasons provided in IPR2024-00338 and supporting exhibits, including the expert declaration of Dr. Todd Mowry.

It would also have been obvious to modify any of the references to replace any of their interconnects with a NoC based on the AAPA or Dally. In particular, the AAPA admits that NoCs were known and that there were known motivations to use a NoC for an interconnect in place of a bus. *See* '449 patent at 1:15-49. Dally also indicates that networks on chip are generally preferable to a bus because they have higher bandwidth and support multiple concurrent communications. *See* Dally at pp. 1.

It would also have been obvious to modify any of the references to combine discrete components together into a single integrated circuit ("IC") in the form of a system-on-chip ("SoC"). In particular, the text entitled *Modern VLSI Design: System-on-Chip Design, Third Edition* by Wayne Wolf explains that at the time of the patent, it was known that integrating discrete components onto an integrated circuit allowed designers "to build systems with many more transistors, allowing much more computing power to be applied to solving a problem." W. Wolf, *Modern VLSI Design: System-on-Chip Design, Third Edition*, Prentice Hall 2002 ("Wolf") at 1. Wolf teaches that integrated circuits are "much easier to design and manufacture and are more reliable than discrete systems," and that the small sizes of integrated circuits "leads to advantages in speed and power consumption, since smaller components have smaller parasitic resistances, capacitances, and inductances." *Id.* at 2. Wolf further explains, "Communication within a chip can occur hundreds of times faster than communication between chips on a printed circuit board" because on-chip circuits are smaller, and "smaller components and wires have smaller parasitic capacitances to slow down the signal." *Id.* Wolf notes that the small size of a device is "often an advantage in itself," and that replacing discrete components with a single chip reduces power consumption, which has ripple effects on the rest of the system. *Id*. at 3. For example, with reduced power consumption, a smaller and cheaper power supply can be used. *Id*.

Lower power consumption means less heat, so a fan may no longer be necessary. *Id*. Finally, Wolf explains that reducing the number of components, power supply requirements, and so on will "inevitably reduce system cost." *Id*. Indeed, as Wolf explains, many motivations exist to combine discrete components together to form a single IC.

The Applicant's Admitted Prior Art (AAPA) in the '449 patent also confirms that SoCs were previously known, and that it was known to combine discrete components together into a single IC in the form of an SoC, and thus the AAPA in the patent confirms it would have been obvious to modify any of the references to combine discrete components together into a single IC in the form of an SoC. Specifically, the Applicant for the '449 patent explained that the alleged invention arose out of "a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions" in ICs and by "the increasing density with which components can be integrated on an integrated circuit." '449 patent at 1:15-19.

The combinations of references provided are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendants may rely on such combination(s) in this litigation. In particular, Defendants are currently unaware of Plaintiff's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendants are also unaware of the extent, if any, to which Plaintiff may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendants as anticipatory, and the extent to which Plaintiff will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendants do not yet know how the Court will construe terms in the asserted claims. Defendants are also continuing its investigation of the

universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Plaintiff may also be in possession of prior art that Defendants may receive as discovery progresses in this case. Defendants reserve the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

C. Disclosures For U.S. Patent 7,594,052

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits C-1 to C-20 demonstrate where each limitation of the claims is found in, either expressly or inherently in the larger context of the passage, or rendered obvious by, certain of the references listed below, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a) Prior Art Patents, Patent Publications, and Non-Patent Publications to the Asserted Claims of the ’052 patent.

Chart	Reference	Filing Date	Date of Issue or Publication	Citation	Claims
C-1S	U.S. 7,165,094	Mar. 9, 2001	Jan. 16, 2007	Weber	Anticipated: 6 Obvious: 6
C-1S	U.S. Pub. No. 2002/0129173	Mar. 9, 2001	Sept. 12, 2002	Weber	Anticipated: 6 Obvious: 6
C-2	U.S. 6,330,225	May 26, 2000	Dec. 11, 2001	Weber II	Anticipated: 6 Obvious: 6

C-3	International Publication Number WO00/29961	Nov. 13, 1998	May 25, 2000	Wingard	Anticipated: 6 Obvious: 6
C-4	U.S. 7,200,137	July 29, 2002	Apr. 3, 2007	Dorr	Anticipated: 6
C-4	U.S. Pub. No. 2004/0017807	July 29, 2002	Jan. 29, 2004	Dorr	Obvious: 6
C-5	A. Radulescu & K. Goossens, *Communication Services for Networks on Chip*		July 2002	2002 Radulescu	Anticipated: 6
C-6	J. Dielissen, et al., *Concepts and Implementation of the Philips Network-on-Chip*		Jan. 2004	Dielissen	Obvious: 6
C-7	P. Guerrier, *An Interconnection Network for Integrated Systems*		2000	Guerrier Thesis	Obvious: 6
C-8	TriMedia TM1100 Databook		1999	TriMedia	Obvious: 6
C-9	CoreConnect		1999	CoreConnect	Anticipated: 6 Obvious: 6
C-10	U.S. 6,430,154	Aug. 10, 2000	Aug. 6, 2002	Hunt	Obvious: 6
C-11	U.S. Pub. No. 2001/0037435	Mar. 21, 2001	Nov. 1, 2001	Van Doren	Obvious: 6
C-12	K. Goossens, et al., *Guaranteeing the Quality of Services in Networks on Chip*		Jan. 2003	2003 Goossens	Anticipated: 6 Obvious: 6

C-13	U.S. 7,373,449 & U.S. 7,594,052	Oct. 7, 2003 Mar. 7, 2005	May 13, 2008 Sept. 22, 2009	AAPA	Anticipated: 6 Obvious: 6
C-14	U.S. Pub. No. 2002/0129173	Mar. 9, 2001	Sept. 12, 2002	Weber - Alternative	Anticipated: 6 Obvious: 6
C-15	U.S. Pub. No. 2001/0042147	Dec. 5, 2000	Nov. 15, 2001	Adams	Anticipated: 6 Obvious: 6
C-16	Andrew S. Tanenbaum, *Computer Networks,* Third Edition		1996	Tanenbaum	Anticipated: 6 Obvious: 6
C-17	William J. Dally, et al., *Router Packets, Not Wires: On-Chip Interconnection Networks*		June 2001	Dally	Obvious: 6
C-18S	A. Radulescu, et al., *An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared Memory Abstraction, and Flexible Network Configuration*		Feb. 16, 2004	2004 Radulescu	Anticipated: 6 Obvious: 6
C-19	Evgeny Bolotin, *QNoC: QoS architecture and design process for network on chip*		July 4, 2003	Bolotin	Anticipated: 6 Obvious: 6
C-20S	Open Core Protocol Specification, Release 1.0, OCP-IP Association (2001)		2001	OCP	Anticipated: 6 Obvious: 6

b) Prior Art Systems/Services To The Asserted Claims of the ’052 patent.

Defendants further identify the commercial embodiments of the inventions described in Exhibits C-1 to C-20, to the extent those systems or services were on sale or in public use before the priority date of the ’052 patent. Moreover, on information and belief, IBM and other companies sold, offered for sale, and/or publicly used products incorporating IBM’s CoreConnect architecture (“CoreConnect”) that constitutes prior art to the ’052 patent. Chart C-9 demonstrates where each limitation of the claims is found in the CoreConnect architecture.

2. Obviousness Combinations

A person having ordinary skill in the art would have been motivated to modify or combine the references described in attached Exhibits C-1 to C-20 with knowledge of a person of ordinary skill in the art and/or as listed below, or further as shown in the exemplary omnibus reference chart C-21, and for the reasons described below.

Reference	In Combination With	Claims
Weber	AAPA	6
	Dorr	6
	Hunt	6
	Van Doren	6
	Radulescu	6
	Dielissen	6
	2003 Goossens	6
	Dally	6
	OCP	6
	Hunt and Van Doren	6
	AAPA/Dally and Hunt	6
	AAPA/Dally and Van Doren	6
	AAPA/Dally and Hunt and Van Doren	6
	Radulescu and Hunt	6
	Radulescu and Van Doren	6
	Radulescu and Hunt and Van Doren	6
	Dielissen and Hunt	6
	Dielissen and Van Doren	6
	Dielissen and Hunt and Van Doren	6
	Weber-Alternative	6
Dorr	AAPA	6
	Weber	6
	Hunt	6
	Van Doren	6

	Radulescu	6
	Dielissen	6
	2003 Goossens	6
	Dally	6
	OCP	6
	Hunt and Van Doren	6
	AAPA/Dally and Weber	6
	AAPA/Dally and Hunt	6
	AAPA/Dally and Van Doren	6
	AAPA/Dally and Weber and Van Doren	6
	Weber and Radulescu	6
	Weber and Dielissen	6
	Weber and 2003 Goossens	6
	Weber and Hunt	6
	Van Doren and Radulescu	6
	Van Doren and Dielissen	6
	Van Doren and Hunt	6
2002 Radulescu	AAPA	6
	Weber	6
	Weber-Alternative	6
	Dorr	6
	Hunt	6
	Van Doren	6
	Dielissen	6
	2003 Goossens	6
	Tanenbaum	6
	OCP	6
	Weber and Hunt	6
	Weber and Van Doren	6
	Hunt and Van Doren	6
	Dielissen and 2003 Goossens	6
	Dielissen and 2003 Goossens and Tanenbaum	6
Dielissen	AAPA	6
	Weber	6
	Dorr	6
	Hunt	6
	Van Doren	6
	Radulescu	6
	2003 Goossens	6
	Tanenbaum	6
	OCP	6
	Weber and Hunt	6
	Weber and Van Doren	6
	Hunt and Van Doren	6
	Radulescu and 2003 Goossens	6
	Radulsecu and 2003 Goossens and Tanenbaum	6
2003 Goossens	AAPA	6
	Weber	6

	Dorr	6
	Hunt	6
	Van Doren	6
	Radulescu	6
	Dielissen	6
	Tanenbaum	6
	OCP	6
	Weber and Hunt	6
	Weber and Van Doren	6
	Hunt and Van Doren	6
	Radulescu and Dielissen	6
	Radulescu and Dielissen and Tanenbaum	6
Weber II	AAPA	6
	Wingard	6
	Dorr	6
	Hunt	6
	Radulescu	6
	Dielissen	6
	2003 Goossens	6
	Dally	6
	OCP	6
Wingard	AAPA	6
	Weber II	6
	Dorr	6
	Hunt	6
	Radulescu	6
	Dielissen	6
	2003 Goossens	6
	Dally	6
	OCP	6
Guerrier Thesis	AAPA	6
	Weber	6
	Dorr	6
	Weber II	6
	Wingard	6
	Radulescu	6
	Dielissen	6
	2003 Goossens	6
	Dally	6
	OCP	6
TriMedia	AAPA	6
	Weber	6
	Guerrier Thesis	6
Tanenbaum	AAPA	6
2004 Radulescu	AAPA	6
	Weber	6
	Weber-Alternative	6
	Dorr	6

	Hunt	6
	Van Doren	6
	Dielissen	6
	2003 Goossens	6
	Tanenbaum	6
	OCP	6
	Weber and Hunt	6
	Weber and Van Doren	6
	Hunt and Van Doren	6
	Dielissen and 2003 Goossens	6
	Dielissen and 2003 Goossens and Tanenbaum	6
Bolotin	AAPA	6
	Weber	6
	Weber-Alternative	6
	Dorr	6
	Hunt	6
	Van Doren	6
	Dielissen	6
	2003 Goossens	6
	Tanenbaum	6
	OCP	6
	Weber and Hunt	6
	Weber and Van Doren	6
	Hunt and Van Doren	6
	Dielissen and 2003 Goossens	6
	Dielissen and 2003 Goossens and Tanenbaum	6
OCP	AAPA	6
Adams	AAPA	6
	Weber	6
	Weber-Alternative	6
	Dorr	6
	Hunt	6
	Van Doren	6
	Dielissen	6
	2003 Goossens	6
	Tanenbaum	6
	OCP	6
	Weber and Hunt	6
	Weber and Van Doren	6
	Hunt and Van Doren	6
	Dielissen and 2003 Goossens	6
	Dielissen and 2003 Goossens and Tanenbaum	6

A person having ordinary skill in the art at the time of filing of the ’052 patent would also have understood the references listed above, alone or in combination, to contain explicit and/or

implicit teaching, suggestion, and/or rationales to combine them. It would have been obvious to a person of ordinary skill in the art at the time of the alleged invention to combine a reference with one or more of the other references for the following reasons:

- Combining the prior art limitations according to known methods would have yielded predictable results.
- Simple substitution of one known limitation for another would have yielded predictable results.
- Use of known technique to improve similar devices in the same way would have been obvious.
- Applying a known technique to a known device ready for improvement would have yielded predictable results.
- References disclosing these concepts teach the beneficial utility of them, including as cited in the claim charts submitted herewith.

In addition, a person of ordinary skill in the art would have been motivated to make the combinations based on the general industry trends and other considerations discussed in connection with the state of the art. For example, as explained above in Section IV that describes the state of the art prior to the alleged dates of alleged inventions in the Asserted Patents, the industry was moving towards using system-on-chips (SoCs). Mirroring the general trend of higher integration with time (also referred to as Moore's Law), the SoCs were integrating greater number of modules all on one chip. A person of skill in the art was aware of the need for interconnection networks to connect the modules on a single chip as well as they traditionally connected modules on different chips. As further explained in Section IV, researchers were advocating the need to adopt principles and techniques from computer networking domains in

the context of SoCs. A person of ordinary skill in the art would have been aware of such trends and suggestions to incorporate techniques from closely-related domains to address and overcome challenges in the SoC arena.

A person of ordinary skill in the art at the time of the alleged invention would have combined the references because each generally relates to similar technology (e.g., Weber at para. [0095-0098], Fig. 14; 2002 Radulescu at 287–91; 2004 Radulescu at Abstract; Dielissen at 5, Fig. 11; 2003 Goossens at 71–77; Weber II at Fig. 1; Wingard at 6–7, Fig. 1; Tanenbaum at pp. 1-2; Adams at Abstract, OCP at xi). Moreover, to the extent the ’052 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, it would also have been obvious to a person of ordinary skill in the art to combine all the combinations listed above with the Applicant Admitted Prior Art (“AAPA”) of the ’052 patent. The ’052 patent admits that systems on silicon and networks on chip are prior art, and that there were known motivations to use a NoC instead of a bus. *See, e.g.*, ‘052 patent at 1:14-48. For example, the ‘052 patent indicates that it was known that a NoC “resolve[s] the electrical problems in new deep-submicron technologies, as they structure and manager global wires” and a NoC “share[s] wires, lowering their number and increasing their utilization”. *Id. at* 1:39-41. The ’052 patent also admits that it was known that NoCs are “energy efficient and reliable and are scalable compared to buses”. *Id.* at 1:41-42. The ’052 patent further admits that it was known that NoCs “decouple computation from communication, which is essential in managing the design of billion-transistor chips.” *Id.* at 43-45. The ’052 patent also admits that off-chip network technology is related and applicable to on-chip networks. *See, e.g.*, ’052 patent

at 1:59-64. In addition, the ’052 patent admits that “existing protocols” utilized threads and address ranges as communication service identifiers. *See, e.g.*, ’052 patent at 4:15–21, 5:53–6:3, 8:21–25; *see also id*. at 2:63–3:2, 6:30–387:34–39, 8:41–58. Furthermore, the ’052 patent admits that “interconnect[s] supporting connections” were known in the art. *See, e.g.*, ’052 patent at 8:47–51. To the extent the ’052 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, the AAPA of the ’052 patent would have provided additional motivation to combine according to the combinations listed above.

For example, Weber teaches an on-chip system utilizing data flows and further describes mapping threads to connections. *See, e.g.*, Weber at 19:57–20:8, 21:4–34. It would have been obvious to combine Weber with 2002 Radulescu, 2004 Radulescu, Dielissen, 2003 Goossens or Hunt, each of which teaches mapping communication services to connections based on connection properties. *See, e.g.*, 2002 Radulescu at 288, 291–96; 2004 Radulescu at 1-2,3-7, 9; Dielissen at 4, Figs. 3–4, 10; 2003 Goossens at 71–77; Hunt at 4:56–5:11, 11:4–49; IPR2024-00343 and supporting exhibits, including the expert declaration of Dr. Marwan Hassoun. In addition, it would have been obvious to combine Weber, or Weber and one of 2002 Radulescu, 2004 Radulescu, Dielissen, 2003 Goossens, or Hunt with Van Doren, which describes mapping address ranges to connections. *See, e.g.*, Van Doren at [0011], [0013].

As another example, it would have been obvious to combine Weber with Weber-Alternative in order to implement the connections of Weber in the communication system of Weber-Alternative. Weber-Alternative describes an embodiment of Weber in which a

communication system communicatively coupling function blocks includes multiple communications sub-systems. *See* Weber-Alternative at FIG. 14. It would have been obvious to implement the connections of Weber in the communications system of Weber-Alternative in order to implement global connection identification. *See* Weber at ¶ 48.

As another example, Dorr teaches an on-chip communication system including an on-chip network. *See, e.g.*, Dorr at 3:56-67. In particular, Dorr teaches that communication transactions are mapped to logical communication pathways based on communication properties. *See, e.g.*, Dorr at 29:16–51. It would have been obvious to combine Dorr with Van Doren, which describes mapping address ranges to connections, and/or with Weber, which describes mapping threads to connections. *See, e.g.*, Van Doren at [0011], [0013]; Weber at 19:57–20:8, 21:4–34. In addition, it would have been obvious to combine Dorr, alone or in combination with Van Doren or Weber, with 2002 Radulescu, 2004 Radulescu, Dielissen, 2003 Goossens, or Hunt, each of which teaches mapping communication services to connections based on connection properties. *See, e.g.*, 2002 Radulescu at 288, 291–96; 2004 Radulescu at 1-2,3-7, 9; Dielissen at 4, Figs. 3–4, 10; 2003 Goossens at 71–77; Hunt at 4:56–5:11, 11:4–49.

As another example, Bolotin teaches a network on chip (NoC) architecture that implements Quality of Service (QoS). *See, e.g.*, Bolotin at Abstract. Bolotin teaches a priority scheme in which different QoS services are given different priority, which is implemented by the NoC. *Id.* at 108-109. It would have been obvious to combine Bolotin with Van Doren, which describes mapping address ranges to connections implementing services, and/or with Weber, which describes mapping threads to services. *See, e.g.*, Van Doren at [0011], [0013]; Weber at 19:57–20:8, 21:4–34. In addition, it would have been obvious to combine Bolotin, alone or in combination with Van Doren or Weber, with 2002 Radulescu, 2004 Radulescu, Dielissen, 2003

Goossens, or Hunt, each of which teaches mapping communication services to connections implementing services based on connection properties. *See, e.g.*, 2002 Radulescu at 288, 291–96; 2004 Radulescu at 1-2,3-7, 9; Dielissen at 4, Figs. 3–4, 10; 2003 Goossens at 71–77; Hunt at 4:56–5:11, 11:4–49.

As another example, Adams teaches a system on chip (SoC) including a system-resource router that interfaces initiators through protocol adapting sockets to a plurality of sub-buses. Adams at para. [0001, 0013]. Adams teaches address remapping in which sectors of a socket can be remapped such that different address bits as inputs are mapped to an output. *Id.* at para. [0074]. It would have been obvious to combine Adams with Van Doren, which describes mapping address ranges to connections implementing services, and/or with Weber, which describes mapping threads to services. *See, e.g.*, Van Doren at [0011], [0013]; Weber at 19:57–20:8, 21:4–34. In addition, it would have been obvious to combine Bolotin, alone or in combination with Van Doren or Weber, with 2002 Radulescu, 2004 Radulescu, Dielissen, 2003 Goossens, or Hunt, each of which teaches mapping communication services to connections implementing services based on connection properties. *See, e.g.*, 2002 Radulescu at 288, 291–96; 2004 Radulescu at 1-2,3-7, 9; Dielissen at 4, Figs. 3–4, 10; 2003 Goossens at 71–77; Hunt at 4:56–5:11, 11:4–49.

As another example, it would have been obvious to combine 2002 Radulescu and Weber-Alternative in order to implement the data flow mapping of Weber-Alternative for the connections of 2002 Radulescu. Weber-Alternative describes that a data flow mapping process is performed in order to provide end-to-end system performance guarantees. Weber at para. [0104]. It would have been obvious to implement the mapping of Weber-Alternative with the

connections of 2002 Radulescu in order to provide end-to-end system performance guarantees to the connections.

As another example, it would have been obvious to combine 2002 Radulescu and OCP in order to implement the mapping of OCP for the connections of 2002 Radulescu. OCP describes that threads can be mapped to connections. OCP at 47. It would have been obvious to implement the mapping of OCP with the connections of 2002 Radulescu in order to provide end-to-end services.

As another example, it would have been obvious to combine 2004 Radulescu and Weber-Alternative in order to implement the data flow mapping of Weber-Alternative for the connections of 2004 Radulescu. Weber-Alternative describes that a data flow mapping process is performed in order to provide end-to-end system performance guarantees. Weber at para. [0104]. It would have been obvious to implement the mapping of Weber-Alternative with the connections of 2004 Radulescu in order to provide end-to-end system performance guarantees to the connections.

As another example, it would have been obvious to combine 2004 Radulescu and OCP for at least the reasons provided in IPR2024-00343 and supporting exhibits, including the expert declaration of Dr. Marwan Hassoun.

As another example, it would have been obvious to combine 2003 Goossens and OCP in order to implement the mapping of OCP for the connections of 2003 Goossens. OCP describes that threads can be mapped to connections. OCP at 47. It would have been obvious to implement the mapping of OCP with the connections of 2003 Goossens in order to provide end-to-end services.

As another example, it would have been obvious to combine Dielissen and Weber-Alternative in order to implement the data flow mapping of Weber-Alternative for the connections of Dielissen. Weber-Alternative describes that a data flow mapping process is performed in order to provide end-to-end system performance guarantees. Weber at para. [0104]. It would have been obvious to implement the mapping of Weber-Alternative with the connections of Dielissen in order to provide end-to-end system performance guarantees to the connections.

As another example, it would have been obvious to combine 2002 Radulescu and Tanenbaum in order to implement the connections of Tanenbaum in the NoC of 2002 Radulescu. Tanenbaum describes details about connection-oriented systems. *See* Tanenbaum at pp. 39-40. It would have been obvious to use the connection-oriented systems and processes of Tanenbaum in the connection-oriented service of Radulescu. It would also have been obvious to combine AAPA with 2002 Radulescu and Tanenbaum. AAPA indicates that computer networking concepts like those implemented in Tanenbaum are "very much related" and "applicable" to on-chip interconnects like 2002 Radulescu. '052 patent at 1:62-64.

As another example, it would have been obvious to combine 2004 Radulescu and Tanenbaum in order to implement the connections of Tanenbaum in the NoC of 2004 Radulescu. Tanenbaum describes details about connection-oriented systems. *See* Tanenbaum at pp. 39-40. It would have been obvious to use the connection-oriented systems and processes of Tanenbaum in the connection-oriented service of Radulescu. It would also have been obvious to combine AAPA with 2004 Radulescu and Tanenbaum. AAPA indicates that computer networking concepts like those implemented in Tanenbaum are "very much related" and "applicable" to on-chip interconnects like 2004 Radulescu. '052 patent at 1:62-64.

As another example, it would have been obvious to combine Weber II with Wingard. Both Weber II and Wingard teach a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Weber II at Fig. 1; Wingard at 6–7, Fig. 1. Both Weber II and Wingard share the same co-inventor Drew Wingard, and Weber II explicitly references Wingard as providing more details about the system disclosed in Weber II. *See* Weber II at 4:56–58. In addition, it would have been obvious to combine Weber II, Wingard, or Weber II and Wingard with 2002 Radulescu, 2004 Radulescu, Dielissen, 2003 Goossens, or Hunt, each of which teaches mapping communication services to connections based on connection properties. *See, e.g.*, 2002 Radulescu at 288, 291–96; 2004 Radulescu at 1-2,3-7, 9; Dielissen at 4, Figs. 3–4, 10; 2003 Goossens at 71–77; Hunt at 4:56–5:11, 11:4–49. Moreover, to the extent the ’052 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

As another example, it would have been obvious to combine the Guerrier Thesis with one of the following: Weber, Weber II and Wingard. Guerrier Thesis discloses a high-performance and scalable interconnection network for connecting multiple modules on a single chip. Weber teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Weber at 15:30–16:21, Fig. 14, Wingard at 6–7, Fig. 1. Both Weber II and Wingard share the same co-inventor Drew Wingard, and Weber II explicitly references Wingard as providing more details about the system disclosed in Weber II. *See* Weber II at 4:56–58.

As another example, it would have been obvious to combine TriMedia with either Weber or with Guerrier Thesis. TriMedia teaches a high-performance integrated circuit for multi-media applications that combines multiple modules on a single chip to offer a broad array of

functionality. Guerrier Thesis discloses a high-performance and scalable interconnection network for connecting multiple modules on a single chip. Weber teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Weber at 15:30–16:21, Fig. 14.

As another example, Tanenbaum describes connection-oriented systems for computer networks. *See* Tanenbaum at pp. 39-40. It would also have been obvious to combine AAPA with Tanenbaum in order to implement the connection-oriented systems of Tanenbaum in an on-chip network. AAPA indicates that computer networking concepts like those implemented in Tanenbaum are "very much related" and "applicable" to on-chip interconnects. '449 patent at 1:61-66.

It would also have been obvious to modify any of the references to replace any of their interconnects with a NoC based on the AAPA or Dally. In particular, the AAPA admits that NoCs were known and that there were known motivations to use a NoC for an interconnect in place of a bus. *See* '052 patent at 1:16-47. Dally also indicates that networks on chip are generally preferable to a bus because they have higher bandwidth and support multiple concurrent communications. *See* Dally at pp. 1. The combinations of references provided are exemplary and are not intended to be exhaustive.

It would also have been obvious to modify any of the references to combine discrete components together into a single integrated circuit ("IC") in the form of a system-on-chip ("SoC"). In particular, the text entitled *Modern VLSI Design: System-on-Chip Design, Third Edition* by Wayne Wolf explains that at the time of the patent, it was known that integrating discrete components onto an integrated circuit allowed designers "to build systems with many more transistors, allowing much more computing power to be applied to solving a problem." W.

Wolf, *Modern VLSI Design: System-on-Chip Design, Third Edition*, Prentice Hall 2002 ("Wolf") at 1. Wolf teaches that integrated circuits are "much easier to design and manufacture and are more reliable than discrete systems," and that the small sizes of integrated circuits "leads to advantages in speed and power consumption, since smaller components have smaller parasitic resistances, capacitances, and inductances." *Id.* at 2. Wolf further explains, "Communication within a chip can occur hundreds of times faster than communication between chips on a printed circuit board" because on-chip circuits are smaller, and "smaller components and wires have smaller parasitic capacitances to slow down the signal." *Id.* Wolf notes that the small size of a device is "often an advantage in itself," and that replacing discrete components with a single chip reduces power consumption, which has ripple effects on the rest of the system. *Id*. at 3. For example, with reduced power consumption, a smaller and cheaper power supply can be used. *Id*. Lower power consumption means less heat, so a fan may no longer be necessary. *Id*. Finally, Wolf explains that reducing the number of components, power supply requirements, and so on will "inevitably reduce system cost." *Id*. Indeed, as Wolf explains, many motivations exist to combine discrete components together to form a single IC.

The Applicant's Admitted Prior Art (AAPA) in the '052 patent also confirms that SoCs were previously known, and that it was known to combine discrete components together into a single IC in the form of an SoC, and thus the AAPA in the patent confirms it would have been obvious to modify any of the references to combine discrete components together into a single IC in the form of an SoC. Specifically, the Applicant for the '052 patent explained that the alleged invention arose out of "a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions" in ICs and by "the

increasing density with which components can be integrated on an integrated circuit." '052 patent at 1:14-18.

Additional obviousness combinations of the references identified here are possible, and Defendants may rely on such combination(s) in this litigation. In particular, Defendants are currently unaware of Plaintiff's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendants are also unaware of the extent, if any, to which Plaintiff may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendants as anticipatory, and the extent to which Plaintiff will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendants do not yet know how the Court will construe terms in the asserted claims. Defendants are also continuing its investigation of the universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Plaintiff may also be in possession of prior art that Defendants may receive as discovery progresses in this case. Defendants reserve the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

D. Disclosures For U.S. Patent No. 7,769,893

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits D-1 to D-12 demonstrate where each limitation of the claims is found in, either expressly or inherently in the larger context of the passage, or rendered obvious by, certain of the references listed below, as understood by a person

having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), (e) or (g)(2).

a) Prior Art Patents, Patent Publications, and Non-Patent Publications to the Asserted Claims of the '9893 patent.

Chart	Reference	Filing Date	Date of Issue or Publication	Citation	Claims
D-1	U.S. 7,266,786	Nov. 5, 2002	Sept. 4, 2007	Chou	Anticipated: 4-6, 9, 11 Obvious: 4-11
D-1	U.S. Pub. No. 2004/0088566	Nov. 5, 2002	May 6, 2004	Chou	Anticipated: 4-6, 9, 11 Obvious: 4-11
D-2	U.S. 7,165,094	Mar. 9, 2001	Jan. 16, 2007	Weber	Obvious: 4-11
D-2	U.S. Pub. No. 2002/0129173	Mar. 9, 2001	Sept. 12, 2002	Weber	Obvious: 4-11
D-3	U.S. 7,302,691	May 10, 2002	Nov. 27, 2007	Masri	Obvious: 4-11
D-3	U.S. Pub. No. 2003/0212743	May 10, 2002	Nov. 13, 2003	Masri	Obvious: 4-11
D-4	K. Goossens, et al., *Networks on Silicon: Combining Best-Effort and Guaranteed Services*		Mar. 2002	2002 Goossens	Obvious: 4-11
D-5	U.S. 6,754,752	Jan. 11, 2001	June 22, 2004	Marietta	Anticipated: 4, 5 Obvious: 4-11
D-5	U.S. Pub. No. 2001/0025328	Jan. 11, 2001	Sept. 27, 2001	Marietta	Obvious: 4-11
D-6	A. Radulescu & K. Goossens, *Communication Services for Networks on Chip*		July 2002	Radulescu	Obvious: 4-11
D-7	K. Goossens, et al., *Guaranteeing the Quality of Services in Networks on Chip*		Jan. 2003	2003 Goossens	Obvious: 4-11
					Anticipated: 4-11

D-8	CoreConnect		1999	CoreConnect	Obvious: 4-11
D-9	U.S. 7,076,595	May 18, 2001	July 11, 2006	Kim Dao	Anticipated: 4-11 Obvious: 4-11
D-10	U.S. 6,996,651	July 29, 2002	Feb. 7, 2006	Garinger	Anticipated: 4-11 Obvious: 4-11
D-10	U.S. Pub. No. 2004/0019733	July 29, 2002	Jan. 29, 2004	Garinger	Anticipated: 4-11 Obvious: 4-11
D-11	William J. Dally, et al., *Router Packets, Not Wires: On-Chip Interconnection Networks*		June 2001	Dally	Obvious: 4-11

b) Prior Art Systems/Services To The Asserted Claims of the ’9893 patent.

Defendants further identify the commercial embodiments of the inventions described in Exhibits D-1 to D-11, to the extent those systems or services were on sale or in public use before the priority date of the ’9893 patent. Moreover, on information and belief, IBM and other companies sold, offered for sale, and/or publicly used products incorporating IBM’s CoreConnect architecture (“CoreConnect”) that constitutes prior art to the ’9893 patent. Chart D-8 demonstrates where each limitation of the claims is found in the CoreConnect architecture.

c) Prior Art Pursuant to 35 U.S.C. 102(g)(2)

On information and belief, the inventors of the Chou patent (i.e., Chien-Chun Chou, Jay Tomlinson, Wolf-Dietrich Weber, Drew Wingard, and Sricharan Kasetti) conceived of the invention disclosed in the Chou patent in the U.S. before the priority date of the ’9893 patent or the date of the conception of the alleged inventions described and claimed in the ’9893 patent. Having conceived the invention disclosed in the Chou patent, the inventors exercised reasonable

diligence in constructively reducing their invention to practice when they filed the application with the USPTO that matured into the Chou patent. The inventors of the Chou patent did not abandon, suppress, or conceal their invention.

2. Obviousness Combinations

A person having ordinary skill in the art would have been motivated to modify or combine the references described in attached Exhibits D-1 to D-11 with knowledge of a person of ordinary skill in the art and/or as listed below, or further as shown in the exemplary omnibus reference chart D-12, and for the reasons described below.

Reference	In Combination With	Claims
Chou	AAPA	4-11
	2002 Goossens	4-11
	Masri	4-11
	Weber	4-11
	Kim Dao	4-11
	Garinger	4-11
	2003 Goossens	4-11
	Radulescu	4-11
	Dally	4-11
	2002 Goossens and Masri	4-11
	2002 Goossens and Kim Dao	4-11
	2002 Goossens and Garinger	4-11
	Weber and Kim Dao	4-11
	Weber and Garinger	4-11
	Weber and Masri	4-11
Marietta	AAPA	4-11
	2002 Goossens	4-11
	Masri	4-11
	Weber	4-11
	2003 Goossens	4-11
	Radulescu	4-11
	Kim Dao	4-11
	Garinger	4-11
	Dally	4-11
	2002 Goossens and Masri	4-11
	2002 Goossens and Kim Dao	4-11
	2002 Goossens and Garinger	4-11
	Weber and Kim Dao	4-11
	Weber and Garinger	4-11

	Weber and Masri	4-11
CoreConnect	AAPA 2002 Goossens Masri Weber 2003 Goossens Radulescu Dally 2002 Goossens and Kim Dao 2002 Goossens and Garinger 2002 Goossens and Masri Weber and Kim Dao Weber and Garinger Weber and Masri	4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11
Kim Dao	2002 Goossens Masri Weber 2003 Goossens Radulescu Garinger Dally 2002 Goossens + Garinger Weber + Masri 2002 Goossens + Garinger Weber + Garinger	4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11
Garinger	2002 Goossens Masri Weber 2003 Goossens Radulescu Dally 2002 Goossens + Masri Weber + Masri	4-11 4-11 4-11 4-11 4-11 4-11 4-11 4-11

A person having ordinary skill in the art at the time of filing of the ’9893 patent would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them. It would have been obvious to a person of ordinary skill in the art at the time of the alleged invention to combine a reference with one or more of the other references for the following reasons:

- Combining the prior art limitations according to known methods would have yielded

predictable results.

- Simple substitution of one known limitation for another would have yielded predictable results.
- Use of known technique to improve similar devices in the same way would have been obvious.
- Applying a known technique to a known device ready for improvement would have yielded predictable results.
- References disclosing these concepts teach the beneficial utility of them, including as cited in the claim charts submitted herewith.

In addition, a person of ordinary skill in the art would have been motivated to make the combinations based on the general industry trends and other considerations discussed in connection with the state of the art. For example, as explained above in Section IV that describes the state of the art prior to the alleged dates of alleged inventions in the Asserted Patents, the industry was moving towards using system-on-chips (SoCs). Mirroring the general trend of higher integration with time (also referred to as Moore's Law), the SoCs were integrating greater number of modules all on one chip. A person of skill in the art was aware of the need for interconnection networks to connect the modules on a single chip as well as they traditionally connected modules on different chips. As further explained in Section IV, researchers were advocating the need to adopt principles and techniques from computer networking domains in the context of SoCs. A person of ordinary skill in the art would have been aware of such trends and suggestions to incorporate techniques from closely-related domains to address and overcome challenges in the SoC arena.

A person of ordinary skill in the art at the time of the alleged invention would have combined the references because each generally relates to similar technology (e.g., Chou at 1:9–11; Marietta at 2:22–3:42; 2002 Goossens at 423; Masri at 1:6–8, 1:26–46, Figs. 1–2; Weber at 15:30–6:21, Fig. 14; 2003 Goossens at 71–77; Radulescu at 287–91). Moreover, to the extent the ’9893 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, it would also have been obvious to a person of ordinary skill in the art to combine all the combinations listed above with the Applicant Admitted Prior Art (“AAPA”) of the ’9893 patent. The ’9893 patent admits that systems on silicon and networks on chip are prior art, and that there were known motivations to use a NoC instead of a bus. *See, e.g.*, ’9893 patent at 1:14-48. For example, the ’9893 patent indicates that it was known that a NoC “resolve[s] the electrical problems in new deep-submicron technologies, as they structure and manager global wires” and a NoC “share[s] wires, lowering their number and increasing their utilization”. *Id. at* 1:39-41. The ’9893 patent also admits that is was known that NoCs are “energy efficient and reliable and are scalable compared to buses”. *Id.* at 1:41-42. The ‘9893 patent further admits that it was known that NoCs “decouple computation from communication, which is essential in managing the design of billion-transistor chips.” *Id.* at 43-45. The ’9893 patent also admits that off-chip network technology is related and applicable to on-chip networks. *See, e.g.*, ’9893 patent at 1:60-65. The ’9893 patent also admits that “transactions” comprising requests and responses were known in the art. *See, e.g.*, ’9893 patent at 2:57–3:5; *see also id*. at 9:51–54. Furthermore, the ’9893 patent admits that prior art protocols “allow transactions to be performed on

connections." *See, e.g.*, '449 patent at 2:57–3:5; *see also id*. at 10:27–29. To the extent the '9893 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, the AAPA of the '9893 patent would have provided additional motivation to combine according to the combinations listed above.

Chou "relates to a method and apparatus for a configurable address mapping and protection architecture and hardware for on-chip systems." Chou at 1:9–11. Chou teaches an on-chip system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Chou at 1:15–23, Fig. 3.

Similarly, Marietta teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Marietta at 2:22–3:42. Marietta teaches that this system may be implemented on a single integrated chip. *See, e.g.*, *id.* at 10:6–9.

It would have been obvious to combine Chou or Marietta with 2002 Goossens. Like Chou and Marietta, 2002 Goossens teaches an on-chip system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, 2002 Goossens at 423. In particular, 2002 Goossens teaches "a combination of circuit and packet switching, in the spirit of ATM." *See id.* at 425. "A channel implements a simplex point-to-point communication between two network interfaces (possibly with multiple paths)." *Id.* "A channel can have a combined throughput and latency guarantee (GT) . . . ." *Id.* "A connection combines multiple channels and can include flow control and reordering for lossless in-order (multicast) transmission." *Id.* 2002 Goossens teaches that such a system with guaranteed services offer many advantages over a system with best-effort services. *See, e.g.*, *id.* at 423.

It would also have been obvious to combine Chou or Marietta with Masri. Like Chou and Marietta, Masri teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Masri at 1:6–8, 1:26–46, Figs. 1–2. Masri teaches that this system may be implemented on a single integrated chip. *See, e.g.*, *id.* at 6:63–7:4, 7:54–56. Masri teaches a way to broadcast a message to all targets, *see, e.g.*, *id.* at 2:48–52, as well as a way to send a message to a narrower group of targets, *see, e.g.*, *id.* at 3:1–4:9, Figs. 5–7.

It would also have been obvious to combine Chou or Marietta with Weber. Like Chou and Marietta, Weber teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Weber at 15:30–16:21, Fig. 14. In particular, Weber teaches that "[p]rovision of per-thread flow control permits end-to-end performance guarantees to be determined across the interconnect." *Id.* at 15:30–32. Weber further teaches that "[e]nd-to-end data channels are linked using the threads of the interconnect, and per-thread flow control allows for end-to-end flow control between a particular initiator and target." *Id.* at 15:32–35.

It would also have been obvious to combine Chou or Marietta with 2003 Goossens. Like Chou and Marietta, 2003 Goossens teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, 2003 Goossens at 71–77. 2003 Goossens teaches communicating over connections, including simple, narrowcast, and multicast connections. *See id.* 2003 Goossens teaches various connection properties. *See, e.g.*, *id.* at 72–74.

It would also have been obvious to combine Chou or Marietta with Radulescu. Like Chou and Marietta, Radulescu teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Radulescu at 287–91. Radulescu teaches communicating over connections, including simple, narrowcast, and multicast connections. *See id.* Radulescu teaches various connection properties. *See, e.g.*, *id.* at 291–97.

It would have been obvious to combine Chou or Marietta with 2002 Goossens and Masri for substantially the same reasons it would have been obvious to combine Chou or Marietta with 2002 Goossens and it would have been obvious to combine Chou or Marietta with Masri.

It would have been obvious to combine CoreConnect with any one of the following: 2002 Goossens, Masri, Weber, 2003 Goossens, and Radulescu. CoreConnect discloses a high-performance interconnect technology to connect multiple modules on a single chip to form an SoC. Further, would have been obvious to combine CoreConnect and 2002 Goossens further with Masri. Further, would have been obvious to combine CoreConnect and Weber further with Masri. Like CoreConnect, Masri teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Masri at 1:6–8, 1:26–46, Figs. 1–2. Weber teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Weber at 15:30–16:21, Fig. 14. 2003 Goossens teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, 2003 Goossens at 71–77. Radulescu teaches a system in which multiple initiators communicate with multiple targets over a network. *See, e.g.*, Radulescu at 287–91.

It would also have been obvious to modify any of the references to replace any of their interconnects with a NoC based on the AAPA or Dally. In particular, the AAPA admits that NoCs were known and that there were known motivations to use a NoC for an interconnect in place of a bus. *See,* '9893 patent at 1:14-48. Dally also indicates that networks on chip are generally preferable to a bus because they have higher bandwidth and support multiple concurrent communications. *See* Dally at pp. 1.

It would also have been obvious to modify any of the references to combine discrete components together into a single integrated circuit ("IC") in the form of a system-on-chip

("SoC"). In particular, the text entitled *Modern VLSI Design: System-on-Chip Design, Third Edition* by Wayne Wolf explains that at the time of the patent, it was known that integrating discrete components onto an integrated circuit allowed designers "to build systems with many more transistors, allowing much more computing power to be applied to solving a problem." W. Wolf, *Modern VLSI Design: System-on-Chip Design, Third Edition*, Prentice Hall 2002 ("Wolf") at 1. Wolf teaches that integrated circuits are "much easier to design and manufacture and are more reliable than discrete systems," and that the small sizes of integrated circuits "leads to advantages in speed and power consumption, since smaller components have smaller parasitic resistances, capacitances, and inductances." *Id.* at 2. Wolf further explains, "Communication within a chip can occur hundreds of times faster than communication between chips on a printed circuit board" because on-chip circuits are smaller, and "smaller components and wires have smaller parasitic capacitances to slow down the signal." *Id.* Wolf notes that the small size of a device is "often an advantage in itself," and that replacing discrete components with a single chip reduces power consumption, which has ripple effects on the rest of the system. *Id*. at 3. For example, with reduced power consumption, a smaller and cheaper power supply can be used. *Id*. Lower power consumption means less heat, so a fan may no longer be necessary. *Id*. Finally, Wolf explains that reducing the number of components, power supply requirements, and so on will "inevitably reduce system cost." *Id*. Indeed, as Wolf explains, many motivations exist to combine discrete components together to form a single IC.

The Applicant's Admitted Prior Art (AAPA) in the '9893 patent also confirms that SoCs were previously known, and that it was known to combine discrete components together into a single IC in the form of an SoC, and thus the AAPA in the patent confirms it would have been obvious to modify any of the references to combine discrete components together into a single

IC in the form of an SoC. Specifically, the Applicant for the ’9893 patent explained that the alleged invention arose out of “a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions” in ICs and by “the increasing density with which components can be integrated on an integrated circuit.” ’9893 patent at 1:14-18.

The combinations of references provided are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendants may rely on such combination(s) in this litigation. In particular, Defendants are currently unaware of Plaintiff’s allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendants are also unaware of the extent, if any, to which Plaintiff may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendants as anticipatory, and the extent to which Plaintiff will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendants do not yet know how the Court will construe terms in the asserted claims. Defendants are also continuing its investigation of the universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Plaintiff may also be in possession of prior art that Defendants may receive as discovery progresses in this case. Defendants reserve the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

E. Disclosures For U.S. Patent No. 8,072,893

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits E-1 to E-21 demonstrate where each limitation of the claims is found in, either expressly or inherently in the larger context of the passage, or rendered obvious by, certain of the references listed below, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a) Prior Art Patents, Patent Publications, and Non-Patent Publications to the Asserted Claims of the '2893 patent.

Chart	Reference	Filing Date	Date of Issue or Publication	Citation	Claims
E-1	U.S. 7,200,137	July 29, 2002	Apr. 3, 2007	Dorr	Anticipated: 10 Obvious: 10
E-1	U.S. Pub. No. 2004/0017807	July 29, 2002	Jan. 29, 2004	Dorr	Anticipated: 10 Obvious: 10
E-2S	U.S. 6,081,844	Jan. 26, 1998	Jun. 27, 2000	Nowatzyk	Obvious: 10
E-3	D. Bertozzi *et al.*, *NoC Synthesis Flow for Customized Domain Specific Multiprocessor Systems-on-Chip*		Jan. 2005	Bertozzi	Anticipated: 10 Obvious: 10
E-4	M. Dall'Osso *et al.*, *Xpipes: a Latency Insensitive Parameterized Network-on-chip Architecture for Multi-Processor SoCs*		Oct. 13, 2003	Dall'Osso	Anticipated: 10 Obvious: 10

E-5S	D. Bertozzi *et al*., *Xpipes: A Network-on-Chip Architecture for Gigascale Systems-on-Chips*		Sep, 3, 2004	Xpipes	Anticipated: 10 Obvious: 10
E-6	K. Goossens, et al., *Networks on Silicon: Combining Best-Effort and Guaranteed Services*		2002	2002 Goossens	Obvious: 10
E-7	ARM AMBA Specification (Rev 2.0)		1999	AMBA 2 Spec.	Anticipated: 10 Obvious: 10
E-8	P. Kurup and T. Abbasi, *Logic Synthesis Using Synopsys* Second Edition		1997	Kurup	Anticipated: 10 Obvious: 10
E-9	J. Plosila et al, *Pipelined On-Chip Bus Architecture with Distributed Self-Timed Control*		2003	Plosila	Anticipated: 10 Obvious: 10
E-10	S. Winegarden, *Bus Architecture of a System on a Chip with User- Configurable System Logic*		2000	Winegarden	Anticipated: 10 Obvious: 10
E-11	D. Wingard and A. Kurosawa, *MicroNetwork-Based Integration of SOCs*		1998	Wingard	Anticipated: 10 Obvious: 10
E-12	L. Carloni et al., *Coping with Latency in SoC Design*		Dec. 10, 2002	Carloni	Obvious: 10
E-13S	Axel Jantsch and Hannu Tenhunen, *Networks on Chip*		January 2003	Jantsch	Anticipated: 10 Obvious: 10

E-14	Ron Ho, et al., *The Future of Wires*		April 2001	Ho	Obvious: 10
E-15	U.S. 7,085,913	Feb. 13, 2002	Aug. 1, 2006	Harding	Obvious: 10
E-16S	Soha Hassoun, et al., *Optimal Buffered Routing Path Constructions for Single and Multiple Clock Domain Systems*		Nov. 2002	Hassoun	Obvious: 10
E-17S	John Dielissen, et al., *Concepts and Implementation of the Philips Network-on-Chip*		Nov. 2003	Dielissen	Obvious: 10
E-18S	Jose Duato, et al., *Interconnection Networks an Engineering Approach*		1997	Duato	Obvious: 10
E-19S	Andrei Radulescu, et al., *An Efficient On-Chip NI Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration*		Jan. 2005	Radulescu 2005	Obvious: 10
E-20S	Pasquale Cocchini, *Concurrent Flip-Flop and Repeater Insertion for High Performance Integrated Circuits*		Nov. 2002	Cocchini	Obvious: 10

E-21S	U.S. 6,029,220	Oct. 8, 1992	Feb. 22, 2000	Iwamura	Obvious: 10

b) Prior Art Systems/Services To The Asserted Claims of the ’2893 Patent.

Defendants further identify the commercial embodiments of the inventions described in Exhibits E-1 to E-21, to the extent those systems or services were on sale or in public use before the priority date of the ’2893 patent. Moreover, on information and belief, XpipesCompiler was sold, offered for sale, and/or publicly used prior art for the ’2893 patent. Charts E-3, E-4, and E-5 demonstrate where each limitation of the claims is found in XpipesCompiler. On information and belief, System-on-chips products incorporating the AMBA 2 Specification were on sale, offered for sale or in public use before the priority date of the ’2893 patent. On information and belief, products incorporating design techniques disclosed in Wingard were on sale, offered for sale or in public use by Sonics before the priority date of the ’2893 patent. On information and belief, products designed using software tools that incorporate the design techniques disclosed Wingard were offered for sale, sold or used publicly by the customers of Sonics. Chart E-11 demonstrates where each limitation of the claims may be found in the products offered for sale by Sonics or in products designed using the software tools sold by Sonics. On information and belief, products incorporating design techniques disclosed in Kurup were on sale, offered for sale or publicly used by Synopsys before the priority date of the ’2893 patent. On information and belief, products designed using software tools that incorporate design techniques disclosed in Kurup were on sale, offered for sale or publicly used by customers of Synopsys before the priority date of the ’2893 patent. Chart E-8 demonstrates where each limitation of the claims may be found in

the products offered for sale by Synopsys or in products designed using the software tools sold by Synopsys.

2. Obviousness Combinations

A person having ordinary skill in the art would have been motivated to modify or combine the references described in attached Exhibits E-1 to E-21 with knowledge of a person of ordinary skill in the art and/or as listed below, or further as shown in the exemplary omnibus reference chart E-22, and for the reasons described below.

Reference	In Combination With	Claims
Dorr	AAPA	10
	2002 Goossens	10
	Nowatzyk	10
	Bertozzi	10
	Dall'Osso	10
	Xpipes	10
	AMBA 2 Spec	10
	Kurup	10
	Plosila	10
	Winegarden	10
	Wingard	10
	Jantsch	10
	Ho	10
	Hassoun	10
	Cocchini	10
	Iwamura	10
	Harding	10
	Carloni	10
Nowatzyk	AAPA	10
	2002 Goossens	10
	Dorr	10
	Radulescu 2005	10
	Dielissen	10
	Bertozzi	10
	Dall'Osso	10
	Xpipes	10
	AMBA 2 Spec	10
	Kurup	10
	Plosila	10
	Winegarden	10
	Wingard	10

		Carloni	10
		Jantsch	10
		Ho	10
		Hassoun	10
		Cocchini	10
		Iwamura	10
		AAPA and Bertozzi	10
		AAPA and Dall'Osso	10
		AAPA and Xpipes	10
		AAPA and AMBA 2 Spec	10
		AAPA and Kurup	10
		AAPA and Plosila	10
		AAPA and Winegarden	10
		AAPA and Wingard	10
		AAPA and Ho	10
		AAPA and Hassoun	10
		AAPA and Cocchini	10
		AAPA and Iwamura	10
		2002 Goossens and Bertozzi	10
		2002 Goossens and Dall'Osso	10
		2002 Goossens and Xpipes	10
		2002 Goossens and AMBA 2 Spec	10
		2002 Goossens and Kurup	10
		2002 Goossens and Plosila	10
		2002 Goossens and Winegarden	10
		2002 Goossens and Wingard	10
		2002 Goossens and Ho	10
		2002 Goossens and Hassoun	10
		2002 Goossens and Cocchini	10
		2002 Goossens and Iwamura	10
		Jantsch and Bertozzi	10
		Jantsch and Dall'Osso	10
		Jantsch and Xpipes	10
		Jantsch and AMBA 2 Spec	10
		Jantsch and Kurup	10
		Jantsch and Plosila	10
		Jantsch and Winegarden	10
		Jantsch and Wingard	10
		Jantsch and Hassoun	10
		Jantsch and Cocchini	10
		Jantsch and Iwamura	10
		Jantsch and Ho	10
		Jantsch and Hassoun	10
		Jantsch and Cocchini	10
		Jantsch and Iwamura	10
		Dielissen and Bertozzi	10
		Dielissen and Dall'Osso	10

	Dielissen and Xpipes	10
	Dielissen and AMBA 2 Spec	10
	Dielissen and Kurup	10
	Dielissen and Plosila	10
	Dielissen and Winegarden	10
	Dielissen and Wingard	10
	Dielissen and Ho	10
	Dielissen and Hassoun	10
	Dielissen and Cocchini	10
	Dielissen and Iwamura	10
	Radulescu 2005 and Bertozzi	10
	Radulescu 2005 and Dall'Osso	10
	Radulescu 2005 and Xpipes	10
	Radulescu 2005 and AMBA 2 Spec	10
	Radulescu 2005 and Kurup	10
	Radulescu 2005 and Plosila	10
	Radulescu 2005 and Winegarden	10
	Radulescu 2005 and Wingard	10
	Radulescu 2005 and Ho	10
	Radulescu 2005 and Hassoun	10
	Radulescu 2005 and Cocchini	10
	Radulescu 2005 and Iwamura	10
2002 Goossens	AAPA	10
	Dorr	10
	Nowatzyk	10
	Bertozzi	10
	Dall'Osso	10
	Xpipes	10
	AMBA 2 Spec	10
	Kurup	10
	Plosila	10
	Winegarden	10
	Wingard	10
	Harding	10
	Carloni	10
	Ho	10
	Hassoun	10
	Cocchini	10
	Iwamura	10
	Dorr and Carloni	10
	Dorr and Nowatzyk	10
	Nowatzyk and Carloni	10
Bertozzi	AAPA	10
	AMBA 2 Spec	10
	Kurup	10
	Plosila	10
	Winegarden	10

	Wingard	10
	Ho	10
	Hassoun	10
	Cocchini	10
	Iwamura	10
	Nowatzyk	10
	Jantsch	10
	Duato	10
	Jantsch and Duato	10
	Jantsch and Nowatzyk	10
	Duato and Nowatzyk	10
	Jantsch, Duato and Nowatzyk	10
	Dall'Osso and Xpipes	10
Dall'Osso	AAPA	10
	AMBA 2 Spec	10
	Kurup	10
	Plosila	10
	Winegarden	10
	Wingard	10
	Ho	10
	Hassoun	10
	Cocchini	10
	Iwamura	10
	Nowatzyk	10
	Jantsch	10
	Duato	10
	Jantsch and Duato	10
	Jantsch and Nowatzyk	10
	Duato and Nowatzyk	10
	Jantsch, Duato and Nowatzyk	10
	Dall'Osso and Xpipes	10
Xpipes	AAPA	10
	AMBA 2 Spec	10
	Kurup	10
	Plosila	10
	Winegarden	10
	Wingard	10
	Ho	10
	Hassoun	10
	Cocchini	10
	Iwamura	10
	Nowatzyk	10
	Jantsch	10
	Duato	10
	Jantsch and Nowatzyk	10
	Duato and Nowatzyk	10

	Jantsch, Duato and Nowatzyk	10
	Jantsch and Duato	10
	Dall'Osso and Bertozzi	10
Winegarden	Kurup	10
	Wingard	10
Jantsch	AAPA	10
	Dorr	10
	Nowatzyk	10
	Bertozzi	10
	Dall'Osso	10
	Xpipes	10
	AMBA 2 Spec	10
	Kurup	10
	Plosila	10
	Winegarden	10
	Wingard	10
	Harding	10
	Carloni	10
	Ho	10
	Hassoun	10
	Cocchini	10
	Iwamura	10
	Dorr and Carloni	10
	Dorr and Nowatzyk	10
	Nowatzyk and Carloni	10
Dielissen	AAPA	10
	Hassoun	10
	Cocchini	10
	Iwamura	10
	Bertozzi	10
	Dall'Osso	10
	Xpipes	10
	Nowatzyk	10
	Dorr	10
	AMBA 2 Spec	10
	Kurup	10
	Plosila	10
	Winegarden	10
	Wingard	10
	Harding	10
	Carloni	10
	Ho	10
	Hassoun and Nowatzyk	10
	Cocchini and Nowatzyk	10
	Iwamura and Nowatzyk	10
	Bertozzi and Nowatzyk	10

	Dall'Osso and Nowatzyk	10
	Xpipes and Nowatzyk	10
Radulescu 2005	AAPA	10
	Hassoun	10
	Cocchini	10
	Iwamura	10
	Bertozzi	10
	Dall'Osso	10
	Xpipes	10
	Nowatzyk	10
	Dorr	10
	AMBA 2 Spec	10
	Kurup	10
	Plosila	10
	Winegarden	10
	Wingard	10
	Harding	10
	Carloni	10
	Ho	10
	Hassoun and Nowatzyk	10
	Cocchini and Nowatzyk	10
	Iwamura and Nowatzyk	10
	Bertozzi and Nowatzyk	10
	Dall'Osso and Nowatzyk	10
	Xpipes and Nowatzyk	10

A person having ordinary skill in the art at the time of filing of the '2893 patent would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them. It would have been obvious to a person of ordinary skill in the art at the time of the alleged invention to combine a reference with one or more of the other references for the following reasons:

- Combining the prior art limitations according to known methods would have yielded predictable results.
- Simple substitution of one known limitation for another would have yielded predictable results.

- Use of known technique to improve similar devices in the same way would have been obvious.
- Applying a known technique to a known device ready for improvement would have yielded predictable results.
- References disclosing these concepts teach the beneficial utility of them, including as cited in the claim charts submitted herewith.

In addition, a person of ordinary skill in the art would have been motivated to make the combinations based on the general industry trends and other considerations discussed in connection with the state of the art. For example, as explained above in Section IV that describes the state of the art prior to the alleged dates of alleged inventions in the Asserted Patents, the industry was moving towards using system-on-chips (SoCs). Mirroring the general trend of higher integration with time (e.g., Moore's Law), the SoCs were integrating greater number of modules all on one chip. A person of skill in the art was aware of the need for interconnection networks to connect the modules on a single chip as well as they traditionally connected modules on different chips. As further explained in Section IV, researchers were advocating the need to adopt principles and techniques from computer networking domains in the context of SoCs. A person of ordinary skill in the art would have been aware of such trends and suggestions to incorporate techniques from closely-related domains to address and overcome challenges in the SoC arena.

A person of ordinary skill in the art at the time of the alleged invention would have combined the references because each generally relates to similar technology (e.g., Dorr at 3:56-58; Nowatzyk at 2:19-27; AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Bertozzi at 113; Dall'Osso at 2; 2002 Goossens at 423; Harding at Abstract, 7:12-

28; Carloni at 24-27; Ho at 490, 491; Jantsch at 61, 193; Hassoun at 247; Dielissen at 1; Duato at 1; Radulescu 2005 at 4; Cocchini at 268; Iwamura at 1:6-9). A person of skill in the art also would have been motivated to combine references in order to obtain the benefits of one prior art device, system or method in another device, system or method.

Moreover, it would also have been obvious to a person of ordinary skill in the art to combine all the combinations listed above with the Applicant Admitted Prior Art ("AAPA") of the '2893 patent. The '2893 patent admits that systems on silicon and networks on chip are prior art. *See, e.g.*, '2893 patent at 1:8–33. The '2893 patent also admits that "[s]uch networks typically comprise a plurality of network stations, each associated with a functional block, interconnected via communication channels, e.g. wires" and that "the plurality of network stations include a plurality of data routers and a plurality of network interfaces, each data router being coupled to a functional block via a network interface." *Id*.; *see also id*. at 4:25–44. In addition, the '2893 patent admits that it was known in the art to "introduce a data storage element such as a latch" into communication channels in order to introduce delay. '2893 patent at 1:34–46. The '2893 patent also admits that prior art networks "operate[d] on the principle that a network station such as a data router receives [] routing data incorporated in [a] data packet during a predefined clock cycle." '2893 patent at 1:47–61. In addition, the '2893 patent admits that "known communication techniques" involved storing "a complete data stream" in a router "before it is forward to its next destination." '2893 patent at 4:58–67. The '2893 patent also admits that identifying a "data transfer delay exceeding a predetermined delay threshold" can be done using "available timing behaviour simulation tools." '2893 patent at 5:43–49. To the extent the '2893 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques

identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, the AAPA of the ’2893 patent would have provided additional motivation to combine according to the combinations listed above.

A person of ordinary skill in the art at the time of the alleged invention would have understood that each of the Bertozzi, Dall’Osso and Xpipes references (collectively, the “Xpipes Compiler References”) discloses the same Xpipes architecture that is a scalable and high-performance NoC architecture for multi-processor SoCs. The architecture employs the well-known concept of pipelining to propose a pipelined switch-to-switch architecture that breaks a long path into shorter path to meet timing criteria specified for a design. Each of the Xpipes Compiler References discloses an integrated circuit comprising multiple functional blocks interconnected by a pipelined data communication network (e.g., Bertozzi at 113; Dall’Osso at 1, and Xpipes at 19). In particular, a person of ordinary skill in the art would have combined the three references. Combining these teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Bertozzi discloses “a complete synthesis flow, called NetChip, for customized NoC architectures.” Bertozzi at 113. Bertozzi teaches an integrated circuit containing multiple functional elements communicating with each other over a common interconnect. *See, e.g.*, Bertozzi at 113, Fig. 1. Dall’Osso discloses “a scalable and high-performance NoC architecture for multi-processor SoCs.” Dall’Osso at 1. Dall’Osso teaches an integrated circuit containing multiple functional elements communicating with each other over a common interconnect. *See, e.g.*, Dall’Osso at 2, Figure 1. Xpipes discloses a network-on-chip “targeting high performance and reliable communication for on-chip multi-processors.” Xpipes

at 18. Xpipes teaches an integrated circuit containing multiple functional elements communicating with each other over a common interconnect. *See, e.g.*, Xpipes at 19, Figure 1.

A person of ordinary skill in the art at the time of the alleged invention would have understood that each of the AMBA 2 Spec, Kurup, Plosila, Winegarden, Wingard, Ho, Hassoun, Cocchini, and Iwamura references (collectively, the "Pipelining References") discloses the same well-known concept of "pipelining," in which a long signal path in an integrated circuit is split into multiple shorter paths (a "multicycle" path) in order to satisfy the timing constraints of the underlying system-on-chip. Each of the Pipelining References discloses an integrated circuit comprising multiple functional blocks interconnected by a pipelined data communication network (*e.g.*, AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Ho at 491; Hassoun 248-249; Cocchini at 268; Iwamura at 3:10-24). In particular, a person of ordinary skill would have combined Winegarden with Kurup and Winegarden with Wingard for the reasons stated herein. Combining these teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Similarly, the AMBA 2 Spec teaches a "high performance system backbone bus" for communication between functional elements on a system-on-chip. *See, e.g.*, AMBA 2 Spec at 1-4 and Figure 1-1. The AMBA 2 Spec teaches that the system bus may be pipelined. *See, e.g.*, AMBA 2 Spec at 1-4 to 1-5. Similarly, Plosila teaches an "efficient and reliable interconnect strategy [] for combining the constituent subsystems on a single chip in such a way that sufficient system performance is obtained with an acceptable design effort." Plosila at 257. Plosila teaches that the interconnect may be pipelined. *See, e.g.*, Plosila at 257-259, FIG. 3. Similarly, Winegarden teaches a "dedicated internal system bus" for interconnecting system peripherals in a system-on-chip. Winegarden at 425.

Winegarden teaches that the system bus may be pipelined. *See, e.g.*, Winegarden at 426 and FIG. 2. Similarly, Wingard discloses "an on-chip network as the fundamental communication architecture for a complex SoC design." Wingard at Abstract. Wingard teaches that the network datapath may be pipelined. *See, e.g.*, Wingard at 5.2. Similarly, Kurup teaches fundamental principles of datapath design within an integrated circuit. *See, e.g.*, Kurup at 1. Kurup teaches that a datapath in an integrated circuit may be pipelined. *See, e.g.*, Kurup at 286. Ho similarly teaches the use of repeaters within global wires in order to make wire delays scale with the length of the wire. Ho at 490. Such repeaters also allow for substantial increases in bandwidth. Ho at 496. Hassoun teaches "inserting synchronization elements (such as registers) along the signal path." Hassoun at 248-249. Cocchini teaches the insertion of "flip-flops and repeaters in VLSI circuits." Cocchini at 268. Iwamura discloses a pipelined divided transmission unit. Iwamura at Abstract; 3:10-24.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Dorr with any one of the Pipelining References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Dorr at 1:21-25, 2:36-40; AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Ho at 491; Hassoun at 248-249; Cocchini at 268; Iwamura at 3:10-24). A POSITA would have been motivated to make such a combination in order to satisfy timing constraints of the underlying system-on-chip and improve throughput. Combining these teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. In addition, it would have been obvious to combine Dorr with Nowatzyk, Harding, or Carloni, each of which describes identifying and compensating for a delay in a communication channel (*e.g.*, Nowatzyk

at 11:55-12:2; Harding at 7:12-28; Carloni at 24-27). A POSITA would have been motivated to make such a combination as identifying and compensating for delays in a communication channel allows for improved bandwidth and throughput over such a channel. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Dorr with any one of the Xpipes Compiler References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Dorr at 1:21-25, 2:36-40; Bertozzi at 113; Dall'Ossa at 1, and Xpipes at 19). A POSITA would have been motivated to make such a combination. The Xpipes Compiler References teach a synthesis tool for instantiating and synthesizing an on chip interconnect with modular components. It allows for pipelined links between switches that break long paths into shorter paths to meet timing criteria of the design and improve throughput. Using the known methods taught by the Xpipes Compiler References would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Nowatzyk with 2002 Goossens, Jantsch, Dielissen, or Radulescu 2005 because each relates to similar technology involving communications between functional elements (*e.g.*, Nowatzyk at 2:19-27, 2002 Goossens at 423; Jantsch at 193; Dielissen at 1; Radulescu 2005 at 4). A POSITA would have been motivated to make such a combination in order to make networks interconnecting the various components smaller, more reliable, and more efficient. On chip networks require less energy to transfer data between components and are highly reliable. In addition, it would have been obvious to combine Nowatzyk with Harding and/or Carloni, each of

which describes identifying and compensating for a delay in a communication channel (*e.g.*, Harding at 7:12-28; Carloni at 24-27). A POSITA would have been motivated to make such a combination as identifying and compensating for delays in a communication channel allows for improved bandwidth and throughput over such a channel. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. In addition, it would have been obvious to combine Nowatzyk; Nowatzyk and 2002 Goossens; Nowatzyk and Jantsch; Nowatzyk at Dielissen; or Nowatzyk and Radulescu 2005 with any one of the Pipelining References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Nowatzyk at 2:22-27; 2002 Goossens at 423; Jantsch at 193; AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Ho at 491; Hassoun 248-249; Cocchini at 268; Iwamura at 3:10-24). A POSITA would have been motivated to make such a combination in order to satisfy timing constraints of the underlying system-on-chip and improve throughput. Combining these teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. It would also have been obvious to combine Nowatzyk; Nowatzyk and 2002 Goossens; or Nowatzyk and Jantach with any one of the Xpipes Compiler References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Nowatzyk at 2:22-27; 2002 Goossens at 423; Jantsch at 193; Bertozzi at 113; Dall'Osso at 1, and Xpipes at 19). A POSITA would have been motivated to make such a combination. The Xpipes Compiler References teach a synthesis tool for instantiating and synthesizing an on chip interconnect with modular components. It allows for pipelined links between switches that break long paths into shorter paths to meet timing criteria

of the design and improve throughput. Using the known methods taught by the Xpipes Compiler References would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Bertozzi with any one of the Pipelining References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Bertozzi at 113; AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Ho at 491; Ho at 491; Hassoun 248-249; Cocchini at 268; Iwamura at 3:10-24). A POSITA would have been motivated to make such a combination in order to satisfy timing constraints of the underlying system-on-chip and improve throughput. Combining these teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Moreover, to the extent the ’2893 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Dall’Osso with any one of the Pipelining References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Dall’Osso at 2, Figure 1; AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Ho at 491; Hassoun 248-249; Cocchini at 268; Iwamura at 3:10-24). A POSITA would have been motivated to make such a combination in order to satisfy timing constraints of the underlying system-on-chip and improve throughput. Combining these

teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Xpipes with any one of the Pipelining References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Xpipes at 19, Figure 1; AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Ho at 491; Hassoun 248-249; Cocchini at 268; Iwamura at 3:10-24). A POSITA would have been motivated to make such a combination in order to satisfy timing constraints of the underlying system-on-chip and improve throughput. Combining these teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine 2002 Goossens with any one of the Xpipes Compiler References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, 2002 Goossens at 423; Bertozzi at 113; Dall'Osso at 1; and Xpipes at 19). A POSITA would have been motivated to make such a combination. The Xpipes Compiler References teach a synthesis tool for instantiating and synthesizing an on chip interconnect with modular components. It allows for pipelined links between switches that break long paths into shorter paths to meet timing criteria of the design and improve throughput. Using the known methods taught by the Xpipes Compiler References would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been

obvious. In addition, it would have been obvious to combine 2002 Goossens with Nowatzyk, Harding, and/or Carloni, each of which describes identifying and compensating for a delay in a communication channel (*e.g.*, Nowatzyk at 11:55-12:2; Harding at 7:12-28; Carloni at 24-27). A POSITA would have been motivated to make such a combination as identifying and compensating for delays in a communication channel allows for improved bandwidth and throughput over such a channel. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine 2002 Goossens with any one of the Pipelining References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, 2002 Goossens at 423, Figure 1; AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Ho at 491; Hassoun 248-249; Cocchini at 268; Iwamura at 3:10-24). A POSITA would have been motivated to make such a combination in order to satisfy timing constraints of the underlying system-on-chip and improve throughput. Combining these teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Jantsch with any one of the Xpipes Compiler References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Jantsch at 193; Bertozzi at 113; Dall'Osso at 1, and Xpipes at 19). A POSITA would have been motivated to make such a combination. The Xpipes Compiler References teach a

synthesis tool for instantiating and synthesizing an on chip interconnect with modular components. It allows for pipelined links between switches that break long paths into shorter paths to meet timing criteria of the design and improve throughput. Using the known methods taught by the Xpipes Compiler References would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. In addition, it would have been obvious to combine Jantsch with Nowatzyk, Harding, and/or Carloni, each of which describes identifying and compensating for a delay in a communication channel (*e.g.*, Nowatzyk at 11:55-12:2; Harding at 7:12-28; Carloni at 24-27). A POSITA would have been motivated to make such a combination as identifying and compensating for delays in a communication channel allows for improved bandwidth and throughput over such a channel. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Jantsch with any one of the Pipelining References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Jantsch at 193, Figure 1; AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Ho at 491; Hassoun 248-249; Cocchini at 268; Iwamura at 3:10-24). A POSITA would have been motivated to make such a combination in order to satisfy timing constraints of the underlying system-on-chip and improve throughput. Combining these teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Dielissen with any one of the Xpipes Compiler References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Dielissen at 1; Bertozzi at 113; Dall'Osso at 1; and Xpipes at 19). A POSITA would have been motivated to make such a combination. The Xpipes Compiler References teach a synthesis tool for instantiating and synthesizing an on chip interconnect with modular components. It allows for pipelined links between switches that break long paths into shorter paths to meet timing criteria of the design and improve throughput. Using the known methods taught by the Xpipes Compiler References would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. In addition, it would have been obvious to combine Dielissen (or a combination involving Dielissen) with Nowatzyk, Harding, and/or Carloni, each of which describes identifying and compensating for a delay in a communication channel (*e.g.*, Nowatzyk at 11:55-12:2; Harding at 7:12-28; Carloni at 24-27). A POSITA would have been motivated to make such a combination as identifying and compensating for delays in a communication channel allows for improved bandwidth and throughput over such a channel. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Dielissen with any one of the Pipelining References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Dielissen at 1, Figs. 1 and 11; AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Ho at 491; Hassoun at 248-249; Cocchini at 268; Iwamura at

3:10-24). A POSITA would have been motivated to make such a combination in order to satisfy timing constraints of the underlying system-on-chip and improve throughput. Combining these teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Radulescu 2005 with any one of the Xpipes Compiler References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Radulescu 2005 at 4; Bertozzi at 113; Dall'Osso at 1; and Xpipes at 19). A POSITA would have been motivated to make such a combination. The Xpipes Compiler References teach a synthesis tool for instantiating and synthesizing an on chip interconnect with modular components. It allows for pipelined links between switches that break long paths into shorter paths to meet timing criteria of the design and improve throughput. Using the known methods taught by the Xpipes Compiler References would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. In addition, it would have been obvious to combine Radulescu 2005 (or a combination involving Radulescu 2005) with Nowatzyk, Harding, and/or Carloni, each of which describes identifying and compensating for a delay in a communication channel (*e.g.*, Nowatzyk at 11:55-12:2; Harding at 7:12-28; Carloni at 24-27). A POSITA would have been motivated to make such a combination as identifying and compensating for delays in a communication channel allows for improved bandwidth and throughput over such a channel. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Radulescu 2005 with any one of the Pipelining References because each relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Radulescu 2005 at 4, Figs. 1, 5, 21; AMBA 2 Spec at 1-2; Kurup at 1; Plosila at 257; Winegarden at 425; Wingard at 3; Ho at 491; Hassoun 248-249; Cocchini at 268; Iwamura at 3:10-24). A POSITA would have been motivated to make such a combination in order to satisfy timing constraints of the underlying system-on-chip and improve throughput. Combining these teachings of pipelining according to known methods would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Winegarden with either Kurup or with Wingard. Each of these references relates to similar technology involving communications between functional elements in a system-on-chip (*e.g.*, Kurup at 1; Winegarden at 425; Wingard at 3). Each of these references also discusses how to meet timing requirements of connections during the design of an SoC.

Xpipes anticipates the ’2893 Patent for at least the reasons explained in IPR2024-00355 and supporting exhibits, including the expert declaration of Dr. Marwan Hassoun. The combination of Xpipes and Jantsch and/or Duato renders the ’2893 Patent obvious for at least the reasons explained in IPR2024-00355 and supporting exhibits, including the expert declaration of Dr. Marwan Hassoun. The combination of Dielissen and Hassoun renders the ’2893 Patent obvious for at least the reasons explained in IPR2024-00355 and supporting exhibits, including the expert declaration of Dr. Marwan Hassoun.

It would also have been obvious to modify any of the references to combine discrete components together into a single integrated circuit ("IC") in the form of a system-on-chip ("SoC"). In particular, the text entitled *Modern VLSI Design: System-on-Chip Design, Third Edition* by Wayne Wolf explains that at the time of the patent, it was known that integrating discrete components onto an integrated circuit allowed designers "to build systems with many more transistors, allowing much more computing power to be applied to solving a problem." W. Wolf, *Modern VLSI Design: System-on-Chip Design, Third Edition*, Prentice Hall 2002 ("Wolf") at 1. Wolf teaches that integrated circuits are "much easier to design and manufacture and are more reliable than discrete systems," and that the small sizes of integrated circuits "leads to advantages in speed and power consumption, since smaller components have smaller parasitic resistances, capacitances, and inductances." *Id.* at 2. Wolf further explains, "Communication within a chip can occur hundreds of times faster than communication between chips on a printed circuit board" because on-chip circuits are smaller, and "smaller components and wires have smaller parasitic capacitances to slow down the signal." *Id.* Wolf notes that the small size of a device is "often an advantage in itself," and that replacing discrete components with a single chip reduces power consumption, which has ripple effects on the rest of the system. *Id*. at 3. For example, with reduced power consumption, a smaller and cheaper power supply can be used. *Id*. Lower power consumption means less heat, so a fan may no longer be necessary. *Id*. Finally, Wolf explains that reducing the number of components, power supply requirements, and so on will "inevitably reduce system cost." *Id*. Indeed, as Wolf explains, many motivations exist to combine discrete components together to form a single IC.

The Applicant's Admitted Prior Art (AAPA) in the '2893 patent also confirms that SoCs were previously known, and that it was known to combine discrete components together into a

single IC in the form of an SoC, and thus the AAPA in the patent confirms it would have been obvious to modify any of the references to combine discrete components together into a single IC in the form of an SoC. Specifically, when describing the alleged invention's motivations, the Applicant for the '2893 patent explained that "[n]owadays, most integrated circuits (ICs) are very large scale integration (VLSI) circuits having a large number of features that typically implement a large number of functions on board the IC," and that and IC's "various functions may be located in discrete functional blocks, e.g. system on chip (SoC) architectures." '2893 patent at 1:14-18.

The combinations of references provided are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible, and Defendants may rely on such combination(s) in this litigation. In particular, Defendants are currently unaware of Plaintiff's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendants are also unaware of the extent, if any, to which Plaintiff may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendants as anticipatory, and the extent to which Plaintiff will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendants do not yet know how the Court will construe terms in the asserted claims. Defendants are also continuing its investigation of the universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Plaintiff may also be in possession of prior art that Defendants may receive as discovery progresses in this case. Defendants reserve the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

F. Disclosures For U.S. Patent 8,086,800

1. Identification of Prior Art

The tables below list prior art that anticipates and/or renders obvious one or more of the asserted claims. The attached claim charts in Exhibits F-1 to F-22 demonstrate where each limitation of the claims is found in, either expressly or inherently in the larger context of the passage, or rendered obvious by, certain of the references listed below, as understood by a person having ordinary skill in the art. The following patents, publications, products and/or services are prior art under at least 35 U.S.C. §§ 102(a), (b), or (e).

a) Prior Art Patents, Patent Publications, and Non-Patent Publications to the Asserted Claims of the '800 patent.

Chart	Reference	Filing Date	Date of Issue or Publication	Citation	Claims
F-1S	U.S. 5,434,872	July 28, 1992	July 18, 1995	Petersen	Obvious: 12
F-2S	WIPO Pub. No. 2004/034176	Oct. 7, 2003	Apr. 22, 2004	Radulescu II	Anticipated: 12 Obvious: 12
F-3	L. Peh, *Flow Control and Micro-Architectural Mechanisms for Extending the Performance of Interconnection Networks*		August 2001	Peh	Obvious: 12
F-4	Axel Jantsch and Hannu Tenhunen, *Networks on Chip*		2003	Jantsch	Anticipated: 12 Obvious: 12

F-5	E. Rijpkema, et al., *Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip*		March 2003	Rijpkema	Anticipated: 12 Obvious: 12
F-6	Andrei Radulescu and Kees Goossens, *Communication Services for Networks on Chip*		January 2003	Radulescu	Anticipated: 12 Obvious: 12
F-7	Kenichiro Anjo, et al., *Wrapper-Based Bus Implementation Techniques for Performance Improvement and Cost Reduction*		May 4, 2004	Anjo	Obvious: 12
F-8	U.S. Pat. No. 6,393,500	Aug. 12, 1999	May 21, 2002	Thekkath	Obvious: 12
F-9	Li-Shiuan Peh and William J. Dally, *Flit-Reservation Flow Control*		January 2000	Peh II	Obvious: 12
F-10	U.S. Pat. No. 6,397,287	Jan. 27, 1999	May 28, 2002	Brown	Obvious: 12
F-11	U.S. Pat. No. 6,615,308	Dec. 9, 1999	Sep. 2, 2003	Fanning	Obvious: 12
F-12	U.S. Pat. No. 6,490,630	Apr. 2, 1999	Dec. 3, 2002	Poon	Obvious: 12
F-13	Ilkka Saastamoinen, et al., Buffer Implementation for Proteo Networks-on-Chip		2003	Saastamoinen	Obvious: 12

F-14	Cesar Albenes Zeferino, et al., *SoCIN: A Parametric and Scalable Network-on-Chip*		2003	Zeferino	Obvious: 12
F-15	Praveen Vellanki, et al., *Quality-of-Service and Error Control Techniques for Network-on-Chip Architectures*		April 2004	Vellanki	Obvious: 12
F-16	Evegeny Bolotin, et al., *QNoC: QoS architecture and design process for network on chip*		February 2004	Bolotin	Obvious: 12
F-17	Praveen Bhojwani and Rabi Mahapatra, *Interfacing Cores with On-chip Packet-Switched Networks*		2003	Bhojwani	Obvious: 12
F-18	J. Dielissen, et al., *Concepts and Implementation of the Philips Network- on-Chip*		Jan. 2004	Dielissen	Anticipated: 12 Obvious: 12
F-19S	Andrei Radulescu, et al, *An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration*		Feb. 2004	Radulescu III	Anticipated: 12 Obvious: 12

F-20S	U.S. Pat. App. No. 2002/0186660	Jun. 12, 2001	Dec. 12, 2002	Bahadiroglu	Anticipated: 12 Obvious: 12
F-21S	U.S. Pat. No. 6,769,030	Feb. 7, 2000	July. 27, 2004	Bournas	Anticipated: 12 Obvious: 12
F-22S	U.S. Pat. No. 7,355,971	Oct. 22, 2001	Apr. 8, 2008	Jason	Anticipated: 12 Obvious: 12

b) Prior Art Systems/Services to the Asserted Claims of the ’800 patent.

Defendants further identify the commercial embodiments of the inventions described in Exhibits F-1 to F-22, to the extent those systems or services were on sale or in public use before the priority date of the ’800 patent.

2. Obviousness Combinations

A person having ordinary skill in the art would have been motivated to modify or combine the references described in attached Exhibits F-1 to F-22 with knowledge of a person of ordinary skill in the art and/or as listed below, or further as shown in the exemplary omnibus reference chart F-23, and for the reasons described below.

Reference	In Combination With	Claims
Radulescu II	AAPA Petersen Anjo Poon Saastamoinen	12 12 12 12 12

	Thekkath	12
	Fanning	12
	Brown	12
	Bolotin	12
	Jantsch	12
	Radulescu I	12
	Radulescu III	12
	Rijkema	12
	Dielissen	12
	Zeferino	12
	Vellanki	12
	Peh	12
	Peh II	12
	Bahadiroglu	12
	Bournas	12
	Jason	12
	Peh and Poon	12
	Peh II and Poon	12
	Peh and Petersen	12
	AAPA and Petersen	12
	AAPA and Peh	12
Petersen	AAPA	12
	Radulescu II	12
	AAPA and Radulescu II	12
Peh	AAPA	12
	Radulescu I	12
	Radulescu II	12
	Radulescu III	12
	AAPA and Radulescu II	12
	Jantsch	12
	Rijpkema	12
	Dielissen	12
	Bolotin	12
	Bhojwani	12
	Radulescu I and Bhojwani	12
	Bahadiroglu	12
	Bournas	12
	Jason	12
	Bahadiroglu and Radulescu II	12
	Petersen and Radulescu II	12
Radulescu I	AAPA	12
	Petersen	12
	Anjo	12
	Poon	12
	Saastamoinen	12
	Thekkath	12
	Fanning	12

	Brown	12
	Bolotin	12
	Jantsch	12
	Radulescu II	12
	Radulescu III	12
	Rijkema	12
	Dielissen	12
	Zeferino	12
	Vellanki	12
	Peh	12
	Peh II	12
	Bahadiroglu	12
	Bournas	12
	Jason	12
	Bahadiroglu and Radulescu II	12
	Petersen and Radulescu II	12
	Peh and Poon	12
	Peh II and Poon	12
	Peh and Bhojwani	12
	Peh and Petersen	12
	AAPA and Petersen	12
	AAPA and Peh	12
Jantsch	AAPA	12
	Petersen	12
	Anjo	12
	Poon	12
	Saastamoinen	12
	Thekkath	12
	Fanning	12
	Brown	12
	Bolotin	12
	Radulescu I	12
	Radulescu II	12
	Radulescu III	12
	Rijkema	12
	Dielissen	12
	Zeferino	12
	Vellanki	12
	Peh	12
	Peh II	12
	Bahadiroglu	12
	Bournas	12
	Jason	12
	Bahadiroglu and Radulescu II	12
	Petersen and Radulescu II	12
	Peh and Poon	12

	Peh II and Poon	12
	Peh and Petersen	12
	AAPA and Petersen	12
	AAPA and Peh	12
Rijkema	AAPA	12
	Petersen	12
	Anjo	12
	Poon	12
	Saastamoinen	12
	Thekkath	12
	Fanning	12
	Brown	12
	Bolotin	12
	Radulescu I	12
	Radulescu II	12
	Radulescu III	12
	Dielissen	12
	Zeferino	12
	Vellanki	12
	Peh	12
	Peh II	12
	Bahadiroglu	12
	Bournas	12
	Jason	12
	Bahadiroglu and Radulescu II	12
	Petersen and Radulescu II	12
	Peh and Poon	12
	Peh II and Poon	12
	Peh and Petersen	12
	AAPA and Petersen	12
	AAPA and Peh	12
Dielissen	AAPA	12
	Petersen	12
	Anjo	12
	Poon	12
	Saastamoinen	12
	Thekkath	12
	Fanning	12
	Brown	12
	Bolotin	12
	Radulescu I	12
	Radulescu II	12
	Radulescu III	12
	Rijkema	12
	Zeferino	12
	Vellanki	12

	Peh	12
	Peh II	12
	Bahadiroglu	12
	Bournas	12
	Jason	12
	Bahadiroglu and Radulescu II	12
	Petersen and Radulescu II	12
	Peh and Poon	12
	Peh II and Poon	12
	Peh and Petersen	12
	AAPA and Petersen	12
	AAPA and Peh	12
Radulescu III	AAPA	12
	Petersen	12
	Anjo	12
	Poon	12
	Saastamoinen	12
	Thekkath	12
	Fanning	12
	Brown	12
	Bolotin	12
	Radulescu I	12
	Radulescu II	12
	Dielissen	12
	Rijkema	12
	Zeferino	12
	Vellanki	12
	Peh	12
	Peh II	12
	Bahadiroglu	12
	Bournas	12
	Jason	12
	Bahadiroglu and Radulescu II	12
	Petersen and Radulescu II	12
	Peh and Poon	12
	Peh II and Poon	12
	Peh and Petersen	12
	AAPA and Petersen	12
	AAPA and Peh	12

A person having ordinary skill in the art at the time of filing of the ’800 patent would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them. It would have been obvious to a

person of ordinary skill in the art at the time of the alleged invention to combine a reference with one or more of the other references for the following reasons:

- Combining the prior art limitations according to known methods would have yielded predictable results.
- Simple substitution of one known limitation for another would have yielded predictable results.
- Use of known technique to improve similar devices in the same way would have been obvious.
- Applying a known technique to a known device ready for improvement would have yielded predictable results.
- References disclosing these concepts teach the beneficial utility of them, including as cited in the claim charts submitted herewith.

In addition, a person of ordinary skill in the art would have been motivated to make the combinations based on the general industry trends and other considerations discussed in connection with the state of the art. For example, as explained above in Section IV that describes the state of the art prior to the alleged dates of alleged inventions in the Asserted Patents, the industry was moving towards using system-on-chips (SoCs). Mirroring the general trend of higher integration with time (also referred to as Moore's Law), the SoCs were integrating a greater number of modules all on one chip. A person of skill in the art was aware of the need for interconnection networks to connect the modules on a single chip as well as they traditionally connected modules on different chips. As further explained in Section IV, researchers were advocating the need to adopt principles and techniques from computer networking domains in the context of SoCs. A person of ordinary skill in the art would have been aware of such trends

and suggestions to incorporate techniques from closely-related domains to address and overcome challenges in the SoC arena.

A person of ordinary skill in the art at the time of the alleged invention would have combined the references because each generally relates to similar technology (e.g., Radulescu II at 1:1–4; Petersen at 1:16–21; Peh at 1; Jantsch at 61, 193; Rijkema at 294; Radulescu II at 275; Radulescu III at 1; Dielissen at 1-2; Anjo at 804; Thakkath at 4:44-48; Peh II at 1; Brown at 1:7-10; Fanning at 1:7-9; Poon at 3:7-18; Saastamoinen at II-113; Zeferino at 1; Vellanki at 45; Bolotin at 105; Bhojwani at 1). Moreover, to the extent the ’800 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, it would also have been obvious to a person of ordinary skill in the art to combine all the combinations listed above with the Applicant Admitted Prior Art (“AAPA”) of the ’800 patent. The ’800 patent admits that systems on silicon and networks on chip are prior art. *See, e.g.*, ’800 patent at 1:14-32. The ’800 patent also admits that off-chip network technology is related and applicable to on-chip networks. *See, e.g.*, ’800 patent at 1:59-64. The ’800 patent also admits that “transactions” comprising requests and responses were known in the art, and that it was known in the art for requests to be made by “masters” and responses to be provided by “slaves.” *See, e.g.*, ’800 patent at 2:11–24. In addition, the ’800 patent admits that existing on-chip communication protocols “implement the concept of buffering data which is well-known in the art of chip design” and do so in order to “improve the interconnect utilization.” ’800 patent at 2:42–67. To the extent the ’800 patent identifies any needed improvement in the art, the references provide known techniques that would yield the required

improvement, and given the finite number of techniques identified, it would have been obvious to try those approaches with a reasonable expectation of success.

Moreover, the AAPA of the ’800 patent would have provided additional motivation to combine according to the combinations listed above.

A person of ordinary skill in the art at the time of the alleged invention would understand that each of Radulescu I, Radulescu II, Radulescu III, Peh, Jantsch, Rijpkema, Dielissen, and Vellanki disclose NoC architectures that support both best effort and guaranteed throughput services. *See, e.g.*, Radualescu I at 295, Radulescu II at 15:4-6, Radulescu III at 2, Peh at Chapter 1, Jantsch at 70-71, Rijpkema at 294, Dielissen at 1-2, Vellanki at 47. In particular, these references disclose reserving resources via scheduling, sometimes referred to as time-division multiple access (TDMA). Radualescu I at 295; Radulescu II at 4:17-20, Radulescu III at 2, 19:18-21; Peh at Chapter 2; Jantsch at 70, 75; Rijpkema at 295; Dielissen at 1-2, Vellanki at 47. Such a technique would have been well-known to a POSITA at the time of the alleged invention. A person of ordinary skill would have combined these references. A POSITA would have been motivated to combine these references as they provide additional information regarding the implementation of such a technique. A POSITA would have expected to yield predictable results, and using such known techniques to improve similar devices in the same way would have been obvious.

A person of ordinary skill in the art at the time of the alleged invention would have understood that each of the Petersen, Radulescu I, Radulescu II, Radulescu III, Peh, Anjo, Thekkath, Brown, Fanning, Poon, Saastamoinen, Zeferino, Vellanki, Bolotin, Rijpkema, Dielissen, and Bhojwani (collectively, the “Output Buffering References”) discloses buffering data prior to outputting such data into the interconnect. For example, Petersen discloses a transfer

buffer that is meant to optimize performance. Petersen at 2:13-34. Anjo discloses an output buffer in its write-data buffer. Anjo at 809. Brown disclose optimizes the amount of data transferred from a host computer to a network. Brown at 2:38-51. Radulescu I teaches the use of an output buffer that marshals data and splits it into smaller packets for transportation on the network. Radulescu I at 285. Radulescu II teaches output buffering at a master in order to split outgoing data into smaller packets to be transported over the network. Radulescu II at 8:13-16. Radulescu III discloses message queues that buffer data until a threshold is reached. Radulescu III at 3-4. Peh discloses a flit-reservation flow control system that determines an amount of data that should be buffered by the master (based on the availability of buffers that can be reserved in advance at the slave). Peh at Chapter 2. Poon discloses an optimally sized buffer used to buffer outgoing messages. Poon at 3:66-4:2, 3:10-18. Saastamoinen discloses an outgoing message buffer that is sized to hold maximum sized packets. Saastamoinen at II-114. Thekkath teaches a data buffer with optimized burst lengths based on burst transaction capacity. Thekkath at 5:5-10, 13:5-7, 13:35-40. Fanning discloses modifying the buffer burst length as to optimize the efficiency of the data transfer. Fanning at 5:67-6:6. Bolotin teaches buffering data and scheduling the output of such data. Bolotin at 113. Zeferino discloses buffering data until a packet is scheduled for output. Zeferino at 3. Dielissen teaches message queues and scheduling the output of such message. Dielissen at 3-4. Bhojwani teaches a packetizing module that optimizes the amount of data being sent over the on-chip network. Bhojwani at 5.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Radulescu II with any one of the Output Buffering References because each relates to similar technology involving communications between functional elements. *See, e.g.*, Radulescu II at 1:1–4; Petersen at 1:16–21; Rijpkema at 294; Radulescu I at 275; Radulescu III

at 3-4; Dielissen at 1-2; Anjo at 804; Thakkath at 4:44-48; Brown at 1:7-10; Fanning at 1:7-9; Poon at 3:7-18; Saastamoinen at II-113; Zeferino at 1; Vellanki at 45; Bolotin at 105; Bhojwani at 1. A POSITA would have been motivated to make such a combination in order to decouple computation from communication and optimize the output of data. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Additionally, it would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Radulescu II with Peh or Peh II because relates to similar technology involving communications between functional elements of systems-on-chip. *See, e.g.*, Radulescu II 1:1–4, Peh at 1; Peh II at 1. Peh and Peh II both disclose the flit-reservation flow control that allows for more efficient use of buffers within a network on chip. Peh at 17-19, Peh II at 1. Peh's scheme not only makes use of buffers and resources more efficiently, but is also able to eliminate routing and arbitration decision latency, thus improving overall performance by reducing network latency and providing higher network throughput. Peh at 161; *see also generally id.* at Chapters 7-8. A POSITA would have been motivated to make such a combination in order to schedule the output of buffered data in an efficient manner. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Indeed, the flit-reservation system disclosed by Peh is particularly suited for implementation within a network-on-chip environment, where thick upper metal layer wiring supports the faster control flit signaling. Peh at 32. In addition, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Radulescu II with Bahadiroglu in order to create a NoC with improved performance and efficiency. For example, Bahadiroglu teaches to determine and adjust the "optimal transmit packet size and optimal inter-

packet interval for transmission of packets between the sending node and the receiving node." Bahadiroglu at [0048]. Similarly, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Radulescu II with Bournas in order to improve performance and efficiency of the NoC. For example, Bournas discloses "maximizing a transfer of data to a target." Bournas at 1:45-46. Also, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Radulescu II with Jason in order to improve performance and efficiency of the NoC. Jason teaches to "optimize the efficiency of data communication between [] two interface devices by sending packets of the largest possible size that will not get fragmented." Jason at 2:58-60.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Radulescu I with any one of the Output Buffering References because each relates to similar technology involving communications between functional elements. *See, e.g.*, Radulescu I at 275; Radulescu II at 1:1–4; Radulescu III at 3-4; Petersen at 1:16–21; Rijpkema at 294; Dielissen at 1-2; Anjo at 804; Thakkath at 4:44-48; Brown at 1:7-10; Fanning at 1:7-9; Poon at 3:7-18; Saastamoinen at II-113; Zeferino at 1; Vellanki at 45; Bolotin at 105; Bhojwani at 1. A POSITA would have been motivated to make such a combination in order to decouple computation from communication and optimize the output of data. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Additionally, it would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Radulescu I with Peh or Peh II because relates to similar technology involving communications between functional elements of systems-on-chip. *See, e.g.*, Radulescu I at 275, Peh at 1; Peh II at 1. Peh and Peh II both disclose the flit-reservation flow control that allows for more efficient use of

buffers within a network on chip. Peh at 17-19, Peh II at 1. Peh's scheme not only makes use of buffers and resources more efficiently, but is also able to eliminate routing and arbitration decision latency, thus improving overall performance by reducing network latency and providing higher network throughput. Peh at 161; *see also generally id.* at Chapters 7-8. A POSITA would have been motivated to make such a combination in order to schedule the output of buffered data in an efficient manner. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Indeed, the flit-reservation system disclosed by Peh is particularly suited for implementation within a network-on-chip environment, where thick upper metal layer wiring supports the faster control flit signaling. Peh at 32. In addition, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Radulescu I with Bahadiroglu in order to create a NoC with improved performance and efficiency. For example, Bahadiroglu teaches to determine and adjust the "optimal transmit packet size and optimal inter-packet interval for transmission of packets between the sending node and the receiving node." Bahadiroglu at [0048]. Similarly, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Radulescu I with Bournas in order to improve performance and efficiency of the NoC. For example, Bournas discloses "maximizing a transfer of data to a target." Bournas at 1:45-46. Also, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Radulescu I with Jason in order to improve performance and efficiency of the NoC. Jason teaches to "optimize the efficiency of data communication between [] two interface devices by sending packets of the largest possible size that will not get fragmented." Jason at 2:58-60.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Jantsch with any one of the Output Buffering References because each relates to similar technology involving communications between functional elements. *See, e.g.*, Jantsch at 61, 193; Radulescu I at 275; Radulescu II at 1:1–4; Radulescu III at 3-4; Petersen at 1:16–21; Rijpkema at 294; Dielissen at 1-2; Anjo at 804; Thakkath at 4:44-48; Brown at 1:7-10; Fanning at 1:7-9; Poon at 3:7-18; Saastamoinen at II-113; Zeferino at 1; Vellanki at 45; Bolotin at 105; Bhojwani at 1. A POSITA would have been motivated to make such a combination in order to decouple computation from communication and optimize the output of data. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Additionally, it would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Jantsch with Peh or Peh II because relates to similar technology involving communications between functional elements of systems-on-chip. *See, e.g.*, Jantsch at 61, 193; Peh at 1; Peh II at 1. Peh and Peh II both disclose the flit-reservation flow control that allows for more efficient use of buffers within a network on chip. Peh at 17-19, Peh II at 1. Peh's scheme not only makes use of buffers and resources more efficiently, but is also able to eliminate routing and arbitration decision latency, thus improving overall performance by reducing network latency and providing higher network throughput. Peh at 161; *see also generally id.* at Chapters 7-8. A POSITA would have been motivated to make such a combination in order to schedule the output of buffered data in an efficient manner. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Indeed, the flit-reservation system disclosed by Peh is particularly suited for implementation within a network-on-chip environment, where thick upper metal layer wiring

supports the faster control flit signaling. Peh at 32. In addition, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Jantsch with Bahadiroglu in order to create a NoC with improved performance and efficiency. For example, Bahadiroglu teaches to determine and adjust the "optimal transmit packet size and optimal inter-packet interval for transmission of packets between the sending node and the receiving node." Bahadiroglu at [0048]. Similarly, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Jantsch with Bournas in order to improve performance and efficiency of the NoC. For example, Bournas discloses "maximizing a transfer of data to a target." Bournas at 1:45-46. Also, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Jantsch with Jason in order to improve performance and efficiency of the NoC. Jason teaches to "optimize the efficiency of data communication between [] two interface devices by sending packets of the largest possible size that will not get fragmented." Jason at 2:58-60.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Rijpkema with any one of the Output Buffering References because each relates to similar technology involving communications between functional elements. *See, e.g.*, Rijpkema at 294; Radulescu I at 275; Radulescu II at 1:1–4; Radulescu III at 3-4; Dielissen at 1-2; Petersen at 1:16–21; Anjo at 804; Thakkath at 4:44-48; Brown at 1:7-10; Fanning at 1:7-9; Poon at 3:7-18; Saastamoinen at II-113; Zeferino at 1; Vellanki at 45; Bolotin at 105; Bhojwani at 1. A POSITA would have been motivated to make such a combination in order to decouple computation from communication and optimize the output of data. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Additionally, it would have been

obvious for a person of ordinary skill in the art at the time of the patent to combine Rijpkema with Peh or Peh II because relates to similar technology involving communications between functional elements of systems-on-chip. *See, e.g.*, Rijpkema at 294; Peh at 1; Peh II at 1. Peh and Peh II both disclose the flit-reservation flow control that allows for more efficient use of buffers within a network on chip. Peh at 17-19, Peh II at 1. Peh's scheme not only makes use of buffers and resources more efficiently, but is also able to eliminate routing and arbitration decision latency, thus improving overall performance by reducing network latency and providing higher network throughput. Peh at 161; *see also generally id.* at Chapters 7-8. A POSITA would have been motivated to make such a combination in order to schedule the output of buffered data in an efficient manner. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Indeed, the flit-reservation system disclosed by Peh is particularly suited for implementation within a network-on-chip environment, where thick upper metal layer wiring supports the faster control flit signaling. Peh at 32. In addition, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Rijpkema with Bahadiroglu in order to create a NoC with improved performance and efficiency. For example, Bahadiroglu teaches to determine and adjust the "optimal transmit packet size and optimal inter-packet interval for transmission of packets between the sending node and the receiving node." Bahadiroglu at [0048]. Similarly, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Rijpkema with Bournas in order to improve performance and efficiency of the NoC. For example, Bournas discloses "maximizing a transfer of data to a target." Bournas at 1:45-46. Also, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Rijpkema with Jason in order to improve performance

and efficiency of the NoC. Jason teaches to "optimize the efficiency of data communication between [] two interface devices by sending packets of the largest possible size that will not get fragmented." Jason at 2:58-60.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Dielissen with any one of the Output Buffering References because each relates to similar technology involving communications between functional elements. *See, e.g.*, Dielissen at 1-2; Rijpkema at 294; Radulescu I at 275; Radulescu II at 1:1–4; Radulescu III at 3-4; Petersen at 1:16–21; Anjo at 804; Thakkath at 4:44-48; Brown at 1:7-10; Fanning at 1:7-9; Poon at 3:7-18; Saastamoinen at II-113; Zeferino at 1; Vellanki at 45; Bolotin at 105; Bhojwani at 1. A POSITA would have been motivated to make such a combination in order to decouple computation from communication and optimize the output of data. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Additionally, it would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Dielissen with Peh or Peh II because relates to similar technology involving communications between functional elements of systems-on-chip. *See, e.g.*, Dielissen at 1-2, Peh at 1; Peh II at 1. Peh and Peh II both disclose the flit-reservation flow control that allows for more efficient use of buffers within a network on chip. Peh at 17-19, Peh II at 1. Peh's scheme not only makes use of buffers and resources more efficiently, but is also able to eliminate routing and arbitration decision latency, thus improving overall performance by reducing network latency and providing higher network throughput. Peh at 161; *see also generally id.* at Chapters 7-8. A POSITA would have been motivated to make such a combination in order to schedule the output of buffered data in an efficient manner. Using these known techniques would have yielded predictable results, and

using such known techniques to improve similar devices in the same way would have been obvious. Indeed, the flit-reservation system disclosed by Peh is particularly suited for implementation within a network-on-chip environment, where thick upper metal layer wiring supports the faster control flit signaling. Peh at 32. In addition, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Dielissen with Bahadiroglu in order to create a NoC with improved performance and efficiency. For example, Bahadiroglu teaches to determine and adjust the "optimal transmit packet size and optimal inter-packet interval for transmission of packets between the sending node and the receiving node." Bahadiroglu at [0048]. Similarly, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Dielissen with Bournas in order to improve performance and efficiency of the NoC. For example, Bournas discloses "maximizing a transfer of data to a target." Bournas at 1:45-46. Also, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Dielissen with Jason in order to improve performance and efficiency of the NoC. Jason teaches to "optimize the efficiency of data communication between [] two interface devices by sending packets of the largest possible size that will not get fragmented." Jason at 2:58-60.

It would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Radulescu III with any one of the Output Buffering References because each relates to similar technology involving communications between functional elements. *See, e.g.*, Radulescu III at 3-4; Dielissen at 1-2; Rijpkema at 294; Radulescu I at 275; Radulescu II at 1:1–4; Dielissen at 1-2; Petersen at 1:16–21; Anjo at 804; Thakkath at 4:44-48; Brown at 1:7-10; Fanning at 1:7-9; Poon at 3:7-18; Saastamoinen at II-113; Zeferino at 1; Vellanki at 45; Bolotin at 105; Bhojwani at 1. A POSITA would have been motivated to make such a combination in

order to decouple computation from communication and optimize the output of data. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Additionally, it would have been obvious for a person of ordinary skill in the art at the time of the patent to combine Radulescu III with Peh or Peh II because relates to similar technology involving communications between functional elements of systems-on-chip. *See, e.g.*, Radulescu III at 1, Peh at 1; Peh II at 1. Peh and Peh II both disclose the flit-reservation flow control that allows for more efficient use of buffers within a network on chip. Peh at 17-19, Peh II at 1. Peh's scheme not only makes use of buffers and resources more efficiently, but is also able to eliminate routing and arbitration decision latency, thus improving overall performance by reducing network latency and providing higher network throughput. Peh at 161; *see also generally id.* at Chapters 7-8. A POSITA would have been motivated to make such a combination in order to schedule the output of buffered data in an efficient manner. Using these known techniques would have yielded predictable results, and using such known techniques to improve similar devices in the same way would have been obvious. Indeed, the flit-reservation system disclosed by Peh is particularly suited for implementation within a network-on-chip environment, where thick upper metal layer wiring supports the faster control flit signaling. Peh at 32. In addition, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Radulescu III with Bahadiroglu in order to create a NoC with improved performance and efficiency. For example, Bahadiroglu teaches to determine and adjust the "optimal transmit packet size and optimal inter-packet interval for transmission of packets between the sending node and the receiving node." Bahadiroglu at [0048]. Similarly, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Radulescu III with Bournas in order to improve

performance and efficiency of the NoC. For example, Bournas discloses "maximizing a transfer of data to a target." Bournas at 1:45-46. Also, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Radulescu III with Jason in order to improve performance and efficiency of the NoC. Jason teaches to "optimize the efficiency of data communication between [] two interface devices by sending packets of the largest possible size that will not get fragmented." Jason at 2:58-60.

It would have been obvious to combine Petersen with Radulescu II. Both Petersen and Radulescu II are concerned with buffering data in a network interface for communication over a network. Petersen describes the "transmission of data in a network interface that includes a dedicated transmit buffer" and further describes "optimizing performance" by monitoring the amount of data in the buffer and transmitting the data when the amount of buffered data surpasses a threshold. Petersen at 2:13-34. Radulescu II describes issues related to "[n]etwork flow control and buffering" and further describes network interfaces that include buffers. (Radulescu II at 4:4–13, 8:12–9:2, 14:28–31.)

It would also have been obvious to combine Peh with references that disclose interconnect network designs within a system on chip, such as Radulescu I, Radulescu II, Radulescu III, Jantsch, Rijpkema, Dielissen, Bolotin, and Bhojwani (collectively, the "NoC references"). Like Peh, each of the NoC references describe using networks that are implemented in an integrated circuit. For example, Radulescu II describes "systems on chip" in which "a plurality of modules on the same chip communicate with each other via … a network on chip NOC." Radulescu II at 11:5-7. *See also* Radulescu I at 275 ("In this chapter, we show how networks on chip (NoC) are similar to and differ from both off-chip networks (e.g., computer networks) and current on-chip interconnects (e.g., buses)"; Radulescu III at ("In this paper we

present a network interface for an on-chip network."); Jantsch at Title ("Networks on Chip"), *id.* at vii ("As a consequence, around 1999 several research groups have started to investigate systematic approaches to the design of the communication part of SoCs… Hence, the term *Network on Chip (NoC)* is today used mostly in a very broad meaning, encompassing the hardware communication infra-structure, the middleware and operating system communication services and a design methodology and tools to map applications onto a NoC. All this together can be called a *NoC platform*"; Rijpkema at Title ("Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip"); *see also, e.g., id.* at Abstract; Bolotin at Abstract ("We define Quality of Service (QoS) and cost model for communications in Systems on Chip (SoC), and derive related Network on Chip (NoC) architecture and design process "); *id.* at 105-106 ("This paper presents a design process and a network architecture that satisfy Quality of Service (QoS) (performance) requirements at a measurable VLSI cost which is favorably compared with alternative on-chip interconnection approaches"); Dielissen at Title ("Concepts and Implementation of the Philips Network-on-Chip"); *id.* at 1 ("SoC communication infrastructures, such as the Aethereal network on chip (NoC), will play a central role in integrating Ips with diverse communication requirements."); Bhojwani at Title ("Interfacing Cores with On-Chip Packet-Switched Networks"); *id.* at Abstract (With the goal of reducing this latency we examine the packetization strategies in the NoC communication. In this paper, three schemes of implementations are analyzed, and the costs in terms of latency, and area are projected through actual synthesis."). Similarly, Peh describes "interconnection networks" that are used as "an on-chip interconnect linking modules of a single chip." Peh at 1. Further, Radulescu II describes issues related to "[n]etwork flow control and buffering" (Radulescu II at 4:4–13, 8:12–9:2), and Peh is directed to "flow control," which "determines when a message gets

buffered, and when it gets to move on" (Peh at 6). Indeed, the flit-reservation system disclosed by Peh is particularly suited for implementation within a network-on-chip environment, where thick upper metal layer wiring supports the faster control flit signaling. Peh at 32. Thus, a POSITA would have recognized that the advantages of the flit-reservation teachings set forth in Peh would have been applicable to the network-on-chips in general, including any of the NoCs disclosed in any of the NoC references. A POSITA would have understood that by adding control flits as well as data flits, the overall system will benefit from additional information regarding the availability of resources within the network that is relevant for a given transaction, thus providing improved performance overall to any NoC resource management scheme. A POSITA would have been motivated to adapt the teachings in Peh to any of the NoC references in order to make use of buffers and resources more efficiently as well as to eliminate routing and arbitration decision latency. As one non-limiting example, such a modification would improve overall performance by reducing network latency and providing higher network throughput. Peh at 161; *see also generally id.* at Chapters 7-8. A POSITA would have been motivated to make such a combination in order to schedule the output of buffered data in an efficient manner. In addition, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Peh with Bahadiroglu in order to create a NoC with improved performance and efficiency. For example, Bahadiroglu teaches to determine and adjust the "optimal transmit packet size and optimal inter-packet interval for transmission of packets between the sending node and the receiving node." Bahadiroglu at [0048]. Similarly, it would have been obvious to a person of ordinary skill in the art at the time of the patent to combine Peh with Bournas in order to improve performance and efficiency of the NoC. For example, Bournas discloses "maximizing a transfer of data to a target." Bournas at 1:45-46. Also, it would have been obvious to a person

of ordinary skill in the art at the time of the patent to combine Peh with Jason in order to improve performance and efficiency of the NoC. Jason teaches to "optimize the efficiency of data communication between [] two interface devices by sending packets of the largest possible size that will not get fragmented." Jason at 2:58-60.

The combination of Radulescu III and Bahadiroglu renders the '800 Patent obvious for at least the reasons explained in IPR2024-00339 and supporting exhibits, including the expert declaration of Todd Mowry. The combination of Radulescu III and Petersen renders the '800 Patent obvious for at least the reasons explained in IPR2024-00339 and supporting exhibits, including the expert declaration of Todd Mowry. The combination of Radulescu III, Bahadiroglu, and Radulescu II renders the '800 Patent obvious for at least the reasons explained in IPR2024-00339 and supporting exhibits, including the expert declaration of Todd Mowry. The combination of Radulescu III, Petersen, and Radulescu II renders the '800 Patent obvious for at least the reasons explained in IPR2024-00339 and supporting exhibits, including the expert declaration of Todd Mowry.

It would also have been obvious to modify any of the references to combine discrete components together into a single integrated circuit ("IC") in the form of a system-on-chip ("SoC"). In particular, the text entitled *Modern VLSI Design: System-on-Chip Design, Third Edition* by Wayne Wolf explains that at the time of the patent, it was known that integrating discrete components onto an integrated circuit allowed designers "to build systems with many more transistors, allowing much more computing power to be applied to solving a problem." W. Wolf, *Modern VLSI Design: System-on-Chip Design, Third Edition*, Prentice Hall 2002 ("Wolf") at 1. Wolf teaches that integrated circuits are "much easier to design and manufacture and are more reliable than discrete systems," and that the small sizes of integrated circuits "leads to

advantages in speed and power consumption, since smaller components have smaller parasitic resistances, capacitances, and inductances." *Id.* at 2. Wolf further explains, "Communication within a chip can occur hundreds of times faster than communication between chips on a printed circuit board" because on-chip circuits are smaller, and "smaller components and wires have smaller parasitic capacitances to slow down the signal." *Id.* Wolf notes that the small size of a device is "often an advantage in itself," and that replacing discrete components with a single chip reduces power consumption, which has ripple effects on the rest of the system. *Id*. at 3. For example, with reduced power consumption, a smaller and cheaper power supply can be used. *Id*. Lower power consumption means less heat, so a fan may no longer be necessary. *Id*. Finally, Wolf explains that reducing the number of components, power supply requirements, and so on will "inevitably reduce system cost." *Id*. Indeed, as Wolf explains, many motivations exist to combine discrete components together to form a single IC.

The Applicant's Admitted Prior Art (AAPA) in the '800 patent also confirms that SoCs were previously known, and that it was known to combine discrete components together into a single IC in the form of an SoC, and thus the AAPA in the patent confirms it would have been obvious to modify any of the references to combine discrete components together into a single IC in the form of an SoC. Specifically, the Applicant for the '800 patent explained that the alleged invention arose out of "a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions" in ICs and by "the increasing density with which components can be integrated on an integrated circuit." '800 patent at 1:14-18.

The combinations of references provided are exemplary and are not intended to be exhaustive. Additional obviousness combinations of the references identified here are possible,

and Defendants may rely on such combination(s) in this litigation. In particular, Defendants are currently unaware of Plaintiff's allegations with respect to the level of skill in the art and the qualifications of the typical person of ordinary skill in the art. Defendants are also unaware of the extent, if any, to which Plaintiff may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendants as anticipatory, and the extent to which Plaintiff will contend that elements not disclosed in the asserted patent specifications would have been known to persons of skill in the art. And Defendants do not yet know how the Court will construe terms in the asserted claims. Defendants are also continuing its investigation of the universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Plaintiff may also be in possession of prior art that Defendants may receive as discovery progresses in this case. Defendants reserve the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claims obvious.

VI. INVALIDITY UNDER 35 U.S.C. § 112

Subject to Defendants' reservation of rights, Defendants provide the following contentions relating to the invalidity of the asserted claims under 35 U.S.C. § 112.[6] The asserted claims of the asserted patents are invalid for lack of written description and/or enablement under 35 U.S.C. § 112 ¶ 1, and/or for failing to comply with the definiteness requirements of 35 U.S.C. § 112 ¶ 2. Defendants set forth exemplary limitations that are invalid for failing to comply with these requirements. In addition to the limitations below, Defendants incorporate the claim

[6] Based on Plaintiff's contentions as to the priority dates of the Asserted Claims, Defendants apply pre-AIA 35 U.S.C. § 112 here. However, to the extent that any other form of the patent statute (e.g., post-AIA) regarding invalidity for indefiniteness, non-enablement, or lack of written description applies, Defendants' invalidity contentions and analysis apply just the same.

construction disclosures they have made to date in this litigation, which identify certain claim terms as being indefinite. The disclosures below do not attempt to identify all recitations of a given term or phrase in each claim. Where Defendants have identified an instance of a term or limitation in a particular claim that renders the claim invalid under Section 112, Defendants contend that every instance of the challenged term or limitation, or similar term or limitation, in the claim renders the claim invalid for the same reasons. Defendants contend that each dependent claim that depends from an independent claim that is invalid, as identified below, is also invalid for the same reasons. Defendants further expressly reserve the right to raise and address, once the parties have exchanged claim terms and constructions, any indefiniteness issues arising out of those exchanges. Although complete phrases are sometimes identified below, Defendants reserve the right to argue any word or sub phrase within a larger phrase also violates the written description, enablement, and/or definiteness requirements of 35 U.S.C. § 112.

Defendants reserve the right to amend and/or supplement its contentions, including its contentions based on 35 U.S.C. § 112, as discovery proceeds. In particular, Plaintiff presently asserts an unreasonably large number of claims and has failed to describe its infringement contentions with the required degree of particularity. These contentions are being proffered without expert disclosure or discovery.

In some instances, grounds upon which the asserted claims are invalid for failure to meet the requirements of 35 U.S.C. § 112 may be based upon the apparent constructions being employed by Plaintiff. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, these invalidity positions. Further

these contentions shall not be construed as an admission of acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction as well as Plaintiff's alleged scope of the asserted claims. Consequently, Defendants identify only the issues under 35 U.S.C. § 112 of which they presently aware.

The following contentions are subject to revision and amendment under Federal Rule of Civil Procedure 26(e) and the Orders of record in this matter where appropriate in light of further investigation and discovery regarding the defenses below, the Court's construction of the claims at issue, or the review and analysis of expert witnesses.

Subject to Defendants' reservation of rights, Defendants identify the following written description, enablement, and indefiniteness grounds with respect to the following asserted claims. The following does not purport to list every claim limitation to the foregoing disclosed grounds. Where a particular claim term or limitation is identified, Defendants contend that the identified term or limitation, as well as the surrounding claim language in context as recited in the applicable claim, suffer from the identified Section 112 defect. Furthermore, where a particular claim term or limitation is identified with respect to one or more particular claims, Defendants contend that each other Asserted Claim that recites the same claim term or limitation, or similar claim term or limitation, is subject to the same Section 112 defect. Defendants also reserve the right to assert additional Section 112 defenses as discovery progresses.

A. Legal Principals

1. Indefiniteness

The claims of a patent must "particularly point[] out and distinctly claim[] the subject matter which the inventor or a joint inventor regards as the invention." 35 U.S.C. § 112, second paragraph.[7] Claims are indefinite if they, "read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc.* v. *Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). In evaluating indefiniteness, courts "look to the patent record—the claims, specification, and prosecution history—to ascertain if they convey to one of skill in the art with reasonable certainty the scope of the invention claimed." *Teva Pharms. USA, Inc.* v. *Sandoz, Inc.*, 789 F.3d 1335, 1341 (Fed. Cir. 2015). Although "some modicum of uncertainty" is allowed to ensure "the appropriate incentives for innovation," the claims nonetheless must be "precise enough to afford clear notice of what is claimed, thereby appris[ing] the public of what is still open to them." *Nautilus*, 572 U.S. at 899 (alteration in original) (citations and internal quotation marks omitted). Ultimately, the indefiniteness inquiry is not whether "a court can ascribe *some* meaning to a patent's claims," but rather whether the claims provide "objective boundaries." *Interval Licensing LLC* v. *AOL Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014) (quotation omitted) (discussing *Nautilus*).

Furthermore, when a claim includes a term of degree, such as "substantially" or "essentially," the patent must provide "some standard for measuring" that degree. *See Exmark Mfg. Co.* v. *Briggs & Stratton Power Prods. Group, LLC*, 879 F.3d 1332, 1346 (Fed. Cir. 2018). When a claim includes a term of degree, the patent "must provide 'some standard for measuring

[7] Based on Plaintiff's contentions of the priority dates of the Asserted Claims, Defendants apply pre-AIA 35 U.S.C. § 112 in the first instance here, but to the extent other versions (*e.g.*, post-AIA) regarding invalidity for indefiniteness, non-enablement, or lack of written description applies, Defendants' invalidity contentions and analysis apply just the same.

that degree' such that the claim language provides 'enough certainty to one of skill in the art when read in the context of the invention.'" *GE Lighting Solutions, LLC* v. *Lights of Am., Inc.*, 663 Fed. Appx. 938, 940 (Fed. Cir. 2016) (alteration in original) (citation omitted); *see also Interval Licensing LLC*, 766 F.3d at 1370. For terms of degree, "the patent must provide that additional information in the form of 'objective boundaries.'" *GE Lighting Solutions*, 663 Fed. Appx. at 940 (citation omitted). And the Federal Circuit's "case law is clear that the objective boundaries requirement applies to terms of degree." *Berkheimer* v. *HP Inc.*, 881 F.3d 1360, 1364 (Fed. Cir. 2018). A claim may also be indefinite if its language "'might mean several different things' and the patent itself identifies 'no informed and confident choice . . . among the contending definitions.'" *Otsuka Pharm. Co., Ltd.* v. *Torrent Pharm. Ltd.*, 151 F. Supp. 3d 525, 545 (D.N.J. 2015) (quoting *Nautilus*, 135 S. Ct. at 2130 n.8).

In addition, where a claim term is a "means-plus-function" term governed by 35 U.S.C. § 112 ¶ 6, "the court must determine what structure, if any, disclosed in the specification corresponds to the claimed function" and "[i]f the patentee fails to disclose adequate corresponding structure, the claim is indefinite." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1351–52 (Fed. Cir. 2015). "The standard [for determining whether § 112(6) applies] is whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Id*. at 1349. Although use of the word "means" in a claim creates a "presumption that § 112, ¶ 6 applies," "[w]hen a claim term lacks the word 'means,' the presumption can be overcome and § 112, para. 6 will apply if the challenger demonstrates that the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function." *Id.* (internal quotations omitted).

2. Written Description

The first paragraph of 35 U.S.C. § 112 requires a patent specification to contain "a written description of the invention." The written description must "reasonably convey[] to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1350 (Fed. Cir. 2010) (*en banc*) (citation omitted). Establishing possession as of the filing date is crucial as "[t]he purpose of the written description requirement is to prevent an applicant from later asserting that he invented that which he did not; the applicant for a patent is therefore required to 'recount his invention in such detail that his future claims can be determined to be encompassed within his original creation.'" *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1330 (Fed. Cir. 2003). For example, a written description is inadequate where the claim in question exceeds the scope of what the patent discloses by omitting an attribute of the described invention from the limitations, thereby over-extending the reach of the claim. *ICU Med., Inc. v. Alaris Med. Sys., Inc.*, 558 F.3d 1368, 1377-78 (Fed. Cir. 2009). It is also insufficient that one of ordinary skill in the art might recognize that the disclosure could be modified in light of the prior art to arrive at the claimed subject matter. *Id.* at 1378-79 (citing *Eli Lilly*, 119 F.3d at 1566-67 (explaining that "an applicant complies with the written description requirement by describing the invention, with all its claimed limitations, *not that which makes it obvious*." (internal quotation marks omitted, emphasis added))).

3. Enablement

The enablement requirement of § 112 is separate from and in addition to the written description requirement. *Ariad*, 598 F.3d at 1344. To meet the enablement requirement, the specification must enable a POSITA to "make and use the invention" across the full scope of the

claim, "without undue experimentation." *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988); *see Wyeth & Cordis Corp.* v. *Abbott Labs.*, 720 F.3d 1380, 1384 (Fed. Cir. 2013). When "the teachings set forth in the specifications provide no more than a 'plan' or 'invitation' for those of skill in the art to experiment," the claims are not enabled. *Enzo Biochem, Inc. v. Calgene, Inc.*, 188 F.3d 1362, 1374 (Fed. Cir. 1999). To determine whether "undue" experimentation is required, a court considers: "(1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims." *Wands*, 858 F.2d at 737.

B. § 112 Contentions

1. U.S. Patent No. 7,366,818

The Asserted Claims of the '818 patent fail to meet the requirements of 35 U.S.C. § 112, because the specification of the '818 patent does not contain a written description of the alleged invention, does not enable a person skilled in the art to make and use the alleged invention, or fails to inform with reasonable certainty those skilled in the art about the scope of the invention. In particular, the Asserted Claims of the '818 patent are invalid on § 112 grounds because at least the following terms and limitations are indefinite, lack written description support and/or are not enabled:

Claim Term	Claim(s)	§ 112 Grounds
dropping means (DM) for dropping data exchanged by said first and second module (M, S)	1–3 and 5–7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
dropping means (DM) for dropping data	1-3 and 5-7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)

interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN)	1–3 and 5–7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
a first dropping means (DM) for dropping data	1–3 and 5–7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
connection	1–3 and 5–7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
[wherein] the dropping of data and therefore the transaction completion can be controlled by the interface means	1–3 and 5–7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
[wherein said] dropping means (DM) are adapted to create an error message if data is dropped	3 and 5–7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
[wherein said] dropping means (DM) are adapted to send said error message to said first module (M)	5–7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
[wherein said] interface means (ANIP, PNIP) is adapted to store received error messages	6–7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
[wherein an] interface means (ANIP) associated to the first module (M) is adapted not to drop error messages	7	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)

As an example, the term "dropping means for dropping data exchanged by said first and second module (M, S)" recited in claim 1 (and the claims that depend therefrom) is indefinite at least because it is a term subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed function. The specification also does not describe "dropping means for dropping data exchanged by said first and second module (M, S)" such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "dropping means for

dropping data exchanged by said first and second module (M, S)," nor would a POSITA understand how to practice the claimed invention.

As another example, the limitation term "dropping means for dropping data" recited in claim 1 (and the claims that depend therefrom) is indefinite at least because it is a term subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed function. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "dropping means for dropping data," nor would a POSITA understand how to practice the claimed invention.

The term "interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN)" recited in claim 1 (and the claims that depend therefrom) is indefinite at least because it is a term subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed function. The specification also does not describe "interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN)" such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of an "interface means (ANIP, PNIP) for managing the interface between a module (M, S) and the network (N, RN)" nor would a POSITA understand how to practice the claimed invention.

The term "a first dropping means (DM) for dropping data" recited in claim 1 (and the claims that depend therefrom) is indefinite at least because it is a term subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed function. The

specification also does not describe "a first dropping means (DM) for dropping data" such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "a first dropping means (DM) for dropping data" nor would a POSITA understand how to practice the claimed invention.

The limitation "connection" recited in claim 1 (and the claims that depend therefrom) is indefinite. The specification does not describe "connection" such that a POSITA would understand with reasonable certainty the scope of "connection." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "connection," nor would a POSITA understand how to practice the claimed invention.

The limitation "[wherein] the dropping of data and therefore the transaction completion can be controlled by the interface means" recited in claim 1 (and the claims that depend therefrom) is indefinite. The specification does not describe "the dropping of data and therefore the transaction completion can be controlled by the interface means" such that a POSITA would understand with reasonable certainty its scope. This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "the dropping of data and therefore the transaction completion can be controlled by the interface mean" nor would a POSITA understand how to practice the claimed invention.

The limitation "[wherein said] interface means (ANIP, PNIP) is adapted to store received error messages" recited in claim 6 (and the claims that depend therefrom) is indefinite because

the term "said interface means (ANIP, PNIP)" is subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed function. The specification also does not describe "interface means (ANIP, PNIP) … adapted to store received error messages" such that a POSITA would understand with reasonable certainty its scope. This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "interface means (ANIP, PNIP) … adapted to store received error messages" nor would a POSITA understand how to practice the claimed invention.

The limitations "[wherein said] dropping means (DM) are adapted to create an error message if data is dropped," recited in claim 3 (and the claims that depend therefrom), and "[wherein said] dropping means (DM) are adapted to send said error message to said first module (M)" recited in claim 5 (and the claims that depend therefrom), are indefinite because the term "said dropping mans (DM)" is governed by § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed functions. The specification also does not describe these terms such that a POSITA would understand with reasonable certainty their scope. These limitations likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "dropping means (DM) … adapted to create an error message if data is dropped" or "dropping means (DM) … adapted to send said error message to said first module (M)," nor would a POSITA understand how to practice the claimed invention.

The limitation "[wherein an] interface means (ANIP) associated to the first module (M) is adapted not to drop error messages" recited in claim 7 is indefinite because the term "interface means (ANIP, PNIP)" is subject to § 112, ¶ 6 and the specification does not recite sufficient

structure for performing the claimed function. The specification also does not describe this limitation such that a POSITA would understand with reasonable certainty its scope. This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "interface means (ANIP) associated to the first module (M) … adapted not to drop error messages," nor would a POSITA understand how to practice the claimed invention.

These examples are non-limiting and Defendants reserve the right to raise additional arguments as the case and claim construction process progresses.

Accordingly, the Asserted Claims of the '818 patent are invalid including under § 112 ¶¶ 1, 2, and 6.

2. U.S. Patent No. 7,373,449

The Asserted Claims of the '449 patent fail to meet the requirements of 35 U.S.C. § 112, because the specification of the '449 patent does not contain a written description of the alleged invention, does not enable a person skilled in the art to make and use the alleged invention, or fails to inform with reasonable certainty those skilled in the art about the scope of the invention. In particular, the Asserted Claims of the '449 patent are invalid on §112 grounds because at least the following terms and limitations are indefinite, lack written description support and/or are not enabled:

Claim Element	Claim(s)	§ 112 Grounds
resource manager	10-16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
resource manager [(RM) for managing resources of the network (N)]	10–16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)

communication channel[s]	10-16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
connection	10–16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
connection properties	10-16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
wherein said connections comprises a set of communication channels each having a set of connection properties	10–16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
independently configurable	10-16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
any communication channel being independently configurable	10–16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
communication manager	10-16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
communication manager	10–16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
a request for a connection	10–16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

the communication manager forwarding the request to a resource manager	10–16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
the resource manager responding with the availability of the target connection to the communication manager	10–16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
data transport ordering, flow control, throughput, latency, and lossiness	13, 16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
throughput, latency, and jitter	13, 16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
wherein the connection properties comprise at least one of [data transport ordering, flow control, throughput, latency, and lossiness / throughput, latency and jitter]	13, 16	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
reading of a centralized or distributed property table comprising properties associated with the network	14	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
reading of a centralized or distributed property table comprising properties associated with the network	14	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

As an example, the limitation "communication manager" (claims 10-16) is indefinite at least because it is a term subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed function. If the limitation "communication manager" is not subject to § 112, ¶ 6 it is still indefinite. The specification does not describe "communication manager" such that a POSITA would understand with reasonable certainty its scope. This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "communication manager," nor would a POSITA understand how to practice the claimed invention.

The limitation "resource manager" (claims 10-16) is indefinite at least because it is a term subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed function. If the limitation "resource manager" is not subject to § 112, ¶ 6 it is still indefinite. The specification does not describe "resource manager" such that a POSITA would understand with reasonable certainty its scope. This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "resource manager," nor would a POSITA understand how to practice the claimed invention.

As an example, the term "resource manager [(RM) for managing resources of the network (N)]" recited in claim 10 (and the claims that depend therefrom) is indefinite at least because it is a term subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed function. If the term "resource manager" is not subject to § 112, ¶ 6 it is still indefinite. The specification does not describe a "resource manager" such that a POSITA would understand with reasonable certainty its scope. This limitation likewise lacks sufficient

written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "resource manager," nor would a POSITA understand how to practice the claimed invention.

The limitation "connection" (claims 10-16) is indefinite. The specification does not describe "connection" such that a POSITA would understand with reasonable certainty the scope of "connection." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "connection," nor would a POSITA understand how to practice the claimed invention.

The limitation "connection properties" (claims 10-16) is indefinite. The specification does not describe "connection properties" such that a POSITA would understand with reasonable certainty the scope of "connection properties." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "connection properties," nor would a POSITA understand how to practice the claimed invention.

The limitation "communication channel[s]" (claim 10-16) is indefinite. The specification does not describe "communication channels" such that a POSITA would understand with reasonable certainty the scope of "communication channels." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "communication channels," nor would a POSITA understand how to practice the claimed invention.

The limitation "independently configurable" (claim 10-16) is indefinite. The specification does not describe "independently configurable" such that a POSITA would understand with reasonable certainty the scope of "independently configurable." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "independently configurable," nor would a POSITA understand how to practice the claimed invention.

The limitation "the resource manager determining whether a target connection with the desired connection properties is available," recited in claim 10 (and the claims that depend therefrom), is indefinite because the term "resource manager" is governed by § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed functions. If the term "resource manager" is not subject to § 112, ¶ 6, these limitations are still indefinite. The specification does not describe these limitations such that a POSITA would understand with reasonable certainty their scope. These limitations likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "resource manager [that] determines whether the at least one connection with said communication channels is available based on the connection properties being available" or a "resource manager determining whether a target connection with the desired connection properties is available," nor would a POSITA understand how to practice the claimed inventions.

The term "connection" recited in claim 10 (and the claims that depend therefrom) is indefinite. The specification does not describe a "connection" such that a POSITA would understand with reasonable certainty the scope of "connection." This term likewise lacks

sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "connection," nor would a POSITA understand how to practice the claimed inventions.

The limitation "wherein said [at least one connection /connections] comprises a set of communication channels each having a set of connection properties" recited in claim 10 (and the claims that depend therefrom) is indefinite. The specification does not describe "a set of communication channels" or "connection properties" such that a POSITA would understand with reasonable certainty the scope of "wherein said [at least one connection /connections] comprises a set of communication channels each having a set of connection properties." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "wherein said [at least one connection /connections] comprises a set of communication channels each having a set of connection properties," nor would a POSITA understand how to practice the claimed inventions.

The limitation "any communication channel being independently configurable," recited in claim 10 (and the claims that depend therefrom), is indefinite. The specification does not describe "the connection properties of the different communication channels of said connection being adjustable independently / any communication channel being independently configurable" such that a POSITA would understand with reasonable certainty the scope of "the connection properties of the different communication channels of said connection being adjustable independently / any communication channel being independently configurable." These limitations likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in

possession of "the connection properties of the different communication channels of said connection being adjustable independently / any communication channel being independently configurable," nor would a POSITA understand how to practice the claimed inventions.

The term "communication manager [(CM) for managing the communication between different modules]" recited in claim 10 (and the claims that depend therefrom) is indefinite at least because it is a term subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed function. If the term "communication manager" is not subject to § 112, ¶ 6 it is still indefinite. The specification does not describe a "communication manager" such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "communication manager [(CM) for managing the communication between different modules]," nor would a POSITA understand how to practice the claimed inventions.

The term "a request [(REQ)] for a connection" recited in claim 10 (and the claims the depend therefrom) is indefinite. The specification does not describe "a request [(REQ)] for a connection" such that a POSITA would understand with reasonable certainty the scope of "a request [(REQ)] for a connection." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "a request [(REQ)] for a connection," nor would a POSITA understand how to practice the claimed invention.

The limitation "the communication manager forwarding the request to a resource manager" recited in claim 10 (and the claims that depend therefrom), is indefinite because the term "communication manager" is governed by § 112, ¶ 6 and the specification does not recite

sufficient structure for performing the claimed functions. If the term "communication manager" is not subject to § 112, ¶ 6, these limitations are still indefinite. The specification does not describe this limitation such that a POSITA would understand with reasonable certainty its scope. These limitations likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "communication manager (CM) … adapted to forward said request (REQ) for a connection with communication channels each having a specific set of connection properties to said resource manager (RM)" or a "communication manager forwarding the request to a resource manager," nor would a POSITA understand how to practice the claimed inventions.

The limitation "the resource manager responding with the availability of the target connection to the communication manager" recited in claim 10 (and the claims that depend therefrom), is indefinite because the term "resource manager" is governed by § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed functions. If the term "resource manager" is not subject to § 112, ¶ 6, these limitations are still indefinite. The specification does not describe these limitations such that a POSITA would understand with reasonable certainty their scope. These limitations likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "resource manager (RM) responding with the availability of the requested connection to said communication manager (CM)" or a "resource manager responding with the availability of the target connection to the communication manager," nor would a POSITA understand how to practice the claimed inventions.

The limitation "data transport ordering, flow control, throughput, latency, and lossiness" (claims 13, 16) is indefinite. The specification does not describe "data transport ordering, flow control, throughput, latency, and lossiness" such that a POSITA would understand with reasonable certainty the scope of "data transport ordering, flow control, throughput, latency, and lossiness." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "data transport ordering, flow control, throughput, latency, and lossiness," nor would a POSITA understand how to practice the claimed invention.

The limitation "reading of a centralized or distributed property table comprising properties associated with the network" (claim 14) is indefinite. The specification does not describe "reading of a centralized or distributed property table comprising properties associated with the network" such that a POSITA would understand with reasonable certainty the scope of "reading of a centralized or distributed property table comprising properties associated with the network." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "reading of a centralized or distributed property table comprising properties associated with the network," nor would a POSITA understand how to practice the claimed invention.

The limitation "throughput, latency and jitter" (claims 13, 16) is indefinite. The specification does not describe "throughput, latency and jitter" such that a POSITA would understand with reasonable certainty the scope of "throughput, latency and jitter." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in

possession of "throughput, latency and jitter," nor would a POSITA understand how to practice the claimed invention.

The limitation "whereon the connection properties comprise at least one of [data transport ordering, flow control, throughput, latency, and lossiness / throughput, latency and jitter]" recited in claims 13, and 16 is indefinite. The specification does not describe "data transport ordering, flow control, throughput, latency, and lossiness" such that a POSITA would understand with reasonable certainty the scope of "data transport ordering, flow control, throughput, latency, and lossiness." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "data transport ordering, flow control, throughput, latency, and lossiness," nor would a POSITA understand how to practice the claimed invention.

The limitation "reading of a centralized or distributed property table comprising properties associated with the network" recited in claim 14 is indefinite. The specification does not describe "reading of a centralized or distributed property table comprising properties associated with the network" such that a POSITA would understand with reasonable certainty the scope of "reading of a centralized or distributed property table comprising properties associated with the network." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "reading of a centralized or distributed property table comprising properties associated with the network," nor would a POSITA understand how to practice the claimed invention.

These examples are non-limiting and Defendants reserve the right to raise additional arguments as the case and claim construction process progresses.

Accordingly, the Asserted Claims of the ’449 patent are invalid including under § 112 ¶¶ 1, 2, and 6.

3. U.S. Patent No. 7,594,052

The Asserted Claims of the ’052 patent fail to meet the requirements of 35 U.S.C. § 112, because the specification of the ’052 patent does not contain a written description of the alleged invention, does not enable a person skilled in the art to make and use the alleged invention, or fails to inform with reasonable certainty those skilled in the art about the scope of the invention. In particular, the Asserted Claims of the ’052 patent are invalid on §112 grounds because at least the following terms and limitations are indefinite, lack written description support and/or are not enabled:

Claim Element	Claim(s)	§ 112 Grounds
communication service	6	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
communication properties	6	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
communication service identification	6	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
communication thread	6	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
address range	6	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
connection	6	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
coupling said plurality of processing modules (M, S) by an interconnect means (N)	6	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

enabling a connection based communication having a set of connection properties	6	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification,	6	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)

As an example, the term "communication service" recited in claim 6 is indefinite. The specification does not describe "communication service" such that a POSITA would understand with reasonable certainty the scope of "communication service." This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "communication service," nor would a POSITA understand how to practice the claimed inventions.

The term "communication properties" recited in claim 6 is indefinite. The specification does not describe "communication properties" such that a POSITA would understand with reasonable certainty the scope of "communication properties." This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "communication properties," nor would a POSITA understand how to practice the claimed inventions.

The term "communication service identification" recited in claim 6 is indefinite. The specification does not describe "communication service identification" such that a POSITA would understand with reasonable certainty the scope of "communication service identification." This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in

possession of a "communication service identification," nor would a POSITA understand how to practice the claimed inventions.

The term "communication thread" recited in claim 6 is indefinite. The specification does not describe "communication thread" such that a POSITA would understand with reasonable certainty the scope of "communication thread." This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "communication thread," nor would a POSITA understand how to practice the claimed inventions.

The term "address range" recited in claim 6 is indefinite. The specification does not describe "address range" such that a POSITA would understand with reasonable certainty the scope of "address range." This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of an "address range," nor would a POSITA understand how to practice the claimed inventions.

The term "connection" recited in claim 6 is indefinite. The specification does not describe "connection" such that a POSITA would understand with reasonable certainty the scope of "connection." This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "connection," nor would a POSITA understand how to practice the claimed inventions.

The limitation "coupling said plurality of processing modules (M, S) by an interconnect means (N)" recited in claim 6 is indefinite. The specification does not describe "coupling said plurality of processing modules (M, S) by an interconnect means (N)" such that a POSITA

would understand with reasonable certainty its scope in a manner that is commensurate to Plaintiff's infringement contentions. This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "coupling said plurality of processing modules (M, S) by an interconnect means (N)," nor would a POSITA understand how to practice the claimed invention in a manner that is commensurate to Plaintiff's infringement contentions.

The limitation "enabling a connection based communication having a set of connection properties" recited in claim 6 is indefinite. The specification does not describe "enabling a connection based communication having a set of connection properties" such that a POSITA would understand with reasonable certainty the scope of "enabling a connection based communication having a set of connection properties" in a manner that is commensurate to Plaintiff's infringement contentions. This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "enabling a connection based communication having a set of connection properties," nor would a POSITA understand how to practice the claimed invention in a manner that is commensurate to Plaintiff's infringement contentions.

The term "mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification" recited in claim 6 is indefinite because the specification does not describe "mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification" such that a POSITA would understand with reasonable certainty its scope. This

limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification," nor would a POSITA understand how to practice the claimed inventions.

These examples are non-limiting and Defendants reserve the right to raise additional arguments as the case and claim construction process progresses.

Accordingly, these claims (and claims that depend on them) are invalid including under § 112 ¶¶ 1, 2, and 6.

4. U.S. Patent No. 7,769,893

The Asserted Claims of the '9893 patent fail to meet the requirements of 35 U.S.C. § 112, because the specification of the '9893 patent does not contain a written description of the alleged invention, does not enable a person skilled in the art to make and use the alleged invention, or fails to inform with reasonable certainty those skilled in the art about the scope of the invention. In particular, the Asserted Claims of the '9893 patent are invalid on §112 grounds because at least the following terms and limitations are indefinite, lack written description support and/or are not enabled:

Claim Element	Claims	§ 112 Grounds
first information indicative of a location of an addressed message receiving module S within the network and is comprised of (1) a connection identifier identifying two or more message receiving modules S and (2) an identifier of a passive network interface	4–11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

means associated with the addressed receiving module S		
message request	4–11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
active network interface module	4-11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
passive network interface means associated with the addressed message receiving module S	4–11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
address translation unit	4-11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
arranging, at said address translation unit, the first and the second information comprising said issued message as a single address	4-11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
determining, at said address translation unit, which message receiving module S is being addressed in said message request issued from said addressing module M based on said single address	4-11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
connection properties	4–11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
connection[s]	5, 7, 10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
channel[s]	6	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
simple connections	7, 9	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
multicast connections	7, 10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
narrowcast connections	7, 10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
ordering, flow control, throughput, latency, lossiness, transmission termination, transaction completion, data correctness, priority and data delivery	8	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

[wherein said] active network interface module comprises at least two network interface ports to allow an addressing module M associated with said active network interface module to communicate with a router network or at least one other message receiving module S from among said two or more message receiving modules S	11	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

As an example, limitation "first information indicative of a location of an addressed message receiving module S within the network and is comprised of (1) a connection identifier identifying two or more message receiving modules S and (2) an identifier of a passive network interface means associated with the addressed receiving module S" recited in asserted claim 4 (and the claims that depend therefrom) is indefinite. The specification does not describe this language such that a POSITA would understand with reasonable certainty the scope of the claims. This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "first information indicative of a location of an addressed message receiving module S within the network and is comprised of (1) a connection identifier identifying two or more message receiving modules S and (2) an identifier of a passive network interface means associated with the addressed receiving module S" nor would a POSITA understand how to practice the claimed inventions.

The limitation "message request" recited in asserted claim 4 (and the claims that depend therefrom) is indefinite. The specification does not describe "message request" such that a POSITA would understand with reasonable certainty the scope of "message request." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in

possession of a "message request," nor would a POSITA understand how to practice the claimed invention.

The term "active network interface module associated with said addressing module M," recited in claim 4 (and the claims that depend therefrom), are indefinite at least because they are subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed functions. The specification also does not describe these terms such that a POSITA would understand with reasonable certainty their scope. These terms likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "active network interface means associated with each of said plurality of message sending modules M" or "active network interface module associated with said addressing module M," nor would a POSITA understand how to practice the claimed inventions.

The term recited in claim 4 (and the claims that depend therefrom), are indefinite at least because they are subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed functions. The specification also does not describe these terms such that a POSITA would understand with reasonable certainty their scope. These terms likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "passive network interface means associated with each of said plurality of message receiving modules S" or "passive network interface means associated with the addressed message receiving module S," nor would a POSITA understand how to practice the claimed inventions.

The limitation "address translation unit" is indefinite. The specification does not describe "address translation unit" such that a POSITA would understand with reasonable certainty the

scope of "address translation unit." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of an "address translation unit," nor would a POSITA understand how to practice the claimed invention.

The term "address translation unit," recited in claim 4 (and the claims that depend therefrom), are indefinite at least because they are subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed functions. The specification also does not describe these terms such that a POSITA would understand with reasonable certainty their scope. These terms likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of an "address translation means" or "address translation unit"," nor would a POSITA understand how to practice the claimed inventions.

The limitation "arranging, at said address translation unit, the first and the second information comprising said issued message as a single address" is indefinite. The specification does not describe "arranging, at said address translation unit, the first and the second information comprising said issued message as a single address" such that a POSITA would understand with reasonable certainty the scope of "arranging, at said address translation unit, the first and the second information comprising said issued message as a single address." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "arranging, at said address translation unit, the first and the second information comprising said issued message as a single address," nor would a POSITA understand how to practice the claimed invention.

The limitation "arranging, at said address translation unit, the first and the second information comprising said issued message as a single address," recited in claim 4 (and the claims that depend therefrom), are indefinite. The specification does not describe these limitations such that a POSITA would understand with reasonable certainty their scope. These limitations likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of an invention that "arrange[s] said first information and said second information as a single address" or "arrang[es], at said address translation unit, the first and the second information comprising said issued message as a single address," nor would a POSITA understand how to practice the claimed inventions.

The limitation "determining, at said address translation unit, which message receiving module S is being addressed in said message request issued from said addressing module M based on said single address" is indefinite. The specification does not describe "determining, at said address translation unit, which message receiving module S is being addressed in said message request issued from said addressing module M based on said single address" such that a POSITA would understand with reasonable certainty the scope of "determining, at said address translation unit, which message receiving module S is being addressed in said message request issued from said addressing module M based on said single address." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "determining, at said address translation unit, which message receiving module S is being addressed in said message request issued from said addressing module M based on said single address," nor would a POSITA understand how to practice the claimed invention.

The limitation "determining, at said address translation unit, which message receiving module S is being addressed in said message request issued from said addressing module M based on said single address," recited in claim 4 (and the claims that depend therefrom), are indefinite. The specification does not describe these limitations such that a POSITA would understand with reasonable certainty their scope. These limitations likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of an invention that "determine[s] from said received message requests which of said message receiving modules S is being addressed in said message requests issued from said plurality of message sending modules M based on said single address" or "determine[es], at said address translation unit, which message receiving module S is being addressed in said message request issued from said addressing module M based on said single address," nor would a POSITA understand how to practice the claimed inventions.

The limitation "determining, at said address translation unit, the particular location within the addressed message receiving module S based on said single address" is indefinite. The specification does not describe "determining, at said address translation unit, the particular location within the addressed message receiving module S based on said single address" such that a POSITA would understand with reasonable certainty the scope of "determining, at said address translation unit, the particular location within the addressed message receiving module S based on said single address." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "determining, at said address translation unit,

the particular location within the addressed message receiving module S based on said single address," nor would a POSITA understand how to practice the claimed invention.

The limitation "determining, at said address translation unit, the particular location within the addressed message receiving module S based on said single address," recited in claim 4 (and the claims that depend therefrom), are indefinite. The specification does not describe these limitations such that a POSITA would understand with reasonable certainty their scope. These limitations likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of an invention that "determine[s] the particular location within the addressed message receiving module S based on said single address" or "determine[es], at said address translation unit, the particular location within the addressed message receiving module S based on said single address," nor would a POSITA understand how to practice the claimed inventions.

The term "connection properties" recited in claim 4 (and the claims that depend therefrom) is indefinite. The specification does not describe "connection properties" such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "connection properties," nor would a POSITA understand how to practice the claimed invention.

The term "connection" is indefinite. The specification does not describe this term such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "connections," nor would a POSITA understand how to practice the claimed inventions.

The term “channel” recited in asserted claim 6 (and the claims that depend therefrom) is indefinite. The specification does not describe “channel” such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of “channel,” nor would a POSITA understand how to practice the claimed inventions.

The term “simple connections” recited in asserted claims 7 and 9 (and the claims that depend therefrom) is indefinite. The specification does not describe “simple connections” such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of “simple connections,” nor would a POSITA understand how to practice the claimed inventions.

The limitation “multicast connections” recited in asserted claims 7 and 10 (and the claims that depend therefrom) is indefinite. The specification does not describe “multicast connections” such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of “multicast connections,” nor would a POSITA understand how to practice the claimed inventions.

The limitation “narrowcast connections” recited in asserted claims 7 and 10 (and the claims that depend therefrom) is indefinite. The specification does not describe “narrowcast connections” such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in

possession of "narrowcast connections," nor would a POSITA understand how to practice the claimed inventions.

The limitation "ordering, flow control, throughput, latency, lossiness, transmission termination, transaction completion, data correctness, priority and data delivery" recited in asserted claims 8 is indefinite is indefinite. The specification does not describe "ordering, flow control, throughput, latency, lossiness, transmission termination, transaction completion, data correctness, priority and data delivery" such that a POSITA would understand with reasonable certainty the scope of "ordering, flow control, throughput, latency, lossiness, transmission termination, transaction completion, data correctness, priority and data delivery." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "ordering, flow control, throughput, latency, lossiness, transmission termination, transaction completion, data correctness, priority and data delivery," nor would a POSITA understand how to practice the claimed invention.

The limitation "active network interface module" (claims 4, 11) is indefinite. The specification does not describe "active network interface module" such that a POSITA would understand with reasonable certainty the scope of "active network interface module." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of an "active network interface module," nor would a POSITA understand how to practice the claimed invention.

The limitation "active network interface module comprises at least two network interface ports to allow an addressing module M associated with said active network interface module to

communicate with a router network or at least one other message receiving module S from among said two or more message receiving modules S" recited in asserted claims 11 is indefinite. The specification does not describe "active network interface module comprises at least two network interface ports to allow an addressing module M associated with said active network interface module to communicate with a router network or at least one other message receiving module S from among said two or more message receiving modules S" such that a POSITA would understand with reasonable certainty the scope of "active network interface module comprises at least two network interface ports to allow an addressing module M associated with said active network interface module to communicate with a router network or at least one other message receiving module S from among said two or more message receiving modules S." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "active network interface module comprises at least two network interface ports to allow an addressing module M associated with said active network interface module to communicate with a router network or at least one other message receiving module S from among said two or more message receiving modules S," nor would a POSITA understand how to practice the claimed invention.

These examples are non-limiting and Defendants reserve the right to raise additional arguments as the case and claim construction process progresses.

Accordingly, these claims (and claims that depend on them) are invalid including under § 112 ¶¶ 1, 2, and 6.

5. U.S. Patent No. 8,072,893

The Asserted Claims of the ’2893 patent fail to meet the requirements of 35 U.S.C. § 112, because the specification of the ’2893 patent does not contain a written description of the alleged invention, does not enable a person skilled in the art to make and use the alleged invention, or fails to inform with reasonable certainty those skilled in the art about the scope of the invention. In particular, at least the following limitations of the Asserted Claims of the ’2893 Patent are invalid on §112 grounds:

Claim Element	**Claims**	**§ 112 Grounds**
data package	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
data element[s]	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
data storage element[s]	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
N data elements including a data element	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
M*N data storage elements	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
inserting M*N data storage elements into the data communication network, M being a positive integer	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
channel[s]	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
introducing a delay of M*N cycles on the first communication channel	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

communication channels	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
data routers	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
data routers being coupled to a functional block via a network interface	10	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

The above limitations fail to set forth the scope of the alleged invention with reasonable certainty and/or the ’2893 patent does not provide sufficient written description and/or enablement support for the above claim terms. The limitation “channels” (claim 10) is indefinite. The specification does not describe “channels” such that a POSITA would understand with reasonable certainty the scope of “channels.” This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of “channels,” nor would a POSITA understand how to practice the claimed invention.

The term “data package” recited in claim 10 is indefinite. The specification does not describe “data package” such that a POSITA would understand with reasonable certainty its scope. For example, the specification does not describe how to determine where one data package ends, and the next data package begins. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a “data package,” nor would a POSITA understand how to practice the claimed invention.

The term “data element[s]” recited in claim 10 is indefinite. The specification does not describe “data element[s]” such that a POSITA would understand with reasonable certainty its scope. For example, the specification does not describe how to determine where one data

element ends, and the next data element begins. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "data element[s]," nor would a POSITA understand how to practice the claimed invention.

The term "data storage element[s]" recited in claim 10 is indefinite. The specification does not describe "data storage element[s]" such that a POSITA would understand with reasonable certainty its scope. For example, the specification does not describe how to determine where one data storage element ends, and the next data storage element begins. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "data storage element[s]," nor would a POSITA understand how to practice the claimed invention.

The limitations "each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two" recited in asserted claim 10 is indefinite. The specification does not describe "each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two" such that a POSITA would understand with reasonable certainty its scope. For example, the specification does not describe how to determine what constitutes a data element, let alone where one data element ends and the next data element begins. This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "each data package comprising N data elements including a data

element comprising routing information for the network stations, N being an integer of at least two," nor would a POSITA understand how to practice the claimed invention.

The limitation "inserting M*N data storage elements into the data communication network, M being a positive integer," recited in claim 10 is indefinite. The specification does not describe "M*N data storage elements" such that a POSITA would understand with reasonable certainty its scope. These limitations likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "the data communication network further comprising M*N data storage elements, M being a positive integer" or "inserting M*N data storage elements into the data communication network, M being a positive integer," nor would a POSITA understand how to practice the claimed inventions.

The limitation "introducing a delay of M*N cycles on the first communication channel" recited in claim 10 is indefinite. The specification does not describe "introducing a delay of M*N cycles on the first communication channel" such that a POSITA would understand with reasonable certainty its scope. This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "introducing a delay of M*N cycles on the first communication channel," nor would a POSITA understand how to practice the claimed inventions.

The term "communication channels" recited in claim 10 is indefinite. The specification does not describe "communication channels" such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not

have understood the inventor to be in possession of "communication channels," nor would a POSITA understand how to practice the claimed inventions.

The limitation "N data elements including a data element" (claim 10) is indefinite. The specification does not describe "N data elements including a data element" such that a POSITA would understand with reasonable certainty the scope of "N data elements including a data element." For example, the specification does not describe how to determine the size of a data element, which is not merely arbitrary. These limitations likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "N data elements including a data element," nor would a POSITA understand how to practice the claimed invention.

The limitation "M*N data storage element" (claim 10) is indefinite. The specification does not describe "M*N data storage element" such that a POSITA would understand with reasonable certainty the scope of "M*N data storage element." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "channels," nor would a POSITA understand how to practice the claimed invention.

The term "data routers" recited in claim 10 is indefinite. The specification does not describe "data routers" such that a POSITA would understand with reasonable certainty its scope. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "data routers," nor would a POSITA understand how to practice the claimed inventions.

The limitation "data routers being coupled to a functional block via a network interface" recited in claim 10 is indefinite. The specification does not describe "data routers being coupled to a functional block via a network interface" such that a POSITA would understand with reasonable certainty the scope of "data routers being coupled to a functional block via a network interface." This limitation likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of "data routers being coupled to a functional block via a network interface," nor would a POSITA understand how to practice the claimed invention.

These examples are non-limiting and Defendants reserve the right to raise additional arguments as the case and claim construction process progresses.

Accordingly, these claims (and claims that depend on them) are invalid including under § 112 ¶¶ 1 and 2.

6. U.S. Patent No. 8,086,800

The Asserted Claims of the '800 patent fail to meet the requirements of 35 U.S.C. § 112, because the specification of the '800 patent does not contain a written description of the alleged invention, does not enable a person skilled in the art to make and use the alleged invention, or fails to inform with reasonable certainty those skilled in the art about the scope of the invention. In particular, at least the following limitations of the Asserted Claims of the '800 patent are invalid on §112 grounds:

Claim Element	**Claims**	**§ 112 Grounds**
optimal amount of data to be buffered	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

optimal moment for sending the data in said first wrapper or said second wrapper	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
determination unit	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
first determination unit, second determination unit	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
interconnect module	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2, 6)
[wherein at least one of the first determination unit and the second determination unit is further configured to] determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
the first processing module is connected to the first interconnect module	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
the second processing module is connected to the second interconnect module	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
the first interconnect module is connected between the first processing module and the network	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

the second interconnect module is connected between the second processing module and the network	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
wherein the second determination unit is configured to determine a second optimal amount of data to be buffered by the second memory	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
said first wrapper or said second wrapper	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
according to communication properties of the communication between the master and the slave	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)
connection	12	Lack of enablement, written description and/or indefinite (§ 112 ¶¶ 1, 2)

The above limitations fail to set forth the scope of the alleged invention with reasonable certainty and/or the ’800 patent does not provide sufficient written description and/or enablement support for the above claim terms. As an example, the word “optimal” in the claim terms “optimal amount of data to be buffered” and “optimal moment for sending the data in said first wrapper or said second wrapper” is a subjective “term of degree” and the specification fails to provide objective boundaries for those of skill in the art to determine whether an amount of data to be buffered or a moment for sending the data is “optimal.” For example, the specification refers to multiple conflicting factors for optimal amounts of data buffering (e.g., interconnect utilization, preventing deadlock, sufficiently large amount of data to be transferred as a single package, according to communication properties, conditions for optimal transfer, optimal burst

length for the network, optimal burst length for the interconnect, optimal packet size so that buffered data can be transferred over the network, length optimal for the particular interconnect, etc.), with no objective boundaries, written description and/or enablement to determine a single optimal amount of data to be buffered in view of all the factors referred to in the specification. Similarly, claim 12 recites 10 factors to be considered in determining the optimal moment for sending the data, yet the specification provides no objective boundaries, written description and/or enablement to determine a single optimal moment for sending the data in view of the 10 conflicting factors recited in claim 12. Finally, the specification provides no objective boundaries, written description and/or enablement on when data is actually to be sent when the optimal amount of data to be buffered and the optimal moment for sending the data do not coincide in time.

Claim 12 also recites "wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper …" Yet, there is no previous recitation of "first wrapper" nor "second wrapper." Therefore, claim 12 is indefinite and that '800 patent does not provide sufficient written description and/or enablement support for the above claim terms.

Similarly, claim 12 recites "according to the communication properties of the communication between the master and the slave…." However, there is no previous recitation of "communication", "master", nor "slave." Therefore, claim 12 is indefinite and the '800 patent does not provide sufficient written description and/or enablement support for the above claim terms.

As another example, the term "determination unit" recited in claim 12 is indefinite at least because it is a term subject to § 112, ¶ 6 and the specification does not recite sufficient

structure for performing the claimed function. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "determination unit," nor would a POSITA understand how to practice the claimed invention. The terms "first determination unit" and "second determination unit" lack sufficient written description and enablement for similar reasons.

As further example, the term "interconnect module" recited in claim 12 is indefinite at least because it is a term subject to § 112, ¶ 6 and the specification does not recite sufficient structure for performing the claimed function. This term likewise lacks sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of a "interconnect module," nor would a POSITA understand how to practice the claimed invention.

Claim 12 recites "[wherein at least one of the first determination unit and the second determination unit is further configured to] determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties… wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery." This limitation lacks sufficient written description and enablement because the specification fails to provide any guidance for how each of these communication properties even relate to the "moment" for sending the data, much less

an “optimal moment” that is determined in accordance with the recited communication properties. Indeed, the specification is silent as how to determine an “optimal moment” according to most if not all of the recited communication properties. Therefore, a POSITA would not have understood the inventor to be in possession of this limitation as claimed, nor would a POSITA understand how to practice the claimed invention. This limitation also lacks sufficient written description and enablement because the specification fails to disclose the listed “communication properties”. What the claim calls “communication properties” are referred to as “connection properties” by the specification. ’800 patent at 5:27-35. The specification distinguishes “communication properties” from “connection properties.” *Id.* at 6:47-7:3. Therefore, a POSITA would not have understood the inventor to be in possession of this limitation as claimed, nor would a POSTIA understood how to practice the claimed invention. The ’800 patent does not provide sufficient written description and/or enablement support for the above claim terms. For at least the same reasons, a POSITA would not understand with reasonable certainty the scope of this limitation, rendering the claim indefinite.

The limitations “the first processing module is connected to the first interconnect module”, “the second processing module is connected to the second interconnect module”, “the first interconnect module is connected between the first processing module and the network”, “the second interconnect module is connected between the second processing module and the network”, “wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory”, and “wherein the second determination unit is configured to determine a second optimal amount of data to be buffered by the second memory” recited in claim 12 are indefinite. The specification does not describe any these limitations in a manner such that a POSITA would understand with reasonable certainty the scope of each of

these limitations in a manner that is commensurate to Plaintiff's infringement contentions. These limitations likewise lack sufficient written description and enablement because based on the lack of discussion in the specification a POSITA would not have understood the inventor to be in possession of these limitations nor would a POSITA understand how to practice the claimed invention in a manner that is commensurate to Plaintiff's infringement contentions.

The term "connection" recited in asserted claim 12 is indefinite. The specification does not describe this term such that a POSITA would understand with reasonable certainty its scope. Likewise, the term "connection" lacks sufficient written description and enablement because based on the lack of discussion in the specification, A POSITA would not have understood the inventor to be in possession of these limitations nor would a POSITA understand how to practice the claimed invention in a manner that is commensurate to Plaintiff's infringement contentions. Similarly, the specification does not describe the term "a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module" in such a way that a POSITA would understand with reasonable certainty its scope or have understood the inventor to be in possession of these limitations nor would a POSITA understand how to practice the claimed invention in a manner that is commensurate to Plaintiff's infringement contentions.

These examples are non-limiting and Defendants reserve the right to raise additional arguments as the case and claim construction process progresses.

Accordingly, these claims (and claims that depend on them) are invalid including under § 112 ¶¶ 1, 2, and 6.

VII. SUBJECT MATTER ELIGIBILITY: INELIGIBILITY UNDER 35 U.S.C. § 101

The following Subject Matter Ineligibility Contentions incorporate by reference the Subject Matter Ineligibility Contentions set forth in Appendices G-1 and G-2. These Subject Matter Ineligibility Contentions are subject to revision and amendment pursuant to F.R.C.P. 26(e) and the Scheduling Recommendations, to the extent appropriate, in light of further investigation and discovery regarding the defenses below, the Court's construction of the claims at issue, and/or the review and analysis of expert witnesses.

Whether an invention is eligible for patent protection under 35 U.S.C. § 101 is a "threshold test." *See Bilski v. Kappos*, 130 S. Ct. 3218, 3225 (2010). Section 101 lists four broad categories of patent-eligible subject matter but is subject to "an important implicit exception" that "[l]aws of nature, natural phenomena, and abstract ideas," which form the "basic tools of scientific and technological work," are not eligible for patent protection. *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 573 U.S. 208, 216 (2014) (internal quotation marks omitted). "The 'abstract ideas' category embodies 'the longstanding rule that an idea of itself is not patentable.'" *Id.* at 209 (quoting *Gottschalk v. Benson*, 409 U.S. 63, 67 (1972) (quoting *Rubber-Tip Pencil Co. v. Howard*, 87 U.S. 498 (1874)).

Alice set forth a two-step inquiry. "First, we determine whether the ***claims*** at issue are directed to one of those patent-ineligible concepts." *Id.* at 217 (emphasis added). In making this inquiry, the claims "must be considered as a whole." *Alice*, 573 U.S. at 218 n.3 (quoting *Diamond v. Diehr*, 450 U.S. 175, 188 (1981)). Section 101 is supposed to "prevent patenting of claims that abstractly cover results where 'it matters not by what process or machinery the result is accomplished.'" *McRo Inc. v. Bandai Namco Games Am. Inc.*, 837 F.3d 1299, 1312 (Fed. Cir. 2016). In analyzing step one, courts consider "whether the claims in the patent focus on a specific means or method, or are instead directed to a result or effect that itself is the abstract

idea and merely invokes generic process and machinery." *Two-Way Media Ltd. v. Comcast Cable Commc'ns, LLC*, 874 F.3d 1329, 1337 (Fed. Cir. 2017); *see also Free Stream Media Corp. v. Alphonso Inc.*, 996 F.3d 1355, 1363 (Fed. Cir. 2021).

If the claims recite an abstract idea, the second step requires a "search for an 'inventive concept'—an element or combination of elements that is 'sufficient to ensure that the patent in practice amounts to significantly more than a patent upon the [ineligible concept] itself.'" *Id.* at 218 (quoting *Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 566 U.S. 66, 73 (2016)). "A claim that recites an abstract idea must include 'additional features' to ensure 'that the claim is more than a drafting effort designed to monopolize the abstract idea.'" *Id.* at 221 (quoting *Mayo*, 566 U.S. at 78) (alterations omitted). The recited "additional features must be more than well-understood, routine, conventional activity." *Ultramercial, Inc. v. Hulu, LLC*, 772 F.3d 1335, 1339 (Fed. Cir. 2013) (internal quotations omitted).

Application of an abstract idea using "conventional and well understood techniques" does not "supply an inventive concept." *BSG Tech. LLC v. Buyseasons, Inc.*, 899 F.3d 1281, 1290–91 (Fed. Cir. 2018); *see also Baggage Airline Guest Servs., Inc. v. Roadie. Inc.,* 351 F. Supp. 3d 753, 761 (D. Del. 2019), *aff'd*, 2019 WL 5703890 (Fed. Cir. Nov. 5, 2019) (finding that "reciting generic computer functions and the use of generic computer elements to achieve a more efficient way of 'coordinating and monitoring baggage delivery'" is not an inventive concept). A "critical difference" exists between "patenting a particular concrete solution to a problem" and "attempting to patent the abstract idea of a solution to the problem in general," because the overbroad functional claiming of the latter "purport[s] to monopolize every potential solution to the problem." *BSG*, 899 F.3d at 1290–91. Further, claims are subject matter ineligible if "[w]hat

is claimed is simply a generic environment in which to carry out the abstract idea." *Yu v. Apple Inc.*, 1 F.4th 1040, 1043 (Fed. Cir. 2021).

Defendants identify each Asserted Claim of the '052 and '2893 patents as being directed to the abstract ideas of manipulating, collecting, classifying or otherwise filtering data, and there is nothing in the claims to transform these abstract ideas into inventive concepts. *See* Appendices G-1 – G-2.

VIII. ADDITIONAL INVALIDITY CONTENTIONS

Precise identification of all of the bases upon which the Asserted Claims are invalid and/or unenforceable, including inequitable conduct, improper inventorship, and the judicially-created non-statutory obviousness-type double patenting doctrine, are likely to be revealed only after further developments in the case, including fact and expert discovery. Defendants expressly reserve the right to amend or supplement these Invalidity Contentions to address any additional invalidity arguments that become apparent in view of any relevant facts and information revealed during the course of discovery to the extent required by the Local Rules.

IX. DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS

Based on Defendants' investigation to date and understanding of Plaintiff's Infringement Contentions, Defendants are producing prior art concurrently with these supplemental invalidity contentions.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I certify that counsel of record is being served with a copy of the foregoing document via electronic mail on January 23, 2024.

/s/ J. Derek Vandenburgh
J. Derek Vandenburgh