

Exhibit F-1

Invalidity of U.S. Patent No. 8,086,800 in view of Petersen

U.S. Patent No. 5,434,872 to Petersen et al. (“Petersen”), which was filed on July 28, 1992 and issued on July 18, 1995 qualifies as prior art under at least 35 U.S.C. §§ 102 and 103 as to the asserted claim of U.S. Patent No. 8,086,800 (“’800 patent”), as discussed in greater detail in the chart that follows.¹

To the extent Plaintiff alleges that Petersen does not disclose any particular limitation of claim 12 (the “Asserted Claim”) of the ’800 patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the ’800 patent to modify Petersen and/or to combine the teachings of Petersen with other prior art references, including but not limited to the prior art references presently found in Defendants’ Invalidity Contentions and any supplements thereto and the relevant section of charts for other prior art for the ’800 patent in a manner that would have rendered the Asserted Claim invalid as obvious. The inclusion of the particular limitation into the methods and systems described in Petersen would have been obvious for at least the following reasons: It would have been obvious to modify the methods and/or systems disclosed in Petersen, alone or in combination with the references identified in Defendants’ Invalidity Contentions, to meet this limitation based on: (a) the teachings in Petersen itself; (b) a person of ordinary skill in the art implementing a predictable variation of the methods and/or systems disclosed in Petersen or in the other identified references; (c) the logic, judgment, intelligence, creativity, innovation and common sense a person of ordinary skill in the art would employ; (d) the inferences and creative and routine steps that a person of ordinary skill in the art would employ; (e) market demand for methods and/or systems to include this limitation; and/or (f) design needs or market pressures to solve a problem with a finite number of solutions that could have produced the desired outcome.

Defendants reserve the right to amend or supplement this claim chart at a later date pursuant to the Docket Control Order issued by the Court on June 16, 2023 (Dkt. No. 59).

¹ Nothing in these claim charts should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Defendants’ understanding of the proper scope of the Asserted Claim. Given Plaintiff’s vague and ambiguous infringement contentions, the exemplary citations herein necessarily account for a variety of possible infringement arguments and claim constructions. Defendants reserve the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Plaintiff’s infringement contentions, and/or information obtained during discovery as the case progresses. Various positions put forth in this document are predicated on Plaintiff’s overly broad interpretation of its claims as evidenced by the infringement allegations received to date. Those positions are not intended to and do not necessarily reflect Defendants’ interpretation of the true and proper scope of Plaintiff’s claims, and Defendants reserve the right to adopt claim construction positions that differ from or even conflict with various positions put forth in this document.

A. Claim 12

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[12.pre] An integrated circuit comprising:	To the extent the preamble is limiting, Petersen discloses and/or renders obvious the preamble based on at least the following citations. See, e.g.: <i>See infra</i> Limitation [12.a] To the extent Petersen does not expressly disclose the preamble, a person of ordinary skill in the art would have determined that the preamble is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Petersen. Further, one of ordinary skill in the art would have been motivated to modify Petersen or combine it with any of the present prior art references found in Defendant's Invalidity Contentions and any supplements thereto and the relevant section charts for other prior art for the '800 Patent in a manner that would result in the subject matter of the preamble given, at the very least, the person's understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Petersen.
[12.a] a plurality of processing modules including a first processing module having a first processing memory and a second processing module having a second processing memory;	Petersen discloses and/or renders obvious this limitation based on at least the following citations. See, e.g.: • Petersen at Abstract "Early initiation of transmission of data in a network interface that includes a dedicated transmit buffer is provided in a system which includes logic for transferring frames of data composed by the host computer into the transmit buffer. The amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit data buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to transfer of all of the data of the frame into the transmit buffer. The monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value. Thus, the threshold value may be set by the host system to optimize performance in a given setting." • Petersen at 1:17-21

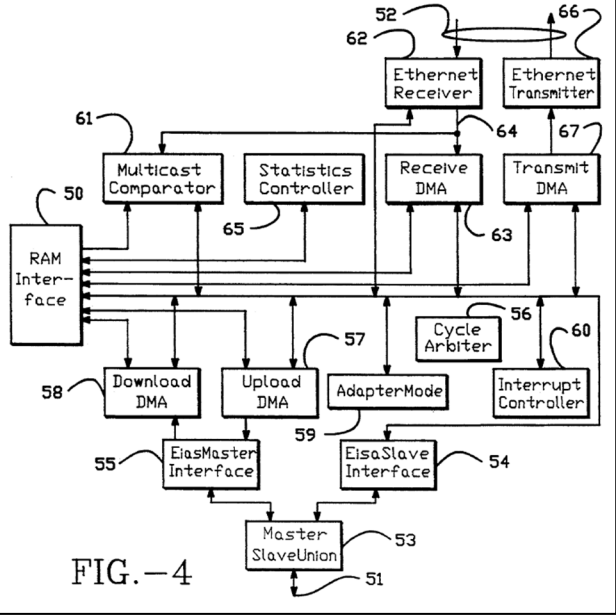
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	“The present invention relates to interfaces between communications networks and data processing systems; in particular, systems which involve the transmission of packets or frames of data across a communications network.” • Petersen at 1:36-54 “Some network adapter interfaces include dedicated transmit buffers into which a frame of data composed by the sending system can be downloaded by the sending system. The frame is then stored in the transmit data buffer until the media access control functions associated with transmitting the frame on the network have successfully transmitted the frame, or cancelled the frame transmission. If the frame transmission is cancelled, the data may be retained in the transmit data buffer until the sending system initiates a second attempt to transmit the frame. Transmit data buffers are to be distinguished from first-in-first-out FIFO systems, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in transmit data buffers.” • Petersen at 2:7-10 “‘It is desirable to provide the advantages of a transmit data buffer, while maintaining the communications throughput available from the simpler FIFO based systems.’” • Petersen at 2:14-34 “‘The present invention provides for the early initiation of transmission of data in a network interface that includes a dedicated transmit buffer. The system includes logic for transferring frames of data composed by the host computer into the transmit buffer. Also, the amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to the transfer of all of the data of the frame into the transmit buffer. In one aspect of the invention, the monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value and logic for posting status information to the host. Thus, the threshold value may be set by the host

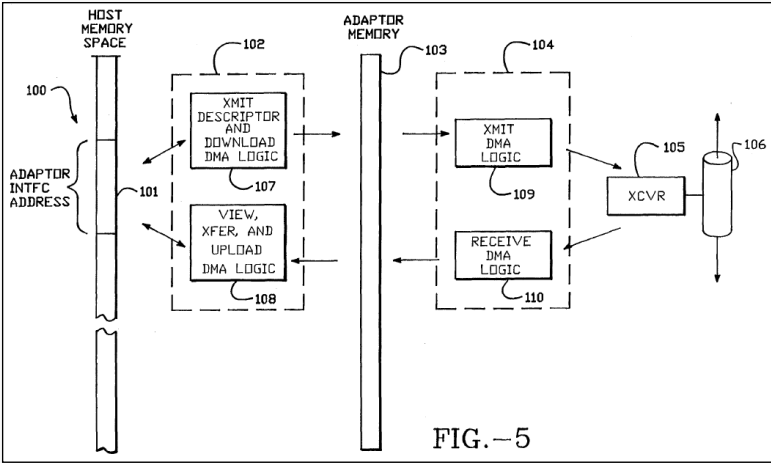
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	system to optimize performance using the alterable threshold store and the posted status information.” Petersen at 5:26-35 “FIG. 3 is a schematic diagram of a computer system including the network interface controller according to the present invention. The computer system includes a host system, including a host processor 10, host memory 11, and other host devices 12, all communicating through a host system bus 13, such as an EISA bus. The host system bus 13 includes address lines which define a host system address space. Typically, for an EISA bus, there are 32 address lines establishing a host system address space of about 4 Gigabytes.” Petersen at 5:36-48 “The network interface controller includes a network interface processor 14, implemented in one preferred system as an application specific integrated circuit designed to implement the functions outlined below using VERILOG design tools as known in the art (available from Cadence, Inc., San Jose, Calif.). The network interface processor 14 is coupled through appropriate buffers to the bus 13. The network interface processor 14 is also coupled to random access memory 15, BIOS ROM 16, and INFO EEPROM 17, a test port 18, an encode/decode chip 19, and a network transceiver 20. The network transceiver 20 is, in turn, coupled to a network medium.” Petersen at 5:56-61 “The RAM 15 is a primary resource on the network interface controller. This resource provides buffer memory outside the host address space used in the transmit and receive operations of the network interface. Details concerning the organization and utilization of this RAM 15 are described below.” Petersen at 6:22-31 “FIG. 4 provides a block diagram of the network interface processor 14 of FIG. 3, including functional blocks and data paths. There are numerous connections not shown having to do with the control of the various data flow paths. The interfaces illustrated include a RAM interface 50, a host bus interface 51, and a transceiver interface 52. The bus interface 51 is implemented for an EISA

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	bus, and operates at times either as a master or as a slave on the bus. Each of the functional units in the implementation shown in FIG. 4 is described below.” Petersen at 8:55-68 “The download DMA module 58 is responsible for issuing requests for bus master downloads of data from the host system to the adapter memory. This data is then deposited within the adapter's onboard transmit data buffer for either immediate or future transmission. As soon as buffer descriptors are defined and one of the transmit data buffers becomes available, as described below, the download DMA module submits requests for download bus master operations to the EISA master interface 55. The download DMA module 58 performs byte alignment, including any required packing and unpacking to align the data as implied by the respective starting addresses of the host and the adapter.” Petersen at 11:47-63 “As mentioned above, the host system will include a host memory space (generally 100) defined by the addresses on the host bus. A pre-specified block 101 of the host memory space is set aside for the adapter interface addresses. The adapter includes host interface logic 102 which is responsive to accesses across the host bus within the adapter interface address block 101. Also in the adapter is a host independent memory 103. The host interface logic operates to map the transfer data between the specified block 101 of addresses and the independent memory. The adapter also includes network interface logic 104 which is coupled to the adapter memory. The network interface logic manages transfers of data from buffers in the independent memory 103 and the network transceiver 105. The network transceiver 105 then supplies the data onto the network medium 106.” Petersen at 13:1-16 “FIG. 7 provides a map of the host independent memory on the adapter. This memory is organized into a transmit data buffer at offset 0 of approximately 3K bytes, a transmit descriptor ring at offset 0C00 (hex) of approximately 5K bytes, a receive buffer ring at offset 2000 (hex) of approximately 22K bytes, and a transfer descriptor area at offset 7800 (hex) of approximately 1K bytes is provided

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	in the independent memory. The last three areas of memory include adapter information, network statistics, and multicast address tables for use by the adapter. In the preferred system, the adapter uses 32K bytes of static RAM for the transmit buffers, receive buffers, control structures, and various status and statistics registers. Several of the regions in the adapter's memory defined in FIG. 5 provide defined data structures.” • Petersen at 13:17-38 “A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffers after choosing the buffer closest to the base of the memory as the power up default. The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. The transmit DMA module switches from one buffer to the other whenever it has completed a transmission. The buffer switch occurs regardless of whether or not the transmission was successful and regardless of whether or not bus master download data were used in the preceding transmission.” • Petersen at Fig. 2

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	FIG. -2 - Petersen at Fig. 3 FIG. -3 - Petersen at Fig. 4

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	 FIG.-4 • Petersen at Fig. 5

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	 The diagram, labeled FIG. 5, illustrates a network adapter architecture. On the left, a vertical bar represents the HOST MEMORY SPACE (100). A bracket labeled ADAPTOR INTFC ADDRESS (101) points to a specific location within this space. To the right of the host memory is the ADAPTOR MEMORY (103). Between these two memory spaces are two dashed boxes containing logic blocks. The first dashed box (102) contains XMIT DESCRIPTOR AND DOWNLOAD DMA LOGIC (107) and VIEW, XFER, AND UPLOAD DMA LOGIC (108). The second dashed box (104) contains XMIT DMA LOGIC (109) and RECEIVE DMA LOGIC (110). Arrows indicate data flow: from host memory (100) to the first dashed box (102), from the first dashed box (102) to the second dashed box (104), and from the second dashed box (104) to the XCVR (105). The XCVR (105) is connected to a vertical cylinder representing a network interface (106). The label FIG. -5 is located at the bottom right of the diagram.

- Petersen at Fig. 7

base address		size
0x0	Transmit Data Buffer	3K
0xc00	Transmit Descriptors	5K
0x2000	Receive Buffer	22K
0x7800	Transfer Descriptor	1K
0x7c00	AdapterInfo Data	256
0x7d00	Network Statistics	196
0x7e00	Muticast Address Table	96

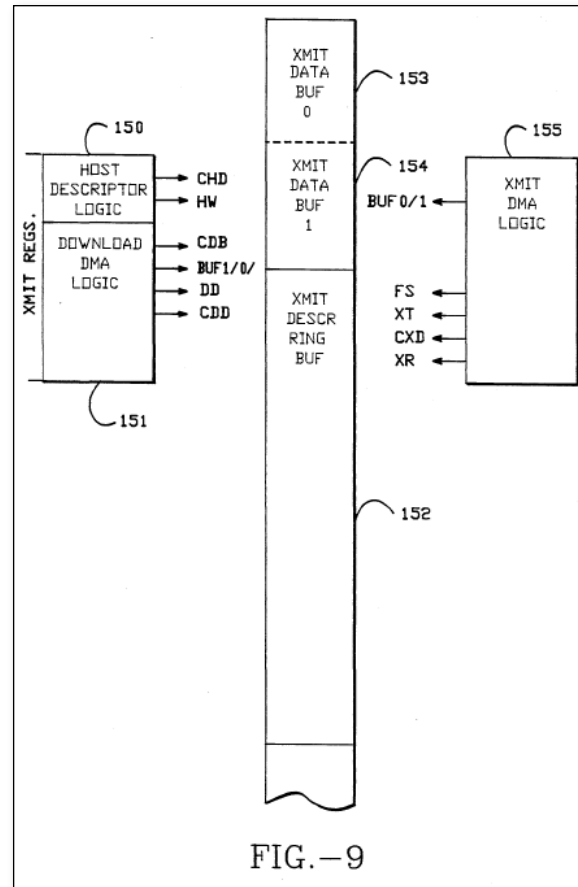
Adapter RAM Memory Map

FIG.—7

- Petersen at Fig. 9

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- Petersen at Claim 1

“For a system transmitting frames of data across a communications medium; an apparatus comprising:
buffer memory for storing data of frames composed by the host computer for transmission on the communications medium;
means, having a host system interface, for transferring data of frames to the buffer memory;

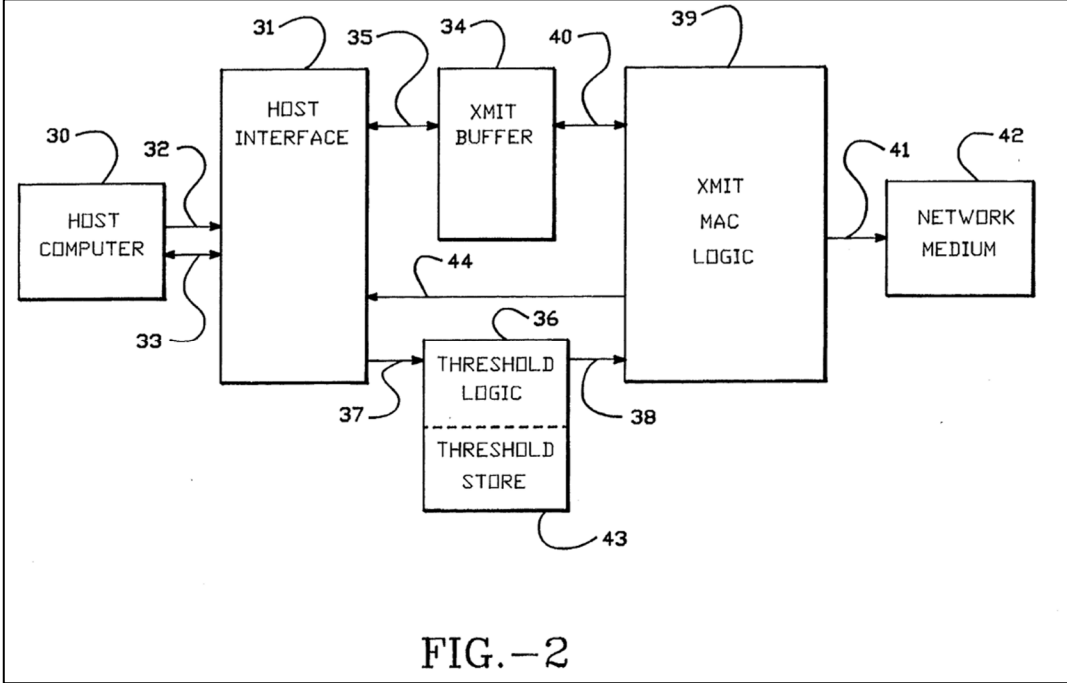
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	means, coupled with the buffer memory, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory; means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data of the frame to the buffer memory from the host computer; transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory and supplying retrieved data for transmission on the communications medium; and underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition.” • Petersen at Claim 10 “An apparatus for controlling communication between a host system and a network transceiver coupled with a network, comprising: a buffer memory; host interface means, having an interface to the host system, for transferring data between the host system and the buffer memory; means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory; and means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer; network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission; and control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value.”

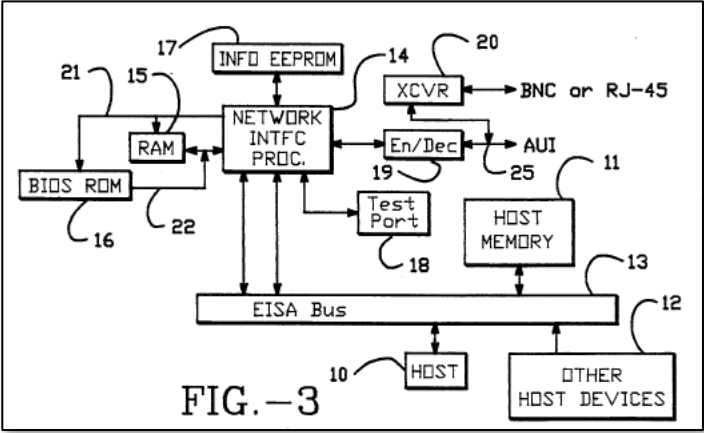
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	• Petersen at Claim 18 “An apparatus for controlling communication between a host system and a network transceiver coupled with a network, comprising: a buffer memory, including a transmit descriptor buffer for storing transmit descriptors identifying data in the host system to be transmitted and including immediate data, and a transmit data buffer for buffering data of frames transferred from the host system; host interface means, having an interface to the host system, for transferring transmit descriptors and data of frames between the host system and the buffer memory and including means, responsive to transmit descriptors in the transmit descriptor buffer, for downloading data of frames from the host system to the transmit data buffer; means, coupled with the buffer memory, for monitoring the immediate data in transmit descriptors in the transmit descriptor buffer and the downloading of data of a frame to the transmit data buffer to make a threshold determination of an amount of data of the frame transferred to the buffer memory; and means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer; network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission; and underrun control means, coupled with the network interface means, for detecting an underrun condition in which the host interface means in downloading data to the transmit data buffer falls behind the network interface means in transferring data to the transceiver, and for supplying a bad frame signal to the network transceiver in response to the underrun condition.” To the extent Petersen does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Petersen. Further, one of ordinary skill in the art would have been motivated to modify Petersen or combine it with any of the present prior art references found in Defendant’s Invalidity Contentions and any supplements thereto and the relevant section charts for other

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	prior art for the '800 Patent in a manner that would result in the subject matter of this limitation given, at the very least, the person’s understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Petersen.
[12.b] a plurality of interconnect modules including a first interconnect module and a second interconnect module, wherein the first processing module is connected to the first interconnect module and the second processing module is connected to the second interconnect module; and	Petersen discloses and/or renders obvious this limitation based on at least the following citations. See, e.g.: • Petersen at Abstract “Early initiation of transmission of data in a network interface that includes a dedicated transmit buffer is provided in a system which includes logic for transferring frames of data composed by the host computer into the transmit buffer. The amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit data buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to transfer of all of the data of the frame into the transmit buffer. The monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value. Thus, the threshold value may be set by the host system to optimize performance in a given setting.” • Petersen at 1:17-21 “The present invention relates to interfaces between communications networks and data processing systems; in particular, systems which involve the transmission of packets or frames of data across a communications network.” • Petersen at 2:14-34 “The present invention provides for the early initiation of transmission of data in a network interface that includes a dedicated transmit buffer. The system includes logic for transferring frames of data composed by the host computer into the transmit buffer. Also, the amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to the transfer of all

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	of the data of the frame into the transmit buffer. In one aspect of the invention, the monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value and logic for posting status information to the host. Thus, the threshold value may be set by the host system to optimize performance using the alterable threshold store and the posted status information.” • Petersen at 3:65-4:10 “As shown in FIG. 1, such system for communicating data includes a host data processing system, generally referred to by reference number 1, which includes a host system bus 2, a host central processing unit 3, host memory 4, and other host devices 5, all communicating across the bus 2. A network interface adapter 6 is coupled to the host bus 2. The adapter 6 is coupled to a transceiver 7 which is, in turn, connected to a network medium 8, such as coaxial cable, a twisted pair conductor, a fiber optic, satellite, wireless, or other communication medium. The network adapter 6 is, in turn, connected to an adapter memory 9, which is managed by the interface controller 6 or by the host CPU 3, depending on a particular implementation provided.” • Petersen at Fig. 1

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	FIG. - 1 • Petersen at 4:23-45 “FIG. 2 illustrates the functional components of the early transmit system according to the present invention. In FIG. 2, a number of functional blocks are represented. The host computer or sending system 30 communicates with a host interface logic 31, receiving data as indicated by line 32 and control signals as indicated by line 33. The host interface logic 31 supplies data to a transmit buffer 34 across line 35. Also, threshold logic 36 is coupled with the host interface logic 31 to monitor the transfer of data from the host computer 30 into the frame buffer 34. The line 37 indicates the coupling of the threshold logic 36 to the host interface logic 31. The threshold logic makes the

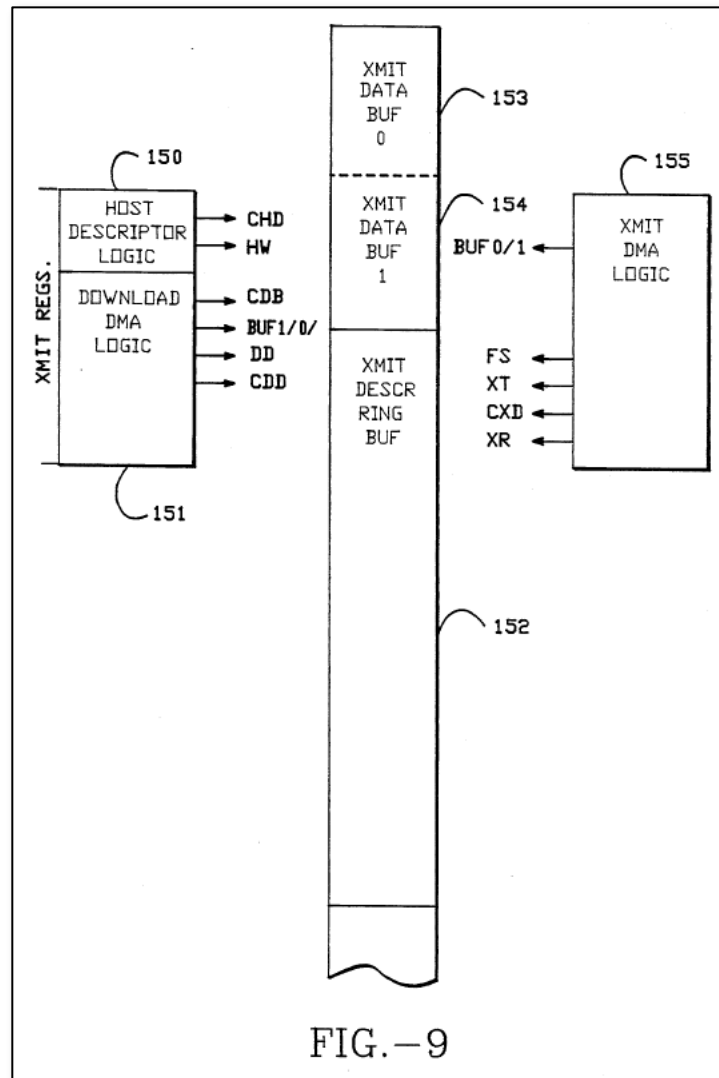
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	threshold determination and generates a signal as indicated by line 38 to transmit logic 39 including, for instance, media access control MAC logic. The transmit logic 39 receives data from the buffer 34 across lines 40 and supplies that data as indicated by line 41 to the network medium 42. Coupled with the threshold logic 36 is a threshold store 43 which stores a threshold value which indicates an amount of data of a frame that must be resident in the frame buffer 34 before transmission of that frame may be initiated by the transmit DMA logic and MAC 39.” - Petersen at Fig. 2  FIG. -2 - Petersen at 7:48-52

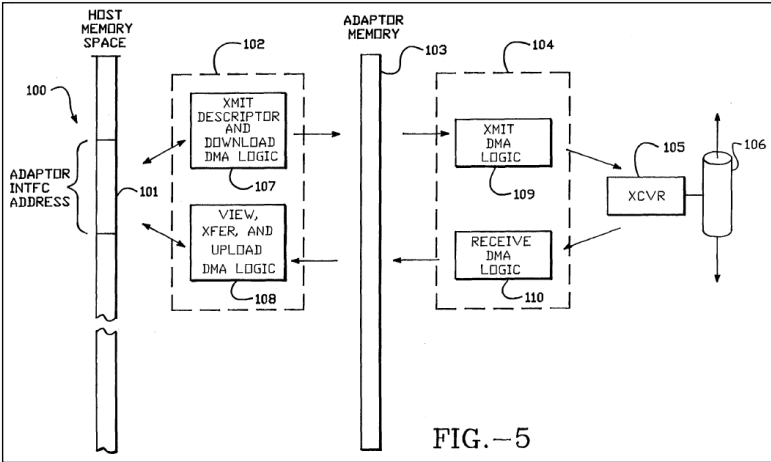
'800 Patent Claim Limitation	U.S. Patent No. 5,434,872 ("Petersen")
	system address space. Typically, for an EISA bus, there are 32 address lines establishing a host system address space of about 4 Gigabytes. The network interface controller includes a network interface processor 14, implemented in one preferred system as an application specific integrated circuit designed to implement the functions outlined below using VERILOG design tools as known in the art (available from Cadence, Inc., San Jose, Calif.). The network interface processor 14 is coupled through appropriate buffers to the bus 13. The network interface processor 14 is also coupled to random access memory 15, BIOS ROM 16, and INFO EEPROM 17, a test port 18, an encode/decode chip 19, and a network transceiver 20. The network transceiver 20 is, in turn, coupled to a network medium." - Petersen at Fig. 3  The diagram, labeled FIG. 3, illustrates a network interface controller. At the center is a 'NETWORK INTFC PROC.' (14). It is connected to several components: 'INFO EEPROM' (17) above it, 'RAM' (15) to its left, 'BIOS ROM' (16) below RAM, and a 'Test Port' (18) below it. To the right of the processor is an 'En/Dec' (19) block, which is connected to a 'XCVR' (20) block. The XCVR is further connected to 'BNC or RJ-45' and 'AUI' (25). Below the processor is an 'EISA Bus' (12). The bus is connected to 'HOST' (10) and 'OTHER HOST DEVICES' (11). A 'HOST MEMORY' (13) is also connected to the bus. Bidirectional arrows indicate data flow between the processor and the bus, and between the bus and the host components. - Petersen at 11:47-63 "As mentioned above, the host system will include a host memory space (generally 100) defined by the addresses on the host bus. A pre-specified block 101 of the host memory space is set aside for the adapter interface addresses. The adapter includes host interface logic 102 which is responsive to accesses across the host bus within the adapter interface address block 101. Also in the adapter is a host independent memory 103. The host interface logic operates to map the transfer data between the specified block 101 of addresses and the independent memory. The adapter also includes

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	network interface logic 104 which is coupled to the adapter memory. The network interface logic manages transfers of data from buffers in the independent memory 103 and the network transceiver 105. The network transceiver 105 then supplies the data onto the network medium 106.” • Petersen at 16:9-23 “FIG. 9 illustrates the network interface logic and host interface logic used in managing the transmit data buffer and transmit descriptor ring buffer in the independent memory on the adapter. On the host interface side, the logic includes host descriptor logic 150 and download DMA logic 151. The host descriptor logic 150 and download DMA logic 151 are coupled to the host address space through the transmit ‘registers’ including the XMIT AREA register, the XMIT COMPLETE THRESH register, the XMIT FAILURE register, the XMIT FRAME LENGTH register, the XMIT FRAME STATUS register, the XMIT PROTID register, the XMIT QUEUE STATUS register, and the XMIT START THRESH register. Details of these registers are described below.” • Petersen at Fig. 9

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	Petersen at 12:7-22 “The network interface logic 104 includes transmit DMA logic, (generally 109) and receive DMA logic (generally 110). The transmit DMA logic 109 is responsive to descriptors stored in the adapter memory 103, as described below, for moving data out of the independent adapter memory 103 to the network transceiver 105. Similarly, the receive DMA logic 110 is responsible for moving data from the transceiver 105 into the independent adapter memory 103. Thus, all communications of data from the network medium 106 are coupled directly into host independent memory 103. Communications from the host independent memory 103 are then controlled through the host interface logic 102 in response to a memory mapped region in the host memory space, greatly simplifying the protocol software necessary to communicate with the network.” Petersen at Fig. 5  FIG. -5 Petersen at 12:33-48 “Although the ‘registers’ are memory mapped to an arbitrary pre-specified block of host address space, none of the reads or writes performed by the host system to these registers actually directly access the adapter memory. Rather, the accesses to the memory mapped space are interpreted by the host interface logic 104 transparent to the host system. Thus, the memory in the adapter is

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	independent of the host address space and of host management. FIG. 6 provides an overview mapping of the host address space used for accessing these registers. The registers include primarily a transmit area register (XMIT AREA) at offset 0010 (hex), a transfer area register (XFER AREA) at offset 0800 (hex), and a look buffer (LOOKBUF) at offset 100C (hex). Various status, statistics, information, and indication registers are distributed throughout the balance of the area.” Petersen at Claim 1 “For a system transmitting frames of data across a communications medium; an apparatus comprising: buffer memory for storing data of frames composed by the host computer for transmission on the communications medium; means, having a host system interface, for transferring data of frames to the buffer memory; means, coupled with the buffer memory, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory; means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data of the frame to the buffer memory from the host computer; transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory and supplying retrieved data for transmission on the communications medium; and underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition.” Petersen at Claim 10 “An apparatus for controlling communication between a host system and a network transceiver coupled with a network, comprising: a buffer memory; host interface means, having an interface to the host system, for transferring data between the host system and the buffer memory;

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	means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory; and means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer; network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission; and control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value.” • Petersen at Claim 18 “An apparatus for controlling communication between a host system and a network transceiver coupled with a network, comprising: a buffer memory, including a transmit descriptor buffer for storing transmit descriptors identifying data in the host system to be transmitted and including immediate data, and a transmit data buffer for buffering data of frames transferred from the host system; host interface means, having an interface to the host system, for transferring transmit descriptors and data of frames between the host system and the buffer memory and including means, responsive to transmit descriptors in the transmit descriptor buffer, for downloading data of frames from the host system to the transmit data buffer; means, coupled with the buffer memory, for monitoring the immediate data in transmit descriptors in the transmit descriptor buffer and the downloading of data of a frame to the transmit data buffer to make a threshold determination of an amount of data of the frame transferred to the buffer memory; and means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer;

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	network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission; and underrun control means, coupled with the network interface means, for detecting an underrun condition in which the host interface means in downloading data to the transmit data buffer falls behind the network interface means in transferring data to the transceiver, and for supplying a bad frame signal to the network transceiver in response to the underrun condition.” To the extent Petersen does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Petersen. Further, one of ordinary skill in the art would have been motivated to modify Petersen or combine it with any of the present prior art references found in Defendant’s Invalidity Contentions and any supplements thereto and the relevant section charts for other prior art for the ’800 Patent in a manner that would result in the subject matter of this limitation given, at the very least, the person’s understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Petersen.
[12.c] a network for connecting the first interconnect module to the second interconnect module in order to provide a communication connection between the first processing module and the second processing module, wherein the first interconnect module is connected between the first processing module and the network, and wherein the second interconnect module is connected between the	Petersen discloses and/or renders obvious this limitation based on at least the following citations. See, e.g.: • Petersen at Abstract “Early initiation of transmission of data in a network interface that includes a dedicated transmit buffer is provided in a system which includes logic for transferring frames of data composed by the host computer into the transmit buffer. The amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit data buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to transfer of all of the data of the frame into the transmit buffer. The monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value. Thus, the threshold value may be set by the host system to optimize performance in a given setting.”

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second processing module and the network;	• Petersen at 1:17-21 “The present invention relates to interfaces between communications networks and data processing systems; in particular, systems which involve the transmission of packets or frames of data across a communications network.” • Petersen at 3:65-4:10 “As shown in FIG. 1, such system for communicating data includes a host data processing system, generally referred to by reference number 1, which includes a host system bus 2, a host central processing unit 3, host memory 4, and other host devices 5, all communicating across the bus 2. A network interface adapter 6 is coupled to the host bus 2. The adapter 6 is coupled to a transceiver 7 which is, in turn, connected to a network medium 8, such as coaxial cable, a twisted pair conductor, a fiber optic, satellite, wireless, or other communication medium. The network adapter 6 is, in turn, connected to an adapter memory 9, which is managed by the interface controller 6 or by the host CPU 3, depending on a particular implementation provided.” • Petersen at 5:26-48 “FIG. 3 is a schematic diagram of a computer system including the network interface controller according to the present invention. The computer system includes a host system, including a host processor 10, host memory 11, and other host devices 12, all communicating through a host system bus 13, such as an EISA bus. The host system bus 13 includes address lines which define a host system address space. Typically, for an EISA bus, there are 32 address lines establishing a host system address space of about 4 Gigabytes. The network interface controller includes a network interface processor 14, implemented in one preferred system as an application specific integrated circuit designed to implement the functions outlined below using VERILOG design tools as known in the art (available from Cadence, Inc., San Jose, Calif.). The network interface processor 14 is coupled through appropriate buffers to the bus 13. The network interface processor 14 is also coupled to random access memory 15, BIOS ROM 16, and INFO EEPROM 17, a test port 18, an encode/decode chip 19, and a network transceiver 20. The network transceiver 20 is, in turn, coupled to a network medium.” • Petersen at Fig. 3

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	FIG. -3 Petersen at 5:49-6:7 “A majority of the functionality is embodied in the network interface processor 14. In the preferred embodiment, all registers that are accessible across the bus 13 by the host system reside either in the processor 14, or in the RAM 15. If resident in the RAM 15, their access is managed by the network interface processor 14. The RAM 15 is a primary resource on the network interface controller. This resource provides buffer memory outside the host address space used in the transmit and receive operations of the network interface. Details concerning the organization and utilization of this RAM 15 are described below. The BIOS ROM 16 provides extension to the host system's basic input/output code through the network interface processor 14 during initialization. The addresses for the BIOS ROM 16 and the data from the BIOS ROM 16 are coupled to the network interface processor 14 across buses 21 and 22, respectively, which are also shared by the RAM 15.

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	The INFO EEPROM 17 stores critical adapter specific data used by drivers, diagnostics, and network management software. This data is stored during the manufacturing process. During initialization of the interface controller, the contents of the EEPROM17 are loaded into a prespecified area of the RAM 15 for use during operation.” • Petersen at 6:22-31 “FIG. 4 provides a block diagram of the network interface processor 14 of FIG. 3, including functional blocks and data paths. There are numerous connections not shown having to do with the control of the various data flow paths. The interfaces illustrated include a RAM interface 50, a host bus interface 51, and a transceiver interface 52. The bus interface 51 is implemented for an EISA bus, and operates at times either as a master or as a slave on the bus. Each of the functional units in the implementation shown in FIG. 4 is described below.” • Petersen at Fig. 4

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	Petersen at 6:33-7:21 “The EISA slave interface 54 provides a path for the EISA host to access the registers and buffers managed by the network interface controller. The module contains configuration registers for the controller, and performs crude decoding of the EISA bus for the purpose of routing signals. The EISA slave interface 54 does not interpret any of the addressing of individual registers distributed throughout the controller. In operation, the EISA slave interface continuously monitors the EISA address bus and determines when the configuration registers, memory mapped network registers, or BIOS ROM of the adapter are being accessed.

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	In addition, for every memory slave cycle initiated by the EISA bus, the EISA slave interface will post a cycle request to the cycle arbiter 56. The cycle arbiter imposes wait states upon the host system until the request has been granted. The EISA slave interface also provides a generic 32 bit bus interface to the remainder of the network controller. The generic nature of the interface allows for easy adaptation of the design to other bus types, such as the microchannel, without requiring redesign of the remainder of the chip. Bits 14-2 of the EISA address bus are latched and pass through to other modules. The least significant two bits (1, 0) of the address are represented by 4 byte enables that are also valid throughout a data transfer cycle. Four 8-bit byte lanes make up the slave data channel. The data bus is actually a pair of unidirectional buses, one for writes and one for reads in a preferred system. The data write bus is wired in a multi-drop fashion to all modules that require connection to the EISA data bus through the slave interface. The read bus is multiplexed and masked in the RAM interface module 50. Write requests by the EISA bus can be held until they are acknowledged by the cycle arbiter 56. When a cycle is held, the EISA bus may be released from wait states while the cycle completes on the adapter. If a second cycle is generated by the EISA bus while the first one is still pending, then the EISA bus will be held off with wait states until the pending write is performed. In this specific embodiment, pipelining of EISA reads is not supported. The EISA slave interface also provides an interface to the EEPROM 17. This interface operates to transfer the contents of the EEPROM17 into the adapter memory after reset. There are numerous registers in the EISA slave interface module 54, primarily related to configuration of the adapter that conform to the EISA bus specification. These registers do such things as set up the adapter's memory base address, the interrupt level, the transceiver type selection, and the BIOS ROM enable. The configuration registers also provide the host with a positive means of identifying the adapter type and to globally disable the adapter.” • Petersen at 11:47-63

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	“As mentioned above, the host system will include a host memory space (generally 100) defined by the addresses on the host bus. A pre-specified block 101 of the host memory space is set aside for the adapter interface addresses. The adapter includes host interface logic 102 which is responsive to accesses across the host bus within the adapter interface address block 101. Also in the adapter is a host independent memory 103. The host interface logic operates to map the transfer data between the specified block 101 of addresses and the independent memory. The adapter also includes network interface logic 104 which is coupled to the adapter memory. The network interface logic manages transfers of data from buffers in the independent memory 103 and the network transceiver 105. The network transceiver 105 then supplies the data onto the network medium 106.” • Petersen at 12:33-48 “Although the ‘registers’ are memory mapped to an arbitrary pre-specified block of host address space, none of the reads or writes performed by the host system to these registers actually directly access the adapter memory. Rather, the accesses to the memory mapped space are interpreted by the host interface logic 104 transparent to the host system. Thus, the memory in the adapter is independent of the host address space and of host management. FIG. 6 provides an overview mapping of the host address space used for accessing these registers. The registers include primarily a transmit area register (XMIT AREA) at offset 0010 (hex), a transfer area register (XFER AREA) at offset 0800 (hex), and a look buffer (LOOKBUF) at offset 100C (hex). Various status, statistics, information, and indication registers are distributed throughout the balance of the area.” To the extent Petersen does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Petersen. Further, one of ordinary skill in the art would have been motivated to modify Petersen or combine it with any of the present prior art references found in Defendant’s Invalidity Contentions and any supplements thereto and the relevant section charts for other prior art for the ’800 Patent in a manner that would result in the subject matter of this limitation given, at the very least, the person’s understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Petersen.
[12.d] wherein the first interconnect module includes a first memory for buffering	Petersen discloses and/or renders obvious this limitation based on at least the following citations. See, e.g.:

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first data from the first processing module, the first interconnect module further including a first determination unit, wherein the first determination unit is configured to determine a first optimal amount of data to be buffered by the first memory, and the second interconnect module includes a second memory for buffering second data from the second processing module, the second interconnect module further including a second determination unit, wherein the second determination unit is configured to determine a second optimal amount of data to be buffered by the second memory,	• Petersen at Abstract “Early initiation of transmission of data in a network interface that includes a dedicated transmit buffer is provided in a system which includes logic for transferring frames of data composed by the host computer into the transmit buffer. The amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit data buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to transfer of all of the data of the frame into the transmit buffer. The monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value. Thus, the threshold value may be set by the host system to optimize performance in a given setting.” • Petersen at 1:36-54 “Some network adapter interfaces include dedicated transmit buffers into which a frame of data composed by the sending system can be downloaded by the sending system. The frame is then stored in the transmit data buffer until the media access control functions associated with transmitting the frame on the network have successfully transmitted the frame, or cancelled the frame transmission. If the frame transmission is cancelled, the data may be retained in the transmit data buffer until the sending system initiates a second attempt to transmit the frame. Transmit data buffers are to be distinguished from first-in-first-out FIFO systems, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in transmit data buffers.” • Petersen at 2:7-10 “it is desirable to provide the advantages of a transmit data buffer, while maintaining the communications throughput available from the simpler FIFO based systems.” • Petersen at 2:14-34

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	“The present invention provides for the early initiation of transmission of data in a network interface that includes a dedicated transmit buffer. The system includes logic for transferring frames of data composed by the host computer into the transmit buffer. Also, the amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to the transfer of all of the data of the frame into the transmit buffer. In one aspect of the invention, the monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value and logic for posting status information to the host. Thus, the threshold value may be set by the host system to optimize performance using the alterable threshold store and the posted status information.” • Peterson at 2:44-55 “When the adapter begins processing of a transmit descriptor, it retrieves immediate data from the descriptor itself, and begins a download process into the transmit data buffer of data identified in the descriptor. The threshold logic determines the amount of immediate data from the descriptor, and monitors the downloading of data of the frame into the download area. When the combination meets the threshold, then actual transmission of the frame is initiated. Thus, transmission of a frame may be initiated before the complete frame has been downloaded into the download area.” • Peterson at 3:59-65 “FIG. 1 illustrates a data communication system according to the present invention with a controller circuit using a dedicated transmit buffer memory which is automatically enabled to begin transmission of a frame on the network when the number of bytes available in the transmit buffer memory exceeds a preprogrammed threshold.” • Peterson at 4:11-17 “The adapter 6 also includes early transmit logic 6A for monitoring the transfer of data from the host system 1 into the adapter memory 9. The early transmit logic 6A makes a threshold

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	determination for a given frame being transferred from the host 1 into the adapter memory 9. When the threshold is met, then the adapter 6 begins transmitting the frame across the network.” • Petersen at 4:23-49 “FIG. 2 illustrates the functional components of the early transmit system according to the present invention. In FIG. 2, a number of functional blocks are represented. The host computer or sending system 30 communicates with a host interface logic 31, receiving data as indicated by line 32 and control signals as indicated by line 33. The host interface logic 31 supplies data to a transmit buffer 34 across line 35. Also, threshold logic 36 is coupled with the host interface logic 31 to monitor the transfer of data from the host computer 30 into the frame buffer 34. The line 37 indicates the coupling of the threshold logic 36 to the host interface logic 31. The threshold logic makes the threshold determination and generates a signal as indicated by line 38 to transmit logic 39 including, for instance, media access control MAC logic. The transmit logic 39 receives data from the buffer 34 across lines 40 and supplies that data as indicated by line 41 to the network medium 42. Coupled with the threshold logic 36 is a threshold store 43 which stores a threshold value which indicates an amount of data of a frame that must be resident in the frame buffer 34 before transmission of that frame may be initiated by the transmit DMA logic and MAC 39. The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30. In this embodiment, the threshold store 43 is a register accessible by the host through the interface logic 31.” • Petersen at Fig. 2

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	FIG. -2 Peterson at 4:56-60 “The transmit logic 39 also supplies status information across line 44 to the host interface logic 31, for posting to the host system. The status information includes indications of underrun conditions and may be used by the host to optimize the value in the threshold store 43.” Petersen at 4:61-5:13 “In operation, the host computer composes a frame of data to be transmitted on the network medium 42. The host computer 30 then identifies that frame through the host interface 31. The host interface coupled with the identifiers of the frame move data from the host computer 30 into the buffer 34 according to the description of the frame. The threshold logic 36 monitors the transfer of data into the buffer 34. When the threshold amount of data is resident in the buffer 34, then the transmit logic 39 is instructed to begin transmission of the frame. The transmit logic 39 then begins retrieving data from the buffer 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing download from the host computer 30, the frame being downloaded into the buffer 34 is larger than the threshold set by the

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	threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired.” • Petersen at 5:56-61 “The RAM 15 is a primary resource on the network interface controller. This resource provides buffer memory outside the host address space used in the transmit and receive operations of the network interface. Details concerning the organization and utilization of this RAM 15 are described below.” • Petersen at 8:47-53 “H. Statistics Controller Module 65 The preferred system also includes a statistics controller module 65. This module monitors activity of various other modules within the controller, most particularly the Ethernet transmitter module 66 and the Ethernet receiver module 62, and updates statistics maintained in RAM 15 as applicable events occur.” • Petersen at 13:17-38 “A. Transmit Data Buffer The transmit data buffer occupies 3K bytes as mentioned above. This region is divided into two 1.5K buffers. Only the data that are downloaded to the adapter via bus master transfers are stored in these buffers. The controller will use both the contents of the transmit data buffer and the immediate data portion of the transmit descriptors, when encapsulating a frame for transmission. The adapter automatically alternates the use of the buffers after choosing the buffer closest to the base of the memory as the power up default. The transmit buffers are shared by the download DMA logic and the transmit DMA logic. The transmit DMA logic may switch from buffer 0 to buffer 1 and back again freely. The only restriction being the availability of transmit data as defined by the transmit start threshold register. The transmit DMA module switches from one buffer to the other whenever it has completed a transmission. The buffer switch occurs regardless of whether or not the transmission was successful and regardless of whether or not bus master download data were used in the preceding transmission.”

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	• Petersen at 21:11-39 “H. XMIT START THRESH XMIT START THRESH provides for an early start of transmission. The XMIT START THRESH register is used to specify the number of transmit bytes that must reside on the adapter before it will start transmission. Values greater than the maximum frame length will prevent this function from operating properly. The method for disabling this function is to set the register to zero. Bytes are counted starting with the first byte of the destination field of the transmit frame. The number of bytes considered to be available is the sum of the immediate data written to XMIT AREA by the host and those bytes transferred to the transmit data buffers in the adapter using bus master DMA operations. The transmit request will be posted immediately after XMIT START THRESH transmit frame bytes are made available from the immediate data or when the adapter has bus-mastered XMIT START THRESH-XMIT IMMED LEN bytes onto the adapter. The number of bytes resident on the adapter must be equal to or greater than the value in XMIT START THRESH for the transmission to commence, unless the total frame size is less than XMIT START THRESH. In that case, the frame will begin transmission when the entire frame has been copied to the adapter. The actual transmission of the frame may be delayed by previous pending transmit frames and by deferrals to network traffic. This register is set to zero during a reset.” • Petersen at 23:20-24:52 “VI. The Early Transmit Logic The early transmit logic 6A illustrated in FIG. 1 is implemented primarily in the download DMA logic 58 in the preferred implementation. The key components of a preferred implementation include data path arithmetic described with reference to FIG. 11, and transmit start control logic illustrated with respect to FIGS. 12-17. *** Thus, this logic is coupled with the host address and monitors the downloading of data from the host into the transmit data buffer for use in making a threshold determination of the amount of data of a given frame resident in the adapter memory.”

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	• Petersen at 24:59-25:18 “FIG. 12 is a block diagram of the transmit start control logic. The transmit start control logic includes a start threshold register 320, and a download compare block 321 which compares the value of the start threshold with the download bytes resident value generated in the data path arithmetic of FIG. 11. Also, an immediate data comparator 322 is included to perform the comparison in the event that immediate data is present in the transmit descriptor. Finally, a data available control block 323 is included which generates the xmitDataAvailable signal for supply to the transmit DMA logic block of the adapter. The transmit start control logic in FIG. 12 is responsible for generating the xmitDataAvailable signal, which is supplied to the transmit DMA module to indicate that there is data available to be transmitted onto the network. The xmitDataAvailable signal is asserted under three conditions: (1) there are one or more complete frames resident on the adapter ready to be transmitted; (2) there are no complete frames on the adapter, but the number of bytes resident for a frame currently being downloaded is greater than the value in the transmit start threshold register; and (3) there are no complete frames on the adapter, and there are no pending download operations, and the number of immediate bytes resident for the frame currently being written to the transmit area register is greater than the value of transmit start threshold.” • Petersen at Fig. 12

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	FIG. - 12 Petersen at 29:12-34 “XMIT START THRESH is used to specify the number of bytes of the transmit frame that must reside on the adapter, either as immediate data or as data transferred onto the adapter via bus master data transfers, or as a combination of the two, before the adapter can commence with the media access control functions associated with transmitting the frame. If the number of immediate data bytes expected by the adapter (as determined by the value written to the XMIT IMMEDIATE LENGTH field of the XMIT AREA) exceeds the value set in XMIT START THRESH, then the adapter will begin transmitting the frame immediately after sufficient writes to the XMIT AREA have occurred. Otherwise, the start of transmission will be delayed until, as a bus master, the adapter has downloaded enough data into its onboard buffer to satisfy the early transmit start threshold requirement. If, however, the threshold value is greater than or equal to the frame length, then transmission will commence once the entire frame is resident on the adapter. Of

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	course, the start of the transmission may be delayed by other queued transmission, or by deferral to network traffic.” Petersen at 29:39-57 “The value for this register may be programmed by the host to optimize performance. If set too low, system latencies or bandwidth limitations may cause the adapter to underrun the network during transmission, causing a partial frame with a guaranteed bad CRC to be transmitted. If the value is set too high, then unnecessary delays will be incurred before the start of transmission. The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver should increase the value on the XMIT START THRESH register. Further underrun indications should cause the driver to continually increase the XMIT START THRESH value. If the XMIT START THRESH value is increased to a value of greater than the maximum length expected by the system, then the early transmit start features should be disabled by writing a zero to the XMIT START THRESH register.” Petersen at Claim 1 “For a system transmitting frames of data across a communications medium; an apparatus comprising: buffer memory for storing data of frames composed by the host computer for transmission on the communications medium; means, having a host system interface, for transferring data of frames to the buffer memory; means, coupled with the buffer memory, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory; means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data of the frame to the buffer memory from the host computer; transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory and supplying retrieved data for transmission on the communications medium; and

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	underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition.” Petersen at Claim 10 “An apparatus for controlling communication between a host system and a network transceiver coupled with a network, comprising: a buffer memory; host interface means, having an interface to the host system, for transferring data between the host system and the buffer memory; means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory; and means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer; network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission; and control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value.” Petersen at Claim 18 “An apparatus for controlling communication between a host system and a network transceiver coupled with a network, comprising: a buffer memory, including a transmit descriptor buffer for storing transmit descriptors identifying data in the host system to be transmitted and including immediate data, and a transmit data buffer for buffering data of frames transferred from the host system; host interface means, having an interface to the host system, for transferring transmit descriptors and data of frames between the host system and the buffer memory and including means,

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	responsive to transmit descriptors in the transmit descriptor buffer, for downloading data of frames from the host system to the transmit data buffer; means, coupled with the buffer memory, for monitoring the immediate data in transmit descriptors in the transmit descriptor buffer and the downloading of data of a frame to the transmit data buffer to make a threshold determination of an amount of data of the frame transferred to the buffer memory; and means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer; network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission; and underrun control means, coupled with the network interface means, for detecting an underrun condition in which the host interface means in downloading data to the transmit data buffer falls behind the network interface means in transferring data to the transceiver, and for supplying a bad frame signal to the network transceiver in response to the underrun condition.” To the extent Petersen does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Petersen. Further, one of ordinary skill in the art would have been motivated to modify Petersen or combine it with any of the present prior art references found in Defendant’s Invalidity Contentions and any supplements thereto and the relevant section charts for other prior art for the ’800 Patent in a manner that would result in the subject matter of this limitation given, at the very least, the person’s understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Petersen.
[12.e] the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches the first optimal	Petersen discloses and/or renders obvious this limitation based on at least the following citations. See, e.g.: • Petersen at Abstract “Early initiation of transmission of data in a network interface that includes a dedicated transmit buffer is provided in a system which includes logic for transferring frames of data composed by the

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amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches the second optimal amount	host computer into the transmit buffer. The amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit data buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to transfer of all of the data of the frame into the transmit buffer. The monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value. Thus, the threshold value may be set by the host system to optimize performance in a given setting.” • Petersen at 1:17-21 “The present invention relates to interfaces between communications networks and data processing systems; in particular, systems which involve the transmission of packets or frames of data across a communications network.” • Petersen at 1:36-54 “Some network adapter interfaces include dedicated transmit buffers into which a frame of data composed by the sending system can be downloaded by the sending system. The frame is then stored in the transmit data buffer until the media access control functions associated with transmitting the frame on the network have successfully transmitted the frame, or cancelled the frame transmission. If the frame transmission is cancelled, the data may be retained in the transmit data buffer until the sending system initiates a second attempt to transmit the frame. Transmit data buffers are to be distinguished from first-in-first-out FIFO systems, in which the sending system downloads data of a frame into the FIFO, while the network adapter unloads the FIFO during a transmission. The data in FIFOs cannot be retained and reused by the media access control functions, or by the host, like data in transmit data buffers.” • Petersen at 2:7-10 “It is desirable to provide the advantages of a transmit data buffer, while maintaining the communications throughput available from the simpler FIFO based systems.” • Petersen at 2:14-34

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	“The present invention provides for the early initiation of transmission of data in a network interface that includes a dedicated transmit buffer. The system includes logic for transferring frames of data composed by the host computer into the transmit buffer. Also, the amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to the transfer of all of the data of the frame into the transmit buffer. In one aspect of the invention, the monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value and logic for posting status information to the host. Thus, the threshold value may be set by the host system to optimize performance using the alterable threshold store and the posted status information.” • Peterson at 2:44-55 “When the adapter begins processing of a transmit descriptor, it retrieves immediate data from the descriptor itself, and begins a download process into the transmit data buffer of data identified in the descriptor. The threshold logic determines the amount of immediate data from the descriptor, and monitors the downloading of data of the frame into the download area. When the combination meets the threshold, then actual transmission of the frame is initiated. Thus, transmission of a frame may be initiated before the complete frame has been downloaded into the download area.” • Peterson at 3:59-65 “FIG. 1 illustrates a data communication system according to the present invention with a controller circuit using a dedicated transmit buffer memory which is automatically enabled to begin transmission of a frame on the network when the number of bytes available in the transmit buffer memory exceeds a preprogrammed threshold.” • Peterson at 4:11-17 “The adapter 6 also includes early transmit logic 6A for monitoring the transfer of data from the host system 1 into the adapter memory 9. The early transmit logic 6A makes a threshold

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	determination for a given frame being transferred from the host 1 into the adapter memory 9. When the threshold is met, then the adapter 6 begins transmitting the frame across the network.” • Petersen at 4:23-49 “FIG. 2 illustrates the functional components of the early transmit system according to the present invention. In FIG. 2, a number of functional blocks are represented. The host computer or sending system 30 communicates with a host interface logic 31, receiving data as indicated by line 32 and control signals as indicated by line 33. The host interface logic 31 supplies data to a transmit buffer 34 across line 35. Also, threshold logic 36 is coupled with the host interface logic 31 to monitor the transfer of data from the host computer 30 into the frame buffer 34. The line 37 indicates the coupling of the threshold logic 36 to the host interface logic 31. The threshold logic makes the threshold determination and generates a signal as indicated by line 38 to transmit logic 39 including, for instance, media access control MAC logic. The transmit logic 39 receives data from the buffer 34 across lines 40 and supplies that data as indicated by line 41 to the network medium 42. Coupled with the threshold logic 36 is a threshold store 43 which stores a threshold value which indicates an amount of data of a frame that must be resident in the frame buffer 34 before transmission of that frame may be initiated by the transmit DMA logic and MAC 39. The threshold store 43, in a preferred system, is dynamically programmable by the host computer 30. In this embodiment, the threshold store 43 is a register accessible by the host through the interface logic 31.” • Petersen at Fig. 2

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	FIG. -2 • Petersen at Fig. 1

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	FIG. -1 Petersen at 4:61-5:13 “In operation, the host computer composes a frame of data to be transmitted on the network medium 42. The host computer 30 then identifies that frame through the host interface 31. The host interface coupled with the identifiers of the frame move data from the host computer 30 into the buffer 34 according to the description of the frame. The threshold logic 36 monitors the transfer of data into the buffer 34. When the threshold amount of data is resident in the buffer 34, then the transmit logic 39 is instructed to begin transmission of the frame. The transmit logic 39 then begins retrieving data from the buffer 34 to support transmission of the frame on the medium 42. This operation begins before the entire frame has been transferred from the host computer 30 into the buffer 34, if the transmit logic 39 is available to transmit the frame subject of the ongoing download from the host

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	computer 30, the frame being downloaded into the buffer 34 is larger than the threshold set by the threshold store 43, and the host computer 30 indicates that immediate transmission of the data is desired.” • Petersen at 10:14-37 “The upload DMA module 57 performs data transfers from the receive buffer through the RAM interface 50 to the host system. Thus, the receive ring buffer is managed by the receive DMA module 63 and interpreted by the upload DMA 57. Actual bus master transfers are carried out by the EISA master interface module 55. The upload DMA module 67 [sic] interprets data structures deposited in the receive ring buffer by the receive DMA module 63 including the location and length of a received frame. It also reads the transfer descriptor which is defined by the host system to determine how many bytes of the frame to transfer, and where in the host memory to transfer the frame. The upload DMA module 57 requests bus master cycles from the EISA master interface module 55 in response to valid transfer requests deposited by the host. The upload DMA module 57 also utilizes an interlock between the receive DMA module 63 and the upload DMA module 57, to reduce the transfer rate to the host system to prevent "getting ahead" of the frame being received through the receive DMA module 63. Finally, this module generates interrupts indicating completion of a transfer for use by the host.” • Petersen at 18:31-40 “The actual frame transmission onto the network will commence when two conditions are met: (1) the XMIT START THRESH (described below) condition has been met, or, if XMIT START THRESH is zero, when the entire frame has been copied to the adapter's RAM, and (2) when there are no previously queued transmit requests. If more than XMIT START THRESH bytes of immediate data are written to XMIT AREA, then network transmission may begin before XMIT QUEUE STATUS is read.”

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	• Petersen at 21:11-39 “H. XMIT START THRESH XMIT START THRESH provides for an early start of transmission. The XMIT START THRESH register is used to specify the number of transmit bytes that must reside on the adapter before it will start transmission. Values greater than the maximum frame length will prevent this function from operating properly. The method for disabling this function is to set the register to zero. Bytes are counted starting with the first byte of the destination field of the transmit frame. The number of bytes considered to be available is the sum of the immediate data written to XMIT AREA by the host and those bytes transferred to the transmit data buffers in the adapter using bus master DMA operations. The transmit request will be posted immediately after XMIT START THRESH transmit frame bytes are made available from the immediate data or when the adapter has bus-mastered XMIT START THRESH-XMIT IMMED LEN bytes onto the adapter. The number of bytes resident on the adapter must be equal to or greater than the value in XMIT START THRESH for the transmission to commence, unless the total frame size is less than XMIT START THRESH. In that case, the frame will begin transmission when the entire frame has been copied to the adapter. The actual transmission of the frame may be delayed by previous pending transmit frames and by deferrals to network traffic. This register is set to zero during a reset.” • Petersen at 29:12-34 “XMIT START THRESH is used to specify the number of bytes of the transmit frame that must reside on the adapter, either as immediate data or as data transferred onto the adapter via bus master data transfers, or as a combination of the two, before the adapter can commence with the media access control functions associated with transmitting the frame. If the number of immediate data bytes expected by the adapter (as determined by the value written to the XMIT IMMEDIATE LENGTH field of the XMIT AREA) exceeds the value set in XMIT START THRESH, then the adapter will begin transmitting the frame immediately after sufficient writes to the XMIT AREA have occurred. Otherwise, the start of transmission will be delayed until, as a bus master, the adapter has downloaded enough data into its onboard buffer to satisfy the early transmit start threshold requirement. If, however, the threshold value is greater than or equal to the frame length, then transmission will commence once the entire frame is resident on the adapter. Of

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	course, the start of the transmission may be delayed by other queued transmission, or by deferral to network traffic." - Petersen at Fig. 12 FIG. - 12 - Petersen at Claim 1 "For a system transmitting frames of data across a communications medium; an apparatus comprising: buffer memory for storing data of frames composed by the host computer for transmission on the communications medium; means, having a host system interface, for transferring data of frames to the buffer memory;

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	means, coupled with the buffer memory, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory; means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data of the frame to the buffer memory from the host computer; transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory and supplying retrieved data for transmission on the communications medium; and underrun control logic, which detects a condition in which the means for transferring falls behind the transmit logic, and supplies a bad frame signal to the communications medium in response to the underrun condition.” • Petersen at Claim 10 “An apparatus for controlling communication between a host system and a network transceiver coupled with a network, comprising: a buffer memory; host interface means, having an interface to the host system, for transferring data between the host system and the buffer memory; means, coupled with the buffer memory and including a host system alterable threshold store for storing a threshold value, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory; and means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer; network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission; and control means, coupled with the network interface means, for posting status information for use by the host system, as feedback for optimizing the threshold value.”

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	• Petersen at Claim 18 “An apparatus for controlling communication between a host system and a network transceiver coupled with a network, comprising: a buffer memory, including a transmit descriptor buffer for storing transmit descriptors identifying data in the host system to be transmitted and including immediate data, and a transmit data buffer for buffering data of frames transferred from the host system; host interface means, having an interface to the host system, for transferring transmit descriptors and data of frames between the host system and the buffer memory and including means, responsive to transmit descriptors in the transmit descriptor buffer, for downloading data of frames from the host system to the transmit data buffer; means, coupled with the buffer memory, for monitoring the immediate data in transmit descriptors in the transmit descriptor buffer and the downloading of data of a frame to the transmit data buffer to make a threshold determination of an amount of data of the frame transferred to the buffer memory; and means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame, prior to transfer of all the data of the frame to the buffer memory from the host computer; network interface means, having an interface to the network transceiver and responsive to the means for initiating, for transferring data between the buffer memory and the network transceiver for transmission; and underrun control means, coupled with the network interface means, for detecting an underrun condition in which the host interface means in downloading data to the transmit data buffer falls behind the network interface means in transferring data to the transceiver, and for supplying a bad frame signal to the network transceiver in response to the underrun condition.” To the extent Petersen does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Petersen. Further, one of ordinary skill in the art would have been motivated to modify Petersen or combine it with any of the present prior art references found in Defendant’s Invalidity Contentions and any supplements thereto and the relevant section charts for other prior art for the ’800 Patent in a manner that would result in the subject matter of this limitation

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	given, at the very least, the person’s understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Petersen.
[12.f] wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave,	Petersen discloses and/or renders obvious this limitation based on at least the following citations. See, e.g.: Petersen at Abstract “Early initiation of transmission of data in a network interface that includes a dedicated transmit buffer is provided in a system which includes logic for transferring frames of data composed by the host computer into the transmit buffer. The amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit data buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to transfer of all of the data of the frame into the transmit buffer. The monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value. Thus, the threshold value may be set by the host system to optimize performance in a given setting.” Petersen at 2:14-34 “The present invention provides for the early initiation of transmission of data in a network interface that includes a dedicated transmit buffer. The system includes logic for transferring frames of data composed by the host computer into the transmit buffer. Also, the amount of data of a frame which is downloaded by the host to the transmit buffer is monitored to make a threshold determination of an amount of data of the frame resident in the transmit buffer. The network interface controller includes logic for initiating transmission of the frame when the threshold determination indicates that a sufficient portion of the frame is resident in the transmit buffer, and prior to the transfer of all of the data of the frame into the transmit buffer. In one aspect of the invention, the monitoring logic includes a threshold store, which is programmable by the host computer for storing a threshold value and logic for posting status information to the host. Thus, the threshold value may be set by the host system to optimize performance using the alterable threshold store and the posted status information.”

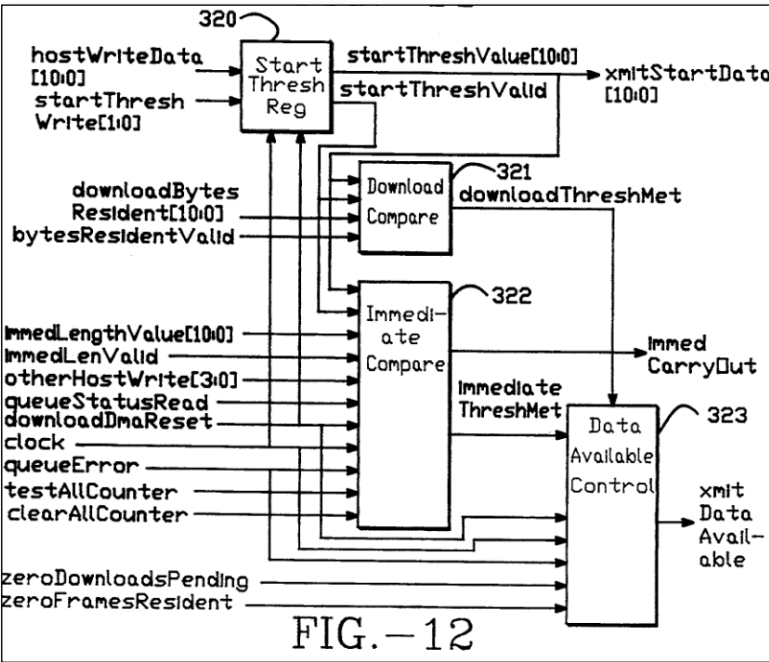
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	• Peterson at 4:56-60 “The transmit logic 39 also supplies status information across line 44 to the host interface logic 31, for posting to the host system. The status information includes indications of underrun conditions and may be used by the host to optimize the value in the threshold store 43.” • Petersen at 18:31-40 “The actual frame transmission onto the network will commence when two conditions are met: (1) the XMIT START THRESH (described below) condition has been met, or, if XMIT START THRESH is zero, when the entire frame has been copied to the adapter's RAM, and (2) when there are no previously queued transmit requests. If more than XMIT START THRESH bytes of immediate data are written to XMIT AREA, then network transmission may begin before XMIT QUEUE STATUS is read.” • Petersen at 21:11-39 “H. XMIT START THRESH XMIT START THRESH provides for an early start of transmission. The XMIT START THRESH register is used to specify the number of transmit bytes that must reside on the adapter before it will start transmission. Values greater than the maximum frame length will prevent this function from operating properly. The method for disabling this function is to set the register to zero. Bytes are counted starting with the first byte of the destination field of the transmit frame. The number of bytes considered to be available is the sum of the immediate data written to XMIT AREA by the host and those bytes transferred to the transmit data buffers in the adapter using bus master DMA operations. The transmit request will be posted immediately after XMIT START THRESH transmit frame bytes are made available from the immediate data or when the adapter has bus-mastered XMIT START THRESH-XMIT IMMED LEN bytes onto the adapter. The number of bytes resident on the adapter must be equal to or greater than the value in XMIT START THRESH for the transmission to commence, unless the total frame size is less than XMIT START THRESH. In that case, the frame will begin transmission when the entire frame has been copied to the adapter. The actual transmission of the frame may be delayed by previous pending transmit frames and by deferrals to network traffic. This register is set to zero during a reset.”

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	• Petersen at 24:59-25:18 “FIG. 12 is a block diagram of the transmit start control logic. The transmit start control logic includes a start threshold register 320, and a download compare block 321 which compares the value of the start threshold with the download bytes resident value generated in the data path arithmetic of FIG. 11. Also, an immediate data comparator 322 is included to perform the comparison in the event that immediate data is present in the transmit descriptor. Finally, a data available control block 323 is included which generates the xmitDataAvailable signal for supply to the transmit DMA logic block of the adapter. The transmit start control logic in FIG. 12 is responsible for generating the xmitDataAvailable signal, which is supplied to the transmit DMA module to indicate that there is data available to be transmitted onto the network. The xmitDataAvailable signal is asserted under three conditions: (1) there are one or more complete frames resident on the adapter ready to be transmitted; (2) there are no complete frames on the adapter, but the number of bytes resident for a frame currently being downloaded is greater than the value in the transmit start threshold register; and (3) there are no complete frames on the adapter, and there are no pending download operations, and the number of immediate bytes resident for the frame currently being written to the transmit area register is greater than the value of transmit start threshold.” • Petersen at Fig. 12

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	FIG. - 12 Petersen at 29:12-34 “XMIT START THRESH is used to specify the number of bytes of the transmit frame that must reside on the adapter, either as immediate data or as data transferred onto the adapter via bus master data transfers, or as a combination of the two, before the adapter can commence with the media access control functions associated with transmitting the frame. If the number of immediate data bytes expected by the adapter (as determined by the value written to the XMIT IMMEDIATE LENGTH field of the XMIT AREA) exceeds the value set in XMIT START THRESH, then the adapter will begin transmitting the frame immediately after sufficient writes to the XMIT AREA have occurred. Otherwise, the start of transmission will be delayed until, as a bus master, the adapter has downloaded enough data into its onboard buffer to satisfy the early transmit start threshold requirement. If, however, the threshold value is greater than or equal to the

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	frame length, then transmission will commence once the entire frame is resident on the adapter. Of course, the start of the transmission may be delayed by other queued transmission, or by deferral to network traffic.” To the extent Petersen does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Petersen. Further, one of ordinary skill in the art would have been motivated to modify Petersen or combine it with any of the present prior art references found in Defendant’s Invalidity Contentions and any supplements thereto and the relevant section charts for other prior art for the ’800 Patent in a manner that would result in the subject matter of this limitation given, at the very least, the person’s understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Petersen.
[12.g] wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data	Petersen discloses and/or renders obvious this limitation based on at least the following citations. See, e.g.: • Peterson at 4:56-60 “The transmit logic 39 also supplies status information across line 44 to the host interface logic 31, for posting to the host system. The status information includes indications of underrun conditions and may be used by the host to optimize the value in the threshold store 43.” • Petersen at 18:31-40 “The actual frame transmission onto the network will commence when two conditions are met: (1) the XMIT START THRESH (described below) condition has been met, or, if XMIT START THRESH is zero, when the entire frame has been copied to the adapter's RAM, and (2) when there are no previously queued transmit requests. If more than XMIT START THRESH bytes of immediate data are written to XMIT AREA, then network transmission may begin before XMIT QUEUE STATUS is read.” • Petersen at 21:11-39 “H. XMIT START THRESH XMIT START THRESH provides for an early start of transmission.

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correctness, priority, and data delivery.	The XMIT START THRESH register is used to specify the number of transmit bytes that must reside on the adapter before it will start transmission. Values greater than the maximum frame length will prevent this function from operating properly. The method for disabling this function is to set the register to zero. Bytes are counted starting with the first byte of the destination field of the transmit frame. The number of bytes considered to be available is the sum of the immediate data written to XMIT AREA by the host and those bytes transferred to the transmit data buffers in the adapter using bus master DMA operations. The transmit request will be posted immediately after XMIT START THRESH transmit frame bytes are made available from the immediate data or when the adapter has bus-mastered XMIT START THRESH-XMIT IMMED LEN bytes onto the adapter. The number of bytes resident on the adapter must be equal to or greater than the value in XMIT START THRESH for the transmission to commence, unless the total frame size is less than XMIT START THRESH. In that case, the frame will begin transmission when the entire frame has been copied to the adapter. The actual transmission of the frame may be delayed by previous pending transmit frames and by deferrals to network traffic. This register is set to zero during a reset.” • Petersen at 24:59-25:18 “FIG. 12 is a block diagram of the transmit start control logic. The transmit start control logic includes a start threshold register 320, and a download compare block 321 which compares the value of the start threshold with the download bytes resident value generated in the data path arithmetic of FIG. 11. Also, an immediate data comparator 322 is included to perform the comparison in the event that immediate data is present in the transmit descriptor. Finally, a data available control block 323 is included which generates the xmitDataAvailable signal for supply to the transmit DMA logic block of the adapter. The transmit start control logic in FIG. 12 is responsible for generating the xmitDataAvailable signal, which is supplied to the transmit DMA module to indicate that there is data available to be transmitted onto the network. The xmitDataAvailable signal is asserted under three conditions: (1) there are one or more complete frames resident on the adapter ready to be transmitted; (2) there are no complete frames on the adapter, but the number of bytes resident for a frame currently being downloaded is greater than the value in the transmit start threshold register; and (3) there are no complete frames on the adapter, and there are no pending download operations, and the number of

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	immediate bytes resident for the frame currently being written to the transmit area register is greater than the value of transmit start threshold.” - Petersen at Fig. 12  FIG. - 12 - Petersen at 29:12-34 “XMIT START THRESH is used to specify the number of bytes of the transmit frame that must reside on the adapter, either as immediate data or as data transferred onto the adapter via bus master data transfers, or as a combination of the two, before the adapter can commence with the media access control functions associated with transmitting the frame. If the number of immediate data bytes expected by the adapter (as determined by the value written to the XMIT IMMEDIATE LENGTH field of the XMIT AREA) exceeds the value set in XMIT START THRESH, then the adapter will begin transmitting the frame immediately after sufficient

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	writes to the XMIT AREA have occurred. Otherwise, the start of transmission will be delayed until, as a bus master, the adapter has downloaded enough data into its onboard buffer to satisfy the early transmit start threshold requirement. If, however, the threshold value is greater than or equal to the frame length, then transmission will commence once the entire frame is resident on the adapter. Of course, the start of the transmission may be delayed by other queued transmission, or by deferral to network traffic.” • Petersen at 29:39-57 “The value for this register may be programmed by the host to optimize performance. If set too low, system latencies or bandwidth limitations may cause the adapter to underrun the network during transmission, causing a partial frame with a guaranteed bad CRC to be transmitted. If the value is set too high, then unnecessary delays will be incurred before the start of transmission. The adapter generates an indication of an underrun condition which is made available to the host through the XMIT FAILURE register. If such an underrun indication occurs, then the host driver should increase the value on the XMIT START THRESH register. Further underrun indications should cause the driver to continually increase the XMIT START THRESH value. If the XMIT START THRESH value is increased to a value of greater than the maximum length expected by the system, then the early transmit start features should be disabled by writing a zero to the XMIT START THRESH register.” To the extent Petersen does not expressly disclose this limitation, a person of ordinary skill in the art would have determined that this limitation is either inherent and/or obvious to one of ordinary skill in the art in view of the teachings of Petersen. Further, one of ordinary skill in the art would have been motivated to modify Petersen or combine it with any of the present prior art references found in Defendant’s Invalidity Contentions and any supplements thereto and the relevant section charts for other prior art for the ’800 Patent in a manner that would result in the subject matter of this limitation given, at the very least, the person’s understanding of the state of the art, the problems addressed and solved in the prior art, and the teachings of Petersen.