

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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QUALCOMM INCORPORATED and  
SAMSUNG ELECTRONICS CO., LTD.  
Petitioners

v.

NETWORK SYSTEM TECHNOLOGIES, LLC  
Patent Owner

Patent No. 7,594,052

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*Inter Partes* Review No. IPR2024-00343

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**DECLARATION OF DR. ERIK CHMELAR**

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## **I. INTRODUCTION**

1. I have been retained on behalf of Plaintiff Network System Technologies, LLC (“NST”), as an expert consultant.

2. As part of this work, I have been requested by counsel for NST to provide this declaration concerning the technical subject matter relevant to the *inter partes* review (“IPR”) petition of U.S. Patent No. 7,594,052 (the “’052 patent”) filed by Qualcomm Incorporated (“Qualcomm”) and Samsung Electronics Co., Ltd. (“Samsung”) (collectively, “Petitioners”).

3. I have provided an exemplary, but not exhaustive, summary of materials that I considered or relied upon in preparing this report, besides my personal knowledge and experience, in Appendix. The paragraphs below may identify additional materials considered or relied upon not listed in Appendix. I reserve the right to rely on additional documents as I become aware of them and to respond to documents relied on by Petitioners’ expert.

4. I am being compensated for my time in the amount of \$600 per hour. I have no financial interest in NST or the ’052 patent, and my compensation is not contingent upon the substance of my declaration, any statements or opinions made, or the outcome of this matter.

## **II. EXPERT QUALIFICATIONS AND BACKGROUND**

5. In 2000, I received a B.S. degree in Electrical Engineering from Michigan Technological University with the highest distinction (summa cum laude). In 2001, I received an M.S. degree in Electrical Engineering from Stanford University, with a focus on computer networks (EE284 Introduction to Computer Networks, EE384A Internet Protocols, EE384S Network Architectures, and EE384S Multimedia Networks). In 2004, I received a Ph.D. degree in Electrical Engineering from Stanford University, with a primary focus on very large-scale integrated (VLSI) systems that culminated in a dissertation entitled “The Test and Diagnosis of Field-programmable Gate Arrays, advised by Dr. Edward J. McCluskey, and with conclusion of a secondary focus on computer networks (EE384X Packet Switch Architectures). While studying at Stanford University from 2000–2004, I taught undergraduate and graduate level courses as a Teaching Assistant (EE284 Introduction to Computer Networks, EE384A Internet Protocols and Standards, Digital Design Laboratory EE121, and E40 Introduction to Electronics), and I was employed as a Research Assistant in the Center for Reliable Computing. In 2011, I received a second B.S. degree in Chemical Physics from Saginaw Valley State University in 2011 with the highest distinction (summa cum laude).

6. During my undergraduate and graduate studies, I was additionally employed at several product-technology companies. From 1999–2002, I was employed as a Manufacturing Engineer at Cisco Systems, Inc, where I oversaw functional testing of layer-2 and layer-3 network switches and determined root-cause failures thereof. During the summers of 2002 and 2003, I was employed as a Product Test Engineer intern at Xilinx, Inc., where I researched and developed software tools to detect and diagnose physical hardware defects in FPGAs.

7. After earning my Ph.D., I was employed at LSI Corp. (now Broadcom, Inc.) from 2004–2012 as a Staff Software Engineer in the Advanced Technology Development department, where I conducted R&D for very large-scale integrated (VLSI) systems and serializer-deserializer (SerDes) circuits for high-speed data communications, for which I was granted approximately 20 U.S. patents. During this period of employment at LSI Corp., I also taught at several Universities. From 2006–2008, I was a consulting Assistant Professor in the Electrical Engineering and Computer Science department at Stanford University, where I advised PhD students in the Center for Reliable Computing on the test and reliability of VLSI systems, and created and taught a PhD-level course on clock and data recovery (CDR) for digital communications (EE391 Clock and Data Recovery Architectures). From 2009–2012, I was an Adjunct Professor in the Electrical and Computer Engineering department at Saginaw Valley State University, where I taught several

undergraduate courses in data communications and computer hardware (ECE455 Data Communications, ECE368 Computer Engineering, ECE368L Computer Engineering Lab, ECE216 Digital Circuits, and ECE216L Digital Circuits Lab).

8. From 2012–2015, I was employed at Stryker Instruments as a Senior Principal Engineer in the Advanced Development department, where I conducted and supervised R&D of computationally intelligent medical instruments and surgical technologies, and I delivered working prototypes for bio-photonic devices and boundary-constraint surgical robotics.

9. From 2015–2018, I was employed at Interdigital, Inc. as a Senior Manager of Innovation Partners, where I conducted and supervised R&D of 5<sup>th</sup> generation wireless (5G) network-enabled technologies including the Internet of Things, connected/autonomous vehicles, and augmented/virtual reality infrastructure, and I managed scientists and engineers to create over 100 new-invention disclosures for patent protection.

10. From 2019–present, I have provided consulting services to a major patent-licensing corporation as a Technical Expert in the areas of semiconductor circuits, microchips, and data communications. My consulting services have included determining whether and how specific patent claims within the aforementioned areas read on various products or product features. I analyze patents, technical specifications, product white papers, and product marketing materials to

produce detailed claim charts used by attorneys to formulate infringement opinions and licensing decisions. I have also performed technology market analysis and developed detailed technology landscapes and roadmaps in the aforementioned areas.

11. I have written technical publications dating back to 2003 on topics in the areas of semiconductor circuits, microchips, and data communications. I have written technical articles published in peer reviewed professional journals, trade journals, and proceedings of peer-reviewed conferences. I have presented at several technical symposia and technical conferences on topics in the aforementioned areas.

12. I am or have been a member or senior member of several professional organizations, including the Institute of Electrical & Electronic Engineers (IEEE), the Association for Computing Machinery (ACM), the American Society of Mechanical Engineers (ASME), the International Society of Optics & Photonics (SPIE), and the American Chemical Society (ACS).

13. I served as a Program Evaluator for the Accreditation Board of Engineering and Technology (ABET) from 2013–2018. As a Program Evaluator, I was responsible for determining ABET accreditation for university engineering programs categorized as Electrical Engineering programs and Computer Engineering programs.

14. I served as an Industry Mentor for National Science Foundation (NSF) I-Corps program in 2013, and served as an Instructor for the same in 2015. In these roles, I provided industry and technical guidance to engineers, inventors, and entrepreneurs launching technology startups.

15. I hold approximately 30 U.S. Patents, many of which concern technologies in the areas of semiconductor circuits, microchips, and data communications.

16. Additional details on my background and experience can be found in my *curriculum vitae*, attached hereto as EX2002.

### **III. UNDERSTANDING OF LEGAL PRINCIPLES**

#### **A. Validity Generally**

17. I have a general understanding of validity based on my experience with patents, my career experience, and my discussions with counsel. I have also reviewed the legal principles used to determine invalidity, such as those set forth in the AIPLA Model Patent Jury Instructions. See, e.g., <https://www.aipla.org/home/news-publications/model-patent-jury-instructions>).

#### **B. Prior Art**

18. I have a general understanding of prior art and priority dates based on my experience with patents, my career experience, and my discussions with counsel.

19. I understand that inventors may be entitled to a priority date earlier than an actual date of filing of a patent application that provides written description support for a particular claim to the extent that they can show a complete possession of such a particular claimed invention at such an earlier priority date, and reasonable diligence to reduce such a particular claimed invention to practice between such an earlier priority date and such an actual date of filing. I understand that if Plaintiff contends that particular claims are entitled to an earlier priority date than the actual date of filing, then Plaintiff has the burden to prove this contention with specificity.

20. I understand that an invention by another must be made before the priority date of a particular patent claim in order to qualify as “prior art” under 35 U.S.C. § 102 or 35 U.S.C. § 103. I also understand that a printed publication or a product usage must be publicly available before the priority date of a particular patent claim in order to qualify as “prior art” under 35 U.S.C. § 102(a), that a printed publication or a product usage or offer for sale must be publicly available in the United States more than one year prior to the actual date of filing of a patent application that provides written description support for a particular claim in order to qualify as “prior art” under 35 U.S.C. § 102(b), and that the invention by another must be described in an application for patent filed in the United States before the priority date of a particular patent claim in order to qualify as “prior art” under 35

U.S.C. § 102(e). I understand that Petitioners have the burden of proving that any particular reference or product usage or offer for sale is prior art.

**C. Anticipation**

21. I have a general understanding of anticipation based on my experience with patents, my career experience, and my discussions with counsel.

22. I understand that the anticipation analysis is a two-step process. The first step is to determine the meaning and scope of the challenged claims. Each claim must be viewed as a whole, and it is improper to ignore any element of the claim. For a claim to be anticipated under U.S. patent law: (1) each and every claim must be identically disclosed, either explicitly or inherently, in a single prior art reference; (2) the claim elements disclosed in the single prior art reference must be arranged in the same way as in the claims; and (3) the identical invention must be disclosed in the single prior art reference, in as complete detail as forth in the claim. Where even one element is not disclosed in a reference, the anticipation contention fails. Moreover, to serve as an anticipatory reference, the reference itself must be enabled. In other words, the reference must provide enough information so that a person of ordinary skill in the art (“POSITA”) can practice the subject matter of the reference without undue experimentation.

23. I further understand that where a prior art reference fails to explicitly disclose a claim element, the prior art reference inherently discloses the claim

element only if the prior art reference must necessarily include the undisclosed claim element. Inherency may not be established by probabilities or possibilities. The fact that an element may result from a given set of circumstances is not sufficient to prove inherency. I have applied these principles in forming my opinions in this matter.

24. I further understand that a dependent claim incorporates each and every limitation of the claim from which it depends. Thus, my understanding is that if a prior art reference fails to anticipate an independent claim, then that prior art reference also necessarily fails to anticipate all dependent claims that depend from that independent claim.

**D. Obviousness**

25. I have a general understanding of obviousness based on my experience with patents, my career experience, and my discussions with counsel.

26. I understand that a patent claim is invalid under 35 U.S.C. § 103 as being obvious only if the differences between the claimed invention and the prior art such that the subject matter as a whole would have been obvious at the time of invention to a POSITA. An obviousness analysis requires consideration of four factors: (1) scope and content of the prior art relied upon to challenge patentability; (2) differences between the prior art and the claimed invention; (3) level of ordinary skill in the art at the time of the invention; and (4) the objective evidence of non-obviousness, such as commercial success, unexpected results, the failure of others to

achieve the results of the invention, a long-felt need which the invention fills, copying of the invention by competitors, praise for the invention, skepticism for the invention, or independent development.

27. I understand that a prior art reference is proper to use in an obviousness determination if the prior art reference is analogous art to the claimed invention. I understand that a prior art reference is analogous art if at least one of the following two circumstances is met. First, a prior art reference is analogous art if it is from the same field of endeavor as the claimed invention, even if the prior art reference addresses a different problem and/or arrives at a different solution. Second, a prior art reference is analogous art if the prior art reference is reasonably pertinent to problem faced by the inventor, even if it is not in the same field of endeavor as the claimed invention.

28. I understand that it must be shown that a POSITA at the time of the invention would have had a reasonable expectation that a modification or combination of one or more prior art references would have succeeded. Furthermore, I understand that a claim may be obvious in view of a single prior art reference, without the need to combine references, if the elements of the claim that are not found in the reference can be supplied by the knowledge or common sense of one of ordinary skill in the relevant art. However, I understand that it is inappropriate to resolve obviousness issues by a retrospective analysis or hindsight reconstruction of

the prior art and that the use of such hindsight reconstruction is improper in analyzing the obviousness of a patent claim.

29. I further understand that the law recognizes several specific guidelines that inform the obviousness analysis. First, I understand that a hindsight reconstruction approach is not permitted. In other words, it is improper to use post-invention information to help perform the selection and combination of prior art references, and it is also improper to use the listing of elements in a claim as a blueprint to identify selected portions of different prior art references in an attempt to show that the claim is obvious.

30. Second, I understand that any prior art that specifically teaches away from the claim subject matter points to non-obviousness. In other words, prior art that would lead a POSITA to a specifically different solution than the claimed invention points to non-obviousness. Conversely, I understand that any prior art that contains any teaching, suggestion, or motivation to modify or combine such prior art references points to obviousness of such a modification or combination.

31. Third, while many combinations of the prior art may be “obvious to try,” I understand that any obvious-to-try analysis will not render a patent invalid unless it is shown that the possible combinations are: (1) sufficiently small in number so as to be reasonable to include that the combination would have been selected; and (2) such

that the combination would have been believed to be one that would produce predictable and well understood results.

32. Fourth, I understand that if a claimed invention that arises from the modification or combination of one or more prior art references uses known methods or techniques that yield predictable results, then that factor also points to obviousness.

33. Fifth, I understand that if a claimed invention that arises from the modification or combination of one or more prior art references is the result of known work in one field prompting variations of it for use in the same field or a different one based on design incentives or other market forces that yield predictable variations, then that factor also points to obviousness.

34. Sixth, I understand that if a claimed invention that arises from the modification or combination of one or more prior art references is the result of routine optimization, then that factor also points to obviousness.

35. Seventh, I understand that if a claimed invention that arises from the modification or combination of one or more prior art references is the result of a substitution of one known prior art element for another known prior art element to yield predictable results, then that factor also points to obviousness.

36. I further understand that a dependent claim incorporates each and every limitation of the claim from which it depends. Thus, my understanding is that if a prior art reference fails or a combination of prior art references fail to render obvious

an independent claim, then that prior art reference fails or that combination of prior art references fail to render obvious all dependent claims that depend from the independent claim.

#### **IV. PERSON OF ORDINARY SKILL IN THE ART**

37. I understand that, in assessing the level of ordinary skill, one may consider several factors, including: (1) the education level of the inventor; (2) the education level of active workers in the field; (3) the types of problems encountered in the art; (4) prior art solutions to these problems; (5) the rate of innovation in the field; and (6) the sophistication of the technology.

38. I understand that the District Court in the TI Litigation adopted the following identification of a person of ordinary skill in the art (“POSITA”): “a POSITA would have at least a Bachelor’s degree in electrical engineering, computer engineering, or a related field, and at least two years of work experience in the field of SoC and NoC technologies.” Claim Construction Order (Dkt. 150) (EX2022). I met and exceeded this level of skill as of around 2002. I have applied the Court’s definition of a POSITA throughout this Report.

#### **V. OVERVIEW OF THE TECHNICAL BACKGROUND AND THE ASSERTED PATENTS**

##### **A. Technical Background**

39. A network-on-chip (“NoC”) is a data communication network on a microchip. In some ways, NoCs are like traditional computer networks, such as local

area networks (“LANs”) and/or wide area networks (“WANs”). For example, both traditional computer networks and NoCs interconnect devices or components: traditional computer networks commonly interconnect discrete devices, such as computers, printers, servers, and so on, whereas NoCs commonly interconnect integrated components, such as processors, cores, caches, memories, input/output (I/O) interfaces, peripherals, and so on. However, implementation of a NoC on a SoC presents many unique challenges, as discussed in more detail below. *Infra*, § VI.B. The components interconnected by a NoC are typically integrated on a very large-scale integrated (“VLSI”) circuit, such as a system-on-chip (“SoC”).

40. An SoC is an integrated circuit in which most or all components of a system are integrated, including memories, processors, high-speed I/O interfaces, and dedicated application-specific logic. *See, e.g.*, EX2003, 1; *see also* EX2004, 4-5. By the early 2000s, certain limitations of statically wired interconnections between components of an SoC were known, and as a result, NoCs were already emerging. *See, e.g.*, EX2004, 7-8, *see also* EX2005. Rather than considering on-chip interconnections as point-to-point wires, they can be abstracted as communication channels over which to transmit data within a “quality-of-service” setting. *See id.*

41. Before describing details of a NoC, it is important to describe how components can be interconnected in an SoC that does not implement a NoC. Interconnections, sometimes called interconnects, traces, wires, and signal lines, are

electrical connections between a first component and a second component. Interconnects that carry similar signals are grouped together into buses, for example interconnects that carry address signals are grouped into an address bus and interconnects that carry data signals are grouped into a data bus. *See* EX2006, 4. A bus can be considered a direct interconnection between components (e.g., the path between a first component and a second component is always the same), where the interconnection may be dedicated or shared. A dedicated bus comprises point-to-point interconnection between components, typically between two components. A shared bus comprises interconnections that can be shared between many components, and requires some type of bus arbitration to resolve conflicts when multiple components attempt to access the shared bus simultaneously.

42. There are several types of bus arbitration methods for shared buses, including centralized and distributed (sometimes called decentralized). In centralized arbitration, a single device, known as a bus controller or bus arbiter, is responsible for managing access to the bus. In distributed arbitration, components compete for access to the bus by sending a request signal to the bus arbiter and waiting for a grant signal. In some distributed arbitration methods, e.g., decentralized, each component has its own priority level, and the component with the highest priority is given access to the bus. A component capable of originating a bus transaction (e.g., requesting control of the bus) is a master component, and a component that cannot originate a

bus transaction (e.g., only listens on the bus for communications intended for it) is a slave component. In large and/or complex SoCs, such shared buses interconnecting master devices and slave devices via bus arbitration may not be sufficiently scalable nor provide enough bandwidth. *See* EX2007, 7, 235.

43. In particular, with increasing quantities of components integrated in SoCs, increasing transistor densities, and increasing clock frequencies, it becomes very difficult to operate all the components synchronously within a same clock domain. This creates a need for a modular approach, where the processing system of the SoC comprises a plurality of relatively independent complex modules. In conventional processing systems, the system modules usually communicate with each other via a shared bus as described above. But as the number of modules increases, shared-bus communication is no longer practical at least because: (1) the large quantity of modules creates too high of an electrical load on the shared bus, and (2) the shared bus forms a communication bottleneck because only one component can control the bus at a time. Consequently, some SoCs implement shared buses that utilize crossbar switches, also called crossbars, cross-point switch, matrix switch, or switch matrix, to achieve higher throughput, with STBus, IBM CoreConnect, and ARM AMBA being several examples of bus standards that may utilize crossbars. *See* EX2007, 320. A crossbar has a plurality of input lines and output lines that form a crossed pattern of intersecting lines between which a connection may be established

by closing a switch located at a given intersection. An  $n$ -input,  $m$ -output crossbar, i.e., an  $n \times m$  crossbar, is the equivalent to a set of  $m$  multiplexers (one per output port), each having  $n$  inputs (one per input port). See EX2007, 332-333. However, a shared bus that utilizes crossbars still has disadvantages. For example, the physical implementation of complex SoCs require large and complex crossbars that are difficult to place-and-route during physical design on the SoC in the areas between the components that implement functional logic of the SoC. See EX2008, 3. An on-chip communication network, e.g., a NoC, is an effective way to overcome some of the aforementioned disadvantages.

44. A NoC interconnect paradigm radically changes the on-chip communication compared to direct interconnects, such as buses or switches. This is because of the multi-hop nature of a network, where components are not directly connected, but separated by one or more network nodes. This is in contrast with buses, where components are directly connected as described above. Several implications of this change include arbitration methods (which can no longer be centralized), and communication properties (e.g., ordering, flow control, and so on). In an SoC that implements a NoC, certain design-specific wiring structures of the SoC, typically the longer “global” wires that interconnect components, are replaced with a general-purpose on-chip communication network. EX2005, 2. Instead of connecting these top-level modules by routing dedicated wires, they are

connected to a network that routes packets between them. *See id.* In doing so, these network-connected modules, or components, can be thought of as “network clients” that communicate with each other through communication channels of a network that provide one or more levels of service, e.g., as may be achieved by various communication properties. *See id.*

45. The 2001 paper by Dally and Towles provides a basic example of a NoC implementation. *See* EX2005, 2-3. It describes dividing a chip into 16 “tiles,” where each tile comprises client logic, such as processors, DSPs, peripheral controllers, memory subsystems, and so on. The client logic within a tile (i.e., nearby logic) may communicate via direct interconnections, but client logic in different tiles (i.e., far-apart logic) must communicate only over the network. In other words, there are no top-level (global) bus-based interconnections, only interconnections provided by the network. Figure 1 of the Dally and Towles paper is reproduced below. *See* EX2005, 2.

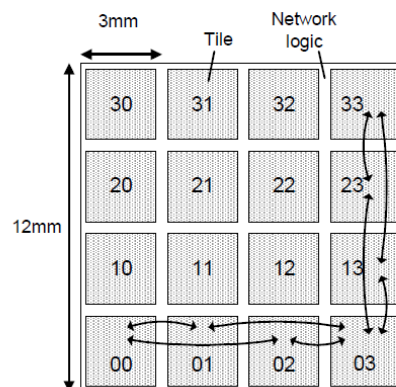


Figure 1 Partitioning the die into module tiles and network logic

46. Each tile interfaces with the network over an input port that is used to insert packets into the network and an output port over which the network delivers packets to the tile (where input and output here refer to packets going in and out of the network, not the tile). Each packet includes a virtual channel field that specifies which virtual channel it may be routed on, to provide different levels of service, and route field to specify a route through the network, i.e., the hops taken from source tile to destination tile. Such a port interface can present a simple and reliable level of service to the network clients. *See* EX2005, 3.

47. Logic local to the network clients can layer higher-level services on top of this interface. For example, this local logic could present a memory read/write service, a flow-controlled data stream, or a logical wire to the client. Local logic can also provide a translation from a destination node to a route. *See* EX2005, 3.

48. The router needed at each tile consists of five input controllers (one for each direction and one for input from the tile) and five output controllers. The router for each tile is distributed across the four edges of a tile with the input and output controller for a given direction (e.g., west) located on that edge of the tile. Figure 2 of the Dally and Towles paper, reproduced below, shows the west input controller and its connection to four output controllers (one for each of the other directions and one for the tile). *See* EX2005, 3.

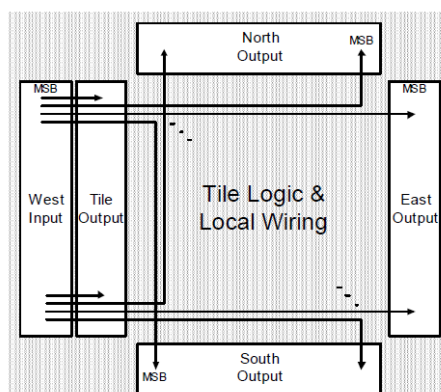


Figure 2 West input connections to output controllers

49. Details of an input controller and output controller are shown in Figure 3 of the Dally and Towles paper, reproduced below. Each input controller has an input buffer and input state logic for each virtual channel. When a head flit (flow control digit, e.g., part of a packet) arrives at each tile, the input controller strips the next entry off the route field and uses these two bits to select one of four output ports. The flit then arbitrates with the other virtual channels on that input port and, if it wins the arbitration, is forwarded to the output port. This arbitration and forwarding takes place in parallel with allocating a virtual channel and checking available buffer space to reduce latency. The output port provides a single stage of buffering for each input port connection. The flits in these buffers arbitrate for the link to the input controller on the next tile. Credits for buffer allocation are piggybacked on flits travelling in the reverse direction. See EX2005, 4.

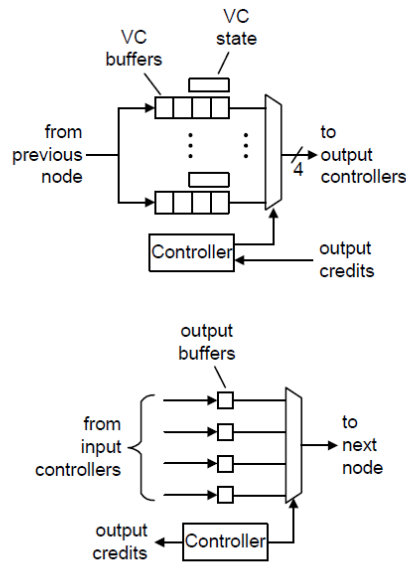


Figure 3 Input (top) and output controllers

50. As indicated earlier, the communication between modules (e.g., components, network clients, etc.) are performed over connections. The specification passages for the '052 patent that utilize the claim term “connection” further indicate that the channels between modules have a set of connection properties. See EX1001 ('052 Patent) at 4:53–55. Some examples of connection properties, which are sometimes called communication properties, are provided below.

The connection properties may include ordering (data transport in order), flow control (a remote buffer is reserved for a connection, and a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data), throughput (a lower bound on throughput is guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data), transmission termination, transaction completion, data correctness, or data delivery.

EX1001 at 4:64–5:5.

51. With such connection properties, on-chip networks are typically able to provide varying levels of communication service, which may be referred to as a quality of service (QoS) levels. “The QoS is a very important feature in the interconnect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic.” EX2007, 325. Traffic here refers to a flow of data between a first module and a second module, for example, a series of data packets transmitted from the first module to the second module. With QoS, different traffic classes can be supported, such as:

- Real time and low latency (RTLL)—Traffic flows that require the lowest possible latency.
- Guaranteed throughput (GT)—Traffic flows that must maintain their throughput over a relatively long time interval.
- Guaranteed bandwidth (GBW)—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval.
- Best effort (BE)—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

EX2007, 326.

## **B. Challenges of On-Chip Networks**

52. The issues and problems of implementing a multi-hop on-chip network interconnect are complex. Prior to the invention of a network-on-chip interconnect, functional blocks of an integrated circuit were typically interconnected using buses or crossbars. However, both buses and crossbars have respective drawbacks, as discussed in more detail below.

53. Buses, such as ARM's Advanced Microcontroller Bus Architecture (AMBA), were an early solution for interconnecting on-chip functional blocks, e.g., initiators and targets. However, "the integration of multiple cores within chips" caused "too many initiators trying to access different targets simultaneously" which "created bottlenecks on the bus." EX2009, 3. Buses also had "latency issues." *Id.* As a result, "[t]he industry wanted to enable concurrent access and more overall system data throughput." *Id.*

54. Following the use of buses, crossbars were introduced as a next interconnect solution. While crossbars cure some of the deficiencies caused by buses, "crossbars require complex control logic to keep track of outstanding transactions" and require "wide data paths for the initiators and targets that need the most throughput as well as signaling for address and control information." EX2009, 3. "To support continued system scaling, crossbars were cascaded with bridges between fabrics" which "carried a significant cost in silicon area" and

“limited clock frequencies and added significant latency to transactions.” *Id.* at 4. Moreover, “during the 2000s, the initiators and targets became so numerous and widely distributed in the physical floorplan of a chip that the crossbar became a physical wiring nightmare.” *Id.*

55. Due to the drawbacks of buses and crossbars, “Network-on-Chip (NoC) technology emerged as a solution to the wiring problem.” EX2009, 5. NoC technology packetizes address and data information on the same wires, thereby allowing transactions to be sent over a smaller number of wires compared to prior interconnect solutions “while maintaining high quality of service for each transmission.” *Id.* NoC technology also contributed to decreased die density by “distributing the interconnect logic throughout the chip rather than having bridges as chokepoints.” *Id.*

56. The ’052 patent describes the distinction between prior interconnects (e.g., busses and crossbars) and a multi-hop interconnect.

NoCs help resolve the electrical problems in new deep-submicron technologies, as they structure and manage global wires. At the same time they share wires, lowering their number and increasing their utilization. ... NoCs also decouple computation from communication, which is essential in managing the design of billion-transistor chips. NoCs achieve this decoupling because they are traditionally designed using protocol stacks, which provide well-defined interfaces separating communication service usage from service implementation.

EX1001 at 1:37–47. Moreover, using multi-hop interconnects “radically changes the communication when compared to direct interconnects, such as buses or switches.” EX1001 at 2:31–42 (“This is because of the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes. This is in contrast with the prevalent existing interconnects (i.e., buses) where modules are directly connected. The implications of this change reside in the arbitration (which must change from centralized to distributed), and in the communication properties (e.g., ordering, or flow control.)”).

57. The '052 Patent also emphasizes that “NoC’s premises are different from off-chip networks, and, therefore, most of the network design choices must be reevaluated” because “[o]n-chip networks have different properties (e.g., tighter link synchronization) and constraints (e.g., higher memory cost) leading to different design choices, which ultimately affect the network services.” EX1001 at 1:64–2:2. Another distinction between an on-chip network compared to off-chip networks is that “[a]n off-chip network interface usually contains a dedicated processor to implement the protocol stack up to network layer or even higher, to relieve the host processor from the communication processing;” however, “[i]ncluding a dedicated processor in a network interface is not feasible on chip, as

the size of the network interface will become comparable to or larger than the IP to be connected to the network.” EX1001 at 2:14–22.

58. Given the technical challenges, I do not agree with Dr. Hassoun’s simplistic assertion that the prior art technologies (e.g., bus-based interconnects and traditional computer networks) could be easily combined without undue experimentation by a person of ordinary skill in the art. A POSITA would have been dissuaded from attempting to modify or combine different prior art to arrive at the respective claimed inventions. My observations and opinions in this respect apply to all alleged modifications and combinations proposed by Dr. Hassoun.

59. I note that all of the elected references suffer from the issues stated immediately above. There is no teaching, and Dr. Hassoun never cites any teachings, for how the prior art systems could be modified or combined to arrive at the claimed multi-hop interconnect that provides the characteristics described above, for example, quality of service guarantees. In my opinion, arriving at this limitation would require extensive re-design, which is neither suggested nor alluded to, and would raise the difficulties and challenges discussed herein.

### **C. Overview of the ’052 Patent**

60. The ’052 Patent relates to “an integrated circuit having a plurality of processing modules and an interconnect means for coupling said plurality of processing modules and a method for communication service mapping in such an

integrated circuit.” EX1001 at 1:6–10. For example, Figure 1 of the ’052 Patents shows an embodiment comprising two master modules, a slave module, and two network interfaces where “[e]ach module M, S is connected to a network N via its associated network interface NI, respectively, i.e. the network interfaces NI are used as interfaces between the master and slave modules M, S and the network N.” *Id.* at 5:6–16. “Between network interfaces and its associated master M and slave S an adapter unit A is arranged, respectively, where the adapter units A may also be arranged in the network interface.” *Id.*

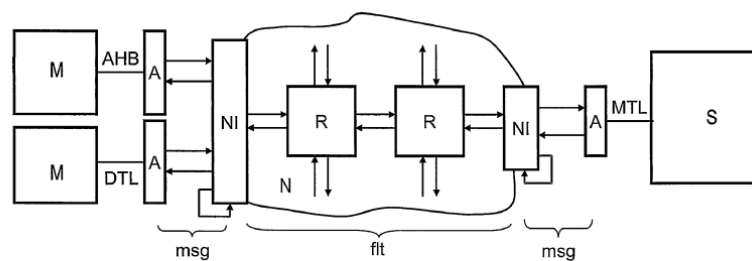


FIG.1

61. The ’052 Patent further discloses that the “master module M requests a communication service, i.e. a request is issued to the slave module S.” *Id.* at 5:53–54. “The slave S receives the request and performs the respective processings based on the received command and returns a response.” *Id.* at 5:55–58. “The adapter units A serve to connect the IP and their communication protocol to the network interface which in turn serve to connect to the network N.” *Id.* at 5:58–61. Accordingly, “the adapter units A translate the requested communication service into messages msg,

which are processed by the network interface NI and are translated into flits fit to be transmitted over the network N, in particular the adaptor unit A maps the identification means of these protocols to connections.” *Id.* 5:61–66. “The identification means in the existing protocols are: communication threads and addresses, i.e. the threads or addresses are mapped to connections through the interconnect based on specific connection properties.” *Id.* at 5:66–6:3.

62. “A communication thread can be directly mapped on a connection, i.e. one thread to one connection,” “[w]here communication threads are used to identify traffic classes of a communication based on specific communication parameters, such a thread and the associated traffic class can be mapped to a connection based on specific corresponding connection properties.” *Id.* at 7:41–48.

63. Thus, the ’052 Patent discloses an integrated circuit including an on-chip network where the interfaces between modules and the network are configured to map between a requested communication service and specific connection properties.

### **1. Challenged Claims of the ’052 Patent**

64. I understand that Petitioners challenge the following claims of the ’052 Patent in this IPR: Claims 1–7.

65. The exact language of independent claim 1 is reproduced below:

1. [preamble] Integrated circuit, comprising:

[a] a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification,

[b] an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a connection based communication having a set of connection properties,

[c] at least one network interface (NI) associated to said at least one first of said processing modules for controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N), and

[d] a mapping means (A) for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S).

66. The exact language of independent claim 6 is reproduced below:

6. [preamble] Method of communication service mapping in an integrated circuit, having a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S), comprising the steps of:

[a] coupling said plurality of processing modules (M, S) by an interconnect means (N) and

[b] enabling a connection based communication having a set of connection properties,

[c] controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N) by at least one network interface (NI) associated to said at least one first of said processing modules,

[d] mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.

67. The exact language of independent claim 7 is reproduced below:

7. [preamble] Data processing system, comprising

[a] a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S),

[b] an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a connection based communication having a set of connection properties,

[c] at least one network interface (NI) associated to said at least one first of said processing modules for controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N), and

[d] a mapping means (A) for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.

## **2. The 052 Patent's File History**

68. The '052 Patent issued from U.S. Application No. 10/598,795 (“the '795 application”). During prosecution of the '795 application, the Examiner rejected the pending claims under 35 U.S.C. § 102(b) as being anticipated by the *Æthereal* NoC (“*Æthereal*”) as disclosed in “Concepts and Implementation of the Philips Network-on-Chip” by Dielissen et al. (“Dielissen”) and “Communication Services for Networks on Chip” by Radulescu et al. (“Radulescu”). *See* EX1002, Office Action dated September 25, 2008. In response, the Applicant did not amend the claims, instead, argued that both Dielissen and Radulescu “fail to disclose or suggest ‘a mapping mean (A) for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification,’ as recited in claim 1.” *See Id.*, Applicant’s Amendment and Response Dated January 6, 2009.

69. Thereafter, the Examiner issued a Final Rejection that maintained the rejection of the pending claims under 35 U.S.C. § 102(b) as being anticipated by the *Æthereal* NoC as disclosed in Dielissen and Radulescu. *See Id.*, Office Action

dated March 9, 2009. In response, Applicant amended the pending claims to recite “wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S).” *See Id.*, Applicant’s Amendment and Response Dated May 11, 2009. Applicant further stated:

Applicants respectfully submit that Radilescu [sic] at pages 287-288 is not describing a mapping means but it instead describing a fixed hardware configuration between IPs and network NI ports (NIP) that is required to be set up a-priori to receiving service requests during an operational stage. In fact, Radilescu [sic] teaches at page 288, second full paragraph, that AThereal connections must be created with the desired properties before being used (i.e. prior to mapping communication service requests).

Applicants respectfully submit that, in contrast to Radilescu [sic], the invention is based on the idea of offering differentiated services for protocols such as DTL, MTL, AXI, and OCP, by mapping the identification means of these protocols to connections. The identification means in the existing protocols are: communication threads and addresses, i.e. the threads or addresses are mapped to connections through the interconnect based on specific connection properties. Applicant submits that this is different from Radilscu [sic] which describes end-to-end flow control and guaranteed throughputs, but is silent with respect to offering differentiated services for protocols such as DTL, MTL, AXI, and OCP, by mapping the identification means of these protocols to connections.

*Id.*

70. Following the applicant’s amendment and response of May 11, 2009, the Examiner granted the ’795 application. *See Id.*, Notification of Allowance Dated May 14, 2009.

71. To the extent the file history is specifically relevant to my opinions, I will note it in the paragraphs below.

#### **D. Claim Constructions**

72. I understand that the following terms of ’052 Patent have proposed constructions by either the Petitioners or the Patent Owner, or have been construed, either by agreement or by the Court:

#### **The Petition’s Proposed Constructions**

##### **1. “interconnect means” (claims 1, and 6-7)**

73. I understand that Petitioners and NST have a dispute over the construction of “interconnect means”:

| <b>Term</b>          | <b>Petitioners’ Proposed IPR Construction</b>                                                                                                                                                                                            | <b>NST’s Proposed IPR Construction</b>                                                                                                                                                                                     |
|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| “interconnect means” | Subject to Section 112 ¶ 6<br><br>Function (claims 1, 6, and 7): coupling said plurality of processing modules (M, S).<br><br>Function (claims 1 and 7): enabling a connection based communication having a set of connection properties | “multi-hop interconnection between modules separated by one or more network nodes”<br><br>(The same construction was adopted by the district court in the TI case. <i>See</i> EX2022, 60).<br><br>If subject to § 112, ¶ 6 |

|  |                                                                   |                                                                                                                                                                                                                                  |
|--|-------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | Structure: any of a bus, switch, point-to-point wire, or network. | Function (claims 1, 6, and 7): coupling said plurality of processing modules (M, S).<br><br>Function (claims 1 and 7): enabling a connection based communication having a set of connection properties<br><br>Structure: circuit |
|--|-------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

Pet., 10.

74. I understand that Samsung did not propose this construction in the Samsung district court litigation:

| <b>Term</b>          | <b>Samsung District Court Construction</b> | <b>NST District Court Construction</b>                                                                                                                                                     |
|----------------------|--------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| “interconnect means” | Plain and ordinary meaning                 | “multi-hop interconnection between modules separated by one or more network nodes”<br><br>(The same construction was adopted by the district court in the TI case. <i>See</i> EX2022, 60). |

EX2033. I understand that Samsung has now adopted Patent Owner’s proposed construction for “interconnect means” as a “multi-hop interconnect between modules separated by one or more network nodes.” EX2035, 2, n. 2.

75. I understand that, in the Qualcomm litigation, Qualcomm argued for the same construction Petitioners argue here:

| Term                 | Qualcomm District Court Construction                                                                                                                                     | NST District Court Construction                                                                                                                                                                                                                                                                                               |
|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| “interconnect means” | <p>Subject to Section 112 ¶ 6</p> <p>Function: coupling said plurality of processing modules (M, S).</p> <p>Structure: bus, switch, point-to-point wire, or network.</p> | <p>“multi-hop interconnection between modules separated by one or more network nodes”</p> <p>(The same construction was adopted by the district court in the TI case. <i>See</i> EX2022, 60).</p> <p>If subject to 112 ¶6</p> <p>Function: coupling said plurality of processing modules (M, S)</p> <p>Structure: circuit</p> |

EX2040, 22.

76. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

77. At the time of the invention, on-chip networks were just emerging as an intersection of computer networks and microchip design. *See, e.g.*, EX2005, 1 (“We propose replacing design-specific global on-chip wiring with a general-purpose on-chip interconnection network.”).

78. Also, at the time of invention, computer networks and other off-chip networks were well-known and understood. For example, as explained in the specification of the ’052 Patent, “issues like out-of order transactions, higher

latencies, and end-to-end flow control . . . have been already the subject of research in the field of local and wide area networks (computer networks) and as an interconnect for parallel machine interconnect networks.” EX1001, 1:56–62. Engineers and/or researchers with backgrounds in computer networks tended to approach and describe on-chip networks from the perspective of computer networks, e.g., LANs and WANs. Thus, “interconnect means” may have been an apt term for some of these engineers and/or researchers to describe an on-chip network, since they were already using the term “network” for off-chip networks. On the other hand, some engineers and/or researchers may have focused too heavily on the “interconnect” portion of “interconnect means,” and inadvertently narrowed its scope to direct interconnects, such as shared buses.

79. Also, at the time of invention, direct interconnections for enabling communication between modules (e.g., IP blocks or components) within a very large-scale integrated (VLSI) system, such as shared buses and switches, were well known and understood. EX1001, 2:32-39. Engineers and/or researchers with backgrounds in microchip design tended to approach and describe on-chip networks from the perspective of shared buses and switches, e.g., clusters of wires or interconnects. Thus, “interconnect means” may have been an apt term for these engineers and/or researchers to describe an on-chip network, since they were already using the term “interconnects” for on-chip wires. On the other hand, some

engineers and/or researchers may have focused too heavily on the “interconnect” portion of “interconnect means,” and inadvertently narrowed its scope to direct interconnects, such as shared buses.

80. As a result of the different approaches and varying ways to describe an on-chip network in the fields of computer networks and microchip design, at the time of invention, “interconnect means,” as it is used in the Asserted Patents, lacked a strictly consistent plain and ordinary meaning. However, based on the intrinsic evidence, the interconnect means does not describe only a direct interconnection, e.g., a shared bus; rather, it describes an indirect interconnection, e.g., a network, as explained below.

81. First, in the ’052 Patent, the label “N” indicates a network portion in several figures, and the label “N” is associated with both the terms “network N” and “interface means (N)” in the specification and claims (recall claim 6 recites steps that describe “an interconnect means (N).”).

82. In the ’052 Patent, “FIG. 1 shows a network on chip according to a first embodiment.” EX1001, 5:6–7; *see also* 4:30–31. FIG. 1 is reproduced below, with annotation in yellow.

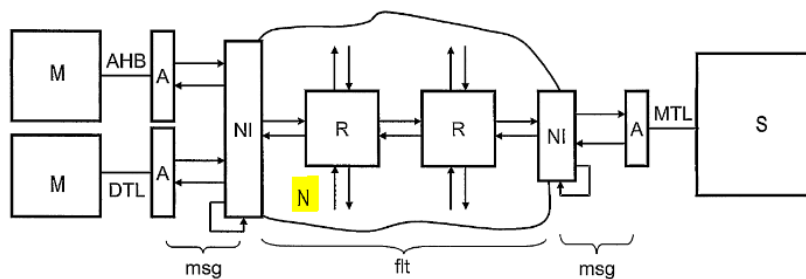


FIG.1

83. According to the description of FIG 1, the portion labeled “N” between the network interfaces corresponds to a network having a plurality of routers for transporting data packets:

The network N may be comprised of a plurality of interconnected network routers R. The routers R can be randomly connected amongst themselves (multiple links between routers are also possible) and to the network interfaces (i.e., there are no topology constraints). The routers R transport packets of data from one network interface NI to another. Such a packet consists of one or more flits, where a flit is the minimal transmission unit.

EX1001, 5:24–31 (emphasis added).

84. In the '052 Patent, “FIG. 4 shows a basic representation of a block diagram of a network on chip according to a further embodiment.” EX1001, 4:37–39; *see also* 8:7–8. FIG. 4 is reproduced below, with annotation in yellow.

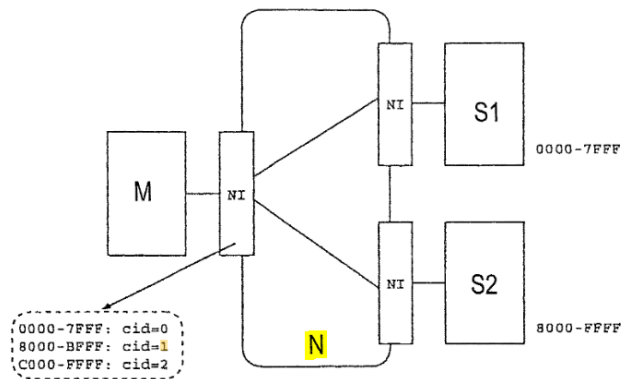


FIG.4

85. According to the description of FIG. 4, “[t]he network on chip comprises a master M and two slaves S1, S2 each being connected to a network via a network interface NI, respectively.” EX1001, 8:9–12. Although FIG. 4 does not illustrate routers in the network N, this can be reasonably expected at least because “FIG. 4 shows a **basic block diagram of a network on chip for illustrating the operation of the mapping of IP block communication via address ranges to connections.**” EX1001, 8:7–9 (emphasis added). In other words, FIG. 4 is provided for illustrating the mapping operation of the network interfaces, not for illustrating a topology of the network. Indeed, the description following FIG. 1, explicitly states “there are no topology constraints.” EX1001, 5:27–28.

86. According to FIGS. 1 and 4 and the descriptions cited above, the network N interconnects modules (M to S in FIG. 1 and M to S1, S2 in FIG. 4). The specification ascribes the same function to the interconnect means, which

several examples cited below. Thus, at least for this reason, a POSITA would understand that the network N and the interconnect means (N) describe the same thing.

Furthermore, an interconnect means (N) is provided for coupling said plurality of processing modules (M, S) and for enabling a connection based communication having a set of connection properties.

EX1001, Abstract.

The invention relates to an integrated circuit having a plurality of processing modules and an interconnect means for coupling said plurality of processing modules.

EX1001, 1:7–8.

At least one network interface is associated to said at least one first of said processing modules for controlling the communication between said at least one first of said plurality of processing modules and said interconnect means.

EX1001, 3:18–22.

Said plurality of processing modules are coupled by an interconnect means and enabling a connection based communication having a set of connection properties.

EX1001, 3:51–54.

Furthermore, an interconnect means is provided for coupling said plurality of processing modules and for enabling a connection based communication having a set of connection properties.

EX1001, 4:1–4.

87. There is additional evidence in the '052 Patent indicating that the network N and the interconnect means (N) describe the same thing. Specifically,

the “interconnect means (N) is provided for coupling said plurality of processing modules (M, S) **and for enabling a connection based communication having a set of connection properties.**” EX1001, Abstract (emphasis added); *see also* 3:15–18; 3:51–54; 4:1–4. As explained in the ’052 Patent:

“At the transport layer of said network, the communication between the modules may be performed over connections. A connection is considered as a set of channels, each having a set of connection properties, between a first module and at least one second module. . . . The connection properties may include ordering (data transport in order), flow control (a remote buffer is reserved for a connection, and a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data), throughput (a lower bound on throughput is guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data), transmission termination, transaction completion, data correctness, priority, or data delivery.”

EX1001, 4:50–5:5.

“The connections may comprise the following services, or connection properties: 1) data integrity, 2) transaction ordering, 3) transaction completion, 4) connection flow control, and 5) connection throughput, latency, and jitter. A connection can request any combination of these properties (e. g. a throughput guarantee, flow control, but no transaction ordering).”

EX1001, 6:13–19.

88. A POSITA would understand that a connection-based communication, which may include the connection properties listed above, is a known attribute of networks, and a POSITA would further understand that a connection-based communication, which may include the connection properties listed above, is not

normally associated with direct interconnections, such as shared buses.

Consequently, because the interconnection means described in the '052 Patent enables a connection-based communication, a POSITA would understand the “interconnection means” to describe a network comprising indirect interconnections between modules, not a direct interconnection between modules. In other words, the POSITA would understand that the network N and the interconnect means (N) describe the same thing.

89. And as detailed earlier, the network N of FIG. 1 explicitly includes interconnected routers R for transporting data packets, consistent with “the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes.” EX1001, 2:33–36. Thus, a network N is a “multi-hop interconnection between modules separated by one or more network nodes.” Consequently, because “interconnect means” and “network” describe the same thing, then “interconnect means” is a “multi-hop interconnection between modules separated by one or more network nodes.”

90. Thus, it is my opinion that the correct understanding that a POSITA would have of “interconnect means,” as used in the Asserted Patents, is the meaning provided by NST of a “multi-hop interconnection between modules separated by one or more network nodes.”

## 2. “mapping means” (claims 1 and 7)

91. I understand that Petitioners and NST have a dispute over the construction of “mapping means”:

| Term                                                                                                                                                                                                                                                         | Petitioners’ Construction                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | NST’s Construction                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| “mapping means (A) for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification” | <p>Subject to Section 112, ¶ 6</p> <p><b>Function:</b> “mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.”</p> <p><b>Structure:</b> adapter unit/shell comprising a sequentializing unit and a desequentializing unit as disclosed in the ’052 Patent at 5:58–6:3, 6:30–7:14, Figs. 1, 2A and 2B.</p> | <p>“mapping means” means “circuit configured to map a requested communication service to a connection,” NST incorporates the agreed upon definition for the term “connection properties,” and the remaining language should be afforded their plain and ordinary meanings.</p> <p>NST disagrees that this term is governed by Section 112 ¶ 6. Nevertheless, if the Court holds that this term is so governed, NST proposes the following construction:</p> <p><b>Function:</b> “mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification”</p> <p><b>Structure:</b> “circuit”</p> |

Pet., 11-12.

92. In the Samsung litigation, Samsung also argued that the “mapping means” is otherwise, indefinite. In the Qualcomm litigation, Qualcomm did not propose a construction for the “mapping means.” See EX2033, Appendix 2; EX2040.

93. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

94. The ’052 Patent describes the mapping means as a circuit. For example, claim 1 recites an “[i]ntegrated circuit, comprising: ...a mapping means (A) . . .” EX1001, 9:25–41 (emphasis added). I understand that NST and Defendants have stipulated that “integrated circuit” means “interconnected circuitry on a chip.” In my opinion, this meaning is consistent with how a POSITA reading the Asserted Patents would understand this term, and it is consistent with authoritative extrinsic sources, for example, The New IEEE Standard Dictionary Of Electrical And Electronics Terms, (5th ed. 1993), which defines an “integrated circuit” as “[a] combination of interconnected circuit elements inseparably associated on or within a continuous substrate.” EX2014. Therefore, a mapping means comprised in an integrated circuit must be a circuit element of the integrated circuit. Because an integrated circuit is interconnected circuitry on a chip, a

POSITA would understand that the mapping means comprised in an integrated circuit discloses that the mapping means is interconnected circuitry of the integrated circuit, i.e., the mapping means is a circuit.

95. The mapping means must be a circuit because the network interface is a circuit (the network interface is comprised in the integrated circuit) and the network interface comprises the mapping means. Specifically, claim 1 recites an “[i]ntegrated circuit, comprising: ...at least one network interface (NI) . . .” EX1001, 9:25–36 (emphasis added); *see also* EX1001, 8:9–12 (“The network on chip comprises a master M and two slaves S1, S2 each being connected to a network via a network interface NI, respectively.”); EX1001, 2:18–21 (“Including a dedicated processor in a network interface is not feasible on chip, as the size of the network interface will become comparable to or larger than the IP to be connected to the network.”); EX1001, 5:6–8 (“FIG. 1 shows a network on chip according to a first embodiment. In particular, two master modules M and a slave module S each with an associated network interface NI are depicted.”). Because an integrated circuit is interconnected circuitry on a chip, a POSITA would understand that the network interface comprised in an integrated circuit discloses that the network interface is interconnected circuitry of the integrated circuit, i.e., the network interface is a circuit. Further, the specification of the ’052 Patent states “said at least one network interface comprises a mapping means,”(EX1001, 3:22–

23), and “said mapping means is arranged in said at least one network interface.”( EX1001, 3:30–31). Thus, a POSITA would understand that the mapping means comprised in the network interface discloses that the mapping means is circuitry of the network interface, i.e., the mapping means is a circuit.

96. The '052 Patent uses several terms to describe the mapping means, where each term is frequently suffixed by the letter “A”: “mapping means (A),” (EX1001, Abstract and Claims 1, 2, and 7); “adapter unit A” or “adapter units A,” (EX1001, 5:10, 5:12, 5:58, 5:61, 6:34, 6:37, 6:41; *see also* EX1001, 6:39–40 (“FIGS. 2A and 2B show a block diagram of the adapter units of FIG. 1 . . .”); EX1001, 6:56–66 (“In FIG. 3 a block diagram of a network interface NI . . . is shown [where] the network interface comprises . . . two adapter units AXI\_A, DTL\_A, . . .”); and “shell A” or “shells A,” EX1001, 6:46; *see also* EX1001, 6:41–42 (“These adapter units A may also be considered as shells to map the communication services . . .”); EX1001, 6:60–61 (“[T]he adapter units or the shells are implemented as part of the network interface NI . . .”); EX1001, 7:1–2 (“[T]he network interface shells or adapter units.”); EX1001, 7:6–7 (“[T]he network interface shells or adapter units . . . .”); EX1001, 7:40–41 (“[T]he adaptor units A, i.e. the shells . . . .”); EX1001, 8:55 (“[B]y means of the adaptor units/shells . . . .”). The specification of the '052 Patent describes the “adapter unit A,” i.e., the “mapping means (A),” as being *between* a network interface and its

associated master and slave (or arranged in the network interface, as described above). EX1001, 5:9–13 (“Between network interfaces and its associated master M and slave S an adapter unit A is arranged, respectively, wherein the adapter units A may also be arranged in the network interface.”); EX1001, 6:36–38 (“These adapter units A may also be arranged **between** the IP blocks and their associated network interfaces.”)(emphasis added)); *see also* FIG. 1 (blocks labeled “A”); FIGS. 2A-2B (blocks labeled “A”), and FIG. 3 (blocks labeled “DTL-A” and “AXI-A”). Placement between circuit elements of an integrated circuit indicates a physical placement of the “mapping means (A),” i.e., the “adapter unit A” or the “shell A,” within the integrated circuit. Further, the specification of the ’052 Patent explains that “[a]ll these shells can be plugged in or left out at instantiation time according to the needs to **optimize area cost.**” EX1001, 7:37–39 (emphasis added). Optimizing area of the shell, i.e., the mapping means, indicates physical structure of the mapping means within an integrated circuit. A POSITA would understand the above indications of placement and area to mean that the mapping means is a physical circuit that is comprised in the integrated circuit.

97. The specification of the ’052 Patent also states before the claims section that “[i]n the device claim enumerating several means, several of these **means can be embodied by one and the same item of hardware.**” EX1001, 9:15–17 (emphasis added). A POSITA understands the term “hardware” to mean

physical circuitry. For example, the Dictionary Of Computer And Internet Terms (7th ed. 2000) defines hardware as “the physical elements of a computer system; the computer equipment as opposed to the programs or information stored in the machine.” EX2015. This term is often used in contrast with the term “software,” which a POSITA understands as describing instructions for execution by computer hardware, e.g., by physical circuitry like a processor (sometimes called a central processing unit (CPU)). For example, the Dictionary Of Computer And Internet Terms (7<sup>th</sup> ed. 2000) defines software as “programs that tell a computer what to do. The term contrasts with *hardware*, which refers to the actual physical machines that make up a computer system.” EX2015 (emphasis in original). The figure below shows a simplified hierarchical view of the hardware-software interface, with hardware at the core and software on the periphery for execution by the core. David Patterson And John Hennessey, Computer Organization & Design § 1, P. 9 (2nd ed. 1998). EX2016.

98. A POSITA would understand that the “mapping means” is hardware, and not software or firmware, for two reasons. First, there is no mention of software or firmware anywhere in the ’052 Patent. Second, a POSITA would not recognize software or firmware operated by general purpose hardware “as a solution to the interconnect problem in highly-complex chips [at least because] NoCs help resolve the electrical problems in new deep-submicron technologies, as

they structure and manage global wires.” See EX1001, 1:35–39. Networks-on-chip (NoCs) comprise circuitry that is designed and built specifically to provide data communication within the chip. Indeed, the ’052 Patent dispels the notion of including a processor (which is a general-purpose hardware for executing software or firmware) in a network interface of an on-chip network, where the mapping means is comprised in the network interface. EX1001, 2:18–21. (“Including a dedicated processor in a network interface is **not feasible on chip**, as the size of the network interface will become comparable to or larger than the IP3to be connected to the network.”) (emphasis added).

99. The ’052 Patent describes the “mapping means” in several locations, where each description is consistent with NST’s construction as a “circuit configured to map a requested communication service to a connection.” EX1001, Abstract (“a mapping means (A) is provided for mapping the requested at least one communication service . . . to a connection,”); EX1001, 3:22–25 (“said at least one network interface comprises a mapping means for mapping the requested at least one communication service . . . to a connection,”); *see also* EX1001, 4:7–11.

100. Given the totality of evidence, it is my opinion that the correct understanding that a POSITA would have of “mapping means,” as used in the Asserted Patents, is the meaning provided by NST of “circuit configured to map a requested communication service to a connection.”

101. I understand the Court may determine this term should be construed under 35 U.S.C. § 112 ¶ 6, means-plus-function. In this event, it is my opinion that NST’s proposed structure of a “circuit” is correct and Petitioners’ proposed structure of “adapter unit/shell comprising a sequentializing unit and a desequentializing unit as disclosed in the ’052 patent at 5:58-6:3, 6:30-7:14, FIGS. 1, 2A, and 2B,” or that this term is otherwise indefinite, is not correct.

102. The function proposed for this term by both NST and Petitioners with respect to claims 1, 2, and 7 appear to be identical: “mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.”

103. Independent claims 1 and 7 of the ’052 Patent recite an integrated circuit and a data processing system, respectively, that describe “a mapping means (A) for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification, . . .” EX1001, 9:25–45, 10:54–58. Descriptions in the specification mirror the language in these claims, as reproduced below.

[A] mapping means (A) is provided for mapping the requested at least one communication service based on said specific communication

properties to a connection based on a set of connection properties according to said at least one communication service identification.

EX1001, Abstract.

[S]aid at least one network interface comprises a mapping means for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.

EX1001, 3:22–27; see also EX1001, 4:7–10. It is therefore my opinion that the correct function of the “mapping means” is “mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.”

104. The '052 Patent uses several terms to describe the mapping means, where each term is frequently suffixed by the letter “A”: “mapping means (A),” (EX1001, Abstract and Claims 1, 2, and 7); “adapter unit A” or “adapter units A,” (EX1001, 5:10, 5:12, 5:58, 5:61, 6:34, 6:37, 6:41; *see also* EX1001, 6:39–40 (“FIGS. 2A and 2B show a block diagram of the adapter units of FIG. 1 . . .”)); EX1001, 6:56–66 (“In FIG. 3 a block diagram of a network interface NI . . . is shown [where] the network interface comprises . . . two adapter units AXI\_A, DTL\_A, . . .”); and “shell A” or “shells A,” EX1001, 6:46; *see also* EX1001, 6:41–42 (“These adapter units A may also be considered as shells to map the

communication services . . .”); EX1001, 6:60–61 (“[T]he adapter units or the shells are implemented as part of the network interface NI . . .”); EX1001, 7:1–2 (“[T]he network interface shells or adapter units.”); EX1001, 7:6–7 (“[T]he network interface shells or adapter units implement. . . .”); EX1001, 7:40–41 (“[T]he adaptor units A, i.e. the shells . . . .”); EX1001, 8:55 (“[B]y means of the adaptor units/shells . . . .”). The specification of the ’052 Patent explains that “[t]he shells A [i.e., the “mapping means (A),] comprise a sequentializing unit seq and a desequentializing unit deseq, respectively.” EX1001, 6:46–48. It is my opinion that reducing the structure of the mapping means to only the sequentializing unit and the desequentializing unit, as Defendants propose under 35 U.S.C. § 112 ¶ 6, is overly narrow for the mapping means, as explained below.

105. First, mapping is well-understood by a POSITA, and a POSITA would readily understand and recognize a circuit for “mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.” For example, mapping is routinely performed using mapping logic, i.e., digital logic circuitry, or gates, that generate a desired mapping result according to a Boolean function of the input signals, and/or using look-up tables, i.e., memory circuitry, that retrieves a desired mapping result according to an index indicated by the input signals, where structures of both

digital logic circuitry and look-up tables for mapping are known to a POSITA. Second, while the mapping performed by the communication service mapping may involve sequentializing of commands, flags, addresses, and write data into a message, and desequentializing of a message into read data and write responses, (EX1001, 6:48–53), such sequentializing and desequentializing is a subset of “mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification” that is described in the ’052 Patent.

106. Thus, it is my opinion that if the Court determines this term should be construed under 35 U.S.C. § 112 ¶ 6, then the correct understanding that a POSITA would have of this term as used in the Asserted Patents is the meaning provided by NST.

### **Agreed District Court Constructions**

#### **3. The preamble**

107. In the Qualcomm Litigation and the Samsung Litigation, the parties agreed that the preamble of claim 6 should be construed as limiting. EX2033, Appendix 1; EX2040, 5-6. The same construction was adopted by the district court in the TI case. See EX2022, 58.

#### **4. “connection properties” (claims 1, 3-7)**

108. In the Qualcomm Litigation and Samsung Litigation, the parties agreed that “connection properties” should be construed as “properties of a connection, including ordering (data transport in order), flow control (a remote buffer is reserved for a connection, and a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data), throughput (a lower bound on throughput is guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data), transmission termination, transaction completion, data correctness, priority, or data delivery.” EX2033, Appendix 1; EX2040, 6. The same construction was adopted by the district court in the TI case. See EX2022, 57.

#### **5. “integrated circuit” (claims 1-6)**

109. In the Qualcomm Litigation and the Samsung Litigation, the parties agreed that the term “integrated circuit” should be construed as “interconnected circuitry on a chip.” EX2033, Appendix 1; EX2040, 6. The district court in the TI case construed “integrated circuit” as “a combination of interconnected circuit elements inseparably associated on or within a continuous substrate.” EX2022, 59.

### **Disputed District Court Constructions**

#### **6. “connection” (claims 1, and 3-7)**

110. In the Qualcomm Litigation, the parties proposed the following constructions for the term “connection.” EX2040, 6.

| Term         | Qualcomm's Construction                                                                                                                                                     | Patent Owner's Construction          |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|
| "connection" | "one or more channels, each having a set of connection properties, between a first module and at least one second module, that are created before use and closed after use" | "one or more communication channels" |

111. In my opinion, NST's proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

112. The term "connection" is used in asserted claims of five of the six Asserted Patents ('818 Patent, '449 Patent, '052 Patent, '9893 Patent, and '800 Patent). Each of these five patents provides a characterization of "connection," reproduced below, which is consistent between all five patents and with NST's construction of the term. Included below each characterization is an excerpt of how the term "connection" is used in the '052 Patent, which is consistent with the use of the term in the specification and with NST's proposed construction of the term.

- **Specification:** "A connection is considered as a set of channels, each having a set of connection properties, between a first module and at least one second module." EX1001, 4:53–55.
- **Claims:** "Method . . . wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) . . . [the method] comprising the steps of: . . .

enabling a connection based communication having a set of connection properties, . . . mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties . . .” EX1001, 10:7–30 (claim 6).

113. What is not provided is support for the additional functional steps provided in Petitioners’ proposed construction, specifically, that connections “are created before use and closed after use.”

The request for the connection are either accepted or rejected. Connection acceptance may lead to resource reservations in the network, e.g. buffers or a link bandwidth percentage. After usage, the connection is closed and these resources are freed.

EX1001, 5:44–49. It is therefore my opinion that a POSITA, reading the asserted claims that use the term “connection” in the context of every respective Asserted Patent, would not understand the term “connection” to include the additional functional steps that Defendants proposed.

114. The ‘052 patent explains that certain aspects of the invention can be used in systems that **do not use connections**. ’052 patent at 8:47-51 (“[T]he above described mapping is relevant for communication protocols **which do not include the notion of connection**”). To be clear, “not connection based” is different than not using connections. Similarly, “notion of connection” is different than a connection and/or using a connection.

115. As explained earlier, the specification of the ‘052 Patent characterizes a connection as a set of communication channels. *See* EX1001, 4:53–55. NST’s proposed construction for “connection” is “one or more communication channels.” The Authoritative Dictionary of IEEE Standards Terms (7<sup>th</sup> ed. 2000) provides the following definitions for “communication,” “channel,” and “communication channel”:

Communication:

- (data transmission) (electric systems) (telecommunications) The transmission of information from one point to another by means of electromagnetic waves.
- The flow of information from one point, known as the source, to another, the receive.

Channel:

- (electric communication) A single path for transmitting electric signals, usually in distinction from other parallel paths. (B) (electric communication) A band of frequencies. Note: The word “path” is to be interpreted in a broad sense to include separation by frequency division or time division. The term “channel” may signify either a one-way path, providing transmission in one direction only, or a two-way path, providing transmission in two directions.

(EEC/PE) [119], 599-1985. The Authoritative Dictionary of IEEE Standards Terms (7<sup>th</sup> ed. 2000)

- (10) A logically independent data path between two Functions. Multiple channels can be used to reach different Functions or to represent independent instances of inter-unit communication. (C/MM) 1212.1-1993
- (15) A single flow path for digital data or an analog signal, usually in distinction from other parallel paths. An IEEE 1451.2 channel provides a path for a single commodity or logical state, either real or virtual, using a single data model and a single set of physical units. (IM/ST) 1451.2-1997
- (17) A physical or logical communication link to a single transducer or to a group of transducers considered as a single transducer. (IM/ST) 1451.1-1999

Communication Channel:

- A facility that permits signaling between terminals.

EX2014, 16.

116. Other authoritative sources provide similar definitions. What is clear from these definitions is that a communication channel is a channel for the transmission of information (e.g., data), and the channel can include physical and virtual aspects. A POSITA understands that a physical aspect of a channel may include a physical medium, such as a wire. Further, a POSITA understands that a virtual aspect of a channel may include a virtual-circuit configuration of a

connection-oriented service. *See, e.g.*, EX2014, 10 (“IEEE 100 Authoritative Dictionary of IEEE Standard Terms Seventh Edition . . . includes the following definition[] for “connection-oriented service” . . . . Connection-Oriented Service: A kind of delivery service where different **virtual circuit configurations are used to transmit messages.**” (emphasis added)). Note that “[i]n the virtual circuit approach, a preplanned route is established before any packets are sent.” EX2010, 11. Thus, NST’s proposed construction of “connection” as “one or more communication channels” is consistent with all asserted claims and all respective specifications including references to “connection-oriented” or “connection based” in the specifications, without requiring inclusion of additional functional steps proposed by Defendants.

117. Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

118. For all other claim terms in the challenged claims of the ’052 Patent that are not identified above, I have applied the plain and ordinary that a POSITA would understand for such terms and/or constructions at the time of the invention.

## VI. ANALYSIS OF THE '052 PATENT

### A. Ground 1: Purported Anticipation by Radulescu2004 (Claims 1-2 and 5-7)

119. In Ground 1, Dr. Hassoun opines that claims 1–2 and 5–7 are anticipated by EX1005 (“Radulescu2004”). *See* EX1003, ¶¶ 120–153.

#### 1. Independent Claim 6

120. Claim 6 of the '052 Patent recites a method of communication service mapping in an integrated circuit where a first module requests a communication service to a second module based on a communication service identification, where a communication service identification includes a communication thread or an address range identifying a second processing module of a memory region therein. The specification explains that “communication threads are used to identify traffic classes of a communication,” such as “a fast traffic class [and] a slow traffic class.” EX1001 at 7:44–54. Claim 6 is reproduced below in relevant part:

Method of **communication service mapping** in an integrated circuit, having a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, . . .

**mapping the requested at least one communication service** based on said specific communication properties **to a connection** based on a set of connection properties according to said at least one communication service identification.

EX1001 at 10:7–32 (emphasis added).

**a. Radulescu2004 Does Not Anticipate “communication service mapping” or “mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.”**

121. Radulescu2004 discloses a network interface for an on-chip network it refers to as the Æthereal NoC, where the network interface provides services via connections. EX1005 at Abstract; *see also* EX1005 at 2 (“The Æthereal NoC offers its services on connections.”). These connections describe and identify communications with different properties.

Connections are composed of unidirectional point-to-point channels (between a single master and a single slave). To each channel, properties are attached, such as guaranteed message delivery or not, in order or un-ordered message delivery, and with or without timing guarantees. As a result, different properties can be attached to the request and response parts of a connection, or for different slaves within the same connection.

EX1005 at 2.

122. Radulescu2004 explains that **“[b]efore the Æthereal NoC can be used by an application, it must be configured. NoC (re)configuration means opening and closing connections in the system.** Connections are set up depending on the application or the mode the system is running. Therefore, we must be able to open and close connections while the system is running.”

Radulescu2004 at 2 (emphasis added). Further, “[c]onnections can be opened and

closed at any time. Opening and closing of connections takes time, and **is intended to be performed at a granularity larger than individual transactions.**” EX1005 at 2 (emphasis added). Transaction comprises request messages sent from a master module to a slave module (e.g., read or write commands) and optional response messages sent from the slave to the master (e.g., data). EX1005 at 1 (“Communication is performed using a transaction-based protocol, where master IP modules issue request messages (e.g., read and write commands at an address, possibly carrying data) that are executed by the addressed slave modules, which may respond with a response message (i.e., status of the command execution, and possibly data).”).

123. Accordingly, Radulescu2004 does not disclose a communication service mapping as recited in claim 6 of the ’052 Patent, but discloses a fixed hardware configuration between modules and network interfaces that is required to be set up prior to receiving service requests during an operational stage, i.e., prior to mapping communication service requests. See EX1005 at 1 (“Before the *Æthereal* NoC can be used by an application, it must be configured. NoC (re)configuration means opening and closing connections in the system.”).

124. During prosecution of the ’052 Patent, the Examiner rejected claims 1–7 under 35 U.S.C. § 102(b) as being anticipated by anticipated by the *Æthereal* NoC as disclosed in “Concepts and Implementation of the Philips Network-on-

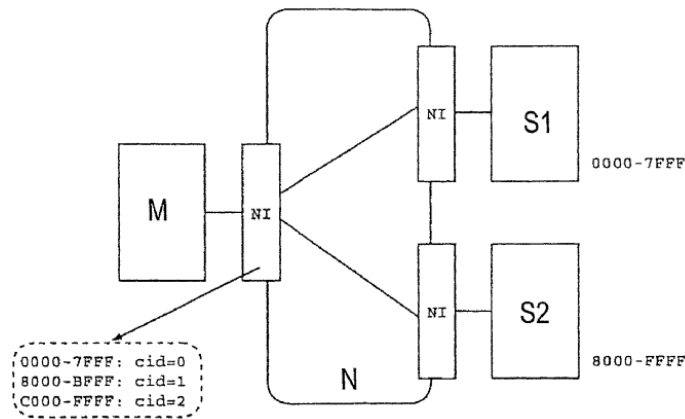
Chip” by Dielissen et al. and “Communication Services for Networks on Chip” by Radulescu et al. EX2018, 82. Like Radulescu2004, these references disclose a fixed hardware configuration between modules and network interfaces that is required to be set up prior to receiving service requests during an operational stage, i.e., prior to mapping communication service requests. See EX2018 at 38-42. For the same reasons provided by the Applicant that overcame these rejections, Radulescu2004 does not anticipate claim 6 of the ’052 Patent.

125. Specifically, in contrast to Radulescu2004, the claimed invention of the ’052 Patent is based on the idea of offering differentiated services for protocols such as DTL, MTL, AXI, and OCP, by mapping the identification means of these protocols to connections. The identification means in the existing protocols are: communication threads and addresses, i.e., the threads or addresses are mapped to connections through the interconnect based on specific connection properties. This is different from Radulescu2004, which describes end-to-end flow control and guaranteed throughputs, but is silent with respect to offering differentiated services for protocols such as DTL, MTL, AXI, and OCP, by mapping the identification means of these protocols to connections.

126. Radulescu2004 discloses the creation of desired properties *prior to their use*, which is different from the communication service mapping recited in claim 6 as explained above. Accordingly, there is no teaching or suggestion in

Radulescu2004 of communication service mapping comprising mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification, as recited in claim 6.

127. The specification and figures of the '052 Patent further highlight the distinction between the exclusive creation of desired properties *prior to their use*, as taught in Radulescu2004, and the claimed invention. FIG. 4 of the '052 Patent (reproduced below) is a block diagram for specifically illustrating the operation of mapping (i.e., communication service mapping) of IP block communication via address ranges to connections. As described below, the network interface, NI, associated to the master M maps the communication to the first slave to an address range 0000–7FFF to a connection id cid=0 and performs a similar operation for mapping the communication to the second slave.



EX1001, FIG. 4

The portion of the specification describing FIG. 4 is provided below.

FIG. 4 shows a basic block diagram of a network on chip for illustrating the operation of the mapping of IP block communication via address ranges to connections. The network on chip comprises a master M and two slaves S1, S2 each being connected to a network via a network interface NI, respectively. The two slaves S1, S2 are implemented as memories, wherein the first slave S1 comprises the address range 0000-7FFF and the second slave S2 comprises the address range 8000-FFFF. **Accordingly, the network interface NI associated to the master M may map the communication to the first slave S1, i.e. to the address range 0000-7FFF, to a connection with the connection id cid=0 and the communication to the second slave S2, i.e. to the address range 8000-FFFF, to a connection with the connection id cid=1.**

Hence, protocols where there are no communication threads (e.g., DTL, MTL), address ranges can be mapped to specific connections. An address range can identify one or more slave modules, or a memory region within a slave module, e.g. a buffer used in some particular communication.

EX1001, 8:7–26 (emphasis added).

128. In contrast, Radulescu2004 describes a network interface (NI) for providing conversion of the packet-based communication of the network to the higher-level protocol that the IP modules use. *See* EX1005, 1 (“Our NI provides services at the transport layer in the ISO-OSI reference model [22], because this is the first layer where offered services are independent of the network implementation. . . . We provide transport-layer services by defining connections.” (brackets in original)); *see also* EX1005, 2 (“Packetization is performed by the NI, and is thus transparent to the IP modules.”). Specifically, Radulescu2004 explains that the network interface is comprised of two parts: (a) the NI kernel, which provides the basic functionality, including arbitration between connections, packetizing of messages and schedules them to the routers, ordering, end-to-end flow control, and a link protocol with the router; and (b) the NI shells, which implement additional functionality, such as multicast and narrowcast connections, and adaptors to existing protocols, such as AXI or DTL.

The network interface (NI) is the component that provides the conversion of the packet-based communication of the NoC to the higher-level protocol that IP modules use. We split the design of the network interface in two parts (see Figure 1): (a) the NI kernel, which implements the channels, packetizes messages and schedules them to the routers, implements the end-to-end flow control, and the clock domain crossing, and (b) the NI shells, which implement the connections (e.g., narrowcast, multicast), transaction ordering for connections, and other higher-level issues specific to the protocol offered to the IP.

EX1005, 3.

For more complex types of connections, such as narrowcast or multicast, and to provide conversions to other protocols, we add shells around the NI kernel. As an example, in Figure 1, we show a NI with two DTL and two AXI ports. All ports provide point-to-point connections. In addition to this, the two DTL ports provide narrowcast connections, and one DTL and one AXI port provide multicast connections. Note that these shells add specific functionality, and can be plugged in or left out at design time according to the requirements.

EX1005, 4. FIG. 1 of Radulescu2004 is reproduced below, showing the network interface kernels and shells.

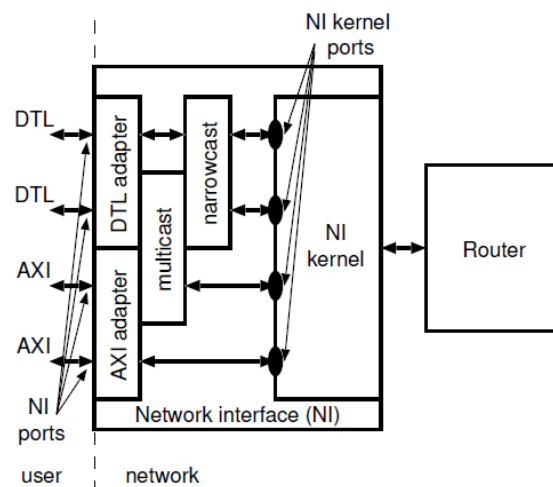


Figure 1. NI kernel and shells

EX1005, FIG. 1

129. The network interfaces (NI) in Radulescu2004 communicate with the NI shells via ports, (e.g., DTL ports and AXI ports). EX1005, 3 (“The NI kernel communicates with the NI shells via ports.”); *see also* Radulescu2004, FIG. 1 (showing two DTL ports and two AXI ports). Radulescu2004 explains that “[a] port can have multiple connections to allow differentiated traffic classes [e.g., best

effort or guaranteed throughput], in which case there are also connid signals to select on which connection a message is supplied or consumed.” EX1005, 3; *see also id.*, Abstract (“Our network interface . . . provides both guaranteed and best-effort services via connections”). Radulescu2004 further shows master and slave shells in FIGS. 5 and 6, respectively (reproduced below). “In Figures 5 and 6, we show a master and slave shells that implement a simplified version of a protocol such as AXI. The basic functionality of such a shell is to sequentialize commands and their flags, addresses, and write data in request messages, and to desequentialize messages into read data, and write responses to sequentialize commands and their flags, addresses, and write data in request messages, and to desequentialize messages into read data and write responses.” EX1005, 5. Examples of message structures after sequentialization are shown in FIG. 7 of Radulescu2004 (reproduced below).

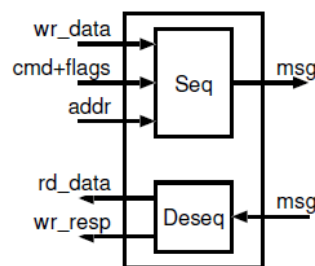


Figure 5. Master shell

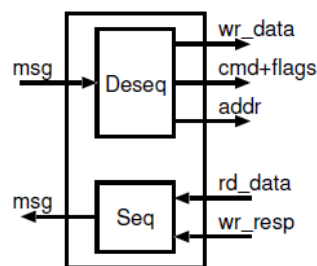


Figure 6. Slave shell

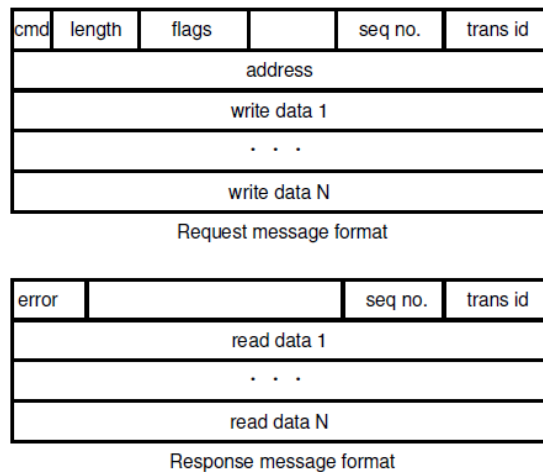


**Figure 7. Message format examples**

EX1005, FIGs. 5, 6, 7

130. In summary, Radulescu2004 discloses the creation of desired properties *prior to their use*, which is different from the communication service mapping recited in claim 6. For at least these reasons, Radulescu2004 does not anticipate the “communication service mapping” or the “mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification” as recited by claim 6 of the ’052 Patent.

**b. Radulescu2004 Does Not Anticipate “at least one communication service . . . based on specific communication properties . . . wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S)”**

131. Section X.A.1.b of Dr. Hassoun’s Declaration addresses only the “at least one address range” option of the communication service identification recited in claim 6 of the ’052 Patent. *See* EX1003, ¶¶124-127. In my opinion, Radulescu2004 does not disclose or suggest such an address range.

132. First, a POSITA understands that a range has a lower bound and an upper bound. Dr. Hassoun’s Declaration provides no evidence that Radulescu2004 discloses any such address range. Instead, Dr. Hassoun’s Declaration conflates two separate concepts in Radulescu2004: (1) that a request for a transaction can include an address (EX1005, 1–4, FIG. 5); and (2) that a slave can be assigned an address range (*id.*, 4). These concepts, even taken together, do not disclose or suggest “communication service identification compris[ing] . . . at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S).”

133. Second, as I explained in Sec. VI.A.1.a above, Radulescu2004 does not disclose a communication service mapping as recited in claim 6 of the ’052

Patent, but discloses a fixed hardware configuration between modules and network interfaces that is *required to be set up prior to receiving service requests* during an operational stage, i.e., prior to mapping communication service requests. See EX1005, 1 (“Before the *Æthereal* NoC can be used by an application, it must be configured. NoC (re)configuration means opening and closing connections in the system.”). Thus, in Radulescu2004, transaction requests—and any addresses associated therewith—come *after* the configuration between modules and network interfaces has already been set up. Consequently, the address associated with a transaction request in Radulescu2004 cannot be the “address range” of a communication service identification on which the communication service is based as recited in claim 6 of the ’052 Patent.

134. For at least the above reasons, Radulescu2004 does not anticipate “at least one communication service . . . based on specific communication properties . . . wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S)” as recited in claim 6 of the ’052 Patent.

## **2. Independent Claim 1**

135. I understand that Dr. Hassoun opines that Radulescu2004 discloses the limitations of independent claim 1 for the same reasons discussed for independent claim 6. See EX1003, ¶¶ 144–147. Thus, my opinions above regarding Radulescu2004 for claim 6 apply to claim 1 as well.

## **3. Independent Claim 7**

136. I understand that Dr. Hassoun opines that Radulescu2004 discloses the limitations of independent claim 7 for the same reasons discussed for independent claim 6. See EX1003, ¶¶ 152–153. Thus, my opinions above regarding Radulescu2004 for claim 6 apply to claim 1 as well.

## **4. Dependent Claims**

137. The dependent claims are not anticipated by Radulescu2004 for at least the same reasons that the independent claims from which they depend are not anticipated by Radulescu2004.

### **B. Ground 2: Purported Obviousness over Radulescu2004 in view of OCP (Claims 1-7)**

138. In Ground 2, Dr. Hassoun opines that claims 1–7 are rendered obvious by Radulescu2004 in view of EX1006 (“OCP”). See EX1003, ¶¶ 154-182.

## **1. Independent Claim 6**

139. As I explained in Sec. VI.A.1 above, Radulescu2004 does not disclose or suggest the “communication service mapping,” the “mapping the requested at

least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification,” and the “at least one communication service . . . based on specific communication properties . . . wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S)” as recited by claim 6 of the ’052 Patent. The combination of Radulescu2004 and OCP does not render these limitations obvious.

140. For example, OCP provides no disclosure that overcomes the fundamental difference I explained in Sec. VI.A.1.a above between Radulescu2004 and the claimed invention of the ’052 Patent.

141. First, to briefly repeat, Radulescu2004 does not disclose a communication service mapping as recited in claim 6 of the ’052 Patent because it discloses a fixed hardware configuration between modules and network interfaces that is *required to be set up prior to receiving service requests* during an operational stage, i.e., prior to mapping communication service requests.

142. Second, as I explained in Sec. VI.A.1.b above, in Radulescu2004, transaction requests—and any addresses associated therewith—come *after* the configuration between modules and network interfaces has already been set up.

143. Thus, even if the transaction requests in Radulescu2004 were modified to use either the alleged address range (e.g., “MAddr,” “MaddrSpace”) or the alleged communication thread (e.g., “MthreadID”) disclosed in OCP as suggested in Sec. X.B.1 of Dr. Hassoun’s Declaration (where claim 6 of the ’052 Patent recites “at least one communication service identification . . . compris[ing] at least one communication thread or at least one address range”), such combination of Radulescu and OCP does not overcome the above-described fundamental difference between Radulescu2004 and the claimed invention of the ’052 Patent. *See* EX1003, ¶¶ 162–173. Further, Dr. Hassoun has not shown how the combination of Radulescu and OCP could overcome the above-described fundamental difference.

144. Accordingly, I disagree that “a POSA would have been motivated to implement the OCP protocol, including its threads and address range teachings, in the system of Rădulescu2004, and would have had a reasonable expectation of success in doing so.” *See* EX1003, ¶ 173. Specifically, Dr. Hassoun has not shown why a POSITA would be motivated to modify Radulescu2004’s fixed hardware configuration between modules and network interfaces that is *required to be set up prior to receiving service requests* during an operational stage. Further, Dr. Hassoun has not shown that a POSITA would have reasonable expectation of success (or would have any success) in modifying Radulescu2004’s fixed

hardware configuration to implement the communication service mapping as recited in claim 6 of the '052 Patent.

145. For at least the reason described above, Radulescu2004 in view of OCP does not render obvious claim 6 of the '052 Patent at least because the combination does not disclose or suggest a “communication service mapping,” “mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification,” or “at least one communication service . . . based on specific communication properties . . . wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S).”

## **2. Independent Claim 1**

146. I understand that Dr. Hassoun opines that Radulescu2004 in view of OCP discloses the limitations of independent claim 1 for the same reasons discussed for independent claim 6. See EX1003, ¶178. Thus, my opinions above regarding Radulescu2004 for claim 6 apply to claim 1 as well.

### **3. Independent Claim 7**

147. I understand that Dr. Hassoun opines that Radulescu2004 in view of OCP discloses the limitations of independent claim 7 for the same reasons discussed for independent claim 6. See EX1003, ¶ 178. Thus, my opinions above regarding Radulescu2004 for claim 6 apply to claim 1 as well.

### **4. Dependent Claims**

148. The dependent claims are not rendered obvious by Radulescu2004 in view of OCP for at least the same reasons that the independent claims from which they depend are not rendered obvious by Radulescu2004 in view of OCP.

### **C. Ground 3: Purported Anticipation by Weber (Claims 1-7)**

149. In Ground 3, Dr. Hassoun opines that claims 1–7 are anticipated by EX1007 (“Weber”). See EX1003, ¶¶ 114–157.

#### **1. Independent Claim 6**

150. Claim 6 of the ’052 Patent recites a method of communication service mapping in an integrated circuit where a first module requests a communication service to a second module based on a communication service identification, where a communication service identification includes a communication thread or an address range identifying a second processing module of a memory region therein. The specification explains that “communication threads are used to identify traffic

classes of a communication,” such as “a fast traffic class [and] a slow traffic class.”

EX1001 at 7:44–54. Claim 6 is reproduced below in relevant part:

Method of communication service mapping in an integrated circuit, having a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein **said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S), . . .**

EX1001 at 10:7–18 (emphasis added).

c. **Weber Does Not Anticipate “at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules”**

**(1) Weber Does Not Anticipate “. . . at least one communication thread”**

151. Weber discloses a communication system including “a bus coupled to each of the functional blocks and configured to carry a plurality of signals. The plurality of signals includes a thread identifier that indicates a transaction stream that the data transfer is part of and a busy signal identified by the thread identifier.”

EX1007, Abstract. Specifically, Weber describes two types of thread identifiers, or Thread IDs: a “Request Thread Identifier (ReqThreadID) . . . that provides the

thread number associated with a current transaction intended for slave[, and a] Response Thread Identifier (RespThreadID) [that] provides a thread number associated with a current response.” EX1007, ¶ [0085], FIG. 11.

152. Dr. Hassoun alleges that the ReqThreadID associated with a request [from a master] discloses the “at least one communication service identification comprises at least one communication thread” recited in claim 6 of the ’052 Patent. EX1003, ¶ 193. The ’052 Patent explains that the communication service identification is “used to **identify traffic classes** of a communication,” such as “a fast traffic class [and] a slow traffic class.” EX1001, 7:44–54 (emphasis added). In contrast, Weber discloses that a thread identifier, e.g., a Thread ID or a ReqThreadID, **identifies a transfer**, e.g., a transaction. EX1007, ¶ [0123] (“thread identifier is an identifier of local scope that simply identifies transfers between the interface module and its connected functional block, . . .”); *id.*, ¶ [0123] (A Thread ID is an identifier of local scope that simply identifies transfers between the interface module and its connected functional block.”); Weber at Abstract (“The plurality of signals includes a thread identifier that indicates a transaction stream that the data transfer is part of . . . .”); *id.*, ¶ [0125] (“using a networking analogy, the Thread ID is a level-2 (data link layer) concept, whereas the CONNID is more like a level-3 (transport/session layer) concept.”). Indeed, the passage of Weber cited on page 123 of Dr. Hassoun’s Declaration explains that the thread identifier,

ReqThreadID, “is a four-bit signal that **provides the thread number associated with a current transaction** intended for slave 1104.” *id.*, ¶ [0085] (emphasis added). A POSITA would understand a “thread number” as used in Weber to be a unique identifier of the transaction, not a traffic class.

153. For at least the above reasons, Weber does not anticipate “at least one communication service identification comprises at least one communication thread” as required by claim 6 of the ’052 Patent.

**(2) Weber Does Not Anticipate “. . . at least one address range”**

154. Weber discloses a communication system including “a bus coupled to each of the functional blocks and configured to carry a plurality of signals.” Weber at Abstract. The plurality of signals may include an address signal, for example the “Addr” signals indicated in FIGS. 5 and 11 of Weber, that indicates “a particular resource that an initiator functional block wishes to access.” EX1007, ¶ [0080]. Dr. Hassoun alleges that this address signal discloses the “at least one communication service identification comprises . . . at least one address range” recited in claim 6 of the ’052 Patent. EX1003, ¶193. I disagree.

155. Dr. Hassoun asserts that “A POSA would understand that this [address signal of Weber] discloses the **capability** of issuing a request based on an address range.” EX1003 ¶ 193. However, as explained in Sec. III.C above, where a

prior art reference fails to explicitly disclose a claim element, the prior art reference inherently discloses the claim element only if the prior art reference must necessarily include the undisclosed claim element. Inherency *may not be established by probabilities or possibilities*. The fact that an element may result from a given set of circumstances is not sufficient to prove inherency. In other words, even if Dr. Hassoun were to show that the address signal in Weber were “capable” of comprising an address range (which in my opinion he has not shown, as discussed below), such a showing would be insufficient to prove anticipation of the claim element that the “communication service identification comprises . . . at least one address range.” For at least this reason, Weber does not anticipate “at least one address range” as required by claim 6 of the ’052 Patent.

156. Dr. Hassoun provides a circuitous four-page narrative that attempts to find an address range in Weber that does not exist. EX1003, ¶193. This confusing narrative is summarized as follows, and is discussed in further detail below (my summaries are below are not endorsements of Dr. Hassoun’s positions):

- (1) Weber discloses that for a read or write transfer, an initiator sends a target an address signal (EX1003, ¶ 193, p. 123);
- (2) Weber discloses that an interface includes a state register that stores a “client address base” (EX1003, ¶ 193, p. 125);

- (3) a POSITA would understand that the “client” in the “client address base” refers to a target (EX1003, ¶ 193, p. 126);
- (4) a POSITA would understand that the “address base” in the “client address base” indicates the target has a range of addresses (EX1003, ¶ 193, p. 125);
- (5) Weber discloses that for a write transfer, a target may be selected by decoding an external address portion of an ADDRE0 address (EX1003, ¶ 193, p. 126);
- (6) a POSITA would understand that the external address portion of the ADDRE0 address refers to the client address base (EX1003, ¶ 193, p. 126);
- (7) a POSITA would understand that there must be remaining portions of the ADDRE0 address distinct from the external address portion (EX1003, ¶ 193, p. 126);
- (8) a POSITA would understand that the alleged remaining portions of the ADDRE0 address must indicate internal portions of the address (EX1003, ¶ 193, p. 126);
- (9) a POSITA would understand that the alleged internal portions of the address indicate a range of addresses at which data is to be written (EX1003, ¶ 193, p. 126), and

(10) a POSITA would understand that the write request is based on the alleged address range.

157. With respect to item (1) above (Weber discloses that for a read or write transfer, an initiator sends a target an address signal), Weber discloses as much in paragraph [0052].

158. With respect to item (2) above (Weber discloses that an interface includes a state register that stores a “client address base”), Weber discloses as much in paragraph [0046].

159. With respect to item (3) above (a POSITA would understand that the “client” in the “client address base” refers to a target), Dr. Hassoun’s Declaration provides no explanation how or why a POSITA would understand this, at least because term “client” is used only twice in Weber, and in both cases, it is part of the compound term “client base address” without any reference to the target (“address base” is also used only twice). Moreover, Weber explains “FIG. 2 is a block diagram of an embodiment of an **initiator interface module 800**,” (EX1007, ¶ [0043] (emphasis added)), where “configuration registers 810 store bits that **determine the state of module 800, including** bandwidth allocation and **client address base**.” (EX1007, ¶ [0045]). In other words, the client address base determines a state of the initiator interface module—the client address base does not refer to a target.

160. With respect to item (4) above, (a POSITA would understand that the “address base” in the “client address base” indicates the target has a range of addresses), Dr. Hassoun’s Declaration provides no explanation how or why a POSITA would understand this, at least because term “range” is never used in Weber. A POSITA would, however, understand that a range has a lower bound and an upper bound. But nothing in Weber suggests that the client address base stored in the status register includes, indicates, or suggests a lower bound and an upper bound.

161. With respect to item (5) above (Weber discloses that for a write transfer, a target may be selected by decoding an external address portion of an ADDRE0 address), Weber discloses as much in paragraph [0056].

162. With respect to item (6) above, (a POSITA would understand that the external address portion of the ADDRE0 address refers to the client address base), Dr. Hassoun’s Declaration provides no explanation how or why a POSITA would understand this. As explained above with reference to item (3), Weber discloses that the client address base determines a state of the initiator module. Weber does not disclose or suggest that an external address portion of the ADDRE0 address refers to the client address base.

163. With respect to item (7) above (a POSITA would understand that there must be remaining portions of the ADDRE0 address distinct from the

external address portion), Dr. Hassoun's Declaration provides no explanation how or why a POSITA would understand this.

164. With respect to item (8) above (a POSITA would understand that the alleged remaining portions of the ADDRE0 address must indicate internal portions of the address), Dr. Hassoun's Declaration provides no explanation how or why a POSITA would understand this.

165. With respect to item (9) above, (a POSITA would understand that the alleged internal portions of the address indicate a range of addresses at which data is to be written), Dr. Hassoun's Declaration provides no explanation how or why a POSITA would understand this.

166. With respect to item (10) above (a POSITA would understand that the write request is based on the alleged address range), Dr. Hassoun's Declaration provides no explanation how or why a POSITA would understand this.

**(3) Weber Does Not Anticipate "said address range for identifying one or more second processing modules"**

167. Weber describes transfers between an initiator and a target that utilize an address signal.

Supported transfer types in this embodiment include, but are not limited to read and write transfers. Address lines 228 carry a multi-bit signal driven by an initiator bus owner **to specify the address of the object to be read or written** during the current transfer.").

EX1007, ¶ [0052]. A POSITA understands that an object to be read or written comprises data to be read from or written to a target. Therefore, the address signal identifies an address that may fall within a possible target; the address signal does not identify the target itself. This becomes crystal clear in the very next sentences of paragraph [0052] of Weber (which were omitted from Dr. Hassoun’s Declaration), which describe possible status indications of a current transfer where the first indication indicates that *the address signal does not select a target*.

Response lines 232 carry a multi-bit signal driven by a target to indicate the status of the current transfer. Supported responses include, but are not limited to the following responses. **A NULL response indicates that the current transfer is to be aborted, presumably because the address does not select any target.**

EX1007, ¶ [0052] (emphasis added). Moreover, Weber explains that a “[t]arget interface module 900 includes . . . state registers in state control block 916 [that] include registers that store, for example, client address base **and an identifier for target functional block 918.**” *Id.*, ¶[0046] (emphasis added). In other words, Weber does in fact disclose an identifier of a target, but that identifier is neither the address signal sent by an initiator nor the client address base stored in the state register of an interface. For at least these reasons, Weber does not anticipate “said address range for identifying one or more second processing modules” as required by claim 6 of the ’052 Patent.

**d. Weber Does Not Anticipate “coupling said plurality of processing modules (M, S) by an interconnect means (N)”**

168. Claim 6 of the '052 Patent further recites “coupling said plurality of processing modules (M, S) by an interconnect means (N) . . . .” '052 Patent at 10:19–20. I understand that the term “interconnect means” has been construed in the TI Litigation to mean “multi-hop interconnection between modules separated by one or more network nodes.” EX2022, 60. I understand that Samsung adopted the same construction in the Samsung litigation. EX2035, 2, n. 2. I understand the construction for the term “interconnect means” remains in dispute in the Qualcomm Litigation. EX2040, 22. It is my opinion that “multi-hop interconnection between modules separated by one or more network nodes” is the proper construction, as explained in Sec. V.D.1 above. Accordingly, Weber does not anticipate an interconnect means, as explained below.

169. Paragraphs 199–201 of Dr. Hassoun’s Declaration alleges that the system shown in FIG. 1 of Weber (reproduced below and annotated in red) discloses a multi-hop interconnection between modules separated by one or more network nodes because the system can include a bridge. Dr. Hassoun opines that “block ‘F’ from Figure 1 is a bridge between bus 114 of subsystem 102 and bus 112 of system 100.” EX1003, ¶ 201. In my opinion, this reasoning is flawed.

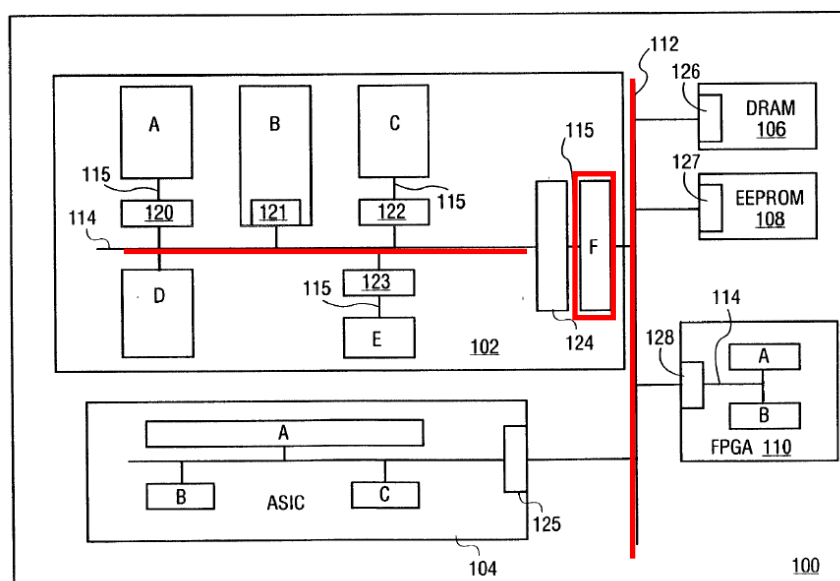


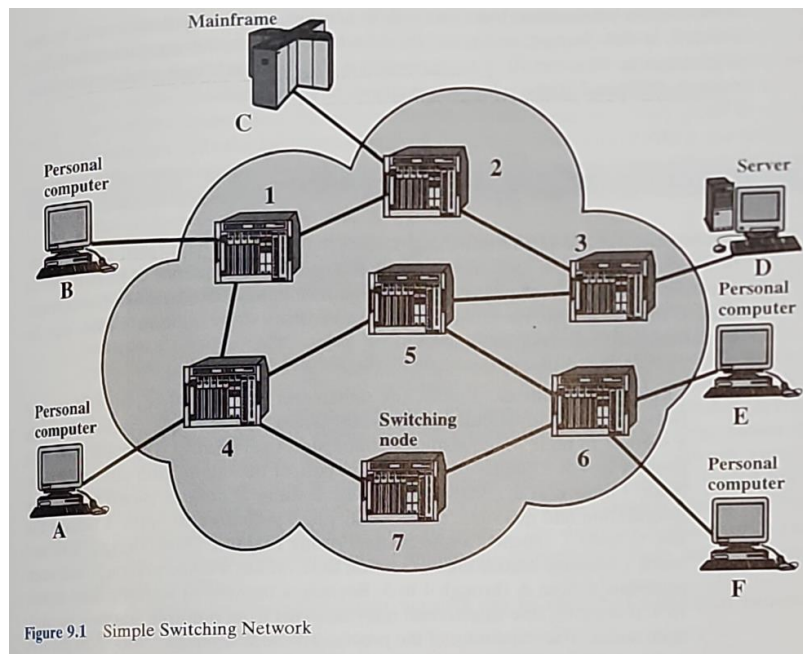
FIG. 1

EX1007, FIG. 1

170. With reference to FIG. 1, Weber identifies functional blocks by capital letters and module 124 as an interface module. EX1007, ¶ [0040]. Weber explains that “there are four fundamental types of functional blocks. . . . initiator, target, **bridge**, and snooping blocks.” EX1007, ¶ [0040]. Weber provides examples of an initiator and a target, but does not provide an example of a bridge or a snooping block because, in my opinion, these terms were well understood by a POSITA. A bridge is a simple device that connects two (or more) interconnects by repeating messages that it observes on a first interconnect to a second interconnect, and vice versa. *See, e.g.*, EX2010, 19-26 (hereafter “Stallings”); *see also* EX2013, 4–7. In contrast to a bridge, a switch or a router is a network node that switches data or messages, i.e., it selectively routes data or messages. *See, e.g.*, EX2010, 8.

Data entering the network from a station are routed to the destination by being switched from node to node. . . . Some nodes connect only to other nodes . . . . Their sole task is the internal (to the network) switching of data. Other nodes have one or more stations attached as well; in addition to their switching functions, such nodes accept data from and deliver data to the attached stations.

FIG. 9.1 of Stallings is reproduced below.



EX2010, 8.

171. A POSITA would understand that two buses (i.e., bus 114 and bus 112 of FIG. 1 of Weber) being connected by a bridge does not disclose or suggest a multi-hop interconnection between modules separated by one or more network nodes. For at least this reason, Weber does not anticipate “coupling said plurality of processing modules (M, S) by an interconnect means (N)” as required by claim 6 of the '052 Patent.

172. Paragraph 199–205 of Dr. Hassoun’s Declaration alleges that the system shown in FIG. 14 of Weber (reproduced below as annotated in red in Dr. Hassoun’s Declaration) discloses the interconnect means of the ’052 Patent because the data flow highlighted in red includes at least two ‘hops.’” EX1003, ¶ 203. I disagree at least because the communication subsystems in Weber are not network nodes and they do not cause data messages of a data flow to incur hops.

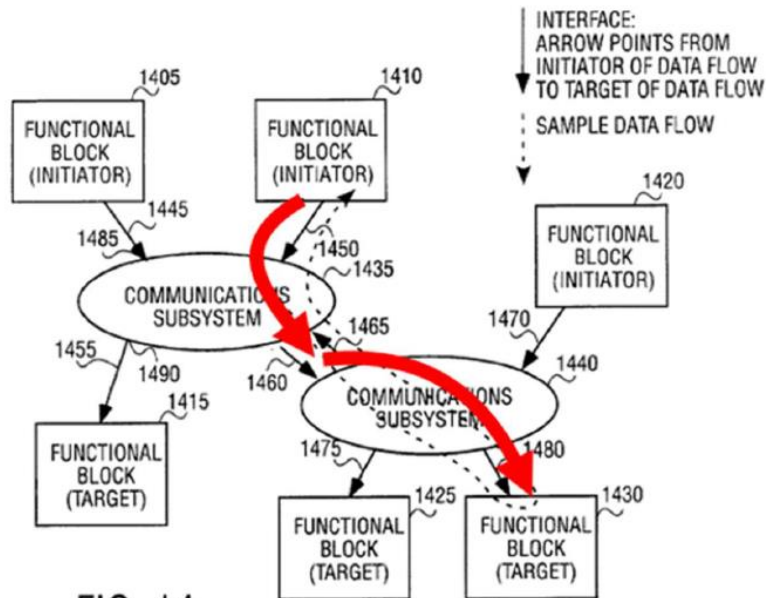


FIG. 14

173. A POSITA understand that each “hop” in a network corresponds to a network node, e.g., a switch or a router, that selectively routes data or messages, such that a “hop count” is the quantity of network nodes that a message encounters from initiator to target. *See, e.g.*, EX2005, 4 (“At each hop, the packet moves from one link to another . . . .”); *id.*, 5 (“[F]olded torus topology trades a longer average flit transmission distance for fewer routing hops.”); see also EX1001, 2:33–36

(“This is because of the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes.”). Page 136 of Dr. Hassoun’s Declaration appears to equate the process in Weber of choosing a channel for a particular data flow among multiple available channels, which is a step in the mapping process disclosed in Weber, to switching of data or messages, and thereby asserts that the communication subsystems cause messages of a data flow to incur hops. As explained below, the communication subsystems in Weber do not switch data or messages, e.g., they do not selectively route data or messages, and they therefore do not correspond to hops.

174. FIG. 17 of Weber (reproduced below and annotated in red) shows a step 1715 in which “a mapping of the data flow through the channels of the system is first determined.” EX1007, ¶ [0104]. FIG. 18 of Weber (reproduced below and annotated in red) shows “exemplary mapping process.” *Id.*, ¶ [0107].

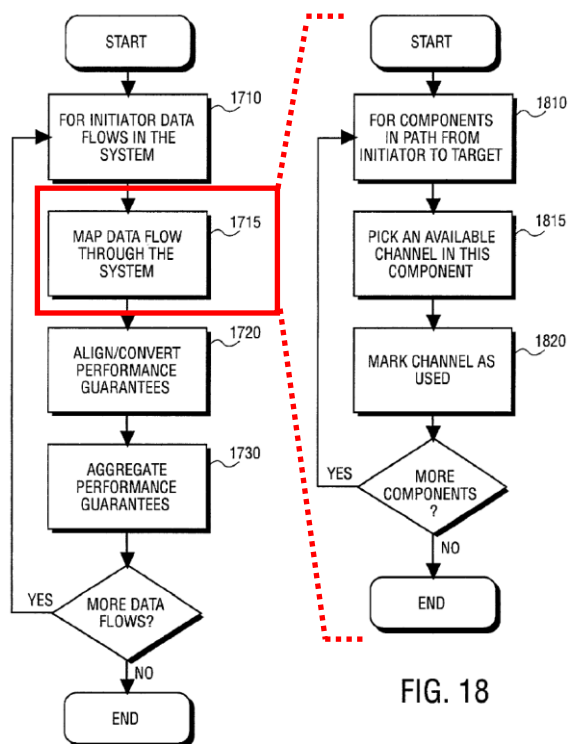


FIG. 17

FIG. 18

EX1007 FIGs. 17, 18

175. Weber explains that, during the mapping process, “[f]or each component in a path from initiator to target, e.g., through several interfaces and one or more communication subsystems step 1710, an available channel **is chosen** . . . [and] **one could choose** the channel that most closely matches the performance requirements of the initiator’s data flow.” EX1007, ¶ [0107] (emphasis added). Weber does not disclose or suggest that an available channel is chosen *by a communication subsystem* or that *a communication subsystem* could choose the channel.

176. Weber provides several embodiments for configuring the system with a mapping, but none disclose or suggest that a communication subsystem performs the channel-choosing step 1815 of the mapping process. “In one embodiment, the system is loaded with a revised mapping and the system is reconfigured accordingly.” EX1007, ¶ [0111]. Here, the mapping is determined prior to loading into the system, so this embodiment precludes the communication subsystems from performing the channel-choosing step 1815 of the mapping process. “In another embodiment, reconfiguration of the system may be accomplished by the system itself . . . .” EX1007, ¶ [0112]. Weber does not suggest any components or classes of components for performing the reconfiguration, e.g., for performing the channel-choosing step 1815 of the mapping process. “[I]n one embodiment, the system may initially be operated using a first mapping that generates an aggregation that does not meet the desired guarantees. However, the system would perform the steps described herein to determine a second mapping of data flows that results in aggregate guarantees that meets the application requirements.” EX1007, ¶ [0113]. Again, Weber does not suggest any components or classes of components for performing the reconfiguration, e.g., for performing the channel-choosing step 1815 of the mapping process.

177. In fact, Weber provides a reason to exclude a component, e.g., a communication subsystem, from a mapping. EX1007, ¶ [0108] (“[I]f a component

does not have enough channels to support the system, that component is not appropriate for the system and a different component should be chosen.”). To a POSITA, this would suggest that communication subsystems are *not* performing the channel-choosing step 1815. Indeed, Weber describes the data flow mapping process as a “global mechanism,” further indicating that the channel-choosing step is not a local process within a communication subsystem. EX1007, ¶ [0107] (“FIG. 18 focuses in on one embodiment of the data flow mapping process that is part of the global mechanism shown in FIG. 17.”)

178. In summary, the communication subsystems of the system of FIG. 14 of Weber do not perform the channel-choosing step of the mapping process, e.g., they do not switch data or messages, so they are not network nodes and they do not correspond to hops in a multi-hop interconnection. For at least the reasons described above, Weber does not anticipate “coupling said plurality of processing modules (M, S) by an interconnect means (N)” as required by claim 6 of the ’052 Patent.

**e. Weber Does Not Anticipate “controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N) by at least one network interface (NI) associated to said at least one first of said processing modules”**

179. At least because Weber does not anticipate the interconnect means of the '052 Patent as explained in Sec. VI.C.1.b, Weber does not anticipate the limitation of claim 6 of the '052 Patent that recites “controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N) by at least one network interface (NI) associated to said at least one first of said processing modules” (emphasis added).

**f. Weber Does Not Anticipate “mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification”**

180. At least because Weber does not anticipate the communication service identification of the '052 Patent as explained in Sec. VI.C.1.a, Weber does not anticipate the limitation of claim 6 of the '052 Patent that recites “mapping the requested at least one communication service . . . according to said at least one communication service identification” (emphasis added).

## **2. Independent Claim 1**

181. I understand that Dr. Hassoun opines that Weber discloses the limitations of independent claim 1 for the same reasons discussed for independent claim 6. See EX1003, ¶¶ 220–225. Thus, my opinions above regarding Weber for claim 6 apply to claim 1 as well.

## **3. Independent Claim 7**

182. I understand that Dr. Hassoun opines that Weber discloses the limitations of independent claim 7 for the same reasons discussed for independent claim 6. See EX1003, ¶¶ 226–227. Thus, my opinions above regarding Weber for claim 6 apply to claim 1 as well.

## **4. Dependent Claims**

183. The dependent claims are not anticipated by Weber for at least the same reasons that the independent claims from which they depend are not anticipated by Weber.

### **D. Ground 4: Purported Obviousness over Weber in view of Radulescu2004 (Claims 1-7)**

184. In Ground 4, Dr. Hassoun opines that claims 1-7 are rendered obvious by Weber in view of Radulescu2004. See EX1003, ¶¶ 232–251.

## **1. Independent Claim 6**

185. Claim 6 of the '052 Patent recites a method of communication service mapping in an integrated circuit where a first module requests a communication

service to a second module based on a communication service identification, where a communication service identification includes a communication thread or an address range identifying a second processing module of a memory region therein. The specification explains that “communication threads are used to identify traffic classes of a communication,” such as “a fast traffic class [and] a slow traffic class.”

’052 Patent at 7:44–54. Claim 6 is reproduced below in relevant part:

Method of communication service mapping in an integrated circuit, having a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein **said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S), . . .**

EX1001 at 10:7–18 (emphasis added).

186. As I explained in Sec. VI.C, Weber does not disclose or suggest many of the limitations of claim 6. The combination of Weber and Radulescu2004 does not cure those deficiencies.

## **2. Independent Claim 1**

187. I understand that Dr. Hassoun opines that Weber in view of Radulescu2004 discloses the limitations of independent claim 1 for the same reasons discussed for independent claim 6. See EX1003, ¶¶ 232–251. Thus, my

opinions above regarding Weber in view of Radulescu2004 for claim 6 apply to claim 1 as well.

### **3. Independent Claim 7**

188. I understand that Dr. Hassoun opines that Weber in view of Radulescu2004 discloses the limitations of independent claim 7 for the same reasons discussed for independent claim 6. See EX1003, ¶¶ 232–251. Thus, my opinions above regarding Weber in view of Radulescu2004 for claim 6 apply to claim 1 as well.

### **4. Dependent Claims**

189. The dependent claims are not rendered obvious by Weber in view of Radulescu2004 for at least the same reasons that the independent claims from which they depend are not rendered obvious by Weber in view of Radulescu2004.

## **VII. CONCLUSION**

190. In addition to the materials identified in Appendix, I may also review other documents in this matter. I may also review and comment upon the testimony of others that has been or will be given in this matter.

191. I reserve the right to add or to modify this expert report in the event that inaccuracies or omissions are discovered or if new or additional information is provided to me. I also reserve the right to make any such other changes as may be deemed necessary or appropriate.

192. I have not yet developed any demonstratives or illustrations to illustrate my opinions and the bases for those opinions; however, I reserve the right to present such demonstratives or illustrations at trial.

193. I reserve the right to supplement and/or amend my analyses and opinions expressed herein in response to any new, additional, or modified positions taken by Defendants, its experts or witnesses in reports, declarations, affidavits, or testimonies, whether in response to my report herein or in their coincident reports (or amendments thereto), to the extent such positions are relevant to the subject matter I have addressed in my report herein, or to the extent such positions cover topics relevant to this report for which Petitioners have the burden of proof.

I declare under penalty of perjury under the laws of the United States that the foregoing is a true and correct reflection of my opinions. This declaration is executed this 27th day of March, 2024.

A handwritten signature in black ink, appearing to read "Erik Chmelar". The signature is fluid and cursive, with the first name "Erik" and last name "Chmelar" clearly distinguishable.

Dr. Erik Chmelar

# APPENDIX 1

## ERIK CHMELAR

(650) 533-7952 | echmelar@yahoo.com

Subject matter expert in semiconductor hardware and software with over two decades of experience developing, implementing, and protecting advanced technologies including digital and mixed-signal systems, high-speed serial communications, 5G/wireless telecommunications, and smart medical devices.

### CREDENTIALS

#### EDUCATION —

- **JD, Intellectual Property**, Univ. Michigan Law School, Ann Arbor, MI 2015-2017
- **MBA, Management**, Western Michigan Univ., Kalamazoo, MI 2012-2013
- **BS, Chemical Physics**, Saginaw Valley State Univ., University Center, MI 2008-2011
- **PhD, Electrical Engineering**, Stanford Univ., Stanford, CA 2002-2004  
Dissertation: “Test and Diagnosis of Field-programmable Gate Arrays.”
- **MS, Electrical Engineering**, Stanford Univ., Stanford, CA 2000-2001
- **BS, Electrical Engineering**, Michigan Technological Univ., Houghton, MI 1997-2000

#### LICENSES AND CERTIFICATIONS —

- **Agile Certified Practitioner** (PMI-ACP, PMI) 2015-pres.
- **Certified Project Management Professional** (PMP, PMI) 2014-pres.
- **Licensed Professional Engineer** (PE, State of Michigan LARA) 2010-pres.
- **Licensed Patent Agent/Attorney** (State Bar of Michigan, USPTO) 2007-pres.

### EXPERIENCE

#### **Technical Expert, Semiconductor Hardware/Software**, Midland, MI 08/2007-pres.

- Serve as a technical expert witness for litigation in court and inter partes review (IPRs)
- Mine and analyze patent portfolios and develop assertion strategies for non-practicing entities (NPEs)
- Recent technology areas include memory, programmable hardware, microcontrollers, and AI devices

#### **Senior Counsel**, Young Basile Hanlon & MacFarlane, PC, Troy, MI 06/2023-pres.

- Draft and prosecute patent applications in a variety of semiconductor, software, and related arts
- Draft legal opinions for non-infringement, invalidity, and freedom-to-operate (FTO)
- Interview inventors, harvest inventions, and manage patent portfolios

#### **Senior Associate**, Dilworth IP, New Haven, CT 10/2020-06/2023

- Drafted and prosecuted patent applications in a variety of semiconductor, software, and related arts
- Drafted legal opinions for non-infringement, invalidity, freedom-to-operate (FTO), and export controls
- Interview inventors, harvest inventions, manage patent portfolios, and create technology landscapes

#### **Senior Associate**, Murphy, Bilak & Homiller, PLLC., Cary, NC 01/2020-06/2020

- Prosecuted patent applications for industry-leading wireless and semiconductor corporations
- Drafted approx. 100 office-action responses for complex 5G technologies
- Routinely referenced ETSI 3GPP specifications for prosecution of standard essential patents (SEPs)

#### **Senior Manager, Innovation Partners**, InterDigital, Inc., Wilmington, DE 09/2015-10/2018

- Created patent portfolios for 5G, IoT, connected/autonomous vehicles, and augmented/virtual reality
- Managed scientists and engineers to create over 100 new invention disclosures / patent applications
- Forged research partnerships with commercial and academic organizations to develop patent portfolios

**Co-founder, Managing Member**, Dera Industries LLC., Midland, MI 05/2016-07/2017

- Developed and productized the award-winning One-Tie™ re-usable tie strap consumer product
- Achieved \$1 million in annual sales prior to licensing the intellectual property

**Senior Principal Engineer, Adv. Dev.**, Stryker Corp., Kalamazoo, MI 02/2012-03/2015

- Supervised R&D of disruptive medical instruments and surgical technologies
- Formalized new business opportunities, developed budgets and timelines, and staffed project teams
- Collaborated with several top-tier universities to bring necessary expertise into the organization
- Delivered working prototypes for biophotonic devices and boundary-constraint surgical robotics

**Staff SW Engineer, Adv. Tech. Dev.**, LSI Corp. (Broadcom), Milpitas, CA 07/2004-01/2012

- Conducted R&D for very large scale integrated (VLSI) and serializer-deserializer (SerDes) circuits
- Granted approx. 20 patents for physical (PHY) interfaces, SerDes, and VLSI test architectures
- Made cutting-edge contributions in SerDes and test that were implemented in customer designs

**Adjunct Professor, ECE Dept.**, SVSU, University Center, MI 01/2009-01/2012

- Taught courses in digital circuits, computer architecture and organization, and data communications

**Consulting Assistant Professor, EE/CS Dept.**, Stanford University, Stanford, CA 09/2006-08/2008

- Advised PhD students on the test and reliability of VLSI circuits
- Created and taught a PhD-level course on clock and data recovery (CDR) for digital communications

**Product Test Engineer**, Xilinx, Inc., Los Gatos, CA (PhD. Intern, two summers) 06/2002-09/2003

- Engineered tools to detect and diagnose defects in FPGAs, which reduced diagnosis time by 75%

**Manufacturing Engineer**, Cisco Systems, Inc., San Jose, CA 11/1999-04/2002

- Oversaw functional testing of layer-2/3 network switches and determined root-cause failures

#### SERVICE AND MENTORING

---

**Admissions Representative**, Univ. Michigan Law School, Ann Arbor, MI 2018

- Advised prospective law students at 30 law fairs and forums

**Instructor**, National Science Foundation, Western Michigan Univ. I-Corps, Kalamazoo, MI 2015

- Taught Lean Startup and Business Canvas fundamentals to a cohort of 30 entrepreneurs

**Engineering Program Evaluator**, Accred. Board of Eng. & Tech. (ABET), Baltimore, MD 2013-2014

- Evaluated electrical engineering and computer engineering university educational programs

**Industry Mentor**, National Science Foundation, Univ. Michigan I-Corps, Ann Arbor, MI 2013

- Mentored teams of medical-device entrepreneurs participating in the I-Corps program

**Industry Mentor**, Western Michigan Univ., Starting Gate Accelerator, Kalamazoo, MI 2013

- Mentored entrepreneurs participating in the university startup-accelerator program

#### SELECT PROFICIENCIES

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- |                                          |                                        |
|------------------------------------------|----------------------------------------|
| • Hardware – Verilog, VHDL, ASICs, FPGAs | • Software – C/C++, Perl, Java, MatLab |
| • Engineering – COMSOL, ANSYS            | • CAD – SolidWorks, AutoCAD, Blender   |

### Select US Patents

US11446109B2, "Metal detection system for use with medical waste container," issued 2022-09-23.

US11389556B2, "Sterilization container capable of providing an indication regarding whether or not surgical instruments sterilized in the container were properly sterilized," issued 2022-07-19.

US11357877B2, "Sterilization enclosure for surgical instruments," issued 2022-06-14.

US§ 11225996B1, "Dual hook clasp," issued 2022-01-18.

US11002308B2, "Hook device with opposing jaws," issued 2021-05-11.

US11000341B2, "Metal detection system for use with medical waste container," issued 2021-05-11.

US10994906B2, "Easy-to-remove cable tie," issued 2021-05-04.

US10731698B2, "Hook device with rotatable opposing jaws," issued 2020-08-04.

US10604317B2, "Reusable tie strap with multiple apertures," issued 2020-03-31.

US10258706B2, "Sterilization container capable of providing an indication regarding whether or not surgical instruments sterilized in the container were properly sterilized," issued 2019-04-16.

US10010636B2, "Sterilization container capable of providing an indication regarding whether or not surgical instruments sterilized in the container were properly sterilized," issued 2018-07-03.

US9292644B2, "Row based analog standard cell layout design and methodology," issued 2016-03-22.

US9087157B2, "Low-loss transmission line TDM communication link and system," issued 2015-07-21.

US9014313B2, "Error signature analysis for data and clock recovery in a communication system," issued 2015-04-21.

US8982941B2, "Predictive selection in a fully unrolled decision feedback equalizer," issued 2015-03-17.

US8929497B2, "Dynamic deskew for bang-bang timing recovery in a communication system," issued 2015-01-06.

US8923382B2, "Tap adaptation with a fully unrolled decision feedback equalizer," issued 2014-12-30.

US8615062B2, "Adaptation using error signature analysis in a communication system," issued 2013-12-24.

US8527912B2, "Digitally obtaining contours of fabricated polygons," issued 2013-09-03.

US8432250B2, "Process variation based microchip identification," issued 2013-04-30.

US8121186B2, "Systems and methods for speculative signal equalization," issued 2012-02-21.

US7956790B2, "Systems and methods for synchronous, retimed analog to digital conversion," issued 2011-07-05.

US7973692B2, "Systems and methods for synchronous, retimed analog to digital conversion," issued 2011-06-07.

US7779320B2, "Low power scan shifting with random-like test patterns," issued 2010-08-17.

US7696915B2, "Analog-to-digital converter having reduced number of activated comparators," issued 2010-04-13.

US7656340B2, "Systems and methods for pipelined analog to digital conversion," issued 2010-02-02.

US7656339B2, "Systems and methods for analog to digital conversion," issued 2010-02-02.

US7328386B2, "Methods for using checksums in X-tolerant test response compaction in scan-based testing of integrated circuits," issued 2008-02-05.

US7293312B2, "Multipurpose skateboard tool," issued 2007-11-13.

US7210083B2, "System and method for implementing postponed quasi-masking test output compression in integrated circuit," issued 2007-04-24.

US7206983B2, "Segmented addressable scan architecture and method for implementing scan-based testing of integrated circuits," issued 2007-04-17.

US7093842B2, "Skateboard truck assembly," issued 2006-08-22.

US6979142B1, “Retractable tip mechanical pencil assembly,” issued 2005-12-27.

US6920621B1, “Methods of testing for shorts in programmable logic devices using relative quiescent current measurements,” issued 2005-07-19.

### Select Publications

- E. Chmelar, “Error signature analysis (ESA) receiver architecture for data communication,” DesignCon, 2012.
- E. Chmelar and C. Ito, “Mostly digital SerDes (MDS): a comprehensive low power receiver architecture,” DesignCon, 2012.
- I. Park, D. Lee, E. Chmelar, and E. McCluskey, “Inconsistent fails due to limited tester timing accuracy,” Proc. 26th VLSI Test Symp., 2008.
- A. Al-Yamani, N. Devta-Prasanna, E. Chmelar, M. Grinchuk, and A. Gunda, “Scan test cost and power reduction through systematic scan reconfiguration,” IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 26, pp. 907–918, 2007.
- A. Al-Yamani, E. Chmelar, and M. Grinchuk, “Segmented addressable scan architecture,” Proc. 23rd VLSI Test Symp., 2005.
- E. Chmelar, “Minimizing the number of test configurations for FPGAs,” Int. Conf. Computer Aided Design, 2004.
- E. Chmelar, “The test and diagnosis of FPGAs,” Ph.D. thesis, Stanford University, 2004.
- E. Chmelar and S. Toutounchi, “FPGA bridging fault detection and location via differential IDDQ,” Proc. 22nd VLSI Test Symp., 2004.
- E. Chmelar, “Subframe multiplexing: FPGA manufacturing test time reduction,” CRC TR-04-01, 2004.
- E. Chmelar, “Subframe multiplexing for FPGA manufacturing test,” Proc. Int. Symp. FPGAs, 2004.
- E. Chmelar, “FPGA interconnect delay fault testing,” Proc. Int. Test Conf., pp. 1239–1247, 2003.

### **Select Professional Organizations**

State Bar of Michigan  
Member (2018-pres.)

Project Management Institute  
Certified Agile Practitioner (2014-pres.)  
Certified Project Management Professional (2015-pres.)

Association for Computing Machinery  
Member (2018-2019)

Accreditation Board of Engineering and Technology  
Program Evaluator (2013-2018)

Institute of Electrical & Electronic Engineers  
Senior Member (2004-2018)

American Chemical Society  
Member (2013-2016)

National Science Foundation I-Corps  
Instructor (2015)  
Industry Mentor (2013)

American Society of Mechanical Engineers  
Member (2014-2015)

International Society of Optics & Photonics  
Member (2015)

## **APPENDIX 2--LISTING OF MATERIALS CONSIDERED**

| <b>Exhibit No.</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                              |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2003               | Neil Weste & David Harris, CMOS VLSI DESIGN: A CIRCUIT AND SYSTEMS PERSPECTIVE (4th ed. 2010)                                                                                                                                                                                                                                   |
| 2004               | Jan Rabaey, Anantha Chandrakasan & Borivoje Nikolic, DIGITAL INTEGRATED CIRCUITS: A DESIGN PERSPECTIVE (2nd ed. 2003)                                                                                                                                                                                                           |
| 2005               | William J. Dally & Brian Towles, <i>Route Packets, Not Wires: On-Chip Interconnection Networks</i> , PROC. 38TH DESIGN AUTOMATION CONF. (2001)                                                                                                                                                                                  |
| 2006               | John F. Wakerly, DIGITAL DESIGN: PRINCIPLES AND PRACTICES (4th ed. 2005)                                                                                                                                                                                                                                                        |
| 2007               | Fayez Gebali, Haytham Elmiligi & Mohamed Watheq El-Kharashi, NETWORKS-ON-CHIPS: THEORY AND PRACTICE (2009)                                                                                                                                                                                                                      |
| 2008               | Kurt Shuler, <i>Busses, Crossbars and NoCs: The 3 Eras of SoC Interconnect History</i> , ARTERISIP (Oct. 22, 2010), <a href="https://www.artemis.com/blog/busses-crossbars-and-nocs-the-3-eras-of-soc-interconnect-history/">https://www.artemis.com/blog/busses-crossbars-and-nocs-the-3-eras-of-soc-interconnect-history/</a> |
| 2009               | Kurt Shuler, <i>The SoC Interconnect Fabric: A Brief History</i> , ARTERISIP (Aug. 6, 2013), <a href="https://www.artemis.com/blog/the-soc-interconnect-fabric-a-brief-history/">https://www.artemis.com/blog/the-soc-interconnect-fabric-a-brief-history/</a>                                                                  |
| 2010               | William Stallings, DATA & COMPUTER COMMUNICATIONS (6th ed. 1999)                                                                                                                                                                                                                                                                |
| 2013               | Frank Derfler, Jr. & Les Freed, HOW NETWORKS WORK, Chapter 22 “Repeaters, Bridges, Routers, and Switches” (4th ed. 1998)                                                                                                                                                                                                        |
| 2014               | IEEE 100: The Authoritative Dictionary of IEEE Standard Terms (7th ed. 2000)                                                                                                                                                                                                                                                    |
| 2015               | Douglas Downing et al., Dictionary of Computer and Internet Terms, BARRON’S (7th ed. 2000)                                                                                                                                                                                                                                      |
| 2016               | David Patterson and John Hennessey, COMPUTER ORGANIZATION & DESIGN (2nd ed. 1998)                                                                                                                                                                                                                                               |

| Exhibit No. | Description                                                                                                                                                                                                                                                           |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2022        | Claim Construction Order, <i>Network System Technologies, LLC v. Texas Instruments Incorporated</i> , Civil Action No. 2:22-cv-00482-RWS (E.D. Tex.), Dkt. 150 (Jan. 3, 2024)                                                                                         |
| 2033        | P.R. 4-3 Claim Construction and Prehearing Statement, <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd.</i> , Civil Action No. 2:22-cv-00482-RWS (E.D. Tex.), Dkt. 91 (Jan. 9, 2024)                                                               |
| 2035        | Defendant Samsung Electronics Co., Ltd.’s Responsive Claim Construction Brief, <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd.</i> , Civil Action No. 2:22-cv-00482-RWS (E.D. Tex.), Dkt. 112 (March 12, 2024)                                   |
| 2040        | Defendants’ Joint Opening Claim Construction Brief, <i>Network System Technologies, LLC v. Qualcomm Incorporated et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.), Dkt. 77 (Oct. 12, 2023)                                                                  |
|             | 2023-12-19 - Paper 3 - Petition for Inter Partes Review of US 7,594,052                                                                                                                                                                                               |
| 1001        | U.S. Patent No. 7,594,052                                                                                                                                                                                                                                             |
| 1002        | File Wrapper for U.S. Patent No. 7,594,052                                                                                                                                                                                                                            |
| 1003        | Declaration of Dr. Marwan Hassoun                                                                                                                                                                                                                                     |
| 1005        | A. Rădulescu, et al. "An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration," Proceedings of the Design, Automation and Test in Europe Conference and Exhibition, 2004 (“Rădulescu2004”) |
| 1006        | Open Core Protocol Specification, Release 1.0, OCP-IP Association (2001) (“OCP”)                                                                                                                                                                                      |
| 1007        | U.S. Patent Publication No. 2002/0129173 A1 (“Weber”)                                                                                                                                                                                                                 |
| 1008        | U.S. Patent No. 5,948,089 (“Wingard”)                                                                                                                                                                                                                                 |
| 1009        | Networks on Chip; Axel Jantsch, Hannu Tenhunen (Eds.). Kluwer                                                                                                                                                                                                         |

| <b>Exhibit No.</b> | <b>Description</b>                                                                                                                                                                     |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                    | Academic Publishers, Boston (2003) (“Jantsch”)                                                                                                                                         |
| 1010               | A. Rădulescu, et al. “Communication Services for Networks on Chip,” Philips Research Laboratories, Eindhoven, The Netherlands, SAMOS, II(), 275–299 (2002) (“Rădulescu2000”)           |
| 1011               | J. Dielissen, et al. “Concepts and Implementation of the Philips Network-on-Chip,” Philips Research Laboratories, Eindhoven, The Netherlands (2003) (“Dielissen”)                      |
| 1016               | Defendant’s Opening Claim Construction Brief, Network System Technologies, LLC v. Qualcomm Inc. et al., 1:22-cv-01331 (W.D. Tex.)                                                      |
| 1017               | Network System Technologies, LLC’s Response to Defendants’ Joint Opening Claim Construction Brief, Network System Technologies, LLC v. Qualcomm Inc. et al., 1:22-cv-01331 (W.D. Tex.) |
| 1020               | U.S. Patent No. 7,366,818                                                                                                                                                              |
| 1021               | P. Guerrier et al., “A generic architecture for on-chip packet-switched interconnections,” Proceedings Design, Automation and Test in Europe Conference and Exhibition 2000 (2000)     |
| 1022               | William J. Dally et al., “Route Packets, Not Wires: On-Chip Interconnection Networks,” Proceedings –Design Automation Conference (2001)                                                |
| 1023               | Shashi Kumar et al., “A Network on Chip Architecture and Design Methodology,” IEEE Computer Society Annual Symposium (2002)                                                            |
| 1024               | José Duato et al., Interconnection Networks, An Engineering Approach. Revised Printing (2003)                                                                                          |
| 1025               | Luca Benini et al., “Powering Networks on Chips, Energy-efficient and reliable interconnect designs for SoCs. Proceedings of the International Symposium on Systems Synthesis” (2001)  |
| 1026               | Andrew S. Tanenbaum, Computer Networks, Third Edition                                                                                                                                  |

| Exhibit No. | Description                                                                                                                                                        |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             | (1996)                                                                                                                                                             |
| 1027        | Network System Technologies, LLC's Sur-Reply Claim Construction Brief, <i>Network System Technologies, LLC v. Qualcomm Inc. et al.</i> , 1:22-cv-01331 (W.D. Tex.) |