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An efficient on-chip network interface offering guaranteed services, shared-memory abstraction, and flexible network configuration

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Abstract:

In this paper we present a network interface for an on-chip network. Our network interface decouples computation from communication by offering a shared-memory abstraction, which is independent of the network implementation. We use a transaction-based protocol to achieve backward compatibility with existing bus protocols such as AXI, OCP and DTL. Our network interface has a modular architecture, which allows flexible instantiation. It provides both guaranteed and best-effort services via connections. These are configured via network interface ports using the network itself, instead of a separate control interconnect. An example instance of this network interface with 4 ports has an area of 0.143 mm²/sup 2/ in a 0.13 /spl mu/m technology, and runs at 500 MHz.

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Contents

1 Introduction

Networks on chip (NoC) have been proposed as a solution to the interconnect problem for highly complex chips [2], [3], [5], [9],[12], [14], [15], [17], [21],[27]. NoCs help designing chips in several ways: they (a) structure and manage wires in deep sub-micron technologies [2], [3], [9], [12], [21], (b) allow good wire utilization through **Signaling (5) CIP (12), R24 (10)** scale better than buses [14], [21], (d) can be energy efficient and reliable [2], [5], and (e) decouple computation from communication through well-defined interfaces, enabling IP modules and interconnect to be designed in isolation, and to be integrated more easily [2], [13], [21],[24].

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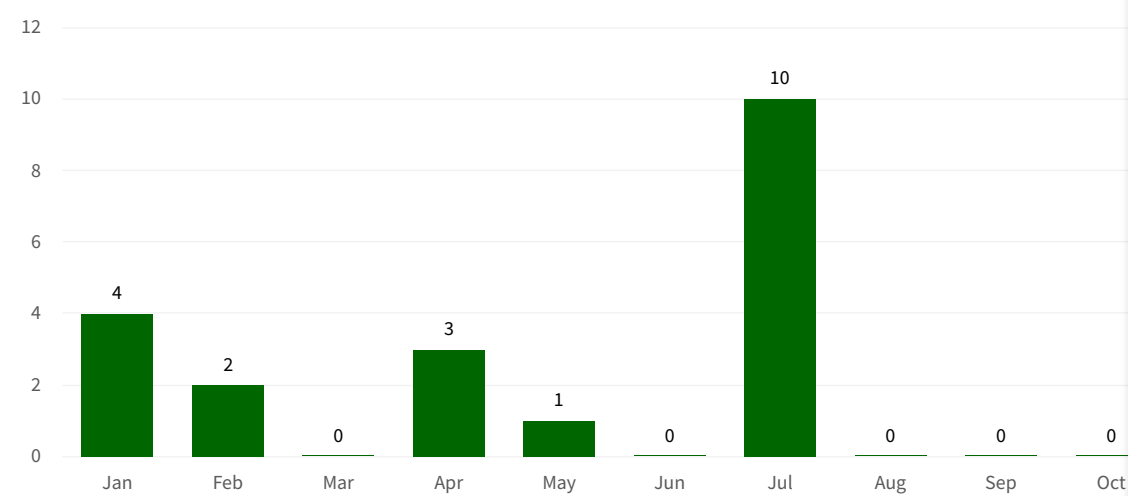
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