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CALL FOR PAPERS

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**Conference and Exhibition:
February 16th - 20th , 2004 CNIT La Défense, Paris, France**

Final Call for Papers

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- ▶ ASP-DAC
- ▶ ITC
- ▶ ICCAD

The 7th DATE conference and exhibition is the main European event bringing together design automation researchers, users and vendors, as well as specialists in the design, test, and manufacturing of electronic systems and circuits.

The five-day event consists of a conference with plenary keynotes, regular papers, interactive presentations, panels and hot-topic sessions, tutorials, master courses and workshops, as well as a Designers' Forum. In addition, DATE has a commercial exhibition showing the state-of-the-art in design and test tools, methodologies, IP and design services, as well as the organisation of a PCB symposium. Both the conference and the exhibition, together with the many user group meetings, fringe meetings, university booth and social events offer a wide variety of opportunities to meet and exchange information.

The conference

The conference addresses all aspects of research into technologies for electronic and (embedded) systems engineering. It covers the design process, test, and tools for design automation of electronic products ranging from integrated circuits to distributed large-scale systems. This includes both hardware and embedded software design issues. The conference scope also includes the elaboration of design requirements and new architectures for challenging application fields such as telecom, wireless communications, multimedia and automotive systems. Persons involved in innovative industrial designs are particularly encouraged to submit papers to foster the feedback from design to research. See the detailed guidelines and topic areas for submission below.

Panels, hot-topic sessions and embedded tutorials highlight and inform about emerging topics. In addition, two Special Days in the program will focus on ULTRA LOW POWER and TRENDS IN MULTIMEDIA, which are two emerging areas bringing new challenges to the system design community.

On the first day of the DATE event, half-day in-depth technical tutorials on selected topics are organised by leading experts in the respective fields. The tutorials are suited for both researchers and tool developers, as well as for designers who want to be brought up to date on the newest developments.

Also, a series of Master Courses will be organised on the last day of the DATE event. Authoritative professionals in the industry and academics alike will bring practical in-depth design knowledge of integrated circuits and embedded systems in important application areas.

To widen the basis for discussions on innovative designs, there will be a Designers' Forum for application-oriented contributions that discuss the use of innovative design and test methods and tools as well as case studies. Also, on the first day of the DATE event, comprehensive designer-oriented Designers' Forum tutorials will be organised, that allow a personal experience of design methodologies and vendor tools in new product areas.

In addition, new in 2004, Friday workshops will be organised on specialised topics.

The exhibition

The conference is complemented by the largest exhibition in Europe for vendors of tools and services for the design, development and test of Systems-on-Chip, IP, Embedded Systems, ASICs, FPGAs and PCBs. The DATE Exhibition has also grown to cover a broad range of design reuse technologies and services, with showcase 'villages' on the show floor dedicated to semiconductor IP, reconfigurable computing and DSP technologies, as well as a PCB symposium.

DATE uses the support of vendor companies and the industrial community to inform attendees on commercial and design related topics. The Exhibition Programme comprises Industry Tutorials, the PCB Symposium, and the Focus on Business and Industry which takes place in a dedicated theatre on the exhibition floor.

TOPIC AREAS FOR SUBMISSION

Within the scope of the conference, the main areas of interest are organised in the following tracks. Submissions can be made to any of the track topics. For detailed descriptions of the track topics, [click here](#).

Track A. Design Methodologies and Experiences, where the emphasis is on challenges and experiences in the design of advanced electronic and embedded systems, not only to obtain designer feedback on existing design methods and tools but also to initiate discussions on requirements of future system architectures, design flows and environments.

This track is organised in the following topics:

- A1 System Design Methods and Case Studies
- A2 Design of RF, Analogue and Mixed-Signal Circuits and Systems
- A3 Design of Low-Power Systems and Case Studies
- A4 Platform design and VC Reuse Methods
- A5 Reconfigurable Computing
- A6 Real-time OS and deeply Embedded Software
- A7 Multi-processors and Networks on Chip

Track B. CAD Tools, Algorithms and Languages, addressing design automation and design tools for electronic and embedded systems. Emphasis is on methods and tools related to the use of computers in designing products. This includes fully automatic as well as computer-assisted methods, data and design management techniques and user interfaces.

This track is organised in the following topics:

- B1 System-Level Specification
- B2 Real-Time Embedded Systems
- B3 Simulation and Emulation
- B4 Hardware-Software Co-Design
- B5 Architectural Synthesis
- B6 Logic and FSM Synthesis
- B7 Physical Design and Verification
- B8 CAD for RF, Analogue and Mixed-Signal Design
- B9 Interconnect, EMC and Packaging Modelling
- B10 Formal Verification

B11 Design Aspects of Emerging Technologies and Applications
B12 Power Estimation and Optimisation

Track C. Methods, Tools and Innovative Experiences in Testing Electronic Circuits and Systems, where emphasis is on design-oriented embedded test solutions as well as defect analysis, modelling, test generation and silicon debugging.

This track is organised in the following topics:

C1 Defect-Based Testing and Test Techniques for Special Architectures
C2 RF, Analogue and Mixed-Signal Test
C3 Test Generation
C4 BIST and Design-for-Testability
C5 SoC / SoB Test and Test Resource Partitioning
C6 Field-Oriented Test and On-line Testing

Track D. Designers' Forum is devoted to the presentation and discussion of design experiences and methodologies using state-of-the-art design tools. The main scope of this Forum is to give designers insight in the design experiences of other designers. Contributions should show the potential of state-of-the-art technology through industrial design experiments or how to address practical design problems that CAD tools cannot solve today. Papers will be published by IEEE in a separate Proceedings volume.

The topics are designs and/or design and test experiences in the fields of:

D1 Embedded Systems and Software
D2 VLSI and Systems-on-Chip
D3 RF, Analogue and Mixed-Signal
D4 Intellectual Property (IP) Platforms and Re-use
D5 System Environments for Reconfigurable Computing
D6 Automotive Hardware and Software Systems
In addition, we welcome proposals for Special Sessions, Tutorials and Master Courses, and submissions for the Special Days on Ultra Low Power and New Trends in Multimedia.

SPECIAL SESSIONS

Special Sessions can take the form of Panels, where visionary and/or controversial issues are discussed, Hot-Topic Sessions, dealing with the introduction and discussion of new R&D problems, and Embedded Tutorial Sessions, addressing trends in the technical domains that are of interest to the conference participants.

Special Session proposals consist of an extended summary of up to 1500 words describing the session content and format, and must be submitted via the Web site by Sept. 7, 2003. Proposals will be evaluated with regard to their potential interest to the audience and cohesion with the scope of the event.

Contributors of accepted special sessions will be asked to submit final texts or statements of panellists, as appropriate, for publication in the Proceedings (deadline Nov. 21, 2003). Panel sessions are entitled to one page only in the Proceedings, whereas Embedded Tutorials and Hot Topic sessions are allocated a maximum of six pages per session. For more information, please contact: Donatella Sciuto sciuto@elet.polimi.it
Tel: +39 022 399 3662 Fax: +39 022 399 3611

TUTORIALS / MASTER COURSES

On the day before (resp. after) the conference and exhibition, half-day technical tutorials (resp. full-day Master Courses) will be organised. Proposals should be sent by Sept. 7, 2003 directly to:
Luca Benini lbenini@deis.unibo.it
Tel: +39 051 209 3782 Fax: +39 051 644 3073

UNIVERSITY BOOTH

A University Booth will be organised in order to help the transfer of technology to industry. Research institutes and universities interested in demonstrating their results should contact by mid January 2004:

Marie-Minerve Louerat marie-minerve.louerat@lip6.fr
Tel: +33 144 27 70 12 Fax: +33 144 27 72 80

PCB SYMPOSIUM

The PCB Symposium will address the challenges of designing high-speed boards and systems. It consists of vendor-neutral technical in-depth papers as well as papers of PCB designers, covering the aspects of signal integrity and timing constraints on board. Submissions for participation with a presentation should be sent by Sept. 21, 2003, to:
Carsten Elgert carsten_elgert@mentorg.com
Tel: +49 89 57096 344 Fax: +49 89 57096 422

FRIDAY WORKSHOPS

DATE also offers the possibility for Friday workshops on novel topics. These workshops may be used by individual researchers, Networks of Excellence, EU projects, etc, to promote novel topics for the DATE conference. For detailed descriptions on how to propose Friday workshops, please refer to the website. Information can be obtained from, and proposals should be sent by Sept. 21, 2003, to:
Teresa Riesgo teresa@upmdie.upm.es
Tel: +34 91 336 31 91 Fax: +34 1 564 5966

FRINGE MEETINGS

There are a limited number of rooms available for the organisation of non-commercial fringe meetings (birds of a feather sessions) open to all DATE attendees, as well as for the organisation of appropriate on-site closed meetings. Requests are considered in the order of their arrival, and should be directed to:
Michel Renovell renovell@lirmm.fr
Tel: +33 467 41 85 23 Fax: +33 467 41 85 00
Requests for commercial meetings should be directed to the Exhibition Secretariat and will incur the standard room charges.

TRAVEL ASSISTANCE

Limited travel assistance is available for worthy individuals. Priority is given to students and conference contributors. See the Web site for more information.

COMMITTEES

[Click here](#) for a full list of the executive and programme committee members.

SPONSORS

The event is sponsored by the European Design and Automation Association, the EDA Consortium, the IEEE Computer Society – TTTC, ECSI, ACM SIGDA, and RAS. In cooperation with IFIP WG 10.5.

CONTACT

Conference Secretariat

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Exhibition Secretariat

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London EC1N 8SR, UK exhibitions@edaltld.co.uk
To add your name to the mailing list, please contact the Conference Secretariat.

SUBMISSION INSTRUCTIONS

All manuscripts for any of the above technical topics must be submitted for review electronically, following the instructions on the conference Web page:

www.date-conference.com

Accepted file formats are PDF and Postscript. Manuscripts received in hard-copy form will not be processed.

Papers can be submitted for either standard oral presentation or for interactive presentation. Standard oral presentations require novel and complete research work supported by experimental results, and are held in front of a full audience. Besides these, for the first time in 2004, DATE will accommodate interactive presentations of novel ideas that may still require additional research work or still lack experimental data, but can be presented in a vivid face-to-face discussion with other researchers working in the same area. The interactive format can take several forms, e.g. laptop presentation, slide show, demo, poster, etc.

Submissions should not exceed 6 pages in length for oral-presentation and 2 pages in length for interactive-presentation papers, and should be formatted as close as possible to the final format: A4 or letter sheets, double column, single spaced, Times or equivalent font of minimum 10pt (templates are available on the DATE Web site for your convenience). To permit blind review, submissions should not include the author names. Any submission not in line with the above rules will be discarded.

All papers will be evaluated with regard to their suitability for the conference, originality and technical soundness. The Programme Committee reserves the right to accept interesting contributions that do not meet the criteria for standard oral presentations, as interactive presentations.

SUBMISSION KEY DATES

A, B, C papers:	September 7, 2003
D papers:	September 7, 2003
Special session proposals:	September 7, 2003
Tutorial/MC proposals:	September 7, 2003
PCB symposium:	September 21, 2003
Notification of acceptance:	November 3, 2003
Camera-ready paper due date:	November 21, 2003

Chairs

General Chair: Joan Figueras, Universitat Politècnica de Catalunya, Spain
<figueras@eel.upc.es>

Program Chair: Georges Gielen, Katholieke Universiteit Leuven, Belgium
<gielen@esat.kuleuven.ac.be>

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