



**Das Medienkonzept**
für Elektronik & Entwicklung

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Press Releases

Official DATE Releases

- ▶ 31/01/2006 DATE'06 extends lead as premier European forum..
- ▶ 15/11/2005 DATE Receives Again Record Submissions
- ▶ DATE06 PRESS SLIDES (PDF 400 KB)

DATE NEWSLETTER ONLINE

DATE IN THE NEWS

- ▶ EETimes DATEnet
- ▶ EPN Online DATE 04: This Season's Paris Collectiont
- ▶ EDA Cafe Weekly: Getting More than You Pay For - Part I
- ▶ Der Markt schrumpft, das Anwenderinteresse steigt

EXHIBITOR PRESS RELEASES

DATE 05 Photos

For press registrations please e-mail date@edatld.co.uk





DATE06

Download DATE06 Logo @ 300 dpi Tiff
(300 Kb Zip)

Quick Index ▼

Committees

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Sponsors & Partners

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Sister Conferences

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DATE Events

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Sponsored by the European Design and Automation Association, the EDA Consortium, the IEEE Computer Society - TTTC, ECSI, RAS and ACM SIGDA

web archive org/web/20060314041112/http //www date conference com/exhibition/press htm

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Qualcomm Exhibit 1040
Qualcomm v. Network System Technologies - IPR2024-00343



DATE Press Preview, London January 31st, 2006





DATE Press Preview, Munich 1 February, 2006





DATE Press Preview, Paris 22 February, 2006





Presentation overview

- The big news...
- What's new at DATE'06
- DATE in numbers
- Conference programme at a glance
- Special events at DATE'06



What's new at DATE'06

DATE - the world's premier electronic system design event

- Reflects the moving industry focus from "traditional ASIC" design to "platform-level" system design
- Programme covers **all system design challenges**
 - Hardware (IC, SoC, FPGA, IP platforms)
 - Embedded Software
 - Test
 - PCB Integration
- Creates a **strong application-specific focus**
 - Stronger and higher-quality designer's forum – direct involvement in programme selection by STM, Infineon, Philips and many other companies
 - Strategic application domains – Wireless Communications and Networking, Media and Signal Processing, Secure Systems, Automotive
- New **System Design Records** track



New Initiatives at DATE'06

To reflect the system-level emphasis :

New **Technical Conference** Features

- **System Design Records** track
 - presentation of "record" system designs implemented on various platforms best performance, first design ever, etc.
- **Embedded Software** track in co-operation with ACM-SIGBED
- Two special days with application focus:
 - 4G Telecom Applications and Design
 - Wireless Sensor Networks
- Full-day special-interest workshops on **Biochips, Automotive, Reconfigurable Computing, Distributed Systems** and **Networks on Chip**

Exhibition

- New "system-level" exhibitors include: **Altera, Rambus**
- Returning "system-level" exhibitors include: **ARM, Mathworks, Tensilica**

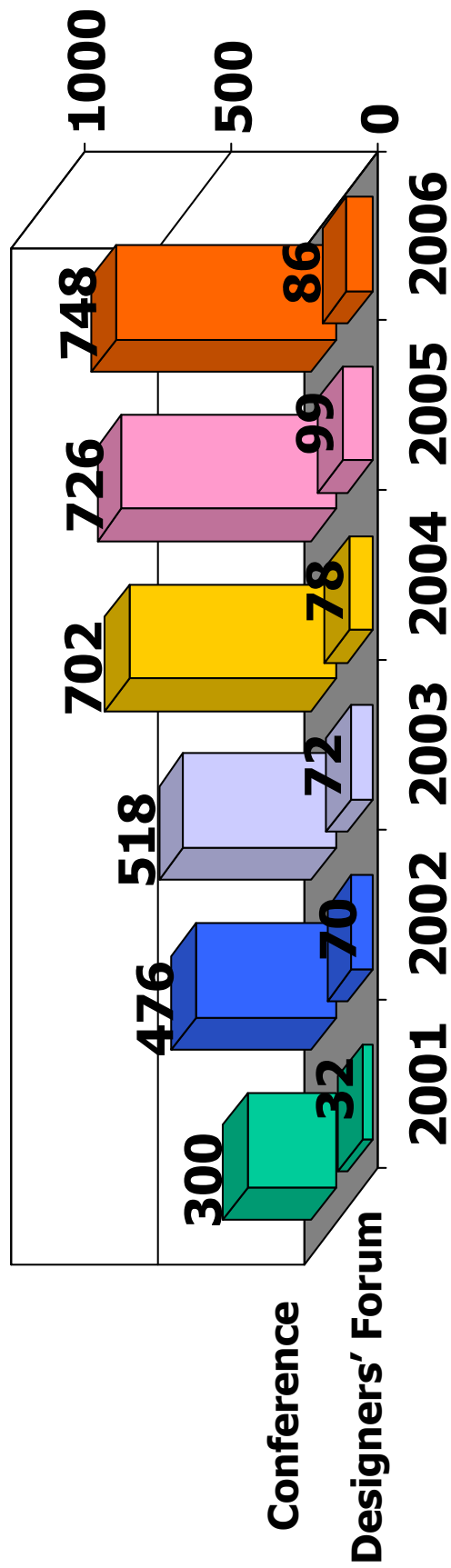
Industry Initiatives

- Greater involvement by 'application-specific' industry groups, e.g. **AUTOSAR**
- Greater involvement by leading edge trade standards initiatives, e.g. **SPIRIT, Accellera**
- Corporate delegate arrangements in place with **Infineon, STM** and **Philips**
- 5 **Designers' Solutions workshops** addressing hot topics in the fields of system design, verification and FPGA design



DATE in numbers

Paper submission trends





Conference Programme

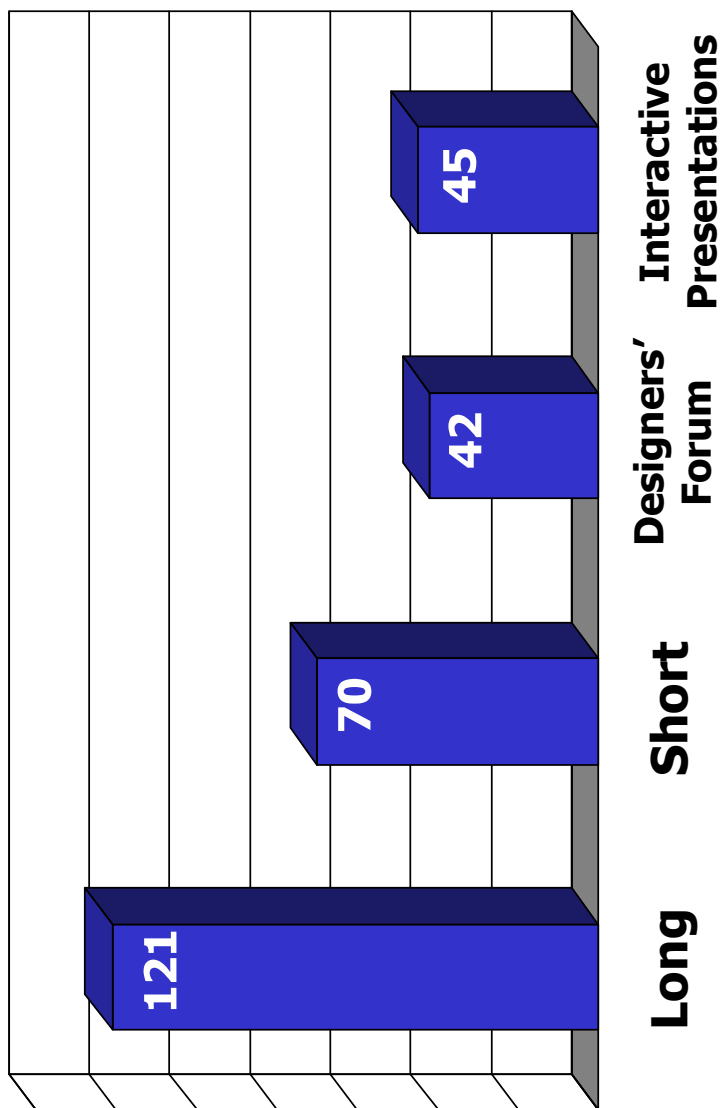
Submissions

	DATE 01	DATE 02	DATE 03	DATE 04	DATE 05	DATE06
Topics	22	24	25+4	25+6	26+9	26+7
Papers submitted (reg+DF)	300+32	476+70	518+72	702+78	726+99	748+86
TPC members	220	260	332	372	342	388
Reviews	1800	2767	2927	4054	3987	3808
Number of tracks	5	6	6 + 1	7+1	7 + 1	7+1



DATE in numbers

Accepted papers





Conference Programme

Quality keeps improving :

- only high-quality papers accepted
- on average 5 reviews per paper !!

Acceptance Rate	DATE 01	DATE 02	DATE 03	DATE 04	DATE 05	DATE 06
Long	27%	19%	17%	17%	18%	16%
Long+Short	35%	30%	26%	26%	26%	28%
Long+Short+DF	46%	35%	33%	33%	29%	33%



DATE in numbers

Conference programme

- 78 technical sessions in total, incl. 7 special sessions
- 2 plenary keynotes
- 2 special focus days (incl. dedicated keynotes)
- Interactive presentations

Executive track (full day)

- 3 panels with CEOs, CTOs, VPs

Exhibition programme

- Exhibition Theatre (Focus on Business and Industry)
- PCB Symposium
- 5 Designers' Solutions workshops

Educational activities

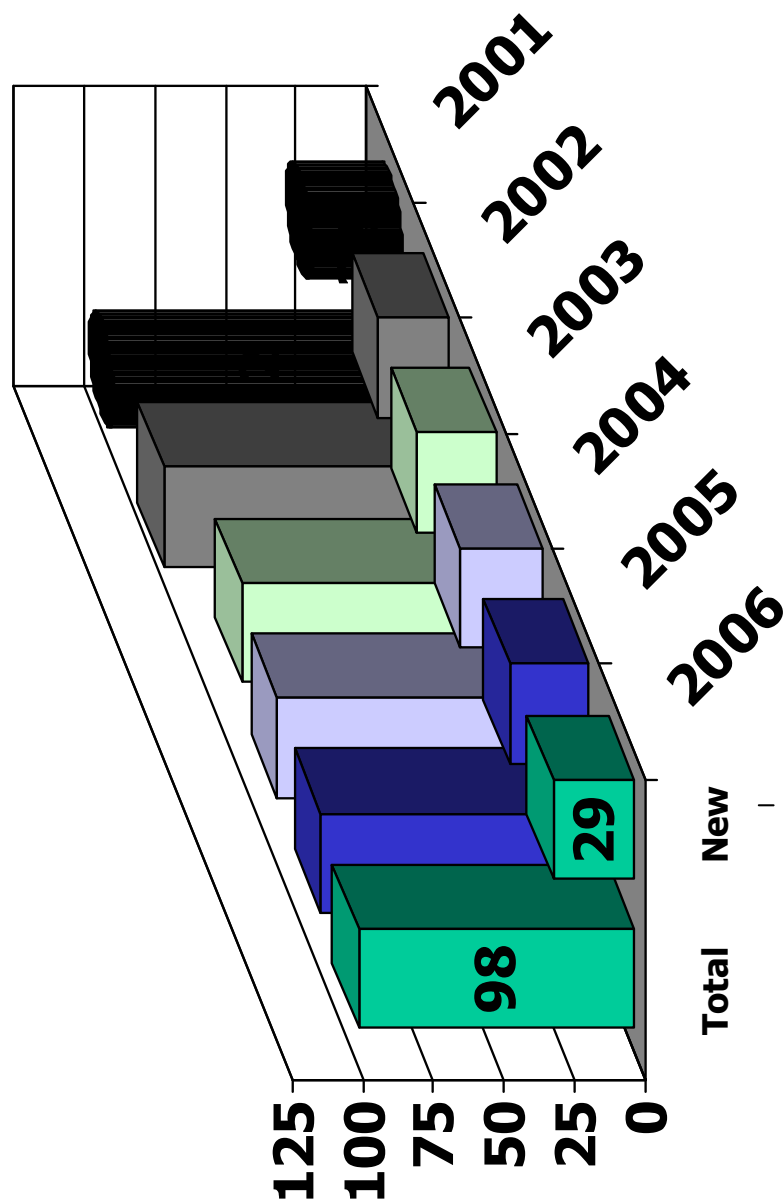
- 8 half-day & 3 full-day Tutorials (Monday)
- 5 special-interest workshops (Friday)

20+ fringe meetings (incl. Accellera, OCP-IP, IBIS, SystemC Users' Group)



DATE in numbers

Exhibiting Companies



* 2006 data : status on Jan 25, 2006



DATE in numbers

Exhibition is smaller but is diversifying into a system-led event with many new exhibitors

- Exhibiting Companies : 98
- Rebooked: 69
- New exhibitors: 29

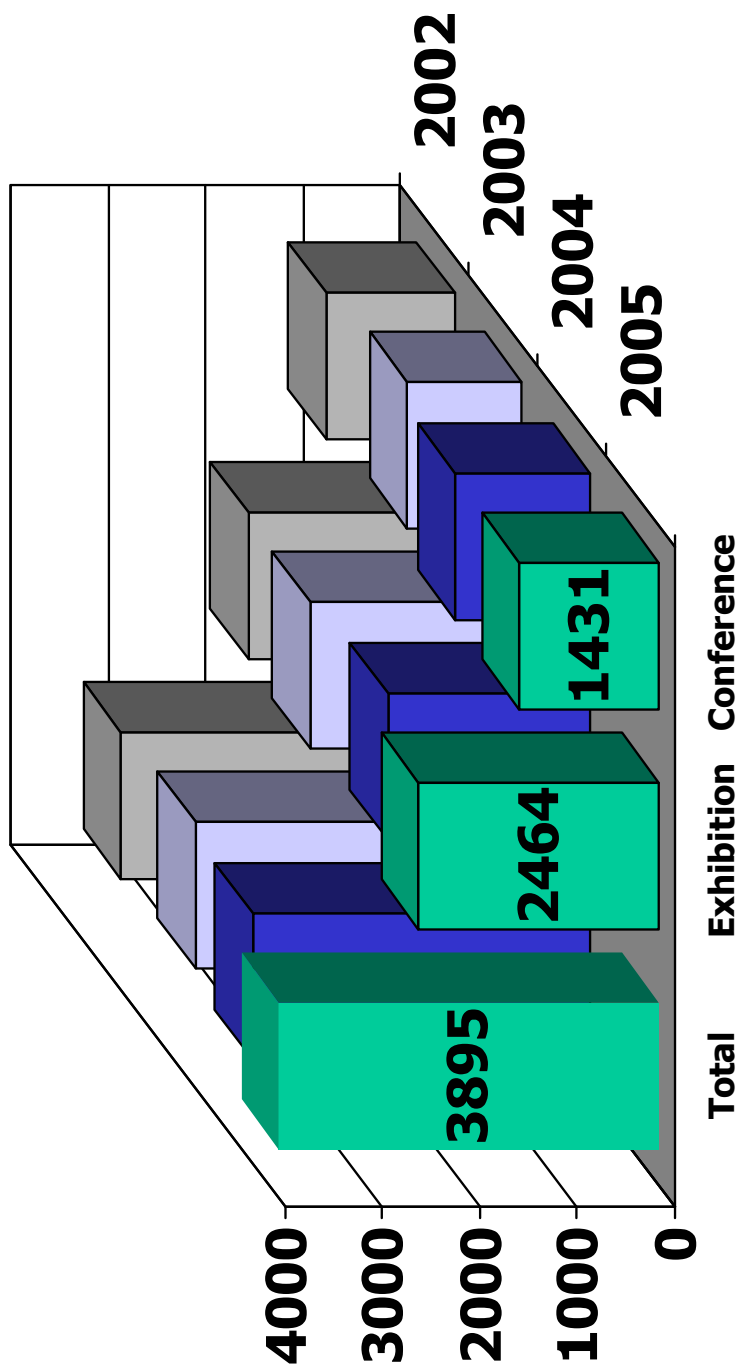
Exhibitors include Market-Leading Vendors for:

- Development Tools
 - Cadence, Synopsys, Mentor Graphics, Mathworks, Synplicity, Altium
- Embedded Processor Cores
 - ARM, Rambus, Tensilica
- New Exhibitors & Start-Ups
 - Infiniscale (Analogue Systems Modelling) (F), Silistix (On-Chip SoC Interconnect Design) (UK)
 - Lynquent (Analog/Mixed Signal Modelling) (USA), Nangate (Library Optimization Tools) (DK)
 - Menta (Audio/Video IP Libraries) (F), SimPlus Verification (Hardware Verification) (Israel)
 - Cavendish Kinetics (Embedded Memory IP) (NL) Enterpoint (FPGA & ASIC Design) (UK)



DATE in numbers

Exhibition and Conference Visitors





Conference Programme

Top 3 most popular topics for submission

- B2: 55 Simulation and Validation
- A3: 43 Design of low power systems and case studies
- B10: 43 Power estimation and optimization

Great success for

- Embedded systems design methods & architectures:
35% of the sessions!
- Test: 17% of sessions

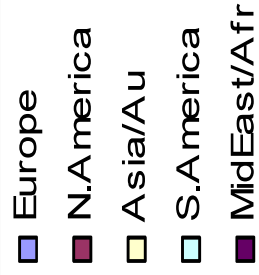


Conference Programme

Worldwide contributions to DATE

Top 5 countries

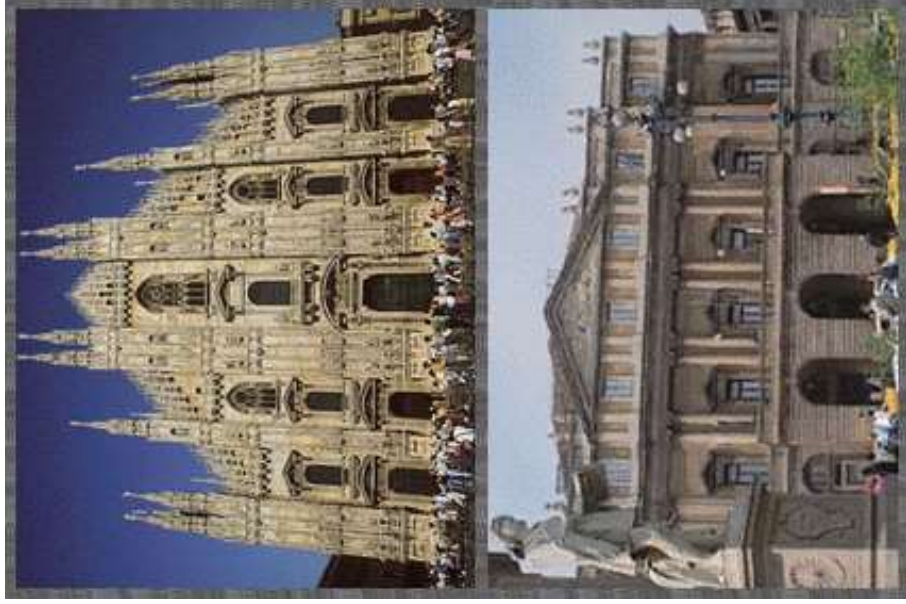
- USA: 291
- Germany: 80
- Italy: 46
- France: 41
- UK: 40





Conference Programme

- More submissions received
- Large TPC
 - TPC meeting on November 3 (Milano)
 - More than 200 people participated
- More than 5 reviews per paper
- High-quality programme!!



Conference Programme



	A	B	C	D	E	F	G	IP
MON		methodologies	Test	Designers' Forum	Embedded Software	Tools & methodologies	Special Focus	Interactive
TUE								
WED								
THU								
	A	B	C	D	E	F	G	IP
MON	09:00-10:30 11:00-12:30 14:30-16:00 16:30-18:00	Tutorials						
TUE	09:00-10:30 11:00-12:30 14:30-16:00 16:30-18:00	plenary	Executive Track					
WED	08:30-10:30 11:30-13:00 14:30-16:00 16:30-18:00	4G Telecom						
THU	08:30-10:30 11:30-13:00 15:00-16:30	Wireless Sensor Networks						
FRI	08:30-10:30 11:00-12:30 14:30-16:30	Workshops						



Special Events at DATE'06

Keynote Speakers – Tuesday, March 7th, 0900

- EDA Challenges in the Converging Application World

René Penning de Vries, SVP & CTO,
Philips Semiconductors, The Netherlands



- Sociology of Design and EDA

Wally Rhines, Chairman and Chief Executive Officer,
Mentor Graphics & Chairman, EDA Consortium, USA





Special Events at DATE'06

Executive Track – Tuesday, March 7th

Presentations by company executives (CEO, CTO, VP) including:

- **D Kish**, Vice President, **Actel**
- **E H Frank**, Vice President R&D, **Broadcom**
- **M Prati**, Vice President, **Cisco Systems**
- **C Simson**, CTO, **Freescale**
- **A Stritter**, VP Design Automation & Test, **Infineon**
- **N Takla**, CEO, **Innovative Semiconductor**
- **J Tung**, Fellow & Chief Strategist, **MathWorks**
- **J Ready**, President & CEO, **MontaVista**
- **P Magarshack**, VP R&D, **STMicroelectronics**
- **C Rowen**, President & CEO, **Tensilica**
- **A Derpmanns**, GM, **Toshiba Electronics Europe**
- **K den Otter**, European President, **TSMC**
- + Representatives of all the leading EDA vendors
(Full session list appended)



Special Events at DATE'06

4G Telecommunications: Applications & Design

Special Focus Topic on **Wednesday, March 8th**

Keynote:

[Next Generation Architectures can dramatically reduce the 4G Deployment Cycle](#)

D. Shaver, Texas Instruments, USA

Director of Communications Systems and SoC R&D Laboratory

Invited sessions:

- Hot Topic - Cross disciplinary aspects of 4G implementations
- Hot Topic - System-level design of System-on-Chip
- Hot Topic - Architectures and Network-on-Chip
- Tutorial - Applications, Architectures, Design Methodology and Tools for MPSoC



Special Events at DATE'06

Wireless Sensor Networks

Special Focus Topic on **Thursday, March 9th**

Keynote:

[HogThrob: Towards a sensor Network Infrastructure for Sow Monitoring](#)

Prof. P. Bonnet, Copenhagen University, DK

Invited sessions:

- Hot Topic - Introduction to and applications for wireless sensor networks
- Hot Topic - Design, Verification, Deployment and Test of WSN Systems
- Panel - Compelling Challenges in WSN Research



Special Events at DATE'06

Special Sessions on Automotive System Design

- Tutorial & Panel: Communication Methods and Networking in Automotive Systems
 - A Sangiovanni-Vincentelli, UC Berkeley, US; T Weber, DaimlerChrysler, DE; A Herkersdorf, TU Munich, DE; P Degardins, Siemens VDO, DE
- Panel: Test and Reliability Challenges in Automotive Microelectronics
 - C Jung, BMW Group, DE; K Harbich, Robert Bosch, DE; S Fuchs, Credence Systems, DE; J Schwarz, DaimlerChrysler, DE; P Goehner, Stuttgart U, DE
- Tutorial: Model Based Design and Test
 - J Friedman, The MathWorks, US; M Conrad and H Doerr, DaimlerChrysler, DE; K Lamberg, dSPACE, DE; J Heighton, Xilinx, UK; Y Vanderperren and W Dehaene, KU Leuven, BE



Special Events at DATE'06

Special Sessions on Design and Design Tools

- Hot Topic: Industrially Proving SPIRIT Consortium Standards for Design Chain Integration (Designers' Forum)
 - M Indovina, Improv Systems, US; F Rémond, STMicroelectronics, FR; M Strik, Philips Semiconductors, NL
- Hot Topic: 'Network' the Next 'Big Idea' in Design? Network Paradigms in Systems, Sensors, and Silicon
 - A Sangiovanni-Vincentelli, UC Berkeley, US; J Rabaey, UC Berkeley, US; R Marculescu, Carnegie Mellon U, US
- Tutorial & Panel: Design for Manufacturability and Yield
 - M Buehler and J Koehl, IBM, DE; U Schlichtmann, TU Munich, DE; M Pronath, MunEDA GmbH, DE; R Sommer, Infineon Technologies, DE
- Tutorial & Panel: Low-Power Design Tools: Are EDA vendors taking this matter seriously?
 - Tutors: E Macii, Politecnico di Torino, IT; M Pedram, South California U, IT;
 - Panellists: D Friebe, Nokia, DE; R Aitken, ARM, US; A Domic, Synopsys, US; R Zafalon, STMicroelectronics, IT



Special Events at DATE'06

System Design Records

Selected designs on SoC, FPGA or reconfigurable platform, that achieve a specific **record** compared to state of the art. Paper selection has resulted in 2 sessions.
Tuesday, March 7th after the opening session.

- **Chip Design Records**

- **TWO-PHASE RESONANT CLOCKING FOR ULTRA-LOW-POWER HEARING AID APPLICATIONS**
F Carbognani, F Buergin, N Felber, H Kaeslin and W Fichtner, IIS, ETH Zurich, CH
- **A NETWORK-ON-CHIP WITH 3GBPS/WIRE SERIALIZED ON-CHIP INTERCONNECT USING ADAPTIVE CONTROL SCHEMES**
S-J Lee, K Kim, H Kim, N Cho and H-J Yoo, Korea Advanced Inst of Science (KAIST), KR CH
- **A SINGLE PHOTON AVALANCHE DIODE ARRAY FABRICATED IN DEEP-SUBMICRON CMOS TECHNOLOGY**
C Niclass, Maximilian Sergio and E Charbon, EPFL Lausanne, CH

- **System Design Records**

- **40-100GBPS TCP PROTOCOL ENGINE FOR INTERNET LAND SPEED RECORD LSR2**
H Shrikumar, Ipsil Inc, US
- **A RECONFIGURABLE HW/SW PLATFORM FOR COMPUTATION INTENSIVE HIGH-RESOLUTION REAL-TIME DIGITAL FILM APPLICATIONS**
A do Carmo Lucas, S Heithecker, R Ernst and P Rueffer, TU Braunschweig, DE
H Rueckert, W Huther, G Wischermann, K Gebel and R Fach, Thomson Grass Valley, DE
S Eichner and G Scheller, TU Ilmenau, DE
- **DISCLOSING THE LDPC CODE DECODER DESIGN SPACE**
T Brack, F Kienle and N Wehn, Kaiserslautern U, DE



Special Events at DATE'06

Designers' Forum - Full 2-day technical programme track

- Secure and Security Systems
- Reconfigurable Computing
- Specification and Verification
- Wireless Communication and Networking
- On-Chip Communication Networks
- Automotive Systems
- Media and Signal Processing

PLUS – Monday Design Tutorials (3 hours)

Four New Ways to Design a High Definition Video CODEC

Speakers' affiliations : Global UniChip; Tensilica; Stanbridge Technologies; Xilinx; CoWare

VHDL-AMS Tutorial Including Automotive and Zigbee Case Studies

Speakers' affiliations : Mentor Graphics; Infineon; Chipcon



Special Events at DATE'06

Designers' Solutions Workshops –

5 workshops on real-world practices and system design methods, presented and administered by **Doulos** in collaboration with leading vendors

- Using SystemVerilog Assertions for AXI bus verification (ARM)
- SystemC Transaction Level Modeling Standards (CoWare)
- Exploiting Processor Cores in FPGA Designs, Large and Small (Altera)
- Using the Verification Methodology Manual for SystemVerilog (Synopsys)
- Verification Methodology in a Mixed Language Environment (Mentor Graphics)

Workshops cost €50 each per delegate and include a lunch.



Special Events at DATE'06

Embedded Systems & Software –

Full 3-day technical programme track

- Processor and Memory Design
- Scheduling for Real-Time and Energy
- System Optimisation with Embedded Software
- Architectures for Predictable Real-Time Computing and Communication
- Code and Data Layout Optimisations for Embedded Software
- Resource Constrained Scheduling
- Architectural Level Synthesis

PLUS – Monday Tutorials (3 hours)

Model-Based Composition of Embedded Software and Systems

Speakers' affiliations : VERIMAG; ISIS-Vanderbilt

UML and Model-Driven Development for System-on-Chip

Speakers' affiliations : Paderborn U; KU Leuven



Special Events at DATE'06

Educational Activities -

Two full days of tutorials (Monday) and workshops (Friday)

HALF-DAY TUTORIALS – Monday, 6th March 2006

- **Organic Computing**
Speakers' affiliations :
- **Tackling Design and Circuit Marginalities during Test**
Speakers' affiliations : Massachusetts U
- **Formal Verification – Today and in the Future**
Speakers' affiliations : Bremen U; IBM
- **Sensor Networks**
Speakers' affiliations : Intel; ETH Zurich; Vanderbilt U; Princeton U
- **Scan-Based Debug and Diagnosis**
Speakers' affiliations : Mentor Graphics; Inovys

FULL-DAY TUTORIALS – Monday, 6th March 2006

- **The CELL Processor**
Speakers' affiliations : IBM
- **DFM Tools and Methodologies for 65nm and Below**
Speakers' affiliations : Blaze DFM; Cadence Design Systems; PDF Solutions; Univ. of Texas at Austin; Texas Instruments



Special Events at DATE'06

Educational Activities -

FULL-DAY WORKSHOPS – Friday, 10th March 2006

- W1 The Renaissance of FPGA-Based High-Performance Computing**
Speakers' affiliations : Xilinx, Altera, Cray Computers, SRC Computers, Celoxica, Nallatech,
- W2 Future Interconnects and Networks on Chip**
Speakers' affiliations : EPFL Lausanne, Technion, KTH Stockholm, Princeton U, IMEC
- W3 Future Trends in Automotive Electronics and Tool Integration**
Speakers' affiliations : DaimlerChrysler, Siemens VDO, Altera, TU Munich, University of York
- W4 Design Issues in Distributed, Communication-Centric Systems**
Speakers' affiliations : VERIMAG, STMicroelectronics, Twente U, TU Denmark, TU Braunschweig
- W5 Emerging CAD Challenges for Biochip Design**
Speakers' affiliations : GE Global Research, Advanced Liquid Logic, Coventor, Fraunhofer IZM



Free Events at DATE'06

Exhibition Theatre – Focus on Business and Industry

Tuesday, 7th March – **DESIGN METHODOLOGY DAY**

- High-Performance, Cost-effective Design at sub-90nm

Panellists from: **Toppan Photomask, Cadence, UMC & Philips**

Each day brings with it the announcement of a sub-90nm process breakthrough, but is this new geometry really living up to the hype and how can semiconductor designers extract all promised benefits.

- Navigating Through 3D Design Space

Panellists from: **LSI Logic, STMicroelectronics, Ericsson, Philips Semiconductors & CriticalBlue**

The panellists will discuss and offer up examples of how to make SoC architecture trade-offs between power consumption and software execution rates; between programmability and performance; between hardware optimization and time to market. Panellists will also debate industry best practices in making these trade-offs and what methodologies and tool flows best support their decision-making.



Free Events at DATE'06

Exhibition Theatre – Focus on Business and Industry

Wednesday, 8th March - **APPLICATIONS DAY**

- FPGAs and ESL for the Path to Accelerated Computing

Panelists from: **Celoxica, Philips SASS, Toshiba Electronics & Sundance**

"Buy more servers" is the conventional wisdom to meet massive processing requirements of today's enterprise and scientific applications. But this "explosive growth" strategy of server acquisition, installation and operation is coming undone because of power, performance, real estate and other costs. Designing outside of conventional EDA environments with ESL design and programming techniques is critical to overcoming the entropy of the IC design "conventional wisdom."

- The Fast Track for Fabless: Getting From Concept to Global Volume

Panelists from: **Synopsys, Micronas, Atlas Venture, Frontier Silicon & UMC**

Today's challenging market conditions require a small fabless company to go from concept to global IC volume at a phenomenal rate or risk being left in the dust of the competition. A myriad of factors and decisions play a role in determining the potential for success.

- Customer Testimonials

Mixed-Signal Experiences – X-Fab, Nokia, Freescale

Using IP standards – Freescale, Texas Instruments, ARM



Free Events at DATE'06

Exhibition Theatre – Focus on Business and Industry

Thursday, 9th March – **R&D & BUSINESS DAY**

- How Innovative EDA Start-ups are Keeping Pace with Exploding Design Sizes and Ever-shrinking Process Geometries

Moderator: **Gary Smith, Senior Analyst, Gartner Dataquest**

Panellists from: **Summit Design, Jasper DA, Sigma-C, Nokia & Cisco**

This Special Session panel will examine three breakthrough EDA solutions, discussing how each “get it right the first time” solution has tackled the challenges. Early adopters of the technologies will discuss their usage experiences and needs for tomorrow.

- Global IC Development Design

Moderator: **Jim Lipman, Contributing Editor, TechOnLine and SOCcentral**

Panellists from: **ARM, Freescale, FTD Technology, Dubai Silicon Oasis & Synopsys**

This panel will discuss some of the specific challenges of designing across geographies, as well as introduce several of the approaches and business models that have proven successful. This interactive session will allow the audience to ask questions of these experts who have faced and overcome these challenges.