HARRY K. CHARLES, JR., TIMOTHY G. BOLAND, and G. DONALD WAGNER

VERY LARGE SCALE INTEGRATED CIRCUITRY

Very large scale integrated circuitry is playing a key role in the development of modern electronic systems at APL. In the Microelectronics Group, activities have been focused on creating a resource to ensure that all personnel have access to high-performance, high-reliability integrated circuits. This article describes progress in the design, acquisition, packaging, testing, and insertion of very large scale integrated circuits.

INTRODUCTION

The fabrication of integrated circuits has progressed to the point where a million transistors can be placed on a single piece of silicon about one-quarter the size of a U.S. dime. Such a "chip" or integrated circuit is shown in Fig. 1. Chips possessing that level of complexity are generally classified as very large scale integrated (VLSI) circuits.

VLSI chips are being produced by major semiconductor manufacturers primarily for the computer, automobile, and home entertainment markets. Typical chips in production include 32-bit microprocessors and large, 256-kilobit (and even 1-megabit) random access memories.

With most manufacturers of semiconductor devices directing their products toward the mass markets, the military, which by integrated circuit industry standards uses very few chips, found itself without sources of VLSI circuitry to meet its stringent future performance needs. The military requires fast chips (up to 10^{14} gate-hertz per square centimeter[1]) that are extremely reliable and can survive the rigors of a broad spectrum of applications environments. To create and acquire suitable high-performance VLSI-like integrated circuits, the Department of Defense established[2] in 1978 its own VLSI program, called the Very High Speed Integrated Circuit (VHSIC) Program. Both commercial VLSI manufacturers and the VHSIC program are now producing individual devices, circuits, and families of multiple chips suitable for use in future military systems.

It is quite clear that high-performance systems must contain the latest, fastest, and most flexible VLSI/VHSIC chips available. APL, in its role as a prime developer of advanced prototype electronic systems for use in space, under water, in avionics, and for Fleet defense, needs access to these VLSI/VHSIC devices. Consequently, several years ago, APL created a VLSI task team.[3] Based on the team's findings and the growing impact of VLSI worldwide, VLSI was made both an important part of Independent Research and Development efforts and a focused development activity in the Microelectronics Group.

It is the mission of the VLSI effort to ensure access to high-performance, high-reliability integrated circuits.

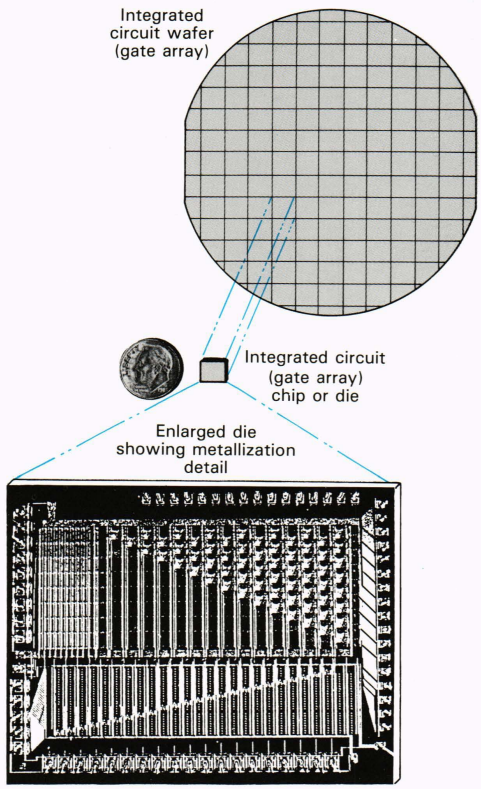

Figure 1—Integrated circuit chip.

Progress has been made in several areas, including design, acquisition (fabrication), packaging, testing, and system insertion. The interrelation of these activities in the development sequence for an application-specific integrated circuit (ASIC) is shown in Fig. 2. The colored lines represent optional hand-off points between in-house development and outside vendor development or ser-

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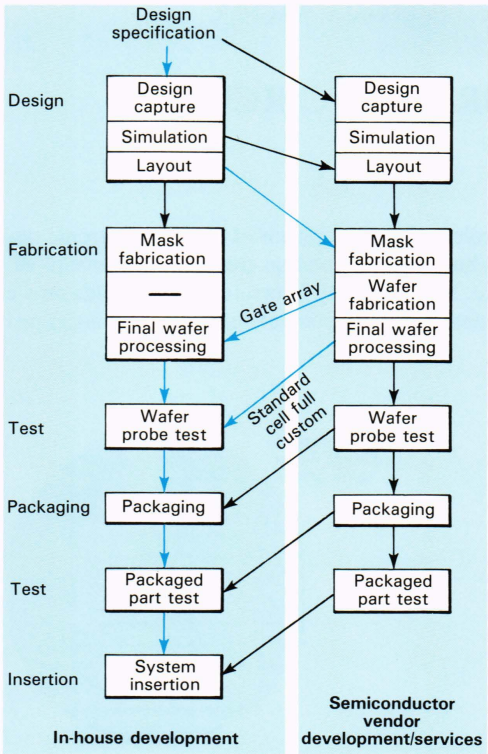

Figure 2—Flow diagram for the development of an ASIC.

vices. The chip development and insertion process involves not only the expenditure of significant resources, but also the need to make several decisions concerning internal versus external activities, especially in the area of acquisition.

ASICs are available in several different forms, including full-custom, standard cell, gate-array, and linear array circuits. The principal difference among the forms is the degree of customization of the layout of transistors that implement the desired circuit. The transistor layouts and interconnections for full-custom and standard cell circuits are unique. Gate arrays (digital) and linear arrays (analog) have regular arrays of prediffused transistors whose interconnection can be customized to implement different circuits simply by patterning one or two metallization levels. The patterning is performed in a manner analogous to patterning a printed wire board on a hybrid substrate[4] and thus represents a natural extension of APL's photolithographic technology.

DESIGN

APL's custom or application-specific design and development capabilities (from gate arrays to full-custom circuits) are based on the Mentor computer-aided engineering workstation, a powerful single-user system that provides a generic set of tools for all design tasks. The

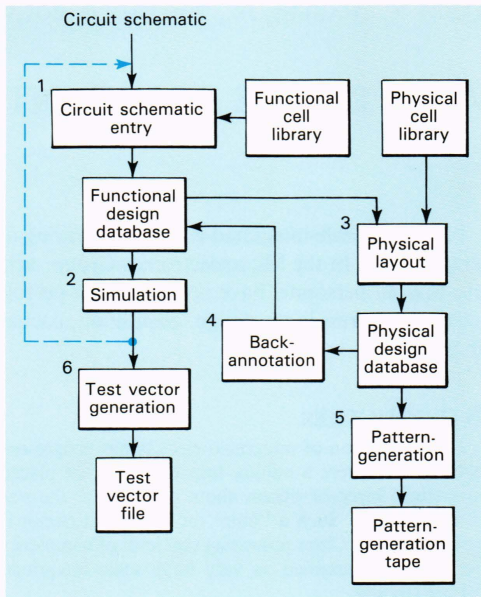

Figure 3—Flow diagram of a typical ASIC design.

Mentor software has been augmented with different library file sets specific to various vendor's ASIC structures.

Figure 3 shows a flow diagram of a typical application-specific chip design process. The process begins (step 1 in Fig. 3) with the entry of a logic schematic (circuit design at the logic-gate level) into the Mentor system using its graphical input and editing tools. The schematic may begin as a high-level functional block diagram that is successively refined until the design is drawn entirely with precharacterized logic macros or cells that include the common functions used by logic designers. The functional cell library contains symbols, behavioral models, and the performance characteristics for each cell. The library data are combined with the cell-incidence and connectivity data from the schematic to create a functional design database that serves as the input to the simulation and layout operations.

In the next step (2), behavior and performance data for all cells in the design are combined to simulate the function and timing for the entire design. Using the Mentor interactive logic simulator, test inputs are applied to the circuit model, and outputs are calculated and displayed for analysis by the designer. Internal circuit nodes can be easily "probed" during simulation by simply pointing to them in the schematic. Timing waveforms are calculated using typical values for cell propagation delays and estimates for interconnection path delays. (Accurate values for interconnection delays are calculated during the back-annotation step described below.) On the basis of simulation results, changes to the design may be required as indicated by the dashed line in Fig. 3. Design and simulation is an iterative process that continues

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until the simulation results satisfy all functional and performance specifications.

Once the design has been verified through simulation, the physical layout of the circuit consisting of two parts, cell placement and the routing of cell interconnections, can be done (step 3). The tasks are guided and constrained by design rules contained in the physical library, which also contains either a transistor interconnection pattern for each cell (for array structures) or a complete set of masking-level patterns to fabricate each cell from scratch (for standard cell and full-custom approaches).

After physical layout, accurate signal interconnection delays can be calculated from the actual path lengths recorded in the physical design database. The delay values are used to update the timing estimates in the functional design database so that a more accurate simulation can be performed. The process, called back-annotation (step 4), will help designers identify timing problems and may dictate further changes to the schematic or layout.

A pattern generation program (step 5) is used to write (on tape) the top-level metal interconnection pattern for gate arrays or the multiple mask-level patterns for standard cell or full-custom designs. The pattern tape is used by the semiconductor fabrication house or a foundry to produce the optical masks required for wafer processing. (A wafer is a thin slice of semiconductor material on which hundreds of chips are fabricated.) The final step in the design process (step 6) involves extracting test inputs from a log produced by the software simulation of the design to produce a test vector file for wafer and packaged part testing. The file can be transferred electronically to the test equipment as required.

ACQUISITION

As shown in Fig. 2, acquisition of the custom VLSI circuits can follow several routes, depending on factors such as circuit type and complexity, in-house capabilities, and cost. In most custom VLSI (full-custom and standard cell) design methodologies, fabrication cannot begin until the circuit design and layout have been completed because the size and placement of transistors on the chip are different for each design. However, gate arrays allow most of the semiconductor processing steps to proceed independently of the design process because the size and placement of transistors are fixed. Processing of a gate-array integrated circuit comprised of arrays of standard transistors or logic gates with interconnection space is partially completed by a silicon foundry. The interconnections of those transistors or gates to implement the desired circuit function are made later. The partially completed circuits are called "uncommitted gate arrays" because all the active devices (transistors and gates) have been fabricated but they have not been interconnected for a specific application. The gate-array circuits are fabricated on wafers and then stockpiled until the interconnections of transistors or gates have been defined. In order to complete the circuit or customize it, the desired pattern of interconnections is derived from a circuit design and then etched on the surface of the wafer by a photolithographic process.

The major advantages of gate arrays when compared to other custom VLSI design alternatives are faster turnaround of designs, lower cost for small quantities,[5] higher designer productivity (transistors per manhour),[6] and most mature ASIC technology.

As in all engineering, some compromises are made in order to gain these advantages. Hence, some of the limitations of gate arrays are their less-than-optimum circuit density, power consumption, and speed performance, and their greater cost for large quantities (more than 10,000 to 100,000 devices).

In 1976, APL began using gate arrays in a variety of designs. Since then, more than 10 different designs have been created, nearly all in complementary metal oxide semiconductor (CMOS) technology, but there was at least one in high-speed bipolar technology. The gate arrays have been used primarily for biomedical and space applications that require low power and small size, and the number of logic gates in these arrays has varied from 250 to 1000. Since each gate array replaces many standard integrated circuits, system reliability has been improved.

While APL's experience with developing functional gate arrays has been good, dealing with the semiconductor manufacturers for small quantities has not been as successful. Generally, APL has been restricted to working with smaller companies and has not been assured of getting the best response on service for small tasks. Other laboratories with similar goals have noted the same problems and concerns. A few, including the Lawrence Livermore Laboratory[7] and the Ft. Monmouth Army Laboratory, have developed internal capabilities for patterning their own gate arrays. It is for these reasons that APL has established an in-house gate-array development service.

The wafer processing step in fabrication, shown on the left side of Fig. 2, involves purchasing uncommitted gate-array wafers from outside suppliers. The capital investment required to produce them in-house is not justified because of our very low production requirements. However, it is reasonable to customize the wafers here because most of the facilities are already in place in the Microelectronics Laboratory for hybrid circuit development.

The selection of a gate array and a supplier was guided by several factors: anticipated circuit size and performance requirements, existing processing capabilities, existing computer-aided engineering facilities, past experience with commercial gate-array products and services, and cost. A thorough evaluation of commercially available gate-array wafers[8] led to the selection of the GA-2500 gate array from Gould Semiconductors. The array is fabricated by means of a 3-micrometer CMOS technology that offers many desirable characteristics: low power consumption, high noise immunity, high performance, and high density. The array contains over 10,000 transistors (or the equivalent of 2500 2-input NAND gates) and 84 pads for input and output signals. One level of metallization is used on the array for transistor interconnections.

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As our experience with the gate array develops, other arrays (both digital and analog) will be added to the list of those available in-house. A high-priority new array will be one that has significant radiation hardness. Another array will extend the processing capability to double-level metal (where two levels of metal are used on the array for interconnection), thus allowing uses of larger and higher performance arrays to meet future needs. Design and engineering support for the acquisition of custom chips and arrays (which do not fall into the range of the current internally available gate arrays) will be readily available from the Microelectronics Group.

PACKAGING

Packaging—the science and art of providing electrical interconnections, thermal management, mechanical support, and environmental protection for integrated circuits—it is an extremely important activity in the VLSI/VHSIC arena. High-performance integrated circuit chips must have well-designed packaging to ensure that their performance integrity will be maintained when they are inserted into the system. Poor packaging can significantly slow a high-speed chip or can prevent it from functioning. The VLSI/VHSIC era puts special demands on packaging, including low-inductance and -capacitance interconnections for high-speed operation, packaging materials having matched temperature coefficients of expansion and high thermal conductivity to handle the increased chip power densities that result from device scaling,[9] and configurations that can support input/output requirements ranging to 300 leads and beyond. Such demands cannot be satisfied by today's dominant packaging technology: the dual in-line package. Dual in-line packages are basically limited to 64 leads (on 100-mil centers down two long sides of a rectangular package structure) because of their poor input/output count-to-area ratio. Sixty-four-lead dual in-line packages are typically several inches long and 1 inch wide and weigh approximately 12 ounces in the ceramic form. Fortunately for VLSI/VHSIC, there is at least one high-density packaging option, the ceramic chip carrier, that promises to satisfy the stringent demands of the new technologies. Figure 4 compares various package input/output capabilities with major device and system input/output requirements. Chip carriers offer high-density input/output performance while providing reduced size and weight and improved electrical parameters over the dual in-line package. They are designed for surface mounting, which involves mounting the leadless (or, in some cases, leaded) components directly to the top surface of a circuit board. In contrast, the dual in-line package leads must be soldered into predrilled and plated holes; this technique is known as through-hole mounting. As shown in Fig. 4, the pin grid array is a high-density packaging alternative for through-hole mounting.

In through-hole mounting packages that have bottom leads such as pin grid arrays, the leads are soldered into plated through holes (vias) in multiple-layer printed wire boards. The holes are typically placed on 100-mil centers (100-mil grid). In addition to holding the component lead, they serve as a via for interconnection between circuit board layers. This type of mounting has several disadvantages for VLSI and VHSIC applications, including reduced board density (due to via structure), difficulty to repair (as input/output numbers increase), and increased inductance due to round wire leads. The repair or removal of this type of package can be facilitated by the use of a socket that is permanently mounted into the board. The package can then be plugged into and

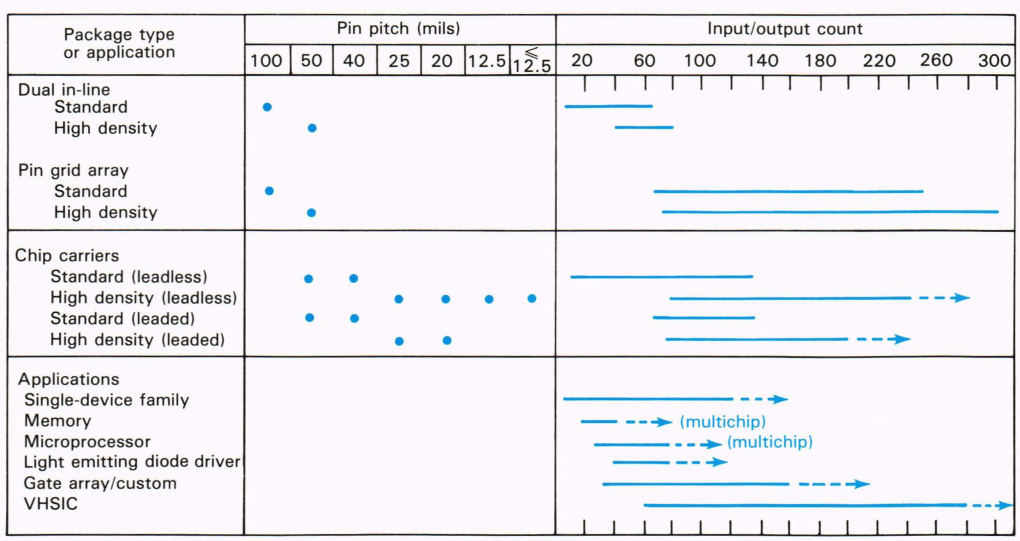

Figure 4—Package and application input/output capability and requirements.

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out of the socket. However, sockets add additional inductance and resistance to the circuit path that can degrade device performance. Mechanical integrity would also be questionable for high-reliability applications.

The Group has geared its VLSI/VHSIC packaging technology toward surface mounting with ceramic chip carriers on multilayer ceramic boards to effect the best possible temperature coefficient of expansion match. A description of the Microelectronics Laboratory's multilevel thick-film ceramic board technology is given in an article by Romenesko et al. elsewhere in this issue. To verify that the ceramic chip carrier provides a viable high-performance package for APL's custom chip first-level packaging requirements, comprehensive electrical, thermal, and mechanical modeling activities have been undertaken. The models, based on finite-element modeling techniques, have been validated by controlled experimentation and have already been used to develop design guidelines for dense circuit applications such as the digital signal processor in the Naval Remote Ocean Sensing System program. A detailed description of the methodology for thermal and thermomechanical modeling is given in an article by Clatterbaugh and Charles elsewhere in this issue. The article also presents various validation experiments that show that the ceramic chip carrier/ceramic board system can be reliable under extreme environmental conditions such as temperature cycling (−55 to +125°C) and power cycling.[10]

Finite-element modeling has been used to numerically estimate the capacitance, inductance, and characteristic impedance of signal lines in multiconductor environments typical of high-speed digital signal-processing applications that are representative of VHSIC brassboard systems. If a bipolar logic family were selected, for example, a design concern might be the characteristically low impedance (8 to 20 ohms) of a standard thick-film multilayer circuit. Low-impedance lines that connect bipolar logic forms can cause significant propagation delays for logical 1-to-0 transitions and, to a lesser extent, for logical 0-to-1 transitions with an undetermined amount of loss in noise margin. The problem worsens with increasing line length.

Finite-element modeling techniques can be used to develop design guidelines for increasing the characteristic impedance and hence for improving the performance of this bipolar logic family, especially at high frequencies. Design guidelines are focused on reducing the overall capacitance of critical signal lines, on providing adequate power supply decoupling of switching transients, and on ensuring low-impedance ground returns. A typical impedance-versus-buried-layer position curve is shown in Fig. 5.

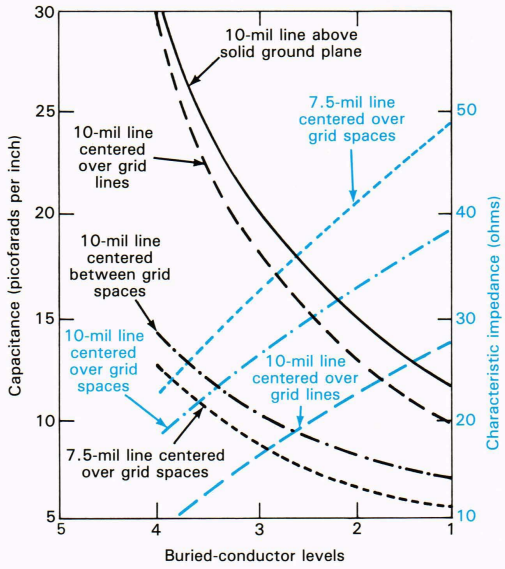

Figure 5—Calculated signal line capacitance and high-frequency (≈ 100 megahertz) impedance for a multilayer thick-film ceramic circuit board with a gridded ground plane (0.015-inch lines on 0.050-inch centers). A 0.001-inch dielectric thickness between conductor levels is assumed ($\epsilon_r \approx 10$). The level numbers indicate inverse distance from the ground plane with level 1 being the farthest removed and level 4 the closest.

TESTING

We are developing a flexible test system and procedures for the automated testing of fast, complex integrated circuits. The automated test equipment system is built around Hewlett Packard 16- and 32-bit computers driving a suite of bus-programmable test equipment. A typical equipment configuration for conducting several important parametric and functional tests is shown in Fig. 6. The equipment can handle both packaged chips, using a socketed fixture, and unpackaged chips/wafers, using a compatible probe card or precision micromanipulator probes. One especially powerful feature of this modular type of system is its flexibility. The equipment shown can easily be reconfigured or replaced with higher performance equipment to satisfy unique or new test requirements. The test system is programmed to apply a sequence of stimuli (test vectors) to the device under test, to sample the outputs, and to compare them to the design specifications. The test vectors can be extracted from the Mentor computer-aided engineering workstation after software simulation of the design, or they can be programmed directly at the test computer console.

In the VLSI/VHSIC world, device testing (and packaging) should be an integral part of the design process. Consequently, we have emphasized a design-for-testability philosophy, and we encourage all designers to include some form of on-chip testing and self-diagnosis capabilities.

Many testing operations have already been performed on VLSI/VHSIC devices, including the APL-developed APL-1A and spectrum accumulator chips,[11] VHSIC Static Random Access Memories (SRAMs), APL-developed gate arrays, and some commercial silicon and gallium arsenide parts. The system in Fig. 6 was used for most of these tests although, in a few cases, a special-purpose dedicated tester was required to provide some unique function or capability. For example, two stand-

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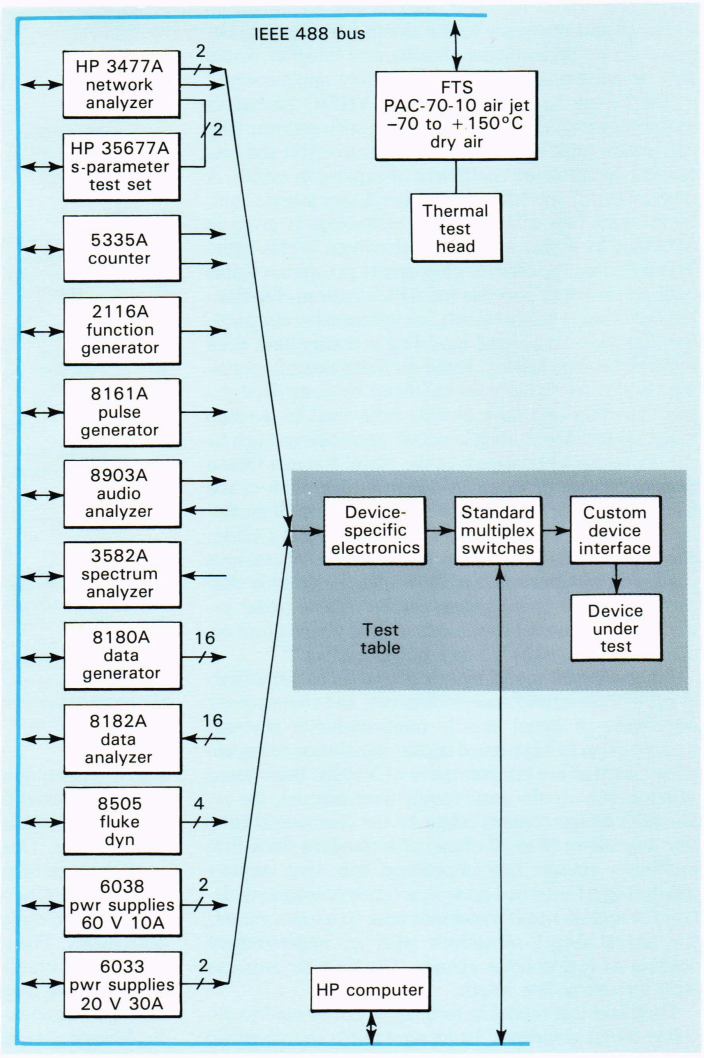

Figure 6—A configuration of the automated test equipment system.

alone dedicated testers were developed to test the VHSIC 72K SRAMs supplied by Texas Instruments. With the two, we were able to verify the high-speed performance of the SRAM, measure the nonpipeline memory timing parameters, and display a real-time bit-error map to observe the pattern sensitivity of the chip. While the Texas Instruments SRAM was specified at 25 megahertz, actual peformance at room temperature was demonstrated up to 50 megahertz (which was the limit of our tester).

A further example of VLSI testing is that recently performed on a 1000-gate CMOS array developed for the Bird-Borne Tracking System. The custom gate array was designed as part of a system that would be attached to migratory birds in order to track their flight via satellite. A test program was developed to verify and measure performance of the devices using an earlier version of the Hewlett Packard computer-based test system.

Since the effects of radiation on VLSI circuits were not well understood, special tests using the APL cobalt 60 radiation tester were performed on the bird-borne CMOS gate arrays. Using the tests developed for the Hewlett Packard system, we were able to perform functional and parametric testing of the gate-array devices promptly after subjecting them to radiation doses up to 10^5 rads. These particular devices performed adequately up to radiation levels of 5×10^4 rads although some performance degradation was clearly evident at those doses. Figure 7 illustrates how one of the crucial parameters, the operating current, increased as the radiation dose accumulated.

TECHNOLOGY INSERTION

We have been active in the introduction of custom chip technology into several programs, including towed array chain electronics, space tracking and switching applications, and VHSIC interoperability.

The towed array project involves the design of a 3500-gate CMOS array for use in the second-generation underwater data acquisition module. The gate array replaces 10 medium- and large-scale integrated circuits used in the initial design, reduces the size and power consumption of the circuit, and permits the addition of new functional capabilities. All aspects of the development of this gate array except the integrated-circuit processing were completed in-house using the facilities and methodology described in this article.

A particularly interesting interoperability project is the VHSIC Programmable Interface Adapter (VPIA). The goal of the VPIA design team is to design and simulate a preliminary interface of the Texas Instruments VHSIC bus (Mbus) to the Honeywell VHSIC bus (Lbus). To simplify the design effort, it was decided to implement an Mbus slave to the Lbus master interface. The Mbus side or slave side of the VPIA looks like a peripheral to the Mbus central processing unit. The Lbus side (the master side) looks like a central processing unit in that it can take control of the bus and generate control and address signals. This allows direct memory access read or write transfers on the Lbus side to a central processing unit or a direct memory access device on the Mbus via the VPIA. A block diagram of the currently configured VPIA is shown in Fig. 8.

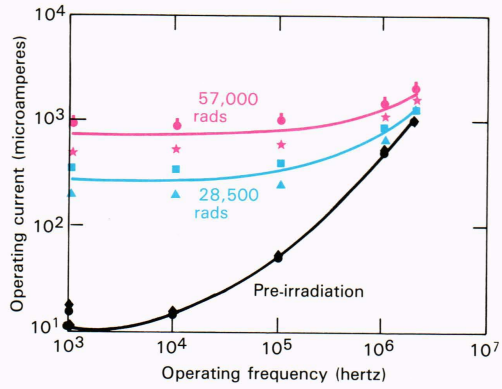

Figure 7—Operating current versus frequency during a functional test, with the radiation dose as a parameter.

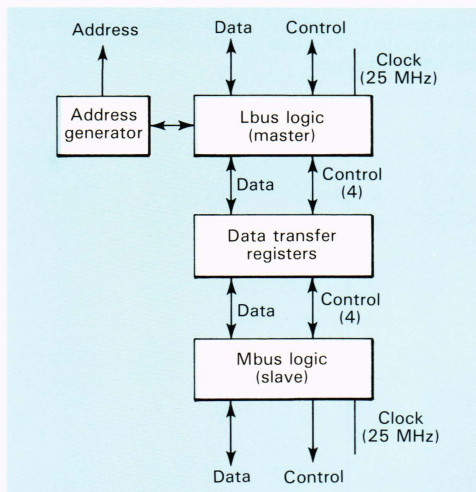

Figure 8—Block diagram of the VHSIC Programmable Interface Adapter.

REFERENCES and NOTE

[1] Chip functional throughput rate is defined as the product of the equivalent gates per chip times the maximum clock rate of a gate, f_{max}, where f_{max} is equal to $\frac{1}{4}T_d$, where T_d is the gate delay.

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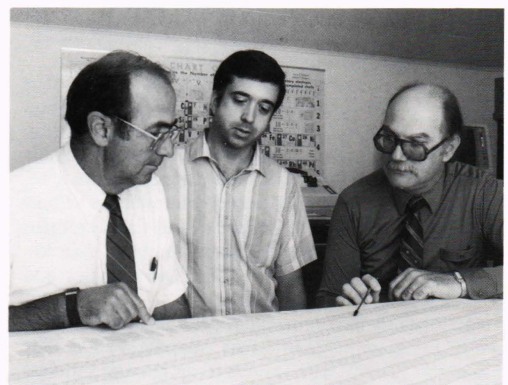

G. DONALD WAGNER's (left) biography can be found on p. 270.

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