



Kees Goossens's Publications Page

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Here is a list of my publications, in reverse chronological order. Note that the copyright on some of the files below may not be owned by me, please comply with the owner's conditions. Files are provided to allow browsing of documents, much like in a paper library. Let me know if you have problems retrieving a file.

To get started

- network-on-chip architecture and design flow
 - [Aethereal overview](#)
 - router with [both guaranteed and best-effort service](#) or with [guaranteed service only](#)
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 - [composability and predictability](#)

Composability is also known as performance virtualisation for independent development of applications. Predictability is also known as hard or firm real time.

 - [real-time memory controller](#)
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- monitoring and debug
 - monitoring and monitoring and design flows
 - communication-centric debug
- digital TV; set-top box; DVB-T
- hardwired network on chip in FPGA
- network on chip as a test access mechanism (TAM)
- network on chip as internet router switch fabric

Journal and conference papers and book chapters

1. **"Efficient multicast support in buffered crossbars using networks on chip"**
Iria Varela Senin, Lotfi Mhamdi, and Kees Goossens.
In Proc. Global Telecommunications Conference, December 2009.
[bibtex](#)
2. **"An on-chip interconnect and protocol stack for multiple communication paradigms and programming models"**
Andreas Hansson and Kees Goossens.
In Int'l Conf. on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2009.
[bibtex](#)
3. **"Dynamic Workload Peak Detection For Slack Management"**
Aleksandar Milutinovic, Kees Goossens, and Gerard Smit.
In Proc. Int'l Symposium on Systems on Chip (SoC), October 2009.
[bibtex](#)
4. **"Multi-Path Routing in Time-Division-Multiplexed**

- Networks on Chip"**
 Radu Stefan and Kees Goossens.
 In Proc. IFIP Int'l Conference on Very Large Scale Integration (VLSI-SoC), October 2009.
bibtex
5. **"Efficient Service Allocation in Hardware Using Credit-Controlled Static-Priority Arbitration"**
 Benny Akesson, Liesbeth Steffens, and Kees Goossens.
 In Proc. Embedded and Real-Time Computing Systems and Applications (RTCSA), August 2009.
bibtex
 6. **"Conservative dynamic energy management for real-time dataflow applications mapped on multiple processors"**
 Anca Molnos and Kees Goossens.
 In Proc. Euromicro Symposium on Digital System Design (DSD), August 2009.
bibtex
 7. **"Composable resource sharing based on latency-rate servers"**
 Benny Akesson, Andreas Hansson, and Kees Goossens.
 In Proc. Euromicro Symposium on Digital System Design (DSD), August 2009.
bibtex
 8. **"Internet-router buffered crossbars based on networks on chip"**
 Kees Goossens, Lotfi Mhamdi, and Iria Varela Senin.
 In Proc. Euromicro Symposium on Digital System Design (DSD), August 2009.
bibtex
 9. **"A network-on-chip monitoring infrastructure for communication-centric debug of embedded multi-processor SoCs"**
 Bart Vermeulen and Kees Goossens.
 In Proc. Int'l Symposium on VLSI Design, Automation and Test (VLSI-DAT), 2009.
bibtex
 10. **"Modeling reconfiguration**

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**in a FPGA with a
 hardwired network on
 chip"**
 Muhammad Aqeel Wahlah
 and Kees Goossens.
 In Proc. Reconfigurable
 Architecture Workshop
 (RAW), 2009.
bibtex
11. **"aelite: A Flit-
 Synchronous Network on
 Chip with Composible
 and Predictable Services"**
 Andreas Hansson, Mahesh
 Subbaraman, and Kees
 Goossens.
 In Proc. Design, Automation
 and Test in Europe
 Conference and Exhibition
 (DATE), April 2009.
bibtex
12. **"A High-Level Debug
 Environment for
 Communication-Centric
 Debug"**
 Kees Goossens, Bart
 Vermeulen, Ashkan
 Beyranvand Nejad.
 In Proc. Design, Automation
 and Test in Europe
 Conference and Exhibition
 (DATE), April 2009.
bibtex
13. **"Enabling Application-
 Level Performance
 Guarantees in Network-
 Based Systems on Chip
 by Applying Dataflow
 Analysis"**
 Andreas Hansson, Maarten
 Wiggers, Arno Moonen,
 Kees Goossens, Marco
 Bekooij.
 In IET Computers & Digital
 Techniques, 2009.
bibtex
14. **"CoMPSoC: A template for
 composable and
 predictable multi-
 processor system on
 chips"**
 Andreas Hansson, Kees
 Goossens, Marco Bekooij,
 and Jos Huisken.
 ACM Transactions on
 Design Automation of
 Electronic Systems, 2009.
bibtex DOI
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15. **"Hardwired NOC
 Infrastructure with
 Integrated Configuration
 and Functional
 Architectures"**
 Muhammad Aqeel Wahlah,
 and Kees Goossens

- and Kees Goossens.
In Proc. Annual Workshop
on Circuits, Systems and
Signal Processing (ProRisc),
November 2008.
16. **"You can catch more bugs
with transaction level
honey"**
Miron Abramovici, Neal
Stollon, Kees Goossens,
Bart Vermeulen, Jack
Greenbaum, and Adam
Donlin.
In Int'l Conf. on
Hardware/Software
Codesign and System
Synthesis (CODES+ISSS),
2008.
[bibtex](#) [DOI](#)
17. **"Performance analysis of
soft and hard single-hop
and multi-hop circuit-
switched interconnects for
FPGAs"**
Jae Young Hur, Kees
Goossens, and Lotfi
Mhamdi.
In Proc. IFIP Int'l
Conference on Very Large
Scale Integration (VLSI-
SoC), October 2008.
[bibtex](#)
18. **"Impact of power-
management granularity
on the energy-quality
trade-off for soft and hard
real-time applications."**
Aleksandar Milutinovic,
Kees Goossens, and Gerard
Smit.
In Proc. Int'l Symposium on
Systems on Chip (SoC),
October 2008.
[bibtex](#)
19. **"Real-time scheduling
using credit-controlled
static-priority arbitration"**
Benny Akesson, Liesbeth
Steffens, Eelke Strooisma,
and Kees Goossens.
In Proc. Embedded and
Real-Time Computing
Systems and Applications
(RTCSA), August 2008.
[bibtex](#)
20. **"Bandwidth Analysis for
Reusing Functional
Interconnect as Test
Access Mechanism"**
Ardy van den Berg, Pengwei
Ren, Erik Jan Marinissen,
Georgi Gaydadjiev, and
Kees Goossens.
In Proc. European Test
Symposium (ETS), May
2008.

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21. **"Analysis to Dimension Buffers for Guaranteed Performance in Networks on Chip"**
Andreas Hansson and Maarten Wiggers and Arno Moonen and Kees Goossens and Marco Bekooij.
In Proc. Int'l Symposium on Networks on Chip (NOCS), April 2008.
bibtex
 22. **"Hardwired Networks on Chip in FPGAs to unify Data and Configuration Interconnects"**
Kees Goossens, Martijn Bennebroek, Jae Young Hur, and Muhammad Aqeel Wahlah.
In Proc. Int'l Symposium on Networks on Chip (NOCS), April 2008.
bibtex
 23. **"Debugging Distributed-Shared-Memory Communication at Multiple Granularities in Networks on Chip"**
Bart Vermeulen, Kees Goossens, and Siddharth Umrani.
In Proc. Int'l Symposium on Networks on Chip (NOCS), April 2008.
bibtex
 24. **"Trade offs in the design of a router with both guaranteed and best-effort services for networks on chip"**
E. Rijpkema, K. G. W. Goossens, A. Radulescu, J. Dielissen, J. van Meerbergen, P. Wielage, and E. Waterlander.
In Rudy Lauwerijns and Jan Madsen, editors, Design Automation, and Test in Europe. The Most Influential Papers of 10 Years DATE, Circuits and Systems, Chapter 2 (Networks on Chip). Springer, January 2008.
DATE version; extended CDT journal version; bibtex
 25. **"A monitoring-aware network-on-chip design flow"**
Calin Ciordas, Andreas Hansson, Kees Goossens, and Twan Basten

- and their system.
In Journal of Systems
Architecture, 2007.
[bibtex](#) [DOI](#)
26. **"Slack exploitation for
aggressive dynamic
power reduction in SoC"**
Aleksandar Milutinovic,
Kees Goossens, and Gerard
J.M. Smit.
In Proc. Annual Workshop
on Circuits, Systems and
Signal Processing (ProRisc),
November 2007.
[bibtex](#) [poster](#)
27. **"Comparison of an
Aethereal network on chip
and traditional
interconnects - two case
studies"**
Arno Moonen, Chris Bartels,
Marco Bekooij, Rene van
den Berg, Harpreet Bhullar,
Kees Goossens, Patrick
Groeneveld, Jos Huiskens,
and Jef van Meerbergen.
In Giovanni De Micheli,
Salvador Mir, and Ricardo
Reis, editors, VLSI-SoC:
Research Trends in VLSI
and Systems on Chip,
number 249 in IFIP
International Federation for
Information Processing.
Springer, 2007.
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28. **"Predator: A predictable
SDRAM memory
controller"**
Benny Akesson, Kees
Goossens, and Markus
Ringhofer.
In Int'l Conf. on
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29. **"Channel trees: Reducing
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slots in time-multiplexed
networks on chip."**
Andreas Hansson, Martijn
Coenen, and Kees
Goossens.
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October 2007.
[bibtex](#) [DOI](#)
30. **"The Future of Computing
- Essays in Memory of
Stamatis Vassiliadis"**
Koen Bertels, Sorin
Cotofana, Georgi N.
Goudonov, Kees

- Gaydadjiev, Kees
Goossens, Said Hamdioui,
Arjan van Genderen, and
Stephan Wong, editors.
September 2007.
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31. **"Wrapper design for the
reuse of a bus, network-
on-chip, or other
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test access mechanism"**
Alexandre M. Amory, Kees
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32. **"A unified approach to
mapping and routing on a
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best-effort and guaranteed
service traffic"**
Andreas Hansson, Kees
Goossens, and Andrei
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In VLSI Design - Special
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33. **"Avoiding message-
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Andreas Hansson, Kees
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34. **"Trade-offs in the
configuration of a network
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cases"**
Andreas Hansson and Kees
Goossens.
In Proc. Int'l Symposium on
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May 2007.
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35. **"Transaction-based
communication-centric
debug"**
Kees Goossens, Bart
Vermeulen, Remco van
Steeden, and Martijn
Bennebroek.
In Proc. Intl Symposium on
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May 2007.
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36. **"Communication-centric**

SOC debug using transactions"

Bart Vermeulen, Kees Goossens, Remco van Steeden, and Martijn Bennebroek.

In Proc. European Test Symposium (ETS), May 2007.

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37. **"Test wrapper design that allows a core to be tested via a network-on-chip or other functional interconnect"**

Pengwei Ren, Alexandre M. Amory, Erik Jan Marinissen, Kees Goossens, Sandeep K. Goel, Georgi N. Gaydadjiev, Marcelo Lubaszewski, and Fernando Moraes.

In Diagnostic Services in Networks-on-Chips workshop at Design, Automation and Test in Europe Conference and Exhibition (DATE), April 2007.

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38. **"Undisrupted quality-of-service during reconfiguration of multiple applications in networks on chip"**

Andreas Hansson, Martijn Coenen, and Kees Goossens.

In Proc. Design, Automation and Test in Europe Conference and Exhibition (DATE), April 2007.

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39. **"Congestion-controlled best-effort communication for networks-on-chip"**

Jan Willem van den Brand, Calin Ciordas, Twan Basten, and Kees Goossens.

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40. **"A buffer-sizing Algorithm for Networks on Chip using TDMA and credit-based end-to-end Flow Control"**

Martijn Coenen, Srinivasan Murali, Andrei Radulescu, Kees Goossens, and Giovanni De Micheli.

In Int'l Conf. on Hardware/Software

- Codesign and System Synthesis (CODES+ISSS), October 2006.
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41. **"Transaction Monitoring in Networks on Chip: The On-Chip Run-Time Perspective"** Calin Ciordas, Kees Goossens, Twan Basten, Andrei Radulescu, Andre Boon.
 In Proc. Symposium on Industrial Embedded Systems (IES), October 2006.
[bibtex](#) [DOI](#)
42. **"Comparison of An Aethereal Network on Chip and A Traditional Interconnect for A Multi-Processor DVB-T System on Chip"**
 Chris Bartels, Jos Huisken, Kees Goossens, Patrick Groeneveld, and Jef van Meerbergen.
 In Proc. IFIP Int'l Conference on Very Large Scale Integration (VLSI-SoC), October 2006.
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43. **"A monitoring-aware NoC design flow"**
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44. **"Network and transport layers in networks on chip."**
 Israel Cidon and Kees Goossens
 In Giovanni De Micheli and Luca Benini, editors, Networks on Chips: Technology and Tools, The Morgan Kaufmann Series in Systems on Silicon, chapter 5, pages 147–202. Morgan Kaufmann, July 2006.
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45. **"Mixed adaptation and fixed-reservation QoS for improving Picture Quality and Resource Usage of Multimedia (NoC) Chips"**
 Milan Pastrnak, Peter H.N. de With, Calin Ciordas, Jef van Meerbergen, Kees

- van Meerbergen, Kees
Goossens
In Proc. Int'l Symposium on
Consumer Electronics
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[bibtex](#) [DOI](#)
46. **"Sixth International
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Kees Goossens and Laure
Petrucci, editors.
Turku, Finland, June 2006.
[bibtex](#)
47. **"Wrapper Design for the
Reuse of Networks-on-
Chip as Test Access
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Alexandre M. Amory, Kees
Goossens, Erik Jan
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48. **"NoC monitoring: Impact
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In Proc. Int'l Symposium on
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[bibtex](#) [DOI](#)
49. **"Multiple Use-Cases for A
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Flow"**
Kees Goossens
In Future Interconnects and
Network on Chip workshop
at Design, Automation and
Test in Europe Conference
and Exhibition (DATE),
March 2006.
[bibtex](#)
50. **"Synchronous Latency-
Insensitive Design in
Aethereal NoC"**
Xiao Ru, John Diehlissen,
Christer Svensson, Kees
Goossens
In Future Interconnects and
Network on Chip workshop
at Design, Automation and
Test in Europe Conference
and Exhibition (DATE),
March 2006.
[bibtex](#)
51. **"Networks on Chips for
High-End Consumer-
Electronics TV System
Architectures"**
Frits Steenhof and Harry

- Duque and Bjorn Nilsson
and Kees Goossens and
Rafael Peset Llopis
In Proc. of Design,
Automation and Test
Conference in Europe,
March 2006.
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52. **"A Methodology for
Mapping Multiple Use-
Cases on to Networks on
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Srinivasan Murali, Martijn
Coenen, Andrei Radulescu,
Kees Goossens, and
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In Proc. of Design,
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53. **"Mapping and
Configuration Methods for
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on Chips"**
Srinivasan Murali, Martijn
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in Proc. Design Automation
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Pacific (ASP-DAC), January
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54. **"An Event-based
Monitoring Service for
Networks on Chip"**
Calin Ciordas, Twan Basten,
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ACM Transactions on
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Oct 2005.
[bibtex](#)
55. **"The Aethereal network on
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architectures, and
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Kees Goossens, John
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IEEE Design and Test of
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421, Sept-Oct 2005.
[bibtex](#) [DOI](#)
56. **"A Unified Approach to
Constrained Mapping and
Routing on Network-on-
Chip Architectures"**
Andreas Hansson, Kees
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Synthesis (CODES+ISSS),
Sep 2005.
[bibtex poster DOI](#)
**Best paper award, and
most-cited CODES+ISSS
2005 article**
57. **"Networks on Chip for
Consumer Electronics"**
Kees Goossens.
In Proc. Int'l Summer School
on Advanced Computer
Architecture and
Compilation for Embedded
Systems (ACACES), Jul
2005.
[bibtex poster](#)
58. **"Formal Methods for
Networks on Chip"**
Kees Goossens.
In Proc. Int'l Conference on
Application of Concurrency
to System Design (ACSD),
Jun 2005.
[bibtex DOI](#)
59. **"Deadlock Prevention in
the AEthereal
Protocol"** (longer technical
note)
Biniam Gebremichael, [Frits
Vaandrager](#), Miaomiao
Zhang, Kees Goossens,
Edwin Rijpkema, and Andrei
Radulescu.
In Proc. Working
Conference on Correct
Hardware Design and
Verification Methods
(CHARME), Oct 2005.
[bibtex](#)
60. **"Building Predictable
Systems on Chip: An
Analysis of Guaranteed
Communication in the
AEthereal Network on
Chip"**
Om Prakash Gangwal,
Andrei Radulescu, Kees
Goossens and Santiago
Gonzalez Pestana, and
Edwin Rijpkema.
In Peter van der Stok, editor,
Dynamic and Robust
Streaming In and Between
Connected Consumer-
Electronics Devices.
Springer, 2005.
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61. **"Service-Based Design of
Systems on Chip and
Networks on Chip"**
Kees Goossens, Santiago
Gonzalez Pestana, John
Dielissen, Om Prakash
Gangwal, before

Gangwal, Jef van
Meerbergen, Andrei
Radulescu, Edwin Rijpkema,
and Paul Wielage.
In Peter van der Stok, editor,
Dynamic and Robust
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Connected Consumer-
Electronics Devices.
Springer, 2005.
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62. **"A Design Flow for
Application-Specific
Networks on Chip with
Guaranteed Performance
to Accelerate SOC Design
and Verification"**

Kees Goossens, John
Dielissen, Om Prakash
Gangwal, Santiago
Gonzalez Pestana, Andrei
Radulescu, and Edwin
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Proceedings of Design,
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63. **"An Efficient On-Chip
Network Interface Offering
Guaranteed Services,
Shared-Memory
Abstraction, and Flexible
Network Programming"**

Andrei Radulescu, John
Dielissen, Santiago
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64. **"An Event-based Network-
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Calin Ciordas, Twan Basten,
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65. **"An Efficient On-Chip
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Andrei Radulescu, John
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- Edwin Rijpkema, and Paul Wielage.
 Proceedings of Design, Automation and Test Conference in Europe, February 2004.
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66. **"Cost-Performance Trade-offs in Networks on Chip: A Simulation-Based Approach"**
 Santiago Gonzalez Pestana, Edwin Rijpkema, Andrei Radulescu, Kees Goossens, Om Prakash Gangwal.
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bibtex DOI
67. **"Interconnect and Memory Organization in SOCs for advanced Set-Top Boxes and TV --- Evolution, Analysis, and Trends"**
 Kees Goossens, Om Prakash Gangwal, Jens Roever, A. P. Niranjana.
 In Interconnect-Centric Design for Advanced SoC and NoC, Jari Nurmi, Hannu Tenhunen, Jouni Isoaho, Axel Jantsch, editors.
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68. **"Communication Services for Networks on Silicon"**
 Andrei Radulescu and Kees Goossens.
 In Domain-Specific Processors: Systems, Architectures, Modeling, and Simulation, Shuvra Bhattacharyya and Ed Deprettere and Juergen Teich, editors. Marcel Dekker, 2004.
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69. **"Concepts and Implementation of the Philips Network-on-Chip"**
 John Dielissen, Andrei Radulescu, Kees Goossens, and Edwin Rijpkema.
 IP-Based SOC Design, November, 2003.
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70. **"Bringing Communication Networks On Chip: Test and Verification Implications"**
 Bart Vermeulen and John Dielissen and Kees Goossens and Calin Ciordas.

- IEEE Communications Magazine, September, 2003.
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71. **"Trade-Offs in the Design of a Router with Both Guaranteed and Best-Effort Services for Networks on Chip"**
 E. Rijpkema and K. Goossens and A. Radulescu, J. Dielissen and van Meerbergen, J. and P. Wielage and E. Waterlander.
 IEE Proceedings: Computers and Digital Techniques, September 2003.
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72. **"Guaranteeing the quality of services in networks on chip"**
 Kees Goossens, John Dielissen, Jef van Meerbergen, Peter Poplavko, Andrei Radulescu, Edwin Rijpkema, Erwin Waterlander, and Paul Wielage.
 In Networks on Chip, Axel Jantsch and Hannu Tenhunen, editors. Kluwer, March 2003.
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73. **"Trade offs in the design of a router with both guaranteed and best-effort services for networks on chip"**
 E. Rijpkema, K. G. W. Goossens, A. Radulescu, J. Dielissen, J. van Meerbergen, P. Wielage, and E. Waterlander.
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74. **"Networks on Silicon: Blessing or Nightmare?"**
 Paul Wielage and Kees Goossens.
 In Euromicro Symposium On Digital System Design (DSD 2002), Dortmund, Germany, September 2002.
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75. **"C-HEAP: A Heterogeneous Multi-**

**processor Architecture
Template and Scalable
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Andre Nieuwland, Jeffrey
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76. **"The Cost of
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K.G.W. Goossens and O.P.
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Networks on Silicon"**

Edwin Rijpkema, Kees
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between QoS and costs"**

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- Networks on Processors
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- Nikkei Microdevices
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Investigating NoCs In
 addition to the SPIRIT
 announcement, Philips
 Research Laboratories also
 presented the results of an
 investigation into the utility
 of using network-on-chip
 (NoC) technology to
 interconnect multiple ICs.
 NoC technology is viewed
 as a replacement to the on-
 chip bus, and offers
 advantages such as the
 ability to interconnect
 multiple IP cores, and
 increased data freedom in
 handling data between IP
 cores. Compared to a bus,
 however, it also suffers
 penalties in terms of chip
 area and dissipation. Philips
 Research Labs redesigned
 an existing bus-type
 application-specific IC
 (ASIC) for TVs to use NoC
 technology, and evaluated
 the resulting disadvantages.
 The change from bus to
 NoC increased chip area by
 4.4%, and the 300MHz
 operating frequency of the
 NoC region increased
 dissipation by 10.8%. When
 the network configuration
 was changed from 2x2 to
 1x3, however, the operating
 frequency of the NoC region
 dropped to 160MHz, with an
 increase in dissipation of
 only 5.4%. The 1x3
 configuration does reduce
 the degree of network
 freedom, however.

<http://homepages.inf.ed.ac.uk/kgoossen/research.html>

02-10-2009
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According to Kees Goossens of Philips Research Labs, the investigation indicated that the penalty is sufficiently low. As a result, designer interest in NoCs is rising, and he commented that the development of the first SoCs using NoC technology would be started in 2007.

- [EETimes](#) coverage of MPSOC 2005
- [EE times](#) coverage of DATE 2005

In developing its Aethereal Network-on-Silicon (NoS), Philips decided to use a combination of circuit and packing switching, a la asynchronous transfer mode, to enable communications between IP blocks. Philips managers described NoS as "a hardware architecture with a programming model based on the OSI reference model, which allows the structuring of communication complexity from the physical implementation up to the application in a number of layers." In this way a communications-centric architecture in an SoC can be used to serve numerous specific applications, possibly leading one day to an entire application-specific SoC industry.

- August 2003 Nikkei Microdevices Aethereal coverage (in Japanese)

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