IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

NETWORK SYSTEM TECHNOLOGIES, LLC, Plaintiff, v. QUALCOMM INCORPORATED; QUALCOMM TECHNOLOGIES, INC.; ARTERIS, INC., Defendants.	)	Civil Action No. 1:22-cv-1331

DECLARATION OF DR. MARWAN HASSOUN

TABLE OF CONTENTS

I. INTRODUCTION AND QUALIFICATIONS 1

II. SCOPE OF OPINION 4

III. LEGAL PRINICIPLES 4

IV. TECHNICAL BACKGROUND 7

V. THE ASSERTED PATENTS 8

A. The '818 Patent 8

B. The '449 Patent 10

C. The '052 Patent 11

D. The '9893 Patent 12

E. The '2893 Patent 12

F. The '800 Patent 15

VI. CLAIM CONSTRUCTION OPINIONS 16

A. Common Terms 16

1. "connection" 16

B. '818 Patent Terms 23

1. "dropping means / dropping means (DM) for dropping data exchanged by said first and second module (M, S) / a first dropping means (DM) for dropping data / said dropping means (DM)" 23

C. '449 Patent Terms 26

1. "resource manager determining whether a target connection with the desired connection properties is available" 26

2. "communication manager" 32

D. '052 Patent Terms 36

1. "interconnect means" 36

E. '9893 Patent Terms 38

1. "arranging . . . the first and second information comprising said issued message as a single address" 38

F. '2893 Patent Terms 40

1. "each data package comprising N data elements" 40

2. "data package" 51

3. "data storage elements" 51

G. '800 Patent Terms 53

1. "first determination unit" / "second determination unit" 53

2. "optimal amount of data" 58

3. "optimal moment for sending the data in said first wrapper or said second wrapper 62

4. "said first wrapper" / "said second wrapper" 65

I. INTRODUCTION AND QUALIFICATIONS

1. My name is Dr. Marwan Hassoun, and I have been retained by Defendants Qualcomm Incorporated, Qualcomm Technologies, Inc., and Arteris Inc. (collectively, "Defendants") as an expert witness in the above captioned proceeding to opine on claim construction related to U.S. Patent Nos. 7,366,818 (the "'818 patent") (Ex. 2), 7,373,449 (the "'449 patent") (Ex. 3), 7,594,052 (the "'052 Patent") (Ex. 4), 7,769,893 ("'the '9893 Patent") (Ex. 5), 8,072,893 (the "'2893 Patent") (Ex. 6), and 8,086,800 (the "'800 Patent") (Ex. 7) (collectively, the "Asserted Patents").

2. My opinions provided herein are based on my years of education, research and experience, as well as my review of the materials identified below and throughout this report. I set forth my education, experience, and qualifications in my resume, attached as Appendix A to this declaration. I also provide a summary below.

3. In 1983, I earned a bachelor's degree in electrical engineering from South Dakota State University. In 1984 and 1988, I earned a master's degree and a Ph.D., respectively, in Electrical Engineering from Purdue University with specialization in software and algorithms for computer-aided design of electronic circuits.

4. I was a Professor of Electrical and Computer Engineering at Iowa State University from 1988–2000, teaching and performing research in very-large-scale integration (VLSI) integrated circuits and was a Professor-of-the-Practice in the Electrical and Computer Engineering department at Tufts University teaching integrated circuits design from 2020-2021.

5. I am a named inventor on 56 issued patents and 3 pending patent applications related to highly integrated circuits with novel functionality in the areas of multi-gigabit serial transceivers, power conversion, memories, analog-to-digital converters (ADCs), digital-to-

analog converters, RF devices, FPGAs, robotics, and digital signal processor filters. In addition, I have over 70 publications that include papers on high-speed interleaved analog-to-digital converters and digital-to-analog converters.

6. My work in industry and academia has included more than 30 years of experience in integrated circuits and systems-on-chip (SOC) design and products including hardware and software for digital and analog systems.

7. I am currently the President of Green Semiconductor, Inc. (d/b/a Intellectual Inspiration) and have over 30 years of experience in a variety of technologies relating to hardware and software for systems and devices including computers and mobile devices. I also hold a position at the Massachusetts Institute of Technology (MIT) as Director of Partnerships for the Sandbox Innovation Fund supervising and guiding startups in various areas of technology including hardware and software.

8. I have received or been nominated for several awards for my work, including the Innovation of the Year award at Xilinx, Inc.; the Distinguished Engineer Award at South Dakota State University; the Faculty of the Year award at Iowa State University; and the Warren Bost Teaching Award at Iowa State University. I also am a senior member of the Institute of Electrical and Electronics Engineers (IEEE).

9. I have held a variety of senior professional positions, including Senior Vice President of Engineering at KeyEye Communication, Inc.; Senior Director of Engineering for the Communications Technology Division at Xilinx, Inc.; President & Managing Partner in TraCHip, LLC; Co-Founder of MadMax Optics, Inc.; and Vice President of Wired Products at RocketChips, Inc. I have worked as a software engineer and a hardware engineer during my career.

10. I have been involved in building analog, digital, and mixed-signal integrated circuits products that involve communications, processor and co-processors, analog-to-digital converters, digital-to-analog converters, and serial and parallel interconnect (and their integration into large complex integrated SOCs), FPGAs, boards and multi-chip modules with multiple analog and digital subcomponents including on-chip and off-chip interconnect technologies.

11. During my tenure at RocketChips, Xilinx and KeyEye Communications, I was involved in building Integrated Circuits products that involve hardware and software for communications and processor and co-processor design and integration on large complex integrated System-on-Chips (SOCs) with multiple analog and digital subcomponents. I have been involved in all aspects of integrated circuits product lifecycle, including planning, design, licensing, verification, integration, synthesis, physical design (including layout), testing, qualification, fabrication, software, debug, fixing, revisions, ECOs (Engineering Change Orders) and customer support. My involvement included performing these tasks myself, managing large engineering groups that cover the entire spectrum of the product cycle, and outsourcing to third parties. The chips developed went into various customer products such as computers, servers, network equipment and mobile devices.

12. I have authored several chapters in several books: The Circuits and Filters Handbook, first, second and third editions, and Analog CAD Tools: Symbolic Techniques And Applications in 1995, 2003, 2009 and 1998, respectively. The chapters I authored relate to the use of software algorithms to analyze various circuits and systems used in electronic devices. In addition to the examples provided above, additional relevant information related to my education and professional experiences is provided in my Curriculum Vitae and related materials.

13. The opinions, their factual support, and the related discussion of background technology presented herein are true to the best of my knowledge and, if called to testify, I could and would testify competently as to them.

14. My analysis of the relevant materials is ongoing, and I will continue to review any new material as it is provided. This declaration represents only those opinions that I have formed to date. I reserve the right to revise, supplement, or amend my opinions below based on new information and on my continuing analysis of the materials already provided.

15. I am being compensated on a per-hour basis for my time spent working on issues in this case at an hourly rate of $650 per hour. My compensation does not depend on the outcome of this matter or the opinions I express.

16. The materials I considered in forming the opinions set forth in this declaration are identified in Appendix B. The cases for which I have provided testimony in the past four years are set forth in Appendix C.

II. SCOPE OF OPINION

17. I have been asked to provide my opinions regarding the meaning and interpretation of certain claim terms from the Asserted Patents. I understand that the parties will submit additional arguments and evidence related to claim construction. I may provide additional opinions on this topic upon my review of those materials.

III. LEGAL PRINICIPLES

18. The legal principles set forth in this declaration were provided to me by Defendants' lawyers. I understand that a purpose of claim construction is to determine the meaning and scope of patent claims asserted to be infringed. I understand that patent claims are generally given the meaning that the terms would have to a person of ordinary skill in the art

("POSITA") in question as of the earliest claimed priority date who is deemed to have read the intrinsic record.

19. For the purpose of this Declaration, I have been asked to assume the following earliest claimed priority dates for the patents in suit.

- '818 patent: October 8, 2002
- '449 Patent: October 8, 2002
- '052 Patent: March 17, 2004
- '9893 Patent: October 8, 2002
- '2893 Patent: April 21, 2005
- '800 Patent: May 18, 2004

I have therefore analyzed the claim constructions and knowledge of a POSITA for these patents as of that date or somewhat before that date. For claim terms that appear in multiple patents, my opinion set forth below applies equally for each of the priority date of the respective patents. Should there be a determination that any of the patents have a different priority date, I reserve the right to consider my opinions in view of that date.

20. I understand that claim construction is considered from the perspective of a POSITA. I understand that to determine the appropriate level of skill in the art, the following factors may be considered: (a) the types of problems encountered by those working in the field and prior art solutions thereto; (b) the sophistication of the technology in question and the rapidity with which inventions occur in the field; (c) the education level of active workers in the field; and (d) the education level of the inventor. Applying these considerations, it is my opinion that the relevant POSITA for the Accused Patents would typically have had at least either a Master's degree in Electrical Engineering, or a related field, as well as at least three years of

work experience in the field of SoC design, or a Bachelor's degree in Electrical Engineering, or related field, as well as at least five years of work experience in the field of SoC design. This POSITA would have had an understanding of SoC interconnects. They would also have a working understanding of the concepts of large-scale networks. I was at least a person of ordinary skill in this art in October 2002 (if not well before then). My opinions regarding claim construction set forth in this declaration would not change if the POSITA is found to have a slightly higher or lower level of experience and education.

21. As stated above, I understand that for claim construction a POSITA is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification, and the patent's prosecution history. When construing the claims of a patent, the principal considerations are the plain language of the claim (including the surrounding claim language and context), the patent specification and the prosecution history, which are called, collectively, the "intrinsic evidence."

22. I understand that as part of claim construction, certain claims may be found to be indefinite. I understand that a patent claim is indefinite if, when read in light of the specification and prosecution history, it fails to inform with reasonable certainty those skilled in the art about the scope of the invention.

23. I understand that claim elements may be expressed as a means for performing a recited function, and that these elements can be called "means-plus-function" claim elements. I understand that means-plus-function elements are to be construed to cover the structure, material or acts described in the patent specification for performing the recited function and equivalents thereof. I further understand that in the case of a means-plus-function claim element, the scope

of the claim element is limited to only structure that is disclosed in the patent specification and clearly linked or associated to the claimed function.

24. I understand that even if a claim element does not use the word "means," such a claim element should be treated as a means-plus-function element if a POSITA would understand that the claim element recites a function and that the words of the claim do not recite sufficiently definite structure for performing the claimed function.

25. I understand that if a claim element is found to be a means-plus-function claim element, there is a two part analysis that involves: (1) identifying the function and (2) identifying the corresponding structure from the specification that performs the function.

26. I further understand that a structure in the specification can qualify as "corresponding structure" only if the specification clearly links or associates that structure to the function specified in the claim. I understand that if a corresponding structure for a means-plus-function element cannot be identified in the specification, then the claim is indefinite. I understand that the knowledge of a POSITA cannot be used to create a disclosed structure for a means-plus-function element when the patent specification does not otherwise provide a sufficiently definite disclosure of corresponding structure that is clearly linked to performing the claimed function.

IV. TECHNICAL BACKGROUND

27. Historically, electronic systems consisted largely of discrete components scattered across printed circuit boards, which limited miniaturization and posed challenges for performance and power efficiency. However, SoC technology, which gained prominence in the late 20th century, integrates multiple functions, including processing cores, memory, peripherals,

and specialized hardware (sometimes called "modules"), onto as few as a single semiconductor chip. Modern electronic equipment almost all use SoCs.

28. These modules need to communicate with each other. Before the earliest priority date of the patents-in-suit, these communications were implemented in a variety of ways which were tailored to meet specific design requirements and constraints. Examples of known communication techniques included point-to-point wires, busses, crossbars, switches, routers, communication fabrics, and network-on-chips (NoCs).

29. One type of communication technique that was known before the priority date of the Asserted Patents were NoCs. NoCs used the concepts from large scale networks and applied them to embedded SoCs. NoCs were perceived as valuable due to their potential to efficiently address the escalating complexity of integrated circuits and SoC designs. As electronic devices became more intricate, traditional bus-based communication techniques struggled to scale, leading to performance bottlenecks and increased power consumption. By using the concepts from large scale networks, NoCs were able to offer scalability, improved performance, reduced latency, and more power efficiency.

V. THE ASSERTED PATENTS

30. The Asserted Patents relate to specific implementations of NoCs. The Background of the patents explain that NoCs were known. Therefore, the inventors do not claim that they invented NoCs. Instead, the patents suggest that the inventions were particular NoC implementations.

A. The '818 Patent

31. The '818 Patent is entitled "Integrated Circuit Comprising a Plurality of Processing Modules and a Network and Method for Exchanging Data Using Same." It discloses

an integrated circuit comprising a plurality of processing modules and a network arranged for providing at least one connection between a first and at least one second module in a "system-on-chip" ("SoC"). *See* '818 Patent at Abstract. Figure 2 illustrates an SoC according to one of the embodiments disclosed in the '818 patent:

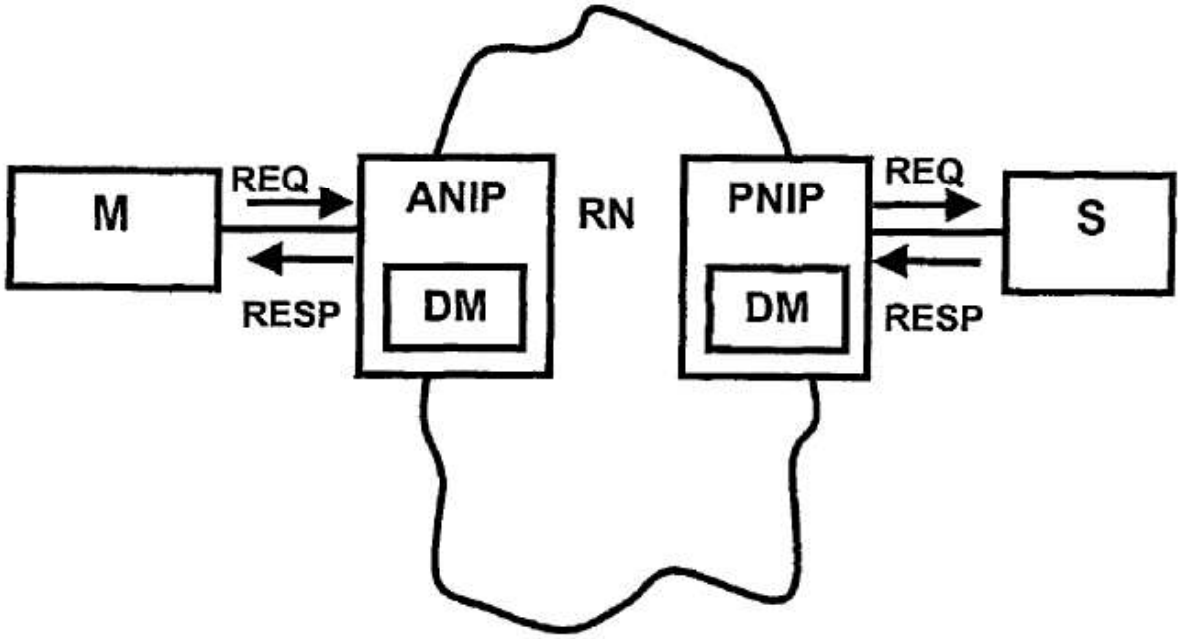


FIG.2

'818 Patent at Fig. 2.

32. Figure 2 discloses a master module (M) and slave module (S), each connected to the router network (RN) through a network interface (ANIP or PNIP). Each of the network interfaces includes a "dropping manager (DM)." According to the '818 Patent, "[t]hese dropping managers DM are responsible for the dropping of data or massages [*sic*], i.e. only the network interfaces are able to drop data or messages." *Id.* at 7:48-51. The patent further explains that "[t]he dropping manager DM may drop data in case of buffer overflow, *id.* at 8:38-39, wherein

either (a) the oldest message is dropped (milk policy), or (b) the newest message is dropped wine policy)," *id.* at 7:54-56.

B. The '449 Patent

33. The '449 Patent is entitled "Apparatus and Method for Communicating in an Integrated Circuit." The patent discloses an integrated circuit comprising a plurality of processing modules and a network arranged for providing at least one connection between a first and at least one second module. *See* '449 Patent at Abstract. Figure 3 shows one embodiment according to the '449 Patent:

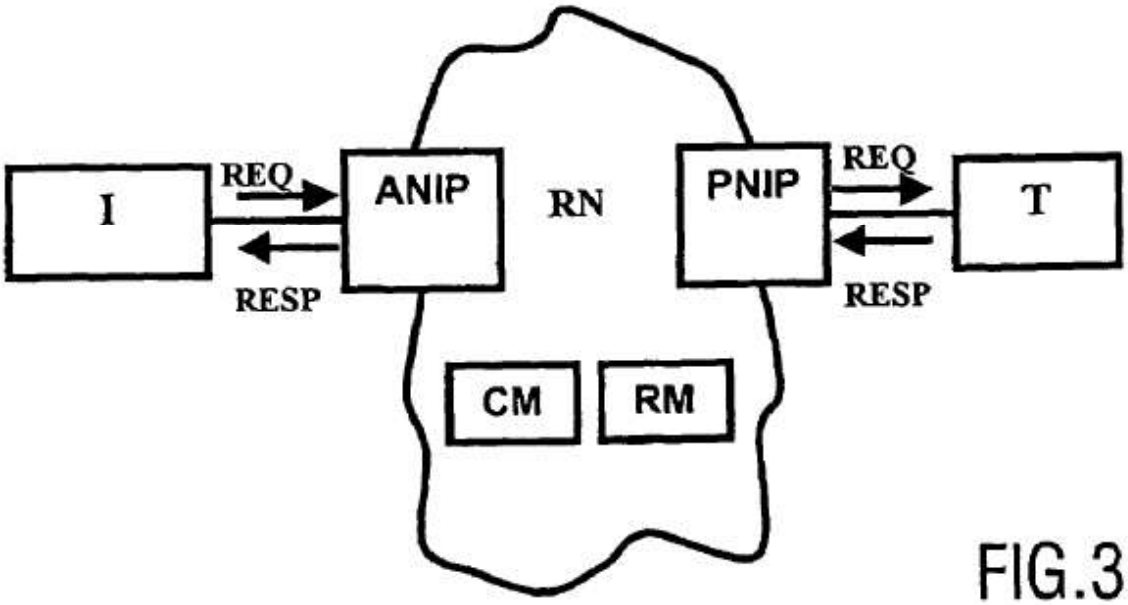


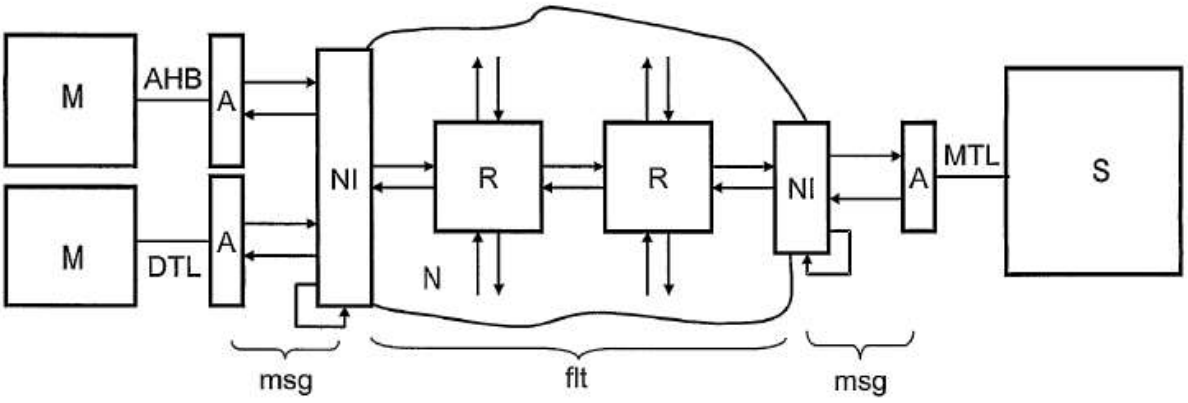
FIG.3

34. Figure 3 discloses an initiator module (I) and target module (T), each connected to a router network (RN) through a network interface (ANIP or PNIP). Included within the router network (RN) are a communication manager (CM) and a resource manager (RM). The patent further explains that "[t]he communication manager CM request [sic] a connection with a set of properties between two modules from the resource manager RM, after receiving the request REQ from the active network interface ports ANIP." *Id.* at 10:19–22. Then, "[t]he resource manager

RM allocates the necessary resources and enquires if such a connection based on these resources is possible." *Id.* At 10:24–26. "After enquiring of the available connection properties, the resource manager RM reserves the available connection i.e. the required resources, and responds to the communication manager CM which connection is available," after which the connection manager can accept or refuse the connection. *Id.* at 10:41–61.

C. The '052 Patent

35. The '052 patent is entitled "Integrated Circuit and Method of Communication Service Mapping". The patent describes an integrated circuit including multiple processing modules coupled by an interconnect means that provides "a connection-based communication having a set of connection properties." '052 patent at Abstract. It describes that "a mapping means (A) is provided for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties". *Id.* Figure 1 depicts a basic block diagram of a network on chip according to an embodiment of the alleged invention, which resides within a SoC.

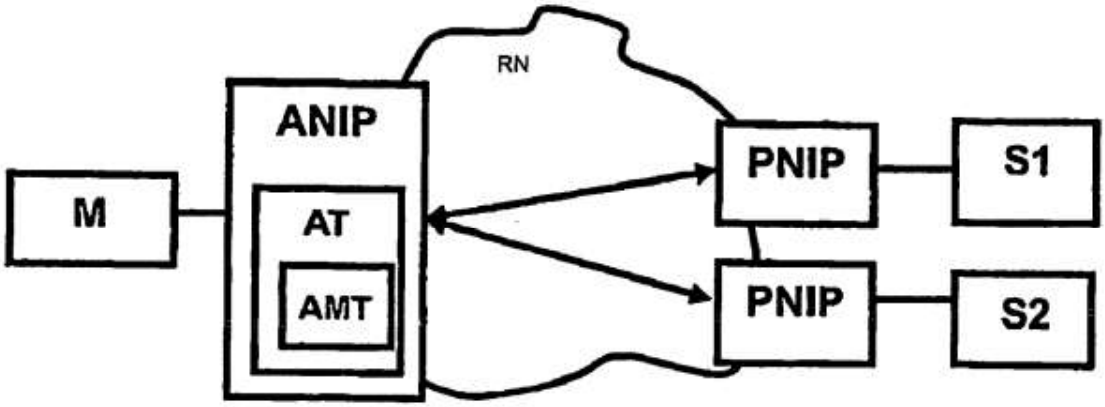


36. Figure 1 discloses master modules (M) and a slave module (S), each connected to a network (N) of routers (R) through an adapter unit (A) and network interface (NI). The '052 patent explains that "the network interfaces NI are provided to manage the communication

between the respective modules M, S and the network N, so that the modules can perform their dedicated operation without having to deal with the communication with the network or other modules." '052 patent at 5:6-23.

D. The '9893 Patent

37. The '9893 patent is entitled "Integrated Circuit and Method for Establishing Transactions." Figure 3 of the '9893 patent shows a system on a chip according to an embodiment of the alleged invention.



38. Figure 3 shows a master module M, two slave modules S1, S2, a router network RN, and three network interfaces ANIP, PNIP between the modules and the router network RN. Within the ANIP, Figure 3 shows "an address translation manager AT having an address mapping table AMT, wherein the address translation manager AT performs the decoding of address of the target slave based on information stored in an address mapping table AMT." '9893 patent at 6:14-26.

E. The '2893 Patent

39. The '2893 Patent is entitled "Integrated Circuit With Data Communication Network and IC Design Method." Figure 1 depicts an integrated circuit ("IC") designed according to an embodiment of the invention disclosed in the '2893 Patent. The IC has four

functional blocks (101-104), e.g., processing units, that are interconnected through a data communication network (100). '2893 Patent at 4:26-27. The network (100) includes data routers (110-140) that are connected to the functional blocks (101-104) via respective network interfaces (105-108). The data routers (110-140) and the network interfaces (105-108) comprise network stations of the data communication network (100). *Id.* at 4:26-33.

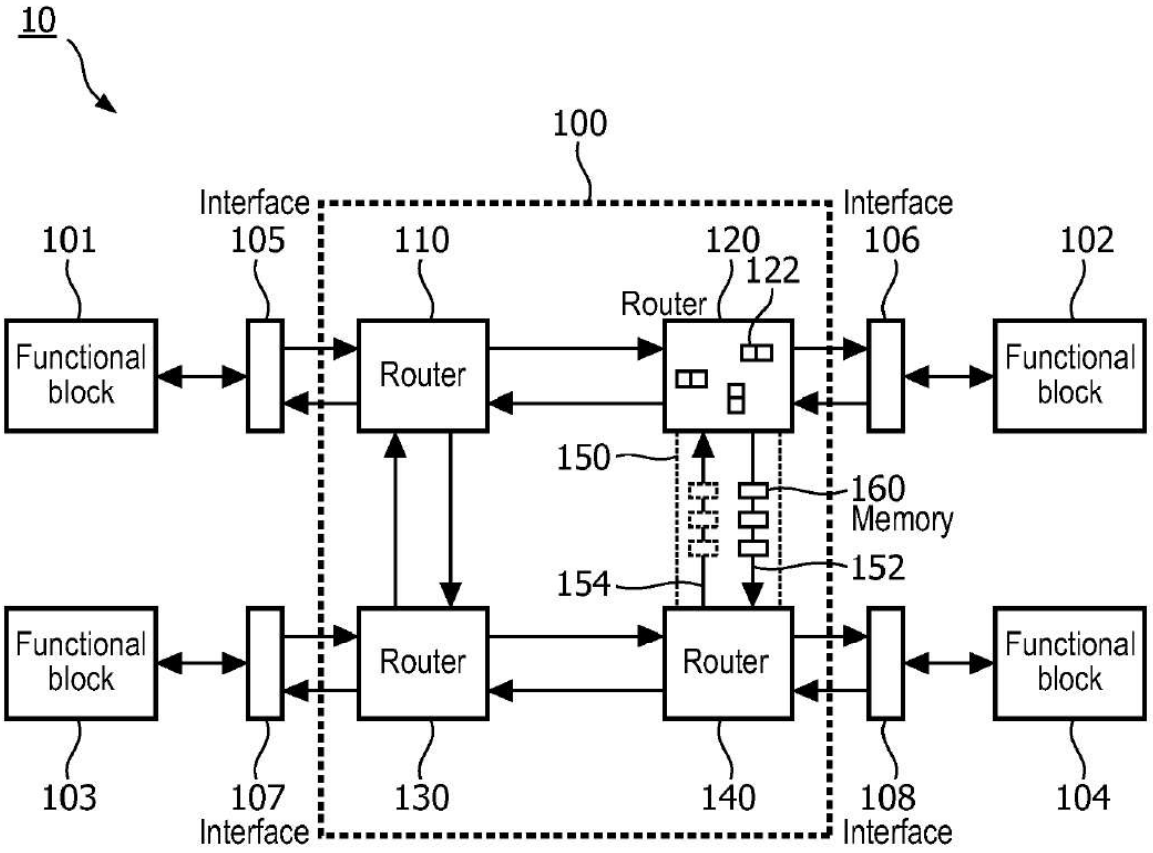


FIG. 1

Id. at Fig. 1.

40. The network stations are interconnected via a plurality of data communication channels 150. *Id.* at 4:45-47. The network stations communicate data packages between the functional blocks. *Id.* at 2:2-3; 4:51-53. The "data packages have a fixed size of N data

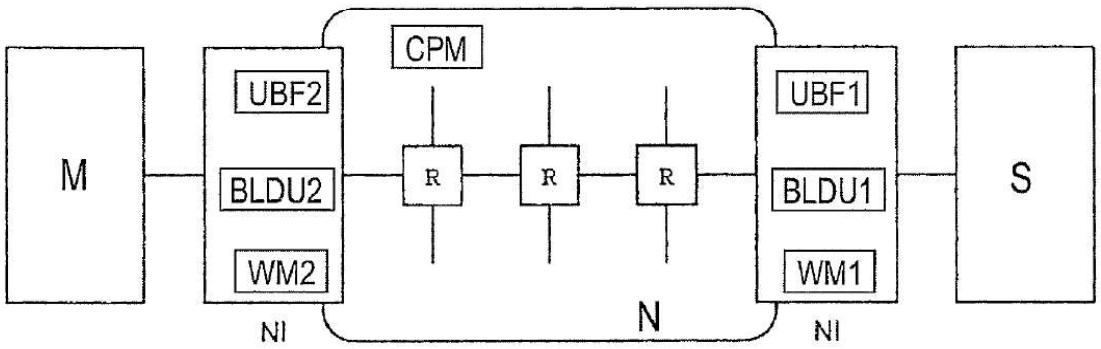
elements." *Id.* at 2:17-18. Each data package has at least one data element, typically the first data element referred to as a header, that contains routing information. *Id.* at 4:53-56. "The routing information, e.g. destination and required service type (e.g. best effort or guaranteed band width) has a fixed position in the data package, e.g. the first data element (i.e. a header), although other data elements may (also) contain such information." *Id.* at 2:22-26. The network stations are designed to expect the routing information to arrive periodically (i.e., after every N cycles). *Id.* at 2:22-28.

41. In Figure 1, the communication channel 150 between data routers 120 and 140 has been identified as the communication channel exhibiting a data transfer delay exceeding a predetermined delay threshold. *Id.* at 5:43-46. Such an identification is made at the IC design stage by subjecting the design to a simulation of the delay behavior of the IC 10 using available timing behavior simulation tools. *Id.* at 5:46-49. To avoid having to limit the clock speed, e.g., the communication speed, of the data communication network 100 based on the delay characteristics of the communication channel 150 between data routers 120 and 140 while maintaining the periodicity required by the network such that the network stations receive the routing information in an expected clock cycle, M*N data storage elements 160 are inserted in the channel 150 to introduce a delay of M*N cycles onto the communication channel.[1] *Id.* at 5:49-58; 2:15-17. The M*N data storage elements 160 cause a delay on the channel that is a multiple of the package size such that the routing information arrives at the network station during a clock cycle when the network station expects routing information while allowing for an increase in the maximum clock speed of the data network 100. *Id.* at 5:58-61; 2:15-33.

[1] N is the number of data elements within every data package, and thus the number of clock cycles it takes to communicate a complete, non-delayed package. *Id.* at 2:17-22. M is a positive integer. *Id.* at 2:12-13.

F. The '800 Patent

42. The '800 Patent is entitled "Integrated Circuit and Method for Buffering To Optimize Burst Length in Networks on Chips." The patent discloses an integrated circuit comprising a plurality of processing modules coupled by a network. *See* '800 Patent at Abstract. Figure 2 shows one embodiment according to the '800 Patent:



Id. at Fig. 2. Figure 2 discloses a master module (M) and slave module (S), each connected to a network (N) through a network interface (NI). *See id.* at 5:37-41 The network interface associated with the master module has a wrapper means (WM2) and a burst length determination unit (BLDU2). *Id.* at 6:10-14; 6:47-49. Likewise, the network interface associated with the slave module has a wrapper means (WM1) and a burst length determination unit (BLDU1). *Id.*

43. The '800 Patent mentions that though "the concept of buffering data . . . is well-known in the art of chip design," *id.* at 2:42-44, both the amount of data that needs to be buffered and the moment when the buffered data is sent over an interconnect can be "optimized." The patent teaches that the wrapper means in the network interfaces can optionally use buffers to store bursts of data before they are sent over an interconnect. *Id.* at 2:55-57. According to the '800 Patent, the burst length determination units (BLDU1 and BLDU2) may determine an

"optimal burst length for transferring data over the network N according to the current communication or connection properties." *Id.* at 6:49-53.

44. The '800 Patent teaches that this determination should be performed according to a list of connection properties, specifically: "ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery." *Id.* at 5:27-35; 6:49-53 and claims 1, 10-12. These same connection properties are repeated in the specification of the patent. *Id.* at 5:27-35 and claims 1, 10-12.

VI. CLAIM CONSTRUCTION OPINIONS

A. Common Terms

1. "connection"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"one or more channels, each having a set of connection properties, between a first module and at least one second module, that are created before use and closed after use"	"one or more communication channels"

45. In my opinion, the term "connection" has a specific meaning in the Asserted Patents, and this meaning aligns with Defendants' proposed construction. Specifically, a POSITA would understand that when the Asserted Patents refer to connections they are incorporating the concepts of "connection-oriented service" as it is used in the networking art, rather than "connectionless service."

46. The distinction between "connection-oriented service" and "connectionless service" is captured by the IEEE 100 Authoritative Dictionary of IEEE Standard Terms Seventh Edition ("IEEE Dictionary") which was published December 2000. Ex. 9 This Authoritative Dictionary includes the following definitions for "connection-oriented service" and "connectionless service".

> **Connection-Oriented Service:** A kind of delivery service where different virtual circuit configurations are used to transmit messages.
>
> * * *
>
> **Connection-less Service:** A kind of delivery service that treats each packet as a separate entity. Each packet contains all protocol layers and destination address at each intermediate node in the network. *Note:* Order of arrival of packets is not necessarily the same as order of transmission.

Ex. 9 at 220-221.

47. The distinction between connection-oriented and connectionless communication is simplistically described as analogous to the difference between communicating over a telephone versus communicating by the mail. In connection-oriented service a request for a connection is made from the master module to a slave, and no data packets are sent until the connection is confirmed and set up. Then after the data packets are sent, the connection is closed. This is analogous to a phone call in which an individual dials a phone number, and does not begin speaking unless the individual on the receiving end of the phone call picks up the phone. At the end of the phone call, the individuals hang up the phone and the connection is broken.

48. In connectionless service, on the other hand, the modules send data packets into the network without first establishing a connection with the receiving module or even checking whether the receiving module is ready or available to receive data. The network then forwards

the data packets through one or more nodes (generally a switch or router) until the packets reach their destination. This is analogous to mailing a letter, where a person puts an addressed letter in a mailbox, and the postal service then forwards the letter through one or more postal facilities until it reaches its destination. Such connectionless communication does not require the receiver to respond or establish a connection.

49. The textbook entitled "Computer Networks" by Andrew S. Tanenbaum, ©1996 ("Tanenbaum") provides a helpful description along these lines:

> **Connection-oriented service** is modeled after the telephone system. To talk to someone, you pick up the phone, dial the number, talk, and then hang up. Similarly, to use a connection-oriented network service, the service user first establishes a connection, uses the connection, and then releases the connection. The essential aspect of a connection is that it acts like a tube: the sender pushes objects (bits) in at one end, and the receiver takes them out in the same order at the other end.
>
> In contrast, **connectionless service** is modeled after the postal system. Each message (letter) carries the full destination address, and each one is routed through the system independent of all the others. Normally, when two messages are sent to the same destination, the first one sent will be the first one to arrive. However, it is possible that the first one sent can be delayed so that the second one arrives first. With a connection-oriented service this is impossible.

Ex. 8 at 23.

50. In my opinion, a POSITA would understand that the Asserted Patents were referring to the connections created in connection-oriented services. The specifications of the Asserted Patents are clear on this point. The patents explicitly refer to "connection-oriented" and "connection based" communications. '449 patent at 15:66-16:1, '9893 patent at 9:54-56, '052 patent at Abstract, 3:51-54, 8:54-58, 10:21-22. The Asserted Patents that claim connections each include the following description of "connections" that is consistent with the connections established in connection-oriented communications:

> At the transport layer of said network, the communication between the modules are performed over connections. A connection is considered as a set of channels, each having a set of connection properties, between a first module and at least one second module. For a connection between a first module and a single second module, the connection comprises two channel, namely one from the first module to the second channel, i.e. the request channel, and a second form the second to the first module, i.e. the response channel. The request channel is reserved for data and messages from the first to the second, while the response channel is reserved for data and messages from the second to the first module. However, if the connection involves one first and N second modules, 2*N channels are provided. The connection properties may include ordering (data transport in order), flow control (a remote buffer is reserved for a connection, and a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data), throughput (a lower bound on throughput is guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data), transmission termination, transaction completion, data correctness, or data delivery.

'818 Patent at 6:34-56; '449 Patent at 8:48-9:3; '052 Patent at 4:50-5:5; '9893 Patent at 4:54-5:11; '800 Patent at 5:13-35.[2]

51. The Asserted Patents also include language particularly referencing the ideas that the connections "must" be set up and closed, like a phone line.

> The connections according to the embodiments of the invention ***must be first created or established*** with the desired properties before being used. . . . ***After usage, connections are closed***, which leads to freeing the resources occupied by that connection.

'818 patent at 10:25-34; *see also* '449 patent at 10:62-11:3; '052 patent at 5:44-49; '9893 patent at 10:34-42. The patents describe this concept repeatedly. For example, the '449 patent "SUMMARY OF THE INVENTION" at 7:40-55, *emphasis added*, ("According to a further aspect of the invention, said first module M; I issues a request for *a connection* to at least one of said second modules to said communication managing means CM. Said communication

[2] There are slight differences in this paragraph between the Asserted Patents, but they are substantively the same and each of them provide this general description that is consistent with the connections established in connection-oriented services.

managing means CM forwards the request for *a connection with communication channels each having a specific set of connection properties* to said resource managing means (RM). Said resource managing means RM determines whether the requested connection based on said communication channels with said specific connection properties *is available*, and responds *the availability* of the requested connection to said communication managing means CM. A connection between the first and second module *is established* based on *the available* properties *or available network resource required to implement the properties of said communication channels of said connection*."), and 7:56-65, *emphasis added*, ("According to a still further aspect of the invention, said communication managing means CM rejects establishing a connection based on the available connection properties when *the available connection properties are not sufficient to perform the requested connection* between said first and second module. The connection properties *require that some network resources are implemented*, e.g. a throughput requires *slot reservation and flow control requires buffering*. Therefore, *a connection requiring some properties is opened or not depending on the availability* of these resources. Accordingly, the communication manager CM has some control over the minimum requirements for a connection."). Additional examples include: '449 patent at 10:55-61 ("[T]he resource manager RM sets the connection properties, and establishes a connection with accepted properties between said initiator and target modules. After said two modules I, T have performed the transactions as requested by the initiator module, the communication manager CM issues a request to said resource manager RM to reset the connection or the connection properties"), 10:19-61, 6:64-7:1 ("At connection *set up* between a master and one or more slaves, buffer space is allocated at the network interfaces of the slaves . . ."); 16:32-45 (discussing steps for opening connection); 16:58-60 ("*establishes* a connection with said properties between said two

modules"). It also discusses how a NoC can "handle a connection (i.e., *creating, closing, modifying* service)". *Id.* at 11:56-63. The other patents contain similar discussions. *See e.g.* '052 patent at 5:49-51 ("Different connections are *created and closed* independently . . ."); 6:4-6 ("Once a connection has been *created*, the master initiates the transactions by means of requests which zero or more slaves execute . . ."); 6:30-32 ("The network interfaces NI are responsible . . . for implementing the connections and services . . ."); '9893 patent at 9:56-60 ("Connections can be *configured* independently."), 10:20-23 ("Connections are introduced to describe and identify communication with different properties . . ."); '800 patent at 6:56-58 ("the optimal burst length may be determined dynamically (1) every time a connection is *set up* . . .").

52. Therefore, by incorporating aspects of connection-oriented services that are understood in the art and directly included in the specification, Defendants' proposed construction aligns with the understanding a POSITA would have of the term "connections" as it is used in the Asserted Patents. This construction is also consistent with the statements in the patents-in-suit (identified above) that state what a connection is and must do ("a set of channels each having a set of connection properties, between a first module and at least one second module" which "must be first created or established" and "after usage [] are closed").

53. In my opinion, Plaintiff's construction, on the other hand, is far too broad. Plaintiff's construction merely recites "one or more communication channels." This does not include any of the concepts related to connection-oriented services discussed above. It also appears to suggest that any communication channel is a connection. This is directly inconsistent with the specifications of the patents which, as discussed above, repeatedly describe "connections" as things that need to be opened/established/created before use and then closed

after use. It is also directly inconsistent with the specifications' explanation that connections can be used, but are not always used:

- '449 patent at 4:36-38 ("To solve this problem, recent extensions to bus protocols allow transactions to be performed on connections."), 6:63-65 ("To avoid input buffer overflow connections can be used"); 15:66-16:1 ("To fully utilize the NoC capabilities, such as high bandwidth and transaction concurrency, connection-oriented communications are provided."); 18:6-8 ("Third, the interface extends traditional bus interfaces to fully exploit the power of NoCs. For example, connection-based communication . . .").

- '052 patent at Abstract ("An interconnect means (N) is provided for coupling said plurality of processing modules (M,S) and for enabling a connection based communication . . ."); 3:51-54 ("Said plurality of processing modules are coupled by an interconnect means and enabling a connection based communication . . ."); 4:2-4; 8:54-58 ("Backward compatibility of on-chip networks is achieved . . . to use differential services as offered by a connection based interconnect . . ."); 10:21-22 (claiming "enabling a connection based communication").

- '9893 patent at 9:54-56 ("To fully utilize the NoC capabilities . . . connection-oriented communication are provided."); 10:28-34 ("Connections as defined here are similar to the concept of threads and connections from OCP and VCI. Where in OCP and VCI connections are used only to relax transaction ordering, we generalize . . .").

- '818 patent at 4:66-67 ("To avoid input buffer overflow connections can be used").

- '818 patent at 11:28-31 ("In another alternative embodiment of the invention, the transaction completion can be implemented in systems which are not connection based").

- '052 patent at 8:47-51 ("[T]he above described mapping is relevant for communication protocols which do not include the notion of connection").

See also '052 patent at 4:50-52; '800 patent at 5:13-15.

54. In conclusion, my opinion is that Defendants' construction aligns with the understanding a POSITA would have when they read the Asserted Patents, and a POSITA would understand that Plaintiff's construction is too broad.

B. '818 Patent Terms

1. "dropping means / dropping means (DM) for dropping data exchanged by said first and second module (M, S) / a first dropping means (DM) for dropping data / said dropping means (DM)"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"dropping means" subject to Section 112 ¶ 6. Function (claim 1): "dropping data exchanged by said first and second module (M, S)" Function (claim 3): claim 1 function + "creating an error message if data is dropped" Function (claim 5): claim 3 function + "sending said error message to said first module (M)" Structure: Indefinite (insufficient structure disclosed)	"dropping means" means "circuit configured to drop messages," the remaining language should be afforded their plain and ordinary meaning (not subject to Section 112 ¶ 6). If the Court holds that Section 112 ¶ 6 applies, NST proposes the following construction: Function (claim 1): "drop data exchanged by said first and second module" Function (claim 3): claim 1 function + "create an error message if data is dropped" Function (claim 5): claim 3 function + "send said error message to said first module" Structure: "circuit"

55. Claim 1 recites "dropping means" as follows (emphasis added):

- "the integrated circuit comprising at least one ***dropping means (DM)*** for dropping data exchanged by said first and second module (M, S)"
- "wherein said interface means (ANIP, PNIP) comprises a ***first dropping means*** (DM) for dropping data"

56. Claim 3 further recites (emphasis added):

- "wherein said ***dropping means (DM)*** are adapted to create an error message if data is dropped."

57. Claim 5 further recites (emphasis added):

- "wherein said ***dropping means (DM)*** are adapted to send said error message to said first module (M)"

58. In each of these three claims, the dropping means is defined solely by its functions ("dropping data exchanged by said first and second module (M, S)"; "dropping data"; "create an error message if data is dropped"; "send said error message to the said first module (M)"). There is no structure recited in these claims for performing any of recited functions for the dropping means. Therefore, claims 1, 3 and 5 are simply devoid of any structure with respect to the functions of the dropping means.

59. The specification of the '818 discloses that the dropping of data is performed by "dropping managers DM":

> "Here, it is assumed, that the network N, RN, i.e. the routers, do not drop data. The active network interface ANIP as well as the passive network interface PNIP comprise a ***dropping manager DM***, respectively. These ***dropping managers DM*** are responsible for the dropping of data or massages, i.e. only the network interfaces are able to drop data or messages." '818 patent, 7:45-51 (emphasis added).

60. The dropping managers DM are shown in Figure 2 as boxes labeled "DM" contained within the boxes labeled "ANIP" and "PNIP." However, other than the label "DM", the boxes are empty, showing no structure for the dropping managers DM.

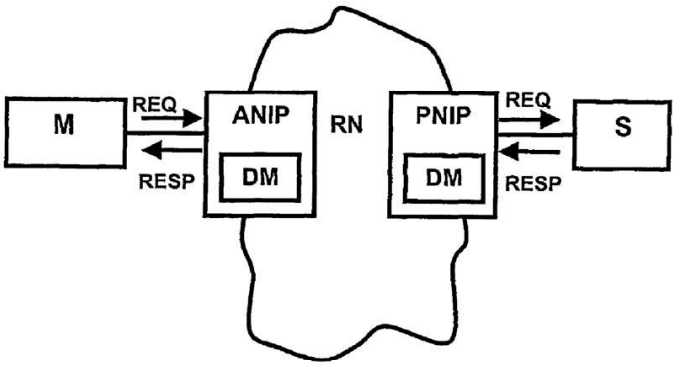


FIG.2

61. The specification fails to describe what is inside the "DM" box, let alone identify any structure that might perform the functions recited above. Instead, the specification describes the *functions* of the dropping managers, but not any structure to perform such functions.

> "Here, it is assumed, that the network N, RN, i.e. the routers, do not drop data. The active network interface ANIP as well as the passive network interface PNIP comprise a ***dropping manager DM***, respectively. These ***dropping managers DM*** are responsible for the dropping of data or massages, i.e. only the network interfaces are able to drop data or messages." '818 patent, 7:45-51 (emphasis added).
>
> The ***dropping manager DM*** may drop data in case of buffer overflow. All of CMD, OUTDATA, and RETDATA may be dropped. To guarantee transaction completion, RETSTAT is not allowed to be dropped." '818 patent, 8:38-41 (emphasis added).
>
> If the connection has no flow control, messages can be dropped by the ***dropping managers DM***, resulting also in RETSTAT-RETLOST messages. Again, combinations as those above can be made." '818 patent, 8:64-67 (emphasis added).
>
> The master module M should always receive a response to a transaction. This is achieved by the ***dropping managers DM***. If the ***dropping manager DM*** in the passive network interface ports PNIP drops data or messages possibly because of a buffer overflow, it always returns a FAIL/ERROR message to the ANIP. This return status (RETSTAT) message will never be dropped by the dropping manager of the active network interface ports ANIP because the ANIP that initiated the transaction will reserve space for return messages of every transaction that it initiates." '818 patent, 9:1-10 (emphasis added).

These passages are devoid of disclosing the required structure for the dropping managers DM.

62. A "dropping means" or "dropping manager" are not terms of art. Nor do they connote a structure known to a POSITA. Plaintiff's proposed construction for dropping means is "circuit configured to drop messages," or if the Court holds that Section 112 ¶ 6 applies, then the disclosed structure is "circuit." However, there is no specific, known, type of circuitry that is referred to as a "dropping means" or "dropping manager" and there is no circuit disclosed anywhere in the specification for the dropping managers, dropping means, or otherwise that

performs the dropping data function. A POSITA would understand that the patent is not directed to a circuit level of abstraction and provides no circuit level details or implementation (for example, I performed a word search, and the word "circuit" does not appear anywhere in the DESCRIPTION OF THE PREFERRED EMBODIMENTS section of the specification).

63. The title of the '818 patent, and the preamble of claim 1, include "integrated circuit." However, that does not link the function of "dropping data exchanged by said first and second module (M, S)" to the circuit. The term "integrated circuit" does not convey a circuit structure for the dropping means. Integrated circuits of the type contemplated by the '818 patent are incredibly complex, which would include on the order of millions up to billions of transistors that interact with each other to perform very complex functions. There are millions of circuits that could be included on an integrated circuit and particularly designed to accomplish a given function. A general reference to "integrated circuit" by no means provides to a POSITA anything structurally other than large groups of interconnected transistors formed on, for example, a silicon substrate. More importantly, even in the context of an integrated circuit, the dropping means need not be a circuit. For example, the dropping functions can be implemented as software or firmware operated by general purpose hardware in the integrated circuit, which was a known way to configure functionality within an integrated circuit. Therefore, the dropping means is not necessarily just a circuit even in the context of an integrated circuit.

C. '449 Patent Terms

1. "resource manager determining whether a target connection with the desired connection properties is available"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"resource manager determining whether a connection between modules with desired properties is available to be opened and is not	Resource manager" means "circuit that manages network resources," and the remaining language should be afforded their plain and ordinary meanings.

an arbiter prioritizing which port of a switching device is to be utilized."[3]	

64. I understand that one relevant principle of claim construction is that if a patent applicant unequivocally and unambiguously disavows a certain meaning of a claim during prosecution, a disclaimer narrows the meaning of the claim consistent with the scope of the claim surrendered.

65. In my opinion, during prosecution of the '449 patent the applicant unequivocally and unambiguously disavowed any meaning of "resource manager determining whether a target connection with the desired connection properties is available" that would encompass an arbiter prioritizing which port of a switching device is to be utilized.

66. By way of background, the connections described in the '449 patent (and all the Asserted Patents that claim connections) go all the way through the network, i.e. from a first module to a second module.[4] Networks often employ one or more switches within the network. When two or more resources need to access a shared switch, the network needs a mechanism to decide which resource can use the switch at any given time. These networks can employ an "arbiter" that prioritizes and routes traffic through that single switching node in the network.

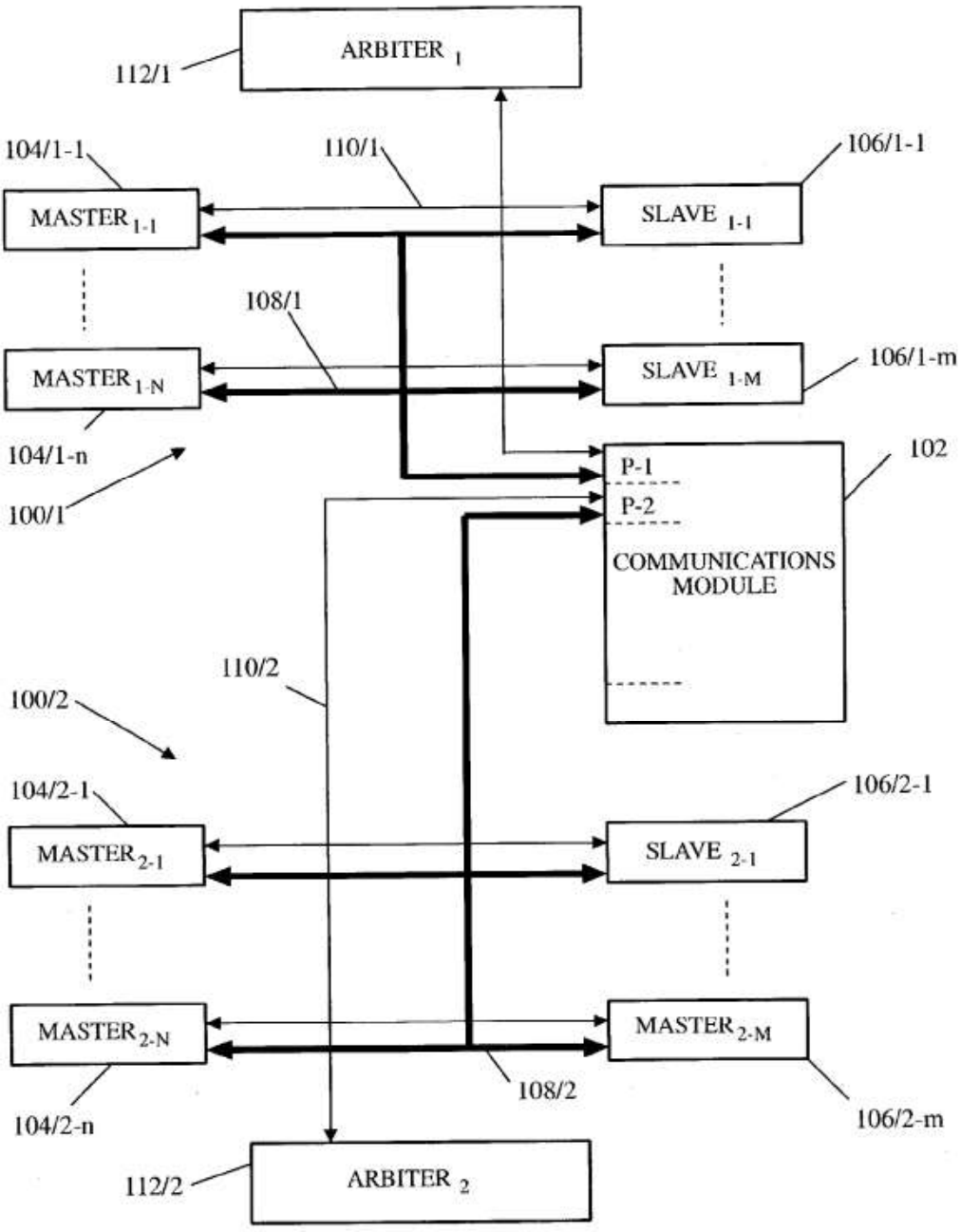
[3] Defendants contend "resource manager" is a term governed by 35 U.S.C. § 112(6) and is indefinite. However, the argument for this term largely overlaps with the "communication manager" discussion below, so Defendants agreed not to advance this argument in order to limit the disputes for the Court to resolve.

[4] *See, e.g.*, '449 patent at 8:50-52 ("A connections is considered as a set of channels, each having a set of connection properties, between a first module and at least one second module."), Abstract ("An integrated circuit comprising a plurality of processing modules (M; I; S; T) and a network (N; RN) arranged for providing at least one connection between a first and at least one second module is provided."), 7:15-18, 6:64-66 ("At connection set up between a master and one or more slaves, buffer space is allocated . . ."), 7:51-55 ("A connection between the first and second module is established based on the available properties or available network resources required to implement the properties of said communication channels of said connection.").

67. During prosecution, the claims of the '449 patent, including the claim that issued as claim 10, were rejected over a prior art reference called Emerson (Ex. 13). *See* '449 Patent Prosecution History, August 23, 2007, Office Action (Ex. 10) at 2, citing U.S Patent Pub. No. 2004/0103230 ("Emerson").

68. The Emerson reference discloses data communication modules that support data communications between subsystems in system-on-chips. Emerson (Ex. 13) at [0001]. Figure 1 of Emerson is a block diagram illustrating a system on chip that includes this communication module.

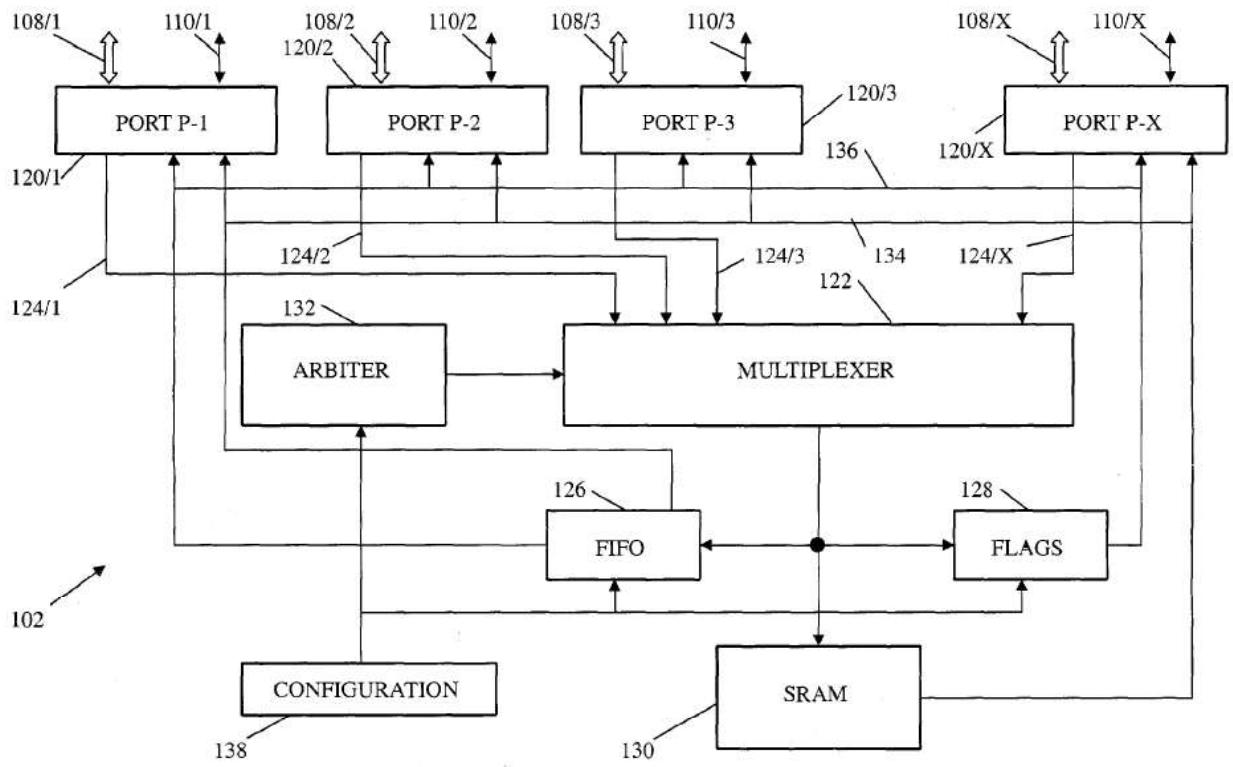
Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343



69. Figure 1 depicts a plurality of master devices that are connected to a plurality of slave devices through a bus. A data bus 108/1 connects these devices to port P-1 of a communications module 102. A control bus 110/1 connects the devices to the communications module 102 and also to an arbiter 112/1. The arbiter 112/1 decides which master or slave device controls the bus system 100/1 to transfer data. Emerson (Ex. 13) at [0018]. Additionally,

another plurality of master devices 104/2-1, 104/2-n are connected to a plurality of slave devices 106/2-1, 106/2-m through another bus 100/2. *Id.* at [0016]-[0017]. The master and slave devices are connected to the communications module 102 through a data bus 108/2. Control bus 110/2 connects the master and slave devices, communications module 102 and arbiter 112/2. The arbiter controls the transfer of data between the modules by deciding who controls the bus.

70. Figure 2 of Emerson is a block diagram of communications module 102.



71. The module has a number of input ports (shown at the top) that are connected to SRAM 130 via multiplexer 122. The configuration of multiplexer 122 determines which port is connected to SRAM. Arbiter 132 controls the configuration of the multiplexer, and therefore which port has access to SRAM. Specifically, it arbitrates between competing requests from different ports, selects which port should get access to SRAM, and configures the multiplexer to

provide the correct connection. Emerson specifies that it uses arbitration protocols based on priority. Emerson (Ex. 13) at [0026].

72. In summary, the communications module 102 of Emerson is a switching device that switches access amongst certain permutations of input and output ports. The module 102 is coupled to multiple busses and enables processors on one bus to exchange messages, share data, and signal events with processor on other busses. Emerson (Ex. 13) at [0005]. The module 102 includes a plurality of data ports, an arbiter, a multiplexer, and a FIFO, among other components that work together to selectively supply data from an input port to the appropriate output port. *See* Emerson (Ex. 13) at [0022]-[0030]; FIG. 2, 3. By including a plurality of ports and selectively supply data from one port to one or more other ports, the communication module 102 would be understood by a POSITA to be a switching device.

73. After the USPTO Examiner issued an office action rejecting the '449 patent over Emerson, the applicant responded by arguing that the "resource manager determining whether a target connection with desired connection properties is available" is different than the arbiters in Emerson.

> The Office Action asserts that Emerson has a communication manager which is a multi-core module 102 and also has a resource manager which is arbiter 112. The Arbiter 112 of Emerson is a device for prioritizing which port 120 of the module 102 is to be utilized:
>
> > [0026] If the address received at a port matches that of the module for that bus, access to multiplexer 122 and the memory space of FIFO 126 and SRAM 130 is arbitrated by arbiter 132. **Arbiter 132 arbitrates which port has use of multiplexer 122 and of the memory space at a given time. The arbitration protocol may be any protocol suitable for the system, including rotation of the priority among the ports or assigning specific ports a priority over others, or a combination of both**. It is preferred that any given arbitration

> cycle prioritizes ports 120 so that if the port with the highest priority does not have any current requests, the port with the next highest priority will be serviced. (Emerson par. 0026)(emphasis added).
>
> The Arbiter 112 of Emerson does not disclose or suggest the features of claim 1 which include the resource manager determining whether the at least one connection with the communication channels is available based on the connection properties being available and the features of claim 7 which include the first module issuing a request for a connection with the second module to a communication manager, the resource manager determining whether a target connection with the desired connection properties is available, and the resource manager responding with the availability of the target connection to the communication manager.

'449 Patent Prosecution History, Nov. 20, 2007, Applicant Remarks (Ex. 11) at 6-7 (highlighting added). It is my opinion that this statement from the applicant would unequivocally and unambiguously communicate to a POSITA that arbiters prioritizing which port is to be utilized are not "resource manager[s] determining whether a target connection with the desired connection properties is available" as claimed in the '449 patent. The response specifically identifies this arbiter in the Emerson reference, explains the arbiter function, and affirms that it does not meet the claim limitation.

2. "communication manager"

Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
Subject to Section 112 ¶ 6. Function: "receiving a request for a connection from the first module, forwarding the request to a resource manager, and receiving the availability of the target connection from the resource manager" Structure: Indefinite (insufficient structure disclosed)	"communication manager" means "circuit that manages communication between modules" (not subject to Section 112 ¶ 6) If the Court holds that Section 112 ¶ 6 applies, NST proposes the following construction: Function: "forward a request for a connection to the resource manager" Structure: "circuit"

74. Claim 10 of the '449 patent reads (emphasis added):

> 10. Method for exchanging messages in an integrated circuit comprising a plurality of modules, the messages between the modules being exchanged over connections via a network, wherein said connections comprises a set of communication channels each having a set of connection properties, any communication channel being independently configurable, wherein said connection through the network supports transactions comprising at least one of outgoing messages from the first module to the second module and return messages from the second module to the first module and further comprising the steps of:
>
> the first module issuing a request for a connection with the second module to ***a communication manager***, wherein the request comprises desired connection properties associated with the sets of communication channels;
>
> the ***communication manager*** forwarding the request to a resource manager;
>
> the resource manager determining whether a target connection with the desired connection properties is available;
>
> the resource manager responding with the availability of the target connection to ***the communication manager***; and
>
> the target connection between the first and second module being established based on the available properties of said communication channels of said connection.

75. While claim 10 recites the functions of the communication manager, it does not recite any structure for the communication manager. In the field of integrated circuits, the term "manager" at best merely identifies something that manages. Adding "communications" in front of "manger" merely limits the function, and at best merely identifies something that manages communications. "Manager" by itself, or together as "communication manager" is not a term of art that would connote any specific or known structure, and therefore a person skilled in the art would not understand "manager" or "communications manager" to identify or be associated with any specific or known structure. This is the case with "manager" or "communications manager" themselves, as well as in the context of the functions of "communication manager" recited in claim 10 as identified by the parties.

76. The specification of the '449 patent introduces "communication manager" as follows:

> "FIG. 3 shows a system on chip according to a third embodiment. The system of the third embodiment is based on the system according to the second embodiment

> and additionally comprises a ***communication manager CM*** and a resource manager RM. ***Here, the communication manager CM and the resource manager RM are arranged in the router network RN, but they can also be arranged in one or some of the network interfaces NI.***" '449 patent, 9:66-10:6 (emphasis added).

77. Fig. 3 shows "communication manager CM" simply as an empty box (other than the CM name) inside what the patent refers to as the router network RN:

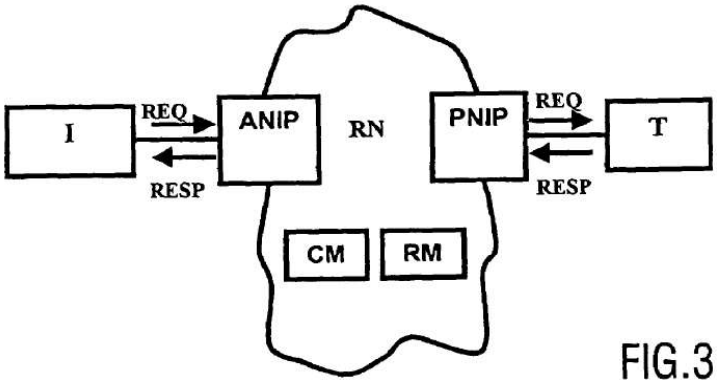


FIG.3

78. The '449 specification describes the "communication manager" only by its functions but not by any structure.

> "The ***communication manager CM*** request a connection with a set of properties between two modules from the resource manager RM, after receiving the request REQ from the active network interface ports ANIP, i.e. the properties of a connection, e.g. throughput, flow control, are to be requested when asking for a connection setup." '449 patent, 10:19-24 (emphasis added).

> "After enquiring of the available connection properties, the resource manager RM reserves the available connection i.e. the required resources, and responds to the ***communication manager CM*** which connection is available, i.e. which connection properties or the required resources thereof are available for the desired channels. Optionally, the ***communication manager CM*** can accept the connection with the available properties, but on the other hand the ***communication manager CM*** may also refuse the offered connection if the available properties or the resources thereof are not acceptable. If the ***communication manager CM*** refuses the offered connection, it sends an error message to the initiator module I (i.e. via the ANIP) and requests the resource module RM to release the reservation of said connections. Otherwise, the resource manager RM sets the connection properties, and establishes a connection with accepted properties between said initiator and target modules. After said two

> modules I, T have performed the transactions as requested by the initiator module, the ***communication manager CM*** issues a request to said resource manager RM to reset the connection or the connection properties." '449 patent, 10:41-61 (emphasis added).

79. Therefore, the '449 specification only describes the location of the communication manager, but provides no description of any structure for communication manager nor performing any of the disclosed or claimed functions of the communication manager.

80. Plaintiff's proposed construction for communication manager is "circuit that manages communication between modules," or if the Court holds that Section 112 ¶ 6 applies, then the disclosed structure is "circuit." However, there is no circuit disclosed anywhere in the specification for the communication manager, or otherwise that performs the functions of communication manager identified by the parties. A POSITA would understand that the patent is not directed to a circuit level of abstraction and provides no circuit level details or implementation (for example, I performed a word search, and the word "circuit" does not appear anywhere in the DESCRIPTION OF THE PREFERRED EMBODIMENTS section of the specification other than two general references to "integrated circuit," neither of which is associated with the communication manager ('449 patent at 16:25 and 16:53)). Moreover, a "communication manager" is not a term of art. Nor does it connote a structure known to a POSITA. There is no specific, known, type of circuitry that is referred to as a "communication manager."

81. The title of the '449 patent, and the preamble of claim 10, include "integrated circuit." However, that does not reasonably convey a circuit structure for the communications manager. As discussed above, integrated circuits of the type contemplated by the '449 patent are

incredibly complex, which would include on the order of millions up to billions of transistors that interact with each other to perform very complex functions. A general reference to "integrated circuit" by no means provides to a POSITA anything structurally other than large groups of interconnected transistors formed on, for example, a silicon substrate. More importantly, even in the context of an integrated circuit, the communication manager need not be a circuit. For example, the functions identified by the parties can be implemented as software or firmware operated by general purpose hardware in the integrated circuit, which was a known way to configure functionality within an integrated circuit. Therefore, the communication manager is not necessarily just a circuit even in the context of an integrated circuit.

D. '052 Patent Terms

1. "interconnect means"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
Subject to Section 112 ¶ 6. Function: coupling said plurality of processing modules (M, S). Structure: bus, switch, point-to-point wire, or network.	"Multi-hop interconnection between modules separated by one or more network nodes." NST disagrees that this term is governed by 35 U.S.C. 112, ¶ 6, but offers the following backup position if the Court holds that it is so governed: Function "coupling said plurality of processing modules (M, S)." Structure: "circuit"

82. Claim 6 of the '052 patent reads (emphasis added):

> 6. Method of communication service mapping in an integrated circuit, having a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S), comprising the steps of:

coupling said plurality of processing modules (M, S) by an interconnect means (N) and

enabling a connection based communication having a set of connection properties,

controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N) by at least one network interface (NI) associated to said at least one first of said processing modules,

mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.

83. Claim 6 recites no structure for "interconnect means." Rather, it only recites its function: "coupling said plurality of processing modules (M, S)."

84. The '052 patent specification identifies structures that are clearly linked to the function of coupling the plurality of processing modules:

- "In conventional processing systems the systems modules usually communicate to each other via ***a bus***. '052 patent, 1:24-26 (emphasis added).
- "A communication network forms an effective way to overcome these disadvantages. ***Networks on chip (NoC)*** have received considerable attention recently as a solution to the interconnect problem in highly-complex chips." '052 patent, 1:33-36 (emphasis added).
- "This is because, in contrast to ***existing on-chip interconnects*** (e.g., ***buses***, ***switches***, or ***point-to-point wires***), where the communicating modules are directly connected, in a ***NoC*** the modules communicate remotely via network nodes." '052 patent, '052 patent, 1:50-54 (emphasis added).
- "Introducing ***networks as on-chip interconnects*** radically changes the communication when compared to ***direct interconnects***, such as ***buses or switches***." '052 patent, 2:31-34 (emphasis added).
- "This is in contrast with the ***prevalent existing interconnects (i.e., buses)*** where modules are directly connected." '052 patent, 2:36-38 (emphasis added).
- "The ***interconnect*** is embodied as ***a network on chip NOC***, allowing communication between all aforementioned modules. The network on chip may include ***wires, bus, time-division multiplexing, switches, and/or routers within a network***." '052 patent, 4:46-50 (emphasis added).

85. The '052 specification also discloses that each module M, S is connected to network via its associated network interface NI:

- "Each module M, S is connected to a network N via its associated network interface NI, respectively, i.e. the network interfaces NI are used as interfaces

between the master and slave modules M, S and the network N." '052 Patent, 5:46-50.

86. Therefore, putting all these disclosures together, but excluding the network interface NI because it is separately claimed in claim 6, the structures broadly disclosed that are clearly linked to performing the function of "coupling said plurality of processing modules (M,S)" are: bus, switch, point-to-point wire, or network.

E. '9893 Patent Terms

1. "arranging . . . the first and second information comprising said issued message as a single address"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
Indefinite.	"Arranging … the first and second information comprised in said issued message as a single address"

87. In my opinion, a POSITA would not have a reasonable certainty about the scope of "arranging . . . the first and second information comprising said issued message as a single address." Specifically, a POSITA would have no idea what it meant to "arrange" two pieces of information "as a single address". A POSITA would not know what type of data manipulation (if any) was required for "arranging" two pieces of information into a single address. They also would not know what the boundaries of "single address" were. Moreover, the patents-in-suit do not provide any information clarifying the scope of these terms. For example, the patent does not explain whether "arranging" as a "single address" requires the first and second information to be concatenated to create a larger field (or multiple fields) in the packet, how such a new field is processed and understood to be an address, or how a system can process such a transformation. As another example, the patent does not explain whether "arranging" as a "single address" requires the first and second information to be logically or mathematically manipulated or combined (e.g. XORed, encoded) in order to maintain the appropriate size of such a "single

address" (again not addressed by the patent) and how the addressing system would use such manipulation or combination.

88. The patent uses term "arranged" in several locations, for example: "The invention relates to an integrated circuit having a plurality of processing modules and a network **arranged** for transferring messages between processing modules and a method for exchanging messages in such an integrated circuit," and "Therefore, an integrated circuit comprising a plurality of modules M, S, and a network N **arranged** for transferring messages between said modules M, S is provided," The usage of arranged here seems to mean configured, no details of how such arrangement or configuration happens.

89. Another example is: "According to an aspect of the invention, said integrated circuit comprises at least one interface means ANIP, PNIP associated to one of the modules M, S for managing the communication between said associated module M, S and the network N. Said address translation means AT is **arranged** in one of said interface means ANIP, PNIP," "According to a further aspect of the invention, said address translation means AT is **arranged** in said interface means ANIP, PNIP associated to said first module M," and "However, the address translation manager AT and/or the address mapping table AMT may also be **arranged** not in the network interface but centrally in the network N." These usages of the term seem to mean placed or positioned.

90. The above two usages of "arranged" do not add any clarity to the usage of "arrange" in the claim language, contributes to the ambiguity, and a POSITA would not understand what such arranging means in the claim.

91. As stated above, with reference to the claim element (and also in the specification) "wherein said active network interface means includes address translation means

adapted to **arrange** said first information and said second information as a single address," a PSOITA would not have a reasonable certainty about the scope of "arranging." Further to add to that uncertainty is the other usages in the specification discussed above. For example, using place or position instead of arrange here would not alleviate any uncertainty, on the contrary adds more. A POSITA would not have any clarity or explanation from the claim or specification as to what positioning or placement or configuration of first and second information as a single address means nor how to do it.

F. '2893 Patent Terms

1. "each data package comprising N data elements"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"every data package communicated by the network stations has a fixed size of N data elements"	"NST incorporates its definition for the term 'data package,' 'data elements' are groups of data, and the remaining language should be afforded their plain and ordinary meanings."

92. I understand that Defendants have construed "each data package comprising N data elements" as "every data package communicated by the network stations has a fixed size of N data elements." Based on my reading of the claim language and the specification, I agree with Defendants' construction.

93. I understand that the issue in dispute is whether the language of the claim requires that every data package communicated by the network stations has a fixed size of N data elements. Based on my reading of the claim language and the specification, it is my opinion that the language of the claim requires that every data package communicated by the network stations has a fixed size of N data elements. The invention described by the '2893 patent would not make sense otherwise.

94. The claim language supports Defendants' construction of "each data package comprising N data elements" in that every data package must be considered. Claim 10 previously refers to data packages. I have quoted the relevant portion of claim 10 below:

> a ***data communication network*** comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating ***data packages*** between functional blocks

(emphasis added). From this part of the claim, a POSITA would understand that data packages are what is communicated by the data communication network and its network stations via communications channels. A POSITA would also understand that when the claim uses the term "each data package" it is referring back to every data package communicated by the data communication network and its network stations.

95. The claim language also supports Defendants' construction that every data package has a fixed size. A POSITA would understand that when the claim says N is "an integer" ('2893 Patent at 12:49), it means that the term is an (ostensibly positive) whole number. "N" would be superfluous were it not a fixed value because if data packages have variable size (e.g., some packages having "N" data elements, some sized "N+1" data elements or "N+2" data elements), the limitation "each data package comprising N data elements" would effectively be read out of the claim.

96. Defendants' construction is also supported by the specification. The specification teaches that the "invention" is based on the need to maintain "correct periodicity between network stations." '2893 Patent at 2:15-17. The specification then continues:

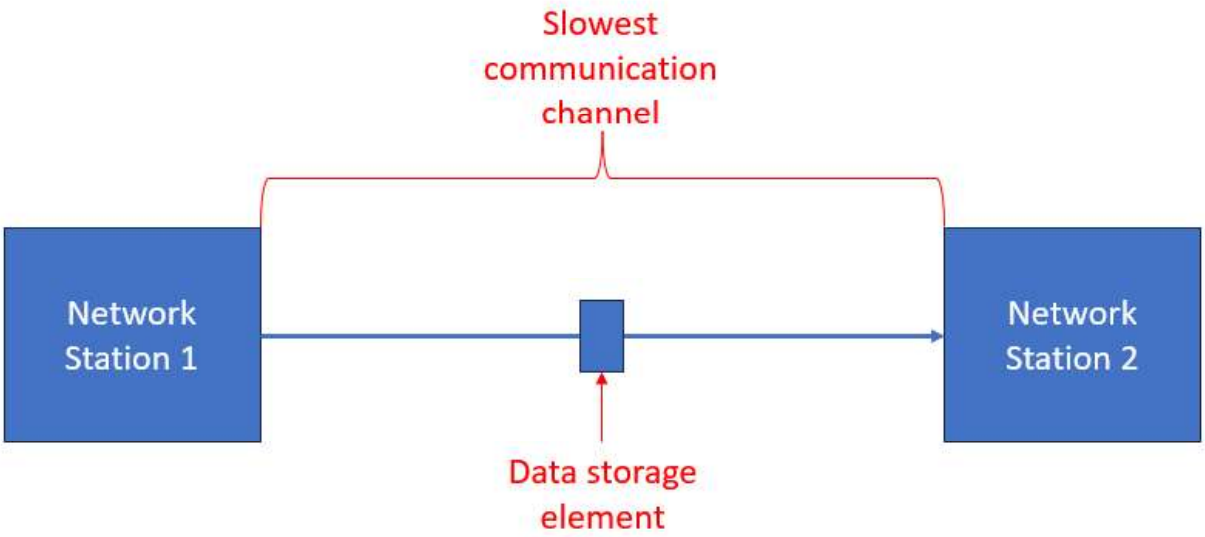
> ***Because the data packages have a fixed size of N data elements***, the communication of a complete package between two network stations takes N clock cycles, or N handshake driven data transfers in case of an asynchronous implementation of the network. The routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package, e.g. the first data element (i.e. a header), although other data elements may (also) contain such information. Since a network station

> expects routing information to arrive periodically ***(i.e. after every N cycles)***, the introduction of a delay on the first communication channel (which typically is the slowest channel of the network) matching such a period, i.e. by delaying the whole data package rather than a single data element, the delayed data package is received by the receiving network station during the appropriate period, e.g. clock cycle.

'2893 Patent at 2:17-33 (emphasis added). A POSITA would understand that the specification teaches that data packages have a "***fixed size*** of N data elements" in order to maintain periodicity such that routing information arrives at network stations at a defined period, i.e., "after every N cycles." *Id.*

97. For a better understanding of why a POSITA would understand that the specification requires data packages have a fixed size of N data elements in order to maintain periodicity, I explain the problem and the solution that the patent is directed to. The specification teaches that the clock speed that an integrated circuit operates at "may be determined by the slowest communication channel, i.e. the channel exhibiting the largest data transfer delay." '2893 Patent at 1:34-38. Electrical signals can only travel so far in a given time period. Thus, the clock rate must be set to a slow enough time period such that an electrical signal can travel through the slowest communication channel in a single clock cycle.

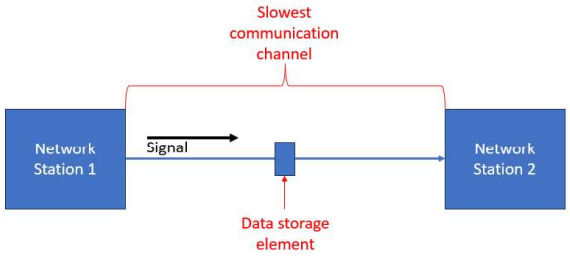
98. The specification discusses a known solution to this problem is to "introduce a data storage element such as a latch into the slowest data communication channel." '2893 Patent at 1:41-43. I have illustrated this below:



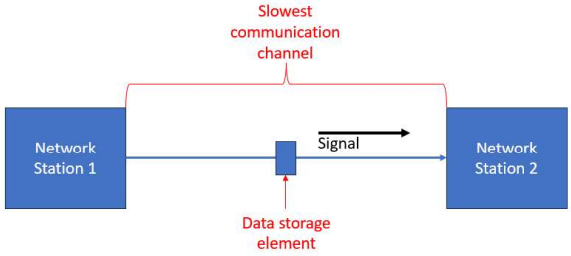
The data storage element functions as a way station breaking up the slowest communication channel into two shorter segments or channels. These shorter segments allow the clock rate to be increased because it takes less time for a signal to traverse one of the segments than the entire channel. This allows the signal to be transferred over two faster clock cycles rather than one slower clock cycle. For example, during the first clock cycle, the signal is transmitted from the sending network station (network station 1) to the data storage element. During the second clock cycle, the signal is transmitted from the data storage element to the receiving network station (network station 2). Breaking the slowest communication channel into segments allows for the use of a faster clock throughout the integrated circuit. A faster clock throughout the integrated circuit allows for faster data transmission and faster completion of tasks. I have illustrated this below and included a timing diagram showing during which clock cycle the signal was output by the sending station and when it was received at the input of the receiving station.

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

Clock Cycle 1



Clock Cycle 2

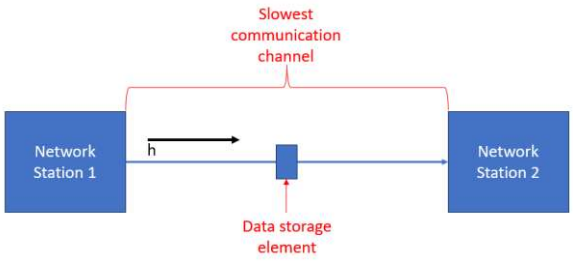


Output of sending station	Signal	
Input of receiving station		Signal
Clock cycle	1	2

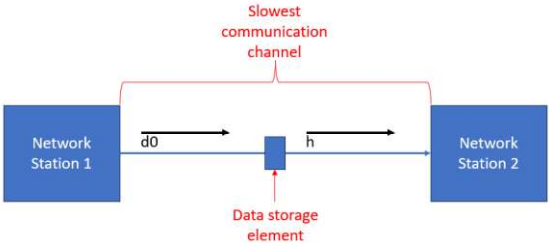
99. The patent identifies an issue with this solution. Some integrated circuits have network stations (e.g., routers) designed to receive routing information within the data packages during a particular predefined clock cycle. *Id.* at 1:54-57. For example, some systems may have data packages that consist of three data elements, such that N=3. Typically, the first data element is referred to as a header and contains routing information. *See id.* at 2:22-26. In this example, the header h is followed by two data elements (d0 and d1) that contain the payload of the data package. The routers or network stations that receive the data packages are designed to receive the routing information every three clock cycles, e.g., at t, t+3, t+6, t+9, etc. The one cycle of delay caused by inserting the data storage element into the channel causes the routing information to arrive outside of its predefined clock cycle resulting in an error. *Id.* at 1:57-61. I have also illustrated the data package being transferred and included another timing diagram below to show the transmission of the data package with only the one delay element (i.e., data storage element) inserted. This timing diagram includes an additional row called "Routing information expected (h)" which refers to when the header is expected at the receiving station. If "YES" appears in a time slot (e.g. at time t below), the network stations expect routing

information, and if a "NO" appears (e.g. at t+1) the network stations do not expect routing information. As discussed above, the network stations expect routing information every three clock cycles (e.g., at t, t+3, t+6, t+9).

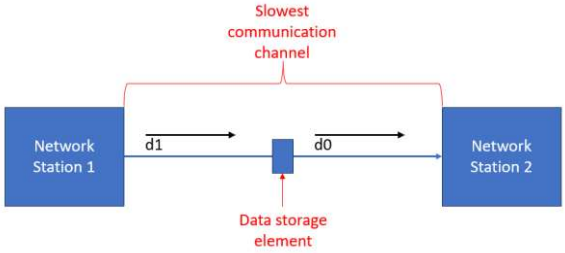
Clock Cycle t



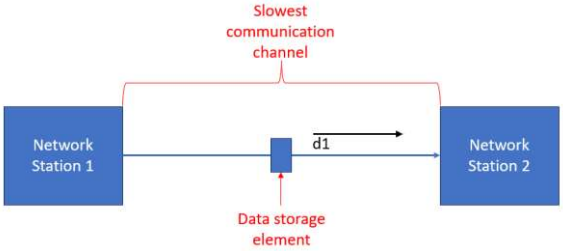
Clock Cycle t+1

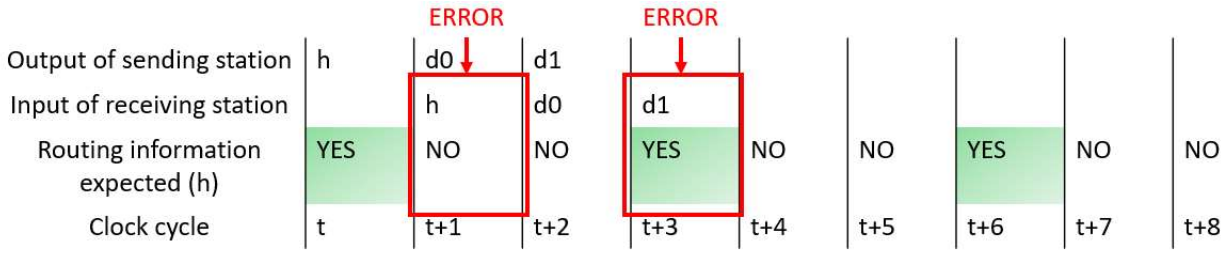


Clock Cycle t+2



Clock Cycle t+3

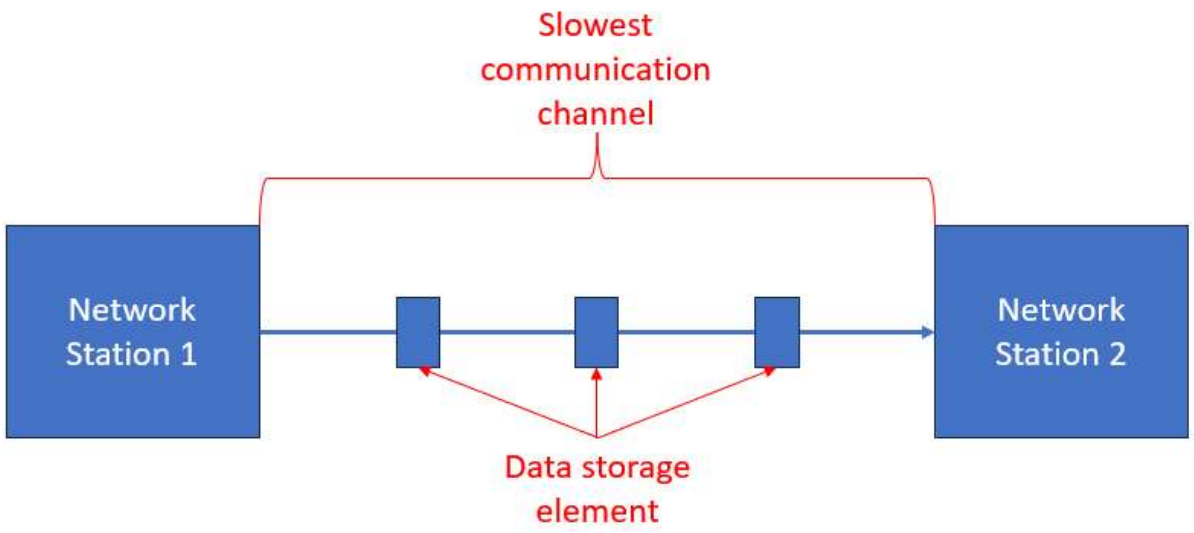




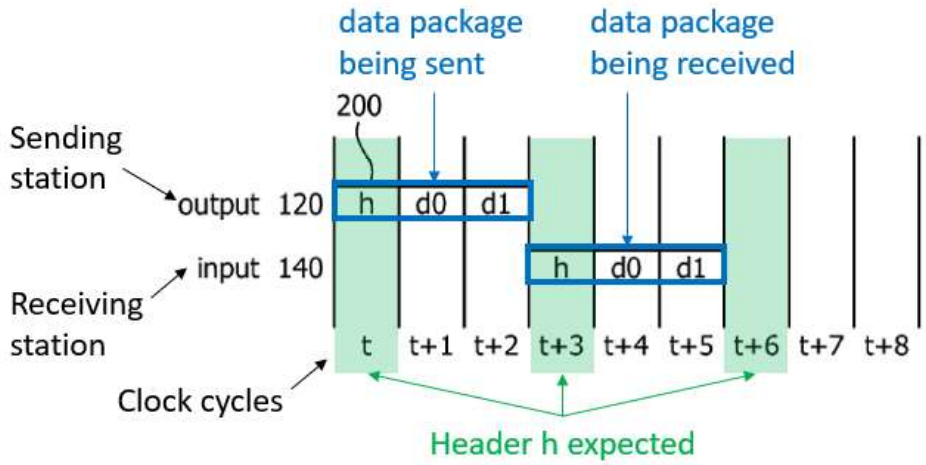
Here, the header h is sent from the output of the sending station to the data storage element at clock cycle t. The header h is then sent from the data storage element to the input of the receiving station at clock cycle t+1. However, because the receiving station did not expect to receive the routing information contained in header h at t+1, an error results. *See id.* at 1:57-61. The

receiving station also receives d1 at clock cycle t+3, a cycle that it expects routing information. This also results in an error.

100. The specification of the '2893 patent teaches a solution to this problem. It teaches to "delay the whole data package rather than a single data element" (*id.* at 2:30-31) by inserting M*N data storage elements, where N is a number of data elements within a package and M is an integer (*id.* at 1:65-2:14). *See also id.* at 5:54-62 ("this communication channel…is equipped with M*N data storage elements to introduce a delay of M*N cycles onto the communication channel, with N corresponding to the size of a data package, thus allowing an increase of the maximum communication frequency of the data network 100 at the expense of the introduction of a delay of a single data package, i.e. the number of clock cycles it takes to communicate such a data package, on the slow communication channel 150."). In other words, the patent teaches to insert data storage elements into the channel such that the number of data storage elements is a *multiple* of the package size (i.e., the number of data elements in a package, N). I have illustrated this below where N=3 and M=1:

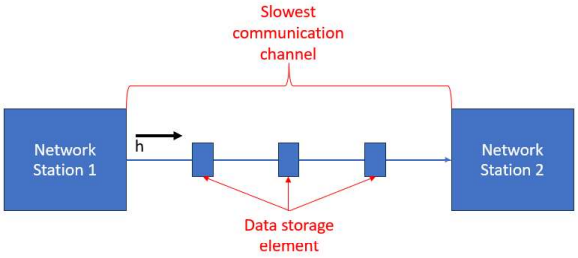


Because the number of data storage elements inserted into the channel is a multiple of the number of data elements in a data package, the arrival of the data package as a whole is shifted such that the data element containing routing information arrives during a clock cycle where the router expects routing information. *See id.* I have annotated Figure 2 below to show this.

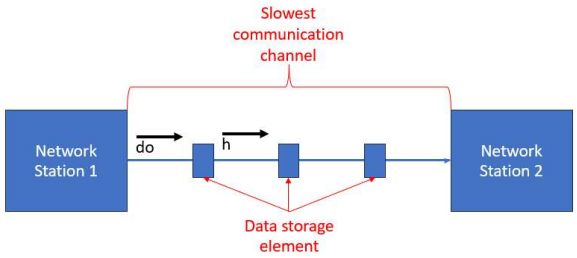


'2893 Patent at Fig. 2 (annotated). I have also illustrated the data package being transferred and provided a timing diagram summarizing the transfer.

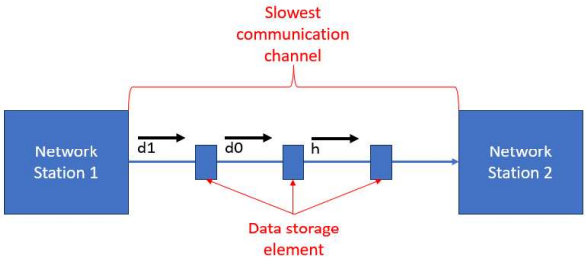
Clock Cycle t



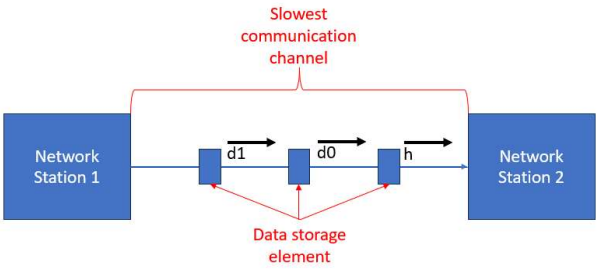
Clock Cycle t+1



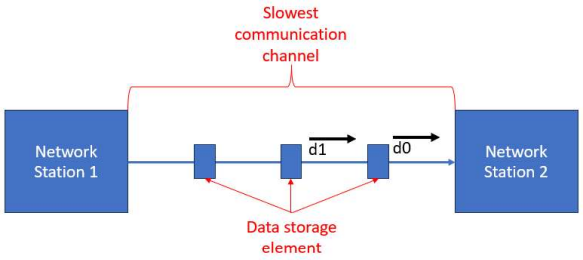
Clock Cycle t+2



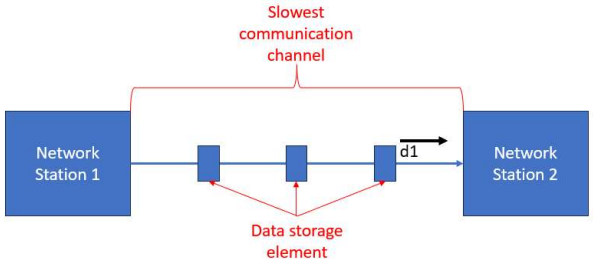
Clock Cycle t+3

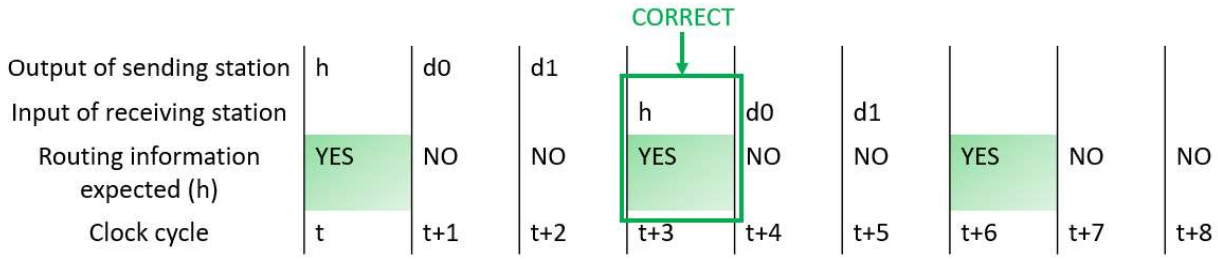


Clock Cycle t+4



Clock Cycle t+5



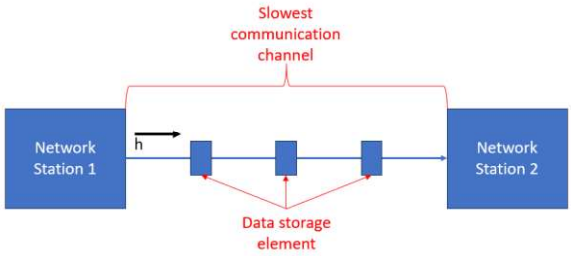


Here, header h is sent by the sending station to the first data storage element during clock cycle t. Header h is then transmitted from the first data storage element to the second data storage element at t+1; from the second data storage element to the third data storage element at t+2; and

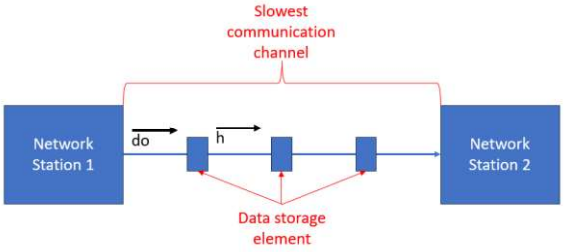
finally from the third data storage element to the receiving station such that it arrives at the receiving station at t+3, a clock cycle where routing information is expected.

101. If any data package communicated by the network did not contain exactly N data elements, the periodicity maintained by the system would be lost and routing information would not arrive at the correct clock cycle. *See id.* at 1:54-61. For example, if one data package had an extra data element (N+1), the entire sequence would be thrown off and the receiving station would receive non-routing information data in a clock cycle intended for it to receive routing information. Below, I have provided a timing diagram for such a data package containing four elements: a header data element (h) and three payload data elements (d0, d1, and d2).

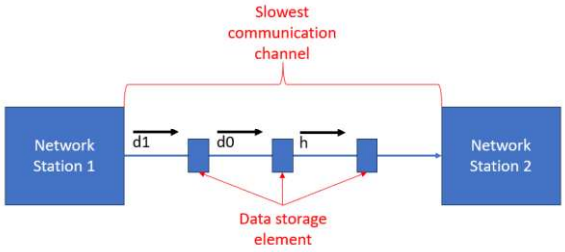
Clock Cycle t



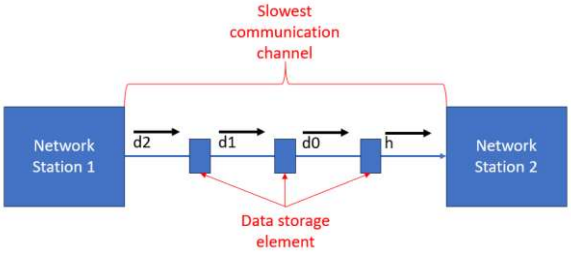
Clock Cycle t+1



Clock Cycle t+2

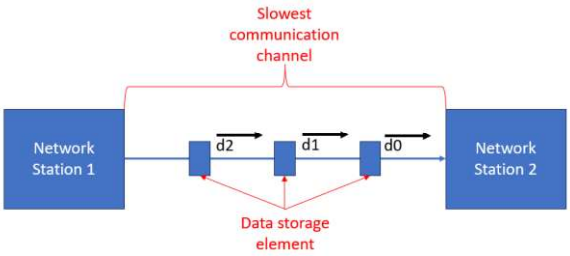


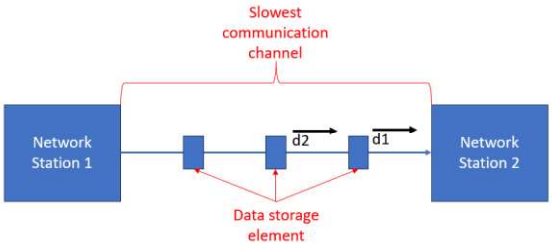
Clock Cycle t+3



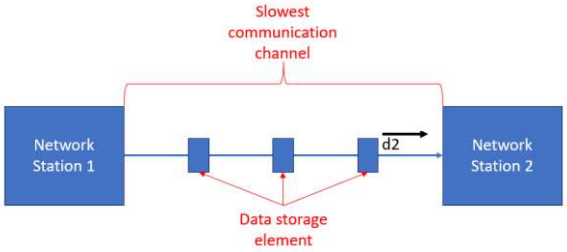
Clock Cycle t+4

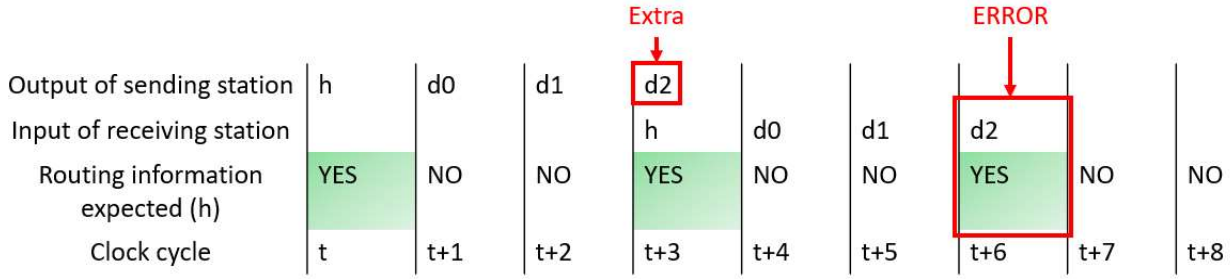
Clock Cycle t+5





Clock Cycle t+6





Because of the extra data element d2 in the data package, the periodicity of the system is lost and extra data element d2 arrives at the input of the receiving station during a clock cycle when routing information is expected.

102. Thus, a POSITA would understand that the solution to the problem described in the '2893 Patent requires every data package communicated by the network stations to have a fixed size of N data elements. Without Defendants' construction, claim 10 would diverge from the solution taught in the specification and would be inoperable.

2. "data package"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
See construction of "each data package comprising N data elements" above.	"Fixed-size arrangement of data"

103. It is my opinion that a POSITA would understand the term "data package" within the context of Defendants' construction of "each data element comprising N data elements" without any additional construction of "data package." NST's construction does not specify whether every data package must have the same fixed size N data elements identified above. It also does not clarify whether all, some, or even just one data package within the system needs to be analyzed as part of the infringement analysis. It is ambiguous as to whether the number of data elements having a fixed size arrangement applies to just a single data package, or the fixed-sized arrangement applies across every data package. It is also ambiguous as to whether the fixed-sized arrangement means that every data package is the same size or that a data package does not change size once it is within the network. As discussed above, the claim language and the specification make clear that every data package communicated by the network stations must have a fixed size of N data elements, and Plaintiff's construction leaves open ambiguity on this issue. Plaintiff's construction also introduces the concept of the "arrangement" of data, which is ambiguous and something not contemplated by the claim language "data package."

3. "data storage elements"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
"each being a structure that stores one data element"	"Array of one or more elements that store data"

104. I understand that Defendants have construed the term "data storage elements" to mean "each being a structure that stores one data element." Based on my understanding of the claim language and the specification, I agree with Defendants' construction.

105. I understand the dispute here is whether a "data storage element" stores one "data element" or if it can store more than one "data element." Based on my understanding of the claim language and the specification, it is my opinion that a "data storage element" stores only one "data element."

106. It is my opinion that the claim language makes it clear that each "data storage element" stores only one "data element." For example, claim 10 requires "inserting M*N data storage elements into the data communication network, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel." This corresponds to the "N data elements" in each data package and creates a mathematical relationship between the number of data elements (N), the number of data storage elements (M*N), and the number of cycles of delay caused by the data storage elements (M*N). A POSITA would understand that if a data storage element stored more than one data element, this mathematical relationship would be lost.

107. It is also my opinion that the specification's use of the terms "data storage element" and "data element" is consistent with Defendants' construction of the term and that a "data storage element" is a structure that stores one "data element." For example, in discussing the asynchronous embodiment, the specification teaches that:

> the FIFO buffer 509 must be capable of storing more than M*N data elements….This can be realized by adding one or more data storage elements to the M*N data storage elements as overwrite protection.

'2893 Patent at 9:47-51. First, if a data storage element could store more than one data element, it would not be necessary to add additional data storage elements to the M*N data storage elements. Second, this passage confirms that a data storage element is not a larger structure that stores multiple data elements, such as the FIFO buffer 509, but rather the individual structures

that store a single data element. For example, a FIFO that can store three data elements is three data storage elements in the context of the patent, not one.

108. As a second example, the specification teaches that the data storage elements store a single data element, such as "first data element h" (*id.* at 6:36), for a clock cycle before passing it on during the next clock cycle. *See id.* at 6:62-66 ("the first data storage element 160 receives the header h at t+3, passes it on to the second data storage element 160 at t+4, which passes it on to the third data storage element 160 at t+5, which finally passes it on to the data router 160 at t+6"); 8:1-4 ("At T=t, data element h is received by data storage element 160 in the first subchannel 152, which stores the data element h and sends it to the data router 140 at T=t+1").

109. I disagree with Plaintiff's construction. A POSITA would not understand NST's construction of "data storage elements" to be consistent with the claim language or the specification in that it allows a data storage element to store "one or more elements." In particular, a POSITA would understand the term "array," which does not appear in the patent, to be an ambiguous term that is potentially overbroad. For example, the term "array" may be used to refer to a register that stores the collection of individual bits within a data element, the collection of data elements, or any type of data storage memory. It would not provide any clarity to the term, on the contrary, it will add ambiguity to it.

G. '800 Patent Terms

1. "first determination unit" / "second determination unit"

Defendants' Proposed Construction	Plaintiff's Proposed Construction
Subject to Section 112 ¶ 6. Function: "determining a first/second optimal amount of data to be buffered by the first/second memory" and for at least one of the first determination unit and the second	NST incorporates its definition for the term "determination unit" (as "circuit that makes determinations based on stored or received information.") and the remaining language should be afforded their plain and ordinary meanings.

determination unit "determining an optimal moment for sending data" Structure: indefinite	

110. Claim 12 of the '800 patent reads in part (emphasis added):

"wherein the first interconnect module includes a first memory for buffering first data from the first processing module, the first interconnect module further including a ***first determination unit***, wherein the ***first determination unit*** is configured to determine a first optimal amount of data to be buffered by the first memory, and the second interconnect module includes a second memory for buffering second data from the second processing module, the second interconnect module further including a ***second determination unit***, wherein the ***second determination unit*** is configured to determine a second optimal amount of data to be buffered by the second memory,

…

wherein ***at least one of the first determination unit and the second determination unit*** is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery."

111. While claim 12 recites the functions of the first and second determination units, it does not recite any structure for the first and second determination units. The term "determination" is simply a repeat of the subsequently recited "to determine…" function. In the field of integrated circuits, the term "unit" is not a term of art that would connote any specific or known structure, whether alone or combined with "determination" and therefore a POSITA would not understand "determination unit" to identify or be associated with any specific or known structure. This is the case with "determination unit" by itself or in combination with the functions of the first and second determination units recited in claim 12.

112. The specification of the '800 patent introduces "determination unit" as follows (notably, the specification interchangeably refers to "first and second determination ***means*** BLDU1, BLDU2" and "first and second determination ***units*** BLDU1, BLDU2"):

> "In addition, a ***first and second determination means*** BLDU1, BLDU2 are arranged in the network interfaces NI associated to the slave S and the master M, respectively. The ***first and second determination units*** BLDU1, BLDU2 serve to determine the optimal burst length for transferring data over the network N according to the current communication or connection properties. The determination of the optimal burst length can be performed statically or dynamically, during the initial phases of the required processing or during predetermined time intervals. Alternatively, the optimal burst length may be determined dynamically (1) every time a connection is set up for transferring data over the network, (2) for every transaction, (3) whenever an IP switches to another connection, (4) for every packet, (5) when the state of the network on chip changes (e.g., reconfiguration, NoC load, buffer fillings, etc.). The determination of the optimal burst length may be performed based on information stored in the determination units BDLU 1, 2 or on information received from the network N or IP blocks. Accordingly, the network N may comprise a communication property means CPM for determining and possibly storing the communication or connection properties for a requested communication or connection. The CPM can be centralized, or distributed (e.g., in every NI)." '800 patent, 6:47-7:3 (emphasis added).

113. Fig. 2 shows "first and second determination ***units*** BLDU1, BLDU2" simply as empty boxes (other than the BLDU1 and BLDU2 names) inside what the patent refers to as the network interfaces NI:

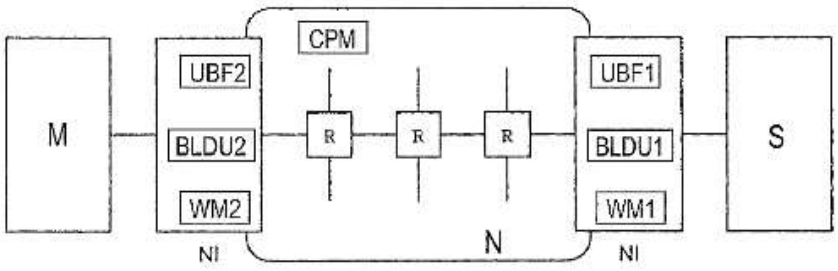


FIG.2

114. The '800 specification describes the first and second determination units/means only by their functions.

> "In addition, a ***first and second determination means*** BLDU1, BLDU2 are arranged in the network interfaces NI associated to the slave S and the master M, respectively. The ***first and second determination units*** BLDU1, BLDU2 serve to determine the optimal burst length for transferring data over the network N according to the current communication or connection properties. The determination of the optimal burst length can be performed statically or dynamically, during the initial phases of the required processing or during predetermined time intervals. Alternatively, the optimal burst length may be determined dynamically (1) every time a connection is set up for transferring data over the network, (2) for every transaction, (3) whenever an IP switches to another connection, (4) for every packet, (5) when the state of the network on chip changes (e.g., reconfiguration, NoC load, buffer fillings, etc.). The determination of the optimal burst length may be performed based on information stored in the determination units BDLU 1, 2 or on information received from the network N or IP blocks. Accordingly, the network N may comprise a communication property means CPM for determining and possibly storing the communication or connection properties for a requested communication or connection. The CPM can be centralized, or distributed (e.g., in every NI)." '800 patent, 6:47-7:3 (emphasis added).
>
> "Besides the optimal burst length determination, also the transmission moment may be determined in a similar way ***by the first and second determination means BLDU1, BLDU2***. For a guaranteed throughput GT connection, data should wait for one of the slots reserved for its connection. Using a "flush"-like signal/flag may force the sending of the data in advance. Alternatively, for a best effort BE connection, a round robin arbitration across connections in the NI can be used. A "flush"-like signal may force a temporarily higher priority for a connection." '800 patent, 7:4-13 (emphasis added).

115. Therefore, the '800 patent specification only describes the locations of the first and second determination units, but provides no description of any structure for the first and second determination units, nor any structure for performing any of the disclosed or claimed functions of the first and second determination units.

116. Plaintiff's proposed construction for "determination unit" is "circuit that makes determinations based on stored or received information." However, there is no circuit disclosed anywhere in the specification for the determination unit, or otherwise that performs the functions

of the first and second determination units. A POSITA would understand that the patent is not directed to a circuit level or abstraction and provides no circuit level details or implementation (for example, I performed a word search, and the word "circuit" does not appear anywhere in the DESCRIPTION OF THE PREFERRED EMBODIMENTS section of the specification). Moreover, a "determination unit" is not a term of art. Nor does it connote a structure known to a POSITA. There is no specific, known, type of circuitry that is referred to as a "determination unit."

117. The title of the '800 patent, and the preamble of claim 12, include "integrated circuit." However, that does not reasonably convey a circuit structure for the first and second determination units. Integrated circuits of the type contemplated by the '800 patent are incredibly complex, which would include on the order of millions up to billions of transistors that interact with each other to perform very complex functions. A general reference to "integrated circuit" by no means provides to a POSITA anything structurally other than large groups of interconnected transistors formed on, for example, a silicon substrate. More importantly, even in the context of an integrated circuit, the first and second determination units need not be a circuit. For example, the functions identified for the first and second determination units can be implemented as software or firmware operated by general purpose hardware in the integrated circuit, which was a known way to configure functionality within an integrated circuit. Therefore, the first and second determination units are not necessarily just a circuit even in the context of an integrated circuit.

118. Finally, the Plaintiff's construction calls for a circuit "that makes determinations based on stored or received information." The specifications states "[t]he determination of the optimal burst length ***may be*** performed based on information stored in the determination units

BDLU 1, 2 or on information received from the network N or IP blocks." '800 patent, 6:62-65 (emphasis added). Therefore, the specification indicates that the use of information stored in the determination units or received from elsewhere is optional. Further, it is conceivable a circuit, software/firmware operated by general purpose hardware, etc., could be designed to perform the functions of the determination units without using stored information or information received from elsewhere. Therefore, I see no basis to include "that makes determinations based on stored or received information" in the construction of "determination unit."

2. "optimal amount of data"

Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
Indefinite	Plain and ordinary.

119. Based on my review of the claim language, the specification and the prosecution history, it is my opinion that the term "optimal amount of data" is indefinite because a POSITA would not be able to understand its bounds with reasonably certainty.

120. A POSITA would not be able to objectively ascertain an "optimal amount of data." There is no industry standard as to the optimal amount of data to be buffered or transferred over a network. A POSITA would understand that the term is purely subjective and left to the user's discretion. The claim term and the surrounding claim language provide no guidance to a POSITA to reasonably ascertain what an "optimal amount of data" is. Claim 12 merely states that first and second "optimal amounts of data" are determined ("the first determination unit is configured to ***determine a first optimal amount of data*** to be buffered by the first memory" and "the second determination unit is configured to ***determine a second optimal amount of data*** to be buffered by the second memory") (emphasis added) and that the data is transferred when the data buffered reaches the optimal amount ("the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory ***reaches***

the first optimal amount" and "the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory ***reaches the second optimal amount***") (emphasis added).

121. Based on my review of the specification, it provides no guidance to a POSITA on how to reasonably ascertain an "optimal amount of data" with any objective bounds. The specification discusses "optimal first or second amounts of data," (4:20-21) "optimal burst length," (3:29, 6:29-30, 6:49-64, 7:51) "optimal packet size," (4:55, 7:24-34) and "optimal transfer" (4:57, 6:16); however, none of these discussions indicate to a POSITA what an "optimal amount of data" is.

122. For example, in column 4:18-24, the specification mirrors the claim language:

> According to a preferred aspect of the invention at least one of said first and second wrapper means comprise ***a determination unit BLDU for determining the optimal first or second amount of data to be buffered in said first or second wrapper means*** before said data is transferred according to the communication properties of said communication between said first and second processing module.

'800 Patent at 4:18-24 (emphasis added). However, the specification fails to provide a POSITA with any understanding of how to ascertain an optimal amount.

123. In column 4:49-57, the specification states an advantage of buffering an optimal amount:

> The invention is based on the idea to ***buffer data until the buffered data is sufficiently large*** to be transferred optimally over an interconnect means in a packet. ***The larger a packet is, the smaller is the amount of packet headers and therefore the overhead is reduced and the interconnect is utilized more efficiently.*** The data is only transferred when sufficient data for an optimal packet size has been buffered even when data can be sent earlier. The data is only transferred from the buffer when the conditions for an optimal transfer are satisfied.

Id. at 4:49-57 (emphasis added). However, this portion of the specification merely provides an advantage of buffering, not what is "sufficiently large" or what an "optimal amount of data" is.

Similarly, in column 7:14-34, the specification touts the advantage of reduced overhead resulting from buffering until an "optimal packet size" is reached:

> In the first and second embodiment the data, i.e. the buffered data, is sent over the network in form of packets. The packets are preferably formed in the respective network interfaces NI and ***should be sufficiently large to be transferred in an optimal way with regard to the network N.*** As every packet comprises a packet header, the larger the packets, ***the smaller the number of required packet headers, which will consequently lead to a reduced overhead and an improved network utilization.*** The data is buffered until the buffered data reach an optimal packet size such that the buffered data can be transferred over the network. If the amount of buffered data has not yet reached the optimal packet size, none of the data is transferred over the network N even if transferring a smaller packet size is possible. The burst size is associated to a bus or to the IP view on communication, while the packet length is only applicable when packetization takes place (not necessary for a bus). All of the burst size determination schemes mentioned in the previous paragraph also apply to the optimal packet size determination.

Id. at 7:14-34 (emphasis added). But again, the specification fails to teach a POSITA how to ascertain an "optimal amount of data."

124. In column 6:53-62, the specification discusses when an optimal amount of data might be determined:

> The determination of the optimal burst length can be performed statically or dynamically, during the initial phases of the required processing or during predetermined time intervals. Alternatively, the optimal burst length may be determined dynamically (1) every time a connection is set up for transferring data over the network, (2) for every transaction, (3) whenever an IP switches to another connection, (4) for every packet, (5) when the state of the network on chip changes (e.g., reconfiguration, NoC load, buffer fillings, etc.).

Id. at 6:53-62. However, this portion of the specification also fails to provide a POSITA with how to reasonably ascertain such an amount.

125. In column 6:62-7:3, the specification discloses that:

> The determination of the optimal burst length may be performed ***based on information stored in the determination units BDLU 1, 2 or on information received from the network N or IP blocks***. Accordingly, the network N may comprise a communication property means CPM for determining and possibly storing the communication or connection properties for a requested

> communication or connection. The CPM can be centralized, or distributed (e.g., in every NI).

Id. at 6:62-7:3 (emphasis added). However, the specification does not teach how the "information stored in the determination units" or the "the information received from the network N or IP blocks" is used to ascertain an "optimal amount of data." It also fails to show a POSITA how "the communication or connection properties" are used to reasonably ascertain an "optimal amount of data."

126. In column 7:44-46, the specification states that "requests and responses are aggregated in bursts with a length optimal for the particular interconnect." *Id.* at 7:45-46. But the specification again fails to provide a POSITA with an objective way to ascertain what an "optimal amount of data" is for a "particular interconnect."

127. In column 6:47-53, the specification discusses the use of communication or connection properties to "determine the optimal burst length":

> In addition, a first and second determination means BLDU1, BLDU2 are arranged in the network interfaces NI associated to the slave S and the master M, respectively. The first and second determination units BLDU1, BLDU2 serve to ***determine the optimal burst length for transferring data over the network N according to the current communication or connection properties***.

Id. at 6:47-53 (emphasis added). The specification provides a list of connection properties. *See id.* at 5:27-35. However, the specification never teaches a POSITA how to reasonably ascertain an optimal amount of data to be buffered from any one of these properties or indicate how to balance these properties to ascertain an "optimal amount of data." Without such guidance from the specification, a POSITA would not know how to reasonably ascertain an "optimal amount of data."

128. The specification also lists a number of other considerations associated with the optimal amount data to be buffered. *See* '800 patent, 2:65-67 ("interconnect utilization"); 3:29-

30 ("in order to prevent deadlock"); 3:60-63 ("until a sufficiently large amount of data to be transferred over the interconnect in a single package is reached"); 4:20-24 ("according to the communication properties of said communication between said first and second processing module"); 4:55-57 ("The data is only transferred from the buffer when the conditions for an optimal transfer are satisfied."); 6:27-20 ("to suit the optimal burst length for the network N"); 6:50-53 ("according to the current communication or connection properties"); 6:53-54 ("the optimal burst length can be performed statically or dynamically," suggesting to a POSITA various optimal amounts without explanation as to when or how the determination is to be made); 7:23-25 ("optimal packet size such that the buffered data can be transferred over the network"); 7:44-46 ("bursts with a length optimal for the particular interconnect"). As discussed above, the specification provides no guidance to a POSITA as to how to determine the optimal amount of data in view of any of these considerations individually. It also does not provide a POSITA any guidance as to how to balance multiple conflicting considerations to determine a single optimal amount of data. Therefore, the specification fails to provide the objective bounds needed for a POSITA to determine an "optimal amount of data" with reasonable certainty, and the term is indefinite.

3. "optimal moment for sending the data in said first wrapper or said second wrapper

Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
Indefinite	Plain and ordinary.

129. Based on my review of the claim language and the specification, it is my opinion that the term "optimal moment for sending the data in said first wrapper or said second wrapper" is indefinite because a POSITA would not be able to understand its bounds with reasonable certainty. A POSITA would find the term "optimal moment for sending the data in said first

wrapper or said second wrapper" to be indefinite for similar reasons as "optimal amount of data." Neither the claim language nor the specification provides a POSITA with objective boundaries for the term.

130. Claim 12 states that "at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties" and then provides a list of communication properties:

> wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, throughput where a lower bound on throughput is guaranteed, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.

131. Neither the claim language nor the specification provide a POSITA with objective boundaries for an "optimal moment for sending the data in said first wrapper or said second wrapper."

132. It is my opinion that even if the claim only required consideration of the individual communication properties (which it does not), it would not be reasonably clear to a POSITA how to ascertain an optimal moment with respect to any of the *individual* communication properties. To the extent the claim requires finding an optimal moment for each one of the communication properties (which it does not), a POSITA would have no idea how to select an optimal moment based on, for example, the communication property data correctness. Data correctness is not something that is dependent on the timing of the transmission of the data, but rather the properties of the interconnect performing the data transfer. Similarly, the specification provides no guidance of how to determine an optimal moment based on any of these factors. Further, to the extent the claim requires finding an optimal moment for each one of

the communication properties recited (which it does not), as stated above, neither the claim language nor the specification provide a POSITA with objective boundaries for an "optimal moment for sending the data in said first wrapper or said second wrapper." The sole discussion of any "moment" in the specification is reproduced below:

> Besides the optimal burst length determination, also the transmission ***moment*** may be determined in a similar way by the first and second determination means BLDU1, BLDU2. For a guaranteed throughput GT connection, data should wait for one of the slots reserved for its connection. Using a "flush"-like signal/flag may force the sending of the data in advance. Alternatively, for a best effort BE connection, a round robin arbitration across connections in the NI can be used. A "flush"-like signal may force a temporarily higher priority for a connection.

'800 Patent at 7:4-13 (emphasis added). Though the passage mentions guaranteed throughput in describing the type of connection used for the communication, it does not provide a way for a POSITA to ascertain an "optimal moment" based on throughput. In a guaranteed throughput (GT) connection as described in the '800 patent, the transmission moment of the data is reserved in slots. The fact that "data should wait for one of the slots reserved for its connection" ('800 Patent at 7:7-8) tells a POSITA nothing about how the slots, and thus the transmission moment, are determined. The passage provides that the "transmission moment may be determined in a similar way" as the "optimal burst length." '800 Patent at 7:4-6. However, the specification's only discussion tying communication properties to determining an optimal amount or optimal moment provides no discussion on how the properties are actually used. *See id.* at 6:49-53 ("The first and second determination units BLDU1, BLDU2 serve to determine the optimal burst length for transferring data over the network N according to the current communication or connection properties.").

133. It is my opinion that the specification similarly provides no way of reconciling the ten communication properties to determine a single optimal amount. Each of these properties could lead to a different optimal moment. A POSITA would have no idea of how to weigh these

communication properties to result in a single optimal moment. For example, a POSITA would not know how to balance the seemingly unrelated properties of "ordering" and "data correctness." Merely identifying ten different properties for determining an optimal moment without providing any procedure for making such a determination renders "optimal moment for sending the data in said first wrapper or said second wrapper" indefinite to a POSITA.

134. It is my opinion that NST's proposed construction of "said first wrapper" and "said second wrapper" as "said first memory" and "said second memory" does not correct the indefiniteness problem with "optimal moment," particularly with respect to the earlier recited language in claim 12 requiring the transfer of data "when" the amount buffered reaches an optimal amount. *See* '800 Patent at 12:8-15 ("the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches the first optimal amount, and the second interconnect module transferring the second data to the first processing module when the second data buffered in the second memory reaches the second optimal amount"), 12:17-21 ("an optimal moment for sending the data in said first wrapper or said second wrapper"). It is not clear to a POSITA which of the optimal amount of data or optimal moment is controlling. If the optimal moment is before the optimal amount of data is achieved, then the transfer at the optimal moment would not occur "when" the optimal amount of data is reached as previously recited in claim 12. If the optimal moment is after the optimal amount of data is achieved, then the transfer would have taken place before the optimal moment and would obviate the need for sending data at an optimal moment. This further supports my opinion that "optimal moment" is indefinite.

4. "said first wrapper" / "said second wrapper"

Defendants' Proposed Construction	**Plaintiff's Proposed Construction**
Indefinite	"said first memory" / "said second memory"

135. It is my opinion that the terms "said first wrapper" and "said second wrapper" as used in claim 12 are indefinite. The terms "first wrapper" and "second wrapper" do not previously appear in claim 12, and a POSITA would not be able to reasonably ascertain what "said first wrapper" and "said second wrapper" are referring to.

136. There are multiple structures previously identified by the claim that "said first wrapper" and "said second wrapper" could be referring to. The specification teaches multiple functions that a wrapper may have. For example, the specification teaches that the wrapper may "buffer data." '800 Patent at 3:41-46 ("A first wrapper means associated to said second processing module buffers data from said second processing module…"); 3:54-60 ("a second wrapper means is associated to the first processing module for buffering data"); 5:58-64 ("The wrapper means WM2, WM1, are responsible for buffering any data sent from the master M and the slave S over the network N."); 6:14-16 ("the wrapper means WM1, WM2 serve to buffer data."). The buffering function in claim 12 is performed by the "first memory" and the "second memory." *Id.* at 11:63-66 ("wherein the first interconnect module includes a first memory for buffering first data from the first processing module"); 12:1-3 ("the second interconnect module includes a second memory for buffering second data from the second processing module"). These structures store data and claim 12 recites that there is "data in said first wrapper or said second wrapper." '800 Patent at 12:18-19. These disclosures suggest to a POSITA that a wrapper may include a memory of some type. But the specification also teaches that the wrapper may "transfer" data. '800 Patent at 3:58-60 ("said second wrapper means then transfers said buffered data…"); 3:64-4:2 ("said first and second wrapper means are adapted to transfer the buffered data"); 4:41-46 ("A second wrapper means associated to said second processing module buffers data from said second processing module to be transferred over said interconnect means until a

first amount of data is buffered and then transfers said first amount of buffered data to said first processing module"); 6:22-25 ("The first and second wrapper means WM1, WM2 are adapted to immediately transfer the buffered data…"). The transferring function in claim 12 is performed by the "first interconnect module" and the "second interconnect module." '800 Patent at 12:8-14 ("the first interconnect module transferring the first data to the second processing module when the first data buffered in the first memory reaches the first optimal amount, and the second interconnect module transfer ring the second data to the first processing module when the second data buffered in the second memory reaches the second optimal amount"). These structures contain the determination units, which the specification teaches the wrapper may contain. '800 Patent at 4:18-24 ("at least one of the first and second wrapper means comprising a determination unit BLDU"). These disclosures may suggest to a POSITA that a wrapper does more than what a memory does, which introduces ambiguity to a POSITA as to what was actually intended by "said first wrapper" and "said second wrapper."

137. "Said first wrapper" and "said second wrapper" may also be referring to an unclaimed interface structure. The specification additionally teaches that "wrappers" have interface functionality that allows IP modules to be designed separately from the interconnect. The following teaches includes additional functionality of the wrapper beyond buffering and transferring data, as described above:

> Intellectual property modules connected to the interconnect via the wrapper or interconnect interfaces can therefore be build independently of the interconnect, i.e. the reuse of these IP modules can be increased, as the knowledge of the interconnect characteristics lies only in the wrappers. As for the requests, this may introduce possible additional latency, however the overall system efficiency is increased.

'800 Patent at 8:13-20. This is consistent with how "wrapper" is used in the extrinsic evidence. Wrappers were known in the art to convert between the protocol used by an IP module and the protocol used by the interconnect or another IP module. For example:

> The wrapper-based bus is a promising technology for reusing IP cores because it separates the communication logic from the cores thereby avoiding the connectivity problems related to physical bus protocols. The wrapper-based approach uses the IP core interface protocol, which is independent of the physical bus protocol, and uses hardware wrappers to handle the core-to-core communication. Hence, IP cores complying with the interface protocol can be integrated into SOCs that have different physical buses as backbones.

Ex. 24 at 804;

> For cores that are neither programmable nor reconfigurable, the only option for interfacing with the networking logic of the tile is to utilize a wrapper, which would have the responsibility of packetizing and depacketizing the cores requests and responses. The wrappers have the responsibility of (i) receiving the contents from the core interface, preparing the packets and dispatching them to the network logic of the tile and (ii) receiving the packets from the networking logic and presenting the contents to the core interface.

Ex. 26 at 5;

> The Proteo topologies presented and analyzed in this paper are ring and tree. Those are constructed from interface IPS and router IPS. Interface IP is the wrapper between the actual communication structure and a functional part of the system. Interface blocks build Proteo packets from interface signals and extract interface signals from packets in the receiving end. Routers control packet flows inside the network. A router connected to a functional IP is called an interface router.

Ex. 27 at II-113;

> The other important aspects of on-chip communication are the methods required to prepare resources to be integrated to the system. This includes methods to check whether the resource meets the physical, layout, electrical and timing constraints for integration. A wrapper or an interface needs to be added to the resource so that its internal working becomes transparent to the network and other resources in the network. We call this wrapper as Resource Network Interface (RNI).

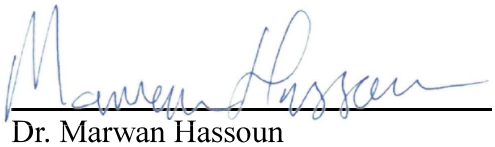
Ex. 23 at 94; *see also id.* at 197-98; Ex. 25 at 30 ("Given particular module *M*, we can devise a method to automatically synthesize an instance of a shell as a wrapper to encapsulate *M*."); Ex.

28 at 2 ("such processing cores require wrappers (the network interfaces) to be attached to the network terminals."). The inventors of the '800 Patent also use wrapper in this manner in their writings. Ex. 22 at 5 ("we present a modular NI architecture, which is split into a kernel, providing core functionality, and a number of shells to extend functionality, e.g., ***wrappers to provide an interface to existing bus protocols***") (emphasis added).

138. Plaintiff's construction selects one of the previously recited structures that "said first wrapper" and "said second wrapper" could be referring to. However, because there are multiple structures that "said first wrapper" and "said second wrapper" could be referring to based on the way the specification is written and would be understood by a POSITA, a POSITA would not be able to reasonably ascertain which of these structures "said first wrapper" and "said second wrapper" refer to. Based on the specification's disclosure of at least three functions performed by a wrapper and the claim's separate recitation of memory and interconnect module, it is my opinion that these terms are indefinite.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Dated: Oct 12, 2023



Dr. Marwan Hassoun

APPENDIX A

Curriculum Vitae

Dr. Marwan Hassoun
Tel. (978) 261-7404, Greater Boston, MA
E-mail: marwan@intellectualinspiration.com

Major Highlights

30+ years of High-Tech Industrial, Academic, Intellectual Property, Entrepreneurship, and Innovation Experience

- Consulting: Intellectual Property and Integrated Circuit Design

  Technical evaluation of IP portfolios; Expert witness for 30+ intellectual property, trade secret and technology dispute cases; Development of innovation and IP protection strategies for startups including development of new IP; Consulting with semiconductor companies on various design and strategic matters. Clients include Samsung, Texas Instruments, Qualcomm, Broadcom, MediaTek, STMicro, nVidia, Maxim, Marvell, HTC, ZTE, LG, Comcast, ViaSat, Huawei, Palo Alto Networks, Power Integration, Intellectual Ventures, RPX and Western Technology Ventures.

- Senior Vice President of Engineering at KeyEye Communication, Inc. Built and lead a team of 50+ Analog, DSP, Systems and Digital engineers distributed in Sacramento, Minneapolis, Florida, India and Australia to the development of industry's lowest power 10GBASE-T solution. The complex chip included custom DSP, 1Gsps 9-bit quad ADCs, 1Gsps 10-bit DACs, 3.2GHz PLLs and an IFFT/FFT custom ultra-low power processor for Echo/Next cancellation all operating as a single system. Also drove the intellectual property strategy, monetized the portfolio and directly involved in fund raising and M&A activities.

- Sr. Director of Engineering for the Communications Technology Division at Xilinx, Inc. This includes a team of 60+ engineers in Austin, Minneapolis, San Jose and Ames. Responsible for producing the high-speed serial Multi-Gigabit Transceiver technology in the platform FPGAs (Virtex Family) programmable to support over 10 different serial technologies. Producing 1st pass working silicon in extremely advanced process technologies using innovation in architecture, circuits, redundancy, calibration and error correction. Awarded innovation of the year award. Served on Patent Committee.

- President & Managing Partner in TraCHip, LLC, an intellectual property company and monetized various patent portfolios.

- Part of establishing and managing a startup company, RocketChips, INC (investor, partner and Vice President of Wired Products) from inception in 1997 till $280 Million acquisition. Managed multi-company and multi-country (Japan, India and US) IC design products as well as major customers including INTEL, SONY and OKI. Major products included cutting edge high-speed serial transceiver technology.

- Responsible for design of power management IC products and ASICs for mobile phones while consulting for Texas Instruments.

- 48 patents granted (36 US and 12 International) and 14+ pending (US and International) in the areas of multi-gigabit serial transceivers, Programmable Logic Devices (FPGAs), high-speed high-resolution ADCs and DACs, Memories, RFID, DSP filters, Power Management, Machine Automation and Networking.

- Over 70 technical publications in National and International Journals and Conferences.

- Tenured professor in Electrical and Computer Engineering, Chair of the VLSI group and Co-Founded the Analog and Mixed-Signal VLSI Design Center at Iowa State University. Served as Director of the Center. Attracted sponsorship for the Center from major companies that include Texas Instruments, Honeywell, Rockwell, RocketChips, Non-Volatile Electronics and VTC.

- Established, drove, participated and negotiated Intellectual Property Strategy at all positions since 1994.

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

EXPERIENCE

2003 – Present **Intellectual Property Consultant**
General Areas: All aspects of Integrated Circuits design and productization (Analog, Digital and Mixed-Signal), Memories, Wired Networking, Processors, RF
Technical evaluation of IP portfolios; Expert witness for intellectual property, trade secret and technology dispute cases; Development of IP protection strategy for startups including development of new IP through collaboration with companies' executives and engineers; Consulting with semiconductor companies on various design and strategic issues. This work since 2008 is done through Green Semiconductor, Inc. and Intellectual Inspiration. Clients include Samsung, Texas Instruments, Qualcomm, Broadcom, MediaTek, STMicro, nVidia, Maxim, Marvell, HTC, ZTE, LG, Comcast, ViaSat, Huawei, Palo Alto Networks, Power Integration, Intellectual Ventures, RPX and Western Technology Ventures.

Litigation experience since 2003 includes more than 23 cases retained as an expert witness. The work included testimony and expert reports on invalidity, validity, non-infringement and infringement as well as IPRs. The testimony included 11 depositions (some included 2 and 4 day depositions) and 4 court/hearing testimonies with at least 26 expert reports authored. List of cases and references will be furnished upon request.

Mar 08 – Present President, CEO and Founder
Green Semiconductor, Inc., Austin, TX and
Intellectual Inspiration, Boston, MA (moved to Boston Area June 2017)
IP and technology consulting firm.

June 2017 – Present **Mentor, MIT Sandbox Innovation Fund**
Massachusetts Institute of Technology, Cambridge, MA
Mentoring student groups on entrepreneurship, technology, organization and intellectual property strategies. Present workshops on technical innovation and intellectual property strategy for startups. Review funding proposals from aspiring startup groups out of MIT Sandbox.

Mar 03 – 2012 President & Managing Partner
TraCHip, LLC, Austin, TX
Private intellectual property company. Manage a portfolio of two patents.

Mar 08 – Mar 10 Chief Technology Officer
Abbey House Media, Austin, TX
Web commerce and software development startup focused on digital media including eBooks and Audio Books.

Oct 05 – March 08 Senior Vice President of Engineering
KeyEye Communications, Inc., Sacramento, CA
Managed and built an organization with 50+ team members (Analog, Systems, DSP, Digital, Verification, Physical Design) with an innovative, startup oriented, staffing strategy across several design sites (Sacramento, Minneapolis, India and Australia). The result is industry's lowest power 10GBASE-T single chip product. In addition to the management and the vision, had hands-on reasonability for the power architecture, modeling and execution.

Jul 01 – Oct 05 Senior Director of Engineering, Communications Technology Division

Xilinx, Inc., Austin, TX
Managed an organization with 60+ team members across 4 sites in analog, digital and mixed-signal IC design, modeling, application engineering, systems engineering, product characterization, product engineering, production test engineering, advanced technologies, layout, CAD and information technology.

- Organizational and technical vision for Xilinx's high-speed serial I/O and ASSP technologies (180nm, 130nm, 90nm, 65nm and 45nm generations). This includes contributing to the vision for UXPi, an industry initiative for evangelizing 10Gbps technology, and the driving of industry standards to support further products.
- Products: Virtex-II PRO X (2 family members), Virtex-4 (5 family members) and RocketPHY (3 non-FPGA family members).
- Technical marketing support for both the platform FPGAs and the ASSPs.
- Customer support and interaction for current and future products.
- Partnership development with several tier 1 and tier 2 companies for process technology, packaging, licensing, high-speed connectors, high-speed backplanes and design. Including establishing industry initiatives at OIF and IEEE committees.
- Involvement in all aspects of the production of IC design including quality assurance and reliability.
- Served on patent committee for the Company.
- Recipient of the innovation of the year award for the Virtex-II Pro X product.

Mar 01 – Jul 01 Co-Founder, President and CEO
MadMax Optics, Inc., Austin, TX
Co-Founded the company to produce revolutionary simulation software for the optical component industry. Opened the main design center in Hamden, CT. Guided the company through the seed round financing. This included putting together a 5 year business plan, prospectus and investor presentations.

Aug 98 – Feb 01 Vice President of Wired Products
RocketChips, INC., Austin, TX (Acquired by **Xilinx**, Inc. in Nov 2000)
Contributed to the technical, managerial, organizational and marketing leadership for the company's three design centers in Minneapolis (MN), Ames (IA) and Austin (TX). Directly responsible for approximately 35 employees in Wired.

- Products and IP: SERDES and PCS layers for Gigabit Ethernet (IEEE 802.3z, 802.3ab), 2.5Gbps products for serial backplane applications (including OC-48), 10Gbps (IEEE 802.3ae and OC-192), IEEE 1394 and high-speed high-resolution ADCs and DACs (80Ms/s – 250Ms/s).
- Involved with the company since its inception in January 1997 as an early investor and technical and product development through the Iowa State University research work.
- Managed multi-company and multi-country (Japan, India and US) projects as well as major customers including INTEL, SONY and OKI.

Aug 96 - Jul 98 **Contract IC Designer** (Cellular and wireless ICs - power management)
Mixed-Signal Products Group, **Texas Instruments**, Dallas, TX
Contract design for mixed-signal power management ASICs for cellular applications. Involved in the design, implementation and test of several high volume production integrated circuits (TPS202X, TPS203X, TPS204X, TPS208X and TPS209X).

Jun 95 - Jul 96 **Contract IC Designer** (Analog-to-Digital Converters)
Defense Systems & Electronics Group, **Texas Instruments**, Dallas, TX
Investigation and recommendation of a very high-speed high-resolution pipelined multi-path analog-to-digital converter architecture for communication applications.

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

Jan 85 - Jul 86 **Software Development Engineer**
Cupertino Integrated Circuits Division, **Hewlett Packard** Company,
Santa Clara, CA
Design, implementation and maintenance of circuit design analysis product (HPSPICE).

ACADEMIC EXPERIENCE

2000 – 2017 **Collaborating Professor**
Department of Electrical and Computer Engineering
Iowa State University, Ames, Iowa
- MS and PhD graduate students and serve on MS and PhD committees at ISU and at University of Texas, Austin.

1994 – 2000 **Associate Professor with Tenure**
Department of Electrical and Computer Engineering
Iowa State University, Ames, Iowa
(On leave of absence from Aug 98-Jul 00. Several leaves while consulting for Texas Instruments)

1988 - 1994 **Assistant Professor**
Department of Electrical and Computer Engineering
Iowa State University, Ames, Iowa

Research & Teaching

Hired in 1988 by ISU to start the VLSI area in the department. This included establishing research area in VLSI CAD (Symbolic Circuit Analysis, Synthesis Methods for Data Converters) and Analog and Mixed-Signal VLSI (Data Converters, Gigabit speeds Communication Circuits, Magneto-resistive devices).
The largest impact has been the establishment of industrial contacts and the founding of the Analog and Mixed-Signal VLSI Design Center. **The funding commitments on which Dr. Hassoun was a PI or Co-PI have grown to approximately $4.3 Million by 1998.**

EDUCATION

Jan 86 - Aug 1988 **Ph.D**. in *Electrical Engineering*, **Purdue University,** West Lafayette, IN.
Thesis: *Symbolic Analysis of Large-Scale Networks*
- Research Assistant (NSF grant) and a Teaching Assistant (VLSI area).

Jan 84 - Dec 1984 **M.S.** in *Electrical Engineering*, **Purdue University,** West Lafayette, IN.
Thesis: A *Study of a Semi-Direct Method for Computer Analysis of Large-Scale Circuits*
- Research Assistant (IBM grant).

Aug 80 -Dec 1983 **B.S.** in *Electrical Engineering*, **South Dakota State University,** Brookings, SD.
- Teaching assistant during senior year.
- Minor in Computer Mathematics and Computer Science

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

PATENTS

48 patents granted (36 US and 12 International) and 14+ pending (US and International) in the areas of multi-gigabit serial transceivers, high-speed high-resolution ADCs and DACs, Magnetic RAMs, RFID, DSP filters, Power Management, Machine Automation and Networking.

Granted US Patents:

1. Richard Willham, Robert Weber, Marwan Hassoun, "Livestock Record System," U. S. Patent No. **5,322,034**, June 21, 1994.
2. Richard Willham, Robert Weber, Marwan Hassoun, "Individual Descriptive Record System," U. S. Patent No. **5,499,626**, March 19, 1996.
3. Roy Hastings, Marwan Hassoun, Neil Gibson, Marco Corsi, "Capacitive-summing switch-mode power conversion control," U. S. Patent No. **6,066,943**, May 23, 2000.
4. William Black, Marwan Hassoun, "Non-volatile magnetic circuit," U. S. Patent No. **6,317,359**, November 13, 2001.
5. William Black, Bodhisattva Das, Marwan Hassoun, "Non-volatile spin dependent tunnel junction circuit," U. S. Patent No. **6,343,032**, January 29, 2002.
6. Yvette Lee, Marwan Hassoun, "Segmented DAC calibration circuitry and methodology," U. S. Patent No. **6,489,905**, December 3, 2002.
7. Yvette Lee, Marwan Hassoun, "Current source calibration circuit," U. S. Patent No. **6,507,296**, January 14, 2003.
8. William Black, Bodhisattva Das, Marwan Hassoun, Edward Lee, "Nonvolatile programmable logic devices," U. S. Patent No. **6,542,000**, April 1, 2003.
9. Weibiao Zhang, Marwan Hassoun, "Apparatus for and method of performing a conversion operation," U. S. Patent No. **6,563,444**, May 13, 2003.
10. Justin Gaither, Marwan Hassoun, "Analog Signal Test Circuit and Method", U. S. Patent No. **6,653,827 B2**, November 25, 2003.
11. Ahmed Younis, Marwan Hassoun, "Method and System for VCO-Based Analog-To-Digital Conversion (ADC)," U. S. Patent No. **6,809,676** B1, October 26, 2004.
12. Moises Robinson, Shahriar Rokhsaz, Marwan Hassoun, Earl Swartzlander, Jr, "Voltage Controlled Oscillator ", U. S. Patent No. **7,315,220**, January 1, 2008.
13. Moises Robinson, Marwan Hassoun, Earl Swartzlander, Jr, "Method and Apparatus for Capacitance Multiplication within a Phase Locked Loop", U. S. Patent No. **7,307,460**, Dec 11, 2007.
14. Marwan Hassoun, Moises Robinson, David Tetzlaff, "Method and Apparatus for Redundant Transceiver Architecture," U. S. Patent No. **7,408,380**, August 5, 2008.
15. David Tetzlaff, Erich Goetting, Steven Young, Marwan Hassoun, Moises Robinson, "Method and Apparatus for Providing Frequency Synthesis and Phase Alignment in an Integrated Circuit," U. S. Patent No. **7,499,513**, March 3, 2009.
16. David Tetzlaff, Marwan Hassoun, "Method and Apparatus for Dynamic Port Provisioning Within A Programmable Logic Device", U. S. Patent No. **7,598,768**, October 6, 2009.
17. James Little, Marwan Hassoun, David Tetzlaff, Chang-Chi Liu, "Combined echo and crosstalk cancellation," U. S. Patent No. **7,920,461**, April 5, 2011.
18. James Little, Marwan Hassoun, David Tetzlaff, Chang-Chi Liu, "Combined echo and crosstalk cancellation," U. S. Patent No. **8,488,438**, July 16, 2013.

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

19. Charles Studor, J. Kevin Nater, Marwan Hassoun, "System and method for managing the generation of brewed beverages using shared resources," U. S. Patent No. **8,515,574**, August 20, 2013.
20. Charles Studor, J. Kevin Nater, Marwan Hassoun, "Apparatus and method for brewed and espresso drink generation," U. S. Patent No. **8,688,277**, April 1, 2014.
21. James Little, Marwan Hassoun, David Tetzlaff, Chang-Chi Liu, "Combined echo and crosstalk cancellation," U. S. Patent No. **8,947,992**, February 3, 2015.
22. Charles Studor, Brent Clafferty, Stephen Miller, Marwan Hassoun, Pete Garcia, Lynn Hamrick, "Frothing assembly and method of operating the same," U. S. Patent No. **8,991,795**, March 31, 2015.
23. Charles Studor, J. Kevin Nater, Marwan Hassoun, "System and method for managing the generation of brewed beverages using shared resources," U. S. Patent No. **8,996,178**, March 31, 2015.
24. Charles Studor, Raymond Hudy, John Craparo, Marwan Hassoun, "Automated beverage generating system and method of operating the same," U. S. Patent No. **9,533,866**, January 3, 2017.
25. Charles Studor, J. Kevin Nater, Marwan Hassoun, "Automated beverage generation system and method of operating the same," U. S. Patent No. **9,545,170**, January 17, 2017.
26. Shahriar Rokhsaz, Brian Young, Marwan Hassoun, "Radio frequency identification (rfid) moisture tag(s) and sensors with extended sensing via capillaries," U. S. Patent No. **9,582,981**, February 28, 2017.
27. Shahriar Rokhsaz, Brian Young, Ahmed Younis, John Paulos, Abhay Misra, Benjamin Cooke, Marwan Hassoun, "Radio frequency identification (rfid) tag(s) and sensor(s)," U. S. Patent No. **9,607,188**, March 28, 2017.
28. Shahriar Rokhsaz, Brian Young, Ahmed Younis, John Paulos, Abhay Misra, Benjamin Cooke, Marwan Hassoun, "Radio frequency identification (rfid) tag(s) and sensor(s)," U. S. Patent No. **9,748,632** August 29, 2017.
29. Brian Young, Shahriar Rokhsaz, Ahmed Younis, Marwan Hassoun, "Power harvesting circuit and applications thereof," U. S. Patent No. **9,768,707**, September 19, 2017.
30. Charles Studor, Raymond Hudy, John Craparo, Marwan Hassoun, "Automated beverage generation system and method of operating the same," U. S. Patent No. **9,950,918**, April 24, 2018.
31. Shahriar Rokhsaz, Brian Young, Marwan Hassoun, "Radio frequency identification (rfid) moisture tag(s) and sensors with extended sensing via capillaries," U. S. Patent No. **10,069,205**, September 4, 2018.
32. John Craparo, Charles Studor, J. Kevin Nater, Jeffrey Mulhausen, Marwan Hassoun, "Facilitating beverage ordering and generation," U. S. Patent No. **10,043,226**, August 7, 2018.
33. Brian Young, Shahriar Rokhsaz, Ahmed Younis, Marwan Hassoun, "Power harvesting circuit and applications thereof," U. S. Patent No. **10,243,479**, March 26, 2019.
34. Shahriar Rokhsaz, Brian Young, Ahmed Younis, John Paulos, Abhay Misra, Benjamin Cooke, Marwan Hassoun, "Radio frequency identification (rfid) tag(s) and sensor(s)," U. S. Patent No. **10,243,255,** March, 26, 2019.
35. Charles Studor, Brent Clafferty, Stephen Miller, Marwan Hassoun, Pete Garcia, Lynn Hamrick, "Frothing assembly and method of operating the same," U. S. Patent No. **10,271,680**, April 30, 2019.

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

36. Charles Studor, Raymond Hudy, John Craparo, Marwan Hassoun, "Automated beverage generation system and method of operating the same," U. S. Patent No. **10,315,908**, June 11, 2019.

GRANTS AND CONTRACTS

-During academic career from 1988 – 1998, secured 25 research grants while at Iowa State University and as part of the Analog and Mixed-Signal VLSI Design Center totaling approximately **$4.3 Million** from 1988- 1998. The sponsors included: Texas Instruments, Honeywell, Rockwell, RocketChips, Computing Devices International, Control Data Corporation (CDC), Defense Advanced Research Projects Agency (DARPA), National Science Foundation, Carver Trust Foundation, US Department of Education, Center for Non-Destructive Evaluation

1. Co-Principal Investigator (with Black, W., Lee, E. and Geiger, R.), "Mixed-Signal Circuits Laboratory," Carver Trust Foundation, **$1,000,000** (includes $500,000 required matching from Iowa State University), August 1998 - July 2000.
2. Principal Investigator (with Geiger, R., Black, W. and Lee, E.), "Analog and Mixed-Signal Center Membership," Texas Instruments, Inc., **$1,000,000**, Jan 1998 - Dec 2000 (continuation of grant 9).
3. Co-Principal Investigator (with Black, W., Lee, E.K.F. and Geiger, R.), "High Density and Low-energy Magneto-resistive Memory Circuits," Honeywell, Inc. (DARPA), **$151,091**, Sep 1997 - Dec 1998.
4. Co-Principal Investigator (with Geiger, R., Black, W., Lee, K., Wright, C.), "Restructuring Basic Electronic Circuits Education Around Integrated Circuit Technology of the 1990s," National Science Foundation Instrumentation and Laboratory Infrastructure Program **$200,000,** Aug 1997 - Jun 1999.
5. Co-Principal Investigator (with Black, W., Geiger, R., Lee, E.), Honeywell, Inc**.** (DARPA), **$22,400,** "Testing of Magneto-resistive Structures," Feb 1997 - April 1997 (continuation of grant 8).
6. Co-Principal Investigator (with Black, W., Geiger, R., Lee, E, Bergland, D., Sapatnekar, S., Tridandapani, S. and Weber, R.), "Gigabit Silicon Integrated Circuits," RocketChips, Inc., **$1,000,000**, Jan 1997 - Dec 2001.
7. Principal Investigator, "Linear IC Product Design", Texas Instruments, Dallas, TX, **$110,000**, Sep 96 - Aug 97.
8. Co-Principal Investigator (with Black, W., Geiger, R., Lee, E., Honeywell, Inc. (DARPA), **$100,000**, "Magneto-resistive Memories," May 1996 - April 1997.
9. Co-Principal Investigator (with Geiger, R., Black, W., Hassoun, M., and Lee, E., Texas Instruments, Inc., **$450,000**, "Analog and Mixed-Signal Center Membership," Jan 1996 - Dec 1998.
10. Principal Investigator (with Geiger, R., Lee, E. and Black, W., Rockwell International Inc., **$300,000**, "Analog and Mixed-Signal Center Membership," Aug 1996 - Dec 1999.
11. Principal Investigator, "Verification of a Pipeline Analog to Digital Converter for Communication", Texas Instruments, Dallas, TX, **$10,017**, Jan 96 - Aug 96 (continuation of grant 11).
12. Principal Investigator, "Pipeline Analog to Digital Converter for Communication", Texas Instruments, Dallas, TX, **$27,755**, Aug 95 - Aug 96.
13. Principal Investigator, "An Investigation of a Pipelined Analog-to-Digital Converter", Texas

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

Instruments, Dallas, TX, **$37,105**, Jun 95 - Aug 95.
14. Co-Principal Investigator (with Richard Hester), "Low Power Analog-To-Digital Converter", Texas Instruments, Dallas, Texas, **$27,000**, Aug 93 - May 95.
15. Principal Investigator (with Jim Davis), "High Speed Multi-Protocol ActiveBus Prototype Development," Computing Devices International, Bloomington, Minnesota, **$2,500**, Aug 93-Dec 93 (continuation of grant 16).
16. Principal Investigator (with Jim Davis), "High Speed Multi-Protocol ActiveBus Prototype Development," Computing Devices International, Bloomington, Minn, **$15,000**, Aug 92-Aug 93.
17. Co-Principal Investigator (with V. Dalal, S. Burns, H. Hsieh, R. Weber, P. Garikepati), "Graduate Assistance in Microelectronics and Photonics," Department of Education, Washington, D.C., **$351,000**, Aug 90-Aug 93.
18. Principal Investigator, "Symbolic Analysis of Nonlinear Large-Scale Systems," Engineering Research Institute, Ames, Iowa, **$3,848**, Oct 92- Jul 93.
19. Faculty Associate (with Charles Wright, Jr.), "A laboratory to Support Computer-Aided Digital Systems Design," National Science Foundation Instrumentation and Laboratory Improvement Program, **$218,317**, Aug 90-Aug 92.
20. Principal Investigator, "Symbolic Sensitivity Analysis of Large-Scale Circuits," University Research Initiation Grant, Ames, Iowa, **$6,600**, Jul 91-Jun 92.
21. Principal Investigator, "Symbolic Circuit Simulation in the Time Domain," Engineering Research Institute, Ames, Iowa, **$4,240**, Oct 91- Jun 92.
22. Principal Investigator, "Application of VLSI Circuit Partitioning Technique to Dynamic Clustering of Distributed Multiprocessor Systems," Engineering Research Institute, Ames, Iowa, **$1,660**, Oct 90-Jun 91.
23. Co-Principal Investigator (with Art Pohm and Jim Davis), "Design of a New High Speed Serial Bus," Control Data Corporation (CDC), Minneapolis, Minnesota, **$114,000**, Aug 89-Dec 91.
24. Principal Investigator, "Investigation Proposal for Hardware Implementation of Non-Destructive Evaluation software," Center for Non-Destructive Evaluation, Ames, Iowa, **$5,000**, Aug 89-Jun 90.
25. Principal Investigator, "ASIC Hardware for Image Processing Applications," Engineering Research Institute, Ames, Iowa, **$4,000**, Oct 89- Jun 90.

GRADUATE STUDENTS

Major Professor for **26 Graduate Students** (8 PhDs and 20 *MS* (all thesis option)) from 1988 – 2005.

TECHNICAL PUBLICATIONS

Authored or co-authored over 70 technical publications in Technical Journals, Conferences and six chapters of three different books on circuit analysis.

Refereed Journals

1. Jorgenson, J., Hassoun, M., Hsu, H., "Breakdown Verification for Fault Modeling in Laminate Microstrip Conductors," *International Journal of Microelectronics and Electronic Packaging*.
2. Zhang, R., Hassoun, M., Black, W., Das, B, Wong, K, "Demonstration of a Sensing Four States From A Single Pseudo-Spin Valve GMR Device," *IEEE Transactions on Magnetics*.

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

3. Shah, J., Younis, A., Sapatnekar, S., Hassoun, M., “A New Method for the Analysis of Power and Ground Busses and its Symbolic Implementation," *IEEE Transactions on Circuits and Systems II*.
4. Hassoun, M. M., Black, W., Lee, K. F., and Geiger, R. L., “Field Programmable Logic Gates Using GMR Devices," *IEEE Transactions on Magnetics,* September 1997.
5. Hassoun, M. M. and Lin, P. M., "A New Method for Symbolic Analysis of Large-Scale Networks," *IEEE Transactions on Circuits and Systems I,* March 1995.
6. Ranmuthu, I., Ranmuthu, K., Pohm, A., Kohl, C., Comstock, C. and Hassoun, M., "A Sensing Scheme for Giant Magneto-Resistive Memories," *IEEE Transactions on Magnetics*, VOL 30, No. 5, September 1994.
7. Hassoun, M. M., Atawale, P., “Hierarchical Symbolic Analysis On A Ncube Multi-Processor," *Alta Frequenza* , (top Italian technical Journal in EE), *invited submission,* VOL 5, No. 6, December 1993, pp. 56-64.
8. Ranmuthu, K., Ranmuthu, I., Pohm, A., Comstock, C. and Hassoun, M., "High Speed (10-20ns) Nonvolatile MRAM with Folded Storage Elements," *IEEE Transactions on Magnetics*, VOL 28, No. 5, September 1992, pp. 2359-2361.
9. Hassoun, M. M. and McCarville, K., "Hierarchical Symbolic Signal-Flow Graph Analysis," *Journal of Analog VLSI and Signal Processing*, Kluwer Publishing, January 1993, pp. 31-42, *invited submission*.
10. Ranmuthu, I., Ranmuthu, K., Kohl, C., Comstock, C. and Hassoun, M., "A 512 Kbit Magneto Resistive Memory with Switched Capacitor Self Referencing Sensing Scheme," *IEEE Transactions on Circuits and Systems II*, VOL. 39, NO. 8, August 1992, pp. 585-587.
11. Ranmuthu, K., Ranmuthu, I., Pohm, A., Comstock, C. and Hassoun, M., "10-35 Nanosecond Magneto-Resistive Memories," *IEEE Transactions on Magnetics*, VOL. 26, No. 5, Sep 1990, pp. 2532-2534.
12. Ranmuthu, I., Ranmuthu, K., Pohm, A., Comstock, C. and Hassoun, M., "Reprogrammable Logic Array Using M-R Elements," *IEEE Transactions on Magnetics*, VOL. 26, No. 5, Sep 1990, pp. 2828-2830.

Refereed Proceedings Articles

13. Zhang, W., Hassoun, M., “A Redundant-Cell-Relay Continuous Self-Calibration Method for Current-Steering DACs,” European Solid-State Circuits Conference, Villach, Austria, September 2001.
14. Xia, H., Hassoun, M., “An analog self-calibration algorithm for multibit per stage pipelined Analog to Digital Converters,” Proceedings of the *Midwest Symposium on Circuits and Systems*, Dayton, OH, August 2001.
15. Chew, S., Hassoun, M., “Implementation, Verification and Synthesis of Gigabit Ethernet 1000BASE-T Physical Coding Sublayer,” Proceedings of the *Midwest Symposium on Circuits and Systems*, Dayton, OH, August 2001.
16. Liu, H., Hassoun, M., “High Speed Re-Configurable Pipeline ADC Cell Design,” *Southwest Symposium on Mixed-Signal Design*, Austin, TX, February 2001.
17. Younis, A., Navin, V., Hassoun, M., “A Calibration Algorithm for a 16-bit Multi-path Pipeline ADC,” Proceedings of the *Midwest Symposium on Circuits and Systems*, East Lancing, MI, August 2000.
18. Younis, A., Hassoun, M., “A High Speed Fully differential CMOS Opamp,” Proceedings of the *Midwest Symposium on Circuits and Systems*, East Lancing, MI, August 2000.

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

19. Zhang, W., Hassoun, M., "A Weighted Reduced Connectivity Matrix Partitioning Algorithm," Proceedings of the *Midwest Symposium on Circuits and Systems*, East Lancing, MI, August 2000.
20. Zhang, W., Hassoun, M., "A Small Signal Analysis of a Gain-Boosting Amplifier," *Southwest Symposium on Mixed-Signal Design*, San Diego, CA, February 2000.
21. Liu, H., Hassoun, M., "Components of a 12-bit 50 Ms/s Non-radix 2 Pipeline Analog-to-Digital Converter," Proceedings of the *Midwest Symposium on Circuits and Systems*, East Lancing, MI, August 2000.
22. Xia, H., Bataineh, K., Hassoun, M., Kryzak, J., " An Algorithm for Symbolic and Numeric Architecture Determination in a Knowledge-Based ADC Synthesis Environment using Fuzzy Membership Functions," *IEEE International Symposium on Circuits and Systems*, Orlando, FL, 1999.
23. Xia, H., Bataineh, K., Hassoun, M., Kryzak, J., " A Mixed-signal Behavioral Level Implementation of 1000BASE-X Physical Layer for Gigabit Ethernet," *IEEE International Symposium on Circuits and Systems*, Orlando, FL.
24. Zhang, W., Xia, H., Al-Omari, R., Hassoun, M., "Symbolic Synthesis Of Analog-to-Digital Conversion Architectures Using Direct-Mapping Techniques," *IEEE International Conference on Electronics, Circuits, and Systems*, Lisbon, Portugal, Oct 1998, Invited Paper.
25. Konczykowska, A., Hassoun, M. and Huelsman, L., "Applications Of Symbolic Methods To Circuit Design: An Overview," *IEEE International Symposium on Circuits and Systems*, Monterey, CA, May 1998.
26. Hassoun, M., and Lin, P-M., "A Formulation Method For Including Ideal Operational Amplifiers In Modified Nodal Analysis," Proceedings of the *Midwest Symposium on Circuits and Systems*, Sacramento, CA, August 1997.
27. Jin, H., Lee, K. F., Hassoun, M., "An Averaging Scheme for multi-path Analog-to-Digital Converters," Proceedings of the *IEEE International Symposium on Circuits and Systems*, Hong Kong, June 1997.
28. Venkata, N., Ray, T., Hassoun, M., Lee, K. F., Black, W., Soenen, E. and Geiger, R. L**.,** "A Simulation Environment for Pipeline Analog-to-Digital Converters," Proceedings of the *IEEE International Symposium on Circuits and Systems*, Hong Kong, June 1997.
29. Hassoun, M. M., Black, W., Lee, K. F., and Geiger, R. L., "Field Programmable Logic Gates Using GMR Devices," Proceedings of the *International Conf on Magnetics,* April 1997.
30. Echtenkamp, J. and Hassoun, M., "Implementation Issues for Symbolic Sensitivity Analysis," Proceedings of the *Midwest Symposium on Circuits and Systems*, Ames, Iowa, August 1996.
31. Hooton, T., O'Farrell, P., Dietrich, W., Salzman, J., Scott, K., Chang, C., Hassoun, M. and Rooks, J., "A 16-bit 25.6 MHz Self-Calibrating Analog-to-Digital Converter," Proceedings of the *Government Microelectronics Applications Conference*, Las Vegas, NV, March 1997.
32. Hassoun, M., Weber, R, Willham, R. and Greenfield, T., "A VLSI Prototype For A Remote Livestock Record System," Proceedings of the *Midwest Symposium on Circuits and Systems*, Rio De Janeiro, Brazil, August 1995.
33. Hassoun, M. and Huelsman, L., "Overview Symbolic Analysis Techniques for Large Analog Integrated Circuits," Proceedings of the *Midwest Symposium on Circuits and Systems*, Rio De Janeiro, Brazil, August 1995.
34. Echtenkamp, J., Hassoun, M., Prabhu, G. and Wright, C., "Symbolic Sensitivity Analysis Method for SCAPP ," 1995 *European Conference on Circuit Theory and Design,* Davos, Switzerland, September 1995, *invited paper* .
35. Hassoun, M. and Huelsman, L., "Overview Symbolic Analysis Techniques for Large Analog

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

Integrated Circuits," *IEEE International Symposium on Circuits and Systems*, Seattle, WA, May 1995, *invited paper* (paper was presented but did not appear in the proceedings due to a clerical error, see R27).

36. McCarville, K., Hassoun, M., "Symbolic Simulation of Semiconductor Devices in SCAPP," Proceedings of the *Midwest Symposium on Circuits and Systems*, Lafayette, LA, August 1994.
37. Hassoun, M., Fernández, F., Gielen, G., Huelsman, L., Konczykowska, A., Manetti, S., Sansen, W. and Vlach, Jiri, "Pleasures, Perils and Pitfalls of Symbolic Analysis," Proceedings of the *IEEE International Symposium on Circuits and Systems*, London, England, June 1994, pp. 1.451-1.457.
38. Greenfield, S., Hassoun, M., "Direct Symbolic Transient Analysis Using Approximate Integration Formulae," Proceedings of the *IEEE International Symposium on Circuits and Systems*, London, England, June 1994, pp. 1.29-1.36.
39. Alspaugh, B., Hassoun, M., "A Mixed Symbolic and Numeric Method for Closed-Form Transient Analysis ," 1993 *European Conference on Circuit Theory and Design,* Davos, Switzerland, September 1993, pp. 1687-1692, *invited paper*.
40. Hassoun, M., Atawale, P., "Symbolic Analysis of Large-Scale Network on Multi-Processor Systems," 1993 *IEEE International Symposium on Circuits and Systems,* Chicago, May 1993, pp. 1651-1654.
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   Editors: A. Rodríguez-Vázquez, F. Fernández & J. Huertas.
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   Editor: Wai-Kai Chen
   Publisher: *CRC Press*, 2009.

INVITED TECHNICAL PRESENTATIONS

Over 40 technical presentations at various conferences, workshops and companies, including workshops at MIT, Texas A&M, University of Texas at Austin, and Iowa State University, Innography, HP, Texas Instruments, Rockwell International, Honeywell, CDC, and Non-

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

Volatile Electronics.

HONORS AND AWARDS

Recipient: Distinguished Engineer Award, South Dakota State University
Recipient: Innovation of the year award, Xilinx, Inc.
Nominee: Iowa State University Faculty of the Year award
Inductee: Senior member Institute of Electrical and Electronics Engineers (IEEE)
Recipient: Warren Bost Teaching Award, Iowa State University
Nominee: ISU Foundation Early Teaching Achievement Award
Nominee: ISU Foundation Early Teaching Achievement Award
Inductee: Eta Kappa Nu (Electrical Engineering Honor Society)
Inductee: Tau Beta Pi (Engineering Honor Society)
Inductee: Phi Kappa Phi (National Honor Society)
Inductee: Alpha Lambda Delta (Freshman Honor Society)

PROFESSIONAL ACTIVITIES

Standards – Participant and voter on IEEE 802 Standards Committee (802.3 group).
Conferences & Workshops – Served as conference chair, on technical program committees, on organizing committees, publicity chair, special sessions chair and steering committees for more than 20 occasions covering more than 7 conferences and workshops.

Reviewer – Editor and Referee for IEEE, IEE and other journals in the area of VLSI and circuits and systems.

Network System Technologies Ex. 2083
Qualcomm v. Network System Technologies - IPR 2024-00343

APPENDIX B

Materials Considered

Patents-in-Suit and Litigation Documents:

U.S. Patent No. 7,366,818 (Ex. 2)

U.S. Patent No. 7,373,449 (Ex. 3)

U.S. Patent No. 7,594,052 (Ex. 4)

U.S. Patent No. 7,769,893 (Ex. 5)

U.S. Patent No. 8,072,893 (Ex. 6)

U.S. Patent No. 8,086,800 (Ex. 7)

File History for U.S. Patent No. 7,366,818

File History for U.S. Patent No. 7,373,449 (Portions of which are included as Exs. 10-12)

File History for U.S. Patent No. 7,594,052

File History for U.S. Patent No. 7,769,893

File History for U.S. Patent No. 8,072,893

File History for U.S. Patent No. 8,086,800 (Portions of which are included as Exs. 16-20)

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Zeferino et al., *SoCIN: A Parametric and Scalable Network-on-Chip* (Ex. 28)

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Radulescu et al., *An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration* (Ex. 22)

Anjo et al., *Wrapper-Based Implementation Techniques for Performance Improvement and Cost Reduction* (Ex. 24)

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Rijpkema et al., *Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip*

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Excerpts from Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, 2d Ed.

Dally and Towles, *Route Packets, Not Wires: On-Chip Interconnection Networks*

Gebali et al., *Networks-On-Chip: Theory and Practice*

Any materials or references cited in my report that are not otherwise listed here

APPENDIX C

Below is a list of all cases in which, during the previous 4 years, Dr. Marwan Hassoun testified in as an expert at trial or by deposition:

- *Parthenon Unified Memory Architecture LLC v. HTC Corporation et al.*, Case No. 14-cv-691, filed June 12, 2014, in the U.S. District Court for District of Delaware (on behalf of HTC, LG Electronics, and ZTE USA).
- *Maxell, Ltd. v. Huawei Device USA Inc. et al.*, United States District Court for The Eastern District of Texas, Case No. 5:16-cv-00178-RWS, (on behalf of Huawei, Inc.)
- *Optis Wireless Tech, LLC, v. Huawei Device USA Inc. et al.*, United States District Court for The Eastern District of Texas, Case No. 2:17-cv-00123-JRG, (on behalf of Huawei, Inc.)
- *Power Integration, Inc. v. On Semi Corp., Northern District of CA*, Case No. 5:16-cv-06371-BLF and Case No. 3:17-cv-03189 BLF (on behalf of Power Integration, Inc.)
- Certain Movable Barrier Operator Systems and Components Thereof (Chamberlain Group, Inc.), International Trade Commission, ITC Inv. No. 337-TA-1209. (on behalf of Chamberlain Group, Inc.)
- On behalf of Xilinx Inc., IPR2020-01531
- On behalf of Monterey Research, LLC, IPR2021-00170
- Certain Integrated Circuits and Products, *MediaTek. v. NXP et al.*, (Inv. No. ITC 337-TA-1272) (on behalf of MediaTek, Inc.)
- Certain Integrated Circuits and Products, *MediaTek. v. NXP et al.*, (Inv. No. ITC 337-TA-1278) (on behalf of MediaTek, Inc.)