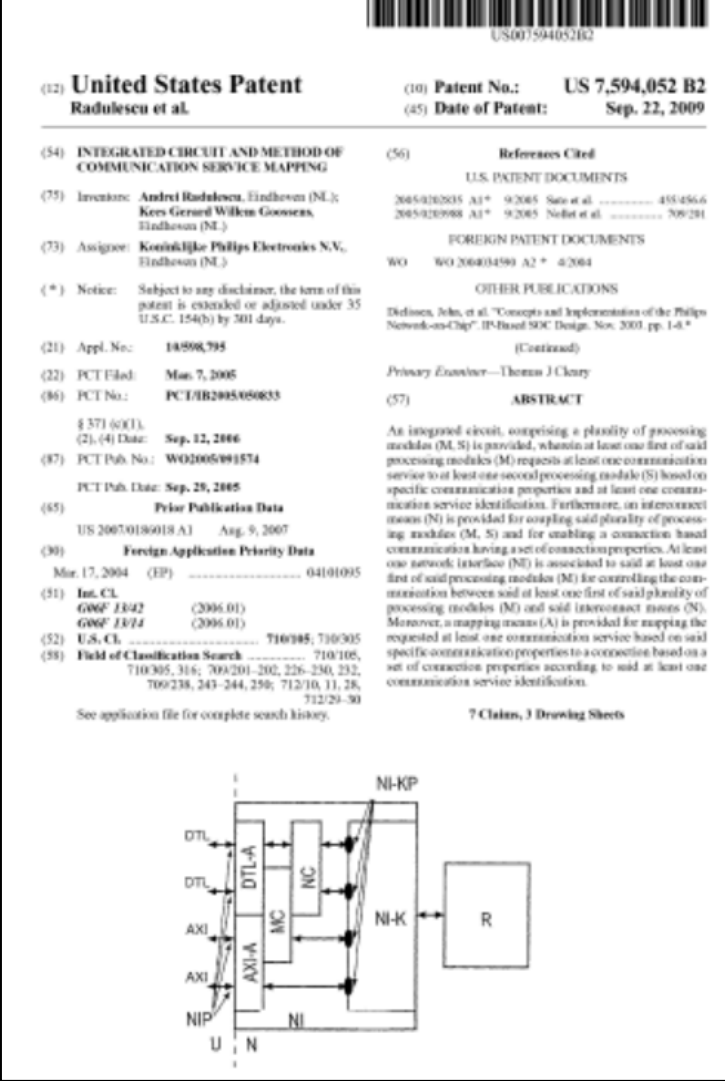


Qualcomm Incorporated
v.
Network System Technologies, LLC

IPR2024-00343
U.S. Patent No. 7,594,052

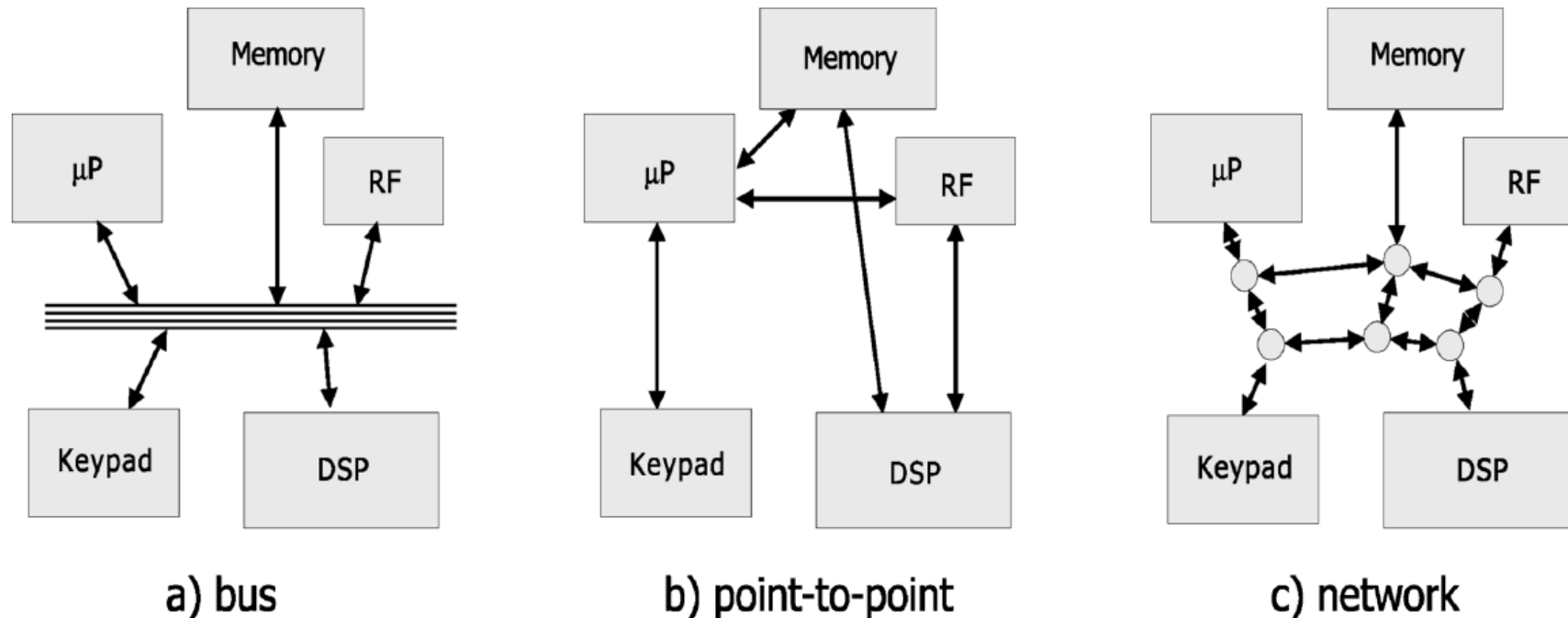
Patent Owner's Demonstrative Exhibit

'052 Patent –
Integrated Circuit and
Method of
Communication Service
Mapping



Technical Background

On-Chip Communication Structures



EX2073, 8 ; EX2070, ¶1122; EX1001, 1:14-25

'052 Patent Overview – “mapping”

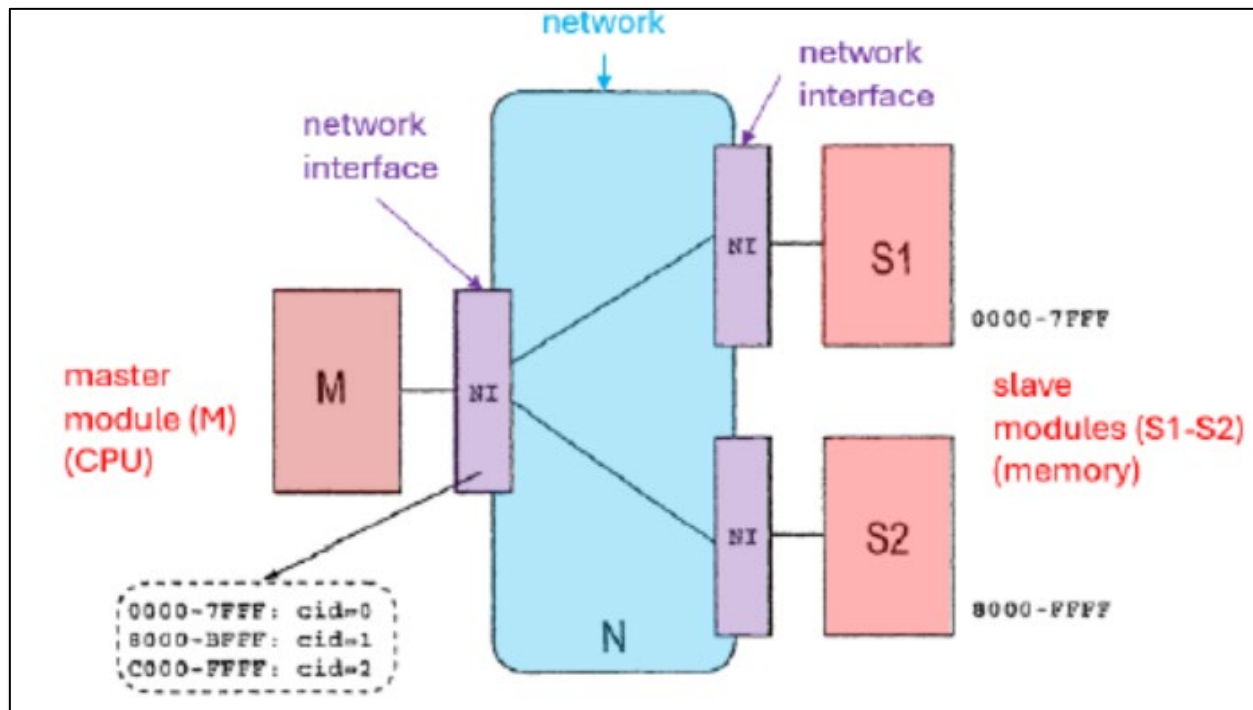
Summarizing it can be said, that the above described mapping is relevant for communication protocols which do not include the notion of connection, but are implemented with an interconnect supporting connections (e.g., AEthereal network on chip). The advantage is that it enables the use of connections for protocols without the notion of connection, allowing the configuration of differential services for different traffic classes. Backward compatibility of on-chip networks is achieved, by means of the adaptor units/shells to enable exiting protocols, such as DTL, AXI and OCP, to use differential services as offered by a connection based interconnect, such as an on-chip network.

EX1001, 8:47-58

Therefore, a system may be provided comprising a plurality of components communicating via a communication facility which at least comprises some identification means to identify the address of a destination and may additionally comprise thread information. In addition, the system comprises a mapping facility to map a range of addresses or a thread information to connection data. The connection data comprises specifications for data transport such as best effort or guaranteed throughput, the maximum allowed jitter, the maximum allowed latency, flow control Y/N, or ordering Y/N. If a message is sent to a particular address range in the system, or belongs to a particular thread, a connection is assigned to assure that the message is transmitted via a particular set of transmission requirements.

EX1001, 8:59-9:5

'052 Patent Overview – “mapping”



EX1001, FIG. 4

FIG. 4 shows a basic block diagram of a network on chip for illustrating the operation of the mapping of IP block communication via address ranges to connections. The network on chip comprises a master M and two slaves S1, S2 each being connected to a network via a network interface NI, respectively. The two slaves S1, S2 are implemented as memories, wherein the first slave S1 comprises the address range 0000-7FFF and the second slave S2 comprises the address range 8000-FFFF. Accordingly, the network interface NI associated to the master M may map the communication to the first slave S1, i.e. to the address range 0000-7FFF, to a connection with the connection id cid=0 and the communication to the second slave S2, i.e. to the address range 8000-FFFF, to a connection with the connection id cid=1.

Hence, protocols where there are no communication threads (e.g., DTL, MTL), address ranges can be mapped to specific connections. An address range can identify one or more slave modules, or a memory region within a slave module, e.g. a buffer used in some particular communication.

Ground 3: Petitioner Has Not Shown That Weber Anticipates Any Challenged Claim

Claim Construction

CLAIMS 1, 7

“MAPPING MEANS (A)”

Independent Claims 1, 6, and 7

Claim 1

1. Integrated circuit, comprising:
 a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification,
 an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a connection based communication having a set of connection properties,
 at least one network interface (NI) associated to said at least one first of said processing modules for controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N), and
 a mapping means (A) for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S).

Claim 7

7. Data processing system, comprising
 a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S),
 an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a connection based communication having a set of connection properties,
 at least one network interface (NI) associated to said at least one first of said processing modules for controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N), and
 a mapping means (A) for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.

Petitioner's "Mapping Means" Construction

Term	Petitioners' Proposed Construction
"mapping means"	Subject to § 112, ¶ 6 Function: mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification Structure: adapter unit including a sequentializer unit and a desequentializer unit

Petitioner's "Mapping Means" Construction

Petitioner's construction requires a "desequentializer"

The Petition

B. "mapping means" (claims 1, 7)⁴

"Mapping means" is presumptively governed by Section 112, ¶ 6. Claims 1 and 7 recite the following as the function for "mapping means":

mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.

The '052 patent indicates that an adapter unit performs this function. Ex-1001, *Id.*, Figs. 2A–B. These adapter units include a sequentializing unit "seq" and a desequentializing unit "deseq." *Id.*, 6:39–53. The '052 patent describes that these

Petition, 11-13

Dr. Hassoun's First Deposition

Q. In your construction of mapping means are the sequentializer and desequentializer required?

A. Yes, that's the structure.

Q. So to practice the claimed mapping means you would need a sequentializer and a desequentializer; is that right?

A. Yes, you would. That is part of the structure.

EX2068, 62:16-23

Patent Owner's Response

FIGs. 1, 2A, and 2B." *Id.* Patent Owner applies Petitioner's construction for purposes of this proceeding because Petitioner failed to meet its burden under this construction. *Infra*, §VIE.2; EX2070, ¶¶130-131.

POR, 23-24

POR, 23-24; POSR, 15-16

Ground 3: Purported Anticipation by Weber

WEBER DOES NOT DISCLOSE THE
CLAIMED “MAPPING MEANS”
(CLAIMS 1-5, 7)

Weber Does not Disclose a “Mapping Means”

Weber does not disclose a “desequentializer” under Petitioner’s construction

Petition

means. Ex-1003, ¶¶223-225.. As discussed above, the ‘052 patent describes that the mapping is performed by adapter units, also referred to as “shells,” that include a sequentializer and a desequentializer. *Supra* V.B. Weber’s interface module, which performs the claimed mapping, is such an adapter unit. Ex-1003, ¶¶223-225. Like the ‘052 patent’s adapters, Weber’s interface modules convert requests received from initiator functional blocks into the message format of Weber’s interconnect. *Id.* For example, Weber describes that the separate command (Cmd), address (Addr), and data (DataOut) signals that the interface modules receive from are initiator functional blocks are “multiplexed” on the shared communication bus and share the same wires. Ex-1007, [0036], [0050]. *Id.* A POSA would have understood that this multiplexing is performed by the interface modules, and that it is the same as or equivalent to the “sequentialize[r]” of the ‘052 patent’s adapter/shell units. *Id.*; Ex-1001, 6:48–51.

Petition, 66

Dr. Bagherzadeh

231. Dr. Hassoun opines that because Weber discloses that it capable of “multiplexing,” Weber discloses the structure of the claimed “mapping means.” Ex. 1003 at ¶ 225. I disagree. First, Dr. Hassoun fails to opine that Weber contains both a sequentializing unit and a desequentializing unit, as required under Petitioner’s proposed claim construction. Dr. Hassoun opines that Weber’s disclosure of “multiplexing” is analogous to the ‘052 Patent’s disclosure of “sequentializing.” *Id.* But Dr. Hassoun does not specifically identify a structure in Weber that multiplexes the signals sent from Weber’s functional units and that performs the function of the sequentializing unit. *Id.* Additionally, Dr. Hassoun fails to identify any purported desequentializing structure or function in Weber. *Id.* A POSITA would understand that Weber does not disclose a desequentializing unit because once signals are multiplexed, there is no reason to de-multiplex them.

EX2070, ¶1231

POR, 57-59; POSR, 15-16

Weber Does not Disclose a “Mapping Means”

Weber does not disclose a “desequentializer” under Petitioner’s construction

Reply

D. Weber Discloses the Mapping Means Structure (Claims 1-5, 7)

PO does not dispute that the structure in the ‘052 patent corresponding to the claimed mapping means is the adapter unit, or that Weber’s interface module is an adapter unit. Paper 3, 11, 66; Paper 38, 23-24, 57-59. While PO raises arguments based on sequentializing and desequentializing units within the adapter unit, PO does not argue that such sequentializing or desequentializing units are required for a mapping means. Even if disclosure of those units were required, Weber discloses the same amount of structure as the ‘052 patent. Ex-1030, ¶¶61-64.

Reply, 25

Ground 3: Purported Anticipation by Weber

WEBER DOES NOT DISCLOSE THE
CLAIMED “INTERCONNECT
MEANS” (CLAIMS 1-7)

Claim Construction

CLAIMS 1, 6-7
“INTERCONNECT MEANS (N)”

Independent Claims 1, 6, and 7

Claim 1

1. Integrated circuit, comprising:
 a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification,
 an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a connection based communication having a set of connection properties,
 at least one network interface (NI) associated to said at least one first of said processing modules for controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N), and
 a mapping means (A) for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S).

Claim 6

6. Method of communication service mapping in an integrated circuit, having a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S), comprising the steps of:
 coupling said plurality of processing modules (M, S) by an interconnect means (N) and
 enabling a connection based communication having a set of connection properties,
 controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N) by at least one network interface (NI) associated to said at least one first of said processing modules,
 mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.

Claim 7

7. Data processing system, comprising
 a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S),
 an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a connection based communication having a set of connection properties,
 at least one network interface (NI) associated to said at least one first of said processing modules for controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N), and
 a mapping means (A) for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.

“Interconnect Means”

18

Term	Petitioners’ Proposed Construction	Patent Owner’s Proposed Construction
“interconnect means”	Subject to § 112, ¶ 6 Function (claim 6): coupling said plurality of processing modules (M, S). Function (claims 1 and 7): the function of claim 6 plus enabling a connection based communication having a set of connection properties Structure: any of a bus, switch, point-to-point wire, or network. Petition at 10.	“multi-hop interconnection between modules separated by one or more network nodes” If subject to § 112, ¶ 6 Function (claims 1, 6, and 7): coupling said plurality of processing modules (M, S). Function (claims 1 and 7): enabling a connection based communication having a set of connection properties Structure: multi-hop interconnection between modules separated by one or more network nodes

“Interconnect Means” is Not a Means-Plus-Function Term

19

A POSITA would understand that “interconnect means” is a name for structure

Dr. Bagherzadeh

103. The term “interconnect means” as used in the ‘052 Patent would be understood by a POSITA to have a sufficiently definite meaning as the name for structure. This is because the specification uses the terms “interconnect means” and “network” interchangeably. A POSITA would understand that a “network” is a structure. I also understand the Board’s Institution Decision found that the corresponding structure for the “interconnect means” is a network. Institution Decision at 18.

EX2070, ¶ 103

Dr. Hassoun’s First Deposition

Q. So for purposes of your declaration, you've assumed that the term "interconnect means" is a means-plus-function term, correct?

A. I have done that and I also rendered opinion on NST's construction as well.

Q. Okay. Just to be clear, so you have assumed that the term "interconnect means" is means-plus-function. You are not offering an opinion that it is a means-plus-function term, correct?

A. That is correct.

EX2068, 47:25-48:11

“Interconnect Means” District Court Construction

20

A district court has construed “interconnect means” as “multi-hop interconnection between modules separated by one or more network nodes”

Case 2:22-cv-00482-RWS Document 150 Filed 01/03/24 Page 1 of 60 PageID #: 4362

IN THE UNITED STATES DISTRICT COURT FOR THE EASTERN DISTRICT OF TEXAS MARSHALL DIVISION

NETWORK SYSTEM TECHNOLOGIES,
LLC,

Plaintiff,

v.

TEXAS INSTRUMENTS
INCORPORATED,

Defendant.

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CIVIL ACTION NO. 2:22-CV-00482-RWS

CLAIM CONSTRUCTION ORDER

Before the Court is Plaintiff Network System Technologies, LLC’s (“Plaintiff” or “NST”) Claim Construction Opening Brief (Docket No. 98),¹ Defendant Texas Instruments Inc.’s (“Defendant” or “TI”) Responsive Claim Construction Brief (Docket No. 107), and Plaintiff’s Claim Construction Reply Brief (Docket No. 110). Also before the Court are the parties’ Joint Claim Construction and Prehearing Statement (Docket No. 84) and the parties’ Joint Claim Construction Chart (Docket No. 115).

The Court held a claim construction hearing on November 8, 2023, to determine the proper construction of the disputed claim terms in U.S. Patent Nos. 7,366,818 (“’818 Patent”), 7,373,449 (“’449 Patent”), 7,594,052 (“’052 Patent”), 7,769,893 (“’9893 Patent”), 8,072,893 (“’2893 Patent”), and 8,086,800 (“’800 Patent”) (collectively, “the Asserted Patents”). Docket No. 135. Shortly before the start of the November 8, 2023 hearing, the Court provided the parties with

EX2022, 1

The Court finds that the term “interconnect means” should be construed the same as the term “network.” First, the patentees used the term “interconnect means” and the term “network” interchangeably in the specification. The specification and claims identify the “network” and “interconnect means” as “N.” ’052 Patent at Abstract (“interconnect means (N)”), 5:13–24 (“network N”), 6:62 (“network N”); 10:25 (“interconnect means (N)”).

EX2022, 47

The specification further contrasts “[u]sing networks for on-chip communication when designing systems on chip (SoC)” to “existing on-chip interconnects (e.g., buses, switches, or point-to-point wires), where the communicating modules are *directly* connected.” ’052 Patent at 1:48–54 (emphasis added); *see also* ’818 Patent at 1:51–57. The specification discloses that “in a NoC the modules communicate remotely via network nodes.” ’052 Patent at 1:48–54; *see also* ’818 Patent at 1:51–57. The specification further describes a number of differences between NoC and off-chip networks. ’052 Patent at 1:54–2:31; ’818 Patent at 1:57–3:35. Importantly, the specification describes the recited “network” as a “radical change” by using the claimed networks as on-chip interconnects. Specifically, the specification states the following:

EX2022, 50

POR, 15-16

The “Interconnect Means” is a Network

The specification teaches that the interconnect is embodied as a network on chip

Dr. Hassoun

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following embodiments relate to systems on chip, i.e. a plurality of modules on the same chip (including e.g. system in a package, multi-die modules) or on different chips, communicate with each other via some kind of interconnect. The interconnect is embodied as a network on chip NOC, allowing communication between all aforementioned modules. The network on chip may include wires, bus, time-division multiplexing, switches, and/or routers within a network. At the

EX1001, 4:40-50

Q. So here the specification is teaching that the interconnect in the '052 patent is embodied as a network on a chip, correct?

A. Yes.

EX2068, 50:9-19

Dr. Bagherzadeh

109. The specification also repeatedly refers to the “interconnect means” or “interconnect” as a network. For example, the specification teaches that “[t]he interconnect is embodied as a network on chip NOC, allowing communication between all aforementioned modules.” Ex. 1001 at 4:46-50. The Description of the Invention section describes networks as the interconnect means. Ex. 1001, 5:7-31, 6:56-64, 7:25-28, 8:9-12, 8:54-58.

EX2070, ¶¶ 109-110

POR, 16-18, POSR 2

The “Interconnect Means” is a Network

The specification distinguishes NoCs from Direct Interconnects (e.g., bus, and wires)

Introducing networks as on-chip interconnects radically changes the communication when compared to direct interconnects, such as buses or switches. This is because of the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes. This is in contrast with the prevalent existing interconnects (i.e., buses) where modules are directly connected. The implications of this change reside in the arbitration (which must change from centralized to distributed), and in the communication properties (e.g., ordering, or flow control).

EX1001, 2:31-42

relatively independent, complex modules. In conventional processing systems the systems modules usually communicate to each other via a bus. As the number of modules increases however, this way of communication is no longer practical for the following reasons. On the one hand the large number of modules forms a too high bus load. On the other hand the bus forms a communication bottleneck as it enables only one device to send data to the bus.

A communication network forms an effective way to overcome these disadvantages. Networks on chip (NoC) have

EX1001, 1:25-34

Using networks for on-chip communication when designing systems on chip (SoC), however, raises a number of new issues that must be taken into account. This is because, in contrast to existing on-chip interconnects (e.g., buses, switches, or point-to-point wires), where the communicating modules are directly connected, in a NoC the modules communicate remotely via network nodes. As a result, intercon-

EX1001, 1:48-54

Case Law Requires Construing “Interconnect Means (N)” as a Network

23

Petitioner does not address or distinguish case law supporting Patent Owner’s construction

SciMed Life Sys. v. Advanced Cardiovascular Sys.,
242 F.3d 1337, 1343 (Fed. Cir. 2001)

“Thus, the SciMed patents distinguish the prior art on the basis of the use of dual lumens and point out the advantages of the coaxial lumens used in the catheters that are the subjects of the SciMed patents. That discussion in the written description supports the district court’s conclusion that the claims should not be read so broadly as to encompass the distinguished prior art structure”

Openwave Sys. v. Apple Inc.,
808 F.3d 509, 517 (Fed. Cir. 2015)

The specification repeatedly and clearly distinguishes the invention of the patents-in-suit from more powerful—and therefore more costly—mobile devices in combination with “computer modules.” . . .

In this case, however, it is difficult to envisage how, in light of the repeated disparagement of mobile devices with “computer modules” discussed above, one could read the claims of the patents-in-suit to cover such devices. We agree with the district court that they do not.

A “Network” is a Multi-Hop Interconnect Separated by One or More Network Nodes

Specification

Introducing networks as on-chip interconnects radically changes the communication when compared to direct interconnects, such as buses or switches. This is because of the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes. This is in contrast with the prevalent existing interconnects (i.e., buses) where modules are directly connected. The implications of this change reside in the arbitration (which must change from centralized to distributed), and in the communication properties (e.g., ordering, or flow control).

EX1001, 2:31-42

Petitioner’s District Court Construction for “Network”

'818	1-2	“network”	“Multi-hop interconnection between modules separated by one or more network nodes”
'449	10-12		
'9,893	14		
'2,893	4, 11		
'800	12		

EX1016, 13

A “Hop” Requires Traversing a Network Node

Institution Decision

To the extent that Patent Owner’s proposed construction remains relevant at trial or is included in the proposed structure of a means-plus-function construction of interconnect means, further discussion and evidence of what a “hop” entails and whether the cited portions of Weber disclose the requisite hops would be helpful.

Paper 11, 43

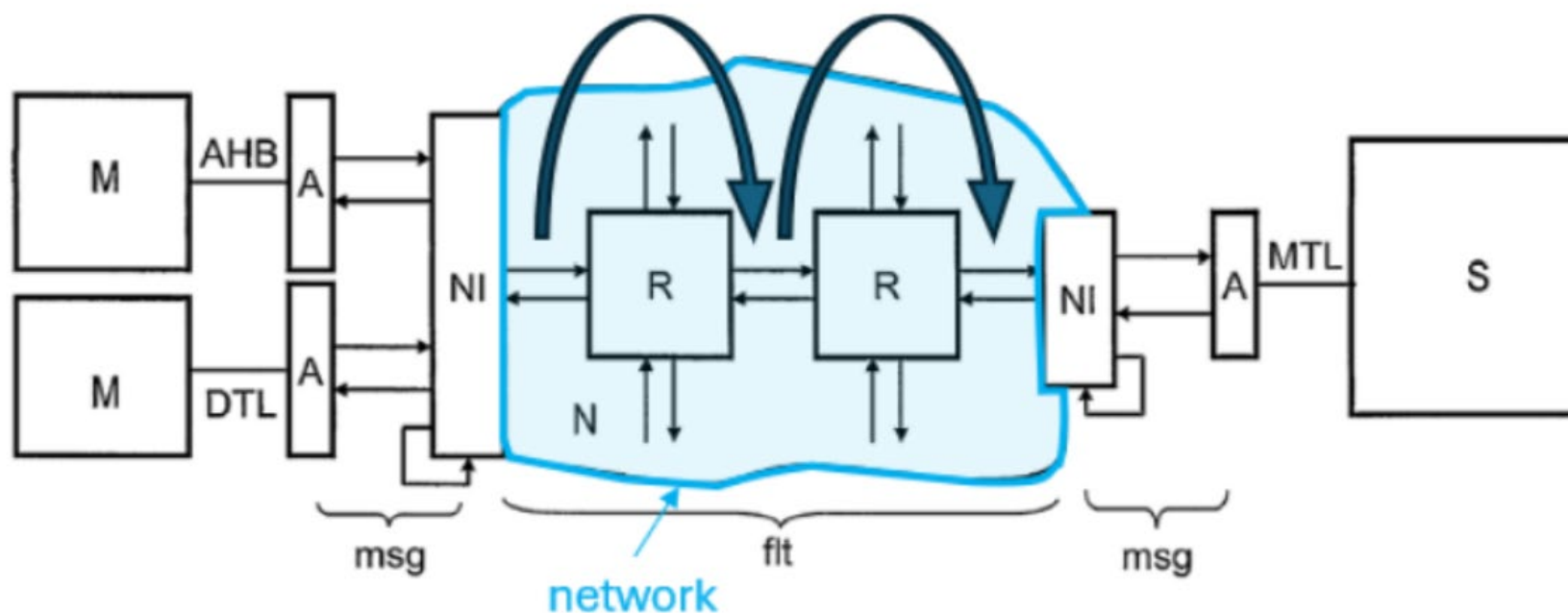
Dr. Bagherzadeh

114. A “multi-hop network” (i.e., a “interconnect means”) is a type of interconnect where data is transmitted from a source to a destination through one or more intermediate routers or switches, or “hops.” A POSITA would understand that a “hop” is a router/switch that a packet originating from an arbitrary protocol may traverse. See Ex. 2005 at 4 (“At each hop, the packet moves from one link to

EX2070, ¶ 114

A “Hop” Requires Traversing a Network Node

The network N in FIG. 1 includes at least two hops



EX1001, FIG. 1 (annotated)

A “Hop” Requires Traversing a Network Node

Dr. Hassoun initially agreed with Patent Owner’s definition of a “hop”

Dr. Hassoun’s First Deposition

When a packet travels from a first network node to a second network node is that a hop?

A. If I understand your example correctly, what you described is a direct connection between one network node to another network node.

Q. So that wouldn’t be a hop?

A. If it’s going directly from one node to another node, then it’s not a hop. That’s – that’s the distinction.

Q. Okay. So if the network had a router and the packet traveled from a first network node to the router and then from the router to a second network node, is that a hop?

A. Yes, the router would be a hop.

Q. So the router itself is the hop or is it the communication traveling between the first node through the router to the second node the hop?

A. The network node that you used in your example, which is the router, provides the hop.

Dr. Hassoun’s Second Declaration

18. From the general understanding in the art, a POSA would understand that a “hop” is a communication link with a node on each end. Webster’s Telecom Dictionary of 2008 defines hop in a similar manner. Ex. 1051, 6 (“In networks, the journey a signal makes across a transmission link between two devices such as bridges, hubs, switches, or routers.”). Each link in an interconnect having a node on each end is a hop. When data traverses from one node across a link to another node, it is said to have “hopped.” Thus, each node of an interconnect creates an additional hop from a master to a slave. If there are zero nodes between a master and a slave, i.e. the master and slave are directly connected, there is a single hop. If

EX1030, ¶18

A “Hop” Entails Packet-Based Communication

Unlike buses, NoCs transmit packets

Dr. Bagherzadeh

118. Another fundamental aspect of a multi-hop network is that it transports “data packets” (or “packets”) along each hop. *See* Ex. 2005 at 4 (“At each hop, the packet moves from one link to another.”); *see also* Ex. 2073 (“packet ... keeps hopping from router to router ...”). A packet is a bundle of data that is transmitted over a network according to specific protocols, some of which include TCP/IP (specific to computer networks, i.e., the Internet) and NTP (specific to NoCs, i.e., on-chip networks).

EX2070, ¶ 118; *see also* EX1050, 14:23-15:20

Dr. Hassoun’s First Deposition

A network on a chip, packets are transmitted over the network, right?
A. Yes.

EX2068, 27:8-28:1

A “Hop” Entails Packet-Based Communication

Patent Owner's definition is supported by the specification and extrinsic evidence

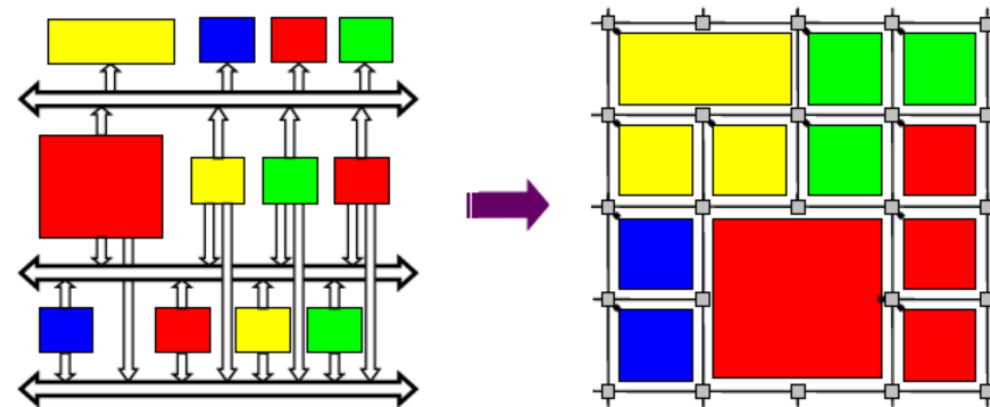
The network N may be comprised of a plurality of interconnected network routers R. The routers R can be randomly connected amongst themselves (multiple links between routers are also possible) and to the network interfaces (i.e., there are no topology constraints). The routers R transport packets of data from one network interface NI to another. Such a packet consists of one or more flits, where a flit is the minimal transmission unit.

EX1001, 5:24-31

The network interfaces NI are responsible for packetization/depacketization, for implementing the connections and services, and for offering a standard interface (e.g., AXI or OCP) to the IP modules connected to the NoC. In particular, the network interfaces NI may implement adapter units A to existing on-chip protocols, such as AXI, OCP and DTL, to seamlessly connect existing IP modules to the NoC. These adapter units A may also be arranged between the IP blocks and their associated network interfaces.

EX1001, 6:30-38

Buses to NoC



- Architectural paradigm shift: Replace wire spaghetti by network
- Usage paradigm shift: Pack everything in packets

EX2073,15

The “Hop” Occurs Inside the Network

The “network node” in Patent Owner’s construction is inside the network

Dr. Hassoun’s Second Declaration

18. From the general understanding in the art, a POSA would understand that a “hop” is a communication link with a node on each end. Webster’s Telecom Dictionary of 2008 defines hop in a similar manner. Ex. 1051, 6 (“In networks, the journey a signal makes across a transmission link between two devices such as bridges, hubs, switches, or routers.”). Each link in an interconnect having a node on each end is a hop. When data traverses from one node across a link to another node, it is said to have “hopped.” Thus, each node of an interconnect creates an additional hop from a master to a slave. If there are zero nodes between a master and a slave, i.e. the master and slave are directly connected, there is a single hop. If

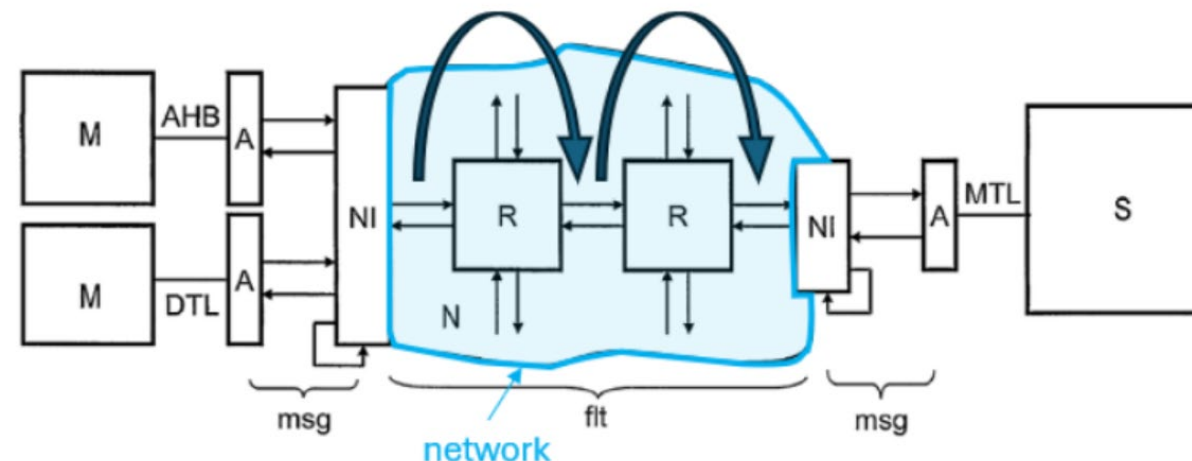
EX1030, ¶ 18

Dr. Hassoun’s Second Deposition

Q. What would be the difference between a network node and something that’s just a node?

A. So a node, if it’s not part of a network, then it’s not a network node. If it’s part of a network, then it happens to be a network node.

EX2084, 202:6-10



EX1001, FIG. 1 (annotated)

Ground 3: Purported Anticipation by Weber

WEBER DOES NOT DISCLOSE THE
CLAIMED “INTERCONNECT
MEANS” BECAUSE IT DOES NOT
DISCLOSE PACKETS

Weber Does Not Disclose Transmitting Packets

The experts agreed that Weber does not disclose transmitting packets

Dr. Bagherzadeh

protocol conversion. Similarly, a POSITA would understand that Weber does not disclose that packets are sent on Weber's buses. Because there is no conversion from the target/initiator protocol (e.g., OCP) to a network-based protocol (e.g., NTTP), Weber cannot disclose the claimed "interconnect means (N)." Similarly, because Weber does not route packets, Weber fails to disclose a "multi-hop" scheme where a "hop" is defined as a router or switch that a packet originating from an arbitrary protocol may traverse. Weber does not expressly disclose any

EX2070, ¶ 262

Dr. Hassoun's First Deposition

Q. Weber does not disclose transmitting packets over a shared bus, correct?

A. No, it does not.

EX2068, 116:18-20

Q. And earlier we discussed Weber does not disclose packets, correct?

A. Yes.

EX2068, 121:11-13

Weber Does Not Disclose Transmitting Packets

Dr. Hassoun's second declaration is inconsistent with his prior deposition testimony

Dr. Hassoun's First Deposition

Q. Weber does not disclose transmitting packets over a shared bus, correct?

A. No, it does not.

EX2068, 116:18-20

Q. And earlier we discussed Weber does not disclose packets, correct?

A. Yes.

EX2068, 121:11-13

Dr. Hassoun's Second Declaration

76. Even if packets were required, Weber discloses packets. Neither the '052 patent, nor Dr. Bagherzadeh provides any particular requirement that a communication must meet in order to be a "packet." In general, "packet" encompasses any collection of information sent in a single operation. *See* Ex. 1052, 787-788; Ex. 1051, 358. Weber discloses sending a collection of information together in a single operation and therefore discloses packets. Ex. 1007, ¶¶0049-0054. To the extent packet requires something more specific, like sending information sequentially including an address and data, Weber's disclosure of multiplexing, which places the address, data, and control signals on the same wire or wires, is a disclosure of packets. Ex. 1007, ¶¶0036, 0050.

EX1030, ¶ 76

Weber does not disclose a “Interconnect Means”

34

Dr. Hassoun testified for the first time during redirect that Weber “suggests” packets

Dr. Hassoun’s First Deposition – Petitioner’s Redirect

(Recess was taken from 4:11 p.m.
to 4:50 p.m.)

COURT REPORTER: Back on the record at
4:50 p.m.

EXAMINATION

BY MR. VANDENBURGH:

**Q. Two things, Dr. Hassoun. First, you testified
earlier that Weber does not talk about packets, right?**

A. Yes.

**Q. Does Weber contain any language that suggests
the use of packets?**

A. Yes.

Weber does not disclose a “Interconnect Means”

35

Dr. Hassoun reaffirmed his earlier testimony that Weber does not disclose packets

Dr. Hassoun's First Deposition – Patent Owner's Recross

Q. So when you testified on redirect that Weber suggests packets, you were offering that opinion for the first time during the deposition after conferring with counsel, correct?

A. I -- that it suggests packets, yes.

EX2068, 146:2-6

Q. Okay. So with respect to whether Weber discloses packets, you would still agree, wouldn't you, that Weber does not expressly disclose packets, correct?

A. Yes, it doesn't use the word "packet" in there.

EX2068, 145:8-12

Weber does not disclose a “Interconnect Means”

36

Dr. Hassoun admitted to rehearsing his redirect testimony with counsel during the recess

Dr. Hassoun's First Deposition - Recross

Q. Dr. Hassoun, did you discuss your testimony in response to my questioning during the break between cross-examination and redirect?

A. Yes.

Q. Did you discuss the questions that counsel would ask you during redirect during the break?

A. Yes.

Q. Did you discuss the answers that you would give to counsel in response to that questioning during the break?

A. Yes.

FLIR Sys., Inc. v. Leak Surveys, Inc., IPR2014-00411,
Paper 45 at 7 (PTAB Feb. 10, 2015)

“when recess conversations occur ... the Board may find that there was witness coaching and may exclude or **give little, or no, weight to the testimony of a coached witness.**”

EX2068, 144:18-145:3

Ground 3: Purported Anticipation by Weber

WEBER DOES NOT DISCLOSE A
MULTI-HOP INTERCONNECT ON
A SINGLE INTEGRATED CIRCUIT
("IC")

Claim Construction

CLAIMS 1-6

“INTEGRATED CIRCUIT”

Independent Claims 1 and 6

Claim 1

1. Integrated circuit, comprising:
 a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification,
 an interconnect means (N) for coupling said plurality of processing modules (M, S) and for enabling a connection based communication having a set of connection properties,
 at least one network interface (NI) associated to said at least one first of said processing modules for controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N), and
 a mapping means (A) for mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S).

Claim 6

6. Method of communication service mapping in an integrated circuit, having a plurality of processing modules (M, S), wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S), comprising the steps of:
 coupling said plurality of processing modules (M, S) by an interconnect means (N) and
 enabling a connection based communication having a set of connection properties,
 controlling the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N) by at least one network interface (NI) associated to said at least one first of said processing modules,
 mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.

“Integrated Circuit”

40

The Parties’ Agreed Construction in District Court

'818	1-3, 5-7	“integrated circuit”	“Interconnected circuitry on a chip”
'449	10		
'052	6		
'9,893	4		
'2,893	10		
'800	12		

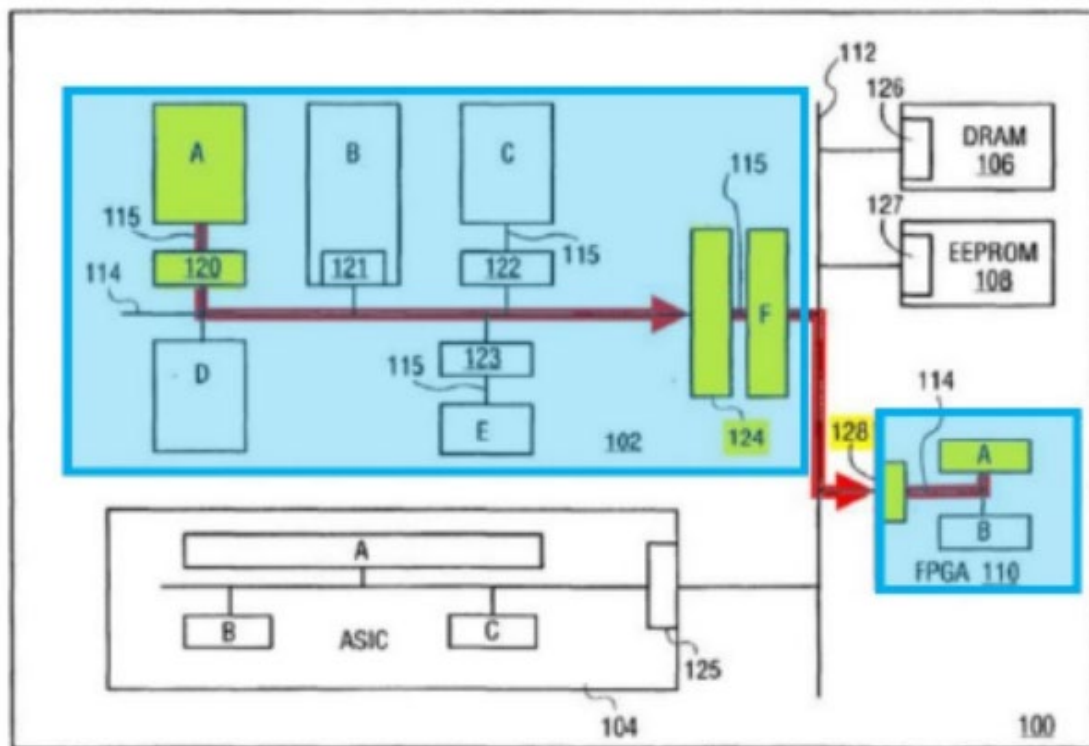
EX1016, 13

District Court Claim Construction (TI Case)

TERM/PHRASE	COURT’S CONSTRUCTION
“integrated circuit” '818 Patent: Claims 1-3, 5-7 '449 Patent: Claim 10 '052 Patent: Claims 6 '9893 Patent: Claim 4 '2893 Patent: Claim 1, 10 '800 Patent: Claim 12	“a combination of interconnected circuit elements inseparably associated on or within a continuous substrate”

EX2022, 59

Weber's shared buses 112 and 114 are **not** on the same integrated circuit



EX1007, FIG. 1 (annotated)

Weber

sub-systems shown in system 100. Integrated circuit 102 includes sub-systems 102A, 102B, 102C, 102D and 102E. ASIC 104 includes functional blocks 101A, 104B and 104C. FPGA 110 includes functional blocks 110A and 110B. A functional block may be a particular block of logic that performs a particular function. A functional block may also be a memory component on an integrated circuit.

EX1007, ¶[0037]

Dr. Bagherzadeh

216. In FIG. 1 of Weber, the sub-system 102 “is a fully custom integrated circuit.” Ex. 1007, ¶ [0037]. Sub-system 104 “is an application specific integrated circuit (ASIC), which, as is known, is an integrated circuit designated to perform a particular function.” *Id.* The communications bus 112 connects “separate integrated circuit chips.” *Id.* In other words, sub-systems 102, 104, 106, 108, 110 are not on the same integrated circuit or chip in FIG. 1 – they are separate and distinct circuits or chips.

EX2070, ¶216

POR, 59-63; POSR, 17-20

Petitioner's First "Interconnect Means" Theory Fails

42

Weber's shared buses 112 and 114 are **not** on the same integrated circuit

Weber

[0038] System 100 is an example of a system that may consist of one or more integrated circuits or chips. A functional block may be a logic block on an integrated circuit such as, for example, functional block 102E, or a functional block may also be an integrated circuit such as fully custom integrated circuit 102 that implements a single logic function.

EX1007, ¶[0038]

circuit designed specifically to operate in system 100. Other embodiments may contain additional sub-systems of the same types as shown, or other types not shown. Other embodiments may also include fewer subsystems than the sub-systems shown in system 100. Integrated circuit 102

EX1007, ¶[0037]

Dr. Bagherzadeh

[0037]. This means that Weber contemplates embodiments with only one of the sub-systems 102, 104, 106, 108, and 110. For example, Weber contemplates an example of the system 110 with only the sub-system 102. As such, a POSITA would understand Weber's statement that the system "may consist of one or more integrated circuits or chips" to be consistent with the fact that the system 100 may only include one of the sub-systems (e.g., sub-system 102), in which case the system 100 would only include one integrated circuit or chip. A POSITA would not read this statement in Weber to mean that all of the sub-systems 102, 104, 106, 108, and 110 (or some combination of those sub-systems) can be implemented on single integrated circuit or chip. In other words, a POSITA would understand Weber to mean that system 100 could include one or more integrated circuits, but not that the system 100 (as depicted in Figure 1) can be deployed as a single integrated circuit. Weber never expressly describes or illustrates any embodiment of system 100 where all of the sub-systems are on one integrated chip – they are shown and described as being separate and distinct.

EX2070, ¶1217

POR, 59-63; POSR, 17-20

Petitioner's First "Interconnect Means" Theory Fails

43

Petitioner's reliance on Dr. Hassoun's testimony that a POSITA would "at once envisage" Weber's subsystems on a single IC is flawed

Petition

⁷ To the extent PO argues that Weber's disclosures come from separate embodiments, a POSA reading Weber would "at once envisage" the claimed method. Ex-1003, ¶¶191, 204-205, 219, 225; *Kennametal*, 780 F.3d at 1381.

Petition, 47 n.7

Dr. Hassoun First Declaration

191. Because Weber also suggests that system 100 can be implemented on a single integrated circuit, a POSA would at once envisage that system 100, which includes a plurality of sub-systems 102, 104, 106, 108, and 110, can also be "an integrated circuit having a plurality of processing modules (M, S)".

EX1003, ¶191

***Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 851 F.3d 1270, 1274-75 (Fed. Cir. 2017)**

explaining that "*Kennametal* does not permit the Board to fill in missing limitations simply because a skilled artisan would immediately envision them."

Petitioner's First "Interconnect Means" Theory Fails

44

A POSITA would not envisage all of Weber's subsystems on a single IC

Dr. Bagherzadeh

219. A POSITA would also understand that it was, at a minimum, highly impractical and unusual in the relevant timeframe to design and employ a single integrated circuit having all the components of system 100. This is because DRAM 106 is inherently incompatible with the logic processes of the integrated circuits 102 and 104 in FIG. 1 of Weber. There are several reasons for this. First, the CPUs

EX2070, ¶1219

Technical problems for integrating DRAM and CPU on one IC:

- Comprised performance
- Increased die size (form factor) and expense
- Thermal management
- Inability to upgrade DRAM

EX2070, ¶¶ 219-226

Dr. Hassoun Second Declaration

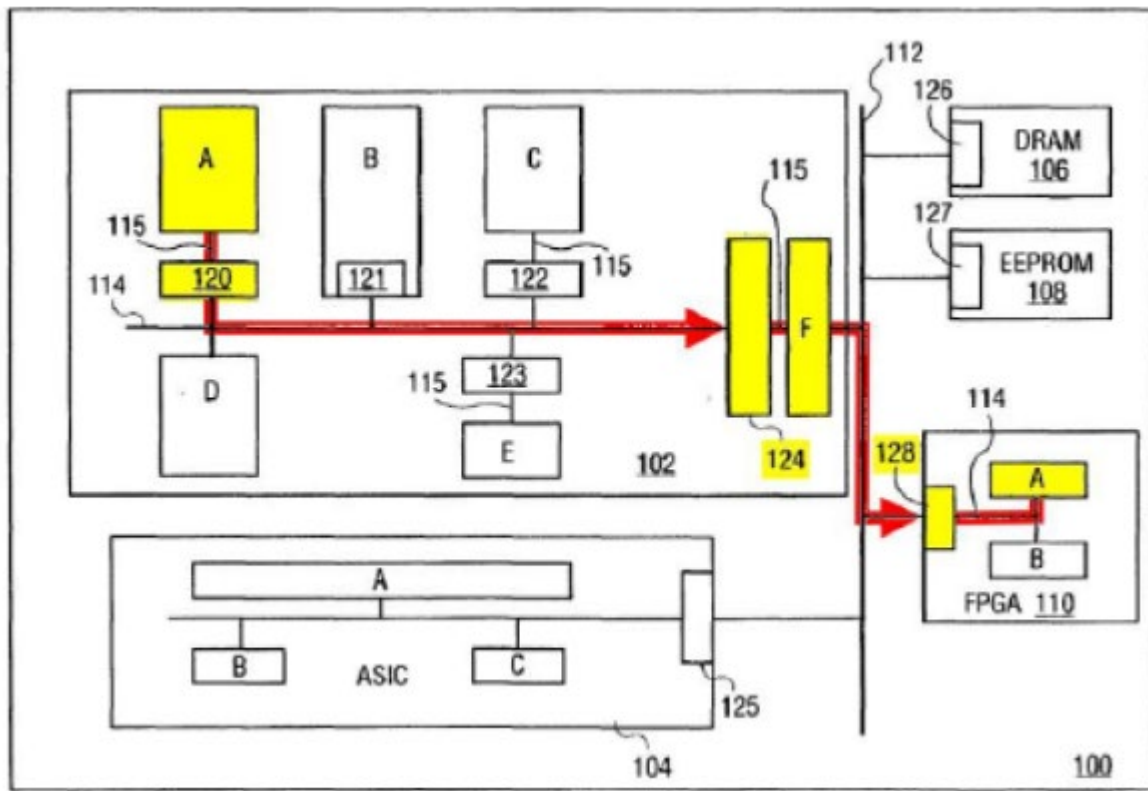
100 on a single IC. Integrating components together always involves tradeoffs, particularly with regard to cost, size, performance, and thermal management. The fact that these tradeoffs exist does not mean that Weber does not disclose integrating the components together. There are probably many aspects of Weber that may be disadvantageous in certain situations, but that does not mean Weber does not disclose them. Moreover, it was known, even at the time of Weber, that integrating DRAM with a processor was both possible and beneficial. *See Ex. 1053*

EX1030, ¶155

Petitioner's First "Interconnect Means" Theory Fails

45

Weber does not disclose a multi-hop interconnect



EX1007, FIG. 1

Reply

2. Weber's Bus-With-Interfaces Is a "Network" Even Under PO's Definition

In Weber Figure 1, the modules ("functional blocks") in each of sub-system 102 and system 100 are not directly connected, but instead are indirectly connected by interface modules (e.g., 120, 122-125), and bridge F, each of which are "network nodes" that create "hops." Paper 3, 56-58.; Ex-1007, ¶¶37, 40, FIG. 1;

Reply, 23

Petitioner's "Interconnect Means" Theory Fails

Dr. Hassoun's opinion that Weber's interfaces 120-128 are network nodes that create hops is inconsistent with his district court testimony

Dr. Hassoun's Second Declaration

6. Weber's Interfaces are "Network" Interfaces

88. Weber's interfaces are network interfaces for the simple reason that Weber discloses a network as discussed above and the interfaces are for that network. *Supra*, §VI.C.4, VI.C.5, Ex. 1003, ¶¶193-196, 209. Dr. Bagherzadeh

EX1030, ¶ 88

'052 patent. As described above, each of the interfaces (and the bridge F) create a hop making Weber a "multi-hop interconnect." *Supra*, §V.B, §VI.C.4. Each of the interfaces (and the bridge F) are also part of the network and therefore "network nodes," thus the functional blocks are "separated by one or more network nodes."

EX1030, ¶ 85

Dr. Hassoun's District Court Declaration

83. Claim 6 recites no structure for "interconnect means." Rather, it only recites its function: "coupling said plurality of processing modules (M, S)."

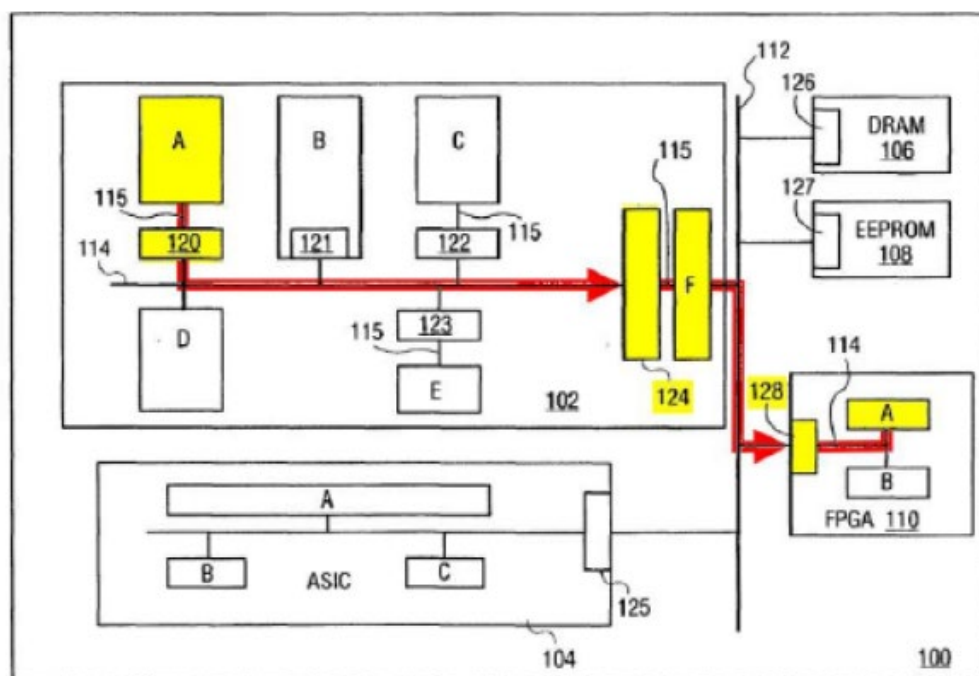
84. The '052 patent specification identifies structures that are clearly linked to the function of coupling the plurality of processing modules:

85. The '052 specification also discloses that each module M, S is connected to network via its associated network interface NI:

86. Therefore, putting all these disclosures together, but excluding the network interface NI because it is separately claimed in claim 6, the structures broadly disclosed that are clearly linked to performing the function of "coupling said plurality of processing modules (M,S)" are: bus, switch, point-to-point wire, or network.

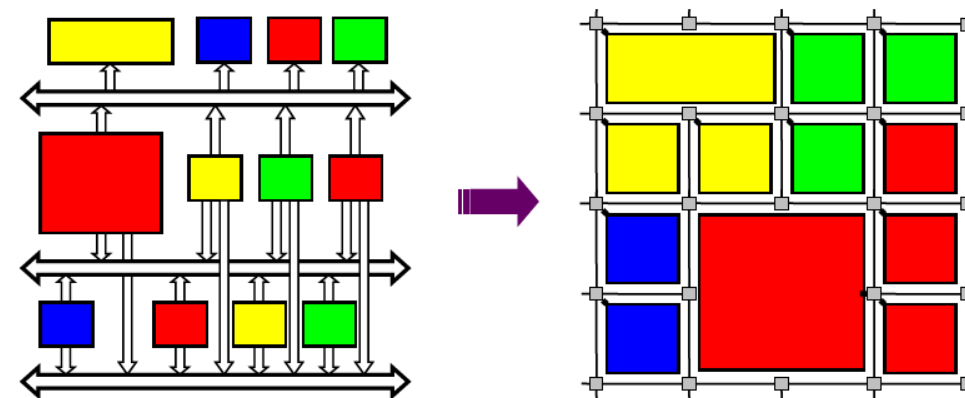
Petitioner's First "Interconnect Means" Theory Fails

Weber's buses are not a multi-hop interconnect



EX1007, FIG. 1

Buses to NoC



- Architectural paradigm shift: Replace wire spaghetti by network
- Usage paradigm shift: Pack everything in packets
- Organizational paradigm shift

EX2073, 15; EX2070, ¶1265

Petitioner's Second "Interconnect Means" Theory Fails

48

Theory 2: there are no hops because the communication subsystems are not network nodes

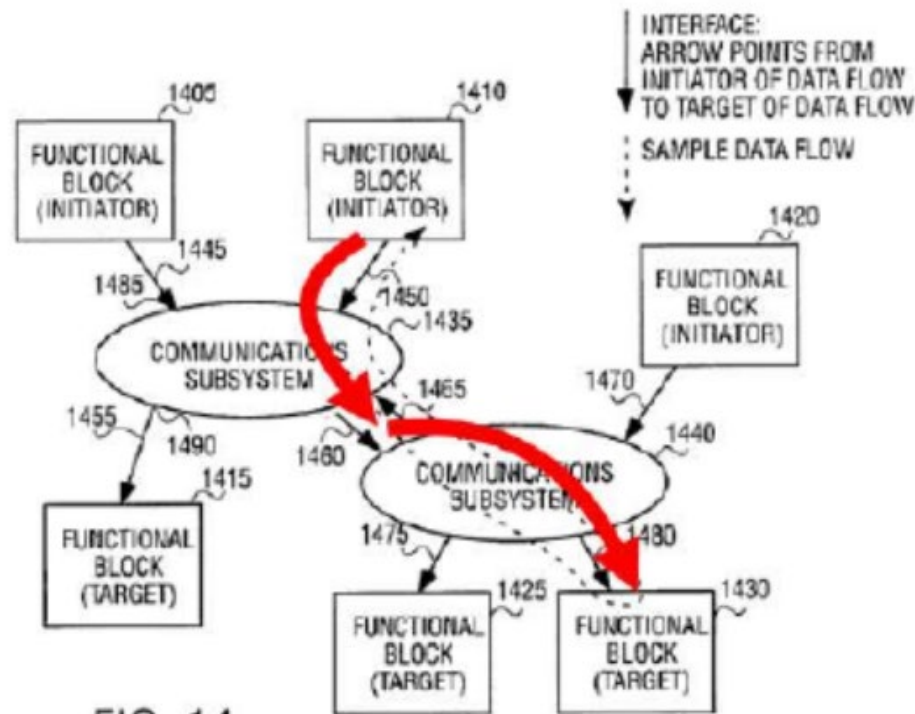


FIG. 14

EX1007, FIG. 14

Dr. Hassoun's Second Declaration

Figure 14 is yet another disclosure of a “multi-hop interconnection between modules separated by one or more network nodes” because there is a hop from the initiator function block 1410 across the first communications sub-system 1435 and a hop across the second communications sub-system 1440 to the target functional block 1430. Ex. 1003, ¶¶203-205.

EX1030, ¶72

Petitioner's Second "Interconnect Means" Theory Fails

49

Theory 2: there are no hops because the communication subsystems are not network nodes

Dr. Hassoun's First Declaration

204. Figure 14 is another independent way in which Weber discloses this element. Weber links the end-to-end flow of Figure 14 with the initiator 1002 to target 1008 communication path of Figure 4. *See e.g.*, Ex-1007 at [0098]. Because of this link, a POSA would immediately envisage that an initiator (e.g., 1410) in Figure 14 could be an initiator (e.g., 102A) of system 100 and a target (e.g., 1430) of Figure 14 could be a target (e.g., 128) of system 100. A POSA would also envisage that the communication sub-systems 1435 and 1440 would be routers or respective shared buses (e.g., 112, 114) of system 100. Thus, it is immediately

EX1003, ¶204

Dr. Bagherzadeh

269. In FIG. 14, the communication subsystems are not network nodes, the system performs no hops, and there is no protocol conversion. Weber does not

EX2070, ¶269

do not switch or route data. Thus, a POSITA would understand that the communication subsystems are not network nodes, nor are the communication subsystems the "hop" in the claimed "multi-hop interconnection separated by one or more network nodes."

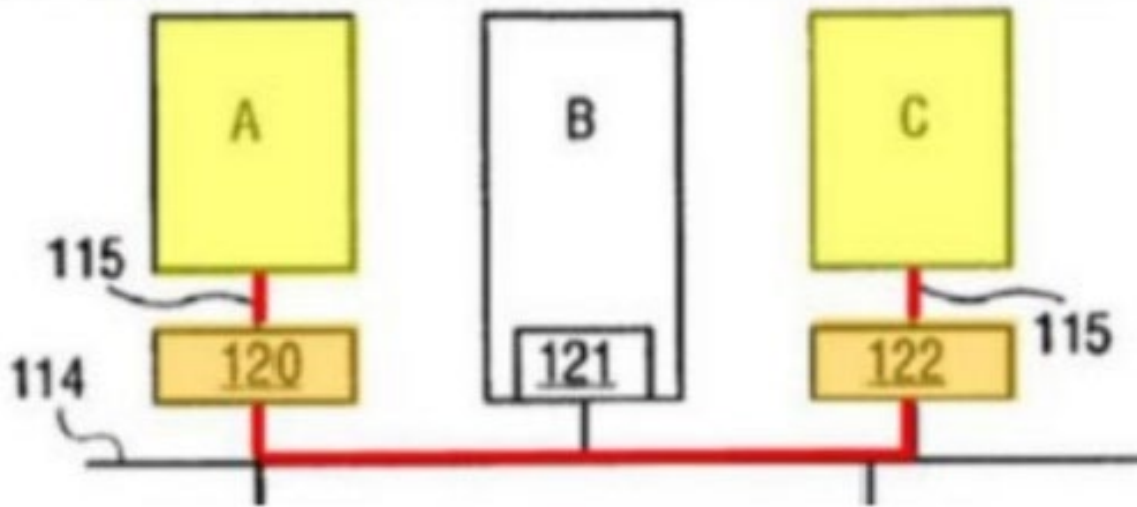
EX2070, ¶274

Petitioner's Third "Interconnect Means" Theory Fails

50

The Reply argues for the first time that shared bus 114 alone is multi-hop

Weber FIG. 1



EX1007, FIG. 1 (excerpted and annotated)

Reply

In Weber Figure 1, the modules ("functional blocks") in each of sub-system 102 and system 100 are not directly connected, but instead are indirectly connected by interface modules (e.g., 120, 122-125), and bridge F, each of which are "network nodes" that create "hops." Paper 3, 56-58.; Ex-1007, ¶¶37, 40, FIG. 1; Ex-1003, ¶¶194, 199-202; Ex-1030, ¶¶17-21, 71-72, 88. Examples include:

Reply, 23

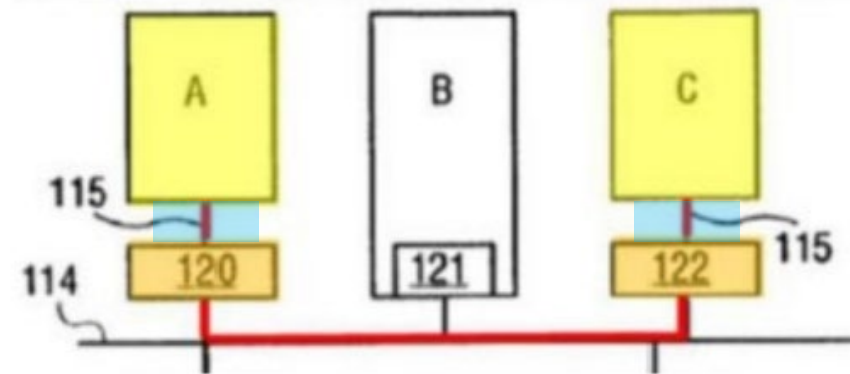
Petitioner's Third "Interconnect Means" Theory Fails

51

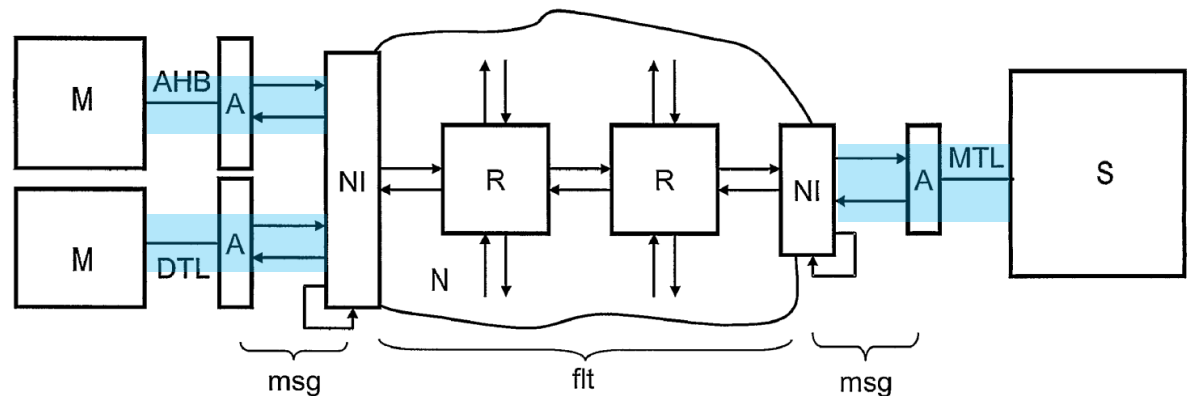
Link 115 does not define a "hop"

[0039] Shared communications bus 112 provides a shared communications bus between sub-systems of system 100. Shared communication bus 114 provides a shared communications bus between sub-systems or functional blocks on a single integrated circuit. Some of the functional blocks shown are connected to interface modules through which they send and receive signals to and from shared communications bus 112 or shared communications bus 114. **Interconnect 115 is a local point-to-point interconnect** for connecting interface modules to functional blocks.

EX2070, ¶ [0037]



EX1007, FIG. 1 (excerpted and annotated)



EX1001, FIG. 1 (annotated)

Ground 4: Petitioner Has Not Met Its Burden to Show Obviousness over Weber in View of Rădulescu2004

Ground 4:
Purported
Obviousness
Over Weber in
view of
Rădulescu2004

ALLEGED OBVIOUSNESS FOR THE
“INTEGRATED CIRCUIT” LIMITATION
(CLAIMS 1-6)

The Petition Did Not Argue Obviousness for the “Integrated Circuit”

54

Petition

1. [6.pre.1]

Both Weber and Rădulescu2004 disclose this part of the preamble for the reason in Grounds 1 and 3. *See supra* X.A.1, VIII.A.1.

Petition, 71

Reply

known reference to a single integrated circuit. Ex-1003, ¶¶122, 185. The Petition also showed that each of Weber and Radulescu2004 disclosed claim element [6.pre.1], which recites the “integrated circuit” limitation. Paper 3, 21 (Ex-1005, Abstract, 1), 47-49 (Ex-1007, [0002], [0035], [0037]-[0040], [0050], Fig. 1), 71. And PO does not dispute that Radulescu2004 discloses a single integrated circuit or that Weber’s sub-system 102 is a single integrated circuit.

Because Weber discloses, and suggests the desirability of use on, a single integrated circuit and Radulescu2004 discloses an SoC, it would have been obvious to implement the combined teachings via a single integrated circuit. *Id.*; *see also* Ex-1003, ¶¶47, 112-113, 185, 191, 233-234; Ex-1030, ¶89.

Reply, 26

The Reply's New Obviousness Argument is Not Supported by Evidence

55

Dr. Hassoun's conclusory assertions are insufficient

Dr. Hassoun's First Declaration

233. It is also my opinion that a POSA would have been motivated, with a reasonable expectation of success, to combine Weber and Rădulescu2004, in view of the teachings of each and the knowledge of a POSA, in a way that meets all of the claimed limitations.

EX1003, ¶ 233

Dr. Hassoun's Second Declaration

89. In my first declaration, I opined that a POSA would have been motivated, with a reasonable expectation of success, to combine Weber and Radulescu2004, in a way that meets all of the claimed limitations. This includes the limitation for an “integrated circuit.” It would have been obvious to implement the combination on an integrated circuit for the reasons discussed above and in my first declaration with respect to Weber's disclosure of an integrated circuit. *Supra*, §VI.C.1; Ex. 1003, ¶¶185, 191, 233-234. Dr. Bagherzadeh disagrees that putting them all on an integrated circuit would have been obvious but provides no further reasoning other than what he provided in Ground 3.

EX1030, ¶ 89

Ground 4: Purported Obviousness by Weber in view of Rădulescu2004

PETITIONER DID NOT EXPLAIN
HOW WEBER AND
RĂDULESCU2004 WOULD BE
COMBINED

Petition Does Not Explain How Weber and Rădulescu2004 Would be Combined

57

Petition

3. [6.a]

Both Weber and Rădulescu2004 disclose this for the reasons identified in Grounds 1 and 3. *See supra* X.A.3, VIII.A.3. To the extent PO advocates a construction of “interconnect means” here as “a multi-hop interconnection between modules separated by one or more network nodes” (Ex-1017, 25) and argues that Weber does not disclose such an interconnect means, this limitation would have been obvious in view of Rădulescu2004 for the reasons described in Ground I. *See supra* VIII.A.3.

Petition, 71

5. [6.c]

Both Weber and Rădulescu2004 disclose this for the reasons identified in Grounds 1 and 3. *See supra* X.A.5, VIII.A.5. To the extent PO argues that Weber’s interface modules are not **network** interfaces because they provide an interface to a shared bus, this limitation would have been obvious in view of Rădulescu2004 for the reasons described in Ground I. *See supra* VIII.A.5.

Petition, 72

Petition Does Not Explain How Weber and Rădulescu2004 Would be Combined

58

Pers. Web. Techs., LLC v. Apple, Inc.,
848 F.3d 987, 994 (Fed. Cir. 2017)

Petitioner failed to meet its burden because it “nowhere clearly explained, or cited evidence showing, how the combination of the two references was supposed to work”

ActiveVideo Networks, Inc. v. Verizon Commc'ns Inc.,
694 F.3d 1312, 1327 (Fed. Cir. 2012)

Finding claims non-obvious because “expert failed to explain ... which combination(s) of elements in specific references would yield a predictable result, or how any specific combination would operate”

Each Potential Weber-Rădulescu2004 Combination Fails

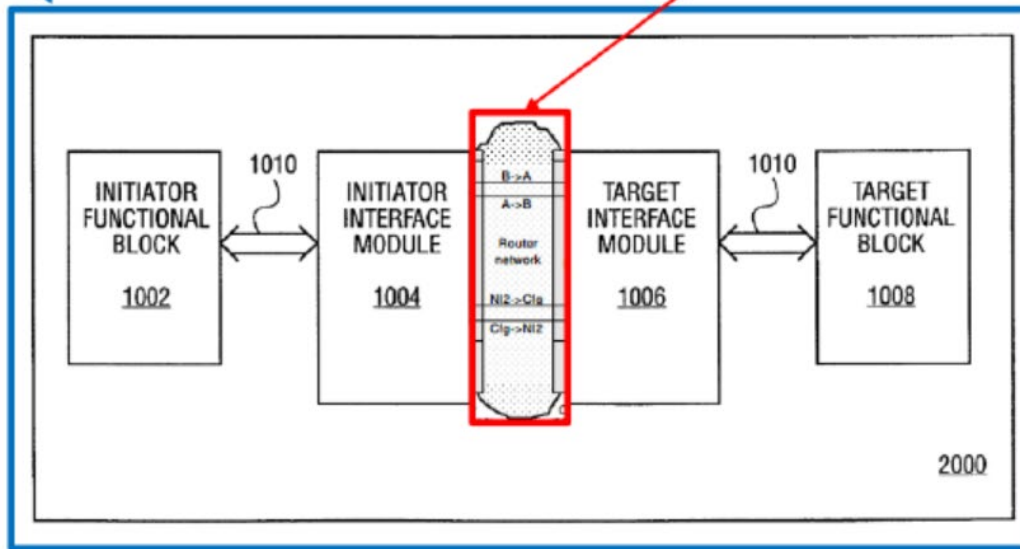
59

First Combination: Weber's SoC with Rădulescu2004's NoC

Dr. Bagherzadeh

Weber's SoC

Rădulescu2004's Network



POR, 70

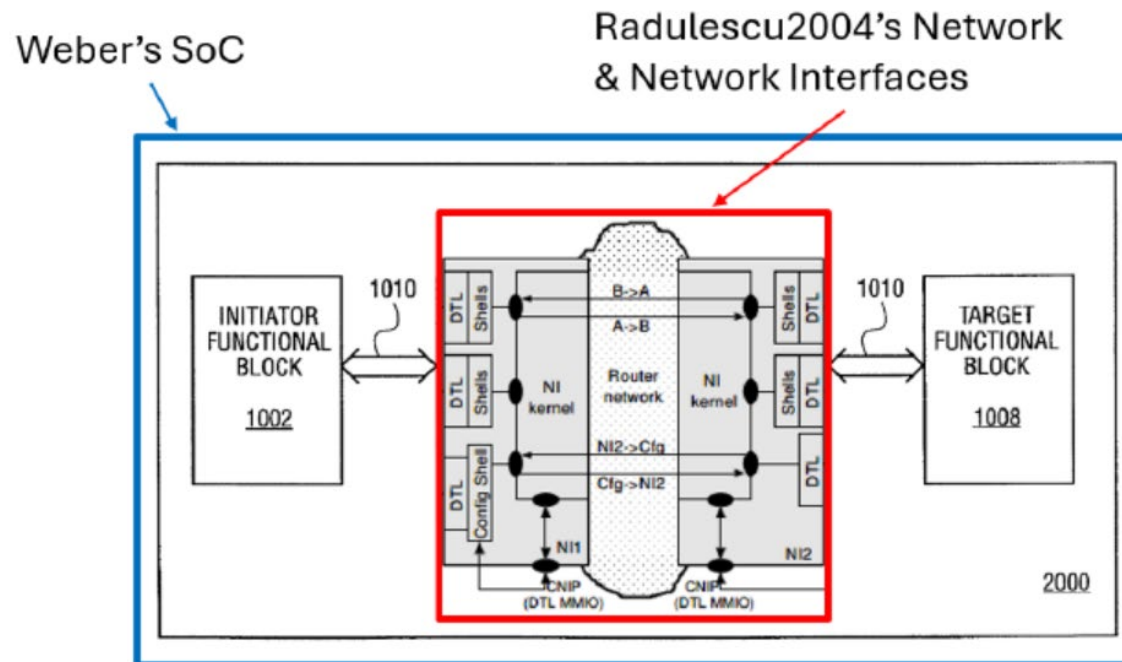
308. A POSITA would readily recognize that this proposed combination is untenable because Weber's interfaces 1004 and 1006 communicate in a different communication protocol than Rădulescu2004's network. Compare Ex. 1007 at ¶

309. A POSITA would not be motivated to swap Weber's bus-based interconnect for Rădulescu2004's network because of the differing communication protocols of Weber's interfaces compared to Rădulescu2004's network. A POSITA would understand that merely inserting a network-based interconnect into a bus-based system would cause the system to be incapable of transmitting communications. The network would not be able to receive the requests issued by the initiator functional blocks and relayed by the interfaces, nor would the interfaces be capable of receiving the request sent over the network in the network communication protocol. Dr. Hassoun does not explain if or how a POSITA would

Each Potential Weber-Rădulescu2004 Combination Fails

60

Second Combination: Weber's SoC with Rădulescu2004's NoC and Network Interfaces



POR, 71

Dr. Bagherzadeh

322. As discussed above, Rădulescu2004 does not disclose the “mapping” claimed in the ‘052 Patent because it does not expressly disclose selecting a specific connection based on connection properties assigned to that connection. *Supra* § IX.A.1.ii. Assuming that Rădulescu2004’s network (including the network interfaces containing the adapter units) were substituted into Weber (which I disagree with), then the resulting Weber and Rădulescu2004 combination would suffer from the same deficiency as Rădulescu2004 and would not disclose the claimed mapping. Dr. Hassoun does not assert that it would have been obvious to

EX2070, ¶ 322

Ground 4: Purported Obviousness by Weber in view of Rădulescu2004

A POSITA WOULD NOT BE
MOTIVATED TO COMBINE
(CLAIMS 1-7)

POSITA Would Not Be Motivated to Combine Weber and Rădulescu2004

62

Weber acknowledges and addresses the limitations of conventional buses

Petition

A POSA would have understood that using Rădulescu2004's NoC and associated network interfaces would improve the scalability and performance of Weber's communication system. Ex-1003, ¶51, ¶¶238-241. For instance,

Petition, 69

Weber

[0006] One disadvantage of computer buses is that each sub-system or component connected to the bus is constrained to use the protocol of the bus. In some cases, this

[0007] Current bus systems provide limited capability to preserve order in one transaction stream by supporting “split transactions” in which data from one transaction may be interleaved with data from another transaction in the same stream. In such a bus, data is tagged as belonging to one

[0008] Current bus systems do not support true concurrency of operations for a sub-system that can process multiple streams of transactions over a single interconnect,

new sub-systems or components. Existing communication approaches thus do not meet the requirements of today's large, complex electronics systems. Therefore, it is desirable for a communications system and mechanism to allow sub-systems of a large, complex electronics system to inter-operate efficiently regardless of their varying performance characteristics and requirements.

EX1007, ¶¶[0006]-[0009]

POSITA Would Not Be Motivated to Combine Weber and Rădulescu2004

63

Weber already provides scalability

Dr. Bagherzadeh

requirements.” Ex. 1007 at ¶ [0009]. According to Dr. Hassoun, scalability refers to whether the interconnect is “suitable for systems with a large number of cores or functional blocks.” Ex. 1003 at ¶ 239. Weber expressly says that its system can meet the requirements of large complex systems, i.e., systems with a large number of cores or functional blocks. Ex. 1007 at ¶ [0009]. In other words, Weber teaches that its solution provides the scalability that may have been missing from traditional bus architectures. Dr. Hassoun does not identify a particular reason why a POSITA would believe Weber lacks scalability, and in view of these teachings, a POSITA would understand that Weber already addressed that problem. As such, I

EX2070, ¶293

Dr. Hassoun's First Deposition

Q. Would you agree that one of Weber's goals is to allow large, complex electronics systems to operate efficiently?

A. Regardless of their varying performance characteristics and requirements, yes.

Q. And Weber teaches that invention is able to allow large, complex electronic systems to operate efficiently, right?

A. Regardless of their varying performance characteristics and requirements, yes.

EX2068, 104:23-105:7

POSITA Would Not Be Motivated to Combine Weber and Radulescu2004

64

The Reply acknowledges that Weber provides benefits over traditional buses

Reply

PO asserts that neither scalability nor performance would have motivated this combination, because Weber already provides these benefits. Paper 38, 65-69. The fact that Weber provides these benefits over traditional buses, however, does not mean that a POSA would be unmotivated to make further improvements to scalability or performance. Ex-1030, ¶90. To the contrary, Weber's teaching that a POSA wanted improved scalability and performance further *supports* the motivation. *Id*; *Intel*, 61 F.4th at 1380.

Reply, 27

Dr. Hassoun Second Declaration

90. Dr. Bagherzadeh asserts that because Weber touts or otherwise provides benefits over traditional buses a POSITA would not have been motivated to combine Radulescu2004 with Weber, because Weber already provides these benefits. Ex. 2070, ¶¶293-299. The fact that Weber provides these benefits over traditional buses, however, does not mean that a POSA would not be motivated to make further improvements to scalability, performance, concurrent data transmissions, fault tolerance, and power efficiency. In fact, Weber's statements relating to the desirability of improved scalability and performance in an interconnect, support the position that these are things that motivate a POSA to make changes to an interconnect.

EX1030, ¶190

POSITA Would Not Be Motivated to Combine Weber and Rădulescu2004

65

Weber already provides for concurrent data transmissions

Petition

SoC. Ex-1005, 1; Ex-1003, ¶241. In addition, a POSA would have understood that a router network like Rădulescu2004's NoC can support many concurrent data transmissions, thus enabling a larger amount of data to be communicated between the various modules and blocks in an SoC. Ex-1003, ¶51, ¶214.

Petition, 69

Dr. Bagherzadeh

294. With respect to performance, Weber teaches that traditional buses suffer from performance problems in that they do not allow for concurrent data transmission. Ex. 1007 at ¶ [0006]. Weber goes on to disclose that unlike traditional buses, its solution does provide for concurrent data transmissions. Ex.

EX2070, ¶293

Weber

[0070] As FIG. 9 implies, the algorithm described above allows a target to actively satisfy transfer requests from multiple CONNID values at the same time. Thus, there may be multiple logical transactions in flight to and/or from the same target, provided that they have separate CONNID values. Thus, the present invention supports multiple connections per target functional block.

EX1007, ¶[0070]

[0071] Additionally, an initiator may require the ability to present multiple transactions to the communications system at the same time. Such a capability is very useful for initiator

EX1007, ¶[0071]

POSITA Would Not Be Motivated to Combine Weber and Rădulescu2004

66

Petitioner failed to acknowledge or consider disadvantages of using an NoC

Dr. Bagherzadeh

301. While Dr. Hassoun's opinions focus on certain advantages associated with NoCs relative to traditional buses, a POSITA would recognize that there are many disadvantages associated with NoCs relative to traditional buses. For example, the table below lists pros and cons of using a NoC versus a bus. These examples are consistent with a POSITA's understanding of these issues.

EX2070, ¶ 301

302. One of the known disadvantages to using a NoC compared to a bus is that it increases the form factor of the device. Weber recognized that "[e]lectronic

EX2070, ¶ 302

303. A POSITA would understand in the relevant timeframe that NoCs would be more expensive and complicated than Weber's shared bus. Not only are

EX2070, ¶ 303

POSITA Would Not Be Motivated to Combine Weber and Rădulescu2004

67

Petitioner's evidence demonstrates the tradeoffs for an NoC

Bus Pros & Cons		Network Pros & Cons	
Every unit attached adds parasitic capacitance, therefore electrical performance degrades with growth.	-	+	Only point-to-point one-way wires are used, for all network sizes.
Bus timing is difficult in a deep submicron process.	-	+	Network wires can be pipelined because the network protocol is globally asynchronous.
Bus testability is problematic and slow.	-	+	Dedicated BIST is fast and complete.
Bus arbiter delay grows with the number of masters. The arbiter is also instance-specific.	-	+	Routing decisions are distributed and the same router is reinstanciated, for all network sizes.
Bandwidth is limited and shared by all units attached.	-	+	Aggregated bandwidth scales with the network size.
Bus latency is zero once arbiter has granted control.	+	-	Internal network contention causes a small latency.
The silicon cost of a bus is near zero.	+	-	The network has a significant silicon area.
Any bus is almost directly compatible with most available IPs, including software running on CPUs.	+	-	Bus-oriented IPs need smart wrappers. Software needs clean synchronization in multiprocessor systems.
The concepts are simple and well understood.	+	-	System designers need <i>reeducation</i> for new concepts.

Table 3: The bus-versus-network arguments

POSITA Would Not Be Motivated to Combine Weber and Rădulescu2004

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Paragraphs 238-241 of Dr. Hassoun's first declaration do not consider any disadvantages

Dr. Hassoun Second Declaration

91. Dr. Bagherzadeh also suggests that the potential disadvantages of Radulescu2004's NoC need to be considered. Ex. 2070, ¶¶301-304. I did take into account any potential disadvantages because I expressly consider Radulescu2004's NoC as compared to a bus and conclude that there can be (on balance) advantages for Radulescu2004's NoC. Ex. 1003, ¶¶238-241. In any case, the mere presence of tradeoffs alone would not discourage a POSA from trying the proposed combination.

EX1030, ¶ 91

Ground 1: Petitioner Has Not Shown That Rădulescu2004 Anticipates Any Challenged Claim

Ground 1: Purported Anticipation by Rădulescu2004

CLAIMS 1, 6-7:

“WHEREIN AT LEAST ONE FIRST OF SAID PROCESSING MODULE (M) REQUESTS AT LEAST ONE COMMUNICATION SERVICE TO AT LEAST ONE SECOND PROCESSING MODULE (S) BASED ON SPECIFIC COMMUNICATION PROPERTIES AND AT LEAST ONE COMMUNICATION SERVICE IDENTIFICATION”

Rădulescu2004 does not disclose a “communication service identification”

71

The evidence does not warrant a difference outcome in the final written decision

Institution Decision

We agree with Patent Owner that Rădulescu2004’s disclosures that its communication service identification contains an address for the “slave” and its “slave” has an address range do not by themselves teach or suggest that Rădulescu2004’s communication service identification contains an address range. Further, Petitioner has not explained why other disclosures or the knowledge of an ordinarily skilled artisan would have provided such a teaching or suggestion. Thus, we determine that Petitioner’s showing for preamble recitation 6.pre.2 is insufficient.

Paper 11, 25

The Reply Attempts to Cure the Petition's Deficient Analysis

73

The Petition argued that Radulescu2004's requests include a communication service identification; the Reply argues the requests need only be "based on" a communication service identification

Petition

Thus, the requests for communication services (read/write operations) made by the Master IP module include a communication service identification corresponding to "at least one address range" that "identif[ies] one or more second processing modules (S) or a memory region within said one or more second processing modules (S)." Ex-1003, ¶¶124-127.

Petition, 25

The Reply

PO argues, and the Board appears to have preliminarily agreed, that to meet [6.pre.2] and the similar limitation in claims 1 and 7, communication service requests must contain an address range or thread. Paper 38, 39-42; Paper 11, 25-26. But that is not what the claim says. Claim 6 only requires that requests be "based on" a communication service identification that is either an address range or thread. Ex-1001, 10:9-15. PO's interpretation of "based on" as "contains" improperly imports a requirement that was not claimed. Ex-1030, ¶¶22-25.

Reply, 8-9

The Reply Presents a New Claim Construction

The Reply failed to show that Radulescu2004's requests "consider" an address range

Dr. Hassoun Second Deposition

What would a person of skill in the art understand the plain and ordinary meaning of the phrase "based on" to be?

So in this example, the "based on" communication service identification means that the communication -- too many words here -- communication service identification, it needs to consider at least a communication thread or one address range.

EX2084, 216:24-217:24

Reply

This is exactly what Radulescu2004 discloses (unsurprising given it describes the same *Æthereal* NoC). Ex-1030, ¶27. The "address range" assigned to each slave is stored (e.g., "configurable") in the narrowcast module, which—like in the '052 patent—is in the network interface. Ex-1005, 4; Ex-1003, ¶124; Ex-1030, ¶27; Paper 3, 24-25. The communication service requests in Radulescu2004 are "based on" these address ranges because the requests contain an address that, using the address ranges "configured" in the narrowcast module, correspond to "the slave for which the transaction is destined." *Id.*

Reply, 11

Ground 1: Purported Anticipation by Radulescu2004

CLAIMS 1, 6-7:

“MAPPING THE REQUESTED AT
LEAST ONE COMMUNICATION
SERVICE BASED ON SAID
SPECIFIC COMMUNICATION
PROPERTIES TO A CONNECTION
BASED ON A SET OF
CONNECTION PROPERTIES
ACCORDING TO SAID AT LEAST
ONE COMMUNICATION
SERVICE IDENTIFICATION”

Radulescu2004 does not disclose “mapping ...
according to the communication service identification”

mapping the requested at least one communication service
based on said specific communication properties to a
connection based on a set of connection properties
according to said at least one communication service
identification.

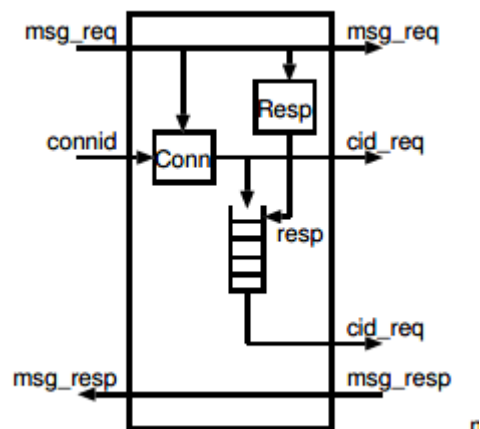
EX1001, Claim 6

Radulescu2004 does not disclose “mapping ... according to the communication service identification”

Radulescu2004

The NI kernel communicates with the NI shells via *ports*. At each port, point-to-point connections can be configured, their maximum number being selected at NI instantiation time. A port can have multiple connections to allow differentiated traffic classes, in which case there are also *connid* signals to select on which connection a message is supplied or consumed.

EX1005, 4



EX1005, FIG. 3

Dr. Hassoun Second Deposition

Q. Radulescu discloses that a *Connid* signal is used to select a connection, correct?

A. That's what it's disclosed, yes.

EX2084, 101:7-9

Dr. Hassoun First Declaration

Rădulescu2004 also teaches communication service mapping that is implemented on the chip, as I explain in further detail in my discussion of element [6.d]. For example, the *Æthereal* NoC “offers its services on *connections*”, which are identified by “*connid*” signals”. *Id.* 2 §2. *Connid* signals are used to “select on which connection a message is supplied or consumed.” *Id.* 3

EX1003, ¶122

Ground 2: Petitioner Has Not Met Its Burden
to Show Obviousness Over Rădulescu2004 in
view of OCP

Ground 2:
Purported
Obviousness by
Rădulescu2004
in view of OCP

A POSITA WOULD NOT BE
MOTIVATED TO COMBINE
(CLAIMS 1-7)

The Petition Overlooked That OCP's MAddrSpace and MThreadID Signals are Merely Optional

Petition

Furthermore, a POSA would have been motivated to look to OCP's disclosure for the format and content of request messages that would be sent by system initiator modules to these adapters. *Id.*, ¶156-157. These requests include “command, control and possibly data” (Ex-1006, 14) and utilize the signals shown in OCP's Table 12:

Table 12 OCP Signal Groups

Group	Signal	Condition
Request	MAddr	always
	MAddrSpace	always
	MBurst	always
	MByteEn	always
	MCmd	always
	MConnID	always
	MData*	datahandshake = 0
	MThreadID	always

Petition, 38

The Petition Overlooked That OCP's MAddrSpace and MThreadID Signals are Merely Optional

OCP interface signals are grouped into dataflow, sideband, and test signals. A small set of the signals from the dataflow group called the basic OCP, is required in all OCP configurations. Optional signals can be configured to support additional core communication requirements. The optional dataflow signals are divided into simple and complex extensions. All sideband and test signals are optional.

EX1006, 23

Simple Extensions

Table 4 lists the simple OCP extensions. The extensions add address spaces, byte enables, burst support, datahandshake, and response flow control.

Table 4 Simple OCP Extensions

Name	Width	Driver	Function
MAddrSpace	1-8	master	Address space
MBurst	3	master	Burst code
MByteEn	1/2/4/8/16	master	Byte enables
MDataValid	1	master	Write data valid
MRespAccept	1	master	Master accepts response
SDataAccept	1	slave	Slave accepts write data

EX1006, 24

Complex Extensions

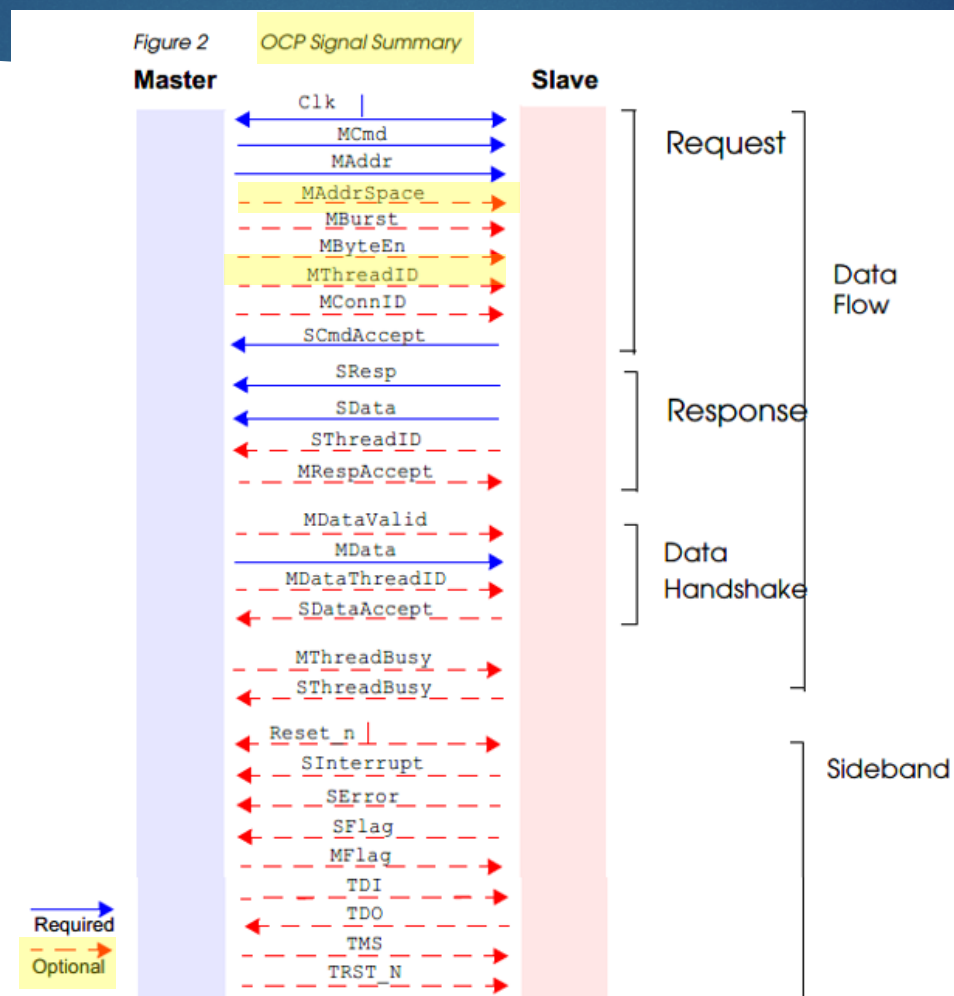
Table 6 shows a list of complex OCP extensions. The extensions add support for threads and connections.

Table 6 Complex OCP Signal Extensions

Name	Width	Driver	Function
MConnID	1-8	master	Connection identifier
MDataThreadID	1-4	master	Write data thread identifier
MThreadBusy	1-16	master	Master thread busy
MThreadID	1-4	master	Request thread identifier
SThreadBusy	1-16	slave	Slave thread busy
SThreadID	1-4	slave	Response thread identifier

EX1006, 27

The Petition Overlooked That OCP's MAddrSpace and MThreadID Signals are Merely Optional



Petitioner Failed to Show a Motivation to use OCP's Optional MThreadID Signal in Rădulescu2004

Petition

One of the Request signals is “MThreadID,” which “provides the thread identifier associated with the current transfer request.” *Id.*, 28; Ex-1003, ¶157. OCP describes numerous advantages of employing threads, including “support[ing] many different burst styles” (*id.*, 46), “support[ing] concurrent activity, and out-of-order completion of transfers” (*id.*) and “enable[ing] busy targets ... to prioritize requests” (*id.*, 181). Rădulescu2004 also teaches the advantages of using connection properties to improve performance of data transfer in an interconnection. Ex-1005, 2; Ex-1003, ¶131. Thus, a POSA would have been motivated to use the OCP threads in the system of Rădulescu2004 in order to achieve these known benefits of threading. Ex-1003, ¶¶156-160.

Petitioner Failed to Show a Motivation to use OCP's Optional MThreadID Signal in Rădulescu2004

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Dr. Bagherzadeh

would be motivated to make this combination. In particular, Rădulescu2004 already discloses a means for providing ordering. Ex. 1005 at 4 § 4.2 (“To provide in-order response delivery, the narrowcast must also keep a history of connection identifiers of the transactions including responses ... In-order delivery per slave of request messages is already provided by the point-to-point connections.”). Similarly, as Dr. Hassoun admits, Rădulescu2004 already provides differentiated traffic classes. Ex. 1003 at ¶ 166 (“Rădulescu2004 also teaches that one of the benefits of its NoC system is that it allows ‘differentiated services’ and ‘differentiated traffic classes’”; Ex. 1005 at 3 § 4.1 (“A port can have multiple connections to allow differentiated traffic classes”).

EX2070, ¶1206

177 (citing Ex. 1006 at 180-181). I disagree that a POSITA would be motivated to make this combination. In particular, Rădulescu2004 already discloses a means for providing priority information. Ex. 1005 at 2 § 2 (“to each channel, properties are attached, such as guaranteed message delivery or not, in order or un-ordered message delivery, and with or without timing guarantees.”). A POSITA would understand that providing guaranteed message delivery and timing guarantees is equivalent to providing priority information.

EX2070, ¶1207

208. Therefore, the alleged benefits of Dr. Hassoun’s proposed combinations (both with respect to incorporating the MAddrSpace signal and the Thread ID into Rădulescu2004) are already realized in Rădulescu2004 without the combination of OCP. A POSITA would realize that there is no benefit gained from these combinations.

EX2070, ¶1208

Petitioner Failed to Show a Motivation to use OCP's Optional MAddrSpace Signal in Rădulescu2004

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Dr. Hassoun's First Deposition

Q. And it doesn't say here that the M address space signal is required in every OCP request, correct?

A. Well, just -- just to be clear what that means, that means a system that implements these extensions would need to have that address signal -- that M address space signal included. And the system that doesn't use those extensions would not need to have it. But the signal itself would be required if the system is architected to use OCP with the extensions.

Q. But you would agree that there can be OCP requests that do not include the M address space signal, right?

A. Same answer. It depends on how you architected the system. So if you've architected the system that you're not going to use the extensions, then you wouldn't need it. But if you've architected the system that that's a requirement, then that would be a requirement in that system.

Dr. Hassoun's Second Declaration

This is because some architectures take advantage of the MAddrSpace signals to identify the "address region of a transfer" such as "the register space versus the regular memory space." Ex. 1006, 26. The MAddr signal would then provide the location within the "address region" in order to identify the proper data. This is

EX1030, ¶139

Petitioner Failed to Show a Motivation to use OCP's Optional MAddrSpace Signal in Rădulescu2004

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Dr. Bagherzadeh

177. Dr. Hassoun fails to articulate why a POSITA would be motivated to use the optional MAddrSpace signal extension in Rădulescu2004's system. Ex. 1003 at ¶¶ 172-173. Dr. Hassoun merely opines that a "POSA would have understood that MAddr and MaddrSpace identify a system target (*i.e.*, second processing module) and/or a memory region within the system target" (*id.* at ¶ 172) and concludes that, for this reason, "a POSA would have been motivated to implement the OCP protocol, including its ... address range teachings, in the system of Rădulescu2004" (*id.* at ¶ 173). I disagree. As I explained above, Rădulescu2004 discloses a communication service identifier in the form of an address (not the claimed "address range") to select "the slave for which the transaction is destined." *Supra* § IX.A.1.i.b; Ex. 1005 at 4 § 4.2. A POSITA would

EX2070, ¶177

178. Rădulescu2004 also provides that "narrowcast connections provide a simple, low-cost solution for a single shared address space mapped on multiple memories." Ex. 1005 at 3 § 4. A POSITA would understand that Rădulescu2004's narrowcast connection already provides a means for "identify[ing] a ... memory region within the system target." Ex. 1003 at ¶ 172. Therefore, a POSITA would know that the optional MAddrSpace extension in OCP is not required in Rădulescu2004's system to identify a memory region. A POSITA would find no benefit in using the optional MAddrSpace extension in Rădulescu2004's system, therefore, a POSITA would not be motivated to combine OCP and Rădulescu2004 in the way Dr. Hassoun proposes.

EX2070, ¶178

Ground 2: Purported Obviousness over Rădulescu2004 in view of OCP

OCP DOES NOT CURE THE
DEFICIENCIES OF
RĂDULESCU2004

No Mapping “According to” OCP’s Optional Signals

Radulescu2004 and OCP Describe Different Types of “Connections”

Petition

In addition, mapping requests to connections according to a communication service identification comprising a Thread ID would have been obvious in view of OCP. Ex-1003, ¶176. As discussed above, OCP describes that requests from a system initiator may include a thread ID. *See supra* IX.B.2; *see also* Ex-1006, 22, 181; Ex-1003, ¶¶156-157. In addition, like Rădulescu2004, OCP describes the use of “connections,” for the transfer of requests with specified communication properties over an interconnect. Ex-1006, 22, 47, 120 (“The components of a chip are joined together using connections.”), 180–181; Ex-1003, ¶¶176-177. OCP further explains that the thread identifier (MThreadID) is mapped to a connection identifier (MConnID) during the request phase. Ex-1006, 47 (describing that the

No Mapping “According to” OCP’s Optional Signals

The “connections” in Rădulescu2004 and OCP are different

Dr. Bagherzadeh

connectionless communication protocol. While I understand that OCP uses the term “connection,” that term is a misnomer and does not exemplify the type of “connection” disclosed in Rădulescu2004 and the ‘052 Patent. *See e.g.*, Ex. 1006 at

(emphasis in original). This is because network-based connections (such as those disclosed in Rădulescu2004 and the ‘052 Patent) transmit data in the form of packets or flits, while the “connection” disclosed in OCP transmits data in the form of a transaction (i.e., via the OCP protocol). *See supra* § VIII.A. OCP also provides a “networking analogy” which emphasizes OCP’s lack of packets. Ex. 1006 at 170 (“Using a networking analogy, the thread ID is a level-2 (data link layer) concept, whereas the connection ID more like a level-3 (transport/session layer) concept.”) (emphasis added). A POSITA would understand that packets are not transmitted in the data link, transport, or session layers of the OSI-model; instead, packets are transmitted in the network layer of the OSI-model. The ‘052 Patent specifically discloses a packet-based communication protocol. In particular, the

Dr. Hassoun’s Second Deposition

Q. You would agree that OCP's connections are not the same as the '052 Patent's connections, correct?

A. I don't disagree. They can be the same. But as I say here, they're -- I don't rely on that so it's irrelevant to the analysis.

EX2084, 289:12-17

No Mapping “According to” OCP’s Optional Signals

The “connections” in Rădulescu2004 and OCP are different

Dr. Hassoun’s Second Declaration

connections. *Id.* The combination does not call for the incorporation of OCP’s interfaces into Radulescu2004’s network or that OCP can natively interface with a NoC as Dr. Bagherzadeh suggests. Ex. 2070, ¶191. I point to OCP’s teaching of a

EX1030, ¶47

Sur-Reply

Dr. Hassoun also testified that the proposed “combination *does not call for the incorporation of OCP’s interfaces* in Radulescu2004’s network,” making clear that the combination relies on Rădulescu2004’s network interfaces. EX1030, ¶47. However, Rădulescu2004 does not disclose using the MThreadID signal, let alone mapping the MThreadID signal. See EX1005; EX2070, ¶146. Dr. Hassoun on one hand opines that a POSITA would be motivated to incorporate OCP’s teaching that OCP interfaces map the MThreadID signal to a MConnID but on the other hand states that the interfaces that teach this mapping would *not* be included in the combination. EX1030, ¶47; EX1006, 38-39, 46-47. Petitioner provides no evidence how Rădulescu2004’s interface would map OCP’s MThreadID signal, or why a POSITA would be motivated to perform mapping using that signal in Rădulescu2004’s interface.

Sur-Reply, 14-15

Claim Construction

CLAIM 6
THE PREAMBLE IS LIMITING

The Preamble of Claim 6 is Limiting

The Parties' Agreed Construction in District Court

Patent	Claim	Term	Agreed Construction
'818	1	Preamble	The preamble is limiting.
'449	10		
'052	6		
'9893	4		
'2893	10		

EX1016, 12

Dr. Hassoun's First Deposition

Q. Do you agree that the preamble of Claim 6 is limiting?

A. Yes.

EX2068, 68:9-11

Petitioner Failed to Meet Its Burden of
Proving that Rădulescu2004 and OCP
Qualify as Prior Art

The Petition is Deficient

The Petition violates the Board's rule against incorporating arguments by reference

The Petition

Rădulescu et al., “*An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration*,” Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (DATE’04) (“Rădulescu2004”; Ex-1005), is prior art under at least pre-AIA §§ 102(a)–(b). Ex-1018 (demonstrating public availability by February 20, 2004); Ex-1012, ¶¶5–23 and accompanying exhibits (same); Ex-1015 at 3 (admitting public availability by the end of February 2004). Rădulescu2004 is prior art under pre-AIA § 102(b) because it was available to the public more than one year prior to the effective U.S. filing date of March 7, 2005. *E.g.*, pre-AIA 35 U.S.C. §102(b) (relevant date is “filing of the application *in this country*”) (emphasis added); pre-AIA 35 U.S.C. §119(a); MPEP §2133; *LG Elecs., Inc. v. Core Wireless Licensing S.A.R.L.*, IPR2015-01988, Paper 31 at 26–28 (PTAB Mar. 16, 2017).

Petition, 2-3

Open Core Protocol Specification, Release 1.0, OCP-IP Association (2001) (“OCP”; Ex-1006). OCP was published in 2001 and is prior art under at least pre-AIA §§102(a)–(b). Ex-1013 (demonstrating public availability by August 2003); Ex-1019 (demonstrating public availability by October 2003); *see also* Ex-1001, 2:65–3:2 (referencing “modern on-chip communication protocols such as ... Open Core Protocol OCP”), 4:15–18, 6:30–38 (“Standard interface (e.g., ... OCP”, “existing on-chip protocols, such as ... OCP”), 6:44–47, 8:41–46 (“existing protocols like . . . Open Core Protocol Specification”), 8:56–59 (same); Ex-1005 at Abstract (“existing bus protocols such as ... OCP”).

Petition, 3

The Petition is Deficient

The Petition violates the Board's rule against incorporating arguments by reference

37 C.F.R. § 42.22(a)(2)

The petition “must include ... a detailed explanation of the significance of the evidence including material facts”

37 C.F.R. § 42.6(a)(3)

“arguments must not be incorporated by reference from one document to another”

***Cisco Sys., Inc. v. C-Cation Techs., LLC,*
IPR2014-00454, Paper 12 at 9 (PTAB Aug. 29, 2014)**

Improper to blanketly cite exhibits “to support conclusory statements for which the Petition does not otherwise provide an argument or explanation”

The Petition is Deficient

The Petition violates the Board's rule against incorporating arguments by reference

Medivis, Inc. v. Novarad Corp.,
IPR2023-00042, Paper 35 at 28-30 (PTAB Mar. 6, 2024)

refusing to consider a declaration and finding Petitioner did not meet its burden of establishing that a reference was publicly accessible prior art because **Petitioner “merely cites [a] declaration without discussion”** and “[t]his terse citation improperly attempts to incorporate by reference the content of the declaration. **But arguments and information not presented and developed in a brief, which are instead incorporated by reference, are not entitled to consideration.**”

Petitioner Did Not Meet its Burden for OCP

Petitioner Has Not Shown That OCP was Publicly Accessible

Petition

Open Core Protocol Specification, Release 1.0, OCP-IP Association (2001) (“OCP”; Ex-1006). OCP was published in 2001 and is prior art under at least pre-AIA §§102(a)–(b). Ex-1013 (demonstrating public availability by August 2003); Ex-1019 (demonstrating public availability by October 2003); *see also* Ex-1001, 2:65–3:2 (referencing “modern on-chip communication protocols such as ... Open Core Protocol OCP”), 4:15–18, 6:30–38 (“Standard interface (e.g., ... OCP”, “existing on-chip protocols, such as ... OCP”), 6:44–47, 8:41–46 (“existing protocols like . . . Open Core Protocol Specification”), 8:56–59 (same); Ex-1005 at Abstract (“existing bus protocols such as ... OCP”).

Petition, 3

EX1013

AFFIDAVIT OF NATHANIEL E FRANK-WHITE

1. I am a Records Request Processor at the Internet Archive. I make this declaration of my own personal knowledge.

EX1013, 1

EX1019

DECLARATION OF NATHANIEL E FRANK-WHITE

1. I am a Records Request Processor at the Internet Archive. I make this declaration of my own personal knowledge.

EX1019, 1

Petitioner Did Not Meet its Burden for OCP

Petitioner Has Not Shown That OCP was Publicly Accessible

Grunenthal GMBH v. Antecip Bioventures II LLC,
PGR2017-00022, Paper 50 at 18-19 (PTAB Nov. 14, 2018)

Internet Archive affidavit “is insufficient by itself” and petitioner did not establish that the materials “would have been located online by interested [POSITAs] exercising reasonable diligence”

Schlumberger Tech. Corp. v. Integrated Drive Sys. LLC
IPR2018-00603, Paper 40 at 16-17, 23-24 (PTAB Sept. 3, 2019)

finding no public accessibility where
“Petitioner’s evidence ... amounts to little more than the ... testimony of [the Wayback Machine declarant] that Joy was available on the Internet by [a certain date]”

Petitioner Did Not Meet its Burden for OCP

Petitioner Has Not Shown That OCP was Publicly Accessible

EX1013

https://web.archive.org/web/20030828000312/http://www-micrel.deis.unibo.it/~benini/NOC/OCP-IP_OpenCoreProtocolSpecification-1.0.pdf

EX1013, 4

Acceleration Bay, LLC v. Activision Blizzard Inc.
908 F.3d 765, 774 (Fed. Cir. 2018)

“ultimate question is whether the reference was ‘available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, can locate it.’ ”

Hulu, LLC v. Sound View Innovations, LLC
IPR2018-01039, Paper 29 at 8-11 (PTAB Dec. 20, 2019)

“reference is publicly accessible upon a satisfactory showing that such document was disseminated or otherwise made available to the extent that [POSITAs] exercising reasonable diligence can locate it.”

Petitioner Did Not Meet its Burden for OCP

Dr. Dutt's Testimony Does Not Establish that OCP was Publicly Accessible

Dr. Dutt Second Deposition

Q The URL in paragraph 19 of your second -343 declaration was provided to you by your attorneys, correct?

A That's correct.

Q So you did not independently search for and find this URL in paragraph 19 of your second -343 declaration, correct?

A That is correct.

EX2085, 52:1-8

And so I'll ask again: In preparing your second -343 declaration, did you try following any of the hyperlinks shown in Exhibit 1019 to access the OCP document?

THE WITNESS: I did not physically click on the links. But I did have access to -- just to finish that,

EX2085, 50:14-21

Q In Exhibit 1039, the citation to OCP data sheet does not indicate a particular version of OCP, correct?

THE WITNESS: This particular paper does not specify the -- the version of the OCP.

EX2085, 58:5-9

Petitioner Did Not Meet its Burden for Rădulescu2004

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The Petition violates the Board's rule against incorporating arguments by reference

The Petition

Rădulescu et al., “*An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration*,” Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (DATE’04) (“Rădulescu2004”; Ex-1005), is prior art under at least pre-AIA §§ 102(a)–(b). Ex-1018 (demonstrating public availability by February 20, 2004); Ex-1012, ¶¶5–23 and accompanying exhibits (same); Ex-1015 at 3 (admitting public availability by the end of February 2004). Rădulescu2004 is prior art under pre-AIA § 102(b) because it was available to the public more than one year prior to the effective U.S. filing date of March 7, 2005. *E.g.*, pre-AIA 35 U.S.C. §102(b) (relevant date is “filing of the application *in this country*”) (emphasis added); pre-AIA 35 U.S.C. §119(a); MPEP §2133; *LG Elecs., Inc. v. Core Wireless Licensing S.A.R.L.*, IPR2015-01988, Paper 31 at 26–28 (PTAB Mar. 16, 2017).

Petition, 2-3

EX1012

DECLARATION OF NIKIL DUTT, PH.D. UNDER 37 C.F.R. § 1.68

EX1012, 1

EX1018



DECLARATION OF GORDON MACPHERSON

EX1018, 1

Petitioner Did Not Meet its Burden for Rădulescu2004

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Petitioner Has Not Shown That Rădulescu2004 was Accessible at the DATE04 Conference

Power Integrations, Inc. v. Semiconductor Components Indus., LLC, IPR2017-01904, Paper 9 at 11-18 (PTAB Mar. 12, 2018)

Petitioner failed to establish public accessibility because:

1. Petition included “single sentence” argument that reference was “published”;
2. Despite testimony that reference was presented at a conference, no evidence that conference was attended by POSITAs or that witness himself was a POSITA; and
3. No evidence whether reference was “provided to conference attendees with or without restriction”

Petitioner Did Not Meet its Burden for Rădulescu2004

103

Petitioner Has Not Shown That Rădulescu2004 was Accessible at the DATE04 Conference

POSITA Definition

A POSA with respect to the '052 patent would typically have had at least either a Master's degree in Electrical Engineering or a related field (such as computer science or computer engineering), as well as at least three years of work experience in the field of SoC design, or a Bachelor's degree in Electrical Engineering or a related field, as well as at least five years of work experience in the field of SoC design. Ex-1003, ¶32. This POSA would have had an understanding of SoC interconnects, as well as the concepts of large-scale networks. *Id.*

Petition, 13-14

Petitioner Did Not Meet its Burden for Rădulescu2004

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There Is No Evidence That DATE04 Was Attended By POSITAs

Dr. Dutt First Deposition

Q Do you have any industry experience with system on a chip design?

THE WITNESS: I'd have to go back and look up my resume in detail to see if I've had engagements on that. So I don't think I'm prepared to answer that question at this time.

EX2067, 82:15-21

Q Just to be clear, you're refusing to answer as to your understanding of what a system on a chip is?

THE WITNESS: I haven't talked enough about it to be able to speak about it today. So I'm not prepared to talk about things other than the items that are in my declaration.

EX2067, 81:14-20

Q Are you familiar with large scale networks?

THE WITNESS: Certainly I've heard of that phrase. But I don't think I'm prepared to discuss anything about that in detail since I haven't prepared for it for this deposition.

EX2067, 82:15-20

Petitioner Did Not Meet its Burden for Rădulescu2004

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DATE04 Attendees Could Not Disseminate Conference Papers

Dr. Dutt First Deposition

Q Were you allowed to upload them online?

A You know, I don't remember what was the situation in 2004. I don't even remember if you had things at the point where you had stuff. I probably think there was a web page online. But you -- as attendee, you were not allowed to distribute the papers yourself without permission from IEEE ACM because they're held -- they're copyright by IEEE ACM.

EX2067, 39:25-40:7

Petitioner Did Not Meet its Burden for Rădulescu2004

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Mr. MacPherson's Testimony Does Not Establish That Rădulescu2004 Was Publicly Available

Mr. MacPherson (IEEE) Deposition

I asked, would it be fair to say that you cannot attest to whether the underlying information, including the metadata, which was received from the conference organizers, is accurate?

A. Yes.

EX2069, 26:6-10

Q. You don't have any personal knowledge regarding the conference in February 2004, right?

A. No, I don't.

EX2069, 20:25-21:2

Q. And does IEEE do anything to independently verify the accuracy of that metadata?

A. At the time of this conference, it predates my time at IEEE by a few years.

EX2069, 16:6-9

Q. So would it be fair to say that you're unsure whether IEEE would do any verification of the metadata in 2004?

A. That's right.

EX2069, 16:17-20