

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED and
SAMSUNG ELECTRONICS CO., LTD.,
Petitioners

v.

NETWORK SYSTEM TECHNOLOGIES, LLC,
Patent Owner

Case IPR2024-00355

U.S. Patent No. 8,072,893

PETITION FOR *INTER PARTES* REVIEW OF
U.S. PAT. NO. 8,072,893

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Ex-1004	Curriculum Vitae of Dr. Marwan Hassoun
Ex-1005	D. Bertozzi, L. Benini, “ <i>Xpipes: A Network-on-Chip Architecture for Gigascale Systems-on-chip</i> ”, IEEE Circuits and Systems Magazine (2004) (“Bertozzi”)
Ex-1006	Networks on Chip, Axel Jantsch, Hannu Tenhunen (Eds.), Kluwer Academic Publishers, Boston (2003) (“Jantsch”)
Ex-1007	J. Dielissen, et al. “ <i>Concepts and Implementation of the Philips Network-on-Chip</i> ,” Philips Research Laboratories, Eindhoven, The Netherlands (2003) (“Dielissen”)
Ex-1008	Design and Reuse Website, https://www.design-reuse.com/search/?area=full&i=Concepts+and+Implementation+of+the+Philips+Network-on-Chip
Ex-1009	Duato et al., Interconnection Networks: An Engineering Approach, IEEE Computer Society (1997)
Ex-1010	M. Dall’Osso, et al. “ <i>Xpipes: a Latency Insensitive Parameterized Network-on-chip Architecture for Multi-Processor SoCs</i> ”, 21st International Conference on Computer Design (2003)
Ex-1011	S. Hassoun et al., “ <i>Optimal Buffered Routing Path Constructions for Single and Multiple Clock Domain Systems</i> ”, ICCAD 2002 (2002) (“Hassoun”)
Ex-1012	E. Rijpkema et al., “ <i>Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip</i> ”, IEEE Proceedings – Computers and Digital Techniques (2003) (“Rijpkema”)

¹ All pin citations are to the branded numbers added by Petitioners in the bottom right corner of the exhibits, except citations to patents and published applications, which are cited to the column/line number or paragraph number.

Ex-1013	U.S. Patent No. 6,614,320 (“Sullam”)
Ex-1014	U.S. Patent No. 6,081,844 (“Nowatzky”)
Ex-1015	A. Shaw, “ <i>Fixed Length Packets versus Variable-Length Packets in Fast Packet Switching Networks</i> ”, The Conference on Computer Communications, IEEE INFOCOM '93 (1994) (“Shaw”)
Ex-1016	William J. Dally et al., “ <i>Route Packets, Not Wires: On-Chip Interconnection Networks</i> ,” Proceedings – Design Automation Conference (2001) (“Dally”)
Ex-1017	P. Guerrier et al., “ <i>A Generic Architecture for On-Chip Packet-Switched Interconnections</i> ,” <i>Proceedings Design, Automation and Test in Europe Conference and Exhibition 2000</i> (2000) (“Guerrier”)
Ex-1018	Kumar et al., “ <i>A Network on Chip Architecture and Design Methodology</i> ,” IEEE Computer Society Annual Symposium (2002) (“Kumar”)
Ex-1019	Network System Technologies, LLC’s Infringement Contentions, Appendix B-5, <i>Network System Technologies, LLC v. Qualcomm Inc. et al.</i> , 1:22-cv-01331 (W.D. Tex.)
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Ex-1021	Declaration of Sylvia Hall-Ellis, Ph.D.
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Ex-1025	Defendant’s Opening Claim Construction Brief, <i>Network System Technologies, LLC v. Qualcomm Inc. et al.</i> , 1:22-cv-01331 (W.D. Tex.)
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Ex-1027	Declaration of Dr. Erik Chmelar, <i>Network System Technologies, LLC v. Qualcomm Inc. et al.</i> , 1:22-cv-01331 (W.D. Tex.)
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Ex-1031	Network System Technologies, LLC, Exhibit 024 (Attachment to Complaint), <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al</i> , No. 2:2022-cv-00481 (E.D. Tex.)
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Ex-1034	S. Gibilisco, <i>The Illustrated Dictionary of Electronics</i> , McGraw-Hill, Eighth Edition (2001)
Ex-1035	Excerpt of <i>The Authoritative Dictionary of IEEE Standards Terms</i> , Seventh Edition (2000)
Ex-1036	U.S. Patent No. 7,366,818 (“Rădulescu”)

I. INTRODUCTION

Qualcomm Incorporated (“Qualcomm”) and Samsung Electronics Co., Ltd. (“Samsung”) (collectively “Petitioners”) request *inter partes* review (“IPR”) of claims 1–3 and 6–10 (“Challenged Claims”) of U.S. Patent No. 8,072,893 (“the ’2893 patent”; Ex-1001).

The ’2893 patent is directed to inserting data storage elements into a data communication network to introduce a certain amount of delay on a communication channel. The alleged improvement relates to the maintenance of the correct periodicity between network stations, e.g., routers and network interfaces, connected by the communication channel.

Prior art references—such as Bertozzi—disclose a pipelined communication channel where data storage elements are inserted into the data communication network in such a number as to satisfy the Challenged Claims. Further, a number of prior art references teach the well-known concept of pipelined communication channels, including in network-on-chip (“NoC”) applications. Thus, for the reasons shown herein, the Challenged Claims are unpatentable in view of the prior art and Petitioners respectfully request that they be cancelled.

II. GROUNDS FOR STANDING

Petitioners certify that IPR is available for the ’2893 patent. Petitioners are not barred or estopped.

III. IDENTIFICATION OF THE CHALLENGE

A. Prior Art

The '2893 patent has an effective U.S. filing date of April 20, 2006 (PCT Application PCT/IB2006/051218).

Bertozzi et al., “*Xpipes: A Network-on-Chip Architecture for Gigascale Systems-on-Chip*,” IEEE Circuits and Systems Magazine, pp. 18-31 (Second Quarter 2004) (“Bertozzi”; Ex-1005), is prior art under at least pre-AIA §§ 102(a)–(b). Ex-1020 and Ex-1021 (demonstrating public availability by October 2004). Bertozzi is prior art under pre-AIA § 102(b) because it was available to the public more than one year prior to the effective U.S. filing date of April 20, 2006. *E.g.*, pre-AIA 35 U.S.C. § 102(b) (relevant date is “filing of the application *in this country*”) (emphasis added); pre-AIA 35 U.S.C. § 119(a); MPEP §2133; *LG Elecs., Inc. v. Core Wireless Licensing S.A.R.L.*, No. IPR2015-01988, Paper 31 at 26–28 (PTAB Mar. 16, 2017).

Jantsch, Axel and Tenhune, Hannu (Eds.), *Networks on Chip*, Kluwer Academic Publishers (2003) (“Jantsch”; Ex-1006). Jantsch is prior art under at least pre-AIA §§ 102(a)–(b). Ex-1021 (demonstrating public availability no later than May 12, 2003).

Duato et al., *Interconnection Networks: An Engineering Approach*, IEEE Computer Society Press (1997) (“Duato”; Ex-1009). Duato is prior art under at

least pre-AIA §§ 102(a)–(b). Ex-1021 (demonstrating public availability no later than March 19, 1998).

Dielissen et al., *Concepts and Implementation of the Philips Network-on-Chip*, IP BASED SOC DESIGN, Grenoble, France (2003) (“Dielissen”; Ex-1007). Dielissen is prior art under at least pre-AIA §§ 102(a)–(b). Ex-1022 (demonstrating public availability by January 16, 2004); *see also* Ex-1008 and Ex-1033 (Resp. to RFA No. 2).

Hassoun et al., *Optimal Buffered Routing Path Constructions for Single and Multiple Clock Domain Systems*, IEEE/ACM International Conference on Computer Aided Design (2002) (“Hassoun”; Ex-1011). Hassoun is prior art under at least pre-AIA §§ 102(a)–(b). Ex-1024 (demonstrating public availability by November 14, 2002).

Sullam et al., U.S. Patent No. 6,614,320 (“Sullam”; Ex-1013). Sullam was patented Sep. 2, 2003 and is prior art under at least pre-AIA §§ 102(a)–(b), (e).

B. Grounds for the Challenge

Petitioners contend that there is a reasonable likelihood that at least one of the Challenged Claims is invalid as obvious or anticipated, and respectfully requests cancellation of all unpatentable claims.

Ground	Claims	Basis for Unpatentability
Ground 1	1–3, 6–7, 10	Anticipated by Bertozzi
Ground 2	1–3, 6–7, 10	Obvious over Bertozzi alone, or in further view of Jantsch or Duato
Ground 3	1–3, 6–7, 9–10	Obvious over Dielissen in view of Hassoun
Ground 4	8	Obvious in view of Grounds 1-3, further in view of Sullam

IV. THE '2893 PATENT

A. Overview of the '2893 Patent

The '2893 patent describes an integrated circuit including “functional blocks and a data communication network having network stations interconnected via communication channels for communicating data packages between the functional blocks.” Ex-1001, Abstract.

The '2893 patent discloses that NoCs are used to “facilitate flexible communication on the one hand and to limit the amount of wires required on the other hand.” *Id.*, 1:19–25. Such NoCs “typically comprise a plurality of network stations, each associated with a functional block, interconnected via communication channels, e.g. wires.” *Id.*

Network stations include data routers and network interfaces. *Id.*, 1:25–28. Data “can be communicated over the network in the form of packages....” *Id.*, 1:28–30. Data packages are described as having a “fixed size of N data elements,” where one of the data elements has routing information. *E.g., id.*, 2:15–33, 2:2–5, 6:35–38.

The '2893 patent discloses that a “problem associated with communication channels, e.g. wires, on ICs [(integrated circuits)] is that the clock speed at which the IC can operate may be determined by the slowest communication channel, i.e. the channel exhibiting the largest data transfer delay.” *Id.*, 1:34–38. A known solution was to “introduce a data storage element such as a latch into the slowest data communication channel.” *Id.*, 1:41–46. In that way, “the clock speed of the data communication part of the IC can be increased at the expense of an additional clock cycle for the communication along the slowest communication channel.” *Id.*

However, the '2893 patent teaches that this solution causes issues in network stations, such as routers, that are designed to “receive[] the routing data incorporated in the data packet during a *predefined clock cycle*.” *Id.*, 1:47–61 (emphasis added). To address this, the '2893 patent teaches to insert “M*N data storage elements . . . for introducing a delay of M*N cycles on the” communication channel, where “each data package compris[es] N data elements” and M is “a positive integer” *Id.*, 1:65–2:17; *see also id.*, 5:63–6:12, 7:11–12, Figs. 1–4 (examples where M=1 and M=2).

Figure 1 illustrates “network 100... is arranged to communicate data packages with size N=3.” *Id.*, 5:63–64. Three data storage elements 160 are inserted into both the first subchannel 152 and the second subchannel 154 (highlighted in yellow), such that M*N data storage elements (here six, with three

on each subchannel) have been inserted into communication channel 150, where “M=2” and “N=3”:

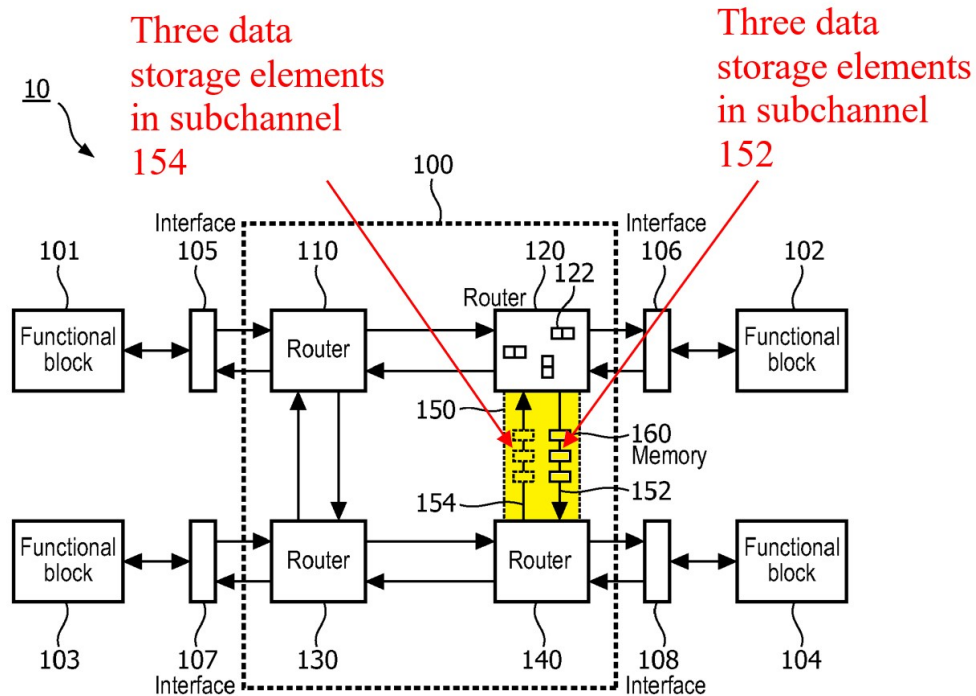


FIG. 1

Ex-1001, Fig. 1 (annotations added), 5:5–10, 5:49–6:2; Ex-1003, ¶62. These data storage elements introduce a total delay of $M \cdot N$ cycles (here six, with a delay of three cycles on each subchannel). Ex-1003, ¶62.

B. Prosecution History

The Examiner first rejected the several claims as obvious in view of U.S. Patent No. 7,362,763 (“Wybenga”) and U.S. Patent No 7,197,009 (“Dispensa”). Ex-1002, 125–34. The Applicant amended the claims and argued they were patentable over the prior art. *Id.*, 144–65.

The Examiner rejected claims in view of additional prior art. *Id.*, 169–85.

The Applicant then made several additional amendments to the claims, including adding to Claim 10 the limitation of “in response to the identifying act” and to claim 1 the limitation of “when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold.” *Id.*, 194–206. The amended claims were then allowed. *Id.*, 211–220.

C. The Challenged Claims

Petitioners challenge claims 1–3 and 6–10 of the ’2893 Patent. Because there is substantial overlap between elements of these claims, similar claim elements will be discussed together.

V. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSA”) is a hypothetical person who is presumed to have known the relevant art at the time of the invention. *See* MPEP § 2141.03. A POSA has ordinary creativity, is not an automaton, and is capable of combining the teachings of the prior art. *See, e.g., KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 420–21 (2007).

A POSA with respect to the ’2893 patent would typically have had at least either a master’s degree in electrical engineering, or a related field as well as at least three years of work experience in the field of SoC design, or a bachelor’s

degree in electrical engineering, or related field, as well as at least five years of work experience in the field of SoC design. Ex-1003, ¶32. This POSA would have had an understanding of SoC interconnects, as well as the concepts of large-scale networks. *Id.*

The result would be the same under the level of ordinary skill proposed by Patent Owner NST (“PO”) in related district court proceedings: “a Bachelor of Science (or equivalent) degree in electrical engineering, computer engineering, or a related field, and 2–3 years of work experience in very large-scale integrated (“VLSI”) systems, such as application-specific integrated circuits (“ASICs”), application-specific standard parts (“ASSPs”), system-on-chip (“SoC”), or field-programmable gate arrays (“FPGAs”), and has an understanding of on-chip interconnection networks.” Ex-1026, 11; Ex-1003, ¶¶32–34.

VI. CLAIM CONSTRUCTION

Petitioners interpret the claims of the ’2893 Patent according to the *Phillips* claim construction standard. 37 C.F.R. § 42.100(b). Petitioners identify several claim terms at issue in pending district court litigation below, but Petitioners do not believe the Board needs to resolve those disputes to decide the issues raised by this *inter partes* review challenge.

Qualcomm and Patent Owner Network System Technologies, LLC (“PO”) have advanced the following claim constructions in *Network System Technologies, LLC v. Qualcomm Inc. et al.*, No. 1:22-cv-01331 (W.D. Tex.)²:

Term	Qualcomm’s Proposed Construction	PO’s Proposed Construction
“each data package comprising N data elements”	“every data package communicated by the network stations has a fixed size of N data elements”	[PO] incorporates its definition for the term “data package,” “data elements” are groups of data, and the remaining language should be afforded their plain and ordinary meanings.
“data package”	See Defendants’ construction of “each data package comprising N data elements” above.	“Fixed-size arrangement of data”
“data storage elements”	“each being a structure that stores one data element”	“Array of one or more elements that store data.”

Ex-1025; Ex-1026; Ex-1027; Ex-1028. As shown below, the Challenged Claims are unpatentable under both Qualcomm’s proposed constructions and PO’s proposed constructions. Therefore, Petitioners do not believe at this time it is

² Samsung is also involved in litigation with PO concerning the ’2893 Patent.

Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al., No. 2:22-cv-00481 (E.D. Tex.). Claim construction briefing in that case will take place in 2024.

necessary for the Board to expressly construe these terms to resolve the issues in this *inter partes* review.

PO has further clarified its constructions with respect to “data package” and “each data package comprising N data elements.” For example, PO explained that under its interpretation, the number of data elements in each data package traveling through the system “can vary between one data package and the next....” Ex-1026, 31. PO also stated that “the term ‘each data package comprising N data elements’ means that each data package comprises N, or more than N, data elements, i.e., at least N data elements.” Ex-1027, ¶164. As a result, PO’s proposed interpretation is significantly broader than Qualcomm’s proposed construction.

Petitioners reserve the right to identify terms for construction in litigation concerning the ’2893 Patent, and to respond to any constructions that PO submits.

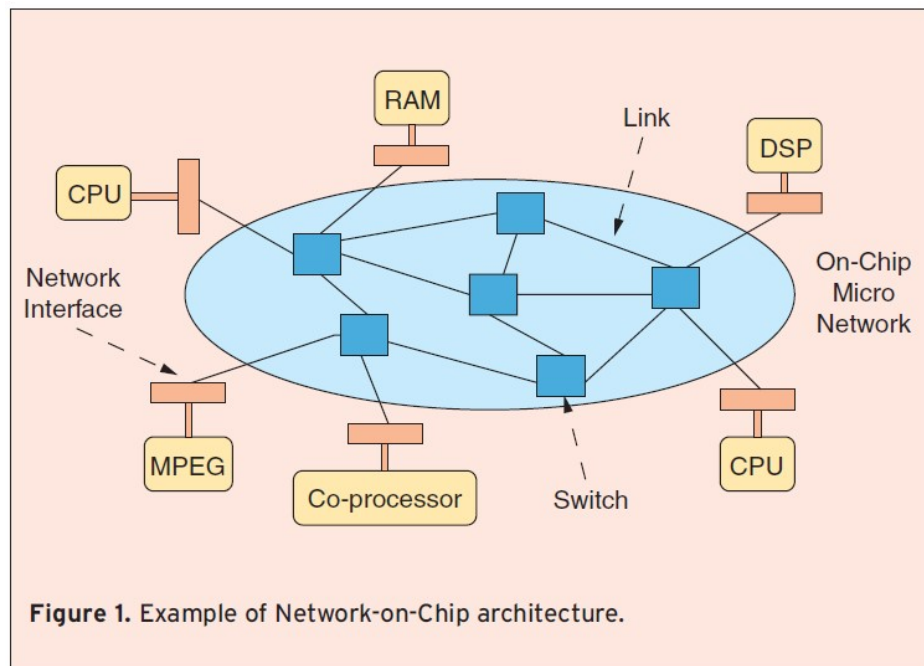
VII. GROUND 1: BERTOZZI ANTICIPATES CLAIMS 1–3, 6–7, AND 10

A. Bertozzi (Ex-1005)

Bertozzi discloses a “Network-on-Chip” (NoC) design architecture called “Xpipes.” Ex-1005, Title, Abstract, 1–2. The Xpipes NoC allows for the communication of data packets (“packetized communication”) between cores (CPUs, RAM, etc.). *Id.*, 2, Fig. 1; Ex-1003, ¶74.

Bertozzi discloses a general “Network-on-Chip” architecture intended to be used for its Xpipes designs. Ex-1005, 2–3; *see also id.* 2 (“The basic idea ...

envisioned on-chip router (or switch)-based networks on which packetized communication takes place”) and 3 (“While describing the basic building blocks of [the Xpipes] solution, the main NoC design principles will be briefly explained”); *see also id.*, 3; Ex-1003, ¶75. Bertozzi shows these components integrated into a NoC below at Figure 1:

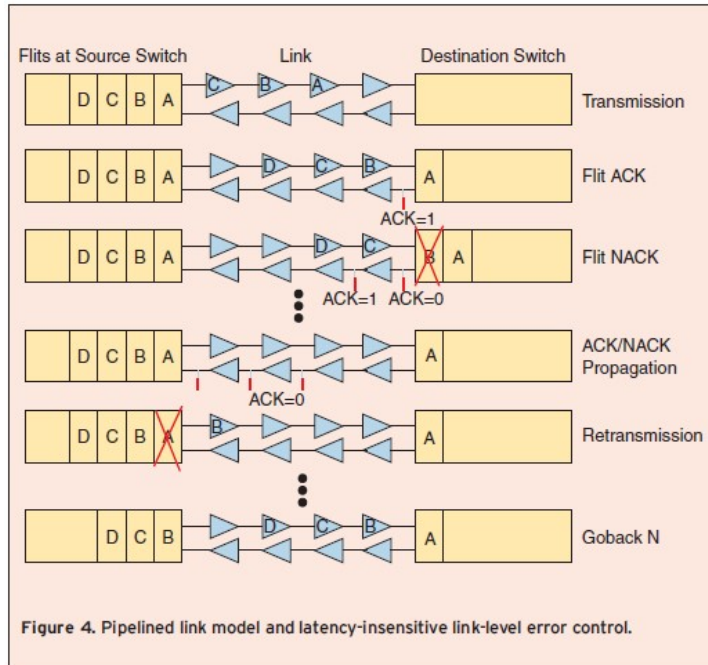


Ex-1005, Fig. 1; Ex-1003, ¶75. Bertozzi also discloses details of the various NoC components depicted in this figure, including the network interfaces, switches and links, which are all part of the same general embodiment. Ex-1005, 2, 5, 7–11, Figs. 4, 5, 7; Ex-1003, ¶75.

Bertozzi also discloses additional general design features of “data packetization” for NoC data packets intended to be used in Bertozzi’s Xpipes

architecture. *E.g.*, Ex-1005, 3, 4–5 (“most relevant tasks of a *network interface (NI)* are . . . data packetization . . .”); Ex-1003, ¶76. Specifically, Bertozzi discloses that “data packetization is a critical task for the network interface” and that messages “are usually partitioned into fixed-length packets.” Ex-1005, 5. Bertozzi further discloses that “[p]ackets in turn are often broken into message flow control units called *flits*” and that “[i]n many implementations a flit is set equal to a phit” (a data element). *Id.*, 5; Ex-1003, ¶¶76–77, 103–110. Bertozzi also discloses that the data packet includes “the packet header, payload and packet tail” and that the header “contains the necessary routing” information. Ex-1005, 5. At Figure 4, Bertozzi shows a specific embodiment of a data packet with four flits A, B, C, and D. Ex-1005, Fig. 4; Ex-1003, ¶77.

Bertozzi explains that “[a] solution to overcome the interconnect-delay problem consists of pipelining interconnects.” Ex-1005, 7. Thus the Xpipes design includes links that are “partitioned into segments (or relay stations, which have a function similar to the one of latches in a pipelined data path)” to break up long links into shorter lengths that “satisf[y] pre-defined timing requirements (e.g., the desired clock speed of the design).” *Id.*, 7; Ex-1003, ¶79. An example of a specific embodiment of Bertozzi’s Xpipes architecture is below, showing links designed to have four relay stations in each subchannel:



Ex-1005, 7, Fig. 4.

B. Independent Claim 10

For ease of presentation, the analysis of the Challenged Claims begins with claim 10, and then addresses the other Challenged Claims. Bertozzi discloses all the limitations of claim 10. Ex-1003, ¶¶93–163.

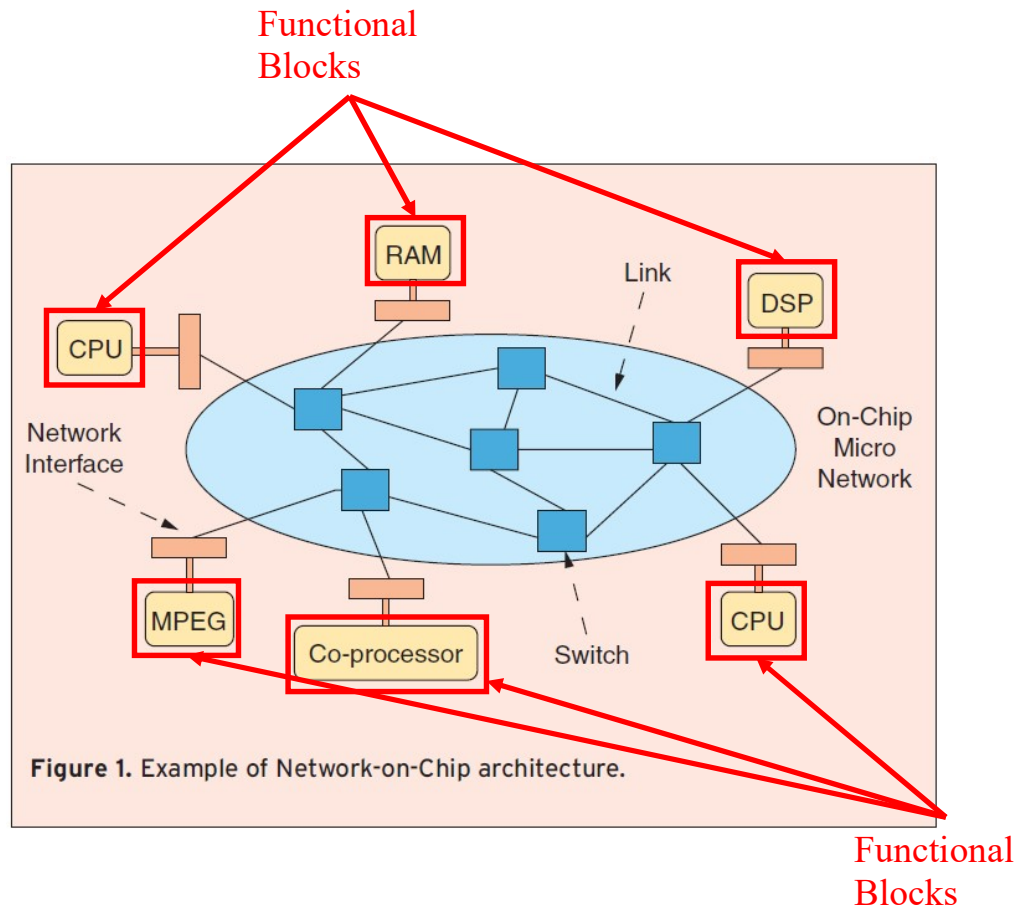
1. [10.pre] A method of designing an integrated circuit comprising

To the extent the preamble is limiting, it is disclosed by Bertozzi. Ex-1003, ¶94. Bertozzi discloses a method for designing an integrated circuit. Ex-1003, ¶¶94, 74–75. Bertozzi teaches the use of the Xpipes architecture and platform to design a NoC interconnect for a System-on-Chip (“SoCs”). *E.g.*, Ex-1005, 3 (“Designing communication architectures for highly integrated deep sub-micron

SoCs...”); *see also id.*, Title, 1–3, 11–12. SoCs are a type of integrated circuit. Ex-1001, 1:8–13; Ex-1003, ¶¶94, 74–75.

2. [10.pre.a] a plurality of functional blocks, and

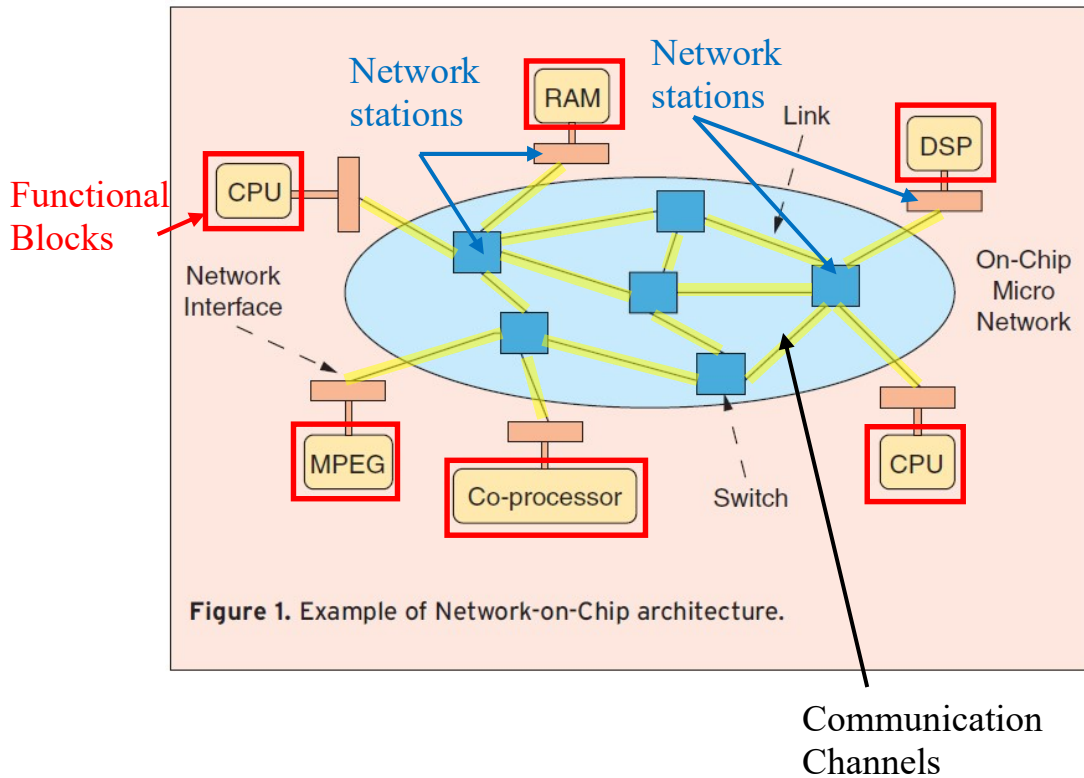
Bertozzi discloses this element. Ex-1003, ¶¶96–97. Bertozzi discloses SoCs with a plurality of cores (*functional blocks*), including “processors, co-processors, DSPs, dedicated hardware accelerators, memory blocks, [and] I/O blocks,” as well as “CPUs” and “RAM” blocks. Ex-1005, 2; Ex-1003, ¶¶96–97, 74–75.



Ex-1005, Fig. 1 (annotated); Ex-1003, ¶97.

3. [10.pre.b] a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks,

Bertozzi discloses this element. Ex-1003, ¶¶98–101. Bertozzi discloses a “Network-on-Chip” (*data communication network*) comprising a plurality of “network interface[s]” and routers or switches (*network stations*) being interconnected via a plurality of “links” (*communication channels*) for communicating data packets (*data packages*) between Bertozzi’s “cores” such as the “CPUs” or “DSP” (the *functional blocks*). Ex-1003, ¶¶98–101; *e.g.*, Ex-1005, Title, Abstract, 2 (describing “on-chip router (or switch)-based networks on which packetized communication takes place . . .”), 3, 5–6 (“Messages that have to be transmitted across the network are usually partitioned into fixed-length packets.”), 5 (“Data packetization is a critical task for the network interface . . . the task of the switch is to carry packets injected into the network to their final destination), Fig. 1, Fig. 4. These elements are annotated below on Bertozzi’s Figure 1:



Ex-1005, Fig. 1; *see also id.*, 3; Ex-1003, ¶100. This is consistent with the '2893 patent, which explains that “network stations” are data routers/switches and/or network interfaces. *E.g.*, Ex-1001, 4:31–33, 5:9–10 (“[n]etwork stations, e.g. data routers 120 and 140.”), 5:51–54; Ex-1003, ¶101.

Bertozzi further discloses that the data packets that are communicated between its “cores” each carry multiple data elements. *E.g.*, Ex-1005, 5, 7–8, Fig. 4 (embodiment showing data packet with four data elements A, B, C, D); Ex-1003, ¶¶98–99, 101, 74–78. Thus, Bertozzi teaches a network for communicating *data packages* as claimed. Ex-1003, ¶¶77, 98–99, 101, 74–78; *see also* Ex-1001, Fig. 2 (showing example of data package with three data elements). As discussed further

below, Bertozzi’s data packets are “data packages” under all of the proposed constructions. Ex-1003, ¶¶98–99, 101.

4. **[10.pre.c] each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two,**

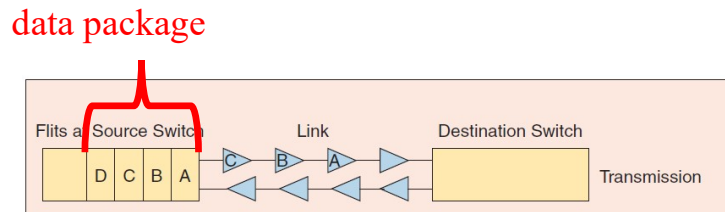
This limitation is disclosed by Bertozzi under all of the proposed constructions. Ex-1003, ¶¶102–126.

Bertozzi discloses that messages in its network can be “partitioned into fixed-length packets” that comprise N flits (*each data package comprising N data elements*). Ex-1005, 5-7 (“Packets in turn are often broken into message flow control units called *flits*.”), Fig. 4; Ex-1003, ¶¶103–110, 116. A POSA would understand that “fixed-length packets” means that each data packet going through the NoC is the same size/length. Ex-1003, ¶¶52–53, 103, 116; Ex-1015, 3; Ex-1035, 3–4 (defining “fixed length” and “fixed format”).

Bertozzi also discloses *data elements* as claimed. Ex-1003, ¶¶103–111, 116 In Bertozzi a flit is set equal to the amount of data sent over one clock cycle. Ex-1005, 9 (“[t]he flit has to propagate across the link (*N* cycles)”); *see also id.*, 5 (“In many implementations, a flit is set to be equal to a *phit*”), 7–9, Fig. 4; Ex-1003, ¶¶103–111. This is exactly how the ’2893 patent uses the term “data

element.”³ Ex-1003, ¶106; *see, e.g.*, Ex-1001, 2:15–22, 6:31–7:2 (“[s]ubsequent data elements d0 and d1 of this data package are received by the data router 120 at respective clock cycles t+1 and t+2.”), Fig. 2.

The number of flits (*data elements*) in Bertozzi’s packet discloses the claimed “each data package comprising N data elements ..., N being an integer of at least two.” Ex-1003, ¶¶103, 114–126. Bertozzi’s Figure 4 shows a data packet (*data package*) that has a fixed length of $N=4$ data elements lettered A through D:



³ The word “flits” also appears once in the ’2893 specification, which notes that data packages are “sometimes” referred to as flits. Ex-1001, 4:56-57. Depending on implementation, a “flit” can have one data element or multiple data elements. Ex-1003, ¶111, 103, 107. In Bertozzi, the flit is set to contain one phit (a *data element*) (flit-to-data element ratio of 1:1); therefore a flit in Bertozzi’s implementation corresponds to a data element. Ex-1003, ¶¶103-111; Ex-1005, 5, 7-9, Figs. 3, 4. In the ’2893 patent, a flit is set to contain multiple data elements (flit-to-data element ratio of 1:3); therefore, in that implementation a flit corresponds to a data package, rather than a data element. Ex-1001, 4:51-57; Ex-1003, ¶111.

Ex-1005, Fig. 4 (annotated); *see also id.*, 7–8; Ex-1003, ¶¶118–120, ¶77 (elements A, B, C, D correspond to a data package). In this figure, $N=4$, which is “an integer of at least two.” Ex-1003, ¶¶118–120, 77. A POSA would also have understood that Bertozzi discloses designing its integrated circuit embodiments for use with fixed length packets. Ex-1003, ¶¶117, 120, 103–104; Ex-1005, 22 (“Messages that have to be transmitted across the network are usually partitioned into fixed-length packets.”). In a network with messages partitioned into “fixed-length” packets, a POSA would have understood that all the packets have the same fixed length (four flits in the Fig. 4 embodiment described above). Ex-1005, 5, 7–8, Fig. 4; Ex-1003, ¶¶52–53, 77, 116–120. In the event that PO argues (incorrectly) that the four flits shown in Fig. 4 are not a packet, a POSA would in any event at once envisage that the example of the fixed-length packets taught by Bertozzi corresponds to a data package having four flits A, B, C, D (each one a data element) as shown in Figure 4. Ex-1003, ¶120, 118–120.

Bertozzi also discloses that its packets, such as the packet in Fig. 4, include a “header” flit (a *data element*) that contains *routing information* for the network stations, and a separate packet tail flit. Ex-1005, 5 (“The header contains the necessary routing and network control information” and “[t]he packet tail indicates the end of a packet and usually contains parity bits for error-detecting or error-

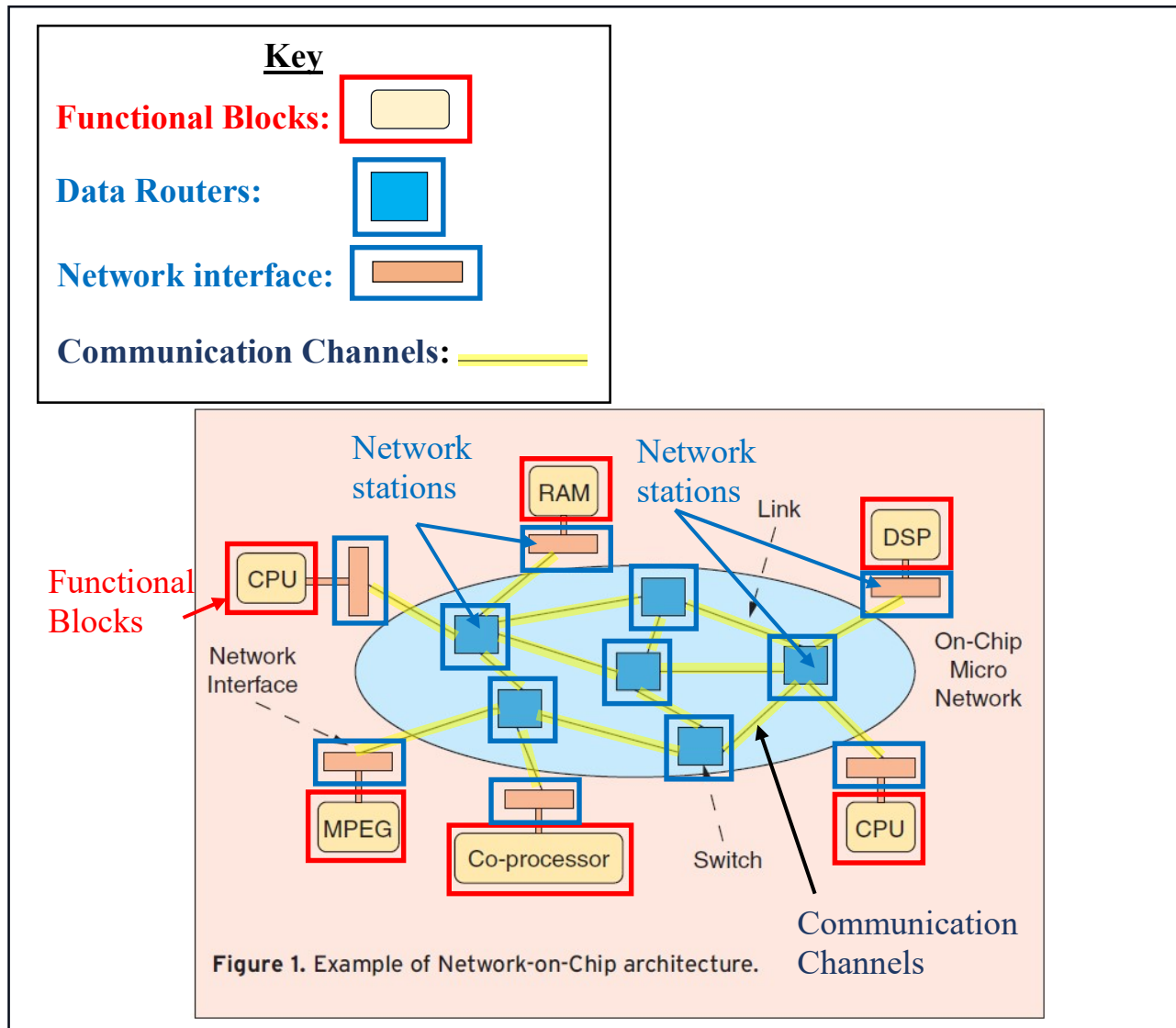
correcting code.”), 6 (“A flit type field allows to identify the head and the tail flit”); *see also id.*, 5, 10–11; Ex-1003, ¶¶112–113, 121.

Bertozzi also discloses this limitation [10.pre.c] under PO’s construction, in multiple ways. Ex-1003, ¶¶122–126. One, Bertozzi discloses this limitation for the same reasons as under Qualcomm’s construction. Ex-1003, ¶¶122, 115–121. Two, PO’s construction only requires each data package to have “at least N data elements,” and each data package does not need to be the same size. *Supra*, §VI. Thus, Bertozzi also discloses element [10.pre.c] under PO’s construction for the same reasons explained above, as Bertozzi explains that its data packages have multiple data elements (e.g., Ex-1005, 22), and Figure 4 also shows a data package with at least N=2 data elements.⁴ Ex-1003, ¶¶122–126.

⁴ Bertozzi’s Figure 3 shows a different embodiment where packets have ten flits. Ex-1005, Fig. 3; Ex-1003, ¶¶126, 78. Under PO’s broader construction, claim 10 would also read on this different embodiment. Ex-1003, ¶126. Under PO’s construction, Figure 3 shows a data package with (at least) N=2 data elements, one of which comprises routing information for the network stations (Ex-1005, 5 (header contains “routing information”)). Ex-1003, ¶126.

5. **[10.pre.d] the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface;**

Bertozzi discloses this element. Ex-1003, ¶¶127–130. Bertozzi discloses that the plurality of network stations comprises a plurality of routers (*data routers*) and a plurality of “*network interfaces*”, each of the routers (*data routers*) being coupled to a core (*functional block*) via a “*network interface*”. Ex-1005, 2–5, Fig. 1:



Ex-1003, ¶128.

Bertozzi discloses a NoC containing a plurality of routers. Ex-1005, 2 (“The basic idea ... envisions on-chip router (or switch)-based networks...”), Fig. 1.

While Figure 1’s labels say “Switch” rather than data router, Bertozzi uses these terms interchangeably. *Id.*, 2 (describing “on-chip router (or switch)-based networks”), 5 (describing “routing logic at the network switches....”); Ex-1003,

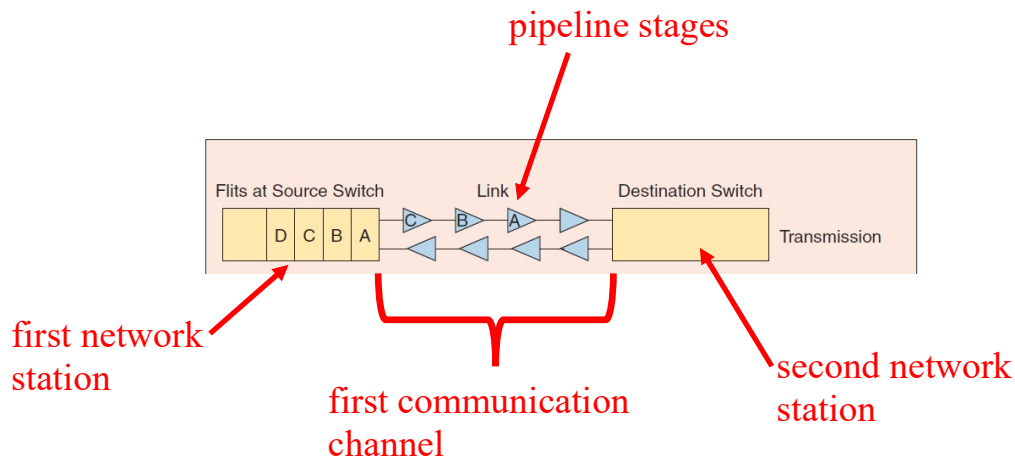
¶¶127–130. A POSA would also at once envisage using data routers where Bertozzi Fig. 1 illustrates switches. Ex-1003, ¶129.

The NoC also contains a plurality of network interfaces. Ex-1003, ¶130; *e.g.*, Ex-1005, 3 (“Xpipes has been designed as a library of highly parameterized soft macros (network interface[s]....”), 6 (“Xpipes network interfaces use OCP as point-to-point communication protocol with the cores....”). The data routers are coupled to the cores via the “network interfaces” allowing the cores to interact with the network. Ex-1005, 2; Ex-1003, ¶¶127, 130. The network interfaces convert between the bus protocol signals communicated by the cores (*e.g.*, VCI, OCP) and the packets communicated over the network of “on-chip router[s] (or switch[es]).” *Id.*, 2, 5–6, 10, 27, Fig. 7 (described as part of the same general “Architecture of Xpipes network”); Ex-1003, ¶¶75, 127, 130. The various network interfaces and networks stations are connected by links made of wires over which packets are transmitted. Ex-1005, 7, Fig. 1; Ex-1003, ¶¶127, 130.

6. **[10.e] the method comprising the acts of: identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and**

Bertozzi discloses this limitation. Ex-1003, ¶¶131–132. Bertozzi discloses identifying a link (*first communication channel*) between a source switch (*first network station*) and a destination switch (*second network station*) that *has a data transfer delay exceeding a predefined delay threshold*. Ex-1005, 7–8, 12, Fig. 4;

Ex-1003, ¶131–132. For example, Bertozzi describes identifying links with a “link delay” that exceeds “pre-defined timing requirements (e.g., the desired clock speed of the design).” Ex-1005, 7; *see also id.*, 6 (describing that “long wires increasingly determine the maximum clock rate, and hence performance, of the entire design.”); Ex-1003, ¶131. As discussed further below, Bertozzi describes using pipeline stages to break such long wires into “segments whose length can be tailored to the desired clock frequency....” *Id.*, 7; Ex-1003, ¶131. An example of such a link (after the insertion of pipeline stages) is shown in Bertozzi’s Figure 4, annotated below:



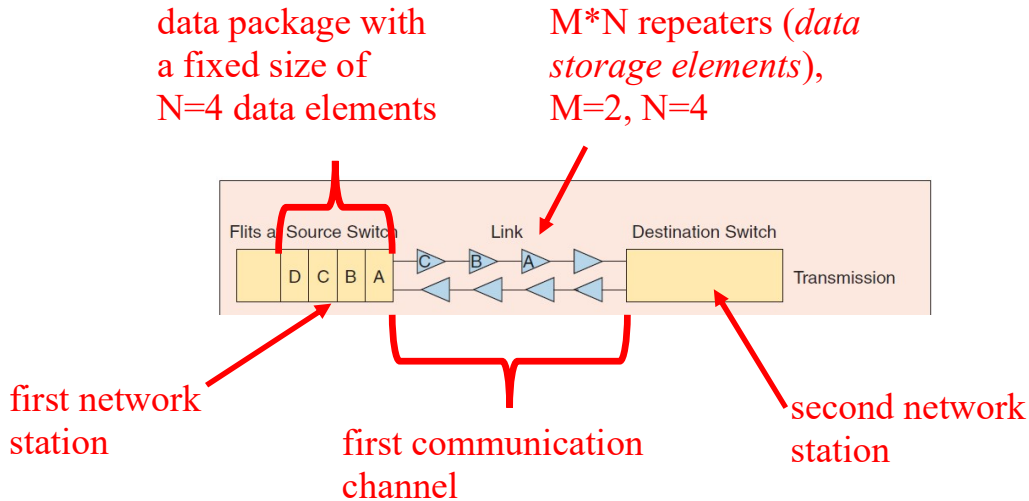
Id., 7, Fig. 4 (annotated); Ex-1003, ¶132.

7. **[10.f] in response to the identifying act, inserting $M \times N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel.**

This limitation is disclosed by Bertozzi under all of the proposed constructions. Ex-1003, ¶¶135–142; Ex-1005, 7-9, 12, Fig. 4. As discussed with

respect to element [10.e], Bertozzi describes identifying links with a delay that exceeds “pre-defined timing requirements.” *Supra*, §VII.B.6. Once such a link is identified, Bertozzi describes *inserting . . . data storage elements into the data communication network*. Ex-1003, ¶135. Specifically, Bertozzi discloses inserting “repeaters” into the link to break it up into smaller segments or “pipeline stages.” Ex-1005, 12, 7–8, Fig. 4; Ex-1003, ¶135. A POSA would have understood that each of Bertozzi’s repeaters is a “data storage element” under both Qualcomm’s and PO’s proposed constructions. Ex-1003, ¶135. Bertozzi explains that its repeaters (also called “relay stations”) function similarly to a latch in a pipelined data path, and that each stores a single flit (*data element*) at a time. Ex-1005, 7–8, Fig. 4; Ex-1003, ¶135. Thus, each repeater is “a structure that stores one data element” (Qualcomm’s construction) and are an “array of one or more elements that store data” (PO’s construction). Ex-1003, ¶135.

Furthermore, Bertozzi’s Figure 4 discloses inserting $M*N$ *data storage elements ... for introducing a delay of $M*N$ cycles on the first communication channel* as claimed. Ex-1003, ¶¶135–142. As explained with respect to element [10.pre.c], Bertozzi describes data packages with a fixed size of $N=4$ data elements. *Supra*, §VII.B.4. In Figure 4, Bertozzi discloses inserting 8 repeaters ($M*N$ *data storage elements*, where $M=2$, and $N=4$) into a link:



Ex-1005, Fig. 4 (annotated); Ex-1003, ¶¶137–139, 135. Because Bertozzi explains that each repeater causes a delay of one clock cycle, the repeaters in Figure 4 introduce a delay of 8 cycles ($M*N$ cycles, where $M=2$ and $N=4$). Ex-1005, 7–9; Ex-1003, ¶¶137–139.

Bertozzi’s Figure 4 shows 8 total repeaters, divided equally between the path from the Source Switch to the Destination Switch and the path from the Destination Switch to the Source Switch. Ex-1003, ¶139; Ex-1005, Fig. 4. This is functionally identical to the embodiment shown in Figure 1 of the ’2893 patent, where 6 data storage elements ($M*N$ data storage elements, where $M=2$, and $N=3$) are split between two subchannels. See Ex-1001, 5:63–6:2, Fig. 1; Ex-1003, ¶139.

Additionally, as discussed above with respect to element [10.pre.c], under PO’s construction the claim only requires each data package to have “at least N data elements.” *Supra*, §VI; Ex-1027, ¶164. Thus, under PO’s construction

Bertozzi discloses this limitation in multiple ways. Ex-1003, ¶¶140–142. One, because PO’s construction is broader, Bertozzi discloses this limitation for the same reasons as under Qualcomm’s construction. Ex-1003, ¶140. Two, Bertozzi also discloses this limitation under PO’s construction because it teaches packets that include at least two flits, such that each contains *at least* $N=2$ data elements. Ex-1003, ¶140, *supra*, VII.B.4. Bertozzi’s Figure 4, for example, shows a data package that has at least two data elements (*e.g.*, Flit A and Flit B), and it shows that 8 repeaters have been inserted. Ex-1005, Fig. 4; Ex-1003, ¶141. That is inserting $M*N$ data storage elements (8 storage elements, where $M=4$, and $N=2$) that introduce a delay $M*N$ cycles (8 cycles). Ex-1005, Fig. 4, 7–8; Ex-1003, ¶140–142.⁵

⁵ Under PO’s broader construction, [10.f] would also, like [10.pre.c] above, read on Bertozzi’s Figure 3 embodiment of a packet having ten flits. Ex-1005, Fig. 3; Ex-1003, ¶142. Under PO’s construction, Figure 3 shows a data package with (at least) $N=2$ data elements. Ex-1003, ¶142. Under PO’s construction, the packet would not need to be a particular fixed length, therefore a POSA would at once envisage designing the NoC with the pipeline structure shown in Figure 4 of Bertozzi, resulting in the claimed $M*N$ repeaters and delay cycles of element [10.f]. Ex-1003, ¶142.

C. Independent Claims 1 and 7

1. [1.pre]/[7.pre] An integrated circuit comprising:

To the extent the preamble is limiting, Bertozzi discloses an integrated circuit. Ex-1003, ¶95; *see also id.* ¶94. Bertozzi teaches the use of the Xpipes architecture and platform to design a NoC interconnect for a SoC. *E.g.*, Ex-1005, 3 (“Designing communication architectures for highly integrated deep sub-micron SoCs...”); *see also id.* 11–12. SoCs were known as a type of integrated circuit. Ex-1001, 1:8–13; Ex-1003, ¶95.

2. [1.a]–[1.f] and [7.a]–[7.f]

Bertozzi teaches elements [1.a]–[1.e] for the reasons explained above with respect to elements [10.pre.a]–[10.e], respectively. *Supra*, §§VII.B.2–6; Ex-1003, ¶¶96–134. At least as applied by PO, Bertozzi discloses element [1.f]—*the data communication introducing a delay of $M*N$ cycles on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold*—for the same reasons explained above with respect to elements [10.e] and [10.f].⁶ Ex-1003, ¶143; *see also id.* ¶¶131–132, 135–142.

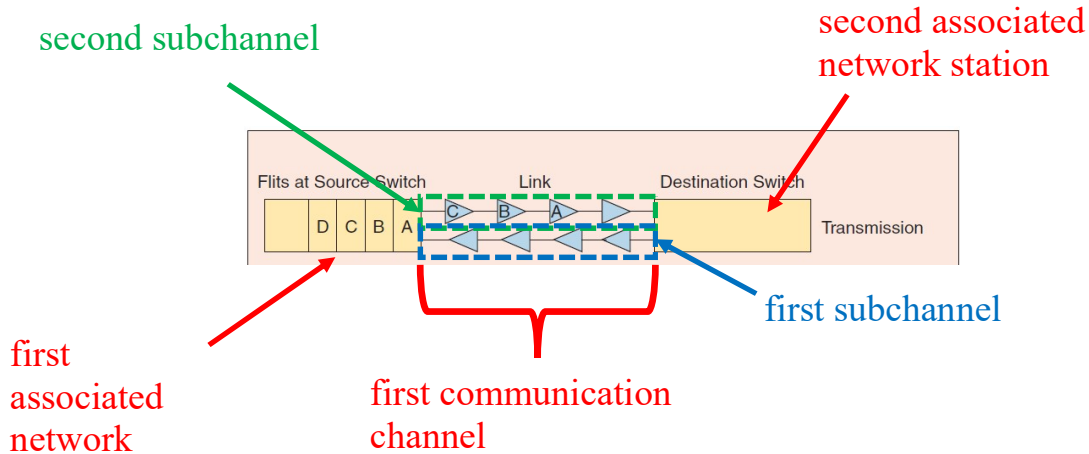
⁶ PO has interpreted this element to have the same scope as claim elements [10.e] and [10.f] in *Network System Technologies, LLC v. Samsung Electronics Co, Ltd.*, No. 2-22-cv-481 (E.D. Tex.). *Compare* Ex-1030, 28–34 *with* Ex-1031, 21–29.

Bertozzi teaches elements [7.a]–[7.f] for the reasons explained above with respect to element [10.pre.a]–[10.f], respectively. *Supra*, §§VII.B.2–7; Ex-1003, ¶¶96–142, 144–149.

3. **[7.g] wherein each communication channel of the plurality of communication channels comprises: a first subchannel between an input port of a first associated network station and an output port of a second associated network station; and a second subchannel between an input port of the second associated network station and an output port of the first associated network station, and**

Bertozzi discloses this limitation. Ex-1003, ¶¶150–154. Each link (*communication channel*) disclosed by Bertozzi is a bidirectional channel comprised of two subchannels, one for each direction of communication between the network stations. *Id.* This is shown, for example, in Bertozzi’s Figure 4, which depicts a *first subchannel* directed from the output of the destination switch (*second associated network station*) to the input of the source switch (*first associated network station*) and a *second subchannel* directed from the output of the source switch (*first associated network station*) to the input of the destination switch (*second associated network station*):

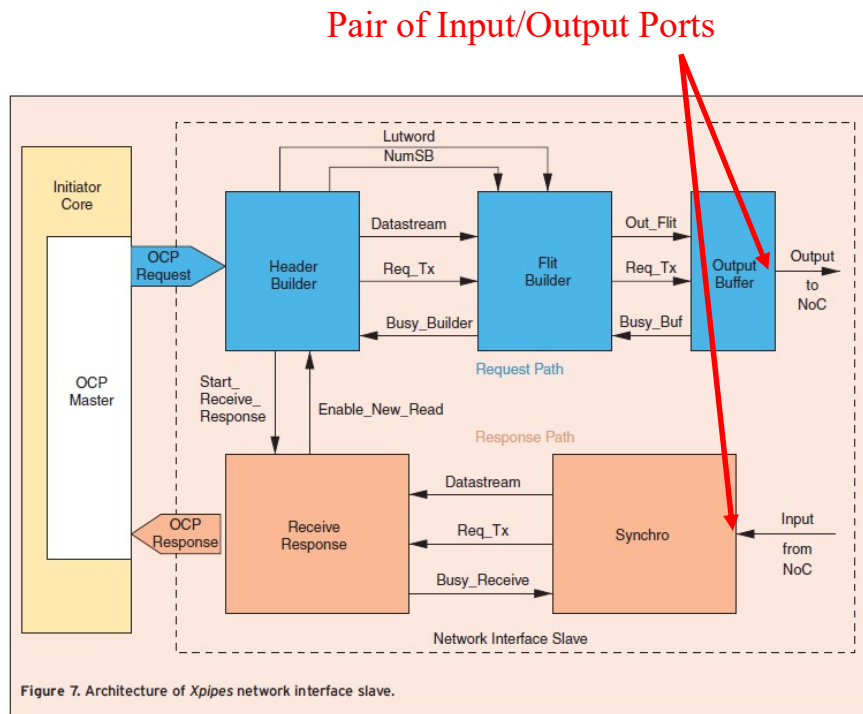
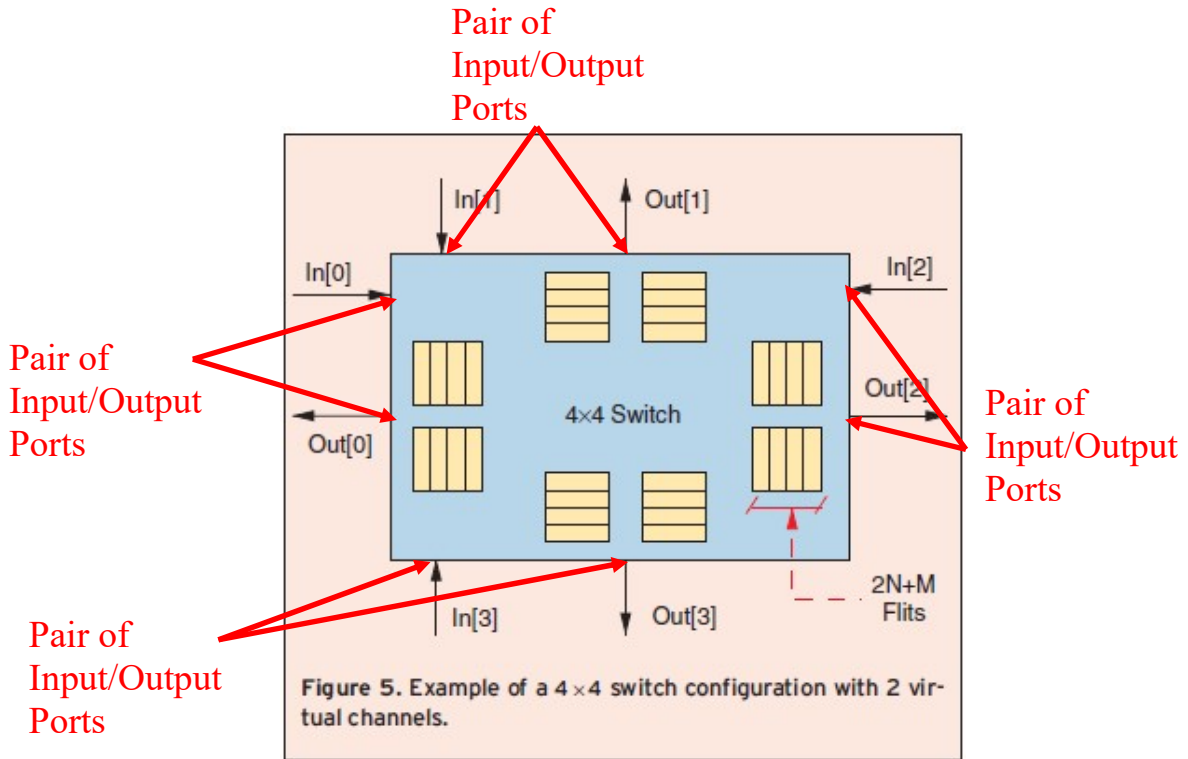
Petitioners disagree with PO’s interpretation. However, for the purposes of this ground, Petitioners apply PO’s interpretation.



Ex-1005, Fig. 4 (annotated); Ex-1003, ¶151.

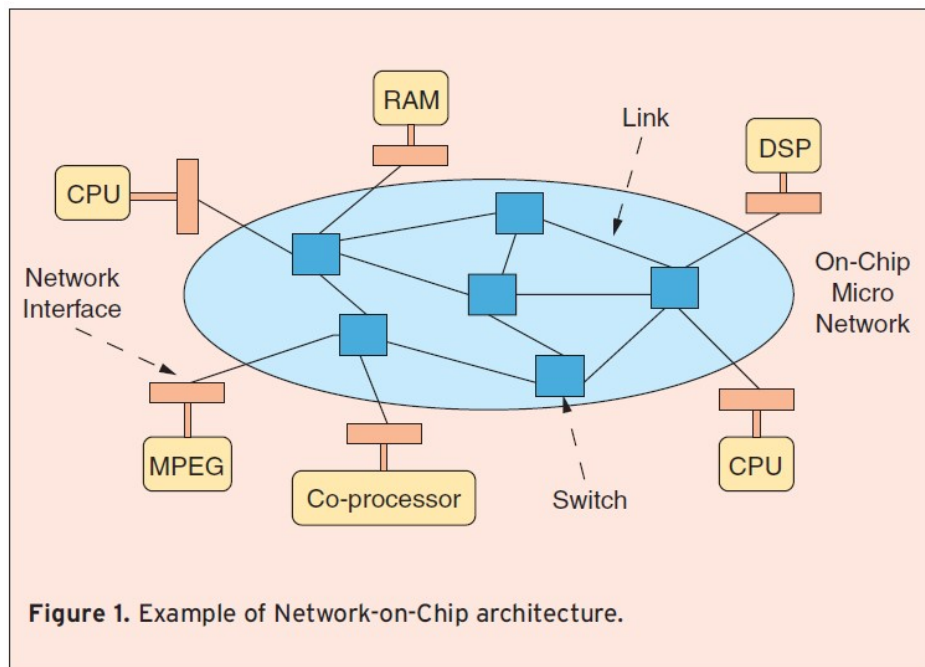
Additionally, Bertozzi describes that these subchannels connect to *input ports* and *output ports* in the network interfaces and switches (*network stations*).

Ex-1005, Figs. 5, 7; Ex-1003, ¶¶152, 150. For example, Bertozzi's Figure 5 (switch) and Figure 7 (network interface) show that the network stations each have at least one pair of input/output ports. Ex-1003, ¶¶152–154, 150. Figures 5 and 7 show aspects applied to all of the Xpipes solutions. Ex-1005, 8-9; Ex-1003, ¶75.



Ex-1005, Figs. 5, 7 (annotated). Ex-1003, ¶¶153–154.

A POSA would have understood that the subchannels described above exist in all the links of (and embodiments of) Bertozzi's network, and at least in a plurality of such links, as required by the claim. Ex-1003, ¶150. For example, a POSA would understand that each of the functional blocks shown in Figure 1 require the ability to both send and receive messages. Ex-1003, ¶150. Thus, their network interfaces include both input and output ports, along with associated subchannels. Ex-1003, ¶¶150, 152–154.



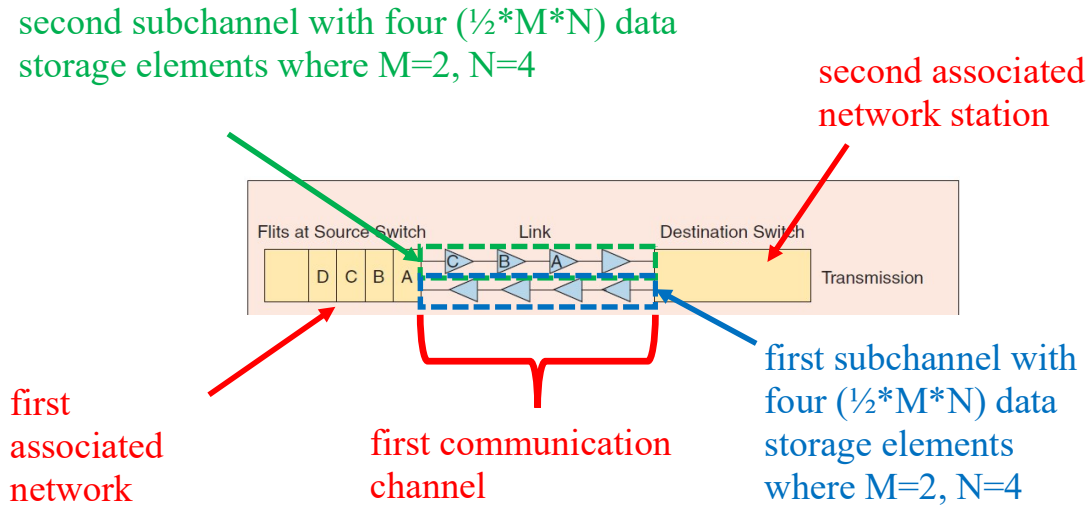
Ex-1005, Fig. 1.

In addition, Bertozzi also teaches that there are acknowledgements sent over links between network stations. Ex-1003, ¶150. Specifically, Bertozzi teaches the use of “distributed error detection with link level retransmission” for error recovery. Ex-1003, ¶150; Ex-1005, 6. Under this approach, for each flit (*data*

element) received by a second associated network station from a first associated network station over a link, the second associated network station must send an acknowledgement (e.g., ACK or NACK) to the first associated network station over the link. Ex-1005, 7-8, Fig. 4; Ex-1003, ¶150. As shown in Bertozzi, such communication uses two subchannels: a first link (*subchannel*) between the output port of the first associated network station to the input port of the second associated network station and a second link (*subchannel*) between the input port of the second associated network station to the output port of the first associated network station. Ex-1005, Fig. 4; Ex-1003, ¶¶150–154.

4. [7.h] wherein the first subchannel and the second subchannel of the first communication channel each comprise a delay introduced by $\frac{1}{2} * M * N$ data storage elements.

Bertozzi discloses this limitation. Ex-1003, ¶¶155–157. This element is satisfied under the Qualcomm's and PO's constructions where $M=2$ and $N=4$, both the first subchannel and the second subchannel of the first link (*communication channel*) comprise a delay introduced by four ($\frac{1}{2} * M * N$) repeaters (*data storage elements*). Ex-1005, Fig. 4. This is illustrated below:



Ex-1005, Fig. 4 (annotated); Ex-1003, ¶156.

Bertozzi also teaches this element under PO's constructions, where $M=4$ and $N=2$ and both the first subchannel and the second subchannel of the first link (*communication channel*) comprise a delay introduced by four ($\frac{1}{2} * M * N$) repeaters (*data storage elements*). Ex-1005, Fig. 4; Ex-1003, ¶157.

D. Dependent Claims 2, 3, 6

Each of dependent claims 2, 3, and 6 depends directly or indirectly from claim 1.

1. Dependent Claim 2

A POSA would understand that bidirectional links enable duplex communication between two associated network stations. Ex-1003, ¶158.

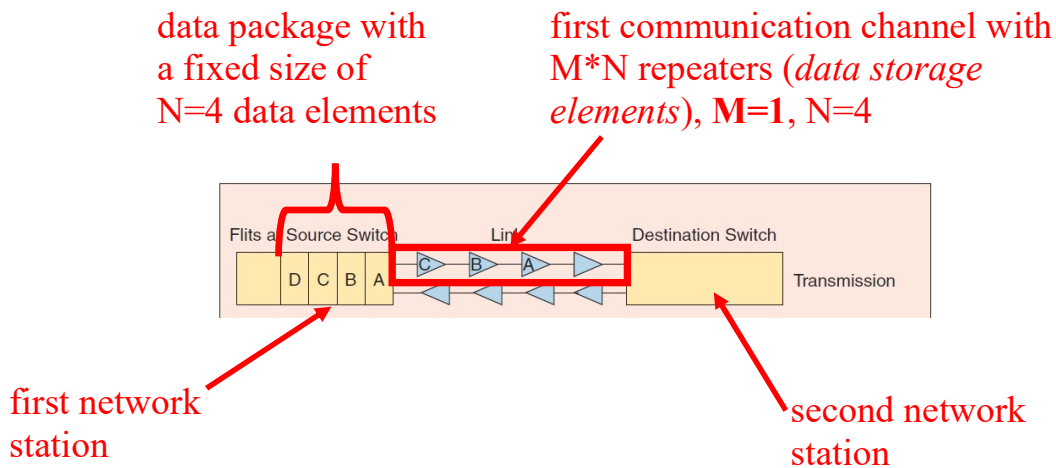
Therefore, Bertozzi discloses dependent claim 2 for the reasons explained above with respect to elements [7.g]. *Supra*, §VII.C.3; Ex-1003, ¶158.

2. Dependent Claim 3

Bertozzi discloses dependent claim 3 for the reasons explained above with respect to element [7.h]. *Supra*, §VII.C.4; Ex-1003, ¶159.

3. Dependent Claim 6

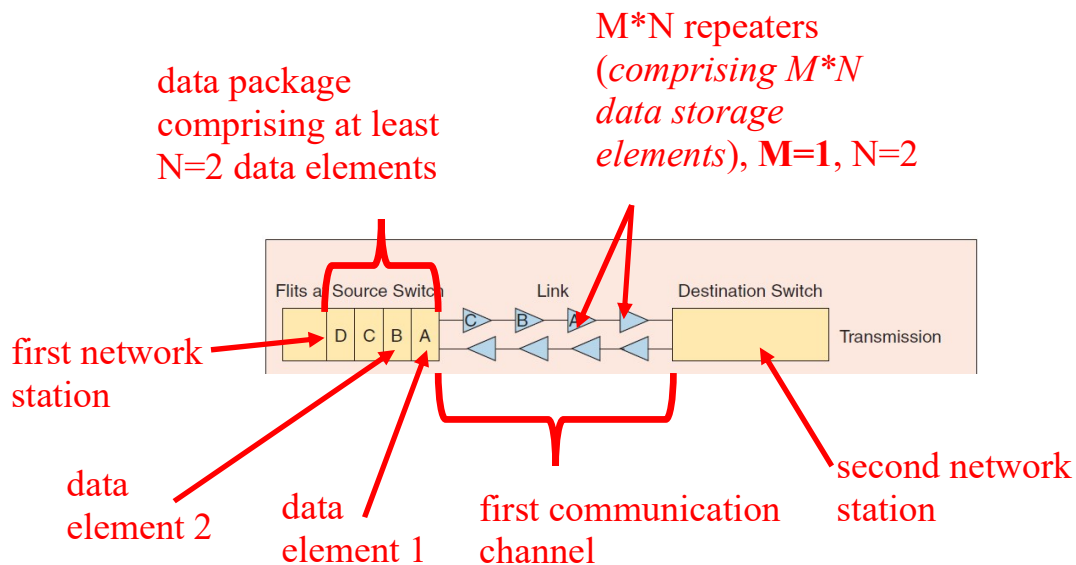
Bertozzi teaches this element, which requires that $M=1$. Ex-1003, ¶¶160-163. Under the Qualcomm's proposed construction and PO's broader proposed construction, claim 6 is met for the same reasons as discussed above regarding element [10.f] and [1.f], except that a POSA would understand that the "first communication channel" to be the link identified below in Bertozzi Fig. 4:



Ex-1005, Fig. 4 (annotated); Ex-1003, ¶161. A POSA would understand such a link to be a communication channel. Ex-1003, ¶¶161–162. The '2893 patent indicates that an example of a communication channel is "wires." Ex-1001, 1:24–35; Ex-1003, ¶162. The link identified above (*first communication channel*) is a segmented wire. Ex-1005, 7; Ex-1003, ¶162. The '2893 patent does not require a

“communication channel” to be bidirectional or duplex. Ex-1001, 5:1–5; Ex-1003, ¶162.

Additionally, as discussed above with respect to element [10.pre.c], under PO’s broader construction the claim only requires each data package to have “at least N data elements.” Ex-1027, ¶164; *supra*, §VI. Bertozzi discloses packets include at least two flits, such that each contains at least $N=2$ data elements. *Supra*, §VII.B.4; Ex-1003, ¶163. Thus, under PO’s construction, Bertozzi discloses the integrated circuit of claim 1, where $M=1$ as recited by dependent claim 6:



Ex-1005, Fig. 4 (annotated); Ex-1003, ¶163.

VIII. GROUND 2: BERTOZZI ALONE OR IN VIEW OF JANTSCH OR DUATO RENDERS CLAIM 1–3, 6–7, AND 10 OBVIOUS

As explained in Ground 1, Bertozzi discloses all of the elements of claims 1–3, 6–7, and 10. *Supra*, §VII. However, to the extent PO argues or the Board finds that Bertozzi does not expressly or inherently teach any element, the claims would have been obvious by Bertozzi alone or in view of Jantsch or Duato. Ex-1003, ¶¶164–189.

A. Jantsch (Ex-1006)

Jantsch is a textbook titled “Networks on Chip.” Ex-1006. It contains a collection of chapters by various authors. Chapter 5, entitled “*On Packet Switched Networks for On-Chip Communication*,” discusses the known approach of borrowing and adapting “the concepts of packet switched communication from computer networks to design on-chip networks.” Ex-1006, 47; Ex-1003, ¶84. Jantsch also teaches designing such NoC systems for a “fixed packet size.” Ex-1006, 56; Ex-1003, ¶¶84–85.

B. Duato (Ex-1009)

Duato is another textbook titled “Interconnection Networks: an Engineering Approach.” Ex-1009. Duato teaches various types of interconnection networks for use in many different applications, including “internal buses in very large-scale integration (VLSI) circuits.” *Id.*, 13; Ex-1003, ¶86. This includes various forms of message switching, including designing networks made up of routers. *E.g.*, Ex-

1009, 31–32. Duato also teaches designing such networks for “fixed-length packets.” *Id.*, 32; Ex-1003, ¶¶86–87.

C. Independent Claim 10

Bertozzi teaches elements [10.pre], [10.pre.a], [10.pre.b], [10.e], and [10.f] for the reasons explained above. *See supra*, §VII; Ex-1003, ¶164.

1. [10.pre.c]

To the extent PO argues that Bertozzi does not disclose that every packet in its NoC has the same fixed-length (*e.g.*, four flits in the embodiment of Fig. 4), as required by Qualcomm’s (but not PO’s) construction, a NoC with fixed length data packages would have been obvious in view Duato or Jantsch. Ex-1003, ¶¶165–176. Each of Jantsch and Duato teaches designing and using systems for fixed packet size. Ex-1006, 56 (teaching NoC systems for a “fixed packet size”); Ex-1009, 32 (teaching router networks for “fixed-length packets”); Ex-1003, ¶¶166–167, 84–87. A POSA would have found it obvious to design, and for the integrated circuit disclosed by Bertozzi to use, *data packages*, each having a fixed-length of four *data elements* like the *data package* shown in Figure 4 (identified A–D; Ex-1005, 6–8, Fig. 4; Ex-1003, ¶¶166–176.

In fact, Bertozzi itself discloses the use of a “fixed-length” packet. Ex-1005, 5 (“Messages that have to be transmitted across the network are usually partitioned into fixed-length packets.”); Ex-1003, ¶167. And with good reason, as it was

known and disclosed in Jantsch, there were two ways to communicate—fixed and variable-length packets—and a fixed-length packet provided efficiencies in comparison to variable-length packets. Ex-1003, ¶167; *see also* Ex-1006, 56 (“[A] fixed packet size with a payload of eight will be efficient compared to a variable packet size.”); Ex-1009, 32 (“[E]ach message may be partitioned into fixed-length *packets*.”). For example, it was known that fixed-length packets provided the benefit of keeping packets moving within a priority based NoC such as Bertozzi’s, which uses arbitrators within its switches. Ex-1005, 10, Fig. 6; Ex-1003, ¶168. In contrast, variable-length packets, which were known to include a few long packets, occupied a router or switch for an extended period of time. Ex-1009, 98–99; Ex-1003, ¶168. In addition, fixed length packets were known to improve deadlock recovery and would have been expected to make it easier to allocate buffer space in network stations. Ex-1003, ¶¶169–170; Ex-1009, 67, 35. Fixed length packets would also have predictably allowed simpler hardware implementation of various NoC components. Ex-1003, ¶171. In such cases, network stations did not need to deal with variations in packet length that can lead to more complex designs. Ex-1003, ¶171.

A POSA would have been motivated, with a reasonable expectation of success, to perform the method of designing an integrated circuit as claimed for communicating fixed-length packets in Bertozzi’s NoC. Ex-1003, ¶¶172–176.

One, Bertozzi explicitly teaches that “[m]essages ... are usually partitioned into fixed-length packets,” clearly indicating that it was routine and well within the ordinary skill of a POSA at the time to design a system for fixed-length packets. Ex-1005, 5; *see also* Ex-1003, ¶173; Ex-1006. **Two**, the technology taught by Jantsch and Duato is closely related to the technology in Bertozzi. Ex-1003, ¶174. For example, Bertozzi teaches a packet switched NoC interconnect for SoCs (Ex-1005, 1), and Chapter 5 of Jantsch, the referenced portion, is titled “On Packet Switched Networks for On-Chip Communication.” Ex-1006, 47; Ex-1003, ¶174. Duato is a textbook teaching interconnection networks, which includes “very large-scale integrated (VLSI) circuits.” Ex-1009, 13; Ex-1003, ¶174. SoCs are a type of VLSI circuit. Ex-1001, 1:8–11; Ex-1003, ¶174. **Three**, as discussed above, a POSA would have known that a network using fixed-length packets can be implemented using simpler hardware. Ex-1003, ¶¶175, 171. This is because network stations in a fixed-length packet network do not need to be designed to deal with variations in packet length, which can add complexity as network stations need to be able to operate without knowing when a packet is going to end. Ex-1003, ¶¶175, 171. Fixed-length packets were known to be predictable, such that network stations could be designed to expect data formatted in a certain way at a certain time. Ex-1003, ¶¶175, 171. This was known to simplify various processes, such as error checking. Ex-1003, ¶¶175, 171. Further, a POSA would understand that hardware

designed to operate using variable-length packets could easily transport fixed-length packets with little to no modification. Ex-1003, ¶176.

2. [10.pre.d]

As discussed in Ground 1, Bertozzi discloses network stations comprising “data routers.” *See supra*, §VII.B.5. To the extent PO mischaracterizes Bertozzi’s network and argues it discloses only switches and not routers, it would have been obvious to use data routers in Bertozzi’s network. Ex-1003, ¶¶177–178. Indeed, Bertozzi uses the terms routers and switches interchangeably: “the basic idea [of the disclosed NoC] ... envisions on-chip *router (or switch)-based networks* on which packetized communication takes place, as depicted in Fig. 1.” Ex-1005, 2 (emphasis added); Ex-1003, ¶177. Even if they are distinct (and they are not in the context of Bertozzi), a POSA would have been motivated to use data routers instead of switches given Bertozzi’s express disclosure and would have known it would be a simple substitution of one known element for another to obtain a predictable result. Ex-1003, ¶¶177-178; *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). Thus, a POSA would have a reasonable expectation of success. Ex-1003, ¶¶177–178.

D. Independent Claims 1 and 7

1. [1.pre]/[7.pre]

See supra, §§ VII.B.1, VII.C.1.

2. [1.a]/[7.a]

See supra, §§ VII.B.2, VII.C.2.

3. [1.b]/[7.b]

See supra, §§ VII.B.3, VII.C.2.

4. [1.c]/[7.c]

This element is taught by Bertozzi for the reasons explained in Ground 1 above with respect to element [10.pre.c]. *See supra*, §VII.B.4. This element is also obvious in view of Bertozzi alone, or further in view of Jantsch or Duato, for the reasons explained in this Ground 2 with respect to element [10.pre.c]. *See supra*, §VIII.C.1; Ex-1003, ¶¶165-176.

5. [1.d]/[7.d]

This element is taught by Bertozzi for the reasons explained in Ground 1 above with respect to element [10.pre.d]. *See supra*, VII.B.5. This element is also obvious in view of Bertozzi alone, or further in view of Jantch or Duato, for the reasons explained in this Ground 2 with respect to element [10.pre.d]. *See supra*, §VIII.C.2; Ex-1003, ¶¶177–178.

6. [1.e]/[7.e]

See supra, § VII.B.6, VII.C.2.

7. [7.f]

See supra, § VII.B.7, VII.C.2.

8. [1.f]

As discussed in Ground 1, Bertozzi discloses “the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold” as this element has been applied by PO. *See supra*, §VII.C.2. To the extent this element requires that the data communication network itself identify a delay during the operation of the claimed integrated circuit (rather than a delay being identified during the design stage), which is contrary to what PO argues in its litigation against Petitioner Samsung (*see* note 6, *supra*), the detection of such delays in operational networks would have been obvious to a POSA. Ex-1003, ¶¶179–184.

For example, it was well-known that certain networks require packets to arrive at network stations “at precisely scheduled time slots.” Ex-1003, ¶180 (citing Ex-1014, 11:23–27). This is just what is described in the ’2893 patent. *See* Ex-1001, 1:47–61 (describing *prior art* networks in which data packets are received “during a predefined clock cycle.”); Ex-1003, ¶180. It was also well-known that delays could arise in operational networks. Ex-1003, ¶181. As such, in networks with precisely scheduled time slots, it was known to detect delay in a transmission channel (*e.g.*, using “probe” signals) that would result in a packet being received in an inappropriate time slot (*a data transfer delay exceeding a predefined delay threshold*) and to use data storage elements like those described

by Bertozzi to adjust the delay to be an “integral multiple of the packet transmission time” (*a delay of $M*N$ cycles*) so that the packet arrives in an appropriate time slot. Ex-1003, ¶182 (citing, *e.g.*, Ex-1014, 11:47–67, 12:38–44 (describing a “temporal alignment buffer”), 15:52–16:25 (describing the use of probe signals to “to set the temporal alignment delay so that the probe words arrive synchronized to the respective routing cycles.”)).

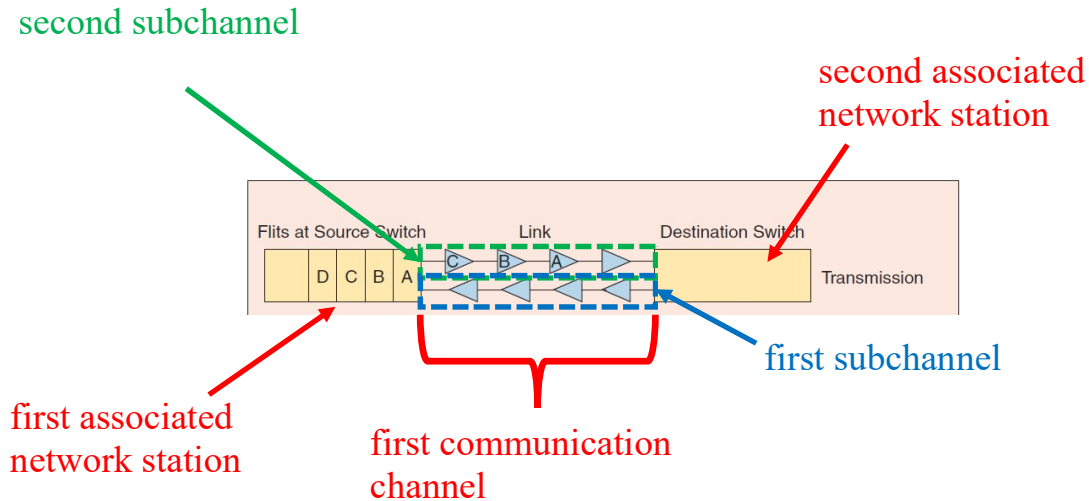
A POSA would have been motivated to implement this delay detection functionality in the SoC described by Bertozzi to provide an SoC with increased communication functionality. Ex-1003, ¶183. In particular, a POSA would have understood that doing so would enable the SoC to service communications with precise timing constraints like audio and video data. Ex-1003, ¶183 (citing Ex-1014, 8:7–9 (describing “time critical communications such as video or audio data traffic.”)). Indeed, Bertozzi describes that its SoC is used for “audio processing” and “video processing.” Ex-1005, 2; Ex-1003, ¶183. A POSA would also have had a reasonable expectation of success including such functionality into an SoC like the one described by Bertozzi, as doing so merely combines prior art elements according to known methods to yield predictable results. Ex-1003, ¶184. Indeed, a POSA would have understood that Bertozzi’s repeaters pipeline stages could be used to provide the requisite delay adjustment. Ex-1003, ¶184. Furthermore, and as discussed above, borrowing and adapting “the concept of packet switched

communication from computer networks to design on-chip networks” was well-known and common at the time of the alleged invention. Ex-1006, 47; *see also* Ex-1005, 2 (“The basic idea [of the NoC architecture] is borrowed from traditional large-scale multi-processors and the wide-area networks domain....”); Ex-1003, ¶184.

9. [7.g]

As discussed in Ground 1, Bertozzi discloses “subchannels.” *See supra*, §VII.C.3. To the extent PO argues that Bertozzi does not disclose a plurality of communication channels comprising subchannels as required by this element, this also would have been obvious in view of Bertozzi. Ex-1003, ¶¶185–189.

Bertozzi discloses a bidirectional link with a first subchannel between an input port of a first associated network station and an output port of a second associated network station and a second subchannel between an input port of the second associated network station and an output port of the first associated network station, and a POSA would have understood that this structure exists in at least a plurality of Bertozzi’s communication channels. Ex-1005, Figs. 4, 5, 7; *supra*, §VII.C.3.



Ex-1005, Fig. 4 (red annotations added); Ex-1003, ¶186.

Even if Bertozzi had not expressly disclosed subchannels, using subchannels as claimed would have been an obvious feature in view of Bertozzi's own teaching and the knowledge of a POSA. Ex-1003, ¶¶187–189. First, a POSA would understand that bidirectional links allow request and response messages to be sent along the same path, which can be more efficient for sending response messages. Ex-1003, ¶187. Second, a POSA would have known that bidirectional links can reduce congestion throughout the network and make it less likely that a deadlock will develop. Ex-1003, ¶187. Third, bidirectional links were known to allow for acknowledgements to be sent between network stations. Ex-1005, 7-8, Fig. 4; Ex-1003, ¶187. Additionally, a POSA would have found it obvious from Figures 5 and 7 to connect the paired input and output ports of one network station to the paired

input and output ports of a second network station via the same link. *Id.*, Figs. 5, 7; *supra*, VII.C.3; Ex-1003, ¶188.

A POSA would have had a reasonable expectation of success in implementing subchannels as claimed in Bertozzi’s NoC in view of the teachings of Bertozzi itself and the knowledge and routine skill of a POSA. Ex-1003, ¶189. Bidirectional links were a known option in the art. Ex-1003, ¶189; Ex-1005, 7–8; Fig. 4. Bertozzi itself teaches the use of a bidirectional link. Ex-1005, 7–9, Fig. 4; Ex-1003, ¶189. Additionally, the network stations are shown as having pairs of input/output ports for connection with bidirectional links. Ex-1003, ¶189. Therefore, a POSA would have had a reasonable expectation of success. *Id.*

10. [7.h]

See supra, § VII.C.4.

E. Dependent Claims 2, 3, 6

As explained above in Ground 1, Bertozzi discloses each of the elements of dependent claims 2, 3, and 6. *See supra*, §§ VII.D.1–3. Therefore, these claims are obvious over Bertozzi in view of Jantsch for at least the same reasons. Ex-1003, ¶¶164–189.

IX. GROUND 3: DIELISSIN IN VIEW OF HASSOUN RENDERS CLAIMS 1–3, 6, 7, 9, AND 10 OBVIOUS

Claims 1–3, 6, 7, 9, and 10 and are also obvious over Dielissen in view of Hassoun. Ex-1003, ¶¶190–248. Hassoun discloses the well-known solution of

pipelining (e.g., introducing three data storage elements/delay stations) to improve the performance of long wires in on-chip interconnects, which would have been an obvious way to improve Dielissen’s NoC. Ex-1003, ¶¶88–89, 54–56, 215.

A. The References

1. Dielissen (Ex-1007)

Dielissen describes the “Æthereal” NoC. The Æthereal NoC “consists of routers and network interfaces.” Ex-1007, 1. “The routers transport packets of data from one NI [(network interface)] to another.” *Id.* Figure 1 shows the routers and network interfaces:

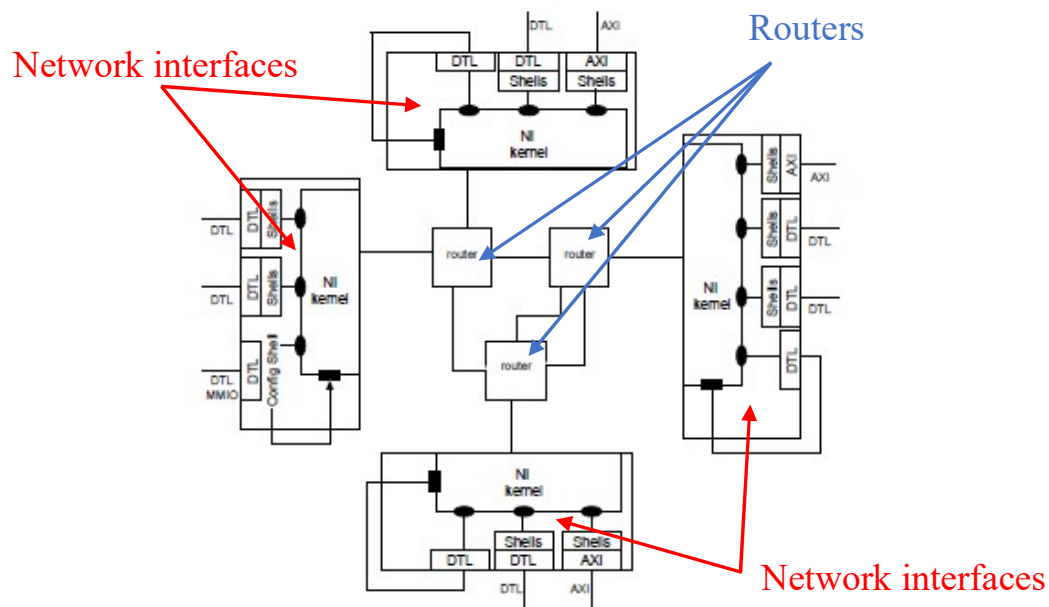


Figure 1. network example

Ex-1007, Fig. 1 (annotated); Ex-1003, ¶82.

Dielissen teaches packets that are made up of “one or more flits.” Ex-1007,

2. Each flit in turn is a fixed size that contains three “words.”⁷ *Id.*

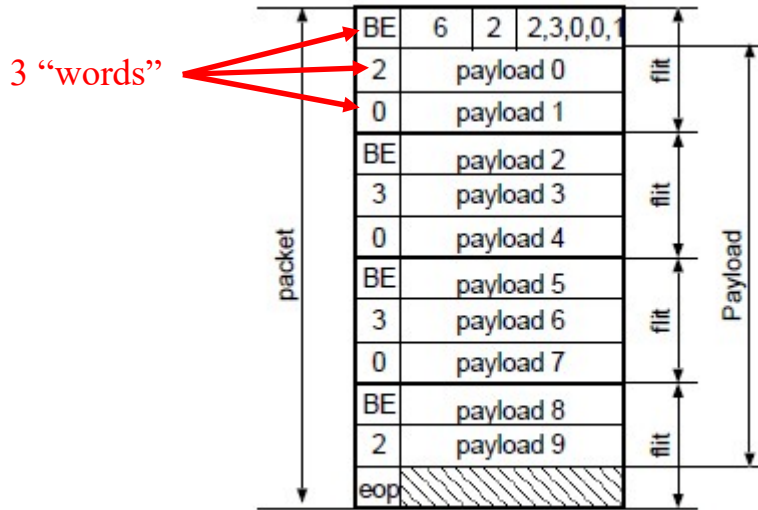


Figure 4. BE-packet example

Ex-1007, Fig. 4 (annotated); *see also* Ex-1003, ¶197.

2. Hassoun (Ex-1011)

Hassoun discloses the use of buffered routing paths on wires when “multiple clock cycles are required.” Ex-1011, 2. Such buffered routing paths contain a number of registers. *Id.*, 3. Each such register results in one clock cycle of delay on the path. *Id.* Figure 2 shows an example of such a path with three registers (and therefore three delay cycles):

⁷ A “word” is another term for “phit.” Ex-1003, ¶199.

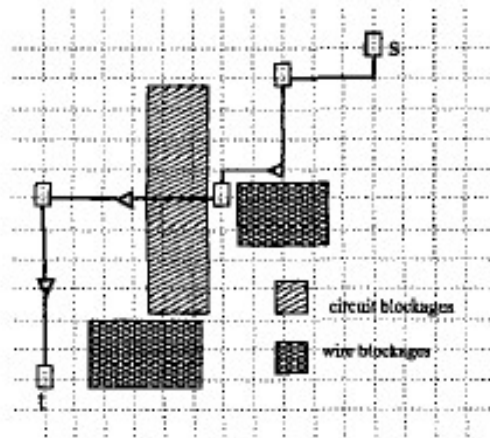


Figure 2. An example of routing within a single clock domain

Ex-1011, Fig. 2; Ex-1003, ¶¶88–89.

B. Independent Claim 10

1. [10.pre]

To the extent the preamble is limiting, it is disclosed by Dielissen. Ex-1003, ¶190. Dielissen teaches the use of the “Æthereal network on chip (NoC).” Ex-1007, 1. A POSA would understand that in designing an SoC, an Æthereal NoC could be used to “integrat[e] IPs with diverse communication requirements.” *Id.*; Ex-1003, ¶190. For instance, Dielissen teaches that some features “can be plugged in or left out at design time according to the requirements.” Ex-1007, 4.

2. [10.pre.a]

Dielissen discloses a plurality of IP modules sometimes referred to as masters and slaves (*functional blocks*). Ex-1007, 1, 3-5, Fig. 11; Ex-1003, ¶192.

For example, annotated Fig. 11 shows a plurality of masters and slaves.

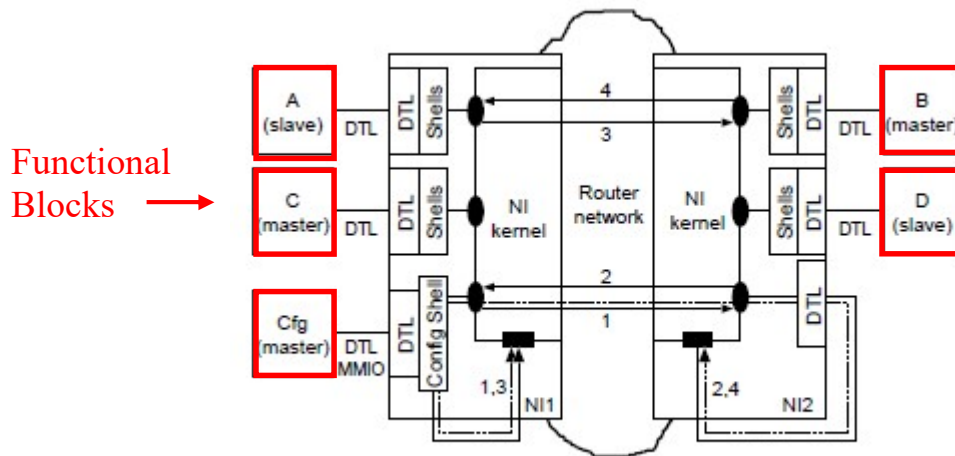


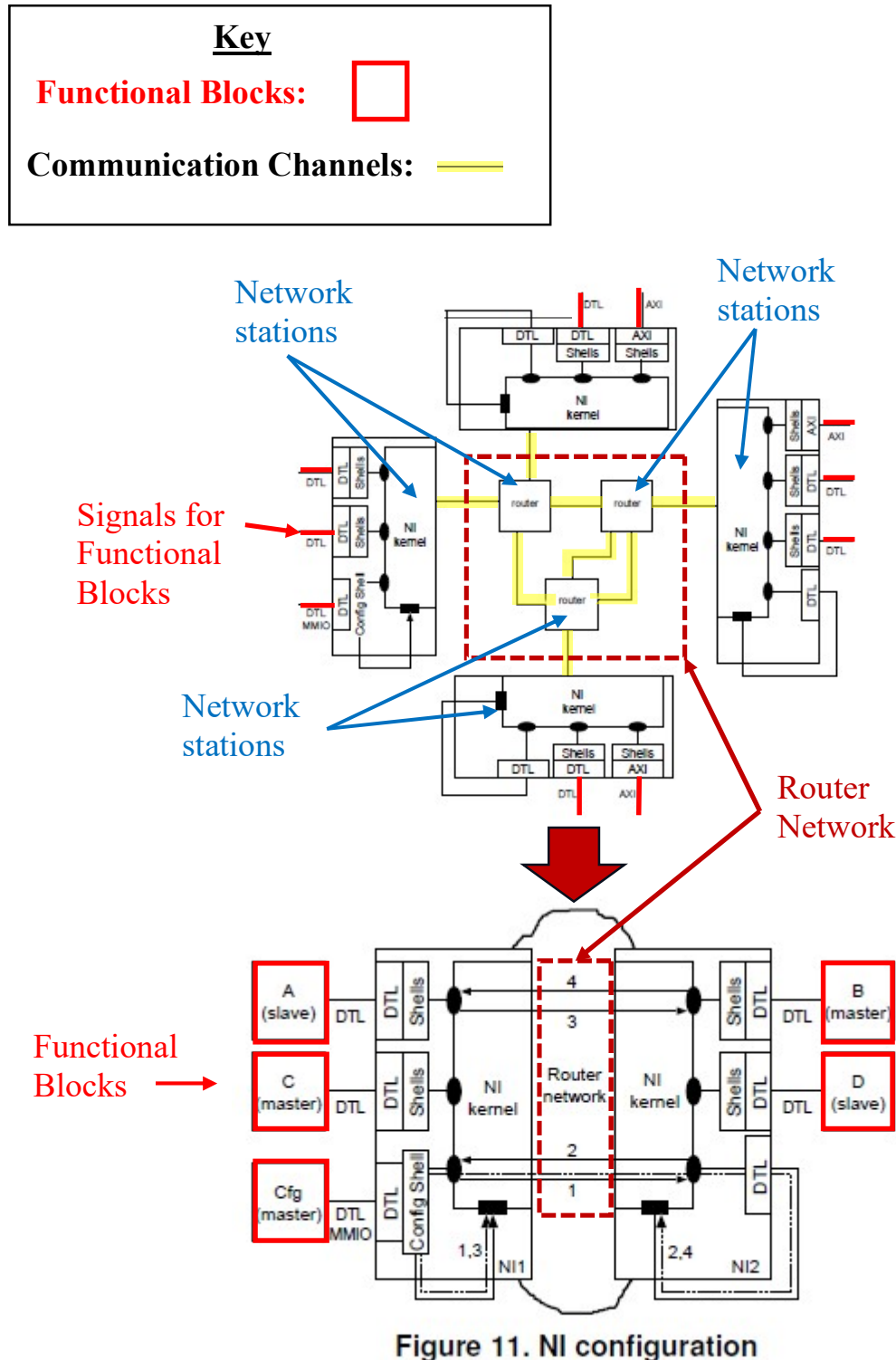
Figure 11. NI configuration

Ex-1007, Fig. 11 (annotated); Ex-1003, ¶193.

3. [10.pre.b]

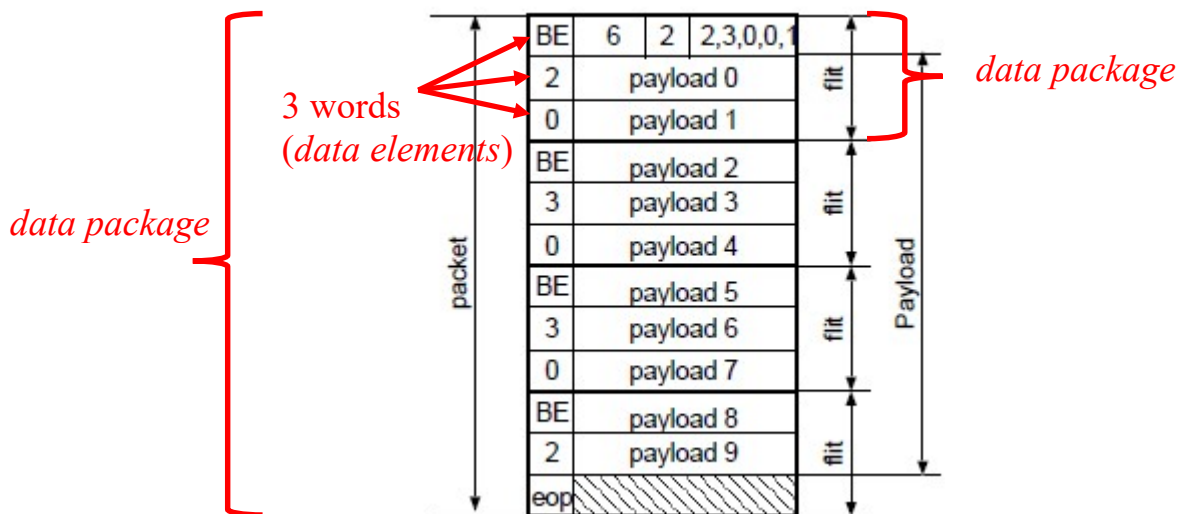
Dielissen discloses a NoC (*data communication network*) comprising a plurality of network interfaces and routers (*network stations*) being interconnected via a plurality of links (*communication channels*) for communicating *data packages* (Dielissen's flits or packets, as explained further in [10.pre.c]) between the IP modules (*functional blocks*). Ex-1003, ¶¶194-197; Ex-1007, 1-2, Figs. 1, 11. The NoC “consists of two components: the routers and the network interfaces (NI).” Ex-1007, 1; Ex-1003, ¶¶194–195. The routers and NIs are connected by

links. Ex-1007, 1; Ex-1003, ¶¶194–195. These elements are identified in annotated Figures 1 and 11 below:



Ex-1007, Figs. 1, 11; Ex-1003, ¶196.

The routers and NIs communicate *data packages* between the functional blocks. Ex-1003, ¶¶194, 197. Dielissen discloses the claimed *data packages* in at least two different ways: via its disclosure of data packets and via its disclosure of flits within the data packets. Ex-1003, ¶197. Dielissen teaches that “Routers send data from one network interface to the other by means of packets” and that each packet “consists of one or more flits.” Ex-1007, 2, Figs. 3, 4; Ex-1003, ¶197, 194. Each of Dielissen’s packets, and each flit within the packet, contains multiple data elements and corresponds to a data package as claimed:



Ex-1007, Fig. 4 (annotated); Ex-1003, ¶197. Dielissen discloses an implementation where each flit is set to a fixed size of 3 words (i.e., *data elements*). Ex-1007, 2; Figs. 3, 4.

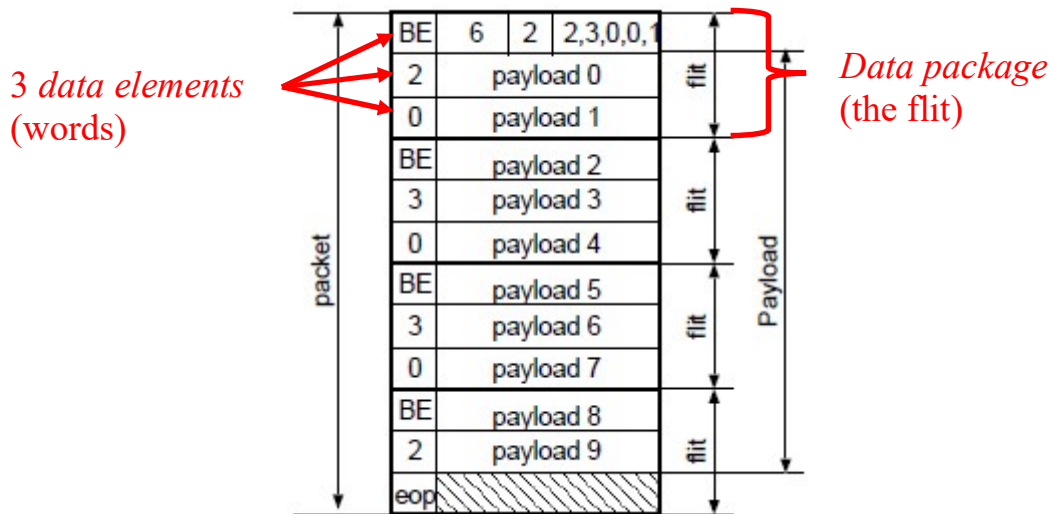
4. [10.pre.c]

Dielissen discloses this element under either Qualcomm's or PO's constructions. Ex-1003, ¶¶198–208; Ex-1007, 2, Figs. 3, 4; *see also, supra* §VI.

Qualcomm's Construction requires that “every data package communicated by the network stations has a fixed size of N data elements.” *Supra*, §VI; Ex-1025, 32. Dielissen teaches this. Ex-1003, ¶¶198–205.

As shown in Figure 4, Dielissen discloses that each flit has a fixed size of 3 words. Ex-1007, 2 (“[T]he flit size is chosen 3”); Ex-1003, ¶¶198, 202. A word, which a POSA would have understood corresponds to the claimed *data element*, is the unit of information that can be transferred across a physical channel in a single clock cycle. Ex-1003, ¶202. Thus, Dielissen teaches a *data package* (a flit)⁸ that comprises a fixed size of N=3 *data elements* (three “words”), as illustrated below:

⁸ Dielissen—like the specification of the '2893 patent—describes an implementation where each flit contains more than one data element (specifically, three in Dielissen). As explained above, a POSA would recognize that a flit in this implementation corresponds to a data package. As also explained above, in an implementation such as Bertozzi where each flit contains only one data element, a POSA would recognize that a flit corresponds to a data element. *Supra* VII.A.



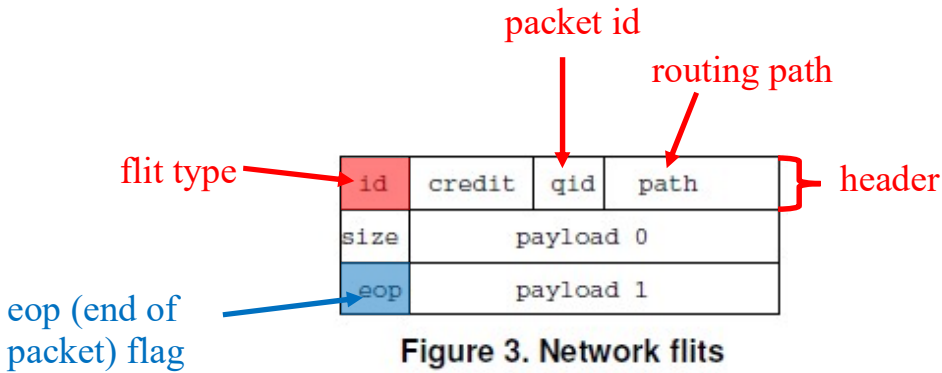
Ex-1007, Fig. 4 (annotated); Ex-1003, ¶¶202, 198–205.

Each flit includes a word (*data element*) comprising *routing information* for the routers and NIs. Ex-1003, ¶¶203–205. Dielissen discloses a data element comprising routing information for the network stations in the same way as the '2893 patent. The '2893 patent indicates that routing information includes “destination and required service type (e.g. best effort or guaranteed bandwidth)” Ex-1001, 2:22–24; Ex-1003, ¶203. The '2893 patent teaches that the first data package of a stream will contain a header data element. Ex-1001, 5:29–34. This header will contain “information about the destination of the data package as well as the service level of the data package, e.g. guaranteed bandwidth or best effort service.” *Id.* After a header is received, “[t]he service level will be flagged by setting a bit in the appropriate memory element of the destination output port. . . .” Ex-1001, 5:32–34; Ex-1003, ¶203. For subsequent data packages of the same

stream, the service level is identified and “the data router will know that these data packages belong to” the same data stream that is in progress. Ex-1001, 5:34-38; Ex-1003, ¶203. The data packages also have an indicator to tell the router if the current data package is the last of the data stream. *Id.*

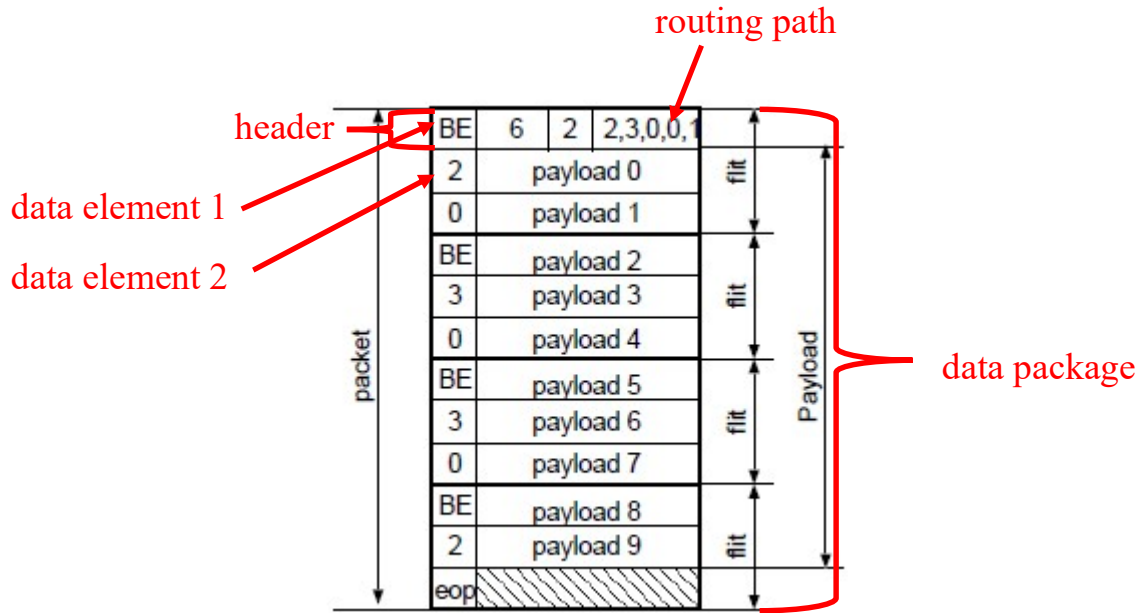
Similarly, Dielissen discloses that the first word of a packet is a packet header that contains the routing path, the packet id, and the flit type. Ex-1007, 2–3, Figs. 3, 4; Ex-1003, ¶204. Subsequent flits of the packet contain a flit type field that indicates whether the flit is a guaranteed throughput or best effort and an end of packet (“eop”) flag in the sideband information.⁹ Ex-1007, 2–3; Ex-1003, ¶204. The flit type field is like the service type identified in the ’2893 patent and the eop flag is like the last data package indicator. Ex-1003, ¶204; *compare* Ex-1007, 2–3 *with* Ex-1001, 5:29–40. Therefore, a POSA would have recognized that each of Dielissen’s data packages (in the form of flits) contain routing information in the form of the flit type field and the eop flag:

⁹ Petitioners do not agree that sideband signals are considered to be part of the data package or that such signals can be routing information. However, PO has identified analogous signals in its infringement contentions. Ex-1019, 14-19.



Ex-1007, Fig. 3 (color and annotations added), p.2–4; Ex-1003, ¶¶204–205; *see also* Ex-1007, Fig. 4.

Dielissen also discloses this element under PO's broader construction, where the number N can be *different* from one data package to the next, and a data package need only contain *at least* N=2 data elements (it can contain more). *Supra*, §VI; Ex-1003, ¶¶206–208. Dielissen discloses this element under PO's construction for the same reasons as discussed above under Petitioners' construction. Ex-1003, ¶¶198–207. And Dielissen discloses this element, under PO's construction, in a different way: that every data packet (*data package*) comprises a flit with at least N=2 words (*data elements*) including a header word (*data element*) that comprises routing information for the routers and NIs (*network stations*), 2 being an integer N of at least two. Ex-1003, ¶¶207–208. This is illustrated below:

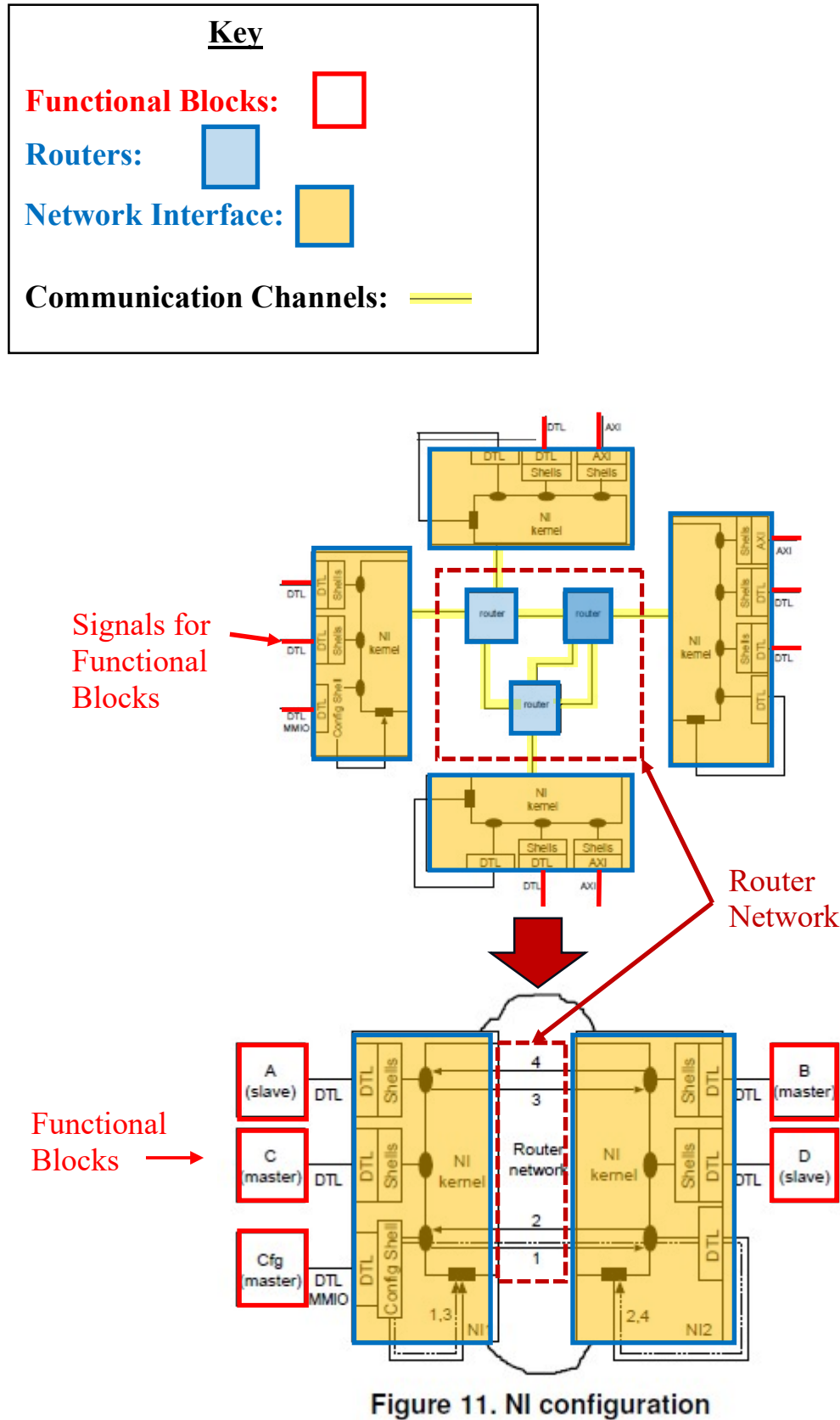


Ex-1007, Fig. 4 (red annotations added); Ex-1003, ¶208. Each data package (the packet) includes a header word comprising routing information for the routers and NIs. Ex-1003, ¶208. Dielissen discloses that the first word of a packet is a packet header that contains the routing path. Ex-1007, 2–3, Fig. 3, 4; Ex-1003, ¶208. A POSA would have understood that the routing path would be routing information. Ex-1003, ¶208.

5. [10.pre.d]

Dielissen's NoC comprises a plurality of network stations, including a plurality of routers (*data routers*) and a plurality of network interfaces. Ex-1003, ¶¶209–210; Ex-1007, 1–2, Figs. 1, 11. Each of the routers (*data routers*) is coupled to an IP module (*functional block*) via a network interface. Ex-1003, ¶¶209–210; Ex-1007, 1–3, Figs. 1, 11. Figures 1 and 11 show that the routers are coupled to the

IP modules via Nis. Ex-1003, ¶¶209–210. A POSA would have understood that the signals on the outside of the Nis in Figure 1 are to be connected to IP modules. Ex-1003, ¶¶209–210; Ex-1007, 1 (“The Nis are responsible for packetization / depacketization, for implementing the connections and services, and for offering a standard interface (e.g., AXI or OCP) to the *IP modules* connected to the NoC.”) (emphasis added). A POSA would also have understood (and also at once envisaged) that the “Router network” of Figure 11 would be made up of routers like those in Figure 1. Ex-1003, ¶210. These elements are identified in annotated Figures 1 and 11 below:



Ex-1007, Figs. 1, 11 (annotated), 1, 5; Ex-1003, ¶210.

6. [10.e] and [10.f]

Dielissen in view of Hassoun teaches these limitations. Ex-1003, ¶¶211–227.

A known problem in on-chip interconnects, including NoCs such as that shown by Dielissen, was delay caused by “long” or “global” wires¹⁰. Ex-1003, ¶¶211–214; Ex-1005, 3, 6 (“[L]ong wires increasingly determine the maximum clock rate, and hence performance, of the entire design.”); Ex-1010, 1, 2; Ex-1006, 36. Long wires were thus known to limit the performance of a chip by causing a data transfer delay exceeding a predefined threshold, such as exceeding the time allocated for a single clock cycle. Ex-1003, ¶¶211–214; Ex-1005, 3, 6; Ex-1010, 1, 2.

A POSA would have recognized this as a problem (and at least as a potential problem) with the Æthereal network that is described in Dielissen. Ex-1003, ¶¶213–215. For example, other papers by the same authors discussing the Æthereal NoC, mention global wires. Ex-1012, 1, 6; Ex-1006, 36 (“[S]everal *deep-submicron problems* must be solved: the increasing disparity between transistor and wire speeds....”); Ex-1003, ¶214.

¹⁰ “Global” wires was a term in the art that referred to long wires that communicate signals across the chip. Ex-1003, ¶212.

Hassoun teaches a known solution to this problem was to “pipeline” long links with a set of three repeaters, as shown below:

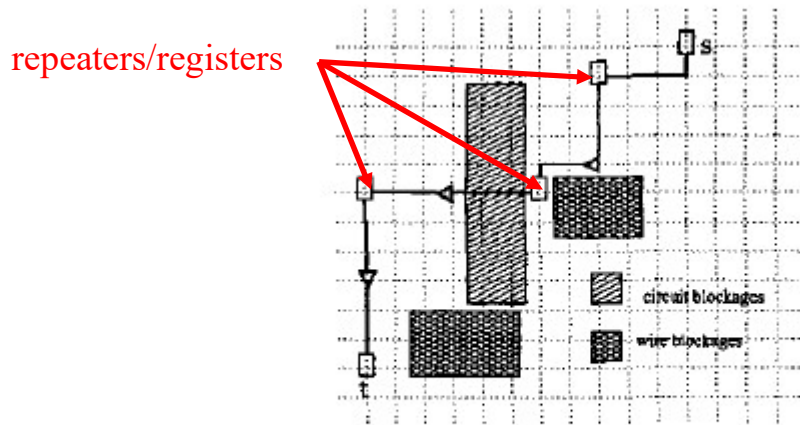


Figure 2. An example of routing within a single clock domain

Ex-1011, Fig. 2 (annotated); Ex-1003, ¶217; *see also* Ex-1007, Fig. 4; Ex-1010, Fig. 2; Ex-1003, ¶¶215, 54–56, 131–142. Hassoun teaches to insert these repeaters when “multiple clock cycles are required.” Ex-1011, 2–3; *see also* Ex-1005, 3, 7–8; Ex-1010, 1–3; Ex-1012, 6; Ex-1003, ¶¶215, 212, 88–89. This means identifying a communication channel between network stations that has a data transfer delay exceeding a predefined delay threshold, and then inserting repeaters at intervals along the wire. Ex-1003, ¶216. Repeaters allow wires to be partitioned into segments that are short enough to satisfy a faster clock rate. Ex-1003, ¶216; Ex-1011, 3; *see also* Ex-1005, 7 (“tailored to the desired clock frequency”); Ex-1010, 2.

The repeaters taught by Hassoun are *data storage elements*. Ex-1011, 3; *see also* Ex-1003, ¶¶219, 217, 211 (also citing Ex-1005, 7–8; Ex-1010, 1). Each repeater causes a delay of one clock cycle on the channel. Ex-1011, 3; Ex-1003, ¶219, 211, 89 (*also citing* Ex-1005, 7-9; Ex-1010, 2, 3). Thus, Hassoun teaches to insert three repeaters into the communication channel, where the data transfer delay has exceeded a predefined delay threshold (e.g. when “multiple clock cycles are required”). Ex-1011, 2–3; Ex-1003, ¶220, 217, 211. This results in introducing a delay of 3 cycles on the communication channel. Ex-1003, ¶¶220, 89.

A POSA would have been motivated, with a reasonable expectation of success, to modify Dielissen in view of the teachings of Hassoun and the knowledge of a POSA, first identifying a data transfer delay exceeding a predefined threshold (given the known long wire problem) and then predictably improving the chip by adding the repeaters as taught by Hassoun to allow or maintain a higher clock rate within the chip. Ex-1003, ¶¶221–225. In fact, another prior art paper by the authors of Dielissen regarding the *Æthereal* NoC expressly suggests adding repeaters to the *Æthereal* NoC to solve the long wire problem. Ex-1012, 6 (“[L]ong wires can be pipelined”); Ex-1003, ¶222. Further, it would have been apparent to a POSA that a large SoC such as that described by Dielissen would realistically need to have links with multiple repeaters. Ex-1003, ¶¶221, 217, 215; Ex-1011, 1; Ex-1010, 1.

A POSA also would have been motivated to modify Dielissen in view of Hassoun for a separate reason: to implement the specific number of data storage elements in a communication channel that corresponds to an integer multiple of the number of data elements, because some networks with fixed-length packets required “synchronization of packet transmissions.” Ex-1014, 2:48–52, 6:53–67, 12:21–27; Ex-1003, ¶222. Dielissen teaches that *Æthereal* was such as network. Ex-1007, 1 (“This requires a logical notion of synchronicity, where all routers and NIs are in the same slot.”); Ex-1003, ¶¶222–223; *see also* Ex-1012, 3-4; Ex-1001, 1:54–57. In such systems, it was known to adjust the “transmission delay between adjacent nodes to be equal to an integral number of packet transmission times” allowing each node to know “when to expect the header” of the packet. Ex-1014, 6:57–67; Ex-1003, ¶223. A POSA would understand that the transmission time for a flit as disclosed by Dielissen would be the number of words in the flit, i.e., $N=3$ cycles. Ex-1007, 2; Ex-1003, ¶223. Adding an integer multiple of 3 cycles of delay would thus require an integer multiple of 3 repeaters placed into the communication channel (i.e. 3 repeaters, 6 repeaters, or 9 repeaters, etc.). Ex-1003, ¶224. Adding such a delay would allow the router to know “when to expect [a] header.” Ex-1014, 6:57–67; Ex-1003, ¶224. Thus, for this reason also claim elements [10.e] and [10.f] would have been obvious under Qualcomm’s construction (requiring a data package of a fixed length of $N=3$ data elements) and

PO's construction (requiring only a data package *having at least* $N=2$ data elements). Ex-1003, ¶¶211–224.

As explained above with respect to element [10.pre.c], Dielissen teaches an integrated circuit using data packages with $N=3$ data elements. *Supra*, §IX.B.4. And as claimed and described M is any positive integer. Ex-1003, ¶225; Ex-1001, 3:50-51. Thus the obvious combination of Dielissen's integrated circuit designed for data packages with three data elements ($N=3$) with Hassoun's teaching of identifying a data transfer delay exceeding a predetermined delay threshold and then inserting three data storage elements in a communication link (as explained above), with an M of one, results in the elements of [10.e] and [10.f]: *introducing $M*N$ data storage elements* ($1*3=3$ data storage elements) into the data communications network, for *introducing a delay of $M*N$ cycles* ($1*3=3$ delay cycles) on the communication channel.¹¹ Ex-1003, ¶225. An example is illustrated below:

¹¹ Dielissen also teaches subchannels for communicating data in both directions between the network stations. *Infra*, §IX.C.5. It would also be obvious to implement Hassoun's repeaters in both subchannels such that $M=2$, $N=3$. Ex-1003, ¶225, n.17.

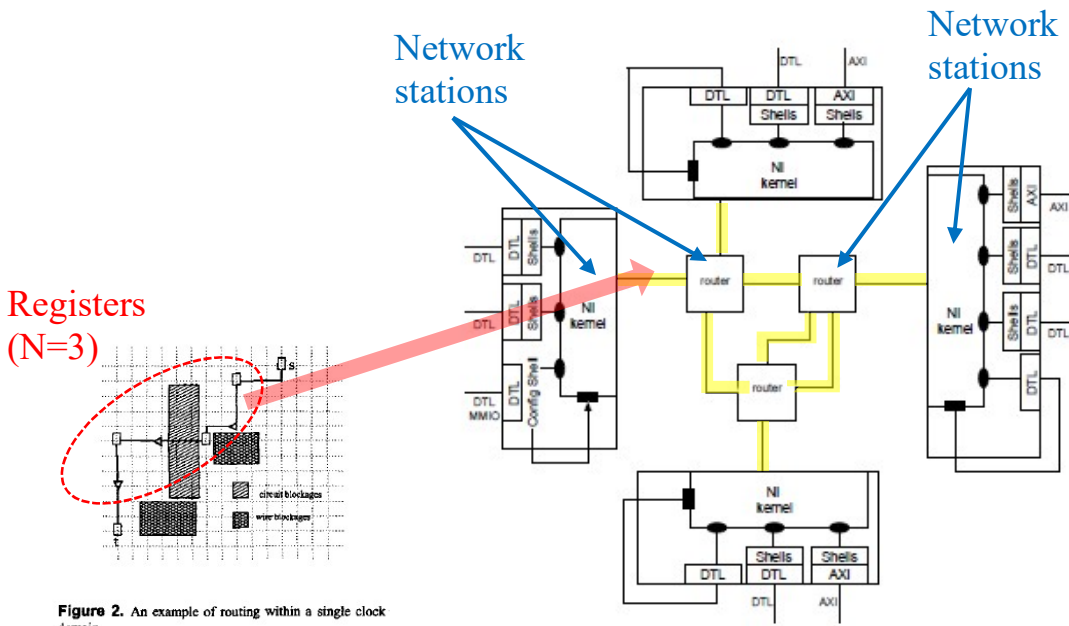


Figure 2. An example of routing within a single clock domain

Ex-1003, ¶225 (equally obvious to insert the repeaters on any other channel); Ex-1005, Fig. 1 (annotated); Ex-1011 Fig. 3. A POSA would have expected this known option to predictably improve Dielissen. Ex-1003, ¶225.

A POSA would have had a reasonable expectation of success in inserting repeaters as taught by Hassoun because doing so was no more than using a known solution for a known issue. Ex-1003, ¶¶226; 54–56, 131–142. Further, Hassoun is in the same field of on-chip technology as Dielissen. Ex-1003, ¶226; Ex-1011, 1. Further, pipelining (using repeaters) to improve the long wire / global wire delay problem was already known specifically in NoC applications. Ex-1003, ¶226 (citing Ex-1005, 1, 3, 7-8; Ex-1010, 1–3); *see also* Ex-1003, ¶¶56; 131–142. Another prior art paper by the authors of Dielissen—also regarding the Æthereal NoC—teaches that pipelining was an option on long links. Ex-1012, 6 (“Long

wires can be pipelined”); Ex-1003, ¶226. Therefore, adding M*N repeaters as claimed to the long wires in the *Æthereal* NoC to improve the long wire delay problem would have been merely the application of a known solution using only routine skill to predictably improve Dielissen. Ex-1003, ¶226.

Particularly under PO’s broader construction, inserting the data storage elements as recited by elements [10.e] and [10.f] also would have been obvious to try. Ex-1003, ¶227. As discussed above, the long wire problem in NoCs was a known issue with a known solution: inserting repeaters (data storage elements). *E.g.*, Ex-1011, 1, 3; Ex-1010, 1-3, Fig. 2; Ex-1005, 5, 7–8; Ex-1003, ¶¶211-215. In view of these references and the knowledge in the art, there were only a finite number of known, predictable solutions: insert a small number of repeaters, depending on wire length. Ex-1003, ¶227. Each of these options would have been obvious. *Id.*; *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007). And under PO’s construction, three of the first four of those options (inserting two, three or four repeaters into Dielissen) would not only satisfy element [10.e]; they would also meet the M*N requirements of element [10.f]. Ex-1003, ¶227. Thus, claim 10 would have been obvious for this additional reason. *Id.*

C. Independent Claims 1 and 7

1. [1.pre]/[7.pre]

To the extent the preamble is limiting, it is disclosed by Dielissen. Ex-1003, ¶191, 190. Dielissen discloses an integrated circuit. Dielissen teaches the use of the “Æthereal network on chip (NoC)” for “integrating IPs with diverse communication requirements” into an SoC communication infrastructure. Ex-1007, 1; Ex-1003, ¶191. SoCs are a type of integrated circuit. Ex-1001, 1:8–13; Ex-1003, ¶191.

2. [1.a]–[1.e]/[7.a]–[7.e]

Dielissen discloses elements [1.a]–[1.e] and [7.a]–[7.e] for the reasons explained above with respect to elements [10.pre.a]–[10.e], respectively. *Supra*, §§IX.B.1–6; Ex-1003, ¶¶192–210, 228.

3. [1.f]

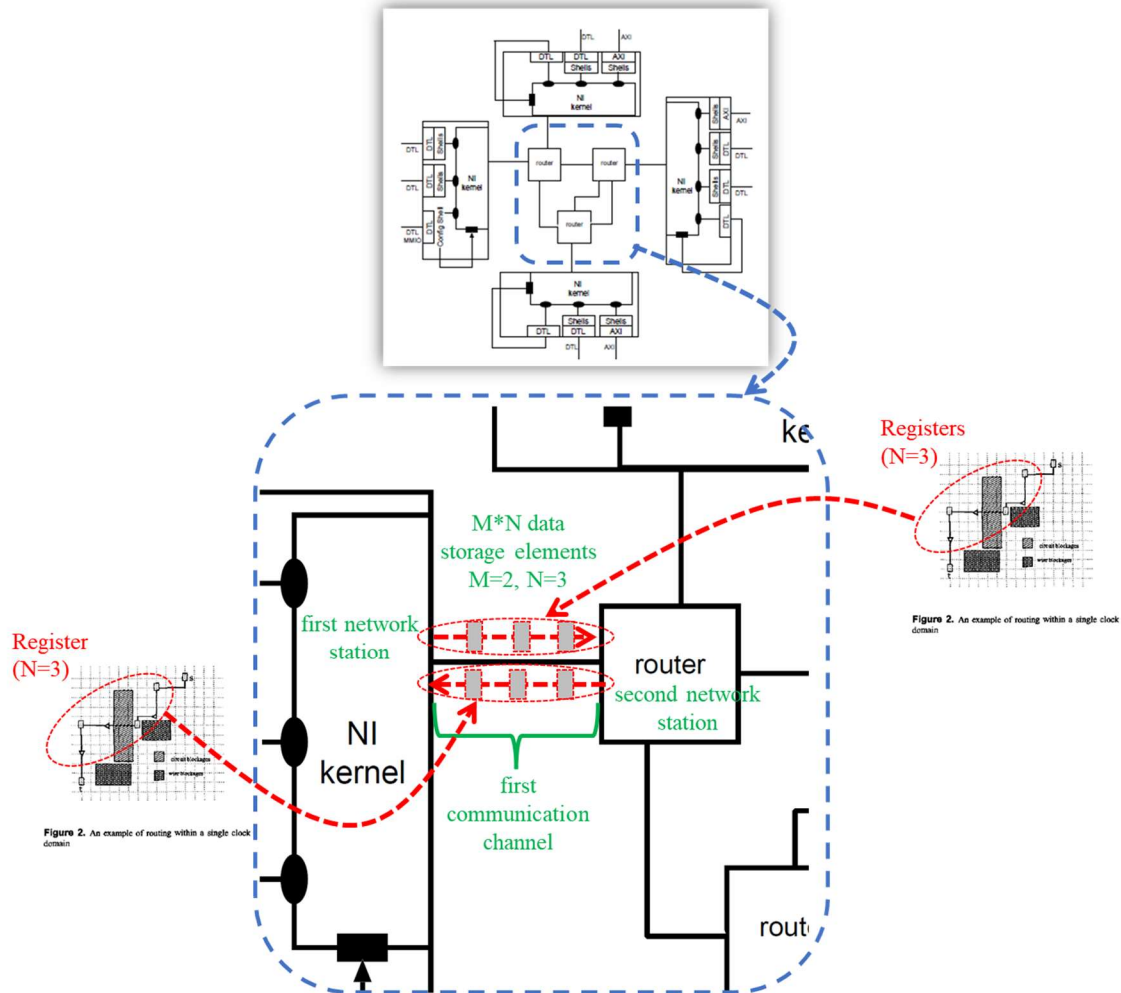
Dielissen in view of Hassoun renders this limitation obvious, at least as applied by PO, for the same reasons explained above with respect to elements [10.e] and [10.f].¹² *Supra*, §IX.B.6; Ex-1003, ¶234.

4. [7.f]

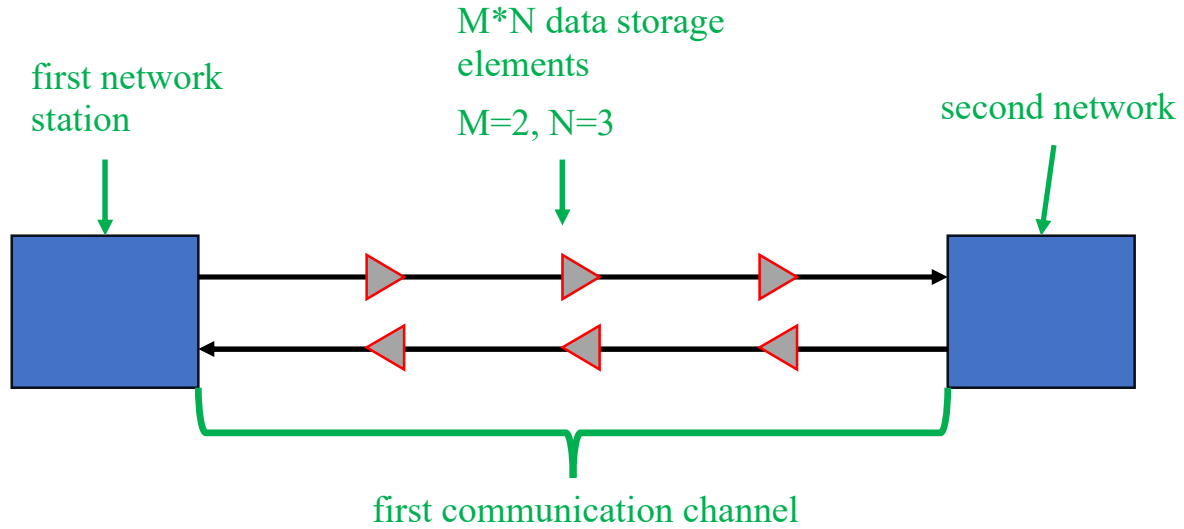
Dielissen in view of Hassoun renders this limitation obvious for the reasons explained above with respect to elements [10.e] and [10.f]. *See supra*, §IX.B.6; Ex-

¹² *See* note 6, *supra*.

1003, ¶¶230–233. For example, the combination would result in a NoC (“data communications network”) further comprising 6 repeaters (“data storage elements” where $M=2$, $N=3$) for introducing a delay of 6 cycle ($M*N$ cycles) on the first communication channel:

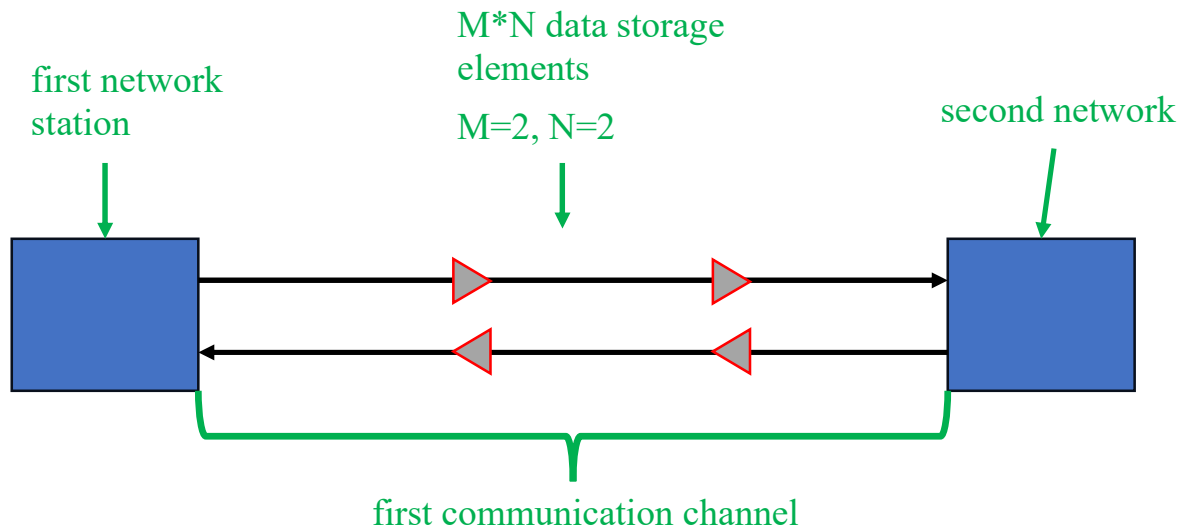


Ex-1007, Fig. 1; Ex-1011, Fig. 2 (annotated); Ex-1003, ¶232. Simplified below:



Supra, §IX.B.6; Ex-1003, ¶232.

Alternatively, under PO's construction, the combination would result in the NoC ("data communications network") further comprising 4 repeaters ("data storage elements" where $M=2$, $N=2$) for introducing a delay of 4 cycles ($M*N$ cycles) on the first communication channel:



Supra, §IX.B.6; Ex-1003, ¶233.

5. [7.g]

Dielissen discloses this limitation. Ex-1003, ¶¶235-238. Each link (*communication channel*) disclosed by Dielissen is bidirectional—it would have subchannels for communicating data in each direction between the network stations. Ex-1003, ¶¶235–236; Ex-1007, 3, Fig. 6. First, Figure 6 shows a network interface with data ports (for communicating with various functional blocks) and a router port. Ex-1007, 3, Fig. 6; Ex-1003, ¶236. The router ports show both input and output ports, indicating to a POSA that both the network interface and routers have bidirectional communication with both input and output ports. Ex-1003, ¶236; Ex-1007, Fig. 6:

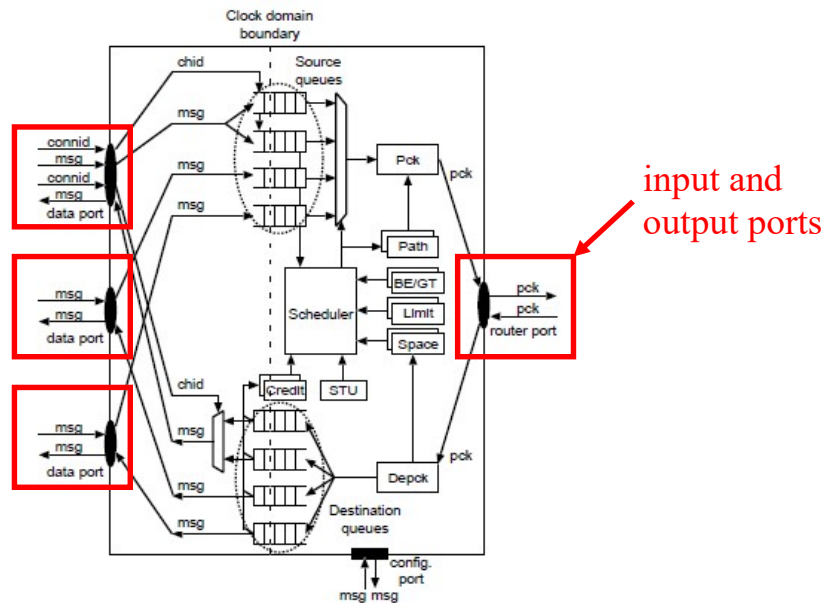


Figure 6. Network interface kernel

Ex-1007, Fig. 6 (annotated); Ex-1003, ¶236.

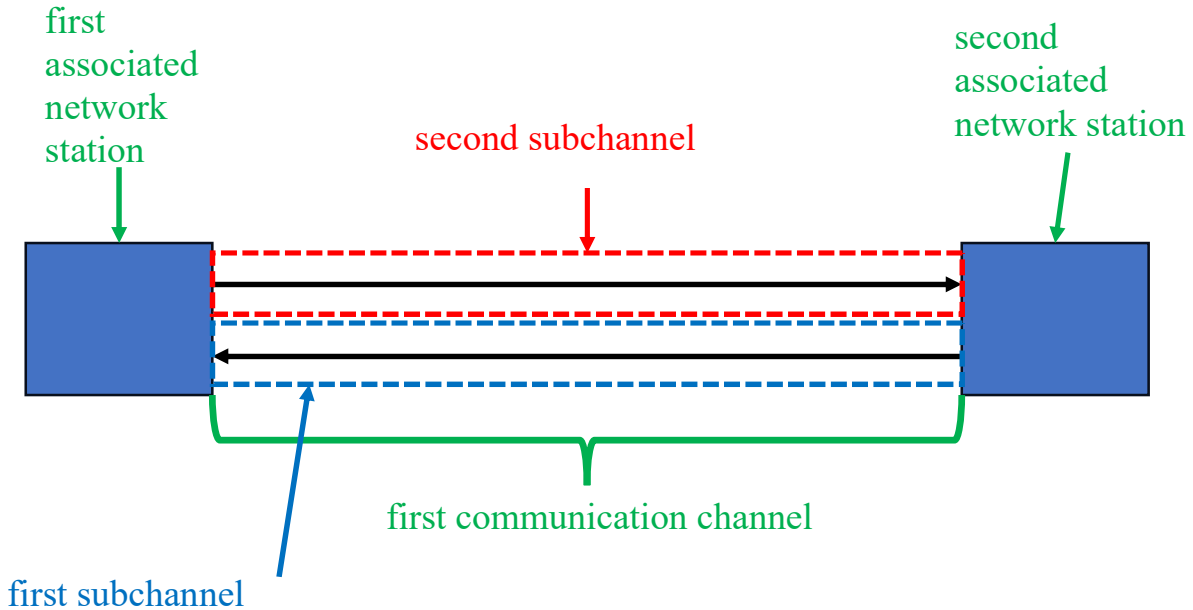
Second, Dielissen discloses that end-to-end connections have both a request and a response channel. Ex-1007, 5; Ex-1003, ¶236. A POSA would understand the individual sublinks used within the end-to-end connections would also have a request and response link. Ex-1003, ¶236.

Third, Figure 12 of Dielissen shows the “path” only transmitted from NI1 side to NI2 side. Ex-1007, Fig. 12; Ex-1003, ¶236. A POSA would understand that the messages from NI2 to NI1 necessarily traverse the same path back indicating that every link is bidirectional. Ex-1003, ¶236.

Fourth, Dielissen’s NoC uses link-level flow control. Ex-1007, 1, 3. Link-level flow control requires connected network stations to communicate regarding free space within their buffer, thus requiring bidirectional communication at the link level. *Id.*, 3; Ex-1003, ¶236.

Such communication would require two subchannels: a first subchannel between the input port of the first associated network station to the output port of the second associated network station and a second subchannel between the input port of the second associated network station to the output port of the first associated network station. Ex-1003, ¶237. A POSA would understand that a sublink taught by Dielissen is connected between the output port of one network station and the input port of another network station as the routers and network

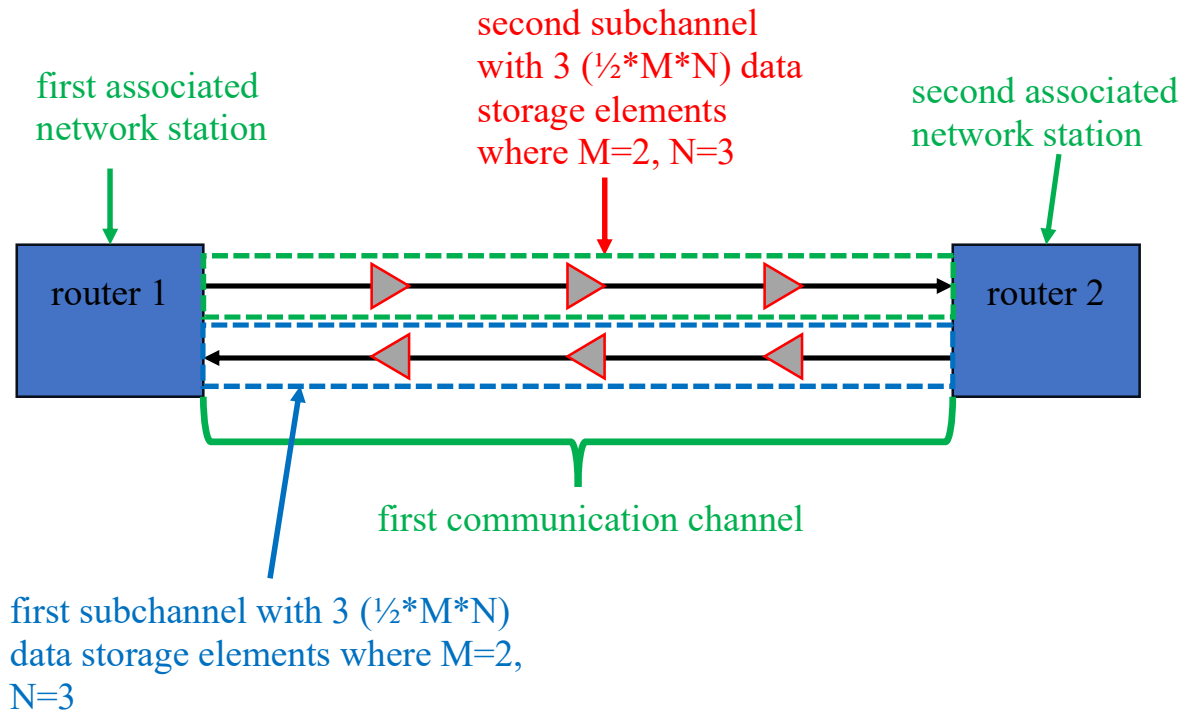
interfaces taught by Dielissen have input and output ports. Ex-1007, 2–3, Figs. 2, 6, 7; Ex-1003, ¶237.



Ex-1003, ¶238.

6. [7.h]

Dielissen in view of Hassoun renders this element obvious. *Supra*, §IX.B.6; Ex-1003, ¶¶239–241. Under this combination, both the first subchannel and the second subchannel of the first link (*communication channel*) comprise a delay introduced by 3 (that is, $\frac{1}{2} * M * N$, where $M=2$ and $N=3$.) repeaters (*data storage elements*). Ex-1003, ¶240:



Ex-1003, ¶240. This element is also obvious under PO's broader construction, including where M=2 and N=2. *Id.* ¶241.

D. Dependent Claims 2, 3, 6, and 9

Each of dependent claims 2, 3, 6, and 9 depend directly or indirectly from independent claim 1.

1. Dependent Claim 2

A POSA would understand that bidirectional links enable duplex communication between two associated network stations. Ex-1003, ¶242. Dielissen in view of Hassoun renders obvious dependent claim 2 for the reasons explained above with respect to elements [7.g]. *Supra*, §IX.C.5.

2. Dependent Claim 3

Dielissen in view of Hassoun renders obvious dependent claim 3 for the reasons explained above with respect to element [7.h]. *Supra*, §IX.C.6. Ex-1003, ¶243.

3. Dependent Claim 6

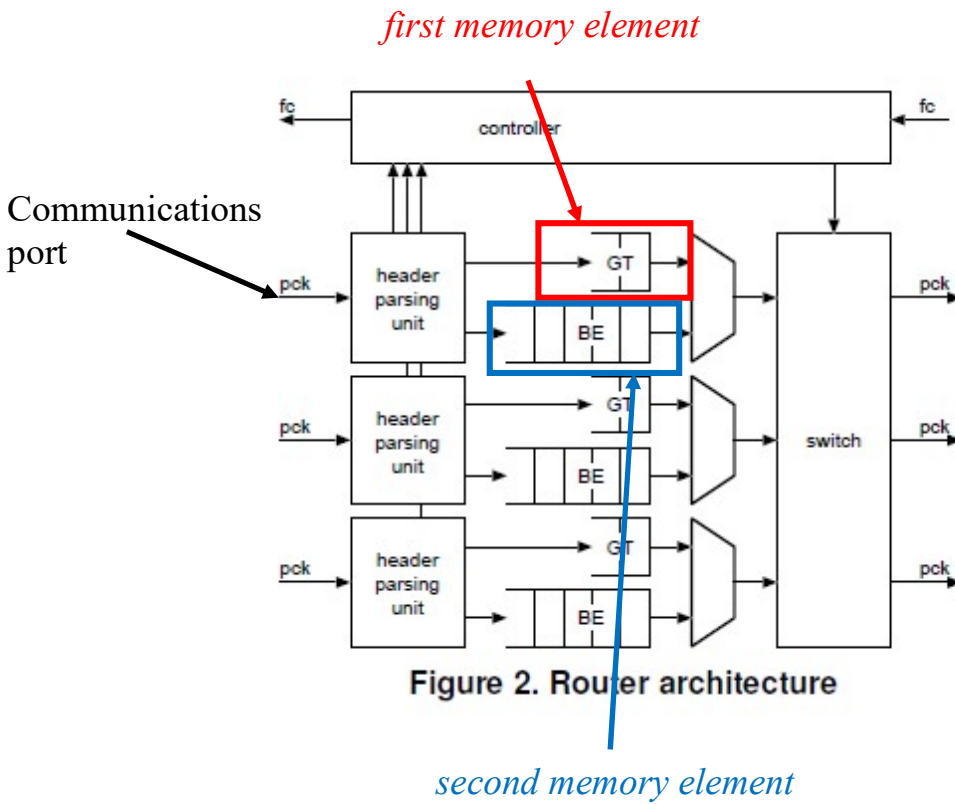
Dielissen in view of Hassoun renders obvious dependent claim 6 for the reasons explained above with respect to elements [10.e] and [10.f]. *Supra*, §IX.B.6; Ex-1003, ¶244.

4. Dependent Claim 9

This is disclosed by Dielissen. Ex-1003, ¶¶245–248. Dielissen discloses that each network station (*routers and network interfaces*) comprises a first queue (*memory element*) and a second queue (*memory element*) associated with a communication port of said network station, the first queue (*memory element*) being arranged to store routing information from a data package requiring a guaranteed throughput service (*first service level*) associated with said communication port and the second queue (*memory element*) being arranged to store routing information from a data package requiring a best effort service (*second service level*) associated with said communication port. *Id.*

Figure 2 is an example of a router architecture with first and second memories, which Dielissen refers to as queues, at least one for guaranteed throughput (GT) and a second for best effort (BE). Ex-1007, Fig. 2; Ex-1003, ¶246.

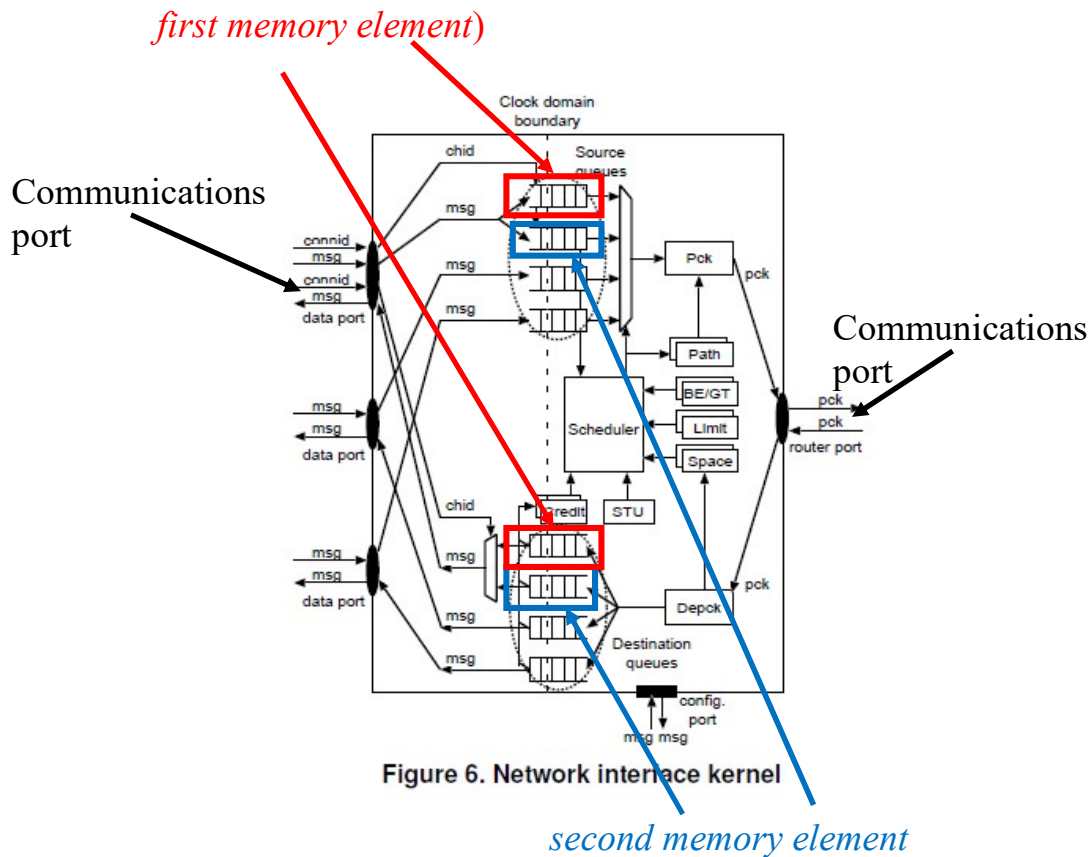
Such queues store the data packages, including the data elements that contain the routing information. Ex-1003, ¶246. An exemplary set of memories is illustrated below:



Ex-1007, Fig. 2 (annotated); Ex-1003, ¶246.

Similarly, Dielissen explains that the network interfaces have separate connections for “guaranteed throughput” and “best effort” traffic, and that each of these connections has a separate source queue. Ex-1007, 3; Ex-1003, ¶247. A POSA would therefore understand that Figure 6 shows a port where a “msg” (*data package*) is supplied to and stored in one source queue (*first memory element*) if it

is a msg requiring guaranteed throughput (*first service level*) and a different source queue (*second memory element*) if it is a best effort msg (*second service level*). Ex-1003, ¶247.



Ex-1007, Fig. 6 (annotated); Ex-1003, ¶247.

Dielissen describes that these queues are implemented with FIFOs, which a POSA would have understood are a kind of memory. Ex-1003, ¶248; Ex-1007, 6 (“All queues are 32-bit wide and 8-word deep, and are implemented using custom-made fifos.”); Ex-1003, ¶248; *see also* Ex-1007, 5 (describing “hardware fifos” of the queues as an alternative to “RAMs,” or “random access memories”).

X. GROUND 4: GROUNDS 1-3 FURTHER IN VIEW OF SULLAM RENDERS CLAIM 8 OBVIOUS

A. Sullam

Sullam discloses on-chip clocking circuitry. Ex-1013, 6:15–16 (“The microcontroller 100 of FIG. 1 also includes clocking circuitry 112....”), 6:18-21, 1:51–56; Fig. 1; Ex-1003, ¶¶90, 250. The clocking architecture includes an on-chip oscillator. Ex-1013, 7:35–37; Ex-1003, ¶¶90, 250. A POSA would understand the clocking circuitry taught by Sullam to be a clock signal generator. Ex-1003, ¶¶90, 250.

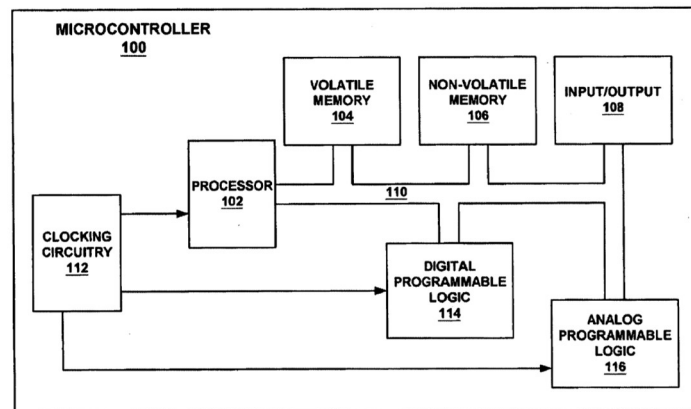


FIGURE 1

Ex-1013, Fig. 1.

B. Dependent Claim 8

Claim 8 depends from Claim 1 and is obvious in view of Bertozzi and Sullam. Ex-1003, ¶¶249–255. Bertozzi discloses a singular clock signal that all the switches/routers and network interfaces (including the pipeline stages) (*plurality of network stations*) and repeaters (*M*N data storage elements*) are responsive to. Ex-1003, ¶¶250–251. For example, Bertozzi references a single “desired clock speed of the design.” Ex-1005, 7; *see also id.*, 8; Ex-1003, ¶¶250–251. It further teaches that the network interfaces, links, and switches have a singular “clock speed target.” Ex-1005, 12.

Dielissen discloses that the routers/switch and network interfaces (“plurality of network station”) and the repeaters (“M*N data storage elements”) of Hassoun would be responsive to various clock signal. Ex-1003, ¶¶250, 252. Dielissen discloses that its network interfaces “implement...clock domain crossing.” Ex-1007, 3. Dielissen teaches that “Queues provide the clock domain crossing between the network and the IP modules.” *Id.*, *see also id.*, 6. To a POSA, this indicates that the network is in a clock domain such that Dielissen’s network interfaces and routers and the repeaters of Hassoun would be responsive to the same clock. Ex-1003, ¶¶250, 252. Further, a POSA would understand that a single clock signal generator can produce the various clocks needed from a single source. Ex-1003, ¶¶250, 253, 90; Ex-1013, 6:18–21.

A POSA would have been motivated, with a reasonable expectation of success, to include on-chip clocking circuitry (“a clock signal generator”), such as taught by Sullam, such that *the plurality of network stations and the M*N data storage elements* would be *responsive to the clock signal generator* as claimed. Ex-1003, ¶¶253–255. For Grounds 1 and 2, the clocking circuitry would have been expected to provide the clock signal as required by Bertozzi. Ex-1003, ¶¶251, 253. For Ground 3, the clocking circuitry would have predictably provided “a wide variety of clocking signal frequencies to the different” clock domains as required by Dielissen. Ex-1013, 6:18–21; Ex-1003, ¶¶252–253.

A POSA would have been motivated to use on-chip clocking circuitry (“clock signal generator”) with Bertozzi (Grounds 1–2) or the Dielissen combination (Ground 3). Ex-1003, ¶254. First, as discussed above, Dielissen and Bertozzi teach the need for clocking on an integrated circuit. Ex-1003, ¶254. Second, an on-chip clock signal generator would have predictably simplified the chip by eliminating the need for external hardware. Ex-1003, ¶254. Third, an on-chip clock signal generator was known to require less total space. Ex-1003, ¶254.

A POSA would have had a reasonable expectation of success. Ex-1003, ¶255. One, the use of on-chip clocking circuitry was well known by the date of the purported invention. Ex-1003, ¶255; *see also*, Ex-1013. Two, Sullam is closely related to the technology disclosed by Bertozzi and Dielissen: all relate to on-chip

technology, specifically on-chip computers. Ex-1005, 2, Fig. 1; Ex-1007, 1, 5, Fig. 11; Ex-1013, 1:51–56 and 6:15–22; Ex-1003, ¶255; *see also* Ex-1003, 96–97, 74 (Bertozzi), 192–193, 82 (Dielissen). Three, as discussed above, Bertozzi and Dielissen disclose the integration of various cores onto an integrated circuit. Ex-1005, 2; Ex-1007, 1; Ex-1003, ¶255. A POSA would understand that Sullam’s clocking circuitry 112 could have been predictably integrated in Bertozzi or Dielissen as a core to generate the needed clocks, using only routine skill. Ex-1003, ¶255.

XI. DISCRETIONARY DENIAL IS NOT APPROPRIATE

A. Discretionary Denial Under 35 U.S.C. §325(d) is Not Warranted

All six Becton Dickinson factors weigh in favor of institution. *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017); *see also Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020). The Board has consistently “held that a reference that ‘was neither applied against the claims nor discussed by the Examiner’ does not weigh in favor of exercising [] discretion under § 325(d).” *Fasteners for Retail, Inc. v. RTC Indus., Inc.*, IPR2019-00994, Paper 9 at 7–11 (PTAB Nov. 5, 2019). Here, none of the prior art references relied upon by Petitioners’ Grounds 1 and 2 are cited on the face of the ’2893 patent, and

none of the grounds in this Petition were evaluated during prosecution.¹³ The Examiner improperly concluded that the Challenged Claims were not anticipated or obvious because the Examiner did not consider the asserted prior art, particularly in the references and combinations presented herein. *Bowtech, Inc. v. MCP IP, LLC*, IPR2019-00383, Paper 14 at 5 (PTAB Aug. 6, 2019) (petitioner did not need to explain how the Examiner erred “because the Examiner did not consider the combinations of the references asserted in the Petition at all...”).

B. Discretionary Denial Under 35 U.S.C. §314(a) Is Not Warranted

Evaluation of the factors under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) and the clarifications made by the Director of the United States Patent and Trademark Office favors institution. *See* USPTO Memorandum, Interim Procedure for Discretionary Denials in AIA Post Grant Proceedings with Parallel District Court Litigation, 2 (June 21, 2022) (“Director’s Memo”).

First, Petitioners hereby stipulate “that if the PTAB institutes *inter partes* review, ‘Petitioner[s] will not pursue in [*Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00481 (E.D. Tex.) and *Network*

¹³ The Dielissen reference forming part of Ground 3 was disclosed in an IDS and is cited on the face of the patent but was not cited or discussed by the Examiner during prosecution.

System Technologies, LLC v. Qualcomm Inc. et al., 1:22-cv-01331 (W.D. Tex.)] the specific grounds [asserted in this petition], or on any other ground ... that was raised or could have been reasonably raised in an IPR.’” *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 13–14 (PTAB Dec. 1, 2020) (precedential as to § II.A). Based on this stipulation alone, discretionary denial under § 314(a) is not appropriate. Director’s Memo at 3.

Moreover, other relevant factors also weigh against discretionary denial under §314(a). First, no trial date has been set yet in the Qualcomm Litigation and, while a tentative trial date has been set for the Samsung Litigation, that setting could change. Second, it is still relatively early in both Litigations. No claim construction opinions have been issued, no depositions have been taken, and no expert reports have been submitted. Finally, PO has not pressed for early trial or decision in the Litigations, nor would such relief be appropriate, particularly considered that many of the products accused of infringement have been on the market for well more than a decade.

Finally, this Petition presents “compelling” arguments for unpatentability of the Challenged Claims, including clear anticipation by a reference not considered during prosecution, as shown in Ground 1. *See* Director’s memo at 4–5 (“the PTAB will not deny institution based on *Fintiv* if there is compelling evidence of unpatentability”); *see also CommScope Techs. LLC v. Dali Wireless, Inc.*,

IPR2022-01242, Paper 23 at 3–5 (Feb. 27, 2023) (precedential) (evidence is compelling when it is “highly likely that the petitioner would prevail with respect to at least one challenged claim”). Thus, institution is consistent with the significant public interest against “leaving bad patents enforceable.” *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

XII. MANDATORY NOTICES

A. Real Parties-in-Interest

Qualcomm Incorporated, Qualcomm Technologies, Inc., Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC are the real parties-in-interest.

B. Related Matters

The '2893 Patent is the subject of multiple parallel proceedings in the Eastern District of Texas and Western District of Texas, including a suit against Samsung captioned *Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00481 (E.D. Tex.) (“the Samsung litigation”), and a suit against Qualcomm captioned *Network System Technologies, LLC v. Qualcomm Inc. et al.*, No. 1:22-cv-01331 (W.D. Tex.) (“the Qualcomm

litigation”).¹⁴ The ’2893 Patent is also the subject of the following proceedings: *Network System Technologies, LLC v. Texas Instruments Inc.*, No. 2:22-cv-00482 (E.D. Tex.); *Network System Technologies, LLC v. Lenovo Group Ltd.*, No. 2:23-cv-00167 (E.D. Tex.); *Network System Technologies, LLC v. Ford Motor Co.*, No. 2:23-cv-00440 (E.D. Tex.); *Network System Technologies, LLC v. OnePlus Technology (Shenzhen) Co., Ltd.* 2:23-cv-00520 (E.D. Tex.). These actions may affect, or be affected by, decisions in this proceeding. Nothing herein should be taken as an endorsement of PO NST’s positions in the co-pending litigations.

C. Lead and Back-up Counsel

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¹⁴ Arteris, Inc. (“Arteris”) is named as a Defendant in the Qualcomm litigation.

However Arteris is an independent entity unrelated to Petitioners and is not a real party-in-interest to this Petition.

Back-up Counsel	Back-up Counsel
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D. Service Information

Please address all correspondence to lead and back-up counsel at the addresses shown above. Petitioners consent to electronic service by e-mail.

E. Fees

The Board is authorized to charge Carlson Caspers Vandenburg & Lindquist, P.A.'s deposit account, No. 50-2880, for all fees required for filing this IPR.

XIII. CONCLUSION

In view of the evidence presented, Petitioner respectfully requests that the Board institute this IPR and cancel each challenged claim.

Dated: December 20, 2023

Respectfully submitted,

/ J. Derek Vandenburg/

J. Derek Vandenburg (Lead Counsel)

Registration No. 32,179

Carlson, Caspers, Vandenburg
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APPENDIX: LISTING OF CHALLENGED CLAIMS

U.S. Patent No. 8,072,893

Independent claims 10, 1, 7, Dependent claims 2, 3, 6, 8, 9

Reference	Claim Limitation
Independent Claim 10	
[10.pre]	A method of designing an integrated circuit comprising
[10.pre.a]	a plurality of functional blocks, and
[10.pre.b]	a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks,
[10.pre.c]	each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two,
[10.pre.d]	the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface;
[10.e]	the method comprising the acts of: identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and
[10.f]	in response to the identifying act, inserting M*N data storage elements into the data communication network, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel.
Independent Claim 1	
[1.pre]	An integrated circuit comprising:
[1.a]	a plurality of functional blocks; and

[1.b]	a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks,
[1.c]	each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two,
[1.d]	the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface,
[1.e]	the data communication network comprising a first network station and a second network station interconnected through a first communication channel,
[1.f]	the data communication network further comprising M*N data storage elements, M being a positive integer, the data communication introducing a delay of M*N cycles on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold.
Dependent Claim 2	
[2]	The integrated circuit as claimed in claim 1, wherein each communication channel of the plurality of communication channels comprises: a first subchannel between an input port of a first associated network station and an output port of a second associated network station; and a second subchannel between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations.
Dependent Claim 3	
[3]	The integrated circuit as claimed in claim 2, wherein the M*N data storage elements are distributed over the first subchannel and the second subchannel of the first communication channel.

Dependent Claim 6	
[6]	The integrated circuit as claimed in claim 1, wherein $M=1$.
Dependent Claim 8	
[8]	The integrated circuit as claimed in claim 1, further comprising a clock signal generator, the plurality of network stations and the $M*N$ data storage elements being responsive to the clock signal generator.
Dependent Claim 9	
[9]	The integrated circuit as claimed in claim 1, wherein each network station comprises a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port.
Independent Claim 7	
[7.pre]	An integrated circuit comprising:
[7.a]	a plurality of functional blocks; and
[7.b]	a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks,
[7.c]	each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two,
[7.d]	the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface,

[7.e]	the data communication network comprising a first network station and a second network station interconnected through a first communication channel,
[7.f]	the data communication network further comprising $M*N$ data storage elements, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel,
[7.g]	wherein each communication channel of the plurality of communication channels comprises: a first subchannel between an input port of a first associated network station and an output port of a second associated network station; and a second subchannel between an input port of the second associated network station and an output port of the first associated network station, and
[7.h]	wherein the first subchannel and the second subchannel of the first communication channel each comprise a delay introduced by $\frac{1}{2}*M*N$ data storage elements.

CERTIFICATE OF COMPLIANCE

The undersigned hereby certifies that the foregoing Petition for *Inter Partes* Review contains 13,978 words, excluding those portions identified in 37 C.F.R. §42.24(a), as measured by the word-processing system used to prepare this paper.

/ J. Derek Vandenburg/
J. Derek Vandenburg

CERTIFICATE OF SERVICE

I certify that on December 20, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,072,893 and supporting exhibits to be served via overnight delivery on the Patent Owner at the following correspondence address of record as listed on PAIR:

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