

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket

DIELISSEN et al.

000268

Serial No.

Group Art Unit

Filed: CONCURRENTLY

Ex.

INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN
METHOD

Commissioner for Patents
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified
application as follows:

IN THE CLAIMS

Please amend the claims as follows:

1. (original) An integrated circuit (10) comprising:
 - a plurality of functional blocks (101, 102, 103, 104); and
 - a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108), the data communication network (100) comprising a first network station (140) and a second network station (120) interconnected through a first communication channel (150), the network comprising M*N data storage elements (160), M being a positive integer, for introducing a delay of M*N cycles on the first communication channel (150).

2. (original) An integrated circuit (10) as claimed in Claim 1, wherein each communication channel (150) comprises:
 - a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station; and

a second subchannel (154) between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations.

3. (original) An integrated circuit (10) as claimed in Claim 2, wherein the $M*N$ data elements (160) are distributed over the first subchannel (152) and the second subchannel (152; 154) of the first communication channel (150).

4. (original) An integrated circuit as claimed in claim 3, wherein:

the first network station is arranged to evaluate the routing information in a first cycle and the second network station is arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles; and

the first subchannel (152) of the first communication channel (150) exhibits a delay of A cycles implemented by A data storage elements (160) and the second subchannel (154) exhibits a delay of B cycles implemented by B data storage elements (160), A and B being positive integers, with $A + B = M*N$.

5. (original) An integrated circuit as claimed in claim 4, wherein any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with $C \text{ modulo } N = A$; and any network path to the further network station from the first network station comprises D delay elements; D being a positive integer with $D \text{ modulo } N = B$.

6. (currently amended) An integrated circuit (10) as claimed in ~~Claim 1-5~~Claim 1, wherein $M = 1$.

7. (original) An integrated circuit (10) as claimed in Claim 3, wherein the first subchannel (152) and the second subchannel (154) of the first communication channel (150) each comprise a delay introduced by $\frac{1}{2} * M * N$ data storage elements (160).

8. (currently amended) An integrated circuit (10) as claimed in Claim 1-~~or 2~~, further comprising a clock signal generator, the plurality of network stations (110, 120, 130, 140) and the $M * N$ storage elements (160) being responsive to the clock signal generator.

9. (currently amended) An integrated circuit (10) as claimed in claim 1-~~or 2~~, wherein each network station (110, 120, 130, 140) comprises a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port.

10. (original) A method of designing an integrated circuit (10) comprising a plurality of functional blocks (101, 102, 103, 104), and a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks

(101, 102, 103, 104), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface; the method comprising:

identifying a first communication channel (150) between a first network station (140) and a second network station (120) that has a data transfer delay exceeding a predefined delay threshold; and

inserting $M \times N$ data storage elements (160) into the data communication network (100), M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel (150).

11. (original) A method as claimed in Claim 10, wherein each communication channel (150) comprises a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station and a second subchannel (154) between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations; and

the first network station being arranged to evaluate the routing information in a first cycle and the second network station being arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles, the method further comprising:

inserting A data storage elements into the first subchannel (152) of the first communication channel (150) for introducing a delay of A cycles onto said first subchannel; and

inserting B data storage elements into the second subchannel (154) of the first communication channel (150) for introducing a delay of B cycles onto said second subchannel; A and B being positive integers, with $A + B = M \cdot N$.

REMARKS

This is a preliminary amendment. The claims are amended for non-statutory reasons: to remove multiple dependencies, to correct one or more informalities, to remove figure label number(s), and/or to replace European-style claim phraseology with American-style claim language. The claims are not narrowed in scope and no new matter is added.

The amendment to the claims does not address issues of patentability. Applicant(s) reserve(s) the right to continue prosecution of any subject matter canceled, or not claimed because of eliminating multiple dependencies, in this, a divisional, or other continuing application.

Examination of the application is now respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

By /Yan Glickberg/
Yan Glickberg, Reg. 51,742
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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD		
First Named Inventor/Applicant Name:		JOHN DIELISSSEN		
Filer:		Michael E. Marion/JEANNE RUSCIANO		
Attorney Docket Number:		000268 US1		
Filed as Large Entity				
U.S. National Stage under 35 USC 371 Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
National Stage Fee	1631	1	310	310
Natl Stage Search Fee - Report provided	1642	1	410	410
National Stage Exam - all other cases	1633	1	210	210
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				930

Electronic Acknowledgement Receipt	
EFS ID:	2349393
Application Number:	11912175
International Application Number:	PCT/IB06/51218
Confirmation Number:	5577
Title of Invention:	INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD
First Named Inventor/Applicant Name:	JOHN DIELISSSEN
Customer Number:	24737
Filer:	Michael E. Marion/JEANNE RUSCIANO
Filer Authorized By:	Michael E. Marion
Attorney Docket Number:	000268 US1
Receipt Date:	22-OCT-2007
Filing Date:	
Time Stamp:	13:09:53
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 930
RAM confirmation Number	6236
Deposit Account	141270
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	000268-ADS.PDF	1018638	no	4
			b46c64502a20804e05e0ca0ad722195b8dffe3c		
Warnings:					
Information:					
2	Oath or Declaration filed	000268-Dec.pdf	1120001	no	4
			021a72772d2d8acac7b16aee7d7df7d41f971c9		
Warnings:					
Information:					
3	Documents submitted with 371 Applications	WO2006111931-Publ.pdf	1158351	no	27
			36bfe1df0f9d08cd6e8f2a413ed4a8f624b229df		
Warnings:					
Information:					
4		000268-PRELIM.pdf	60068	yes	7
			b893733445c002bec67aec59f8ac2fe4d2a5ab59		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Preliminary Amendment		1	1	
	Claims		2	6	
	Applicant Arguments/Remarks Made in an Amendment		7	7	
Warnings:					
Information:					
5	Fee Worksheet (PTO-06)	fee-info.pdf	8458	no	2
			78a839297eabe8da8692d6832d4b4397f4f9134e		
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Total Files Size (in bytes):			3365516		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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New International Application Filed with the USPTO as a Receiving Office

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	000268 US1
		Application Number	
Title of Invention	INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

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Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	JOHN		DIELISSEN		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
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Citizenship under 37 CFR 1.41(b)ⁱ		NL			
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City	WEERT	State/Province			
Postal Code	6003 CS	Countryⁱ	NL		
Applicant 2					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	EDWIN		RIJPKEMA		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
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Citizenship under 37 CFR 1.41(b)ⁱ		NL			
Mailing Address of Applicant:					
Address 1		KLEEFKRUID 4			
Address 2					
City	NIEUWERKERK A/D IJSSEL	State/Province			
Postal Code	2914 BK	Countryⁱ	NL		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence Information of this application.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	000268 US1	
		Application Number		
Title of Invention	INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD			
Customer Number	24737			
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Application Information:

Title of the Invention	INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD			
Attorney Docket Number	000268 US1	Small Entity Status Claimed	☐	
Application Type	Nonprovisional			
Subject Matter				
Suggested Class (if any)		Sub Class (if any)		
Suggested Technology Center (if any)				
Total Number of Drawing Sheets (if any)		Suggested Figure for Publication (if any)		
Publication Information:				
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)				
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not been and will not be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.				

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ US Representative (37 CFR 11.9)
Customer Number	24737		

Domestic Priority Information:

This section allows for the applicant to claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c). Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	a 371 of international	PCT/IB2006/051218	2006-04-20
Additional Domestic Priority Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	000268 US1
		Application Number	
Title of Invention	INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD		

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
05103232.4	EP	2005-04-21	☒ Yes ☐ No

Additional Foreign Priority Data may be generated within this form by selecting the Add button.

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Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1

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If the Assignee is an Organization check here. ☒

Organization Name KONINKLIJKE PHILIPS ELECTRONICS, N.V.

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Country ⁱ	NL	Postal Code	5621 BA
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Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Yan Glickberg/		Date (YYYY-MM-DD)	2007-09-19
First Name	YAN	Last Name	GLICKBERG	Registration Number
				51742

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
26 October 2006 (26.10.2006)

PCT

(10) International Publication Number
WO 2006/111931 A1

(51) International Patent Classification:
H04L 12/56 (2006.01)

(21) International Application Number:
PCT/IB2006/051218

(22) International Filing Date: 20 April 2006 (20.04.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
05103232.4 21 April 2005 (21.04.2005) EP

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

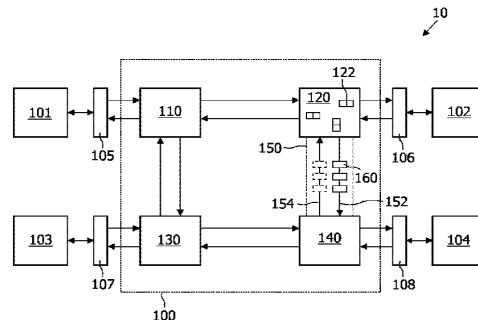
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD



(57) Abstract: An integrated circuit (10) comprises a plurality of functional blocks (101, 102, 103, 104) and a data communication network (100) comprising a plurality of network stations being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104). Each data package comprising N data elements including a data element comprising routing information for the network stations (110, 120, 130, 140), N being an integer of at least two. The plurality of network stations comprises a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces, each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108), the data communication network (100) comprising a first network station (140) and a second network station (120) interconnected through a first communication channel (150), the network comprising M*N data storage elements (160), M being a positive integer, for introducing a delay of M*N cycles on the first communication channel (150). An integrated circuit (10) comprises a plurality of functional blocks (101, 102, 103, 104) and a plurality of data routers (110, 120, 130, 140), each being coupled to a functional block (101, 102, 103, 104). The introduction of a delay of one or more data packages on a slow communication channel (150) facilitates an increase of the maximum clock speed of the data communication over the data communication network (100).

WO 2006/111931 A1

DESCRIPTION**INTEGRATED CIRCUIT WITH DATA COMMUNICATION
NETWORK AND IC DESIGN METHOD**

The present invention relates to an integrated circuit having a plurality of functional blocks interconnected via a data communication network.

Nowadays, most integrated circuits (ICs) are very large scale integration (VLSI) circuits having a large number of features that typically implement a large number of functions on board the IC. The various functions may be located in discrete functional blocks, e.g. system on chip (SoC) architectures. The interconnect of the functional blocks poses a design challenge, because the high clock speeds of modern ICs facilitate the processing of large amounts of data, which means that the interconnect of the IC must be capable of communicating large amounts of data between the functional blocks.

To facilitate flexible communication on the one hand and to limit the amount of wires required on the other hand, ICs may incorporate a data communication network, also referred to as a network on chip (NoC). Such networks typically comprise a plurality of network stations, each associated with a functional block, interconnected via communication channels, e.g. wires. The plurality of network stations include a plurality of data routers and a plurality of network interfaces, each data router being coupled to a functional block via a network interface. The data can be communicated over the network in the form of packages that include a mixture of data and routing instructions for the network stations. In networks facilitating duplex communication, a pair of network stations is typically interconnected via at least a pair of communication subchannels to facilitate the two-way communication.

A problem associated with communication channels, e.g. wires, on ICs is that the clock speed at which the IC can operate may be determined by the slowest communication channel, i.e. the channel exhibiting the largest data

transfer delay. Several solutions for such a problem exist, see for instance Carloni et al.: Coping with latency in SoC design, IEEE Micro 5, Vol. 22, pages 24-35, IEEE 2002, in which a number of solutions are presented. A possible solution is to introduce a data storage element such as a latch into the slowest data communication channel. Consequently, the clock speed of the data communication part of the IC can be increased at the expense of an additional clock cycle for the communication along the slowest communication channel.

Unfortunately, such a solution cannot straightforwardly be applied to ICs communicating data between the functional blocks via an integrated network, especially when the nature of the communicated data differs per clock cycle; see E. Rijpkema et al.: Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip; IEE Proc.- Comput. Digit. Tech. 2003, page 1-9 (IEE proceedings online no. 20030830), for an example of such a network. Such a network operates on the principle that a network station such as a data router receives the routing data incorporated in the data packet during a predefined clock cycle. Delaying the communication to that router over a slow communication channel by a clock cycle to speed up the rest of the network would cause the routing data to arrive outside the predefined clock cycle, causing erroneous behaviour of the network.

The present invention seeks to improve the data communication speed of a network of an integrated circuit according to the opening paragraph.

According to an aspect of the invention, there is provided an integrated circuit a plurality of functional blocks and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, the data

communication network comprising a first network station and a second network station interconnected through a first communication channel, the network comprising $M \times N$ data storage elements, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel.

The invention is based on the realization that the correct operation of the network relies on the maintenance of the correct periodicity between the network stations. Because the data packages have a fixed size of N data elements, the communication of a complete package between two network stations takes N clock cycles, or N handshake driven data transfers in case of an asynchronous implementation of the network. The routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package, e.g. the first data element (i.e. a header), although other data elements may (also) contain such information. Since a network station expects routing information to arrive periodically (i.e. after every N cycles), the introduction of a delay on the first communication channel (which typically is the slowest channel of the network) matching such a period, i.e. by delaying the whole data package rather than a single data element, the delayed data package is received by the receiving network station during the appropriate period, e.g. clock cycle.

Each communication channel may comprise a first subchannel between an input port of a first associated network station and an output port of a second associated network station and a second subchannel between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations. The $M \times N$ data elements may be distributed over the subchannels of the first communication channel.

In a preferred embodiment, the first network station is arranged to evaluate the routing information in a first cycle and the second network station is arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles; and the first subchannel of the first communication channel exhibits a delay of A cycles implemented by A data storage elements and the second subchannel

exhibits a delay of B cycles implemented by B data storage elements, A and B being positive integers, with $A + B = M*N$.

The introduction of a phase shift in the routing evaluation phase for a one of the network stations in the network has the advantage that the number of delay elements in a data communication (sub)channel can be smaller than the number of data elements in a data package, thus improving the latency of that particular data communication (sub)channel. The drawback is that all communication to the phase-shifted network station has to run via the delayed communication channel to introduce the appropriate phase shift. This limitation can be avoided, however, by ensuring that any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with $C \text{ modulo } N = A$; and any network path to the further network station from the first network station comprises D delay elements; B being a positive integer with $D \text{ modulo } N = B$. This maintains the correct phase relation between the first network station and any other network station that operate on a different router information evaluation phase than the first network station, thus maintaining the optimal flexibility in the network.

In an alternative embodiment, each subchannel of the first communication channel comprises a delay introduced by $\frac{1}{2}*M*N$ data storage elements, with $\frac{1}{2}*M*N$ typically corresponding to the size of a data package. Consequently, since both paths of the duplex communication channel are likely to have similar lengths and similar delay characteristics, the partitioning of both subchannels allows for the improvement of the speed of the network in both communication directions.

Preferably, $M=1$ in order to minimize the number of required delay elements, which will minimize the delay introduced on the first communication channel.

In a synchronous implementation, the IC further comprises a clock signal generator, the plurality of network stations and the $M*N$ storage elements being responsive to the clock signal generator, to ensure that no

data conflicts can arise between the data routers and the $M*N$ storage elements.

Each network station may comprise a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port. Such an implementation allows for the interleaving of packages requiring different service levels, e.g. best effort and guaranteed bandwidth service levels.

According to a further aspect of the invention, there is provided a method of designing an integrated circuit comprising a plurality of functional blocks and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface; the method comprising identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and inserting $M*N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel. Such a method facilitates the design of an integrated circuit of the present invention.

In a preferred embodiment, each communication channel comprises a first subchannel between an input port of a first associated network station and an output port of a second associated network station and a second subchannel between an input port of the second associated network station and an output port of the first associated network station for enabling

duplex communication between the two associated network stations; and the first network station being arranged to evaluate the routing information in a first cycle and the second network station being arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles, the method further comprising inserting A data storage elements into the first subchannel of the first communication channel for introducing a delay of A cycles onto said first subchannel; and inserting B data storage elements into the second subchannel of the first communication channel for introducing a delay of B cycles onto said second subchannel; A and B being positive integers, with $A + B = M \cdot N$. Such a method facilitates the design of a preferred embodiment of the integrated circuit of the present invention.

The invention is described in more detail and by way of non-limiting examples with reference to the accompanying drawings, wherein:

Fig.1 shows an embodiment of an IC of the present invention;

Fig. 2 shows the timing behaviour along a delayed communication channel of said IC;

Fig. 3 shows another embodiment of an IC of the present invention;

Fig. 4 shows the timing behaviour along a delayed communication channel of said IC; and

Fig. 5 shows yet another embodiment of an IC of the present invention including its timing behaviour.

It should be understood that the Figures are merely schematic and are not drawn to scale. It should also be understood that the same reference numerals are used throughout the Figures to indicate the same or similar parts.

Fig. 1 shows an integrated circuit (IC) 10 according to an embodiment of the present invention. The IC 10 has four functional blocks 101-104, e.g. processing units, which are interconnected via a data communication network 100 including data routers 110, 120, 130, 140, which respectively are coupled

to the functional blocks 101-104 via respective network interfaces 105-108. The data routers 110, 120, 130, 140 and the network interfaces 105-108 comprise the network stations of the data communication network 100. Exemplary embodiments of such data routers and network interfaces can for instance be found in: "An efficient On-Chip Network Interface Offering Guaranteed Services, Shared Memory Abstraction and Flexible Network Configuration" by Radulescu et al.; Proceedings of Design, Automation and Test Conference in Europe, February 2004, and in E. Rijpkema et al.: Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip; IEE Proc.- Comput. Digit. Tech. 2003, page 1-9 (IEE proceedings online no. 20030830) as well as in the relevant references therein, the relevant passages thereof being incorporated by reference.

The network stations of the data communication network 100 are interconnected via a plurality of data communication channels 150. The communication channels 150 may comprise one or more wires, e.g. data buses. The data communication network 100 is configured to allow flexible communication of data streams between the functional blocks 101-104. Typically, such a data stream comprises one or more data packages, with each data package comprising N data elements, with N being an integer having a value of at least 2. At least one of the N data elements in a package, e.g. the first data element, comprises routing instructions for the destination network station. Such data packages are sometimes referred to as flow instruction units (flits).

The data streams may be communicated over the network 100 using known communication techniques such as store and forward routing, in which a complete data stream is stored in a data router before it is forwarded to its next destination, or wormhole routing, in which the data routers can send a stored data package to its next destination before the complete data stream has been received. The latter technique has the advantage that the data routers 110, 120, 130, 140 need less storage capacity but both techniques are equally feasible, and other techniques may be used as well.

The data network 100 shown in Fig.1 is a duplex network, i.e. it allows simultaneous data communication in two directions. It is emphasized, however, that the present application is equally applicable to simplex networks, i.e. networks that do not support simultaneous two-way communication. To facilitate the duplex communication over data network 100, each communication channel 150 comprises a first subchannel 152 and a second subchannel 154 between respective inputs and outputs of two neighbouring network stations, e.g. data routers 120 and 140. This facilitates time-division multiple access (TDMA) data communication, for instance of a guaranteed bandwidth and a best effort service. To this end, each network station in the data communication network 100 has a plurality of memories, each comprising a first memory element and a second memory element, e.g. memory 122 in data router 120, associated with a communication port, i.e. an input port or an output port of the data router, or more precisely, associated with a service level of a communication via that communication port. Obviously, the plurality of memories may be implemented as a single memory having enough storage to keep track of each input or output port of the network station, as will be explained below by means of a communication between two data routers by way of example only. It will be appreciated that the same teachings can be applied to communications between a data router and a network interface or to communications between a network interface and a functional block without departing from the teachings of the present invention.

Typically, the header of a first data package will comprise information about the destination of the data package as well as the service level of the data package, e.g. guaranteed bandwidth or best effort service. The service level will be flagged by setting a bit in the appropriate memory element of the destination output port of the data router. For subsequent data packages having the same service level, the data router will know that these data packages belong to a data stream in progress because the appropriate bit has been stored in the associated memory element. The last data package of the data stream contains an indicator causing the data router to reset said bit.

Such a mechanism allows interleaving of data packages of two data streams over a single communication channel.

In Fig. 1, the communication channel 150 between data routers 120 and 140 has been identified as the communication channel in the network 100 exhibiting a data transfer delay exceeding a predetermined delay threshold. Such an identification can be made at the IC design stage by subjecting the design to a simulation of the delay behaviour of the IC 10 using available timing behaviour simulation tools. To avoid having to limit the communication speed, e.g. the clock speed, of the data communication network 100 in accordance with the delay characteristics of the communication channel 150 between two network stations, e.g. data routers 120 and 140, this communication channel (which will be referred to as the slow communication channel 150) is equipped with $M*N$ data storage elements to introduce a delay of $M*N$ cycles onto the communication channel, with N corresponding to the size of a data package, thus allowing an increase of the maximum communication frequency of the data network 100 at the expense of the introduction of a delay of a single data package, i.e. the number of clock cycles it takes to communicate such a data package, on the slow communication channel 150.

The network 100 shown in Fig. 1 is arranged to communicate data packages with size $N=3$. Other values of N are equally feasible. The first subchannel 152 of the slow communication channel 150 is extended with $N=3$ data storage elements 160. Optionally, the second subchannel 154 of the slow communication channel 150 is also extended with $N=3$ data storage elements 160, in which case $M=2$. Since the first subchannel 152 and the second subchannel 154 typically will be in each others vicinity, their respective delay characteristics typically will be similar, thus requiring the introduction of data storage elements 160 on both subchannels. However, in cases where the respective subchannels exhibit different delay characteristics, for instance because the subchannels have different lengths or because of the nature of the timing techniques used, e.g. waterfall clocking, the introduction of N data

elements 160 on only one of the subchannels can be sufficient, in which case $M=1$.

It will be appreciated that the physical placement of the data storage elements 160 on the subchannels 152 and 154 is by way of example only; an implementation where the data storage elements 160 are integrated in the associated network stations, e.g. data router 120 or data router 140 is equally feasible. It will be appreciated that the same teachings can be applied to communications between a data router and a network interface or to communications between a network interface and a functional block without departing from the teachings of the present invention. The same applies to the other embodiments of the data communication network 100, e.g. the embodiments shown in Fig. 3 and 5. The data storage elements 160 may be a pipeline or a buffer of latches or flipflops, and may be implemented using synchronous or asynchronous storage elements. In Fig.1, the data storage elements 160 are responsive to the same clock signal (not shown) as the network stations including data routers 110, 120, 130, 140 and network interfaces 105-108.

Fig. 2 shows the timing behaviour of the communication along the slow channel 150 extended with 3 data storage elements 160 on the first subchannel 152 interconnecting an output port of data router 120 with an input port of the data router 140. At clock cycle t , the data router 120 employing wormhole routing receives the first data element h of a data package (indicated by the bold box) having a size of 3 data elements. The subsequent data elements $d1$ and $d2$ of this data package are received by the data router 120 at respective clock cycles $t+1$ and $t+2$. The data routers 110, 120, 130, 140 are all configured to periodically evaluate the content of a received data package, that is after every N clock cycles for a data package having a size N data elements. In the embodiment of the IC 10 shown in Fig. 1, all the data routers 110, 120, 130, 140 perform this operation simultaneously, i.e. at the same clock cycle, which is clock cycle t plus every N th clock cycle afterwards, i.e. at $t+3$, $t+6$ and so on, at which the arrival of a header h of a new data package is expected. Such a periodical checking mechanism by a data router

may for instance be implemented using modulo N counters. Consequently, it is essential that the headers of the data packages do not arrive at any data router 110, 120, 130, 140 outside such an evaluation clock cycle.

In line with the principle of wormhole routing, data router 120 starts sending the data package upon its complete receipt, i.e. at clock cycle $t+3$ via the first subchannel 152 of the slow communication channel 150. At this point, it is emphasized that data elements sent via a non-delayed communication channel will arrive at the destination data router in the same clock cycle as they were sent. However, due to the presence of $N=3$ data storage elements 160 in the first subchannel 152 of the slow communication channel 150, the first data storage element 160 receives the header h at $t+3$, passes it on to the second data storage element 160 at $t+4$, which passes it on to the third data storage element 160 at $t+5$, which finally passes it on to the data router 160 at $t+6$, which is in phase with the header evaluation cycle of the data routers 110, 120, 130, 140 in the data network 150. This ensures the correct routing of the data package by the data router 140.

In the embodiment of IC 10 according to the present invention as shown Fig. 3, the data router 140 is configured to evaluate the header of a data package A clock cycles later (or B cycles earlier) than the other data routers 110, 120, 130 in the data network 100, with N corresponding to the number of data elements in a data package and A, B being positive integers with $A+B = M*N$. Typically, A modulo N and B modulo N are not equal to zero.

In Fig. 3, $M = 1$, $N = 3$, $A = 1$ and $B = 2$ by way of example only. In other words, the data router 140 has a phase-shifted routing information evaluation cycle compared to the other data routers in the data network 100. To ensure that the routing information is correctly interpreted, i.e. to ensure that this information arrives at any data router during its appropriate clock cycle, two possible implementations can be chosen. In a first implementation, all communication to and from the phase-shifted data router 140 is routed through the slow communication channel 150. Consequently, only the slow communication channel 150 requires the introduction of $M*N$ data storage elements over its subchannels 152 and 154. The drawback of this

implementation is that the flexibility of the data communication network 100 is reduced.

In the preferred implementation, any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with $C \bmod N = A$, and any network path to the further network station from the first network station comprises D delay elements; B being a positive integer with $D \bmod N = B$. This ensures that the correct phase relation between clock cycle and routing information evaluation is maintained throughout the whole data communication network 100. For instance, in Fig. 3, $C = A$ and $B = D$, with C data elements 160 being introduced in the subchannel 152 between the output port of data router 130 and the input port of data router 140 and with D data elements 160 being introduced in the subchannel 154 between the input port of data router 130 and the output port of data router 140.

In other words, every communication channel 150 between two network stations exhibiting a phase-shifted routing information cycle with respect to each other should incorporate the appropriate number of data storage elements 160 to implement the number of cycles to which the phase shift corresponds. In Fig. 3, this means that all subchannels connected to an input port of the data router 140 are extended with A data storage elements 160 to introduce a delay of A cycles on the communication directed towards the data router 140, and all subchannels connected to an output port of the data router 140 are extended with B data storage elements 160 to introduce a delay of B cycles on the communication originating from the data router 140. Since $A+B = M*N$, each communication channel 150 to which data router 140 is connected incorporates $M*N$ data storage elements 160, thus ensuring the introduction of a delay of exactly M data packages on a communication loop between two neighbouring data routers.

This is explained in more detail in Fig. 4, where a data package consisting of data elements h , $d1$ and $d2$ is sent from data router 120 to data router 140 and back again in the network of IC 10 as shown in Fig. 3. The

routing information evaluation clock cycles for data routers 120 and 140 are indicated by bold vertical lines at the beginning of such a cycle. In other words, data router 120 evaluates the routing information of received data packages at t , $t+3$, $t+6$ and so on, whereas data router 140 evaluates the routing information of received data packages at $t+1$, $t+4$, $t+7$ and so on. Data router 120 sends data element h at $T=t$ to data router 140. At $T=t$, data element h is received by data storage element 160 in the first subchannel 152, which stores the data element h and sends it to the data router 140 at $T = t+1$, which receives the data element h during the same clock cycle and evaluates the routing information comprised in header h .

After the data router 140 has received data element $d1$ at $T = t+2$ and data element $d2$ and $T = t+3$, i.e., after the data router 140 has received the complete data package, the data router 140 sends the first data element of the data package to the data router 140 via the second subchannel 154. Due to the presence of two data storage elements 160 on the second subchannel 154, the first data element h is received by the data router 120 at $T = t+6$, i.e. during a cycle at which the data router 120 is scheduled to evaluate the routing information, with the other two data elements $d1$ and $d2$ respectively arriving at the subsequent cycles $t+7$ and $t+8$. It will be recognized that the data storage elements 160 in the subchannels 152 and 154 operate as phase shifters to ensure that routing information is evaluated at the right time in each data router phase domain. The application of phase shifting techniques has the advantage that the delay introduced on the individual subchannels 152, 154 can be less than a full data package, thus improving the performance of the slow communication channel 150 compared to the solution presented in Fig. 1.

At this point, it will be appreciated that the number of different phase domains can be further extended without departing from the teachings of the present invention. It is reiterated that although the exemplary implementations of the data storage elements is given on a communication channel between two data routers, implementations on channels between other types of network stations, e.g. between a data router and a network interface, are equally feasible.

Fig. 5 shows an asynchronous implementation of a delayed duplex communication channel 150 between two network stations, e.g. data routers 120 and 140, which is robust against clock skew. The data routers 120 and 140 are triggered by clock signal CLK. However, due to the fact that the clock signal has to travel over a longer wire to data router 140 than to data router 120, data router 140 receives a delayed clock signal CLK_d, with a delay of t_1 with respect to the clock signal CLK received by data router 120. In completely synchronous data communication networks 100, this can cause communication errors, because a data package sent by data router 140 at clock cycle t to data router 120 or the first delay element 160 over a slow communication channel 150 between the data routers 120 and 140 may arrive at its destination at cycle $t+1$ rather than at cycle t . As previously explained, this will cause the routing information to arrive at the data router 120 outside its routing information evaluation cycle, which will likely cause the loss of the information due to a routing error.

This risk can be reduced by implementing the $M \times N$ data storage elements 160 as asynchronous FIFO buffers 520 and 540 on the first subchannel 152 and the second subchannel 154 respectively between data routers 120 and 140. This implementation is insensitive to clock skew, at least within certain limits. To improve the robustness against clock skew of the asynchronous FIFO buffers 520 and 540, the buffers may include slightly more than the $M \times N$ data storage elements, as will be explained in more detail below.

The asynchronous FIFO buffers 520 and 540 have communication behaviour independent of the clock CLK; the data is rippled through the FIFO buffers 520 and 540 based on handshake protocols. Such behaviour is usually quicker than synchronous communication because the latter is dominated by the slowest path in the synchronous communication network, as previously explained.

A communication of a data package from data router 120 to FIFO buffer 520 is initiated by a handshake validation signal 501 followed by synchronous data communication 502 of the data elements of a data package having size N ; this communication is governed by data router 120, which is responsive to

clock signal CLK. The data elements take a time period t_2 to ripple through FIFO buffer 520, after which a handshake request 503 is sent to the data router 140. The receipt of an initial handshake request initializes data router 140 and triggers the data router 140 to accept the data communication by sending an acknowledge signal 504 to the FIFO buffer 520, which triggers the data communication 505. The data router 140 will remain initialized until the data stream of data packages has been received completely. The data package receipt periods of data routers 120 and 140 are indicated by the bold horizontal lines over the clock signals clk and clk_d respectively. The data router 140 receives the data communication synchronously and sends the data package synchronously, i.e. one data element per clock cycle, to FIFO buffer 540 N clock cycles after receiving the request signal 503, in accordance with a wormhole routing approach, by sending a handshake validation signal 506 and data communication 507 to the FIFO buffer 540. After a period t_3 , i.e. the time it takes the data elements to ripple through the FIFO buffer 540, the FIFO buffer 540 sends a handshake request signal 508 to data router 120.

Crucially, because data router 120 has already been initialized, i.e. it is already engaged in communicating a data stream to data router 140, data router 120 will only send an acknowledge signal 509 to such a handshake request to enable communication 510 at the beginning of a routing information evaluation cycle of data router 120, as indicated by the vertical dashed line. Alternatively, if the transmission of the data stream from data router 120 to data router 140 had completed prior to the handshake request 508 from FIFO buffer 540 to data router 120, this request would initialize the data router 120. In both cases, the receipt of the routing information in the correct timeslot of data router 120 is ensured despite the clock skew on the clock signal triggering the data routers 120 and 140. In case the clock skew between data router 120 and data router 140 is substantial, the data router 140 may send a first data element of a next data package to the FIFO buffer 540 before this buffer has received the acknowledge signal 509. In such a scenario, the FIFO buffer 509 must be capable of storing more than $M \cdot N$ data elements to avoid the loss of data stored in the FIFO buffer 509. This can be realized by adding

one or more data storage elements to the $M*N$ data storage elements as overwrite protection.

An IC 10 comprising a data communication network 100 according to the present invention can be designed using an IC design method modified as follows. After designing a first version of the IC 10, which can be done using well-known IC design tools, and which will not be further explained for that reason, an evaluation step is performed in which a first communication channel between a network station and a second network station having a data transfer delay exceeding a predefined delay threshold is identified. Consequently, the design of the data communication network 100 is modified according to the teachings of the present invention by inserting $M*N$ data storage elements into the network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel. This allows for an increase of the maximum clock speed at which the data communication network 100 can operate.

The insertion step may comprise inserting A data storage elements into the first subchannel (152) of the first communication channel (150) for introducing a delay of A cycles onto said first subchannel and inserting B data storage elements into the second subchannel (154) of the first communication channel (150) for introducing a delay of B cycles onto said second subchannel with A and B being positive integers and with $A + B = M*N$ to create a phase-shifted data communication network 100 as outlined in Fig. 3 and 4 and their detailed description.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements. In

the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS

1. An integrated circuit (10) comprising:
 - a plurality of functional blocks (101, 102, 103, 104); and
 - a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108), the data communication network (100) comprising a first network station (140) and a second network station (120) interconnected through a first communication channel (150), the network comprising M*N data storage elements (160), M being a positive integer, for introducing a delay of M*N cycles on the first communication channel (150).
2. An integrated circuit (10) as claimed in Claim 1, wherein each communication channel (150) comprises:
 - a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station; and
 - a second subchannel (154) between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations.
3. An integrated circuit (10) as claimed in Claim 2, wherein the M*N data elements (160) are distributed over the first subchannel (152) and the second subchannel (154) of the first communication channel (150).

4. An integrated circuit as claimed in claim 3, wherein:
the first network station is arranged to evaluate the routing information in a first cycle and the second network station is arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles; and
the first subchannel (152) of the first communication channel (150) exhibits a delay of A cycles implemented by A data storage elements (160) and the second subchannel (154) exhibits a delay of B cycles implemented by B data storage elements (160), A and B being positive integers, with $A + B = M \cdot N$.
5. An integrated circuit as claimed in claim 4, wherein any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with $C \bmod N = A$; and any network path to the further network station from the first network station comprises D delay elements; D being a positive integer with $D \bmod N = B$.
6. An integrated circuit (10) as claimed in Claim 1-5, wherein $M = 1$.
7. An integrated circuit (10) as claimed in Claim 3, wherein the first subchannel (152) and the second subchannel (154) of the first communication channel (150) each comprise a delay introduced by $\frac{1}{2} \cdot M \cdot N$ data storage elements (160).
8. An integrated circuit (10) as claimed in Claim 1 or 2, further comprising a clock signal generator, the plurality of network stations (110, 120, 130, 140) and the $M \cdot N$ storage elements (160) being responsive to the clock signal generator.

9. An integrated circuit (10) as claimed in claim 1 or 2, wherein each network station (110, 120, 130, 140) comprises a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port.

10. A method of designing an integrated circuit (10) comprising a plurality of functional blocks (101, 102, 103, 104), and a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface; the method comprising:

identifying a first communication channel (150) between a first network station (140) and a second network station (120) that has a data transfer delay exceeding a predefined delay threshold; and

inserting $M \cdot N$ data storage elements (160) into the data communication network (100), M being a positive integer, for introducing a delay of $M \cdot N$ cycles on the first communication channel (150).

11. A method as claimed in Claim 10, wherein each communication channel (150) comprises a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station and a second subchannel (154) between an input port of the

second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations; and

the first network station being arranged to evaluate the routing information in a first cycle and the second network station being arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles, the method further comprising:

inserting A data storage elements into the first subchannel (152) of the first communication channel (150) for introducing a delay of A cycles onto said first subchannel; and

inserting B data storage elements into the second subchannel (154) of the first communication channel (150) for introducing a delay of B cycles onto said second subchannel; A and B being positive integers, with $A + B = M \cdot N$.

1/3

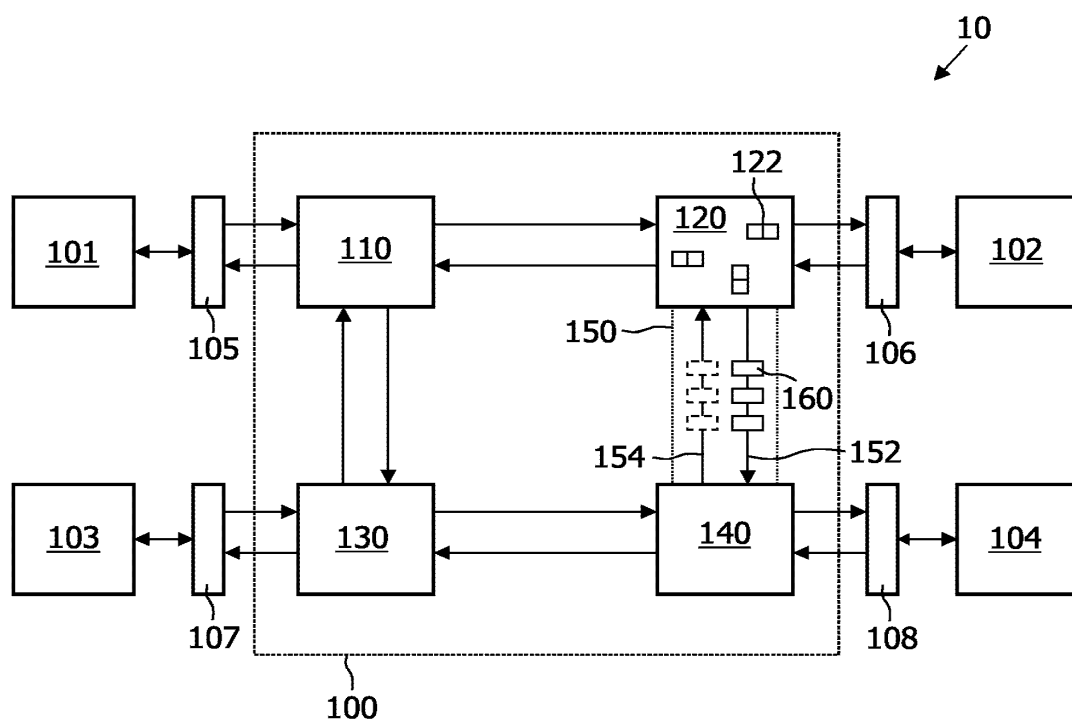


FIG. 1

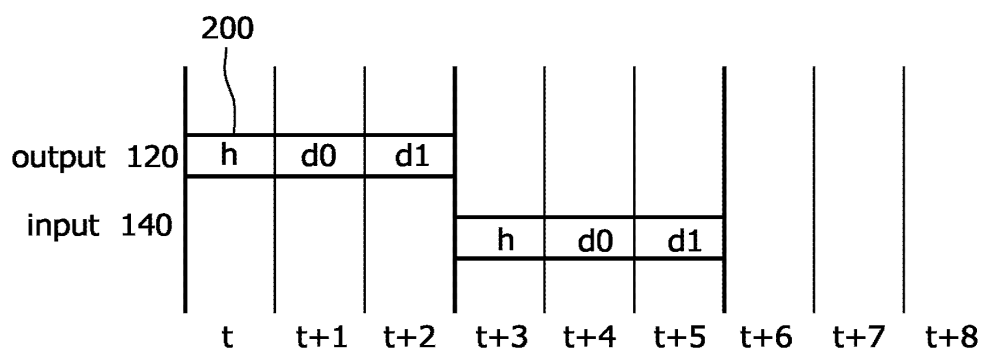


FIG. 2

2/3

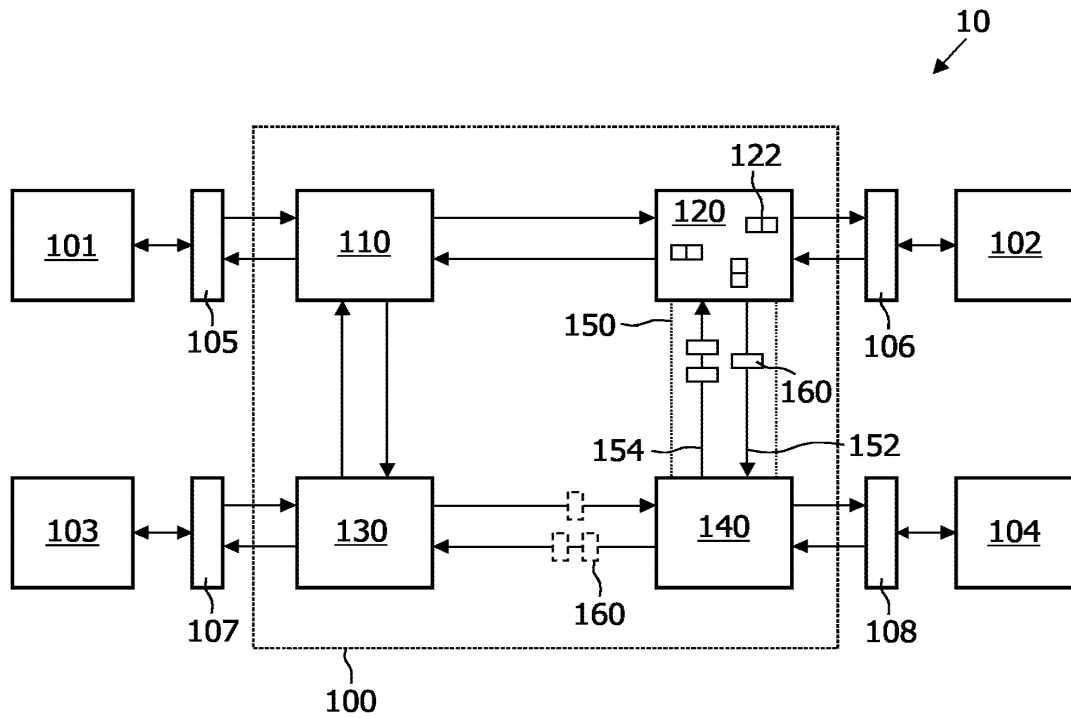


FIG. 3

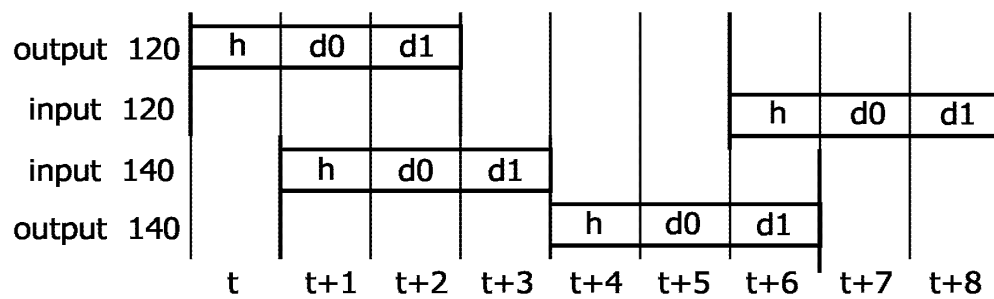


FIG. 4

3/3

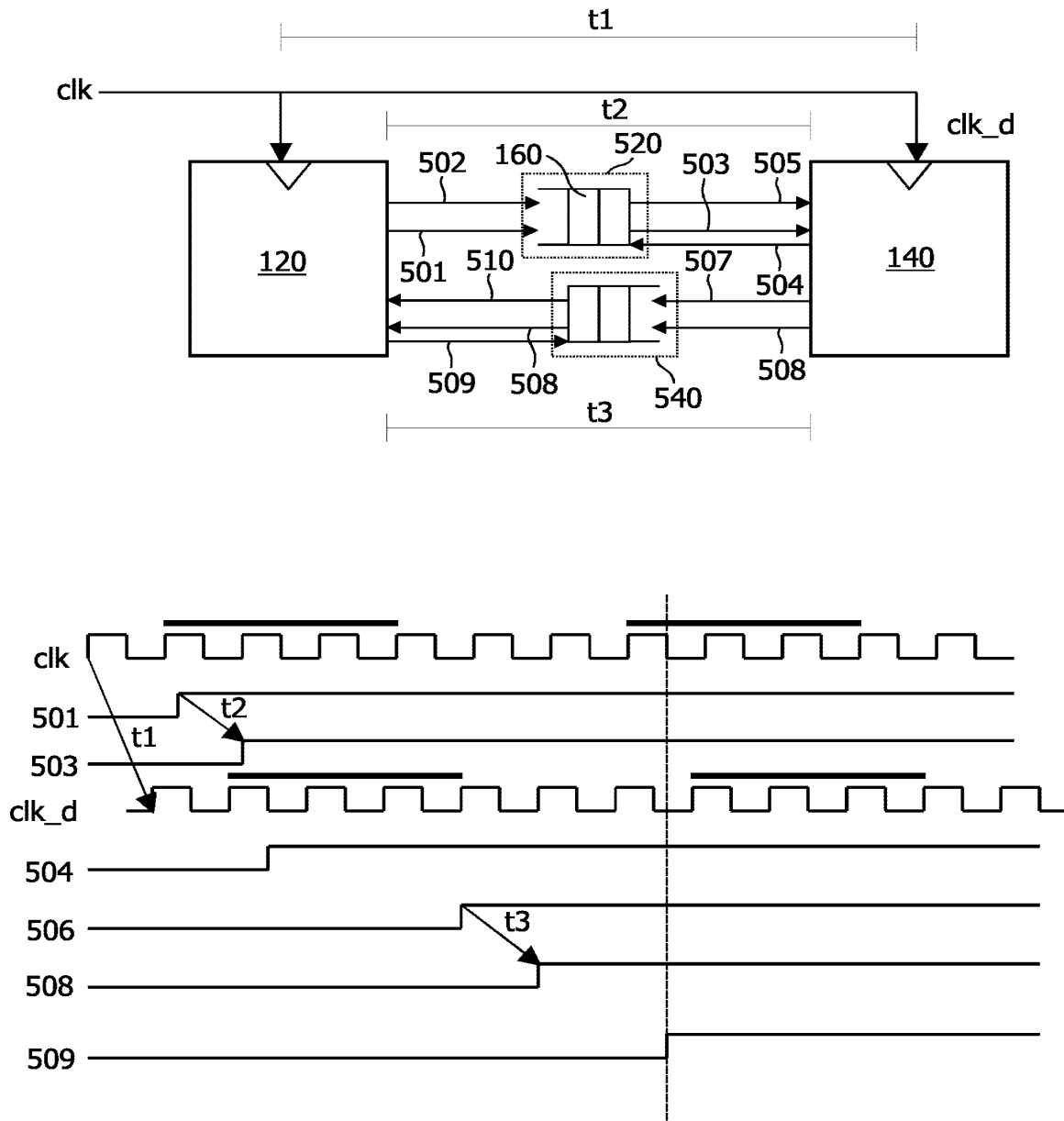


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2006/051218

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04L12/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DIELISSEN J ET AL: "Concepts and Implementation of the Philips Network-on-Chip" INTERNET, [Online] 13 November 2003 (2003-11-13), XP002330547	1,10
Y	abstract page 1, right-hand column - page 2, right-hand column; figures 1-3,11 ----- -/--	2-9,11

☒ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

2 August 2006

Date of mailing of the international search report

16/08/2006

Name and mailing address of the ISA/
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Lastoria, G

INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2006/051218

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	CHANDRA V ET AL: "An interconnect channel design methodology for high performance integrated circuits" DESIGN, AUTOMATION AND TEST IN EUROPE CONFERENCE AND EXHIBITION, 2004. PROCEEDINGS FEB. 16-20, 2004, PISCATAWAY, NJ, USA, IEEE, vol. 2, 16 February 2004 (2004-02-16), pages 1138-1143, XP010684819 ISBN: 0-7695-2085-5 abstract 1 Introduction 2.1 Network-on-Chip Interconnects -----	2-9, 11
A	CARLONI L P; SANGIOVANNI-VINCENTELLI A L: "Coping with latency in SOC design" IEEE MICRO, September 2002 (2002-09), pages 24-35, XP002393174 cited in the application page 26 page 28 page 29, left-hand column; figure 1 page 31; figures 3,4 -----	1-11

Electronic Acknowledgement Receipt	
EFS ID:	2349393
Application Number:	11912175
International Application Number:	PCT/IB06/51218
Confirmation Number:	5577
Title of Invention:	INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD
First Named Inventor/Applicant Name:	JOHN DIELISSSEN
Customer Number:	24737
Filer:	Michael E. Marion/JEANNE RUSCIANO
Filer Authorized By:	Michael E. Marion
Attorney Docket Number:	000268 US1
Receipt Date:	22-OCT-2007
Filing Date:	
Time Stamp:	13:09:53
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 930
RAM confirmation Number	6236
Deposit Account	141270
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	000268-ADS.PDF	1018638	no	4
			b46c64502a20804e05e0ca0ad722195b8dffe3c		
Warnings:					
Information:					
2	Oath or Declaration filed	000268-Dec.pdf	1120001	no	4
			021a72772d2d8acac7b16aee7d7df7d41f971c9		
Warnings:					
Information:					
3	Documents submitted with 371 Applications	WO2006111931-Publ.pdf	1158351	no	27
			36bfe1d0f9d08cd6e8f2a413ed4a8f624b229df		
Warnings:					
Information:					
4		000268-PRELIM.pdf	60068	yes	7
			b893733445c002bec67aec59f8ac2fe4d2a5ab59		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Preliminary Amendment		1	1	
	Claims		2	6	
	Applicant Arguments/Remarks Made in an Amendment		7	7	
Warnings:					
Information:					
5	Fee Worksheet (PTO-06)	fee-info.pdf	8458	no	2
			78a839297eabe8da8692d6832d4b4397f4f9134e		
Warnings:					
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Total Files Size (in bytes):			3365516		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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ATTORNEY'S DOCKET
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My residence, post office address and citizenship are as stated next to my name.

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Serial No _____

on _____

and was amended

on _____

☒ was filed as PCT international application

Number IB2006/051218

On 20 April 2006

and was amended under PCT Article 19

on _____ (if applicable).

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COUNTRY	APPLICATION NUMBER	DATE OF FILING DAY, MONTH, YEAR	PRIORITY CLAIMED UNDER 35 USC 119
EP	05103232.4	21 April 2005	YES

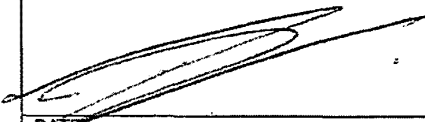
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page 1 of 2

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201	FULL NAME OF INVENTOR	FAMILY NAME DIELISSEN	FIRST GIVEN NAME John	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY WEERT	STATE OR FOREIGN COUNTRY The Netherlands	COUNTRY OF CITIZENSHIP The Netherlands
	POST OFFICE ADDRESS	POST OFFICE ADDRESS Buitenwiek 22	CITY WEERT	STATE & ZIP CODE/COUNTRY 6003 CS, The Netherlands
202	FULL NAME OF INVENTOR	FAMILY NAME RIJPKEMA	FIRST GIVEN NAME Edwin	SECOND GIVEN NAME
	RESIDENCE & CITIZENSHIP	CITY NIEUWERKERK A/D IJSSEL	STATE OR FOREIGN COUNTRY The Netherlands	COUNTRY OF CITIZENSHIP The Netherlands
	POST OFFICE ADDRESS	POST OFFICE ADDRESS Kleefkruid 4	CITY NIEUWERKERK A/D IJSSEL	STATE & ZIP CODE/COUNTRY 2914 BK, The Netherlands

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DATE 21 December 2006	DATE	

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NUMBER
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My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention the specification of which (check only one item below):

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☐ is attached hereto.

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and was amended

on

☒ was filed as PCT international application

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COUNTRY	APPLICATION NUMBER	DATE OF FILING DAY, MONTH, YEAR	PRIORITY CLAIMED UNDER 35 USC 119
EP	05103232.4	21 April 2005	YES

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Combined Declaration For Patent Application and Power of Attorney (Continued) (includes Reference to PCT International Applications)				Attorneys Docket Number PH000268 US	
POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (List name and registration number)					
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201	FULL NAME OF INVENTOR	FAMILY NAME DIELISSEN	FIRST GIVEN NAME John	SECOND GIVEN NAME	
	RESIDENCE & CITIZENSHIP	CITY WEERT	STATE OR FOREIGN COUNTRY The Netherlands	COUNTRY OF CITIZENSHIP The Netherlands	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS Buitenwiek 22	CITY WEERT	STATE & ZIP CODE/COUNTRY 6003 CS, The Netherlands	
202	FULL NAME OF INVENTOR	FAMILY NAME RIJPKEMA	FIRST GIVEN NAME Edwin	SECOND GIVEN NAME	
	RESIDENCE & CITIZENSHIP	CITY NIEUWERKERK A/D IJSSEL	STATE OR FOREIGN COUNTRY The Netherlands	COUNTRY OF CITIZENSHIP The Netherlands	
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DATE		DATE 21 December 2006			

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(July 1994)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
26 October 2006 (26.10.2006)

PCT

(10) International Publication Number
WO 2006/111931 A1

(51) International Patent Classification:
H04L 12/56 (2006.01)

(21) International Application Number:
PCT/IB2006/051218

(22) International Filing Date: 20 April 2006 (20.04.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
05103232.4 21 April 2005 (21.04.2005) EP

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(74) Agents: **WHITE, Andrew, G.** et al.; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill Surrey RH1 5HA (GB).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

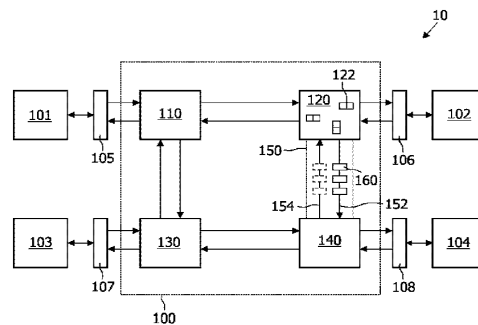
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD



(57) **Abstract:** An integrated circuit (10) comprises a plurality of functional blocks (101, 102, 103, 104) and a data communication network (100) comprising a plurality of network stations being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104). Each data package comprising N data elements including a data element comprising routing information for the network stations (110, 120, 130, 140), N being an integer of at least two. The plurality of network stations comprises a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces, each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108), the data communication network (100) comprising a first network station (140) and a second network station (120) interconnected through a first communication channel (150), the network comprising M*N data storage elements (160), M being a positive integer, for introducing a delay of M*N cycles on the first communication channel (150). An integrated circuit (10) comprises a plurality of functional blocks (101, 102, 103, 104) and a plurality of data routers (110, 120, 130, 140), each being coupled to a functional block (101, 102, 103, 104). The introduction of a delay of one or more data packages on a slow communication channel (150) facilitates an increase of the maximum clock speed of the data communication over the data communication network (100).

WO 2006/111931 A1

DESCRIPTION

**INTEGRATED CIRCUIT WITH DATA COMMUNICATION
NETWORK AND IC DESIGN METHOD**

The present invention relates to an integrated circuit having a plurality of functional blocks interconnected via a data communication network.

Nowadays, most integrated circuits (ICs) are very large scale integration (VLSI) circuits having a large number of features that typically implement a large number of functions on board the IC. The various functions may be located in discrete functional blocks, e.g. system on chip (SoC) architectures. The interconnect of the functional blocks poses a design challenge, because the high clock speeds of modern ICs facilitate the processing of large amounts of data, which means that the interconnect of the IC must be capable of communicating large amounts of data between the functional blocks.

To facilitate flexible communication on the one hand and to limit the amount of wires required on the other hand, ICs may incorporate a data communication network, also referred to as a network on chip (NoC). Such networks typically comprise a plurality of network stations, each associated with a functional block, interconnected via communication channels, e.g. wires. The plurality of network stations include a plurality of data routers and a plurality of network interfaces, each data router being coupled to a functional block via a network interface. The data can be communicated over the network in the form of packages that include a mixture of data and routing instructions for the network stations. In networks facilitating duplex communication, a pair of network stations is typically interconnected via at least a pair of communication subchannels to facilitate the two-way communication.

A problem associated with communication channels, e.g. wires, on ICs is that the clock speed at which the IC can operate may be determined by the slowest communication channel, i.e. the channel exhibiting the largest data

transfer delay. Several solutions for such a problem exist, see for instance Carloni et al.: Coping with latency in SoC design, IEEE Micro 5, Vol. 22, pages 24-35, IEEE 2002, in which a number of solutions are presented. A possible solution is to introduce a data storage element such as a latch into the slowest data communication channel. Consequently, the clock speed of the data communication part of the IC can be increased at the expense of an additional clock cycle for the communication along the slowest communication channel.

Unfortunately, such a solution cannot straightforwardly be applied to ICs communicating data between the functional blocks via an integrated network, especially when the nature of the communicated data differs per clock cycle; see E. Rijpkema et al.: Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip; IEE Proc.- Comput. Digit. Tech. 2003, page 1-9 (IEE proceedings online no. 20030830), for an example of such a network. Such a network operates on the principle that a network station such as a data router receives the routing data incorporated in the data packet during a predefined clock cycle. Delaying the communication to that router over a slow communication channel by a clock cycle to speed up the rest of the network would cause the routing data to arrive outside the predefined clock cycle, causing erroneous behaviour of the network.

The present invention seeks to improve the data communication speed of a network of an integrated circuit according to the opening paragraph.

According to an aspect of the invention, there is provided an integrated circuit a plurality of functional blocks and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, the data

communication network comprising a first network station and a second network station interconnected through a first communication channel, the network comprising $M \times N$ data storage elements, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel.

The invention is based on the realization that the correct operation of the network relies on the maintenance of the correct periodicity between the network stations. Because the data packages have a fixed size of N data elements, the communication of a complete package between two network stations takes N clock cycles, or N handshake driven data transfers in case of an asynchronous implementation of the network. The routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package, e.g. the first data element (i.e. a header), although other data elements may (also) contain such information. Since a network station expects routing information to arrive periodically (i.e. after every N cycles), the introduction of a delay on the first communication channel (which typically is the slowest channel of the network) matching such a period, i.e. by delaying the whole data package rather than a single data element, the delayed data package is received by the receiving network station during the appropriate period, e.g. clock cycle.

Each communication channel may comprise a first subchannel between an input port of a first associated network station and an output port of a second associated network station and a second subchannel between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations. The $M \times N$ data elements may be distributed over the subchannels of the first communication channel.

In a preferred embodiment, the first network station is arranged to evaluate the routing information in a first cycle and the second network station is arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles; and the first subchannel of the first communication channel exhibits a delay of A cycles implemented by A data storage elements and the second subchannel

exhibits a delay of B cycles implemented by B data storage elements, A and B being positive integers, with $A + B = M \cdot N$.

The introduction of a phase shift in the routing evaluation phase for a one of the network stations in the network has the advantage that the number of delay elements in a data communication (sub)channel can be smaller than the number of data elements in a data package, thus improving the latency of that particular data communication (sub)channel. The drawback is that all communication to the phase-shifted network station has to run via the delayed communication channel to introduce the appropriate phase shift. This limitation can be avoided, however, by ensuring that any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with $C \bmod N = A$; and any network path to the further network station from the first network station comprises D delay elements; B being a positive integer with $D \bmod N = B$. This maintains the correct phase relation between the first network station and any other network station that operate on a different router information evaluation phase than the first network station, thus maintaining the optimal flexibility in the network.

In an alternative embodiment, each subchannel of the first communication channel comprises a delay introduced by $\frac{1}{2} \cdot M \cdot N$ data storage elements, with $\frac{1}{2} \cdot M \cdot N$ typically corresponding to the size of a data package. Consequently, since both paths of the duplex communication channel are likely to have similar lengths and similar delay characteristics, the partitioning of both subchannels allows for the improvement of the speed of the network in both communication directions.

Preferably, $M=1$ in order to minimize the number of required delay elements, which will minimize the delay introduced on the first communication channel.

In a synchronous implementation, the IC further comprises a clock signal generator, the plurality of network stations and the $M \cdot N$ storage elements being responsive to the clock signal generator, to ensure that no

data conflicts can arise between the data routers and the $M*N$ storage elements.

Each network station may comprise a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port. Such an implementation allows for the interleaving of packages requiring different service levels, e.g. best effort and guaranteed bandwidth service levels.

According to a further aspect of the invention, there is provided a method of designing an integrated circuit comprising a plurality of functional blocks and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface; the method comprising identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and inserting $M*N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel. Such a method facilitates the design of an integrated circuit of the present invention.

In a preferred embodiment, each communication channel comprises a first subchannel between an input port of a first associated network station and an output port of a second associated network station and a second subchannel between an input port of the second associated network station and an output port of the first associated network station for enabling

duplex communication between the two associated network stations; and the first network station being arranged to evaluate the routing information in a first cycle and the second network station being arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles, the method further comprising inserting A data storage elements into the first subchannel of the first communication channel for introducing a delay of A cycles onto said first subchannel; and inserting B data storage elements into the second subchannel of the first communication channel for introducing a delay of B cycles onto said second subchannel; A and B being positive integers, with $A + B = M \cdot N$. Such a method facilitates the design of a preferred embodiment of the integrated circuit of the present invention.

The invention is described in more detail and by way of non-limiting examples with reference to the accompanying drawings, wherein:

Fig.1 shows an embodiment of an IC of the present invention;

Fig. 2 shows the timing behaviour along a delayed communication channel of said IC;

Fig. 3 shows another embodiment of an IC of the present invention;

Fig. 4 shows the timing behaviour along a delayed communication channel of said IC; and

Fig. 5 shows yet another embodiment of an IC of the present invention including its timing behaviour.

It should be understood that the Figures are merely schematic and are not drawn to scale. It should also be understood that the same reference numerals are used throughout the Figures to indicate the same or similar parts.

Fig. 1 shows an integrated circuit (IC) 10 according to an embodiment of the present invention. The IC 10 has four functional blocks 101-104, e.g. processing units, which are interconnected via a data communication network 100 including data routers 110, 120, 130, 140, which respectively are coupled

to the functional blocks 101-104 via respective network interfaces 105-108. The data routers 110, 120, 130, 140 and the network interfaces 105-108 comprise the network stations of the data communication network 100. Exemplary embodiments of such data routers and network interfaces can for instance be found in: "An efficient On-Chip Network Interface Offering Guaranteed Services, Shared Memory Abstraction and Flexible Network Configuration" by Radulescu et al.; Proceedings of Design, Automation and Test Conference in Europe, February 2004, and in E. Rijpkema et al.: Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip; IEE Proc.- Comput. Digit. Tech. 2003, page 1-9 (IEE proceedings online no. 20030830) as well as in the relevant references therein, the relevant passages thereof being incorporated by reference.

The network stations of the data communication network 100 are interconnected via a plurality of data communication channels 150. The communication channels 150 may comprise one or more wires, e.g. data buses. The data communication network 100 is configured to allow flexible communication of data streams between the functional blocks 101-104. Typically, such a data stream comprises one or more data packages, with each data package comprising N data elements, with N being an integer having a value of at least 2. At least one of the N data elements in a package, e.g. the first data element, comprises routing instructions for the destination network station. Such data packages are sometimes referred to as flow instruction units (flits).

The data streams may be communicated over the network 100 using known communication techniques such as store and forward routing, in which a complete data stream is stored in a data router before it is forwarded to its next destination, or wormhole routing, in which the data routers can send a stored data package to its next destination before the complete data stream has been received. The latter technique has the advantage that the data routers 110, 120, 130, 140 need less storage capacity but both techniques are equally feasible, and other techniques may be used as well.

The data network 100 shown in Fig.1 is a duplex network, i.e. it allows simultaneous data communication in two directions. It is emphasized, however, that the present application is equally applicable to simplex networks, i.e. networks that do not support simultaneous two-way communication. To facilitate the duplex communication over data network 100, each communication channel 150 comprises a first subchannel 152 and a second subchannel 154 between respective inputs and outputs of two neighbouring network stations, e.g. data routers 120 and 140. This facilitates time-division multiple access (TDMA) data communication, for instance of a guaranteed bandwidth and a best effort service. To this end, each network station in the data communication network 100 has a plurality of memories, each comprising a first memory element and a second memory element, e.g. memory 122 in data router 120, associated with a communication port, i.e. an input port or an output port of the data router, or more precisely, associated with a service level of a communication via that communication port. Obviously, the plurality of memories may be implemented as a single memory having enough storage to keep track of each input or output port of the network station, as will be explained below by means of a communication between two data routers by way of example only. It will be appreciated that the same teachings can be applied to communications between a data router and a network interface or to communications between a network interface and a functional block without departing from the teachings of the present invention.

Typically, the header of a first data package will comprise information about the destination of the data package as well as the service level of the data package, e.g. guaranteed bandwidth or best effort service. The service level will be flagged by setting a bit in the appropriate memory element of the destination output port of the data router. For subsequent data packages having the same service level, the data router will know that these data packages belong to a data stream in progress because the appropriate bit has been stored in the associated memory element. The last data package of the data stream contains an indicator causing the data router to reset said bit.

Such a mechanism allows interleaving of data packages of two data streams over a single communication channel.

In Fig. 1, the communication channel 150 between data routers 120 and 140 has been identified as the communication channel in the network 100 exhibiting a data transfer delay exceeding a predetermined delay threshold. Such an identification can be made at the IC design stage by subjecting the design to a simulation of the delay behaviour of the IC 10 using available timing behaviour simulation tools. To avoid having to limit the communication speed, e.g. the clock speed, of the data communication network 100 in accordance with the delay characteristics of the communication channel 150 between two network stations, e.g. data routers 120 and 140, this communication channel (which will be referred to as the slow communication channel 150) is equipped with $M \times N$ data storage elements to introduce a delay of $M \times N$ cycles onto the communication channel, with N corresponding to the size of a data package, thus allowing an increase of the maximum communication frequency of the data network 100 at the expense of the introduction of a delay of a single data package, i.e. the number of clock cycles it takes to communicate such a data package, on the slow communication channel 150.

The network 100 shown in Fig. 1 is arranged to communicate data packages with size $N=3$. Other values of N are equally feasible. The first subchannel 152 of the slow communication channel 150 is extended with $N=3$ data storage elements 160. Optionally, the second subchannel 154 of the slow communication channel 150 is also extended with $N=3$ data storage elements 160, in which case $M=2$. Since the first subchannel 152 and the second subchannel 154 typically will be in each others vicinity, their respective delay characteristics typically will be similar, thus requiring the introduction of data storage elements 160 on both subchannels. However, in cases where the respective subchannels exhibit different delay characteristics, for instance because the subchannels have different lengths or because of the nature of the timing techniques used, e.g. waterfall clocking, the introduction of N data

elements 160 on only one of the subchannels can be sufficient, in which case $M=1$.

It will be appreciated that the physical placement of the data storage elements 160 on the subchannels 152 and 154 is by way of example only; an implementation where the data storage elements 160 are integrated in the associated network stations, e.g. data router 120 or data router 140 is equally feasible. It will be appreciated that the same teachings can be applied to communications between a data router and a network interface or to communications between a network interface and a functional block without departing from the teachings of the present invention. The same applies to the other embodiments of the data communication network 100, e.g. the embodiments shown in Fig. 3 and 5. The data storage elements 160 may be a pipeline or a buffer of latches or flipflops, and may be implemented using synchronous or asynchronous storage elements. In Fig.1, the data storage elements 160 are responsive to the same clock signal (not shown) as the network stations including data routers 110, 120, 130, 140 and network interfaces 105-108.

Fig. 2 shows the timing behaviour of the communication along the slow channel 150 extended with 3 data storage elements 160 on the first subchannel 152 interconnecting an output port of data router 120 with an input port of the data router 140. At clock cycle t , the data router 120 employing wormhole routing receives the first data element h of a data package (indicated by the bold box) having a size of 3 data elements. The subsequent data elements $d1$ and $d2$ of this data package are received by the data router 120 at respective clock cycles $t+1$ and $t+2$. The data routers 110, 120, 130, 140 are all configured to periodically evaluate the content of a received data package, that is after every N clock cycles for a data package having a size N data elements. In the embodiment of the IC 10 shown in Fig. 1, all the data routers 110, 120, 130, 140 perform this operation simultaneously, i.e. at the same clock cycle, which is clock cycle t plus every N th clock cycle afterwards, i.e. at $t+3$, $t+6$ and so on, at which the arrival of a header h of a new data package is expected. Such a periodical checking mechanism by a data router

may for instance be implemented using modulo N counters. Consequently, it is essential that the headers of the data packages do not arrive at any data router 110, 120, 130, 140 outside such an evaluation clock cycle.

In line with the principle of wormhole routing, data router 120 starts sending the data package upon its complete receipt, i.e. at clock cycle $t+3$ via the first subchannel 152 of the slow communication channel 150. At this point, it is emphasized that data elements sent via a non-delayed communication channel will arrive at the destination data router in the same clock cycle as they were sent. However, due to the presence of $N=3$ data storage elements 160 in the first subchannel 152 of the slow communication channel 150, the first data storage element 160 receives the header h at $t+3$, passes it on to the second data storage element 160 at $t+4$, which passes it on to the third data storage element 160 at $t+5$, which finally passes it on to the data router 160 at $t+6$, which is in phase with the header evaluation cycle of the data routers 110, 120, 130, 140 in the data network 150. This ensures the correct routing of the data package by the data router 140.

In the embodiment of IC 10 according to the present invention as shown Fig. 3, the data router 140 is configured to evaluate the header of a data package A clock cycles later (or B cycles earlier) than the other data routers 110, 120, 130 in the data network 100, with N corresponding to the number of data elements in a data package and A, B being positive integers with $A+B = M*N$. Typically, A modulo N and B modulo N are not equal to zero.

In Fig. 3, $M = 1$, $N = 3$, $A = 1$ and $B = 2$ by way of example only. In other words, the data router 140 has a phase-shifted routing information evaluation cycle compared to the other data routers in the data network 100. To ensure that the routing information is correctly interpreted, i.e. to ensure that this information arrives at any data router during its appropriate clock cycle, two possible implementations can be chosen. In a first implementation, all communication to and from the phase-shifted data router 140 is routed through the slow communication channel 150. Consequently, only the slow communication channel 150 requires the introduction of $M*N$ data storage elements over its subchannels 152 and 154. The drawback of this

implementation is that the flexibility of the data communication network 100 is reduced.

In the preferred implementation, any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with $C \bmod N = A$, and any network path to the further network station from the first network station comprises D delay elements; B being a positive integer with $D \bmod N = B$. This ensures that the correct phase relation between clock cycle and routing information evaluation is maintained throughout the whole data communication network 100. For instance, in Fig. 3, $C = A$ and $B = D$, with C data elements 160 being introduced in the subchannel 152 between the output port of data router 130 and the input port of data router 140 and with D data elements 160 being introduced in the subchannel 154 between the input port of data router 130 and the output port of data router 140.

In other words, every communication channel 150 between two network stations exhibiting a phase-shifted routing information cycle with respect to each other should incorporate the appropriate number of data storage elements 160 to implement the number of cycles to which the phase shift corresponds. In Fig. 3, this means that all subchannels connected to an input port of the data router 140 are extended with A data storage elements 160 to introduce a delay of A cycles on the communication directed towards the data router 140, and all subchannels connected to an output port of the data router 140 are extended with B data storage elements 160 to introduce a delay of B cycles on the communication originating from the data router 140. Since $A+B = M*N$, each communication channel 150 to which data router 140 is connected incorporates $M*N$ data storage elements 160, thus ensuring the introduction of a delay of exactly M data packages on a communication loop between two neighbouring data routers.

This is explained in more detail in Fig. 4, where a data package consisting of data elements h , $d1$ and $d2$ is sent from data router 120 to data router 140 and back again in the network of IC 10 as shown in Fig. 3. The

routing information evaluation clock cycles for data routers 120 and 140 are indicated by bold vertical lines at the beginning of such a cycle. In other words, data router 120 evaluates the routing information of received data packages at t , $t+3$, $t+6$ and so on, whereas data router 140 evaluates the routing information of received data packages at $t+1$, $t+4$, $t+7$ and so on. Data router 120 sends data element h at $T=t$ to data router 140. At $T=t$, data element h is received by data storage element 160 in the first subchannel 152, which stores the data element h and sends it to the data router 140 at $T = t+1$, which receives the data element h during the same clock cycle and evaluates the routing information comprised in header h .

After the data router 140 has received data element $d1$ at $T = t+2$ and data element $d2$ and $T = t+3$, i.e., after the data router 140 has received the complete data package, the data router 140 sends the first data element of the data package to the data router 140 via the second subchannel 154. Due to the presence of two data storage elements 160 on the second subchannel 154, the first data element h is received by the data router 120 at $T = t+6$, i.e. during a cycle at which the data router 120 is scheduled to evaluate the routing information, with the other two data elements $d1$ and $d2$ respectively arriving at the subsequent cycles $t+7$ and $t+8$. It will be recognized that the data storage elements 160 in the subchannels 152 and 154 operate as phase shifters to ensure that routing information is evaluated at the right time in each data router phase domain. The application of phase shifting techniques has the advantage that the delay introduced on the individual subchannels 152, 154 can be less than a full data package, thus improving the performance of the slow communication channel 150 compared to the solution presented in Fig. 1.

At this point, it will be appreciated that the number of different phase domains can be further extended without departing from the teachings of the present invention. It is reiterated that although the exemplary implementations of the data storage elements is given on a communication channel between two data routers, implementations on channels between other types of network stations, e.g. between a data router and a network interface, are equally feasible.

Fig. 5 shows an asynchronous implementation of a delayed duplex communication channel 150 between two network stations, e.g. data routers 120 and 140, which is robust against clock skew. The data routers 120 and 140 are triggered by clock signal CLK. However, due to the fact that the clock signal has to travel over a longer wire to data router 140 than to data router 120, data router 140 receives a delayed clock signal CLK_d, with a delay of t_1 with respect to the clock signal CLK received by data router 120. In completely synchronous data communication networks 100, this can cause communication errors, because a data package sent by data router 140 at clock cycle t to data router 120 or the first delay element 160 over a slow communication channel 150 between the data routers 120 and 140 may arrive at its destination at cycle $t+1$ rather than at cycle t . As previously explained, this will cause the routing information to arrive at the data router 120 outside its routing information evaluation cycle, which will likely cause the loss of the information due to a routing error.

This risk can be reduced by implementing the $M*N$ data storage elements 160 as asynchronous FIFO buffers 520 and 540 on the first subchannel 152 and the second subchannel 154 respectively between data routers 120 and 140. This implementation is insensitive to clock skew, at least within certain limits. To improve the robustness against clock skew of the asynchronous FIFO buffers 520 and 540, the buffers may include slightly more than the $M*N$ data storage elements, as will be explained in more detail below.

The asynchronous FIFO buffers 520 and 540 have communication behaviour independent of the clock CLK; the data is rippled through the FIFO buffers 520 and 540 based on handshake protocols. Such behaviour is usually quicker than synchronous communication because the latter is dominated by the slowest path in the synchronous communication network, as previously explained.

A communication of a data package from data router 120 to FIFO buffer 520 is initiated by a handshake validation signal 501 followed by synchronous data communication 502 of the data elements of a data package having size N ; this communication is governed by data router 120, which is responsive to

clock signal CLK. The data elements take a time period t_2 to ripple through FIFO buffer 520, after which a handshake request 503 is sent to the data router 140. The receipt of an initial handshake request initializes data router 140 and triggers the data router 140 to accept the data communication by sending an acknowledge signal 504 to the FIFO buffer 520, which triggers the data communication 505. The data router 140 will remain initialized until the data stream of data packages has been received completely. The data package receipt periods of data routers 120 and 140 are indicated by the bold horizontal lines over the clock signals clk and clk_d respectively. The data router 140 receives the data communication synchronously and sends the data package synchronously, i.e. one data element per clock cycle, to FIFO buffer 540 N clock cycles after receiving the request signal 503, in accordance with a wormhole routing approach, by sending a handshake validation signal 506 and data communication 507 to the FIFO buffer 540. After a period t_3 , i.e. the time it takes the data elements to ripple through the FIFO buffer 540, the FIFO buffer 540 sends a handshake request signal 508 to data router 120.

Crucially, because data router 120 has already been initialized, i.e. it is already engaged in communicating a data stream to data router 140, data router 120 will only send an acknowledge signal 509 to such a handshake request to enable communication 510 at the beginning of a routing information evaluation cycle of data router 120, as indicated by the vertical dashed line. Alternatively, if the transmission of the data stream from data router 120 to data router 140 had completed prior to the handshake request 508 from FIFO buffer 540 to data router 120, this request would initialize the data router 120. In both cases, the receipt of the routing information in the correct timeslot of data router 120 is ensured despite the clock skew on the clock signal triggering the data routers 120 and 140. In case the clock skew between data router 120 and data router 140 is substantial, the data router 140 may send a first data element of a next data package to the FIFO buffer 540 before this buffer has received the acknowledge signal 509. In such a scenario, the FIFO buffer 509 must be capable of storing more than $M \cdot N$ data elements to avoid the loss of data stored in the FIFO buffer 509. This can be realized by adding

one or more data storage elements to the $M*N$ data storage elements as overwrite protection.

An IC 10 comprising a data communication network 100 according to the present invention can be designed using an IC design method modified as follows. After designing a first version of the IC 10, which can be done using well-known IC design tools, and which will not be further explained for that reason, an evaluation step is performed in which a first communication channel between a network station and a second network station having a data transfer delay exceeding a predefined delay threshold is identified. Consequently, the design of the data communication network 100 is modified according to the teachings of the present invention by inserting $M*N$ data storage elements into the network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel. This allows for an increase of the maximum clock speed at which the data communication network 100 can operate.

The insertion step may comprise inserting A data storage elements into the first subchannel (152) of the first communication channel (150) for introducing a delay of A cycles onto said first subchannel and inserting B data storage elements into the second subchannel (154) of the first communication channel (150) for introducing a delay of B cycles onto said second subchannel with A and B being positive integers and with $A + B = M*N$ to create a phase-shifted data communication network 100 as outlined in Fig. 3 and 4 and their detailed description.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements. In

the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS

1. An integrated circuit (10) comprising:
 - a plurality of functional blocks (101, 102, 103, 104); and
 - a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108), the data communication network (100) comprising a first network station (140) and a second network station (120) interconnected through a first communication channel (150), the network comprising M*N data storage elements (160), M being a positive integer, for introducing a delay of M*N cycles on the first communication channel (150).
2. An integrated circuit (10) as claimed in Claim 1, wherein each communication channel (150) comprises:
 - a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station; and
 - a second subchannel (154) between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations.
3. An integrated circuit (10) as claimed in Claim 2, wherein the M*N data elements (160) are distributed over the first subchannel (152) and the second subchannel (154) of the first communication channel (150).

4. An integrated circuit as claimed in claim 3, wherein:
the first network station is arranged to evaluate the routing information in a first cycle and the second network station is arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles; and
the first subchannel (152) of the first communication channel (150) exhibits a delay of A cycles implemented by A data storage elements (160) and the second subchannel (154) exhibits a delay of B cycles implemented by B data storage elements (160), A and B being positive integers, with $A + B = M \cdot N$.
5. An integrated circuit as claimed in claim 4, wherein any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with $C \text{ modulo } N = A$; and any network path to the further network station from the first network station comprises D delay elements; D being a positive integer with $D \text{ modulo } N = B$.
6. An integrated circuit (10) as claimed in Claim 1-5, wherein $M = 1$.
7. An integrated circuit (10) as claimed in Claim 3, wherein the first subchannel (152) and the second subchannel (154) of the first communication channel (150) each comprise a delay introduced by $\frac{1}{2} \cdot M \cdot N$ data storage elements (160).
8. An integrated circuit (10) as claimed in Claim 1 or 2, further comprising a clock signal generator, the plurality of network stations (110, 120, 130, 140) and the $M \cdot N$ storage elements (160) being responsive to the clock signal generator.

9. An integrated circuit (10) as claimed in claim 1 or 2, wherein each network station (110, 120, 130, 140) comprises a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port.

10. A method of designing an integrated circuit (10) comprising a plurality of functional blocks (101, 102, 103, 104), and a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface; the method comprising:

identifying a first communication channel (150) between a first network station (140) and a second network station (120) that has a data transfer delay exceeding a predefined delay threshold; and

inserting $M \times N$ data storage elements (160) into the data communication network (100), M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel (150).

11. A method as claimed in Claim 10, wherein each communication channel (150) comprises a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station and a second subchannel (154) between an input port of the

second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations; and

the first network station being arranged to evaluate the routing information in a first cycle and the second network station being arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles, the method further comprising:

inserting A data storage elements into the first subchannel (152) of the first communication channel (150) for introducing a delay of A cycles onto said first subchannel; and

inserting B data storage elements into the second subchannel (154) of the first communication channel (150) for introducing a delay of B cycles onto said second subchannel; A and B being positive integers, with $A + B = M \cdot N$.

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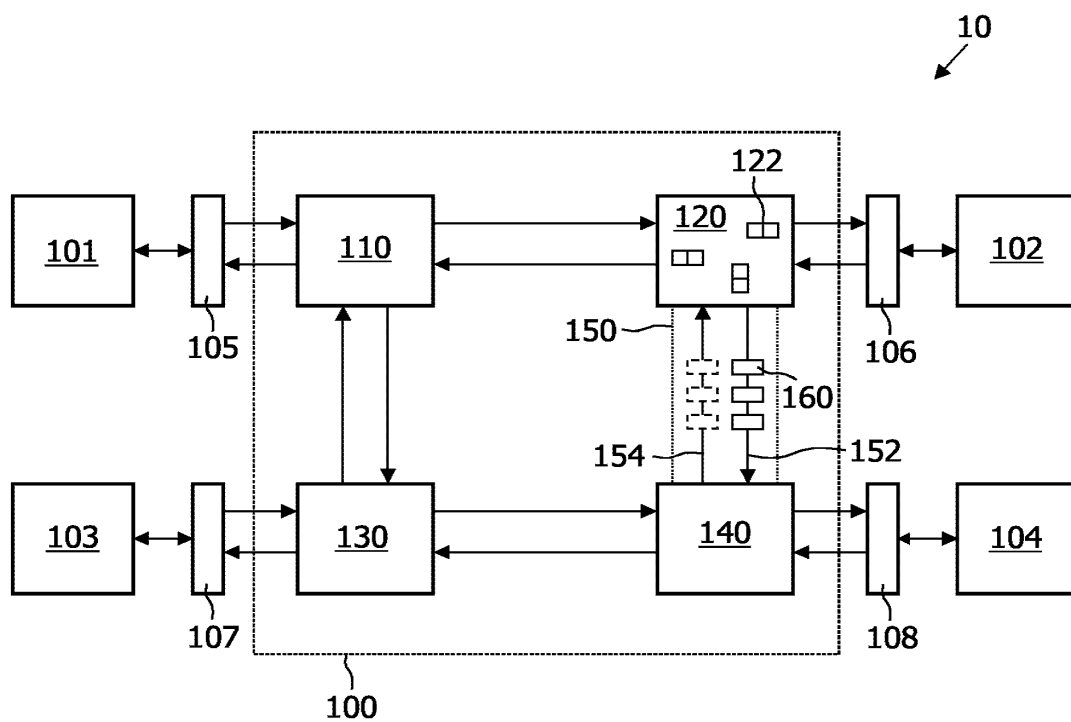


FIG. 1

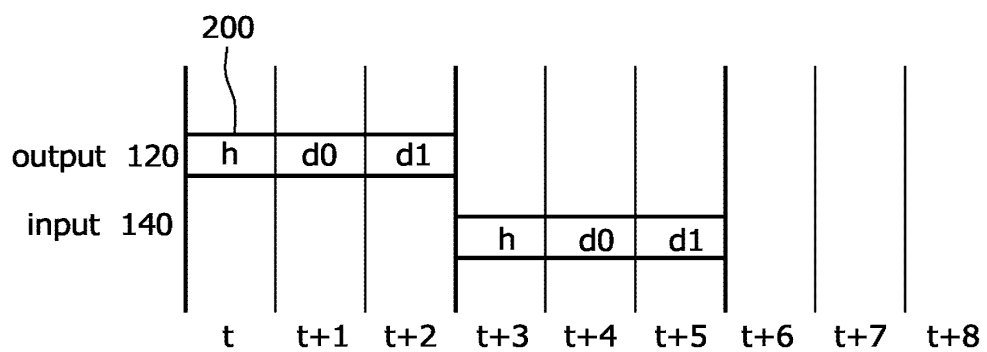


FIG. 2

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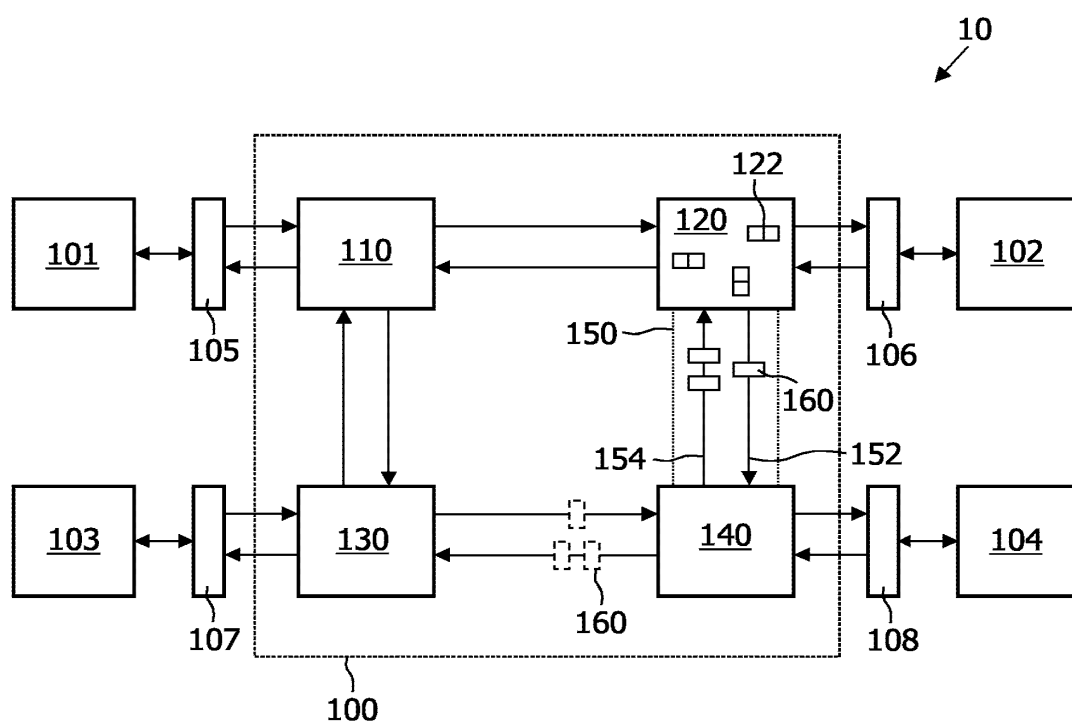


FIG. 3

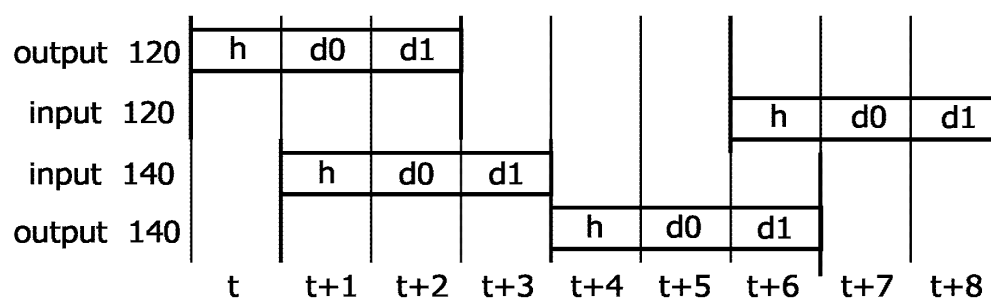


FIG. 4

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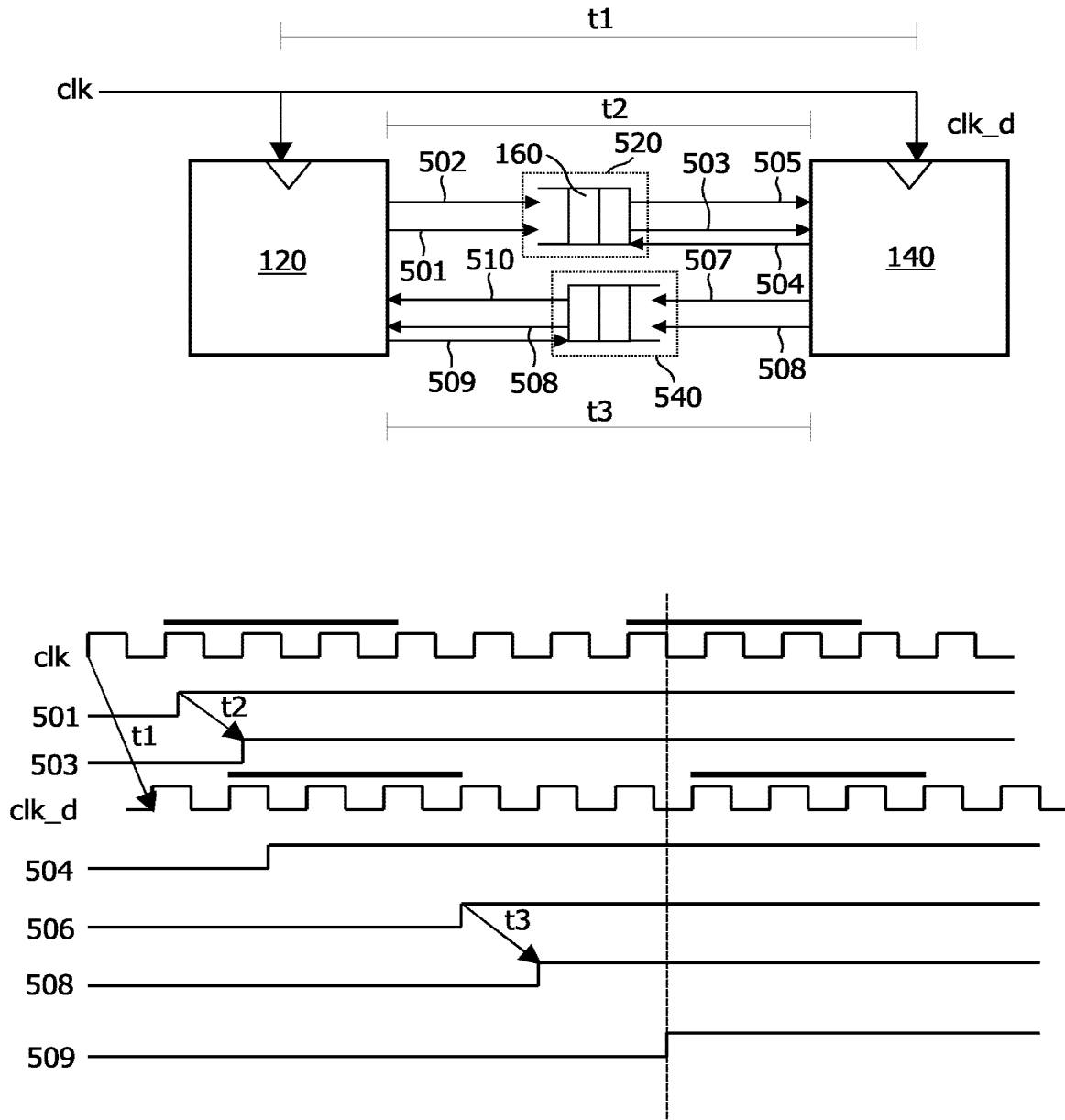


FIG. 5

Document made available under the Patent Cooperation Treaty (PCT)

International application number: PCT/IB2006/051218

International filing date: 20 April 2006 (20.04.2006)

Document type: Certified copy of priority document

Document details: Country/Office: EP
Number: 05103232.4
Filing date: 21 April 2005 (21.04.2005)

Date of receipt at the International Bureau: 12 May 2006 (12.05.2006)

Remark: Priority document submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b)



World Intellectual Property Organization (WIPO) - Geneva, Switzerland
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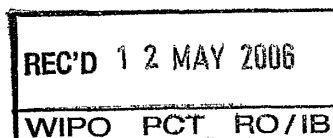
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Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

05103232.4



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Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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Anmeldung Nr:
Application no.: 05103232.4
Demande no:

Anmeldetag:
Date of filing: 21.04.05
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
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Integrated Circuit with Data Communication Network and IC Design Method

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s)
revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

H04L12/00

Am Anmeldetag benannte Vertragsstaaten/Contracting states designated at date of
filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LT LU
MC NL PL PT RO SE SI SK TR LI

DESCRIPTION

INTEGRATED CIRCUIT WITH DATA COMMUNICATION
NETWORK AND IC DESIGN METHOD

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The present invention relates to an integrated circuit having a plurality of functional blocks interconnected via a data communication network.

10 Nowadays, most integrated circuits (ICs) are very large scale integration (VLSI) circuits having a large number of features that typically implement a large number of functions on board the IC. The various functions may be located in discrete functional blocks, e.g. system on chip (SoC) architectures. The interconnect of the functional blocks poses a design challenge, because
15 the high clock speeds of modern ICs facilitate the processing of large amounts of data, which means that the interconnect of the IC must be capable of communicating large amounts of data between the functional blocks.

 To facilitate flexible communication on the one hand and to limit the amount of wires required on the other hand, ICs may incorporate a data
20 communication network, also referred to as a network on chip (NoC). Such networks typically comprise a plurality of network stations, each associated with a functional block, interconnected via communication channels, e.g. wires. The plurality of network stations include a plurality of data routers and a plurality of network interfaces, each data router being coupled to a functional
25 block via a network interface. The data can be communicated over the network in the form of packages that include a mixture of data and routing instructions for the network stations. In networks facilitating duplex communication, a pair of network stations is typically interconnected via at least a pair of communication subchannels to facilitate the two-way communication.

30 A problem associated with communication channels, e.g. wires, on ICs is that the clock speed at which the IC can operate may be determined by the slowest communication channel, i.e. the channel exhibiting the largest data

transfer delay. Several solutions for such a problem exist, see for instance Carloni et al.: Coping with latency in SoC design, IEEE Micro 5, Vol. 22, pages 24-35, IEEE 2002, in which a number of solutions are presented. A possible solution is to introduce a data storage element such as a latch into the slowest
5 data communication channel. Consequently, the clock speed of the data communication part of the IC can be increased at the expense of an additional clock cycle for the communication along the slowest communication channel.

Unfortunately, such a solution cannot straightforwardly be applied to ICs communicating data between the functional blocks via an integrated network, especially when the nature of the communicated data differs per clock cycle;
10 see E. Rijpkema et al.: Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip; IEE Proc.- Comput. Digit. Tech. 2003, page 1-9 (IEE proceedings online no. 20030830), for an example of such a network. Such a network operates on the principle that a
15 network station such as a data router receives the routing data incorporated in the data packet during a predefined clock cycle. Delaying the communication to that router over a slow communication channel by a clock cycle to speed up the rest of the network would cause the routing data to arrive outside the predefined clock cycle, causing erroneous behaviour of the network.

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The present invention seeks to improve the data communication speed of a network of an integrated circuit according to the opening paragraph.

According to an aspect of the invention, there is provided an integrated
25 circuit a plurality of functional blocks and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being
30 an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, the data

communication network comprising a first network station and a second network station interconnected through a first communication channel, the network comprising $M \times N$ data storage elements, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel.

5 The invention is based on the realization that the correct operation of the network relies on the maintenance of the correct periodicity between the network stations. Because the data packages have a fixed size of N data elements, the communication of a complete package between two network stations takes N clock cycles, or N handshake driven data transfers in case of
10 an asynchronous implementation of the network. The routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package, e.g. the first data element (i.e. a header), although other data elements may (also) contain such information. Since a network station expects routing information to arrive
15 periodically (i.e. after every N cycles), the introduction of a delay on the first communication channel (which typically is the slowest channel of the network) matching such a period, i.e. by delaying the whole data package rather than a single data element, the delayed data package is received by the receiving network station during the appropriate period, e.g. clock cycle.

20 Each communication channel may comprise first subchannel between an input port of a first associated network station and an output port of a second associated network station and a second subchannel between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the
25 two associated network stations. The $M \times N$ data elements may be distributed over the subchannels of the first communication channel.

 In a preferred embodiment, the first network station is arranged to evaluate the routing information in a first cycle and the second network station is arranged to evaluate the routing information in a second cycle, the
30 difference between the first cycle and the second cycle being A cycles; and the first subchannel of the first communication channel exhibits a delay of A cycles implemented by A data storage elements and the second subchannel

exhibits a delay of B cycles implemented by B data storage elements, A and B being positive integers, with $A + B = M*N$.

The introduction of a phase shift in the routing evaluation phase for a one of the network stations in the network has the advantage that the number of delay elements in a data communication (sub)channel can be smaller than the number of data elements in a data package, thus improving the latency of that particular data communication (sub)channel. The drawback is that all communication to the phase-shifted network station has to run via the delayed communication channel to introduce the appropriate phase shift. This limitation can be avoided, however, by ensuring that any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with C modulo N = A; and any network path to the further network station from the first network station comprises D delay elements; B being a positive integer with D modulo N = B. This maintains the correct phase relation between the first network station and any other network station that operate on a different router information evaluation phase than the first network station, thus maintaining the optimal flexibility in the network.

In an alternative embodiment, each subchannel of the first communication channel comprises a delay introduced by $\frac{1}{2}*M*N$ data storage elements, with $\frac{1}{2}*M*N$ typically corresponding to the size of a data package. Consequently, since both paths of the duplex communication channel are likely to have similar lengths and similar delay characteristics, the partitioning of both subchannels allows for the improvement of the speed of the network in both communication directions.

Preferably, $M=1$ in order to minimize the number of required delay elements, which will minimize the delay introduced on the first communication channel.

In a synchronous implementation, the IC further comprises a clock signal generator, the plurality of network stations and the $M*N$ storage elements being responsive to the clock signal generator, to ensure that no

data conflicts can arise between the data routers and the M*N storage elements.

Each network station may comprise a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port. Such an implementation allows for the interleaving of packages requiring different service levels, e.g. best effort and guaranteed bandwidth service levels.

According to a further aspect of the invention, there is provided a method of designing an integrated circuit comprising a plurality of functional blocks and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface; the method comprising identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and inserting M*N data storage elements into the data communication network, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel. Such a method facilitates the design of an integrated circuit of the present invention.

In a preferred embodiment, each communication channel comprises a first subchannel between an input port of a first associated network station and an output port of a second associated network station and a second subchannel between an input port of the second associated network station and an output port of the first associated network station for enabling

duplex communication between the two associated network stations; and the first network station being arranged to evaluate the routing information in a first cycle and the second network station being arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles, the method further comprising inserting A data storage elements into the first subchannel of the first communication channel for introducing a delay of A cycles onto said first subchannel; and inserting B data storage elements into the second subchannel of the first communication channel for introducing a delay of B cycles onto said second subchannel; A and B being positive integers, with $A + B = M \cdot N$. Such a method facilitates the design of a preferred embodiment of the integrated circuit of the present invention.

The invention is described in more detail and by way of non-limiting examples with reference to the accompanying drawings, wherein:

Fig.1 shows an embodiment of an IC of the present invention;

Fig. 2 shows the timing behaviour along a delayed communication channel of said IC;

Fig. 3 shows another embodiment of an IC of the present invention;

Fig. 4 shows the timing behaviour along a delayed communication channel of said IC; and

Fig. 5 shows yet another embodiment of an IC of the present invention including its timing behaviour.

It should be understood that the Figures are merely schematic and are not drawn to scale. It should also be understood that the same reference numerals are used throughout the Figures to indicate the same or similar parts.

Fig. 1 shows an integrated circuit (IC) 10 according to an embodiment of the present invention. The IC 10 has four functional blocks 101-104, e.g. processing units, which are interconnected via a data communication network 100 including data routers 110, 120, 130, 140, which respectively are coupled

to the functional blocks 101-104 via respective network interfaces 105-108. The data routers 110, 120, 130, 140 and the network interfaces 105-108 comprise the network stations of the data communication network 100. Exemplary embodiments of such data routers and network interfaces can for instance be found in: "An efficient On-Chip Network Interface Offering Guaranteed Services, Shared Memory Abstraction and Flexible Network Configuration" by Radulescu et al.; Proceedings of Design, Automation and Test Conference in Europe, February 2004, and in E. Rijpkema et al.: Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip; IEE Proc.- Comput. Digit. Tech. 2003, page 1-9 (IEE proceedings online no. 20030830) as well as in the relevant references therein, the relevant passages thereof being incorporated by reference.

The network stations of the data communication network 100 are interconnected via a plurality of data communication channels 150. The communication channels 150 may comprise one or more wires, e.g. data buses. The data communication network 100 is configured to allow flexible communication of data streams between the functional blocks 101-104. Typically, such a data stream comprises one or more data packages, with each data package comprising N data elements, with N being an integer having a value of at least 2. At least one of the N data elements in a package, e.g. the first data element, comprises routing instructions for the destination network station. Such data packages are sometimes referred to as flow instruction units (flits).

The data streams may be communicated over the network 100 using known communication techniques such as store and forward routing, in which a complete data stream is stored in a data router before it is forwarded to its next destination, or wormhole routing, in which the data routers can send a stored data package to its next destination before the complete data stream has been received. The latter technique has the advantage that the data routers 110, 120, 130, 140 need less storage capacity but both techniques are equally feasible, and other techniques may be used as well.

The data network 100 shown in Fig.1 is a duplex network, i.e. it allows simultaneous data communication in two directions. It is emphasized, however, that the present application is equally applicable to simplex networks, i.e. networks that do not support simultaneous two-way communication. To facilitate the duplex communication over data network 100, each communication channel 150 comprises a first subchannel 152 and a second subchannel 154 between respective inputs and outputs of two neighbouring network stations, e.g. data routers 120 and 140. This facilitates time-division multiple access (TDMA) data communication, for instance of a guaranteed bandwidth and a best effort service. To this end, each network station in the data communication network 100 has a plurality of memories, each comprising a first memory element and a second memory element, e.g. memory 122 in data router 120, associated with a communication port, i.e. an input port or an output port of the data router, or more precisely, associated with a service level of a communication via that communication port. Obviously, the plurality of memories may be implemented as a single memory having enough storage to keep track of each input or output port of the network station, as will be explained below by means of a communication between two data routers by way of example only. It will be appreciated that the same teachings can be applied to communications between a data router and a network interface or to communications between a network interface and a functional block without departing from the teachings of the present invention.

Typically, the header of a first data package will comprise information about the destination of the data package as well as the service level of the data package, e.g. guaranteed bandwidth or best effort service. The service level will be flagged by setting a bit in the appropriate memory element of the destination output port of the data router. For subsequent data packages having the same service level, the data router will know that these data packages belong to a data stream in progress because the appropriate bit has been stored in the associated memory element. The last data package of the data stream contains an indicator causing the data router to reset said bit.

Such a mechanism allows interleaving of data packages of two data streams over a single communication channel.

In Fig. 1, the communication channel 150 between data routers 120 and 140 has been identified as the communication channel in the network 100 exhibiting a data transfer delay exceeding a predetermined delay threshold. Such an identification can be made at the IC design stage by subjecting the design to a simulation of the delay behaviour of the IC 10 using available timing behaviour simulation tools. To avoid having to limit the communication speed, e.g. the clock speed, of the data communication network 100 in accordance with the delay characteristics of the communication channel 150 between two network stations, e.g. data routers 120 and 140, this communication channel (which will be referred to as the slow communication channel 150) is equipped with $M \times N$ data storage elements to introduce a delay of $M \times N$ cycles onto the communication channel, with N corresponding to the size of a data package, thus allowing an increase of the maximum communication frequency of the data network 100 at the expense of the introduction of a delay of a single data package, i.e. the number of clock cycles it takes to communicate such a data package, on the slow communication channel 150.

The network 100 shown in Fig. 1 is arranged to communicate data packages with size $N=3$. Other values of N are equally feasible. The first subchannel 152 of the slow communication channel 150 is extended with $N=3$ data storage elements 160. Optionally, the second subchannel 154 of the slow communication channel 150 is also extended with $N=3$ data storage elements 160, in which case $M=2$. Since the first subchannel 152 and the second subchannel 154 typically will be in each others vicinity, their respective delay characteristics typically will be similar, thus requiring the introduction of data storage elements 160 on both subchannels. However, in cases where the respective subchannels exhibit different delay characteristics, for instance because the subchannels have different lengths or because of the nature of the timing techniques used, e.g. waterfall clocking, the introduction of N data

elements 160 on only one of the subchannels can be sufficient, in which case $M=1$.

It will be appreciated that the physical placement of the data storage elements 160 on the subchannels 152 and 154 is by way of example only; an implementation where the data storage elements 160 are integrated in the associated network stations, e.g. data router 120 or data router 140 is equally feasible. It will be appreciated that the same teachings can be applied to communications between a data router and a network interface or to communications between a network interface and a functional block without departing from the teachings of the present invention. The same applies to the other embodiments of the data communication network 100, e.g. the embodiments shown in Fig. 3 and 5. The data storage elements 160 may be a pipeline or a buffer of latches or flipflops, and may be implemented using synchronous or asynchronous storage elements. In Fig.1, the data storage elements 160 are responsive to the same clock signal (not shown) as the network stations including data routers 110, 120, 130, 140 and network interfaces 105-108.

Fig. 2 shows the timing behaviour of the communication along the slow channel 150 extended with 3 data storage elements 160 on the first subchannel 152 interconnecting an output port of data router 120 with an input port of the data router 140. At clock cycle t , the data router 120 employing wormhole routing receives the first data element h of a data package (indicated by the bold box) having a size of 3 data elements. The subsequent data elements $d1$ and $d2$ of this data package are received by the data router 120 at respective clock cycles $t+1$ and $t+2$. The data routers 110, 120, 130, 140 are all configured to periodically evaluate the content of a received data package, that is after every N clock cycles for a data package having a size N data elements. In the embodiment of the IC 10 shown in Fig. 1, all the data routers 110, 120, 130, 140 perform this operation simultaneously, i.e. at the same clock cycle, which is clock cycle t plus every N th clock cycle afterwards, i.e. at $t+3$, $t+6$ and so on, at which the arrival of a header h of a new data package is expected. Such a periodical checking mechanism by a data router

may for instance be implemented using modulo N counters. Consequently, it is essential that the headers of the data packages do not arrive at any data router 110, 120, 130, 140 outside such an evaluation clock cycle.

In line with the principle of wormhole routing, data router 120 starts
5 sending the data package upon its complete receipt, i.e. at clock cycle $t+3$ via the first subchannel 152 of the slow communication channel 150. At this point, it is emphasized that data elements sent via a non-delayed communication channel will arrive at the destination data router in the same clock cycle as they were sent. However, due to the presence of $N=3$ data storage elements
10 160 in the first subchannel 152 of the slow communication channel 150, the first data storage element 160 receives the header h at $t+3$, passes it on to the second data storage element 160 at $t+4$, which passes it on to the third data storage element 160 at $t+5$, which finally passes it on to the data router 160 at $t+6$, which is in phase with the header evaluation cycle of the data routers 110,
15 120, 130, 140 in the data network 150. This ensures the correct routing of the data package by the data router 140.

In the embodiment of IC 10 according to the present invention as shown Fig. 3, the data router 140 is configured to evaluate the header of a data package A clock cycles later (or B cycles earlier) than the other data routers
20 110, 120, 130 in the data network 100, with N corresponding to the number of data elements in a data package and A, B being positive integers with $A+B = M*N$. Typically, $A \bmod N$ and $B \bmod N$ are not equal to zero.

In Fig. 3, $M = 1$, $N = 3$, $A = 1$ and $B = 2$ by way of example only. In other words, the data router 140 has a phase-shifted routing information evaluation
25 cycle compared to the other data routers in the data network 100. To ensure that the routing information is correctly interpreted, i.e. to ensure that this information arrives at any data router during its appropriate clock cycle, two possible implementations can be chosen. In a first implementation, all communication to and from the phase-shifted data router 140 is routed through
30 the slow communication channel 150. Consequently, only the slow communication channel 150 requires the introduction of $M*N$ data storage elements over its subchannels 152 and 154. The drawback of this

implementation is that the flexibility of the data communication network 100 is reduced.

In the preferred implementation, any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with $C \bmod N = A$, and any network path to the further network station from the first network station comprises D delay elements; B being a positive integer with $D \bmod N = B$. This ensures that the correct phase relation between clock cycle and routing information evaluation is maintained throughout the whole data communication network 100. For instance, in Fig. 3, $C = A$ and $B = D$, with C data elements 160 being introduced in the subchannel 152 between the output port of data router 130 and the input port of data router 140 and with D data elements 160 being introduced in the subchannel 154 between the input port of data router 130 and the output port of data router 140.

In other words, every communication channel 150 between two network stations exhibiting a phase-shifted routing information cycle with respect to each other should incorporate the appropriate number of data storage elements 160 to implement the number of cycles to which the phase shift corresponds. In Fig. 3, this means that all subchannels connected to an input port of the data router 140 are extended with A data storage elements 160 to introduce a delay of A cycles on the communication directed towards the data router 140, and all subchannels connected to an output port of the data router 140 are extended with B data storage elements 160 to introduce a delay of B cycles on the communication originating from the data router 140. Since $A+B = M*N$, each communication channel 150 to which data router 140 is connected incorporates $M*N$ data storage elements 160, thus ensuring the introduction of a delay of exactly M data packages on a communication loop between two neighbouring data routers.

This is explained in more detail in Fig. 4, where a data package consisting of data elements h, d1 and d2 is sent from data router 120 to data router 140 and back again in the network of IC 10 as shown in Fig. 3. The

routing information evaluation clock cycles for data routers 120 and 140 are indicated by bold vertical lines at the beginning of such a cycle. In other words, data router 120 evaluates the routing information of received data packages at t , $t+3$, $t+6$ and so on, whereas data router 140 evaluates the routing information of received data packages at $t+1$, $t+4$, $t+7$ and so on. Data router 120 sends data element h at $T=t$ to data router 140. At $T=t$, data element h is received by data storage element 160 in the first subchannel 152, which stores the data element h and sends it to the data router 140 at $T = t+1$, which receives the data element h during the same clock cycle and evaluates the routing information comprised in header h .

After the data router 140 has received data element $d1$ at $T = t+2$ and data element $d2$ and $T = t+3$, i.e., after the data router 140 has received the complete data package, the data router 140 sends the first data element of the data package to the data router 140 via the second subchannel 154. Due to the presence of two data storage elements 160 on the second subchannel 154, the first data element h is received by the data router 120 at $T = t+6$, i.e. during a cycle at which the data router 120 is scheduled to evaluate the routing information, with the other two data elements $d1$ and $d2$ respectively arriving at the subsequent cycles $t+7$ and $t+8$. It will be recognized that the data storage elements 160 in the subchannels 152 and 154 operate as phase shifters to ensure that routing information is evaluated at the right time in each data router phase domain. The application of phase shifting techniques has the advantage that the delay introduced on the individual subchannels 152, 154 can be less than a full data package, thus improving the performance of the slow communication channel 150 compared to the solution presented in Fig. 1.

At this point, it will be appreciated that the number of different phase domains can be further extended without departing from the teachings of the present invention. It is reiterated that although the exemplary implementations of the data storage elements is given on a communication channel between two data routers, implementations on channels between other types of network stations, e.g. between a data router and a network interface, are equally feasible.

Fig. 5 shows an asynchronous implementation of a delayed duplex communication channel 150 between two network stations, e.g. data routers 120 and 140, which is robust against clock skew. The data routers 120 and 140 are triggered by clock signal CLK. However, due to the fact that the clock signal has to travel over a longer wire to data router 140 than to data router 120, data router 140 receives a delayed clock signal CLK_d, with a delay of t_1 with respect to the clock signal CLK received by data router 120. In completely synchronous data communication networks 100, this can cause communication errors, because a data package sent by data router 140 at clock cycle t to data router 120 or the first delay element 160 over a slow communication channel 150 between the data routers 120 and 140 may arrive at its destination at cycle $t+1$ rather than at cycle t . As previously explained, this will cause the routing information to arrive at the data router 120 outside its routing information evaluation cycle, which will likely cause the loss of the information due to a routing error.

This risk can be reduced by implementing the $M*N$ data storage elements 160 as asynchronous FIFO buffers 520 and 540 on the first subchannel 152 and the second subchannel 154 respectively between data routers 120 and 140. This implementation is insensitive to clock skew, at least within certain limits. To improve the robustness against clock skew of the asynchronous FIFO buffers 520 and 540, the buffers may include slightly more than the $M*N$ data storage elements, as will be explained in more detail below.

The asynchronous FIFO buffers 520 and 540 have communication behaviour independent of the clock CLK; the data is rippled through the FIFO buffers 520 and 540 based on handshake protocols. Such behaviour is usually quicker than synchronous communication because the latter is dominated by the slowest path in the synchronous communication network, as previously explained.

A communication of a data package from data router 120 to FIFO buffer 520 is initiated by a handshake validation signal 501 followed by synchronous data communication 502 of the data elements of a data package having size N ; this communication is governed by data router 120, which is responsive to

clock signal CLK. The data elements take a time period t_2 to ripple through FIFO buffer 520, after which a handshake request 503 is sent to the data router 140. The receipt of an initial handshake request initializes data router 140 and triggers the data router 140 to accept the data communication by sending an acknowledge signal 504 to the FIFO buffer 520, which triggers the data communication 505. The data router 140 will remain initialized until the data stream of data packages has been received completely. The data package receipt periods of data routers 120 and 140 are indicated by the bold horizontal lines over the clock signals clk and clk_d respectively. The data router 140 receives the data communication synchronously and sends the data package synchronously, i.e. one data element per clock cycle, to FIFO buffer 540 N clock cycles after receiving the request signal 503, in accordance with a wormhole routing approach, by sending a handshake validation signal 506 and data communication 507 to the FIFO buffer 540. After a period t_3 , i.e. the time it takes the data elements to ripple through the FIFO buffer 540, the FIFO buffer 540 sends a handshake request signal 508 to data router 120.

Crucially, because data router 120 has already been initialized, i.e. it is already engaged in communicating a data stream to data router 140, data router 120 will only send an acknowledge signal 509 to such a handshake request to enable communication 510 at the beginning of a routing information evaluation cycle of data router 120, as indicated by the vertical dashed line. Alternatively, if the transmission of the data stream from data router 120 to data router 140 had completed prior to the handshake request 508 from FIFO buffer 540 to data router 120, this request would initialize the data router 120. In both cases, the receipt of the routing information in the correct timeslot of data router 120 is ensured despite the clock skew on the clock signal triggering the data routers 120 and 140. In case the clock skew between data router 120 and data router 140 is substantial, the data router 140 may send a first data element of a next data package to the FIFO buffer 540 before this buffer has received the acknowledge signal 509. In such a scenario, the FIFO buffer 509 must be capable of storing more than $M*N$ data elements to avoid the loss of data stored in the FIFO buffer 509. This can be realized by adding

one or more data storage elements to the M*N data storage elements as overwrite protection.

An IC 10 comprising a data communication network 100 according to the present invention can be designed using an IC design method modified as follows. After designing a first version of the IC 10, which can be done using well-known IC design tools, and which will not be further explained for that reason, an evaluation step is performed in which a first communication channel between a network station and a second network station having a data transfer delay exceeding a predefined delay threshold is identified. Consequently, the design of the data communication network 100 is modified according to the teachings of the present invention by inserting M*N data storage elements into the network, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel. This allows for an increase of the maximum clock speed at which the data communication network 100 can operate.

The insertion step may comprise inserting A data storage elements into the first subchannel (152) of the first communication channel (150) for introducing a delay of A cycles onto said first subchannel and inserting B data storage elements into the second subchannel (154) of the first communication channel (150) for introducing a delay of B cycles onto said second subchannel with A and B being positive integers and with $A + B = M*N$ to create a phase-shifted data communication network 100 as outlined in Fig. 3 and 4 and their detailed description.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements. In

the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

CLAIMS

1. An integrated circuit (10) comprising:
a plurality of functional blocks (101, 102, 103, 104); and
5 a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104), each data package comprising N data elements including a data element comprising routing information for the
10 network stations (105-108, 110, 120, 130, 140), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108), the data communication network
15 (100) comprising a first network station (140) and a second network station (120) interconnected through a first communication channel (150), the network comprising M*N data storage elements (160), M being a positive integer, for introducing a delay of M*N cycles on the first communication channel (150).
- 20 2. An integrated circuit (10) as claimed in Claim 1, wherein each communication channel (150) comprises:
a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station;
and
25 a second subchannel (154) between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations.
- 30 3. An integrated circuit (10) as claimed in Claim 2, wherein the M*N data elements (160) are distributed over the first subchannel (152) and the second subchannel (152; 154) of the first communication channel (150).

4. An integrated circuit as claimed in claim 3, wherein:
the first network station is arranged to evaluate the routing information
in a first cycle and the second network station is arranged to evaluate the
5 routing information in a second cycle, the difference between the first cycle and
the second cycle being A cycles; and
the first subchannel (152) of the first communication channel (150)
exhibits a delay of A cycles implemented by A data storage elements (160)
and the second subchannel (154) exhibits a delay of B cycles implemented by
10 B data storage elements (160), A and B being positive integers, with $A + B = M \cdot N$.
5. An integrated circuit as claimed in claim 4, wherein any network path
from a further network station being arranged to evaluate the routing
15 information in the second cycle to the first network station comprises C delay
elements, C being a positive integer with $C \text{ modulo } N = A$; and any network
path to the further network station from the first network station comprises D
delay elements; D being a positive integer with $D \text{ modulo } N = B$.
- 20 6. An integrated circuit (10) as claimed in Claim 1-5, wherein $M = 1$.
7. An integrated circuit (10) as claimed in Claim 3, wherein the first
subchannel (152) and the second subchannel (154) of the first communication
channel (150) each comprise a delay introduced by $\frac{1}{2} \cdot M \cdot N$ data storage
25 elements (160).
8. An integrated circuit (10) as claimed in Claim 1 or 2, further comprising
a clock signal generator, the plurality of network stations (110, 120, 130, 140)
and the $M \cdot N$ storage elements (160) being responsive to the clock signal
30 generator.

9. An integrated circuit (10) as claimed in claim 1 or 2, wherein each network station (110, 120, 130, 140) comprises a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information
5 from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port.

10 10. A method of designing an integrated circuit (10) comprising a plurality of functional blocks (101, 102, 103, 104), and a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103,
15 104), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108), each of the data routers (110, 120, 130, 140)
20 being coupled to a functional block (101, 102, 103, 104) via a network interface; the method comprising:

identifying a first communication channel (150) between a first network station (140) and a second network station (120) that has a data transfer delay exceeding a predefined delay threshold; and

25 inserting $M \times N$ data storage elements (160) into the data communication network (100), M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel (150).

11. A method as claimed in Claim 10, wherein each communication channel
30 (150) comprises a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station and a second subchannel (154) between an input port of the

second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations; and

the first network station being arranged to evaluate the routing
5 information in a first cycle and the second network station being arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles, the method further comprising:

inserting A data storage elements into the first subchannel (152) of the first communication channel (150) for introducing a delay of A cycles onto said
10 first subchannel; and

inserting B data storage elements into the second subchannel (154) of the first communication channel (150) for introducing a delay of B cycles onto said second subchannel; A and B being positive integers, with $A + B = M \cdot N$.

15

ABSTRACT

INTEGRATED CIRCUIT WITH DATA COMMUNICATION
NETWORK AND IC DESIGN METHOD

5

An integrated circuit (10) comprises a plurality of functional blocks (101, 102, 103, 104) and a data communication network (100) comprising a plurality of network stations being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104). Each data package comprising N data elements including a data element comprising routing information for the network stations (110, 120, 130, 140), N being an integer of at least two. The plurality of network stations comprises a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces, each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108), the data communication network (100) comprising a first network station (140) and a second network station (120) interconnected through a first communication channel (150), the network comprising M*N data storage elements (160), M being a positive integer, for introducing a delay of M*N cycles on the first communication channel (150). An integrated circuit (10) comprises a plurality of functional blocks (101, 102, 103, 104) and a plurality of data routers (110, 120, 130, 140), each being coupled to a functional block (101, 102, 103, 104). The introduction of a delay of one or more data packages on a slow communication channel (150) facilitates an increase of the maximum clock speed of the data communication over the data communication network (100).

<Fig. 1>

1/3

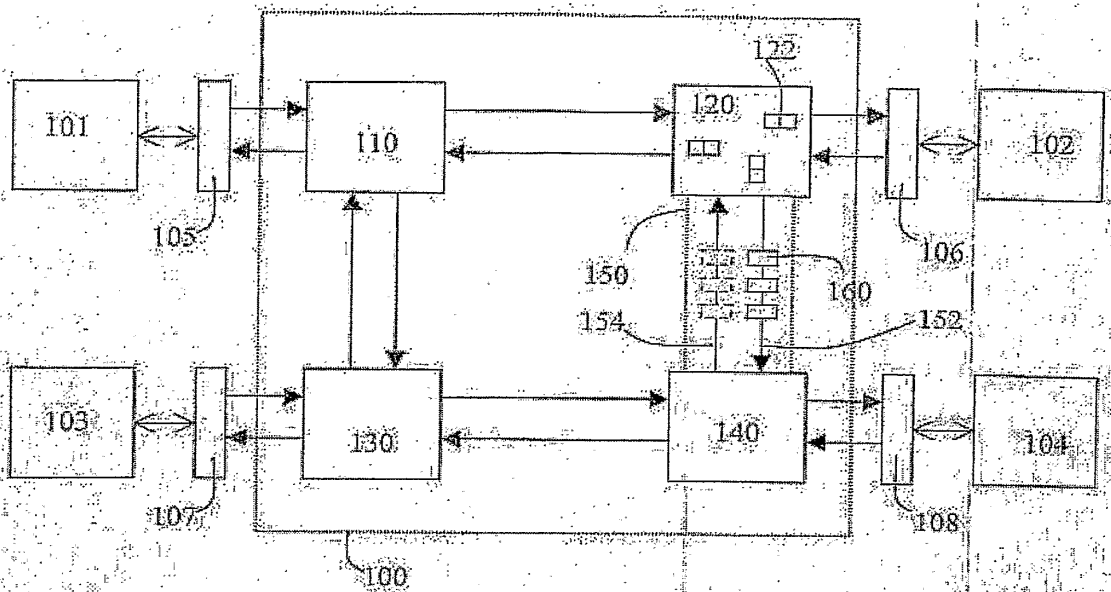


Fig. 1

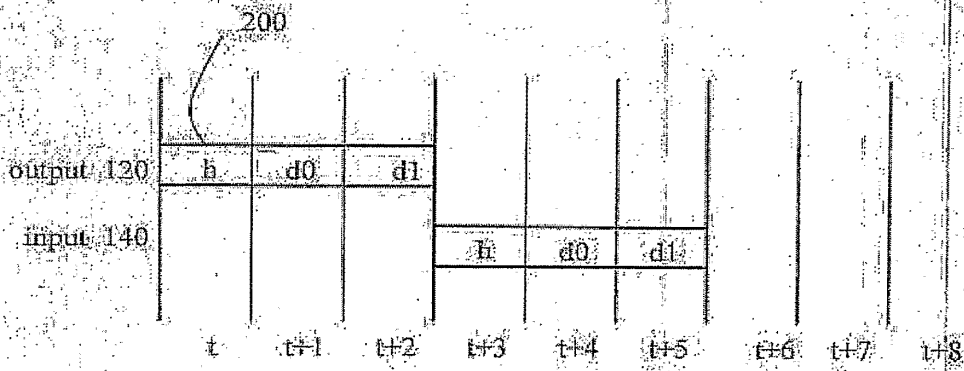


Fig. 2

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2/3

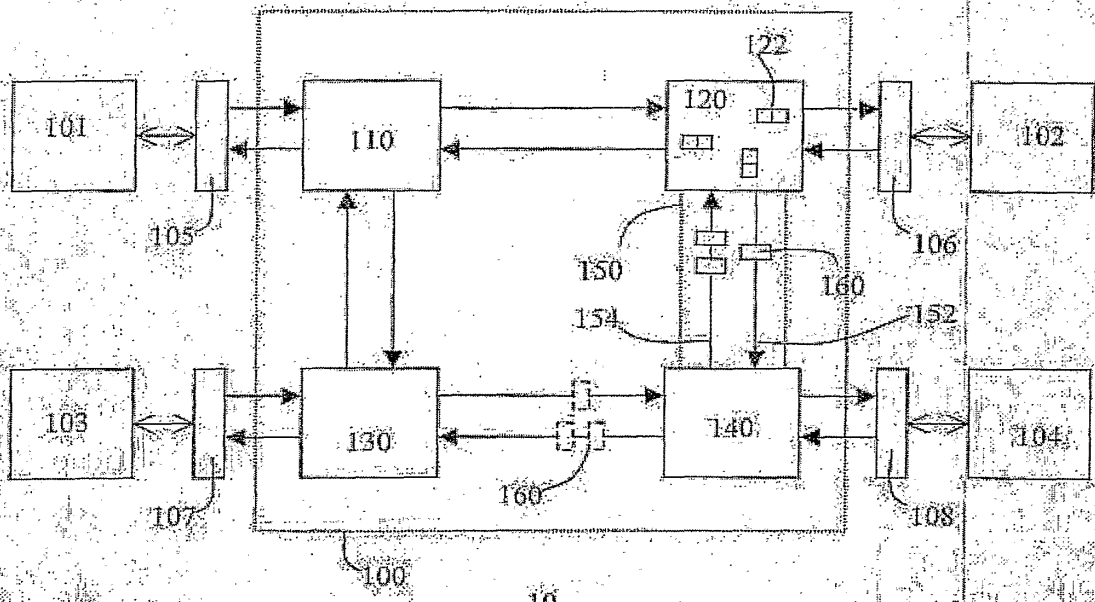


Fig. 3

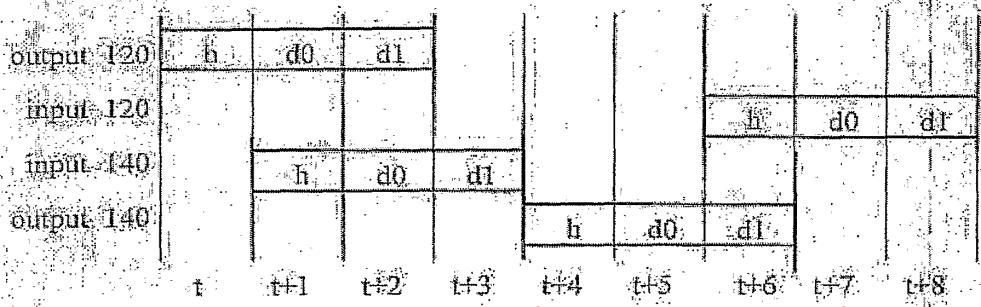


Fig. 4

PH000268EP2

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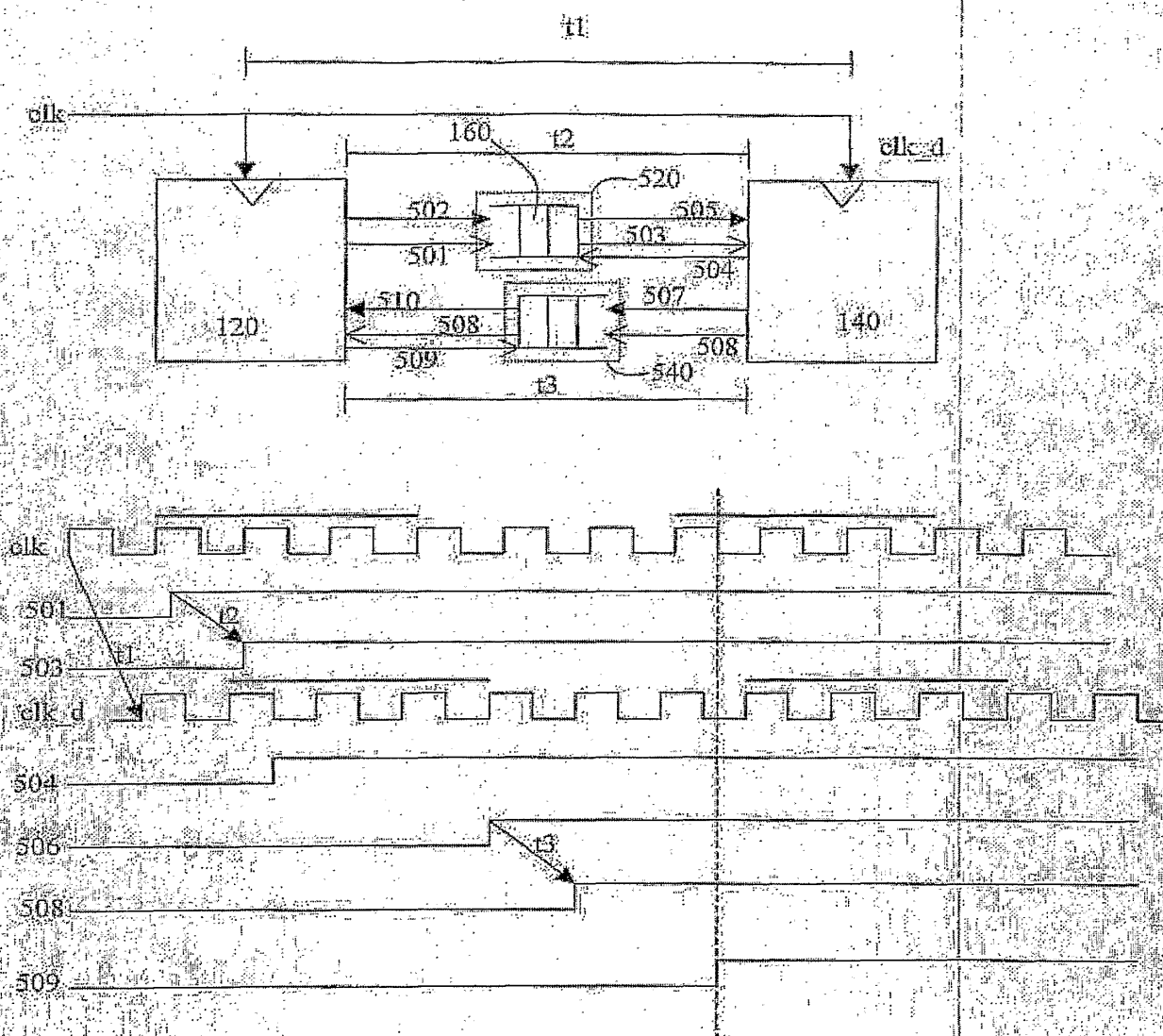


Fig. 5

PH000268EP2

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	First Named Inventor	John DIELISSSEN, AT AL		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		000268US	

U.S.PATENTS								
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	Filing Date		2007-10-22
	First Named Inventor	John DIELISSSEN, AT AL	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		000268US

1	DIELISSEN J. ET AL: Concepts and Implementation of the Philips Network-on-Chip, November 13, 2003, XP002330547	☐
2	CHANDRA V ET AL: An Interconnect Channel Design Methodology for High Performance Integrated Circuits, IEEE Vol. 2, February 16, 2004, pages 1138-1143, XP010684819	☐
3	CAROLONI L. P: Coping with Latency in SOC Design, IEEE MICRO, September 2002, pages 24-35, XP002393174	☐
4	J. DIELISSSEN, ET AL: Introduction of Flit Delay on Links, Philips Research, pages 1-5	☐
5	ANDREI RADULESCU, ET AL: An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration, Philips Research, pages 1-6,	☐
6	E. RIJPKEMA, ET AL: Trade-offs in the Design of a Router with Both Guaranteed and Best-Effort Services for Network on Chip, IEEE Proc. Comput Digit Tech, May 16, 2003.	☐
7	ANTOINE JALABERT, ET AL: X pipesCompiler: A Tool for Instantiating Application Specific Networks on Chip, IEEE 2004, pages 1-6	☐
8	RAMALINGAM SRIDHAR: System-on-Chip (SoC): Clocking and Synchronization Issues, IEEE VLSI Design VLSID 2004, Computer Society, pages 1-8	☐

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Examiner Signature		Date Considered	
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	Filing Date	2007-10-22
	First Named Inventor	John DIELISSSEN, AT AL
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	Examiner Name	
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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Yan Glickberg/	Date (YYYY-MM-DD)	2007-12-17
Name/Print	Yan Glickberg	Registration Number	51,742

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EFS ID:	2624051
Application Number:	11912175
International Application Number:	
Confirmation Number:	5577
Title of Invention:	INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD
First Named Inventor/Applicant Name:	JOHN DIELISSSEN
Customer Number:	24737
Filer:	Yan Glickberg/Burnett James
Filer Authorized By:	Yan Glickberg
Attorney Docket Number:	000268 US1
Receipt Date:	20-DEC-2007
Filing Date:	
Time Stamp:	16:18:04
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no
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Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
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8	NPL Documents	SYSTEM-ON-CHIP_CLOCKI NG_AND_SYNCHRONIXATI ON.pdf	135996 9d38dd3c56b36709fb65592e5de5f316 40b8ba64	no	8
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9	NPL Documents	TRADE-OFF_IN_THE_DESI GN_OF_A_ROUTER.pdf	328780 5603f4c156354005d4ec75a6ba964a4e 5d877d98	no	9
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New International Application Filed with the USPTO as a Receiving Office

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DO/EO WORKSHEET

Paralegal/National Stage Division

U.S. Appl. No. 11/912175

International Appl. No. 1006/051218

Application filed by: ☒ 30 months

WIPO PUBLICATION INFORMATION:

Publication No.: WO /

Publication Language: ☒ English ☐ German ☐ French ☐ Japanese
☐ Russian ☐ Korean ☐ Other: _____

Publication Date: 26 Oct 06

Not Published: ☐ U.S. only designated ☐ EP request Published: ☐

INTERNATIONAL APPLICATION PAPERS IN THE APPLICATION FILE:

☒ International Application

☐ Article 19 Amendments

☐ PCT/IB/331

☐ PCT/IPEA/409 IPER (PCT/IPEA/416 on front)

☐ Annexes to 409 (Article 34 Amendment)

☒ Priority Document (s) No. 1

☐ Request form PCT/RO/101

☒ PCT/ISA/210 - Search Report sp

☐ Search Report References

☐ PCT/IB/306 - Notification of a Change

☐ Other: _____

RECEIPTS FROM THE APPLICANT:

☒ Basic National Fee (or authorization to charge)

☒ Description 17

☒ Claims 4

☒ Drawing Figure(s) - (# of dwgs. 3)

☐ Translation of Article 19 Amendments

☐ entered ☐ not entered:

☐ not a page for page substitution
☐ replaced by Article 34 Amendment

☐ Translation of Annexes to 409

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☐ not a page for page substitution
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☐ Application Data Sheet

☐ Power of Attorney ☐ Change of Address

☒ Preliminary Amendment(s) Filed on:

1. 22 Oct 07 2. _____

☒ Information Disclosure Statement(s) Filed on:

1. 20 Dec 07 2. _____

☐ Assignment Document (forwarded to Assignment Branch)

☐ Assignee PG Publication Notice

☐ Substitute Specification Filed on:

1. _____ 2. _____

☐ Verified Small Status Statement (executed)

☒ Oath/Declaration (executed)

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☐ DNA Diskette

☐ Sequence Listing

☐ Other: 1. _____

☐ Other: 1. _____

NOTES: ☐ I.A. used as Specification ☐ Other: _____

35 U.S.C. 371 - Receipt of Request

22 Oct 07

Date Acceptable Oath/Declaration Received

Date of Completion of requirements under 35 U.S.C. 371(c)(1), (c)(2) and (c)(4)

Date of Completion of ALL requirements under 35 U.S.C. 371

Date of Completion of DO/EO 903 - Notification of Acceptance

Date of Completion of DO/EO 905 - Notification of Missing Requirements

Date of Completion of DO/EO 916 - Notification of Defective Response

Date of Completion of DO/EO 909 - Notification of Abandonment

☐ EP ☐ JP ☐ SE ☐ AU ☐ US ☐

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET (FOR USE WITH FORM PTO-875)							SERIAL NO. 11/912175	FILING DATE
							APPLICANT(S)	
CLAIMS								
	AS FILED		AFTER 1 st AMENDMENT		AFTER 2 nd AMENDMENT			
	IND.	DEP.	IND.	DEP.	IND.	DEP.		
1	1		1					
2		1		1				
3		1		1				
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TOTAL DEP.	11	←	10	←		←		
TOTAL CLAIMS	14		11					
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TOTAL DEP.		←		←		←		
TOTAL CLAIMS								

PTO 1360 (REV. 11/04)

U.S. DEPARTMENT of COMMERCE
Patent and Trademark Office

PATENT APPLICATION FEE DETERMINATION RECORD

Effective December 8, 2004

Application or Docket Number

11/912175

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
U.S. NATIONAL STAGE FEES		
BASIC FEE	SMALL ENT. = \$ 150	LARGE ENT. = \$ 300
EXAMINATION FEE	Satisfies PCT Article 33(1)-(4) = \$ 50 / \$ 100	All other situations = \$ 100 / \$ 200
SEARCH FEE	U.S. is ISA = \$ 50 / \$ 100 ALL other countries = \$ 200 / \$ 400	ALL other situations = \$ 250 / \$ 500
FEE FOR EXTRA SPEC. PGS.	25 minus 100 =	/ 50 =
TOTAL CHARGEABLE CLAIMS	11 minus 20 =	* -
INDEPENDENT CLAIMS	1 minus 3 =	* -
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ OR

OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE		OR	BASIC FEE	310
EXAM. FEE			EXAM. FEE	210
SEARCH FEE			SEARCH FEE	410
X \$ 125 =			X \$ 250 =	
X \$ 25 =		OR	X \$ 50 =	
X \$ 100 =		OR	X \$ 200 =	
+ \$ 180 =		OR	+ \$ 360 =	
TOTAL		OR	TOTAL	930

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	** =
Independent	*	Minus	*** =
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X \$ 25 =		OR	X \$ 50 =	
X \$ 100 =		OR	X \$ 200 =	
+ \$ 180 =		OR	+ \$ 360 =	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	** =
Independent	*	Minus	*** =
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X \$ 25 =		OR	X \$ 50 =	
X \$ 100 =		OR	X \$ 200 =	
+ \$ 180 =		OR	+ \$ 360 =	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

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 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '20', enter "20".
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
11/912,175	10/22/2007		930	000268 US1	11	1

CONFIRMATION NO. 5577

24737
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

FILING RECEIPT



OC000000029587187

Date Mailed: 05/01/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

John Dielissen, Weert, NETHERLANDS;
Edwin Rijpkema, Nieuwerkerk A/d IJssel, NETHERLANDS;

Assignment For Published Patent Application

KONINKLIJKE PHILIPS ELECTRONICS, N.V., EINDHOVEN, NL

Power of Attorney: The patent practitioners associated with Customer Number 24737

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/IB2006/051218 04/20/2006

Foreign Applications

EUROPEAN PATENT OFFICE (EPO) 05103232.4 04/21/2005

Projected Publication Date: 08/07/2008

Non-Publication Request: No

Early Publication Request: No

Title

Integrated Circuit with Data Communication Network and Ic Design Method

Preliminary Class

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent

page 1 of 3

in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).



UNITED STATES PATENT AND TRADEMARK OFFICE

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U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
11/912,175	John Dielissen	000268 US1
24737 PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510		INTERNATIONAL APPLICATION NO. PCT/IB2006/051218
		I.A. FILING DATE 04/20/2006
		PRIORITY DATE 04/21/2005

CONFIRMATION NO. 5577
371 ACCEPTANCE LETTER



OC000000029587188

Date Mailed: 05/01/2008

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

10/22/2007
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1),
(c)(2) and (c)(4) REQUIREMENTS

10/22/2007
DATE OF COMPLETION OF ALL
35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363). Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Copy of the International Application filed on 10/22/2007
- Copy of the International Search Report filed on 10/22/2007
- Preliminary Amendments filed on 10/22/2007
- Information Disclosure Statements filed on 12/20/2007
- Oath or Declaration filed on 10/22/2007
- U.S. Basic National Fees filed on 10/22/2007
- Priority Documents filed on 10/22/2007
- Specification filed on 10/22/2007
- Claims filed on 10/22/2007
- Abstracts filed on 10/22/2007
- Drawings filed on 10/22/2007

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

TAMALA D HOLLAND

Telephone: (703) 308-9140 EXT 209

page 2 of 2

FORM PCT/DO/EO/903 (371 Acceptance Notice)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/912,175	10/22/2007	John Dielissen	000268 US1

CONFIRMATION NO. 5577

24737

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

PUBLICATION NOTICE



Title: Integrated Circuit with Data Communication Network and Ic Design Method

Publication No. US-2008-0186983-A1

Publication Date: 08/07/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/912,175	10/22/2007	John Dielissen	000268 US1	5577
24737 7590 07/22/2010 PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510			EXAMINER SAM, PHIRIN	
			ART UNIT 2476	PAPER NUMBER
			MAIL DATE 07/22/2010	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/912,175	DIELISSEN ET AL.	
	Examiner	Art Unit	
	PHIRIN SAM	2476	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 22 October 2007.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-3,6 and 10 is/are rejected.

7) ☒ Claim(s) 4,5,7-9 and 11 is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 22 October 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 12/20/07.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the label of each block. For example, what is block 101 represent? Each block of the drawing should be labeled as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-3, 6, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 7,362,763 to Wybenga et al. (hereinafter "Wybenga") in view of US Patent 7,197,009 of Dispensa (hereinafter "Dispensa").

Regarding claims 1 and 6, Wybenga discloses an integrated circuit (10) comprising:

- (a) a plurality of functional blocks (101, 102, 103, 104) (see Fig. 1, col. 3, lines 65-67, col. 4, lines 1-2, *distributed architecture router 100 provides scalability and high-performance using up to N independent routing nodes (RN), including exemplary routing nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-speed switch fabrics 155a and 155b*);
- (b) a data communication network (see Fig. 1) comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101, 102, 103, 104) (see Fig. 1, col. 3, lines 65-67, col. 4, lines 1-7, *distributed architecture router 100 provides scalability and high-performance using up to N independent routing nodes (RN), including exemplary routing nodes 110, 120, 130 and 140, connected by switch 150, which comprises a*

pair of high-speed switch fabrics 155a and 155b. Each routing node comprises an input-output processor (IOP) module, and one or more physical medium device (PMD) module), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140) (see Fig. 1, col. 4, lines 18-25, each of IOP modules 116, 126, 136 and 146 classifies requested services, looks up destination addresses from frame headers or data fields, and forwards frames to the outbound IOP module. Moreover, each IOP module also maintains an internal routing table determined from routing protocol messages and provisioned static routes and computes the optimal data paths from the routing table. Each IOP module processes an incoming frame from one of its PMD modules), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108) (see Figs. 1 and 2, elements 110, 120, 130, 140, 112, 114, 122, 124, 132, and 134, col. 4, lines 3-14), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101, 102, 103, 104) via a network interface (105-108) (see Figs. 1 and 2, elements 122, 124, and 126, col. 5, lines 7-16), the data communication network (100) comprising a first network station (140) and a second network station (120) interconnected through a first communication channel (150) (see Fig. 1, elements 110, 140, col. 4, lines 15-21);

Wybenga is silent to disclose the network comprising $M \times N$ data storage elements (160), M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel (150). However, Dispensa discloses the network comprising $M \times N$ data storage elements (160), M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel (150) (see Fig. 4, elements 411 and 412, col. 4, lines 63-67, col. 5, lines 1-10). At the time of the invention, it would have been obvious to a person of ordinary skill in

the art to combine the network comprising $M \times N$ data storage elements (160), M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel (150) teaching by Dispensa with Wybenga. The motivation for doing so would have been to provide to control the flow of data over two links to maintain an acceptable delay variation over the links for reducing the problem of miss-sequenced packets when the links communicate with a common destination read on column 3, lines 4-8. Therefore, it would have been obvious to combine Dispensa and Wybenga to obtain the invention as specified in the claims 1 and 6.

Regarding claim 2, Wybenga is silent to disclose wherein each communication channel (150) comprises: a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station; and a second subchannel (154) between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations. However, Dispensa discloses each communication channel (150) comprises: a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station; and a second subchannel (154) between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations (see Figs. 2 and 4, elements 411 and 412, col. 4, lines 63-67, col. 5, lines 1-24). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine a first subchannel (152) between an input port of a first associated network station and an output port of a second associated network station; and a second subchannel (154) between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations teaching by

Dispensa with Wybenga. The motivation for doing so would have been to provide to control the flow of data over two links to maintain an acceptable delay variation over the links for reducing the problem of miss-sequenced packets when the links communicate with a common destination read on column 3, lines 4-8. Therefore, it would have been obvious to combine Dispensa and Wybenga to obtain the invention as specified in the claim 2.

Regarding claim 3, Wybenga is silent to disclose wherein the M*N data elements (160) are distributed over the first subchannel (152) and the second subchannel (152; 154) of the first communication channel (150). However, Dispensa discloses the M*N data elements (160) are distributed over the first subchannel (152) and the second subchannel (152; 154) of the first communication channel (150) (see Fig. 4, elements 411 and 412, col. 4, lines 63-67, and col. 5, lines 1-10). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the M*N data elements (160) are distributed over the first subchannel (152) and the second subchannel (152; 154) of the first communication channel (150) teaching by Dispensa with Wybenga. The motivation for doing so would have been to provide for controlling the flow of data over two links to maintain an acceptable delay variation over the links for reducing the problem of miss-sequenced packets when the links communicate with a common destination read on column 3, lines 4-8. Therefore, it would have been obvious to combine Dispensa and Wybenga to obtain the invention as specified in the claim 3.

Regarding claim 10, Wybenga discloses a method of designing an integrated circuit (10) comprising a plurality of functional blocks (101,102, 103, 104) (see Fig. 1, col. 3, lines 65-67, col. 4, lines 1-2, *distributed architecture router 100 provides scalability and high-performance using up to N independent routing nodes (RN), including exemplary routing nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-speed switch fabrics 155a and*

155b), and a data communication network comprising a plurality of network stations (105-108, 110, 120, 130, 140) being interconnected via a plurality of communication channels (150) for communicating data packages between the functional blocks (101,102, 103, 104) (see Fig. 1, col. 3, lines 65-67, col. 4, lines 1-7, *distributed architecture router 100 provides scalability and high-performance using up to N independent routing nodes (RN), including exemplary routing nodes 110, 120, 130 and 140, connected by switch 150, which comprises a pair of high-speed switch fabrics 155a and 155b. Each routing node comprises an input-output processor (IOP) module, and one or more physical medium device (PMD) module*), each data package comprising N data elements including a data element comprising routing information for the network stations (105-108, 110, 120, 130, 140) (see Fig. 1, col. 4, lines 18-25, *each of IOP modules 116, 126, 136 and 146 classifies requested services, looks up destination addresses from frame headers or data fields, and forwards frames to the outbound IOP module. Moreover, each IOP module also maintains an internal routing table determined from routing protocol messages and provisioned static routes and computes the optimal data paths from the routing table. Each IOP module processes an incoming frame from one of its PMD modules*), N being an integer of at least two, the plurality of network stations comprising a plurality of data routers (110, 120, 130, 140) and a plurality of network interfaces (105-108) (see Figs. 1 and 2, elements 110, 120, 130, 140, 112, 114, 122, 124, 132, and 134, col. 4, lines 3-14), each of the data routers (110, 120, 130, 140) being coupled to a functional block (101,102, 103, 104) via a network interface (see Figs. 1 and 2, elements 122, 124, and 126, col. 5, lines 7-16);

Wybenga is silent to disclose identifying a first communication channel (150) between a first network station (140) and a second network station (120) that has a data transfer delay exceeding a predefined delay threshold; and inserting M*N data storage elements (160) into the

data communication network (100), M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel (150). However, Dispensa discloses identifying a first communication channel (150) (see Fig. 4, element 410, col. 4, lines 28-29) between a first network station (140) and a second network station (120) (see Fig. 2, between elements 200 and 201 or 200 and 202 or 200 and 203) that has a data transfer delay exceeding a predefined delay threshold; and inserting $M*N$ data storage elements (160) into the data communication network (100), M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel (150) (see Figs. 4 and 5, col. 4, lines 63-67, col. 5, lines 1-52). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine identifying a first communication channel (150) between a first network station (140) and a second network station (120) that has a data transfer delay exceeding a predefined delay threshold; and inserting $M*N$ data storage elements (160) into the data communication network (100), M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel (150) teaching by Dispensa with Wybenga. The motivation for doing so would have been to provide for controlling the flow of data over two links to maintain an acceptable delay variation over the links for reducing the problem of miss-sequenced packets when the links communicate with a common destination read on column 3, lines 4-8. Therefore, it would have been obvious to combine Dispensa and Wybenga to obtain the invention as specified in the claim 10.

Allowable Subject Matter

5. Claims 4, 5, 7-9, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHIRIN SAM whose telephone number is (571)272-3082. The examiner can normally be reached on Increased Flexitime Policy (IFP) Program.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272 - 3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Respectfully submitted,

Date: July 19, 2010

By: /Phirin Sam/
Phirin Sam
Primary Examiner
Art Unit 2476

Notice of References Cited	Application/Control No. 11/912,175	Applicant(s)/Patent Under Reexamination DIELISSEN ET AL.	
	Examiner PHIRIN SAM	Art Unit 2476	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,362,763	04-2008	Wybenga et al.	370/395.1
*	B	US-7,197,009	03-2007	Dispensa, Stephen	370/237
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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	N					
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	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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CONFIRMATION NO. 5577

SERIAL NUMBER 11/912,175	FILING or 371(c) DATE 10/22/2007 RULE	CLASS 370	GROUP ART UNIT 2476	ATTORNEY DOCKET NO. 000268 US1		
APPLICANTS John Dielissen, Weert, NETHERLANDS; Edwin Rijpkema, Nieuwerkerk A/d IJssel, NETHERLANDS; ** CONTINUING DATA ***** This application is a 371 of PCT/IB2006/051218 04/20/2006 ** FOREIGN APPLICATIONS ***** EUROPEAN PATENT OFFICE (EPO) 05103232.4 04/21/2005 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and /PHIRIN SAM/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY NETHERLANDS	SHEETS DRAWINGS 3	TOTAL CLAIMS 11	INDEPENDENT CLAIMS 1
ADDRESS PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510 UNITED STATES						
TITLE Integrated Circuit with Data Communication Network and Ic Design Method						
FILING FEE RECEIVED 930	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes 	Application/Control No. 11912175	Applicant(s)/Patent Under Reexamination DIELISSEN ET AL.
	Examiner PHIRIN SAM	Art Unit 2476

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
370/231-235,351-354,356,389,392,394,395.1,395.21,395.31,400-402,412,413,415,417 (Text search - See text search history printout).	07/19/2010	PS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/PHIRIN SAM/ Acting Examiner.Art Unit 2419/2400	
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<i>Index of Claims</i> 	Application/Control No. 11912175	Applicant(s)/Patent Under Reexamination DIELISSEN ET AL.
	Examiner PHIRIN SAM	Art Unit 2476

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	07/19/2010								
	1	✓								
	2	✓								
	3	✓								
	4	O								
	5	O								
	6	✓								
	7	O								
	8	O								
	9	O								
	10	✓								
	11	O								

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	954913	routers or switches or ((rout\$3 or switch\$3) near (devices or units or modules))	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L2	733702	(function\$3 near (blocks or devices or units or modules)) or (process\$3 near2 (blocks or devices or units or modules)) or processors	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L3	1321804	buffer\$3 or FIFO or queue\$3	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L4	3708104	channel\$3 or bus\$3 or link\$1	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L5	159047	L1 and L2	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L6	69413	L5 and L3	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L7	63175	L6 and L4	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L8	68457	(input adj port\$1) and (output adj port\$1)	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L9	5545	L7 and L8	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L10	77506	rout\$3 near2 information	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36

L11	1469	L9 and L10	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L12	167828	first adj (channel or link or line or path)	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L13	305	L11 and L12	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L14	152179	second adj (channel or link or line or path)	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L15	192	L13 and L14	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 08:36
L16	865	delay\$3 near2 first near2 (channel or bus or link)	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 09:18
L17	281	L16 and L1	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 09:18
L18	223	L17 and (stor\$4 or buffer\$3 or queue\$3)	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 09:18
L19	82	L18 and L12	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 09:19
L20	65	L19 and L14	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 09:19
L23	42197	370/231-235,351-354,356,389,392,394,395.1,395.21,395.31,400-402,412,413,415,417.cols.	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 10:33
L24	7	L23 and L20	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 10:34

L25	10	I23 and I19	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 10:34
L26	68	I23 and I15	US-PGPUB; USPAT; DERWENT	OR	OFF	2010/07/19 10:34

EAST Search History (Interference)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11912175	
	Filing Date		2007-10-22	
	First Named Inventor	John DIELISSSEN, AT AL		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		000268US	

U.S.PATENTS								
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11912175
	Filing Date		2007-10-22
	First Named Inventor	John DIELISSSEN, AT AL	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		000268US

/PS/	1	DIELISSEN J. ET AL: Concepts and Implementation of the Philips Network-on-Chip, November 13, 2003, XP002330547	☐
/PS/	2	CHANDRA V ET AL: An Interconnect Channel Design Methodology for High Performance Integrated Circuits, IEEE Vol. 2, February 16, 2004, pages 1138-1143, XP010684819	☐
/PS/	3	CAROLONI L. P: Coping with Latency in SOC Design, IEEE MICRO, September 2002, pages 24-35, XP002393174	☐
/PS/	4	J. DIELISSSEN, ET AL: Introduction of Flit Delay on Links, Philips Research, pages 1-5	☐
/PS/	5	ANDREI RADULESCU, ET AL: An Efficient On-Chip Network Interface Offering Guaranteed Services, Shared-Memory Abstraction, and Flexible Network Configuration, Philips Research, pages 1-6,	☐
/PS/	6	E. RIJPKEMA, ET AL: Trade-offs in the Design of a Router with Both Guaranteed and Best-Effort Services for Network on Chip, IEEE Proc. Comput Digit Tech, May 16, 2003.	☐
/PS/	7	ANTOINE JALABERT, ET AL: X pipesCompiler: A Tool for Instantiating Application Specific Networks on Chip, IEEE 2004, pages 1-6	☐
/PS/	8	RAMALINGAM SRIDHAR: System-on-Chip (SoC): Clocking and Synchronization Issues, IEEE VLSI Design VLSID 2004, Computer Society, pages 1-8	☐

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EXAMINER SIGNATURE

Examiner Signature	/Phirin Sam/	Date Considered	07/19/2010
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
John DIELISSSEN; et al.

Atty. Docket: 000268US1

Confirmation No. 5577

Serial No. 11/912,175

Group Art Unit: 2476

Filed: October 22, 2007

Examiner: SAM, Phirin

Title: INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC
DESIGN METHOD

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action mailed on July 22, 2010, please amend the above-identified application and consider the remarks as follows:

IN THE DRAWING

Please replace FIGs 1, 3 and 5 with the enclosed replacement FIGs 1, 3 and 5.

IN THE ABSTRACT

Please delete the current Abstract in its entirety and substitute therefor the enclosed
New Abstract.

NEW ABSTRACT

An integrated circuit includes functional blocks and a data communication network having network stations interconnected via communication channels for communicating data packages between the functional blocks. Each data package includes N data elements having a data element with routing information for the network stations, N being an integer of at least two. The network stations include data routers and network interfaces, where each of the data routers is coupled to a functional block via a network interface. The data communication network includes first and second network stations interconnected through a first communication channel. The network includes $M*N$ data storage elements, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel.

IN THE SPECIFICATION

Please amend the specification as follows:

Replace the paragraph spanning pages 10-11, between page 10, line 18, and page 11, line 3 of the specification with the following:

Fig. 2 shows the timing behaviour of the communication along the slow channel 150 extended with 3 data storage elements 160 on the first subchannel 152 interconnecting an output port of data router 120 with an input port of the data router 140. At clock cycle t , the data router 120 employing wormhole routing receives the first data element h of a data package (indicated by the bold box) having a size of 3 data elements. The subsequent data elements $d1$ and $d2$ of this data package are received by the data router 120 at respective clock cycles $t+1$ and $t+2$. The data routers 110, 120, 130, 140 are all configured to periodically evaluate the content of a received data package, that is after every N clock cycles for a data package having a size N data elements. In the embodiment of the IC 10 shown in Fig. 1, all the data routers 110, 120, 130, 140 perform this operation simultaneously, i.e. at the same clock cycle, which is clock cycle t plus every N th clock cycle afterwards, i.e. at $t+3$, $t+6$ and so on, at which the arrival of a header h of a new data package is expected. Such a periodical checking mechanism by a data router may for instance be implemented using modulo N counters. Consequently, it is essential that the

headers of the data packages do not arrive at any data router 110, 120, 130, 140 outside such an evaluation clock cycle.

Replace the paragraph spanning pages 12-13, between page 12, line 30, and page 13, line 10 of the specification with the following:

This is explained in more detail in Fig. 4, where a data package consisting of data elements h , ~~$d1$ and $d2$~~ $d0$ and $d1$ is sent from data router 120 to data router 140 and back again in the network of IC 10 as shown in Fig. 3. The routing information evaluation clock cycles for data routers 120 and 140 are indicated by bold vertical lines at the beginning of such a cycle. In other words, data router 120 evaluates the routing information of received data packages at t , $t+3$, $t+6$ and so on, whereas data router 140 evaluates the routing information of received data packages at $t+1$, $t+4$, $t+7$ and so on. Data router 120 sends data element h at $T=t$ to data router 140. At $T=t$, data element h is received by data storage element 160 in the first subchannel 152, which stores the data element h and sends it to the data router 140 at $T = t+1$, which receives the data element h during the same clock cycle and evaluates the routing information comprised in header h .

Replace the paragraph on page 13, between lines 11-25 of the specification with the following:

After the data router 140 has received data element ~~$d1$~~ $d0$ at $T = t+2$ and data

element d2-d1 and $T = t+3$, i.e., after the data router 140 has received the complete data package, the data router 140 sends the first data element of the data package to the data router 140-120 via the second subchannel 154. Due to the presence of two data storage elements 160 on the second subchannel 154, the first data element h is received by the data router 120 at $T = t+6$, i.e. during a cycle at which the data router 120 is scheduled to evaluate the routing information, with the other two data elements ~~d1 and d2~~ d0 and d1 respectively arriving at the subsequent cycles $t+7$ and $t+8$. It will be recognized that the data storage elements 160 in the subchannels 152 and 154 operate as phase shifters to ensure that routing information is evaluated at the right time in each data router phase domain. The application of phase shifting techniques has the advantage that the delay introduced on the individual subchannels 152, 154 can be less than a full data package, thus improving the performance of the slow communication channel 150 compared to the solution presented in Fig. 1.

Replace the paragraph spanning pages 14-15, between page 14, line 28, and page 15, line 16 of the specification with the following:

A communication of a data package from data router 120 to FIFO buffer 520 is initiated by a handshake validation signal 501 followed by synchronous data communication 502 of the data elements of a data package having size N; this communication is governed by data router 120, which is responsive to clock signal CLK.

The data elements take a time period t_2 to ripple through FIFO buffer 520, after which a handshake request 503 is sent to the data router 140. The receipt of an initial handshake request initializes data router 140 and triggers the data router 140 to accept the data communication by sending an acknowledge signal 504 to the FIFO buffer ~~520~~ 540, which triggers the data communication 505. The data router 140 will remain initialized until the data stream of data packages has been received completely. The data package receipt periods of data routers 120 and 140 are indicated by the bold horizontal lines over the clock signals clk and clk_d respectively. The data router 140 receives the data communication synchronously and sends the data package synchronously, i.e. one data element per clock cycle, to FIFO buffer 540 N clock cycles after receiving the request signal 503, in accordance with a wormhole routing approach, by sending a handshake validation signal 506 and data communication 507 to the FIFO buffer 540. After a period t_3 , i.e. the time it takes the data elements to ripple through the FIFO buffer 540, the FIFO buffer 540 sends a handshake request signal 508 to data router 120.

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) An integrated circuit ~~(10)~~ comprising:
a plurality of functional blocks ~~(101, 102, 103, 104)~~; and
a data communication network comprising a plurality of network stations ~~(105-108, 110, 120, 130, 140)~~ being interconnected via a plurality of communication channels ~~(150)~~ for communicating data packages between the functional blocks ~~(101, 102, 103, 104)~~, each data package comprising N data elements including a data element comprising routing information for the network stations ~~(105-108, 110, 120, 130, 140)~~, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers ~~(110, 120, 130, 140)~~ and a plurality of network interfaces ~~(105-108)~~, each of the data routers ~~(110, 120, 130, 140)~~ being coupled to a functional block ~~(101, 102, 103, 104)~~ via a network interface ~~(105-108)~~, the data communication network ~~(100)~~ comprising a first network station ~~(140)~~ and a second network station ~~(120)~~ interconnected through a first communication channel ~~(150)~~, the network comprising M*N data storage elements ~~(160)~~, M being a positive integer, for introducing a delay of M*N cycles on the first communication

channel-(150).

2.(Currently Amended) ~~An~~The integrated circuit (10)-as claimed in Claim 1, wherein each communication channel (150)-of the plurality of communication channels comprises:

a first subchannel (152)-between an input port of a first associated network station and ~~and~~-an output port of a second associated network station; and

a second subchannel (154)-between an input port of the second associated network station and ~~and~~-an output port of the first associated network station for enabling duplex communication between the two associated network stations.

3.(Currently Amended) ~~An~~The integrated circuit (10)-as claimed in Claim 2, wherein the M*N data storage elements (160)-are distributed over the first subchannel (152)-and the second subchannel (152; 154)-of the first communication channel-(150).

4.(Currently Amended) ~~An~~The integrated circuit as claimed in claim 3, wherein:

the first network station is arranged to evaluate the routing information in a first cycle and the second network station is arranged to evaluate the routing information in a second cycle, the difference between the first ~~eyle~~cycle and the second cycle being A cycles; and

the first subchannel (152)-of the first communication channel (150)-exhibits a delay of A cycles implemented by A data storage elements (160)-and the second subchannel

(154) exhibits a delay of B cycles implemented by B data storage elements (160), A and B being positive integers, with $A + B = M \cdot N$.

5.(Currently Amended) ~~An~~The integrated circuit as claimed in claim 4, wherein any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with $C \bmod N = A$; and any network path to the further network station from the first network station comprises D delay elements; D being a positive integer with $D \bmod N = B$.

6.(Currently Amended) ~~An~~The integrated circuit (10) as claimed in Claim 1, wherein $M = 1$.

7.(Currently Amended) ~~An~~The integrated circuit (10) as claimed in Claim 3, wherein the first subchannel (152) and the second subchannel (154) of the first communication channel (150) each comprise a delay introduced by $\frac{1}{2} \cdot M \cdot N$ data storage elements (160).

8.(Currently Amended) ~~An~~The integrated circuit (10) as claimed in Claim 1, further comprising a clock signal generator, the plurality of network stations (110, 120, 130, 140) and the $M \cdot N$ data storage elements (160) being responsive to the clock signal generator.

9.(Currently Amended) ~~An~~The integrated circuit ~~(10)~~ as claimed in claim 1, wherein each network station ~~(110, 120, 130, 140)~~ comprises a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port.

10.(Currently Amended) A method of designing an integrated circuit ~~(10)~~ comprising a plurality of functional blocks ~~(101, 102, 103, 104)~~, and a data communication network comprising a plurality of network stations ~~(105-108, 110, 120, 130, 140)~~ being interconnected via a plurality of communication channels ~~(150)~~ for communicating data packages between the functional blocks ~~(101, 102, 103, 104)~~, each data package comprising N data elements including a data element comprising routing information for the network stations ~~(105-108, 110, 120, 130, 140)~~, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers ~~(110, 120, 130, 140)~~ and a plurality of network interfaces ~~(105-108)~~, each of the data routers ~~(110, 120, 130, 140)~~ being coupled to a functional block ~~(101, 102, 103, 104)~~ via a network interface; the method comprising the acts of:

identifying a first communication channel ~~(150)~~ between a first network station ~~(140)~~ and a second network station ~~(120)~~ that has a data transfer delay exceeding a predefined delay threshold; and

inserting $M \times N$ data storage elements ~~(160)~~ into the data communication network ~~(100)~~, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel ~~(150)~~.

11.(Currently Amended) A-The method as claimed in Claim 10, wherein each communication channel ~~(150)~~ comprises a first subchannel ~~(152)~~ between an input port of a first associated network station and ~~and~~ an output port of a second associated network station and a second subchannel ~~(154)~~ between an input port of the second associated network station and ~~and~~ an output port of the first associated network station for enabling duplex communication between the two associated network stations; and

the first network station being arranged to evaluate the routing information in a first cycle and the second network station being arranged to evaluate the routing information in a second cycle, the difference between the first ~~cycle~~ cycle and the second cycle being A cycles, the method further comprising the acts of:

inserting A data storage elements into the first subchannel ~~(152)~~ of the first communication channel ~~(150)~~ for introducing a delay of A cycles onto said first subchannel; and

inserting B data storage elements into the second subchannel ~~(154)~~ of the first communication channel ~~(150)~~ for introducing a delay of B cycles onto said second subchannel; A and B being positive integers, with $A + B = M \cdot N$.

REMARKS

This Amendment is being filed in response to the Office Action mailed July 22, 2010, which has been reviewed and carefully considered. Reconsideration and allowance of the present application in view of the amendments made above and the remarks to follow are respectfully requested.

Claims 1-11 are pending in the Application, where claims 1 and 10 are independent.

Applicants thank the Examiner for acknowledging the receipt and consideration of the Information Disclosure Statement filed on December 20, 2007. Applicants further respectfully request the Examiner to acknowledge the claim for priority and receipt of certified copies of all the priority documents.

By means of the present amendment, the current Abstract has been deleted and substituted with the enclosed New Abstract which better conforms to U.S. practice. Further, the specification has been amended to correct certain informalities.

By means of the present amendment, claims 1-11 have been amended for non-statutory reasons, such as for better form including correcting minor informalities, beginning the dependent claims with 'The' instead of 'A' and deleting reference numerals typically used in European practice that are known to not limit the scope of the claims. Such amendments to claims 1-11 were not made in order to address issues of patentability and Applicant respectfully reserves all rights under the Doctrine of Equivalents.

In the Office Action, the Examiner objected to the drawings because of lack of labels. In response, labels have been added to FIGs 1, 3 and 5. In response, labels have been added to FIGs 1, 3 and 5. Further, FIG 5 has been amended to change a duplicate reference numeral "508" at the right side of FIG 5 to --506--, in conformance with the specification, such as page 15, line 14 of the specification. Replacement sheets including FIGs 1, 3 and 5 are enclosed. Further, an annotated marked-up version of the sheet including FIG 5 is also enclosed for convenience. Applicants respectfully request approval of the enclosed proposed drawing changes and withdrawal of the drawing objection.

In the Office Action, the Examiner indicated that claims 4-5, 7-9 and 11 would be allowable if rewritten in independent form. In addition, claims 1-3, 6 and 10 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 7,362,763 (Wybenga) in view of U.S. Patent No. 7,197,009 (Dispensa). Applicants gratefully acknowledge the indication that claims 4-5, 7-9 and 11 contain allowable subject matter. However, Applicants have not rewritten these claims in independent form, since it is believed that independent claims 1 and 10, as well as claims 2-3 and 6, are allowable over Wybenga and Dispensa for at least the following reasons.

Wybenga is directed to an apparatus and method for classifying traffic in a distributed architecture router. As correctly noted on page 4, last paragraph of the Office Action, Wybenga does not disclose or suggest "M*N data storage elements, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel,"

as recited in independent claim 1, and similarly recited in independent claim 10. Elements 411, 412 of FIG 4 and column 4, lines 63 to column 6, line 10 of Dispensa is cited in an attempt to remedy the deficiencies in Wybenga. This allegation is respectfully traversed.

In particular, column 4, lines 63 to column 6, line 10 of Dispensa specifically recite:
(emphasis added)

Consider the situation where a sequence of packets are received from link 410 and will be transferred over links 411 and 412 to a common destination. If the delay on link 411 is the same as the delay of link 412, then the packets on link 411 will arrive on time and in sequence with the packets on link 412. If the delay on link 411 is much greater than the delay of link 412, then the packets on link 411 will arrive late and out of sequence with the packets on link 412. As discussed above for FIG. 3, packet mis-sequencing causes problems. Empirical studies may be taken to determine a threshold amount of delay variation between links 411 and 412 before mis-sequencing becomes unacceptable. The delay variation is the difference between the delay of link 411 and the delay of link 412. Delay can be measured in bits per second.

It is respectfully submitted that the above noted section of Dispensa merely discusses delay differences between two links 411, 412. Such a disclosure does not disclose or suggest any storage elements, let alone disclosing or suggesting any "network comprising M*N data storage elements, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel," as recited in independent claim 1, and similarly recited in independent claim 10.

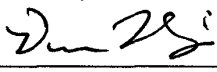
Based on the foregoing, it is respectfully requested that independent claims 1 and 10 be allowed. In addition, it is respectfully submitted that claims 2-3 and 6 should also be allowed at least based on their dependence from independent claims 1 and 10, as well as

their individually patentable elements.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

By 
Dicran Halajian, Reg. 39,703
Attorney for Applicant(s)
October 14, 2010

Enclosure: Replacement drawing sheets (3 sheets including FIGs 1, 3 and 5)
Annotated drawing sheet (1 sheet including FIG 5)

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Please direct all inquiries and correspondence to:

Michael E. Belk, Reg. 33,357
Philips Intellectual Property & Standards
P.O. Box 3001
Briarcliff Manor, NY 10510-8001
(914) 333-9643

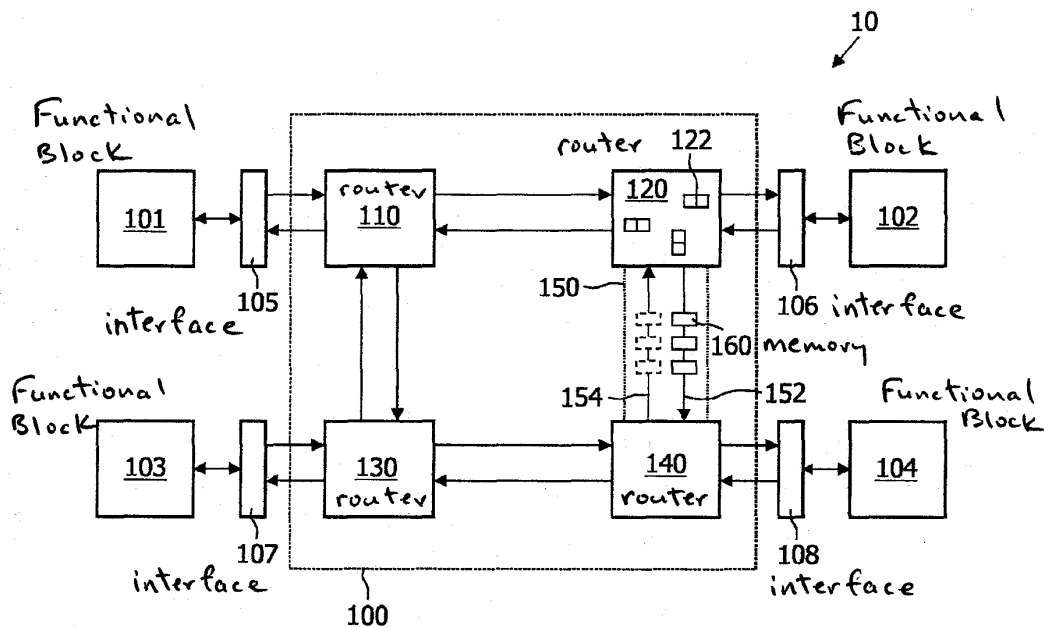


FIG. 1

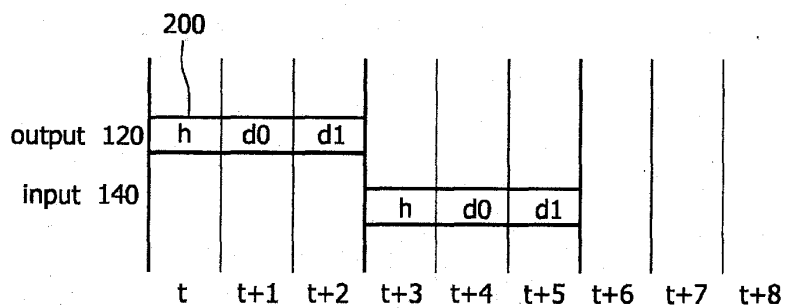
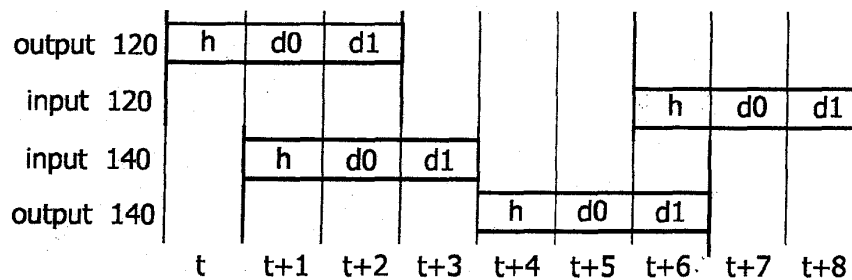
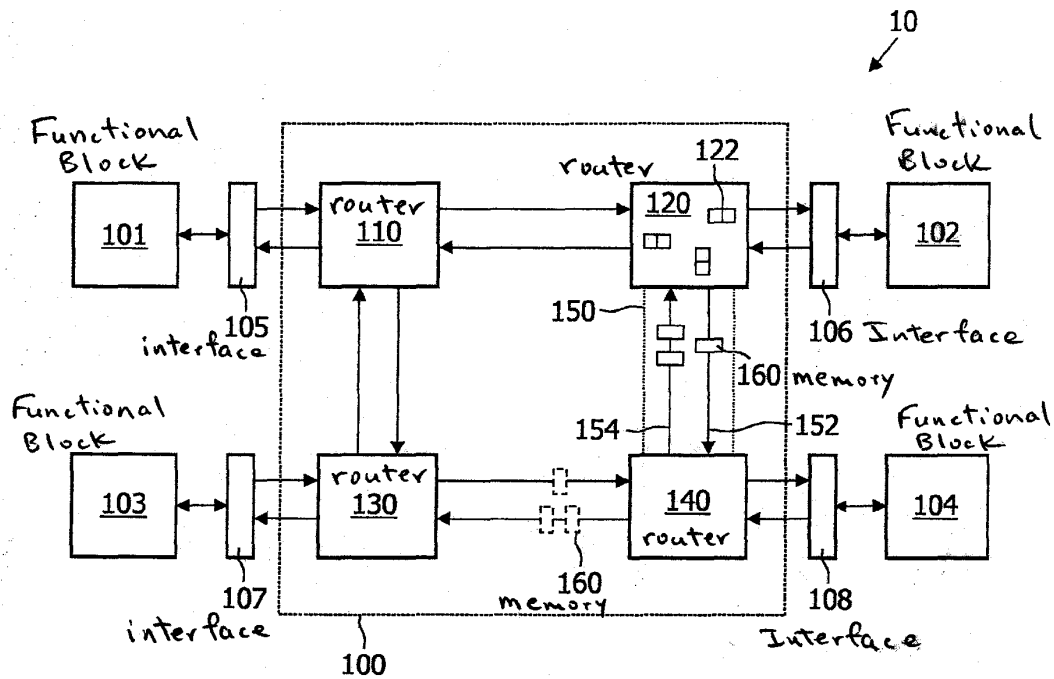


FIG. 2



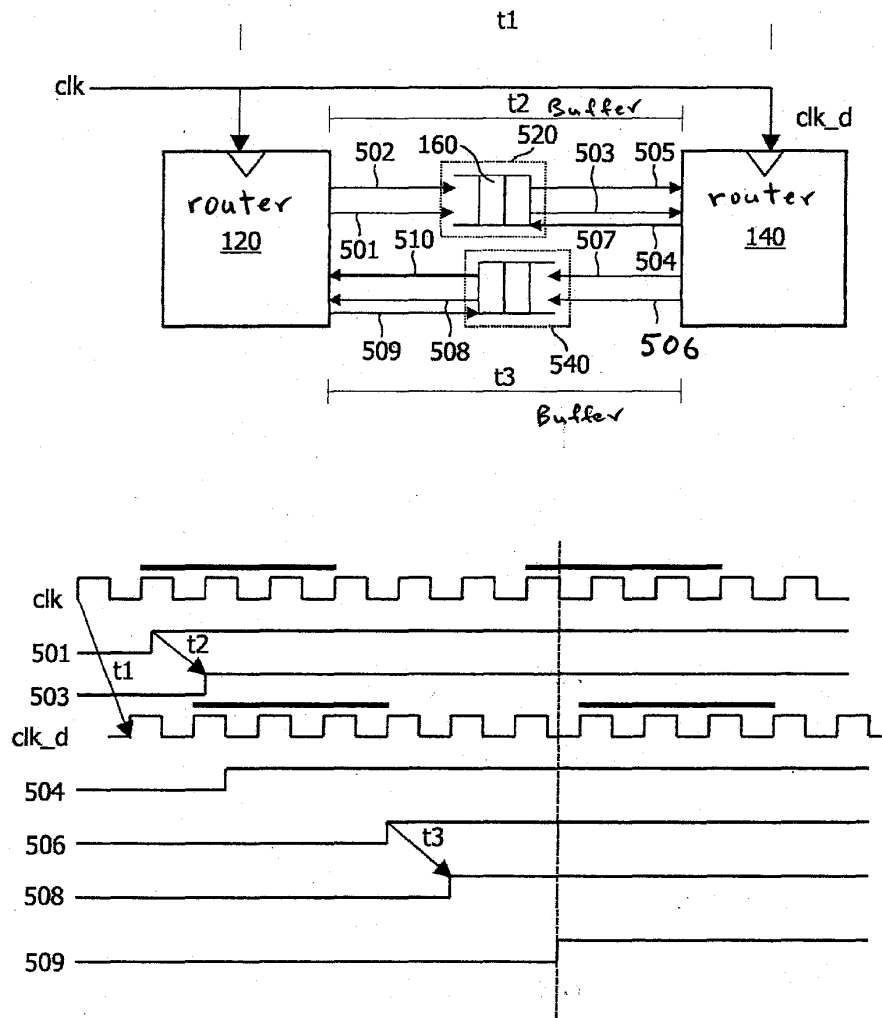


FIG. 5

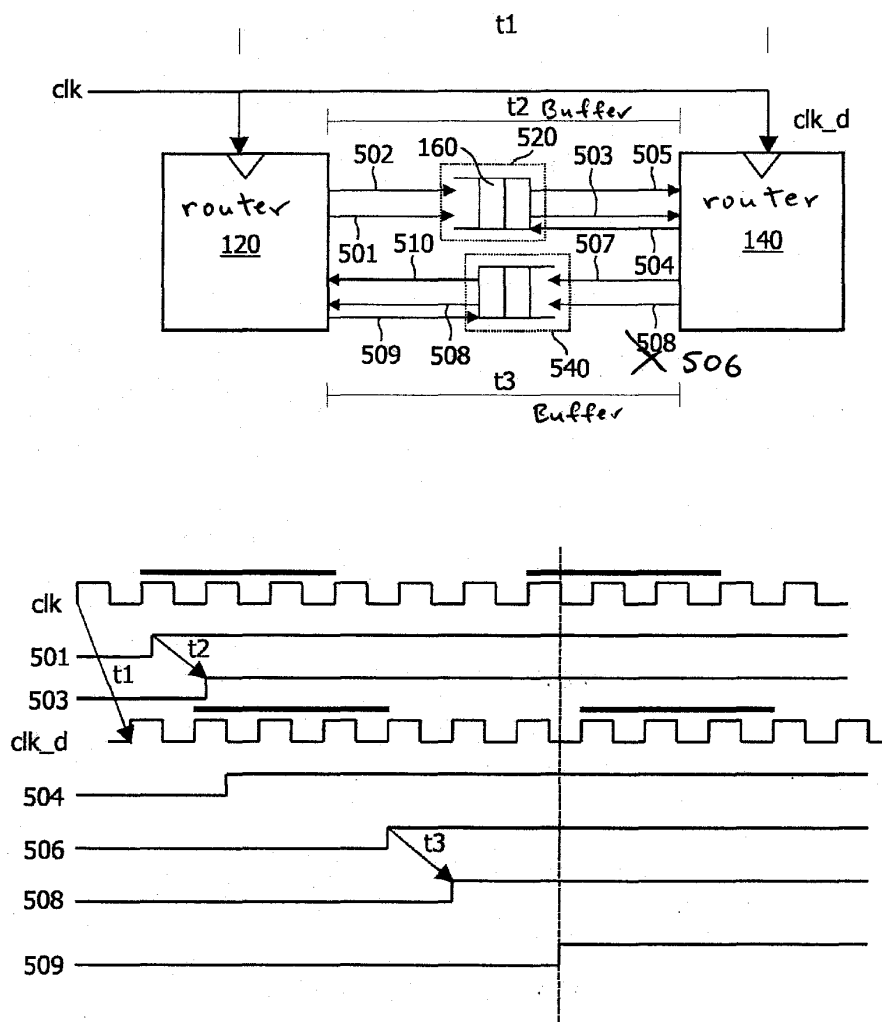


FIG. 5

Electronic Acknowledgement Receipt	
EFS ID:	8636025
Application Number:	11912175
International Application Number:	
Confirmation Number:	5577
Title of Invention:	Integrated Circuit with Data Communication Network and Ic Design Method
First Named Inventor/Applicant Name:	John Dielissen
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	000268 US1
Receipt Date:	15-OCT-2010
Filing Date:	22-OCT-2007
Time Stamp:	14:59:04
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		000268US1_Amd_2010_Oct_15.pdf	649280 ba5dca84228081c3bec14a8911c75f577b8d6537	yes	22

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Drawings-only black and white line drawings	2	2
	Abstract	3	4
	Specification	5	8
	Claims	9	14
	Applicant Arguments/Remarks Made in an Amendment	15	18
	Drawings-only black and white line drawings	19	22
Warnings:			
Information:			
Total Files Size (in bytes):			649280
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/912,175		Filing Date 10/22/2007		☐ To be Mailed	
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APPLICATION AS FILED – PART I						OTHER THAN SMALL ENTITY			
(Column 1)		(Column 2)		SMALL ENTITY ☐		OR		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A		N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A		N/A		N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A		N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		OR	X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		TOTAL				

APPLICATION AS AMENDED – PART II						OTHER THAN SMALL ENTITY					
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	10/15/2010	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)			
Total (37 CFR 1.16(o))	* 11	Minus	** 20	= 0	X \$ =		OR	X \$52=	0		
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$ =		OR	X \$220=	0		
☐ Application Size Fee (37 CFR 1.16(s))							OR				
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR				
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0		

(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)				
Total (37 CFR 1.16(o))	*	Minus	**	X \$ =		OR	X \$ =				
Independent (37 CFR 1.16(h))	*	Minus	***	X \$ =		OR	X \$ =				
☐ Application Size Fee (37 CFR 1.16(s))							OR				
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR				
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE			

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Legal Instrument Examiner:
/EVELYN G. NIMMONS/



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/912,175	10/22/2007	John Dielissen	000268 US1	5577
24737 7590 01/12/2011 PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510			EXAMINER SAM, PHIRIN	
			ART UNIT 2476	PAPER NUMBER
			MAIL DATE 01/12/2011	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/912,175	DIELISSEN ET AL.	
	Examiner	Art Unit	
	PHIRIN SAM	2476	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 15 October 2010.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-3,6 and 8-10 is/are rejected.

7) ☒ Claim(s) 4,5,7 and 11 is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 22 October 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____.
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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 6, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by US 2002/0087716 of Mustafa (hereinafter “Mustafa”).

Regarding amended claims 1 and 6, Mustafa discloses an integrated circuit comprising:

- (a) **a plurality of functional blocks** (see Fig. 3a and 3b, elements 94-97, paragraph [0065], two source data-link devices 94 and 95 in FIG. 3A communicate with the data link device 98 using a data link protocol with the presence of a sub-framing byte in their frame format);
- (b) **a data communication network** (see Fig. 3a and 3b, element 90, paragraph [0065]) comprising **a plurality of network stations** (see Fig. 3a and 3b, elements 98, 93 and 91, 99, paragraph [0065]) **being interconnected via a plurality of communication channels** (see Figs. 3a and 3b, paragraph [0065]) **for communicating data packages between the functional blocks** (see Figs. 3a and 3b, paragraph [0065], two source data-link devices 94 and 95 communicate with the data link device 98 using a data link protocol with the presence of a sub-framing byte in their frame format. The device 98 can prioritize the traffic being received from the device 94 and device 95, and forward the traffic consisted of data link frames through two or more data-link switches in the network 90. Once the data link frames arrive at the destination

devices 96 and 97 the related information contained in the sub-framing byte will be processed and the sub-framing byte will be removed from the data link. The detailed procedure is well explained in the following sections of the preferred embodiment. Before establishing any communication exchange all the end devices involved in the dialogue have to mutually agree upon a pre-defined set of rules required to interpret the bits in the sub-framing byte 115. This "communication understanding" can either be configured statically on each device or a proprietary link control protocol can dynamically exchange the required information to configure this understanding among the participating communication devices. It is not necessary for all the intermediate devices to understand the interpretation of the sub-framing byte(s). Only the participating devices need to know the interpretation. In this regard the intermediate devices 93 and 91 are completely oblivious to the sub-framing byte presence in a passing data link frame and interpret the byte(s) as the part of user data. The data-link frame 115 with the reserved sub-framing byte in it transparently passes through intermediate data-link switches 93 and 91), **each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two** (see Figs. 5 and 6a and 6b, paragraph [0072], typical data link frame 120 which needs to be segmented **into multiple sub-frames (N data elements)**). For illustration purposes, the frame 120 is segmented at a byte boundary Y into two sub-frames, sub-frame #1, 121, and sub-frame #2, 124. Using the following procedure, the frame 120 can be portioned into any number of sub-frames if desired. Each of the two sub-frames described herein carries a partition of original data of the frame 120. Therefore, sub-frame #1, 121 contains the initial d1 data bytes of the frame 120 and the sub-frame #2, 124

carries the remaining portion of data (d2 bytes + original frame CRC (C field)). Each of the segmented sub-frames represents a complete data link frame that can be independently routed from the other sub-frames in a network. The original routing header (RH) and the protocol header (PH) are carried in the sub-frame #1, 121 whereas sub-frame #2, 124 only replicates the routing header necessary for routing the sub-frame through the network. The 7-bit sequence field of the framing byte contains the initial sequence number from the assigned sequence range of the frame service class. Since the sub-frame 121 is NOT the last sub-frame (remaining segment of the frame yet to come) the LS bit in the sub-framing byte is set to 0. Following the sub-framing byte 122 is the sub-frame 2-bytes CRC field 123 which is calculated over the entire sub-frame including the sub-framing byte value. The next sub-frame #2, 124 contains the remaining data bytes plus the original CRC bytes (C field). The 7-bit sequence part of the framing byte in the said sub-frame contains the next incremental sequence number of the service class. Since the sub-frame #2, 124 contains the last segment of the frame 120, the LS bit value is set to 1 in the sub-framing byte. The sub-frame CRC (C2) is calculated over the entire data portion of sub-frame #2, 124 including the s2 and C bytes present in the said sub-frame. A closing flag (7E) follows the sub-frame CRC (C2' field)), **the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces** (see Figs. 3a and 3b or 20a and 20b, elements 98, 93, 91, 99 or 326 and 328, paragraph [0065]), **each of the data router being coupled to a functional block via a network interface** (see Figs. 3a and 3b or 20a and 20b, elements 93 and 91, 98 and 99 or 326 and 328, paragraph [0065], two source data-link devices 94 and 95 in FIG. 3A communicate with the data link device 98 using a data link protocol with

the presence of a sub-framing byte in their frame format. The device 98 can prioritize the traffic being received from the device 94 and device 95, and forward the traffic consisted of data link frames through two or more data-link switches in the network 90), **the data communication network comprising a first network station and a second network station interconnected through a first communication channel** (see Figs. 3a and 3b, elements 98 and 93 are the first network station and elements 91 and 99 are the second network station. They both are coupling by the network link as shown in figures 3a and 3b), **the network comprising M*N data storage elements** (see Figs. 11 and 12, elements 156 and 157, paragraph [0087], the transmission buffer 156 injects the data bytes through a single link 157 to the Network 158. The Network 158 can be any type of data link network to carry the data link frame traffic. The end host 159 interfaced with the network 158 receives the transmitted frames. Since there is only one communication link between the transmission buffer 156 and end host 159 the sequence number of the transmitted sub-frames is always preserved. In this network architecture the system process 155 has access to multiple paths that can simultaneously deliver data traffic to the end host 164. The system processor 155 can deliver the data either through the transmission buffer 156 or transmission buffer 157. The transmission buffer 156 uses the link 158 and via Network 160 delivers the traffic to the end host 164. On the other hand, the transmission buffer forwards the data traffic to the destination host 164 through link 159 and via Network 161), **M being a positive integer, for introducing a delay of M*N cycles on the first communication channel** (see Figs. 11 and 12, paragraphs [0089], [0090], [0092], [0096], [0100], these buffers 156, 157, for buffering sub-frames (N data elements), are provided for delaying the transmission on the link 157 (first

communication channel). The two data segments being carried in two sub-frames should be divided in such a proportion that the trailing bytes (sub-frame CRC and ending flag bytes) of each sub-frame travelling through different networks reach at the end host at the same time. The total delay that a sub-frame consumes to reach from the transmission buffer to the end host is mainly the sum of two factors, serialization delay (S_d) and network delay (N_d). Serialization delay is the amount of time that the line interface takes to put a sub-frame data on the link. Whereas, the network delay represents the time that a sub-frame takes to travel through various switches and access paths to reach to the end host 164. In a typical real world network the access bandwidth of the transmission buffer 156 to link 158 can be quite different than the access bandwidth for the transmission buffer 157 to link 159. Similarly, the network delays experienced by transmitted data-link frames through Network 160 can be significantly different from the Network 161. In addition to different network delays, both networks are subjected to jitter which is unpredictable and varies with time and other network elements).

Regarding amended claim 2, Mustafa discloses wherein each communication channel of the plurality of communication channels comprises a first sub-channel between an input port of a first associated network station and an output port of a second associated network station (see Fig. 13a, paragraphs [0089], [0090]); and a second sub-channel between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations (see Figs. 13a, paragraphs [0089], [0090]).

Regarding amended claim 3, Mustafa discloses wherein the $M \times N$ data storage elements are distributed over the first sub-channel and the second sub-channel of the first communication channel (see Figs. 11, 12, 13a, paragraphs [0088], [0089], [0090]).

Regarding amended claim 9, Mustafa discloses wherein **each network station comprises a first memory element and a second memory element associated with a communication port of said network station** (see Figs. 11 and 12, elements 151-153), **the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port** (see Figs. 11 and 12, element 151, paragraph [0086], the high level system architecture capable of transmitting multi-priority services over a single communication link. Illustrated is the frame processor 150 which delivers the data-link frames in their native format to the respective priority service class buffers 151 to 153. For illustration purpose, the priority hierarchy is assigned in ascending order, i.e., N_1 service being the highest priority and the N_z being the lowest service priority. The system process continuously polls the line interrupt status (Li) of each of the service priority classes. The high state of Li determines which service priority can transfer a single byte of data to the transmission buffer. The Li status of all the service priority classes is control by a System Transmission Policy Algorithm (STPA). The STPA controls the Li status of all the service classes. The STPA can update the line status, Li , if desired, of the service classes with a time resolution equivalent to the transmission time for a single byte on the communication link. In other words, after transmitting a single byte of a frame of any priority service class the STPA can dictate and decide which byte, either belonging to the same priority class or any other

priority class needs to be transmitted next. By implementing this preferred technique the STPA can fully control and manage the transmission of any frame in any priority service class to a resolution equivalent to a single byte of data. The STPA can be used to update the line status, Li, of any service class with a time interval equivalent to the transmission time of one byte or multiple bytes. The frequent updates of line status, Li, of the service classes by SPTA can provide a better bandwidth resolution but may demand a high processing power) and **the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port** (see Figs. 11 and 12, element 152-153, paragraph [0086], the high level system architecture capable of transmitting multi-priority services over a single communication link. Illustrated is the frame processor 150 which delivers the data-link frames in their native format to the respective priority service class buffers 151 to 153. For illustration purpose, the priority hierarchy is assigned in ascending order, i.e., N1 service being the highest priority and the Nz being the lowest service priority. The system process continuously polls the line interrupt status (Li) of each of the service priority classes. The high state of Li determines which service priority can transfer a single byte of data to the transmission buffer. The Li status of all the service priority classes is control by a System Transmission Policy Algorithm (STPA). The SPTA controls the Li status of all the service classes. The SPTA can update the line status, Li, if desired, of the service classes with a time resolution equivalent to the transmission time for a single byte on the communication link. In other words, after transmitting a single byte of a frame of any priority service class the STPA can dictate and decide which byte, either belonging to the same priority class or any other

priority class needs to be transmitted next. By implementing this preferred technique the STPA can fully control and manage the transmission of any frame in any priority service class to a resolution equivalent to a single byte of data. The STPA can be used to update the line status, Li, of any service class with a time interval equivalent to the transmission time of one byte or multiple bytes. The frequent updates of line status, Li, of the service classes by SPTA can provide a better bandwidth resolution but may demand a high processing power).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0087716 of Mustafa (hereinafter “Mustafa”) in view of US 2004/0258099 of Scott et al. (hereinafter “Scott”).

Regarding mended claim 8, Mustafa is silent to disclose the integrated circuit further comprising a clock signal generator, the plurality of network stations and the M*N data storage elements being responsive to the clock signal generator. However, Scott discloses a clock signal generator, the plurality of network stations and the M*N data storage elements being responsive to the clock signal generator (see Figs. 1 and 3, paragraphs [0041], [0085]). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine a clock signal generator, the plurality of network stations and the M*N data storage elements being responsive to the clock signal generator teaching by Scott with Mustafa. The motivation for doing so would have been to provide an improved clock recovery mechanism which better synchronizes the service clock of a TDM transmitter to the service clock at the egress of a packet network read on paragraph [0007]. Therefore, it would have been obvious to combine Scott and Mustafa to obtain the invention as specified in the claim(s).

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0087716 of Mustafa (hereinafter “Mustafa”) in view of US 2004/0193709 of Selvaggi et al. (hereinafter “Selvaggi”).

Regarding amended claim 10, Mustafa discloses a method of designing an integrated circuit comprising

(a) **a plurality of functional blocks** (see Fig. 3a and 3b, elements 94-97, paragraph [0065],

two source data-link devices 94 and 95 in FIG. 3A communicate with the data link device 98 using a data link protocol with the presence of a sub-framing byte in their frame format), **and a data communication network** (see Fig. 3a and 3b, element 90, paragraph [0065]) **comprising a plurality of network stations** (see Fig. 3a and 3b, elements 98, 93 and 91, 99, paragraph [0065]) **being interconnected via a plurality of communication channels** (see Figs. 3a and 3b, paragraph [0065]) **for communicating data packages between the functional blocks** (see Figs. 3a and 3b, paragraph [0065], two source data-link devices 94 and 95 communicate with the data link device 98 using a data link protocol with the presence of a sub-framing byte in their frame format. The device 98 can prioritize the traffic being received from the device 94 and device 95, and forward the traffic consisted of data link frames through two or more data-link switches in the network 90. Once the data link frames arrive at the destination devices 96 and 97 the related information contained in the sub-framing byte will be processed and the sub-framing byte will be removed from the data link. The detailed procedure is well explained in the following sections of the preferred embodiment. Before establishing any communication exchange all the end devices involved in the dialogue have to mutually agree upon a pre-defined set of rules required to interpret the bits in the sub-framing byte 115. This "communication understanding" can either be configured statically on each device or a proprietary link control protocol can dynamically exchange the required information to configure this understanding among the participating communication devices. It is not necessary for all the intermediate devices to understand the interpretation of the sub-framing byte(s). Only the participating devices need to know the interpretation. In this regard the intermediate devices 93 and 91 are completely oblivious to the

sub-framing byte presence in a passing data link frame and interpret the byte(s) as the part of user data. The data-link frame 115 with the reserved sub-framing byte in it transparently passes through intermediate data-link switches 93 and 91), **each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two** (see Figs. 5 and 6a and 6b, paragraph [0072], typical data link frame 120 which needs to be segmented **into multiple sub-frames (N data elements)**). For illustration purposes, the frame 120 is segmented at a byte boundary Y into two sub-frames, sub-frame #1, 121, and sub-frame #2, 124. Using the following procedure, the frame 120 can be portioned into any number of sub-frames if desired. Each of the two sub-frames described herein carries a partition of original data of the frame 120. Therefore, sub-frame #1, 121 contains the initial d1 data bytes of the frame 120 and the sub-frame #2, 124 carries the remaining portion of data (d2 bytes + original frame CRC (C field)). Each of the segmented sub-frames represents a complete data link frame that can be independently routed from the other sub-frames in a network. The original routing header (RH) and the protocol header (PH) are carried in the sub-frame #1, 121 whereas sub-frame #2, 124 only replicates the routing header necessary for routing the sub-frame through the network. The 7-bit sequence field of the framing byte contains the initial sequence number from the assigned sequence range of the frame service class. Since the sub-frame 121 is NOT the last sub-frame (remaining segment of the frame yet to come) the LS bit in the sub-framing byte is set to 0. Following the sub-framing byte 122 is the sub-frame 2-bytes CRC field 123 which is calculated over the entire sub-frame including the sub-framing byte value. The next sub-frame #2, 124 contains the remaining data bytes plus the original CRC bytes

(C field). The 7-bit sequence part of the framing byte in the said sub-frame contains the next incremental sequence number of the service class. Since the sub-frame #2, 124 contains the last segment of the frame 120, the LS bit value is set to 1 in the sub-framing byte. The sub-frame CRC (C2) is calculated over the entire data portion of sub-frame #2, 124 including the s2 and C bytes present in the said sub-frame. A closing flag (7E) follows the sub-frame CRC (C2' field)), **the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces** (see Figs. 3a and 3b or 20a and 20b, elements 98, 93, 91, 99 or 326 and 328, paragraph [0065]), **each of the data router being coupled to a functional block via a network interface** (see Figs. 3a and 3b or 20a and 20b, elements 93 and 91, 98 and 99 or 326 and 328, paragraph [0065], two source data-link devices 94 and 95 in FIG. 3A communicate with the data link device 98 using a data link protocol with the presence of a sub-framing byte in their frame format. The device 98 can prioritize the traffic being received from the device 94 and device 95, and forward the traffic consisted of data link frames through two or more data-link switches in the network 90), the method comprising the acts of:

- (b) **identifying a first communication channel between a first network station and a second network station** (see Figs. 3a and 3b, elements 98 and 93 are the first network station and elements 91 and 99 are the second network station. They both are coupling by the network link as shown in figures 3a and 3b); and
- (c) **inserting M*N data storage elements into the data communication network** (see Figs. 11 and 12, elements 156 and 157, paragraph [0087], the transmission buffer 156 injects the data bytes through a single link 157 to the Network 158. The Network 158 can be any type of

data link network to carry the data link frame traffic. The end host 159 interfaced with the network 158 receives the transmitted frames. Since there is only one communication link between the transmission buffer 156 and end host 159 the sequence number of the transmitted sub-frames is always preserved. In this network architecture the system process 155 has access to multiple paths that can simultaneously deliver data traffic to the end host 164. The system processor 155 can deliver the data either through the transmission buffer 156 or transmission buffer 157. The transmission buffer 156 uses the link 158 and via Network 160 delivers the traffic to the end host 164. On the other hand, the transmission buffer forwards the data traffic to the destination host 164 through link 159 and via Network 161), **M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel** (see Figs. 11 and 12, paragraphs [0089], [0090], [0092], [0096], [0100], these buffers 156, 157, for buffering sub-frames (N data elements), are provided for delaying the transmission on the link 157 (first communication channel). The two data segments being carried in two sub-frames should be divided in such a proportion that the trailing bytes (sub-frame CRC and ending flag bytes) of each sub-frame travelling through different networks reach at the end host at the same time. The total delay that a sub-frame consumes to reach from the transmission buffer to the end host is mainly the sum of two factors, serialization delay (S_d) and network delay (N_d). Serialization delay is the amount of time that the line interface takes to put a sub-frame data on the link. Whereas, the network delay represents the time that a sub-frame takes to travel through various switches and access paths to reach to the end host 164. In a typical real world network the access bandwidth of the transmission buffer 156 to link 158 can be quite different than the access bandwidth for the

transmission buffer 157 to link 159. Similarly, the network delays experienced by transmitted data-link frames through Network 160 can be significantly different from the Network 161. In addition to different network delays, both networks are subjected to jitter which is unpredictable and varies with time and other network elements);

Mustafa is silent to disclose a data transfer delay exceeding a predefined delay threshold. However, Selvaggi discloses a data transfer delay exceeding a predefined delay threshold (see Fig. 2, paragraph [0069]). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine a data transfer delay exceeding a predefined delay threshold teaching by Selvaggi with Mustafa. The motivation for doing so would have been to provide for evaluating network performance read on paragraph [0009]. Therefore, it would have been obvious to combine Selvaggi and Mustafa to obtain the invention as specified in the claim(s).

Allowable Subject Matter

7. Claims 4, 5, 7, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims above have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHIRIN SAM whose telephone number is (571)272-3082. The examiner can normally be reached on Increased Flexitime Policy (IFP) Program.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272 - 3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Respectfully submitted,

Date: January 9, 2011

By: /Phirin Sam/
Phirin Sam
Primary Examiner
Art Unit 2476

Notice of References Cited	Application/Control No. 11/912,175	Applicant(s)/Patent Under Reexamination DIELISSEN ET AL.	
	Examiner PHIRIN SAM	Art Unit 2476	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2002/0087716	07-2002	Mustafa, Shakeel	709/236
*	B	US-2004/0258099	12-2004	Scott et al.	370/503
*	C	US-2004/0193709	09-2004	Selvaggi et al.	709/224
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	103787	routers or (rout\$3 near2 (devices or modules or apparatuses or units))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:09
L2	62239	network\$3 near2 (interfaces or adapters)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:09
L3	4563917	storage\$1 or FIFO\$1 or buffer\$1 or queue\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:09
L4	675874	first near2 (channel or link or path or line)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:09
L5	591764	second near2 (channel or link or path or line)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:09
L6	13913	L1 and L2	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:09
L7	11678	L6 and L3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:09

L8	2979	L7 and L4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:09
L9	1470	L8 and L5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:09
L10	2971	delay\$3 near4 exceed\$3 near4 (predetermin\$7 or threshold\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:11
L11	6	I9 and I10	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:11
L12	50847	370/231-235,351-354,356,389,392,394,395.1,395.21,395.31,400-402,412,413,415,417,503.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L13	459	I12 and I9	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L14	2	I12 and I11	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L15	103787	routers or (rout\$3 near2 (devices or modules or apparatuses or units))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L16	62239	network\$3 near2 (interfaces or adapters)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46

L17	4563917	storage\$1 or FIFO\$1 or buffer\$1 or queue\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L18	675874	first near2 (channel or link or path or line)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L19	591764	second near2 (channel or link or path or line)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L20	13913	L15 and L16	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L21	11678	L20 and L17	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L22	2979	L21 and L18	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L23	1470	L22 and L19	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L24	134207	delay\$3 near3 (channel or link or path or line)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46
L25	207	L23 and L24	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:46

L26	103787	routers or (rout\$3 near2 (devices or modules or apparatuses or units))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L27	62239	network\$3 near2 (interfaces or adapters)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L28	4563917	storage\$1 or FIFO\$1 or buffer\$1 or queue\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L29	675874	first near2 (channel or link or path or line)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L30	591764	second near2 (channel or link or path or line)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L31	13913	L26 and L27	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L32	11678	L31 and L28	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L33	2979	L32 and L29	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L34	1470	L33 and L30	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47

L35	144	L34 and (clock near3 generat\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L36	134207	delay\$3 near3 (channel or link or path or line)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L37	56	L35 and L36	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:47
L38	6	I37 and I12	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:49
L39	39	I35 and I12	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2011/01/09 21:49

EAST Search History (Interference)

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1/9/2011 9:52:56 PM**C:\Documents and Settings\psam\My Documents\EAST\Workspaces\ Template EAST.wsp**

<i>Index of Claims</i> 	Application/Control No. 11912175	Applicant(s)/Patent Under Reexamination DIELISSSEN ET AL.
	Examiner PHIRIN SAM	Art Unit 2476

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	07/19/2010	01/09/2011						
	1	✓	✓						
	2	✓	✓						
	3	✓	✓						
	4	O	O						
	5	O	O						
	6	✓	✓						
	7	O	O						
	8	O	✓						
	9	O	✓						
	10	✓	✓						
	11	O	O						

<i>Search Notes</i> 	Application/Control No. 11912175	Applicant(s)/Patent Under Reexamination DIELISSEN ET AL.
	Examiner PHIRIN SAM	Art Unit 2476

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
370/231-235,351-354,356,389,392,394,395.1,395.21,395.31,400-402,412,413,415,417 (Text search - See text search history printout).	07/19/2010	PS
370/231-235,351-354,356,389,392,394,395.1,395.21,395.31,400-402,412,413,415,417,503 (Text search - See text history printout).	01/09/2011	PS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/PHIRIN SAM/ Acting Examiner.Art Unit 2419/2400	
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PATENT
Serial No. 11//912,175
Reply to Office Action of January 12, 2011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
John DIELISSSEN; et al.

Atty. Docket: 000268US1

Confirmation No. 5577

Serial No. 11/912,175

Group Art Unit: 2476

Filed: October 22, 2007

Examiner: SAM, Phirin

Title: INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC
DESIGN METHOD

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action mailed on January 12, 2011, please amend the
above-identified application and consider the remarks as follows:

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) An integrated circuit comprising:
a plurality of functional blocks; and
a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, the data communication network comprising a first network station and a second network station interconnected through a first communication channel , the data communication network further comprising M*N data storage elements, M being a positive integer, ~~for the data communication~~ introducing a delay of M*N cycles on the first communication channel when the data communication network identifies the first

communication channel as having a data transfer delay exceeding a predefined delay threshold.

2.(Previously Presented) The integrated circuit as claimed in Claim 1, wherein each communication channel of the plurality of communication channels comprises:

a first subchannel between an input port of a first associated network station and an output port of a second associated network station; and

a second subchannel between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations.

3.(Previously Presented) The integrated circuit as claimed in Claim 2, wherein the M*N data storage elements are distributed over the first subchannel and the second subchannel of the first communication channel.

4.(Currently Amended) ~~The integrated circuit as claimed in claim 3, wherein:~~ An integrated circuit comprising:

a plurality of functional blocks; and

a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages

between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, the data communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication network further comprising $M \times N$ data storage elements, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel,

wherein each communication channel of the plurality of communication channels comprises:

a first subchannel between an input port of a first associated network station and an output port of a second associated network station; and

a second subchannel between an input port of the second associated network station and an output port of the first associated network station, and

wherein the first network station is arranged to evaluate the routing information in a first cycle and the second network station is arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles; and

the first subchannel of the first communication channel exhibits a delay of A cycles implemented by A data storage elements and the second subchannel exhibits a delay of B

cycles implemented by B data storage elements, A and B being positive integers, with $A + B = M \cdot N$.

5.(Previously Presented) The integrated circuit as claimed in claim 4, wherein any network path from a further network station being arranged to evaluate the routing information in the second cycle to the first network station comprises C delay elements, C being a positive integer with C modulo $N = A$; and any network path to the further network station from the first network station comprises D delay elements; D being a positive integer with D modulo $N = B$.

6.(Previously Presented) The integrated circuit as claimed in Claim 1, wherein $M = 1$.

7.(Currently Amended) ~~The integrated circuit as claimed in Claim 3,~~ An integrated circuit comprising:
a plurality of functional blocks; and
a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of

at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, the data communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication network further comprising $M*N$ data storage elements, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel,
wherein each communication channel of the plurality of communication channels comprises:

a first subchannel between an input port of a first associated network station and an output port of a second associated network station; and

a second subchannel between an input port of the second associated network station and an output port of the first associated network station, and

wherein the first subchannel and the second subchannel of the first communication channel each comprise a delay introduced by $\frac{1}{2}*M*N$ data storage elements .

8.(Previously Presented) The integrated circuit as claimed in Claim 1, further comprising a clock signal generator, the plurality of network stations and the $M*N$ data storage elements being responsive to the clock signal generator.

9.(Previously Presented d) The integrated circuit as claimed in claim 1, wherein

each network station comprises a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port.

10.(Currently Amended) A method of designing an integrated circuit comprising a plurality of functional blocks, and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface; the method comprising the acts of:

identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and

in response to the identifying act, inserting $M \times N$ data storage elements into the data

communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel.

11.(Currently Amended) ~~The method as claimed in Claim 10~~ A method of designing an integrated circuit comprising a plurality of functional blocks, and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface; the method comprising the acts of:

identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and

inserting $M*N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel,

wherein each communication channel comprises a first subchannel between an input port of a first associated network station and an output port of a second associated network station and a second subchannel between an input port of the second associated

network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations; and

the first network station being arranged to evaluate the routing information in a first cycle and the second network station being arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles, the method further comprising the acts of:

inserting A data storage elements into the first subchannel of the first communication channel for introducing a delay of A cycles onto said first subchannel; and

inserting B data storage elements into the second subchannel of the first communication channel for introducing a delay of B cycles onto said second subchannel; A and B being positive integers, with $A + B = M \cdot N$.

12.(New) The integrated circuit of claim 4, wherein the $M \cdot N$ data storage elements are distributed over the first subchannel and the second subchannel of the first communication channel.

REMARKS

This Amendment is being filed in response to the Office Action mailed January 12, 2011, which has been reviewed and carefully considered. Reconsideration and allowance of the present application in view of the amendments made above and the remarks to follow are respectfully requested.

Claims 1-12 are pending in the Application, where claims 1, 4, 7, 10 and 11 are independent.

In the Office Action, the Examiner indicated that claims 4, 5, 7 and 11 would be allowable if rewritten in independent form. Applicants gratefully acknowledge the indication that claims 4, 5, 7 and 11 contain allowable subject matter. By means of the present amendment, claims 4, 7 and 11 have been rewritten in independent form without including certain features that are believed to be not necessary for patentability. Accordingly, it is respectfully requested that independent claims 4, 7 and 11 be allowed. In addition, it is respectfully requested that claim 5 also be allowed at least based on its dependence from independent claim 4 as well as its individually patentable elements.

In the Office Action, claims 1-3, 6 and 9 are rejected under 35 U.S.C. §102(b) over U.S. Patent Application Publication No. 2002/0087716 (Mustafa). Further, claim 8 is rejected under 35 U.S.C. §103(a) over Mustafa in view of U.S. Patent Application Publication No. 2004/0258099 (Scott). Claim 10 is rejected under 35 U.S.C. §103(a) over

Mustafa in view of U.S. Patent Application Publication No. 2004/0193709 (Selvaggi).

These rejections are respectfully traversed. It is respectfully submitted that claims 1-3, 6 and 8-10 are allowable over Mustafa, Scott and Selvaggi for at least the following reasons.

Mustafa is directed to a system and method to simultaneously support a customized multi-priority services. As shown in FIGs 11-12, transmission buffers 156, 157 are provided for storing active frame data. Transmission buffers 156, 157 are always provided between a system processor 156 and networks 1, 2, also referred to by reference numeral 160, 161 in FIG 12. As correctly noted on page 15, first full paragraph, Mustafa does not disclose or suggest any "data transfer delay exceeding a predefined delay threshold." Selvaggi is cited in an attempt to remedy the deficiencies in Mustafa.

Selvaggi is directed to methods, systems and computer program products for evaluating network performance. Paragraph [0069], lines 1-5 of Selvaggi (referred to on page 15 of the Office Action) recites: (emphasis added)

Ones of the plurality of rules set out below may be dependent on satisfying certain performance and/or configuration criteria. Performance criteria as used herein refers to data that may indicate network performance, for example, delays exceeding a predetermined threshold.

It is respectfully submitted that Mustafa, Selvaggi, and combination thereof, do not disclose or suggest the present invention as recited in independent claim 1, and similarly recited in independent claim 10 which, amongst other patentable elements, recites (illustrative emphasis provided):

the data communication introducing a delay of M*N cycles on the

first communication channel when the data communication network **identifies** the first communication channel as having a data transfer delay exceeding a predefined delay threshold.

It is respectfully submitted that Mustafa and Selvaggi, alone or in combination, do not disclose or suggest introducing any delay, let alone introducing the particular delay of M*N cycles on the first communication channel, when the data communication network **identifies** the first communication channel as having a data transfer delay exceeding a predefined delay threshold, as recited in independent claim 1; or in response to identifying that the first communication channel has a data transfer delay exceeding a predefined delay threshold,, inserting M*N data storage elements into the data communication network for introducing a delay of M*N cycles on the first communication channel, as recited in independent claim 10. Scott is cited to allegedly show other features and does not remedy the deficiencies in Mustafa and Selvaggi

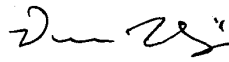
Based on the foregoing, it is respectfully requested that independent claims 1 and 10 be allowed. In addition, it is respectfully submitted that claims 2-3, 6 and 8-9 should also be allowed at least based on their dependence from independent claim 1, as well as their individually patentable elements.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, Applicants reserve the right to submit further arguments in support of

the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

By 
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March 23, 2011

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P.O. Box 3001
Briarcliff Manor, NY 10510-8001
(914) 333-9643

Electronic Acknowledgement Receipt	
EFS ID:	9857664
Application Number:	11912175
International Application Number:	
Confirmation Number:	5577
Title of Invention:	Integrated Circuit with Data Communication Network and Ic Design Method
First Named Inventor/Applicant Name:	John Dielissen
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	000268 US1
Receipt Date:	12-APR-2011
Filing Date:	22-OCT-2007
Time Stamp:	08:19:39
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		000268US1US1_Amd_2011_Ap r_12.pdf	499225 ccced9d6219784d0760738c319aa34e6d4f cddd9	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	9
	Applicant Arguments/Remarks Made in an Amendment	10	13
Warnings:			
Information:			
Total Files Size (in bytes):		499225	
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/912,175		Filing Date 10/22/2007		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	04/12/2011	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(i))	*	12	Minus	** 20	=	0	OR	X \$2=	0	
Independent (37 CFR 1.16(h))	*	5	Minus	***3	=	2	OR	X \$220=	440	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	440	
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(i))	*		Minus	**	=		OR	X \$ =		
Independent (37 CFR 1.16(h))	*		Minus	***	=		OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.										
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".										
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".										
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Legal Instrument Examiner:
/FREDERICK E. BRISCOE/



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NOTICE OF ALLOWANCE AND FEE(S) DUE

24737 7590 08/08/2011
PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER

SAM, PHIRIN

ART UNIT

PAPER NUMBER

2476

DATE MAILED: 08/08/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/912,175	10/22/2007	John Dielissen	000268 US1	5577

TITLE OF INVENTION: INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/08/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

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If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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BRIARCLIFF MANOR, NY 10510

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/912,175	10/22/2007	John Dielissen	000268 US1	5577
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TITLE OF INVENTION: INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/08/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
SAM, PHIRIN	2476	370-400000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

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☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

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Date _____

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/912,175	10/22/2007	John Dielissen	000268 US1	5577
24737	7590	08/08/2011	EXAMINER	
PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510			SAM, PHIRIN	
			ART UNIT	PAPER NUMBER
			2476	

DATE MAILED: 08/08/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 577 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 577 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DETAILED ACTION

Allowable Subject Matter

1. The following is an examiner's statement of reasons for allowance:

Regarding amended claim 1 and claims 2, 3, 6, 8, 9, the prior arts of record do not disclose a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, the data communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication network further comprising $M*N$ data storage elements, M being a positive integer, the data communication introducing a delay of $M*N$ cycles on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold.

Regarding amended claim 4 and claims 5, 12, the prior arts of record do not disclose a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, the data

communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication network further comprising $M*N$ data storage elements, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel, wherein each communication channel of the plurality of communication channels comprises a first subchannel between an input port of a first associated network station and an output port of a second associated network station; and a second subchannel between an input port of the second associated network station and an output port of the first associated network station, and wherein the first network station is arranged to evaluate the routing information in a first cycle and the second network station is arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles; and the first subchannel of the first communication channel exhibits a delay of A cycles implemented by A data storage elements and the second subchannel exhibits a delay of B cycles implemented by B data storage elements, A and B being positive integers, with $A + B = M*N$.

Regarding amended claim 7, the prior arts of record do not disclose a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, the data communication network comprising a first network station and a second network station interconnected through a first communication channel, the data communication network further

comprising $M*N$ data storage elements, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel, wherein each communication channel of the plurality of communication channels comprises a first subchannel between an input port of a first associated network station and an output port of a second associated network station; and a second subchannel between an input port of the second associated network station and an output port of the first associated network station, and wherein the first subchannel and the second subchannel of the first communication channel each comprise a delay introduced by $\frac{1}{2}*M*N$ data storage elements.

Regarding amended claim 10, the prior arts of record do not disclose data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface; the method comprising the acts of identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and in response to the identifying act, inserting $M*N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel.

Regarding amended claim 11, the prior arts of record do not disclose identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and inserting $M*N$ data storage

Art Unit: 2476

elements into the data communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel, wherein each communication channel comprises a first subchannel between an input port of a first associated network station and an output port of a second associated network station and a second subchannel between an input port of the second associated network station and an output port of the first associated network station for enabling duplex communication between the two associated network stations; and the first network station being arranged to evaluate the routing information in a first cycle and the second network station being arranged to evaluate the routing information in a second cycle, the difference between the first cycle and the second cycle being A cycles, the method further comprising the acts of: inserting A data storage elements into the first subchannel of the first communication channel for introducing a delay of A cycles onto said first subchannel; and inserting B data storage elements into the second subchannel of the first communication channel for introducing a delay of B cycles onto said second subchannel; A and B being positive integers, with $A + B = M*N$.

Conclusion

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(1) US 2004/0193709 of Selvaggi et al. discloses evaluating network performance using diagnostic rules.

(2) US Patent 6,466,548 to Fitzgerald discloses hop by hop quality of service measurement system.

(3) US 2004/0252701 of Anandakumar et al. discloses systems, process and integrated circuits for rate and/or diversity adaptation for packet communications.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHIRIN SAM whose telephone number is (571)272-3082. The examiner can normally be reached on Flexible Work Schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Respectfully submitted,

Date: July 31, 2011

By: /Phirin Sam/
Phirin Sam
Primary Examiner
Art Unit 2476

Notice of References Cited	Application/Control No. 11/912,175	Applicant(s)/Patent Under Reexamination DIELISSEN ET AL.	
	Examiner PHIRIN SAM	Art Unit 2476	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2004/0193709	09-2004	Selvaggi et al.	709/224
*	B	US-6,466,548	10-2002	Fitzgerald, Cary W.	370/249
*	C	US-2004/0252701	12-2004	Anandakumar et al.	370/395.21
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 11912175	Applicant(s)/Patent Under Reexamination DIELISSSEN ET AL.
	Examiner PHIRIN SAM	Art Unit 2476

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant					☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE								
Final	Original	07/19/2010	01/09/2011	07/31/2011						
	1	✓	✓	=						
	2	✓	✓	=						
	3	✓	✓	=						
	4	O	O	=						
	5	O	O	=						
	6	✓	✓	=						
	7	O	O	=						
	8	O	✓	=						
	9	O	✓	=						
	10	✓	✓	=						
	11	O	O	=						
	12			=						

Search Notes 	Application/Control No. 11912175	Applicant(s)/Patent Under Reexamination DIELISSEN ET AL.
	Examiner PHIRIN SAM	Art Unit 2476

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
370/231-235,351-354,356,389,392,394,395.1,395.21,395.31,400-402,412,413,415,417 (Text search - See text search history printout).	07/19/2010	PS
370/231-235,351-354,356,389,392,394,395.1,395.21,395.31,400-402,412,413,415,417,503 (Text search - See text history printout).	01/09/2011	PS
370/231-235,242,244,247,248,250,251,252,253,254,351-354,356,386,389,92,394,395.1,395.21,395.31,400-405,412,413,415,417,419,465,503,508,516,517,519 (Text search - See text search history printout).	07/31/2011	PS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	See text search history printout for interference.	07/31/2011	PS

/PHIRIN SAM/ Acting Examiner.Art Unit 2419/2400	
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Issue Classification 	Application/Control No. 11912175	Applicant(s)/Patent Under Reexamination DIELISSSEN ET AL.
	Examiner PHIRIN SAM	Art Unit 2476

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
370		252				G	0	1	R	31 / 08 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
370	351																	

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE		Total Claims Allowed:	
		12	
(Assistant Examiner) /PHIRIN SAM/ Primary Examiner. Art Unit 2476	(Date) 07/31/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1893484	(process\$3 or source\$1) near2 (device\$1 or unit\$1 or node\$1 or terminal\$1 or apparatus)	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:15
L2	247191	(rout\$3 near2 (device\$1 or unit\$1 or node\$1 or apparatus)) or router\$1	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:16
L3	80651	network\$3 near3 station\$1	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:19
L4	283354	network near3 interfac\$3	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:20
L5	3680024	storag\$3 or (stor\$4 near2 (device\$1 or unit\$1 or element\$1 or apparatus)) or buffer\$3	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:37
L6	1244757	delay\$\$3	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:39

L7	155814	I1 and I2	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:39
L8	12703	I7 and I3	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:39
L9	7077	I8 and I4	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:39
L10	6161	I9 and I5	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:39
L11	3023	I10 and I6	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:39
L12	2934	delay\$3 near4 exceed\$3 near4 (pre\$1defin\$3 or threshold or pre\$1determin\$6)	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:40
L13	32	I11 and I12	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:40

L14	79365	I7 and I4	US- PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:56
L15	73501	I14 and I5	US- PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:57
L16	121	I15 and I12	US- PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 11:57
L17	64675	370/ 231-235,242,244,247,248,250,253,254,351- 354,356,386,389,392,394,395.1,395.21,395.31,400- 405,412,413,415,417,419,465,503.ccls.	US- PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 14:07
L18	24	I17 and I16	US- PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 14:08
L19	5	I17 and I13	US- PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 14:08
L20	71813	370/ 231-235,242,244,247,248,250,251,252,253,254,351- 354,356,386,389,392,394,395.1,395.21,395.31,400- 405,412,413,415,417,419,465,503,508,516,517,519.ccls.	US- PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 15:56

L21	31	l20 and l16	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 15:56
L25	8	((storag\$3 or (stor\$4 near2 (device\$1 or unit\$1 or element\$1 or apparatus)) or buffer\$3 or queu\$3) same (first adj2 (channel or link\$3 or line\$1 or path\$1)) same delay\$3 same exceed\$3 same (pre\$1defin\$3 or threshold or pre\$1determin\$6)).clm.	US-PGPUB; USPAT; USOCR; JPO	OR	OFF	2011/07/31 16:49

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L26	8	((storag\$3 or (stor\$4 near2 (device\$1 or unit\$1 or element\$1 or apparatus)) or buffer\$3 or queu\$3) same (first adj2 (channel or link\$3 or line\$1 or path\$1)) same delay\$3 same exceed\$3 same (pre\$1defin\$3 or threshold or pre\$1determin\$6)).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2011/07/31 16:52

7/31/2011 4:54:19 PM

C:\Documents and Settings\psam\My Documents\EAST\Workspaces\370Search.wsp

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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24737 7590 08/08/2011
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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/912,175	10/22/2007	John Dielissen	000268 US1	5577
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TITLE OF INVENTION: INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	11/08/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
SAM, PHIRIN	2476	370-400000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____ (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Koninklijke Philips Electronics N.V. Eindhoven, The Netherlands

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 14-1270. (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Michael E. Belk/

Date October 31, 2011

Typed or printed name Michael E. Belk

Registration No. 33,357

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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1/3

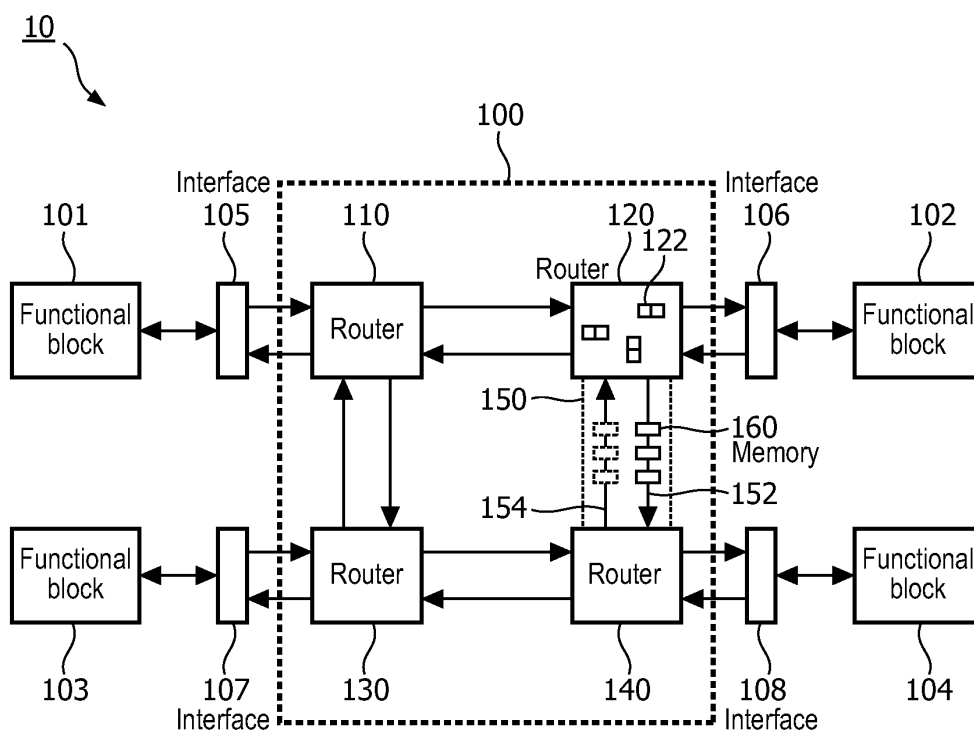


FIG. 1

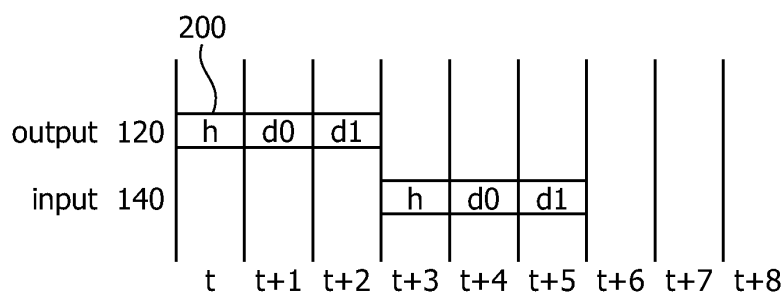


FIG. 2

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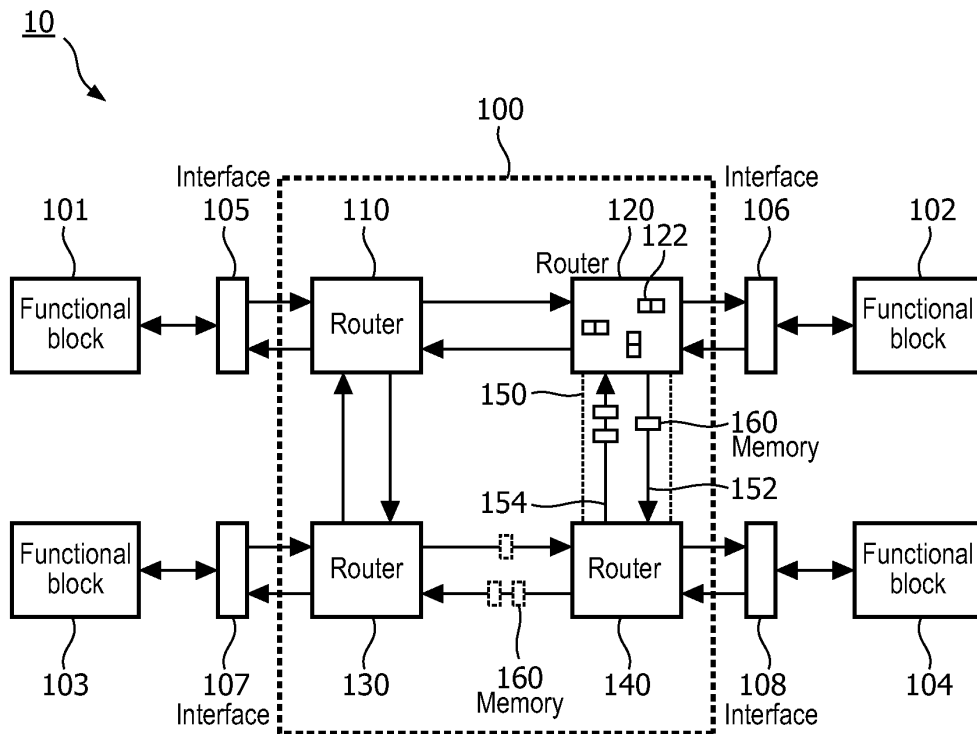


FIG. 3

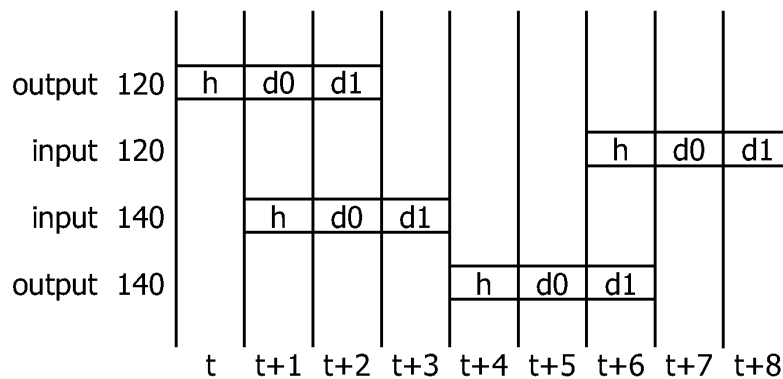


FIG. 4

3/3

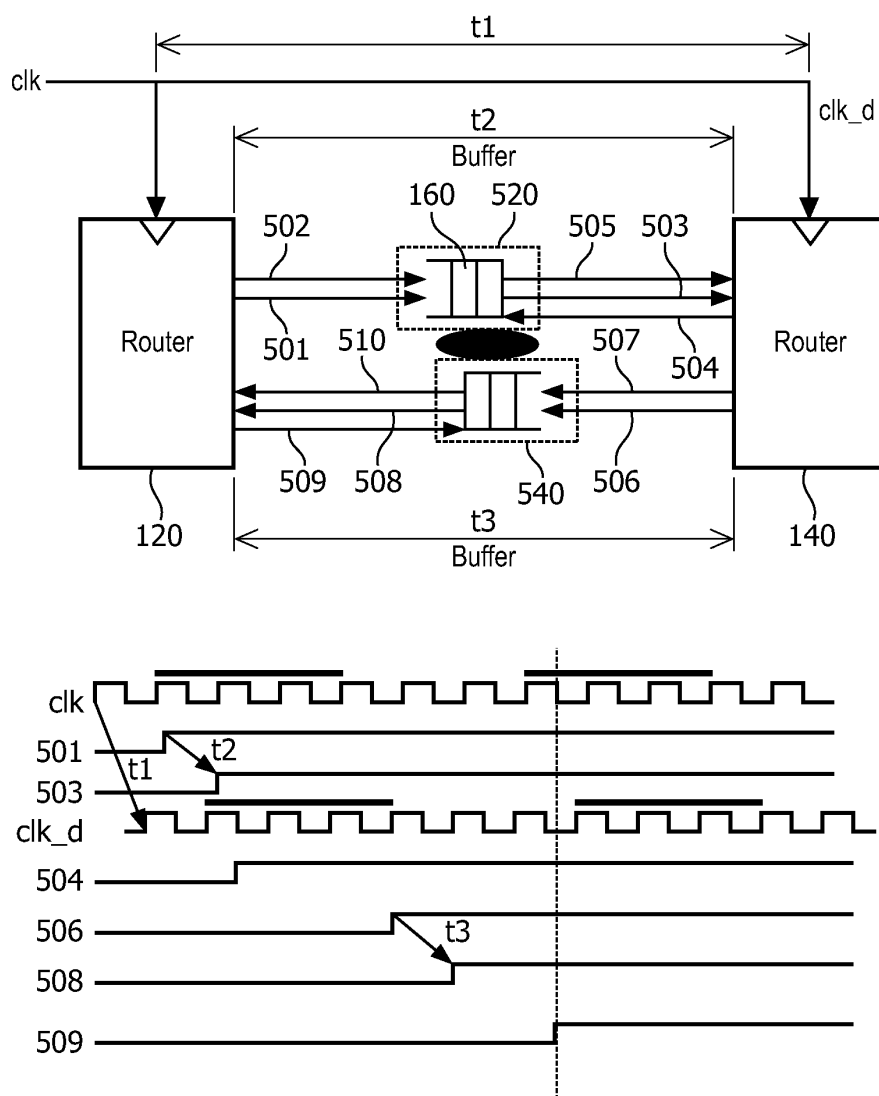


FIG. 5

Electronic Patent Application Fee Transmittal				
Application Number:	11912175			
Filing Date:	22-Oct-2007			
Title of Invention:	INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD			
First Named Inventor/Applicant Name:	John Dielissen			
Filer:	Michael E. Belk/Elissa DeLuccy			
Attorney Docket Number:	2005P00807WOUS			
Filed as Large Entity				
U.S. National Stage under 35 USC 371 Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2040

Electronic Acknowledgement Receipt	
EFS ID:	11306805
Application Number:	11912175
International Application Number:	
Confirmation Number:	5577
Title of Invention:	INTEGRATED CIRCUIT WITH DATA COMMUNICATION NETWORK AND IC DESIGN METHOD
First Named Inventor/Applicant Name:	John Dielissen
Customer Number:	24737
Filer:	Michael E. Belk/Elissa DeLuccy
Filer Authorized By:	Michael E. Belk
Attorney Docket Number:	2005P00807WOUS
Receipt Date:	01-NOV-2011
Filing Date:	22-OCT-2007
Time Stamp:	08:23:48
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$2040
RAM confirmation Number	7111
Deposit Account	141270
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2005P00807WOUS_IF.pdf	104571	no	1
			f6ef20f8eaa4ec45e43e9290c59560cd60bf1f0e		
Warnings:					
Information:					
2	Drawings-only black and white line drawings	2005PF00807_Drawings.pdf	18758	no	3
			00b539db7c45a48be6ef89dc5356da0d94b6fa0e		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	32290	no	2
			f7a81fdc4531e369befa85580d131f21b990d485		
Warnings:					
Information:					
Total Files Size (in bytes):			155619		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

element d2-d1 and $T = t+3$, i.e., after the data router 140 has received the complete data package, the data router 140 sends the first data element of the data package to the data router 140-120 via the second subchannel 154. Due to the presence of two data storage elements 160 on the second subchannel 154, the first data element h is received by the data router 120 at $T = t+6$, i.e. during a cycle at which the data router 120 is scheduled to evaluate the routing information, with the other two data elements ~~d1 and d2~~ d0 and d1 respectively arriving at the subsequent cycles $t+7$ and $t+8$. It will be recognized that the data storage elements 160 in the subchannels 152 and 154 operate as phase shifters to ensure that routing information is evaluated at the right time in each data router phase domain. The application of phase shifting techniques has the advantage that the delay introduced on the individual subchannels 152, 154 can be less than a full data package, thus improving the performance of the slow communication channel 150 compared to the solution presented in Fig. 1.

29

Change(s) applied
to document,

/S.M./
9/2/2011

Replace the paragraph spanning pages 14-15, between page 14, line 28, and page 15, line 16 of the specification with the following:

A communication of a data package from data router 120 to FIFO buffer 520 is initiated by a handshake validation signal 501 followed by synchronous data communication 502 of the data elements of a data package having size N; this communication is governed by data router 120, which is responsive to clock signal CLK.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/912,175	12/06/2011	8072893	2005P00807WOUS	5577

24737 7590 11/16/2011
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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 951 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

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