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## 2 Silicon IP Results for "Concepts and Implementation of the Philips Network-on-Chip"

### [High speed NoC \(Network On-Chip\) Interconnect IP](#)

OPENEDGES is the only total memory system IP company providing both memory controller and on-chip interconnect. OIC is the ORBIT high-speed On-chip Interconnect, which delivers exceptional performance and SoC design flexibility based on automated end-to-end interconnect generation flow. Together with ...

### [I2C Bus Master Controller Core](#)

The I2C-MS core is a controller for the Inter-Integrated Circuit (I2C) bus. The highly configurable core can implement an I2C bus master, slave, or a combined master and slave, and it communicates with the host via an APB, AHB, or Wishbone slave interface. The core supports all variations and configurations ...

## 80 Verification IP Results for "Concepts and Implementation of the Philips Network-on-Chip"

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### [I2C VMM Enabled Verification IP](#)

eInfochips' I2C VMM based VIP is highly configurable, reusable, scalable and extensible verification intellectual property that is suitable for verification of I2C Master/ Slave.

### [SDIO HOST VMM based Verification IP](#)

The Secure Digital Input Output (SDIO) interface is a card interface defined to connect a SD Host Controller with four different types of cards, namely SDIO card, SD memory card, SD Combo card and SD Multimedia Card (MMC). SDIO is a master-slave protocol, where SD Host Controller, as a master, performs ...

### [Verification IP I2C](#)

UST Global VIP for I2C provides a comprehensive set of verification, methodology and protocol features, thus enabling designers to achieve a faster convergence & closure of I2C designs. I2C VIP is implemented in System Verilog and UVM and is capable of running on all standard simulators. The VIP ...

### [I2C Verification IP](#)

The I2C Verification IP provides an effective & efficient way to verify the components interfacing with I2C interface of an ASIC/FPGA or SoC. The I2C VIP is fully compliant with revision 03 of I2C specifications from Philips. This VIP is a light weight VIP with easy plug-and-play interface so that ...

### [DDR5 Memory Model](#)

DDR5 Memory Model provides an smart way to verify the DDR5 component of a SOC or a ASIC. The SmartDV's DDR5 memory model is fully compliant with standard DDR5 Specification and provides the following features. Better than Denali Memory Models.

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## 1 Article Results for "Concepts and Implementation of the Philips Network-on-Chip"

### [Concepts and Implementation of the Philips Network-on-Chip](#)

Jan. 16, 2004 - Concepts and Implementation of the Philips Network-on-Chip

## 8 News Results for "Concepts and Implementation of the Philips Network-on-Chip"

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#### [Imec, Holst Centre and Barco Silex Collaborate on Data Security for Wearables and Internet of Things Networks](#)

May. 25, 2016 - The world-leading nanoelectronics research center imec, Holst Centre (set up by imec and TNO) and micro-electronic design house Barco Silex, belonging to the Barco group, today announced that they will collaborate to implement data security into sensors for wearable devices and Internet of Things (IoT) ...

#### [DECOMSYS Licenses FlexRay IP Proven in Freescale MFR4300 Chip From IPextreme](#)

Nov. 30, 2006 - The FRCC2100 was designed by Freescale and is sold and supported by IPextreme. It is silicon proven in several other Freescale devices including the MC9S12XFR128 16-bit S12 controller and the MPC55xx Power Architecture controllers

#### [Multiple processors mean multiple challenges](#)

Sep. 19, 2005 - While a performance boost can be achieved by adding many processors to a system-on-chip, designers must be prepared to tackle the related speed bumps of software and hardware design

#### [Arteris introduces industry's first products for building networks on Chip \(NoC\)](#)

Mar. 14, 2005 - Arteris introduces industry's first products for building networks on Chip (NoC)

#### [IP model shift: from blocks to app-specific subsystems](#)

Oct. 01, 2004 - IP model shift: from blocks to app-specific subsystems

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#### [NetSpeed Bridges the Gap Between Architecture and Implementation](#)

Jan. 03, 2017 -

#### [Improved Timing Closure for Network-on-Chip based SOC's](#)

Mar. 13, 2017 -

#### [Optimizing Quality-of-Service in a Network-on-Chip Architecture](#)

Oct. 26, 2015 -

#### [Functional verification concepts have to change](#)

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