

Appendix B₅
Exemplary Accused Qualcomm Instrumentality

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)

“Integrated circuit with data communication network and IC design method”

'2893 Patent Claim	Qualcomm Accused Instrumentalities¹
10. A method of designing an integrated circuit comprising a plurality of functional blocks, and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks	Without conceding that the preamble of claim 10 of the '2893 Patent is limiting, Qualcomm Incorporated and Qualcomm Technologies, Inc.'s (collectively, “Qualcomm”) Accused Instrumentalities are integrated circuits and Qualcomm performs a method of designing an integrated circuit comprising a plurality of functional blocks, and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, either literally or under the doctrine of equivalents. Included in the Accused Instrumentalities are Qualcomm’s integrated circuits that incorporate, implement, utilize, include, or otherwise comprise one or more network on chip interconnects. For example, the Snapdragon 8+ Gen 1 Mobile Platform (hereinafter, “Snapdragon SoC”) is an integrated circuit comprising a plurality of functional blocks:

¹ The Accused Instrumentalities include Qualcomm’s integrated circuits (“ICs”) that incorporate, implement, utilize, include, or otherwise comprise one or more network on chip interconnects (“NoCs”); and products, devices, systems or apparatuses, whether Qualcomm’s or others’, incorporating, implementing, utilizing, including, or otherwise comprising such Qualcomm ICs. The Qualcomm Snapdragon 8+ Gen 1 Mobile Platform SoC is charted as representative of the Accused Instrumentalities. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence already cited herein.

'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	 Snapdragon 8+ Gen 1 Mobile Platform New power and performance enhancements deliver the ultimate boost across all your on-device experiences. The Snapdragon® 8+ Gen 1 Mobile Platform is our premium-tier powerhouse. Qualcomm® Adreno™ GPU offers a 10% increase in GPU clock speeds and 30% GPU power reduction while the Qualcomm® Kryo™ CPU provides 10% better CPU performance and 30% CPU improved power efficiency. Plus, this platform delivers additional power savings and extended performance across the board—including over 80 minutes longer video streaming and more than 50 minutes longer web browsing. https://www.qualcomm.com/products/application/smartphones/snapdragon-8-series-mobile-platforms/snapdragon-8-plus-gen-1-mobile-platform The Accused Instrumentalities comprise a plurality of modules, for example Qualcomm Adreno GPU; Qualcomm Kryo CPU; Qualcomm Hexagon Processor; and Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU):

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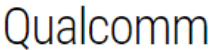
'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	 Snapdragon 8+ mobile platform Gen 1 SPECIFICATIONS & FEATURES Artificial Intelligence Qualcomm® Adreno™ GPU Qualcomm® Kryo™ CPU Qualcomm® Hexagon™ Processor • Fused AI Accelerator • Hexagon Tensor Accelerator • Hexagon Vector eXtensions • Hexagon Scalar Accelerator • Support for mix precision(INT8+INT16) • Support for all precisions (INT8, INT16, FP16) Qualcomm® Sensing Hub 5G Modem-RF System Snapdragon® X65 5G Modem-RF System • 5G mmWave and sub-6 GHz, standalone • (SA) and non-standalone (NSA) modes, FDD, TDD • Dynamic Spectrum Sharing • mmWave: 8 carriers, 2x2 MIMO • Sub-6 GHz: 4x4 MIMO • Qualcomm® 5G PowerSave 2.0 • Qualcomm® Smart Transmit™ 2.0 technology • Qualcomm® Wideband Envelope Tracking • Qualcomm® AI-Enhanced Signal Boost • Global 5G multi-SIM Downlink: Up to 10 Gbps Multimode support: 5G NR, LTE including CBRS, WCDMA, HSPA, CDMA 1x, EV-DO, GSM/EDGE Camera Qualcomm Spectra™ Image Signal Processor • Triple 18-bit ISPs • Up to 3.2 Gigapixels per Second computer vision ISP (CV-ISP) • Up to 36 MP triple camera @ 30 FPS with Zero Shutter Lag • Up to 64+36 MP dual camera @ 30 FPS with Zero Shutter Lag • Up to 108 MP single camera @ 30 FPS with Zero Shutter Lag • Up to 200 Megapixel Photo Capture Rec. 2020 color gamut photo and video capture Up to 10-bit color depth photo and video capture 8K HDR Video Capture + 64 MP Photo Capture 10-bit HEIF: HEIC photo capture, HEVC video capture Video Capture Formats: HDR10+, HDR10, HLG, Dolby Vision 8K HDR Video Capture @ 30 FPS 4K Video Capture @ 120 FPS Slow-mo video capture at 720p @ 960 FPS Bokeh Engine for Video Capture Video super resolution Multi-frame Noise Reduction (MFNR) Locally Motion Compensated Temporal Filtering Multi-Frame and triple exposure staggered/digital overlap HDR dual-sensor support AI-based face detection, auto-focus, and CPU Kryo CPU • Up to 3.2 GHz*, with Arm Cortex-X2 technology • 64-bit Architecture Visual Subsystem Adreno GPU • Vulkan® 1.1 API support • HDR gaming (10-bit color depth, Rec. 2020 color gamut) • Physically Based Rendering • Volumetric Rendering • Adreno Frame Motion Engine • API Support: OpenGL® ES 3.2, OpenCL™ 2.0 FP, Vulkan 1.1 • Hardware-accelerated H.265 and VP9 decoder • HDR Playback Codec support for HDR10+, HDR10, HLG and Dolby Vision Security Platform Security Foundations, Trusted Execution Environment & Services, Secure Processing Unit (SPU) Trust Management Engine Qualcomm® wireless edge services (WES) and premium security features Qualcomm® 3D Sonic Sensor and Qualcomm® 3D Sonic Max (fingerprint sensor) Qualcomm® Type-1 Hypervisor

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	Wi-Fi & Bluetooth* Qualcomm* FastConnect™ 6900 System • Wi-Fi Standards: Wi-Fi 6E, Wi-Fi 6 (802.11ax), • Wi-Fi 5 (802.11ac), 802.11a/b/g/n • Wi-Fi Spectral Bands: 24 GHz, 5 GHz, 6 GHz • Peak speed: 3.6 Gbps • Channel Bandwidth: 20/40/80/160 MHz • 8-stream sounding (for 8x8 MU-MIMO) • MIMO Configuration: 2x2 (2-stream) • MU-MIMO (Uplink & Downlink) • 4K QAM • OFDMA (Uplink & Downlink) • 4-Stream (2x2 + 2x2) Dual Band Simultaneous (DBS) • Wi-Fi Security: WPA3-Enterprise, WPA3- Enhanced Open, WPA3 Easy Connect, WPA3-Personal Integrated Bluetooth • Bluetooth Features: Bluetooth* 5.3, LE Audio, Dual Bluetooth antennas • Bluetooth audio: Snapdragon Sound™ Technology with support for Qualcomm* aptX™ Voice, aptX Lossless, aptX Adaptive, and LE audio snapdragon.com Audio Qualcomm Aqstic™ audio codec (WCD9385) New Qualcomm Aqstic smart speaker amplifier (WSA8835) Total Harmonic Distortion + Noise (THD+N), Playback: -108dB Qualcomm* Audio and Voice Communication Suite Display On-Device Display Support: • 4K @ 60 Hz • QHD+ @ 144 Hz Maximum External Display Support: up to 4K @ 60 Hz • 10-bit color depth, Rec. 2020 color gamut • HDR10 and HDR10+ Demura and subpixel rendering for OLED Uniformity Charging Qualcomm* Quick Charge™ 5 Technology Location GPS, Glonass, BeiDou, Galileo, QZSS, NavIC capable Dual Frequency GNSS (L1/L5) Sensor-Assisted Positioning • Urban pedestrian navigation with sidewalk accuracy • Global freeway lane-level vehicle navigation Memory Support for LP-DDR5 memory up to 3200 MHz Memory Density: up to 16 GB General Specifications Full Suite of Snapdragon Elite Gaming™ features 4 nm Process Technology USB Version 3.1; USB Type-C Support Part Number: SM8475 *Snapdragon 8+ Gen 1 Mobile Platform also available in 3 GHz CPU version. Maximum CPU speed will vary based on platform version. Consult OEM specifications for device CPU speed. Certain optional features available subject to Carrier and OEM selection for an additional fee. Snapdragon, Qualcomm, Qualcomm Hexagon, Qualcomm 5G PowerSave, Qualcomm Kryo, Qualcomm Smart Transmit, Qualcomm Wideband Envelope Tracking, Qualcomm AI-Enhanced Signal Boost, Qualcomm Spectra, Qualcomm Aqstic, Qualcomm 3D Sonic Sensor, Qualcomm Type-1 Hypervisor, Qualcomm Adreno, Qualcomm Sensing Hub, Qualcomm 3D Sonic Max, Qualcomm FastConnect, Snapdragon Sound, Qualcomm aptX, Snapdragon Elite Gaming, and Qualcomm Quick Charge are products of Qualcomm Technologies, Inc. and/or its subsidiaries. Qualcomm wireless edge services are offered by Qualcomm Technologies Inc. and/or its subsidiaries. Snapdragon, Qualcomm, Hexagon, Snapdragon Elite Gaming, Adreno, FastConnect, Snapdragon Sound, Kryo, Smart Transmit, Qualcomm Spectra, Qualcomm Aqstic, Snapdragon Sight, and Quick Charge are trademarks or registered trademarks of Qualcomm Incorporated. aptX is a trademark or registered trademark of Qualcomm Technologies International, Ltd. ©2022 Qualcomm Technologies, Inc. and/or its affiliated companies. All Rights Reserved. Snapdragon 8+ Gen 1 Mobile Platform Product Brief, https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/Snapdragon-8-plus-Gen-1-Product-Brief.pdf, at 2.

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	The Accused Instrumentalities utilize Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the “Arteris NoC”)² to exchange messages:   Arteris-developed NoC technology is the backbone of Snapdragon application processors & LTE modems, Atheros wireless connectivity SoCs, and CSR IoT products. LEARN MORE » https://web.archive.org/web/20210514110614/https://www.arteris.com/customers

² To the extent that the Snapdragon SoC does not use an NoC provided by Arteris Inc. in the wake of Qualcomm Technologies, Inc.’s 2013 acquisition of Arteris technology (see https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31; <https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team>), on information and belief, the Snapdragon SoCs use one or more NoCs that are derived from, based upon, and/or sufficiently similar in all respects material to NST’s infringement contentions as, the structure, function and operation of the Arteris NoC technology described in the materials cited and reproduced herein. NST expressly reserves its right to supplement these contentions upon receipt of technical discovery from Qualcomm and Arteris.

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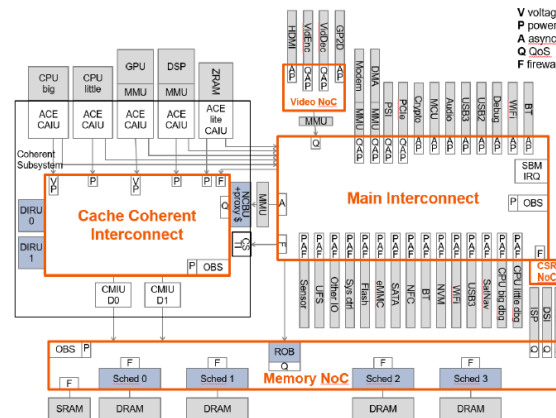
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	Certain Arteris Technology Assets Acquired by Kurt Shuler, on October 31, 2013 Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial network-on-chip (NoC) interconnect IP solutions, today announced that Qualcomm Technologies, Inc. (“Qualcomm”), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris. “Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris’ Network-on-Chip interconnect IP technology. ARTERIS^{IP} K. Charles Janac, President and CEO, Arteris https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31; https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team Large SoCs, such as the Accused Instrumentalities may include multiple classes of Arteris NoC data communication network:

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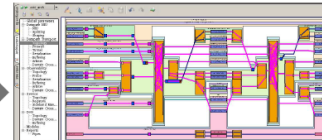
Qualcomm Accused Instrumentalities¹

Logical Interconnect Topology Development

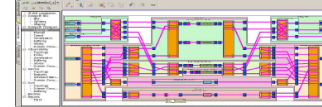
FLEXNOC & NCORE INTERCONNECT IPS DEFINE ARCHITECTURES



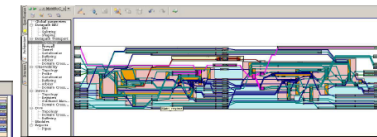
Ncore Cache Coherent NoC



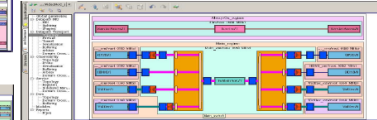
Memory NoC



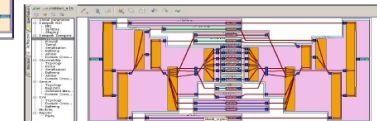
Main NoC



Service NoC



Video NoC



- ArChip16 Example: Large SoCs have multiple classes of interconnect
 - Non-coherent, Coherent, Control/Status, Observability, etc.
- Ncore & FlexNoC interconnects are managed separately from IP blocks, increasing design flexibility

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See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.

The Arteris NoC in the Accused Instrumentalities is a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, either literally or under the doctrine of equivalents.

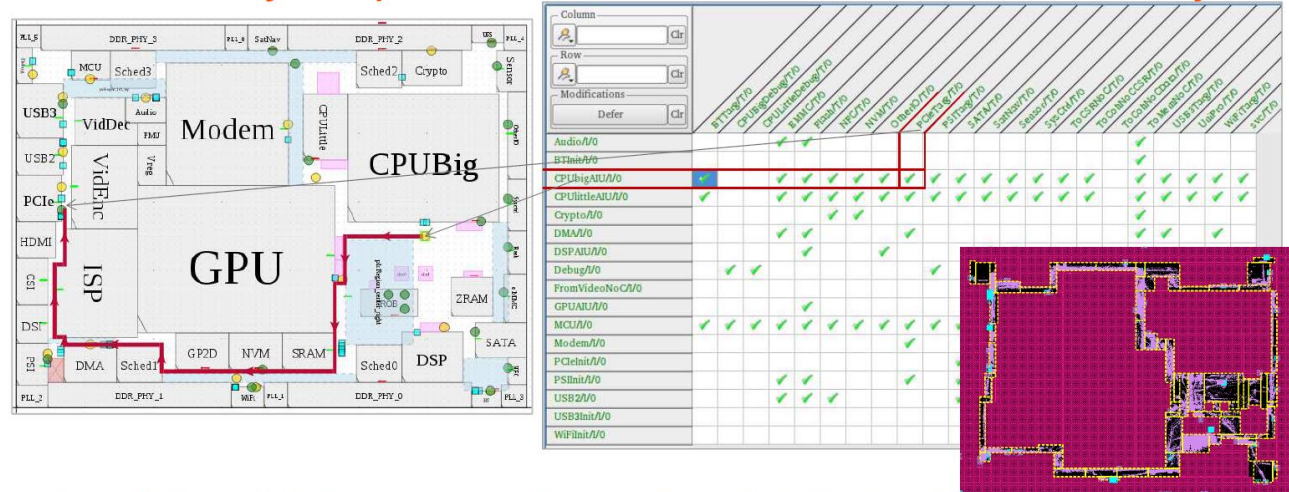
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Qualcomm Accused Instrumentalities¹

For example, connections between modules within the Arteris NoC may be defined by a connectivity table:

Connectivity Map → Interconnect Connections → Layout



- Connectivity table defines interconnect connections within the floorplan
- Routes must pass through available channels in the floorplan
- Connectivity passes from initiator NIU to switch, to link, to RC buffers and finally to target NIU

DC-Topographical

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See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12.

As another example, in an implementation of the Arteris NoC by Texas Instruments, which on current information and belief is the same or similar to Qualcomm’s implementation, a connectivity matrix and “ConnIDs” are used:

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Qualcomm Accused Instrumentalities¹

Figure 14-3 shows the functional paths between the L3_MAIN master NIUs and the L3_MAIN and L3 slave NIU agents. The functional paths in L3_MAIN are indicated by the following:

- A cell contains the letter C when a functional path exists.
- A cell is empty when a functional path does not exist.

Figure 14-3. Connectivity Matrix

		TARGETS																																									
		DMMP1	DMMP2	OCMC RAM1	GPC	DSP1 SDMA	IPU1	IPU2	IVA1 SL2F	MMU1	MMU2	OSPI	GPU	BB2D	TC1 EDMA	TC2 EDMA	TPCC EDMA	IVA CONFIG	DSS	PCIE SS1	PCIE SS2	MCASP1	MCASP2	MCASP3	L4_PER1 P1	L4_PER1 P2	L4_PER1 P3	L4_PER2 P1	L4_PER2 P2	L4_PER2 P3	L4_PER3 P1	L4_PER3 P2	L4_PER3 P3	L4_WKUP	L4_CFG	L3 MAIN SN	L3 INSTR	DEBUGSS CT_TBR	VCP1	VCP2	PRU-ICSS1		
INITIATORS	MPU	C																																									
	DSP1 MDMA	C																																									
	DSP1 DMA	C																																									
	DSP1 CFG	C																																									
	IPU1	C																																									
	IPU2	C																																									
	VIP1 P1	C																																									
	VIP1 P2	C																																									
	CAL	C																																									
	MLB	C																																									
	VPE P1	C																																									
	VPE P2	C																																									
	DSS	C																																									
	IVA	C																																									
	GPU P1	C																																									
	GPU P2	C																																									
	BB2D P1	C																																									
	BB2D P2	C																																									
	DMA_SYSTEM_RD	C																																									
	DMA_SYSTEM_WR	C																																									
	EDMA_TC0_RD	C																																									
	EDMA_TC0_WR	C																																									
	EDMA_TC1_RD	C																																									
	EDMA_TC1_WR	C																																									
	MMU1	C																																									
	PCIE SS1	C																																									
	PCIE SS2	C																																									
	MMU2	C																																									
	GMAC_SW	C																																									

DRA79x SoC Technical Reference Manual,

https://www.ti.com/lit/ug/spruif7c/spruif7c.pdf?ts=1638387986460&ref_url=https%253A%252F%252Fw at pg. 2965.

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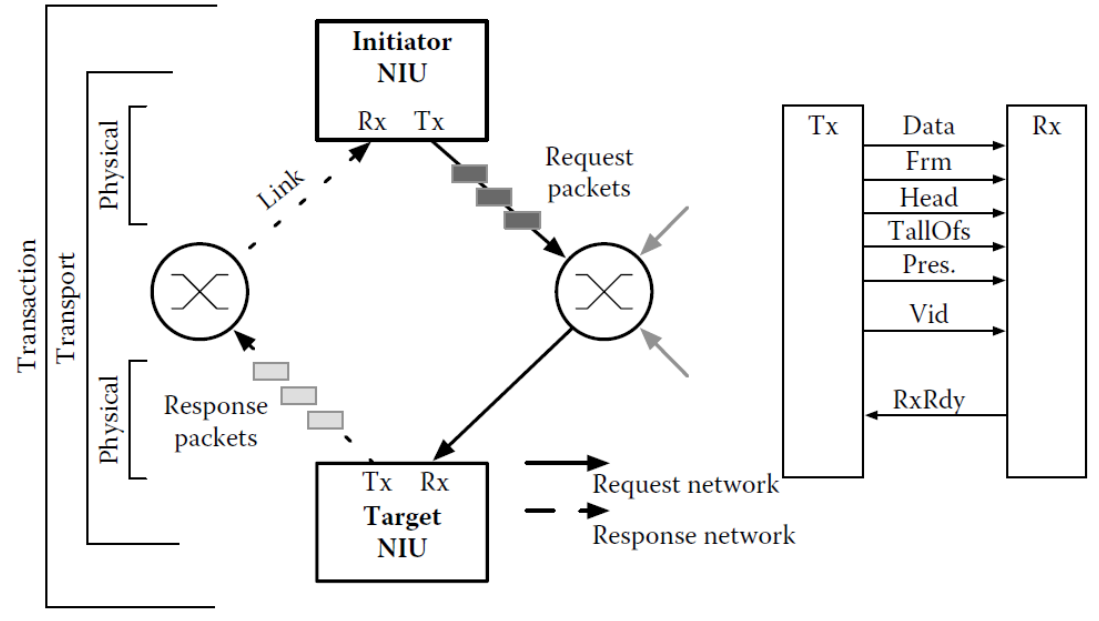
'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹															
	14.2.3.2.3 Master NIU Identification A master NIU ID (ConnID) is assigned to every module in the device. The ID uniquely identifies the master NIU for an interconnect transfer (see Table 14-10). The interconnect uses ConnID values for a number of purposes, including: • Master source identification for the protection mechanism • Response route generation • Firewall error logging • L3_MAIN interconnect error logging Table 14-10. ConnID Values <table><tr><th>8-bit ConnID (hex)</th><th>4-bit ConnID (hex)</th><th>Master NIU</th></tr><tr><td>0</td><td>0</td><td>MPU</td></tr><tr><td>10</td><td>1</td><td>CS_DAP</td></tr><tr><td>20</td><td>2</td><td>DSP1 MDMA</td></tr><tr><td>24</td><td>2</td><td>DSP1 CFG</td></tr></table> DRA79x SoC Technical Reference Manual, https://www.ti.com/lit/ug/spruif7c/spruif7c.pdf?ts=1638387986460&ref_url=https%253A%252F%252Fw at pg. 2966. The Arteris NoC uses Network Interface Units (NIUs) “at the boundary of the NoC” and which “connect[] IP blocks to the network”:	8-bit ConnID (hex)	4-bit ConnID (hex)	Master NIU	0	0	MPU	10	1	CS_DAP	20	2	DSP1 MDMA	24	2	DSP1 CFG
8-bit ConnID (hex)	4-bit ConnID (hex)	Master NIU														
0	0	MPU														
10	1	CS_DAP														
20	2	DSP1 MDMA														
24	2	DSP1 CFG														

'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	11.3.1.1 Transaction Layer The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network. See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313; see <i>id</i> at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: “In this chapter

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	we will present an MPSoC platform [...] using Arteris NoC as communication infrastructure.”). On current belief, this book describes the structure, function and operation of Arteris NoCs (including any derivatives thereof) from approximately 2009 to present day. As a further illustration, in the Arteris NoC, “[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path.”

'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	 FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312.
each data package comprising N data elements including a data element comprising routing information for the	Without conceding that the preamble of claim 10 of the '2893 Patent is limiting, in the Arteris NoC utilized by the Accused Instrumentalities, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, either literally or under the doctrine of equivalents. For example, the “Arteris NTTP protocol is packet-based” and the packets, which have “header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet

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network stations, N being an integer of at least two	target address,” are “transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes”: 11.3.1.2 Transport Layer The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target. See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313. As yet a further illustration, packets in the Arteris NoC are “delivered as words that are sent along links and “[o]ne link (represented in Figure 11.1) defines the following signals”:

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	11.3.1.3 Physical Layer The delivery of packets within the NoC is the responsibility of the physical layer. Packets, which have been split by the transport layer into cells, are delivered as words that are sent along links. Within a single clock cycle, the physical layer may carry words comprising a fraction of a cell, a single cell, or multiple cells. The link size, or width (i.e., number of wires), is set by the designer at design time and determines the number of cells of one word. NTTP defines five possible link-widths: quarter (QRT), half (HLF), single (SGL), double (DBL), and quad (QUAD). A single-width (SGL) link transmits one cell per clock cycle, a double-width link transmits two cells per clock cycle, and so on. Words travel within point-to-point links, which are independent from other protocol layers: a word is sent through a transmit port, Tx, over a link to a receive port, Rx. The actual number of wires in a link depends on the

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	maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals: • Data—Data word of the width specified at design-time. • Frn—When asserted high, indicates that a packet is being transmitted. • Head—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only. • TailOfs—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only. • Pres.—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2). • Vld—Data valid: when asserted high, indicates that a word is being transmitted. • RxRdy—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTP communications.

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'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹																																							
	<i>Id.</i> at 313-314. As a further example, the packets sent in the Arteris NoC are “composed of cells that are organized into fields, with each field carrying specific information”: <table><tr><th>Field</th><th>Size</th><th>Function</th></tr><tr><td>Opcode</td><td>4 bits/3 bits</td><td>Packet type: 4 bits for requests, 3 bits for responses</td></tr><tr><td>MstAddr</td><td>User Defined</td><td>Master address</td></tr><tr><td>SlvAddr</td><td>User Defined</td><td>Slave address</td></tr><tr><td>SlvOfs</td><td>User Defined</td><td>Slave offset</td></tr><tr><td>Len</td><td>User Defined</td><td>Payload length</td></tr><tr><td>Tag</td><td>User Defined</td><td>Tag</td></tr><tr><td>Prs</td><td>User defined (0 to 2)</td><td>Pressure</td></tr><tr><td>BE</td><td>0 or 4 bits</td><td>Byte enables</td></tr><tr><td>CE</td><td>1 bit</td><td>Cell error</td></tr><tr><td>Data</td><td>32 bits</td><td>Packet payload</td></tr><tr><td>Info</td><td>User Defined</td><td>Information about services supported by the NoC</td></tr><tr><td>Err</td><td>1 bit</td><td>Error bit</td></tr></table>	Field	Size	Function	Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses	MstAddr	User Defined	Master address	SlvAddr	User Defined	Slave address	SlvOfs	User Defined	Slave offset	Len	User Defined	Payload length	Tag	User Defined	Tag	Prs	User defined (0 to 2)	Pressure	BE	0 or 4 bits	Byte enables	CE	1 bit	Cell error	Data	32 bits	Packet payload	Info	User Defined	Information about services supported by the NoC	Err	1 bit	Error bit
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'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹																					
	<table><tr><td>StartOfs</td><td>2 bits</td><td>Start offset</td></tr><tr><td>StopOfs</td><td>2 bits</td><td>Stop offset</td></tr><tr><td>WrpSize</td><td>4 bits</td><td>Wrap size</td></tr><tr><td>Rsv</td><td>Variable</td><td>Reserved</td></tr><tr><td>CtlId</td><td>4 bits/3 bits</td><td>Control identifier, for control packets only</td></tr><tr><td>CtlInfo</td><td>Variable</td><td>Control information, for control packets only</td></tr><tr><td>EvtId</td><td>User defined</td><td>Event identifier, for event packets only</td></tr></table> 3529 2825 2415 145 4 30 HeaderInfoLenMaster AddressSlave AddressPrsOpcode NeckerTagErrSlave offsetStartOfsStopOfs DataBEData ByteBEData ByteBEData ByteBEData Byte DataBEData ByteBEData ByteBEData ByteBEData Byte 32 31 3027 2620 1914 135 4 30 HeaderRsvLenInfoTagMaster AddressPrsOpcode DataCEData DataCEData FIGURE 11.2 NTTP packet structure. Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 314-315.	StartOfs	2 bits	Start offset	StopOfs	2 bits	Stop offset	WrpSize	4 bits	Wrap size	Rsv	Variable	Reserved	CtlId	4 bits/3 bits	Control identifier, for control packets only	CtlInfo	Variable	Control information, for control packets only	EvtId	User defined	Event identifier, for event packets only
StartOfs	2 bits	Start offset																				
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CtlInfo	Variable	Control information, for control packets only																				
EvtId	User defined	Event identifier, for event packets only																				
the plurality of network stations	Without conceding that the preamble of claim 10 of the '2893 Patent is limiting, in the Arteris NoC utilized by the Accused Instrumentalities, the plurality of network stations comprise a plurality of																					

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comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface	data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, either literally or under the doctrine of equivalents. For example, the Arteris NoC uses Network Interface Units (NIUs) “at the boundary of the NoC” and which “connect[] IP blocks to the network”: 11.3.1.1 Transaction Layer The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU’s transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets

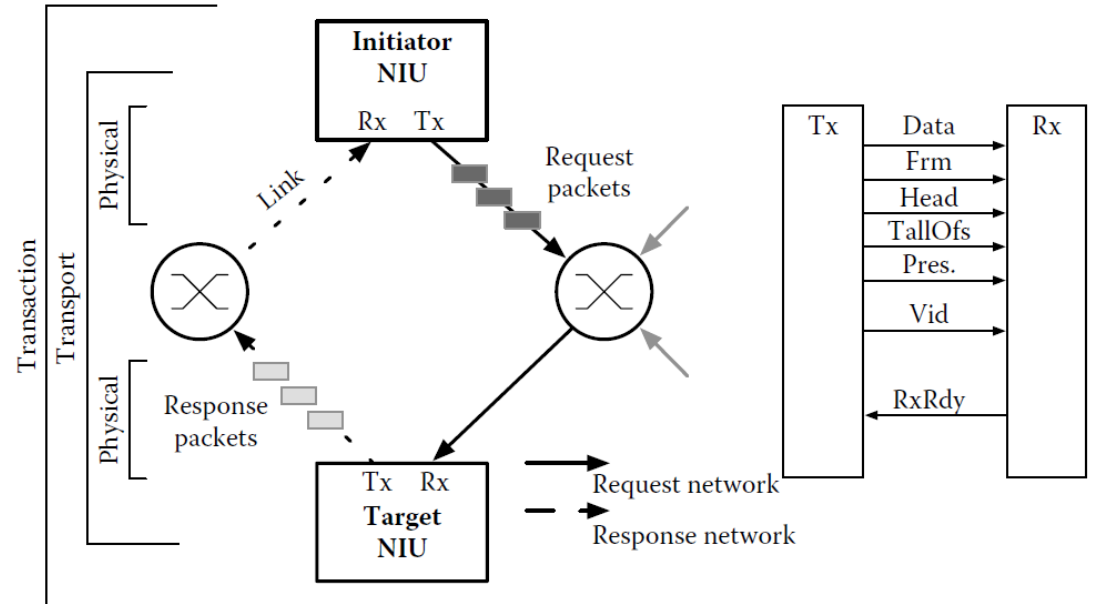
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'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network. See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313. As a further illustration, in the Arteris NoC, “[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path.”

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	 FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312. As a further illustration of the routers in the Arteris NoC:

11.3.3.2 Routing

The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address

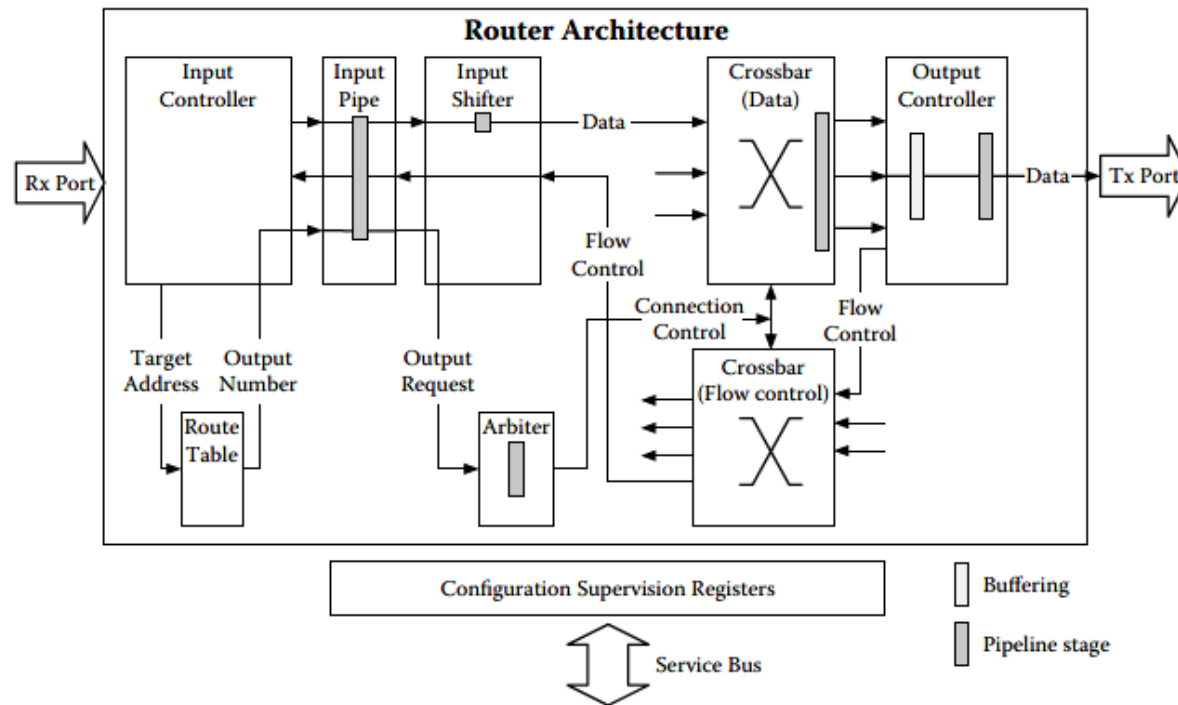
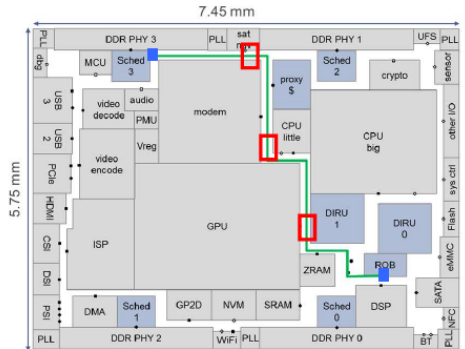


FIGURE 11.6
Packet transportation unit: Router architecture.

'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	<i>Id.</i> at 320. As a further illustration of the network interfaces in the Arteris NoC: 11.3.2.1 Initiator NIU Units Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU. Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.

'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	11.3.2.2 Target NIU Units Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always <i>Id.</i> at 318.
the method comprising the acts of: identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and	The method of designing the Accused Instrumentalities includes identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold, either literally or under the doctrine of equivalents. For example, when it is identified that a signal cannot cross a chip in one clock cycle, designing the Accused Instrumentalities incorporating the Arteris NoC includes pipelining for distance spanning, either literally or under the doctrine of equivalents. As an illustration, a signal traveling “~6mm” has a propagation delay of “~400ps/mm”, requiring at least “2400ps to span the Distance”; thus requiring “at least 3 pipeline stages and 4 clock cycles to meet timing.”

'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	Wire Delays – Can’t Cross a Chip in 1 Clock Cycle PHYSICAL DISTANCE DICTATES THE NUMBER OF PIPELINE STAGES   ■ Endpoint (NIU) — 1-cycle path □ Pipeline • Interconnect Frequency: 1.2GHz = 833ps • Distance to travel = ~6mm • Propagation delay = ~400ps/mm in 16nm FinFET; Needs 2400ps to span the distance • Requires at least 3 pipeline stages and 4 clock cycles to meet timing Large 14nm FinFET SoC may have >6,000 pipelines with 6K factorial pipeline combinations and 60 timing parameters – Too much for human comprehension! ARTERISIP ISPD 2018, 28 March 2018 Copyright © 2018 Arteris IP 3 See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 3.
in response to the identifying act, inserting M*N data storage elements into the data communication network, M being	In response to the identifying act, the method of designing the Accused Instrumentalities includes inserting M*N data storage elements into the data communication network, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel, either literally or under the doctrine of equivalents. For example, in the Arteris NoC, “[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response

'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
a positive integer, for introducing a delay of M*N cycles on the first communication channel.	network.... Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path." FIGURE 11.1 NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312.

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	As a further example, a “delay pipeline is automatically inserted in the input controller to keep data and routing information in phase” and an input pipe “introduces a one-word-deep FIFO”: Depending on the kind of routing table chosen, more than one cycle may be required to make a decision. A delay pipeline is automatically inserted in the input controller to keep data and routing information in phase, thus guaranteeing one-word-per-cycle peak throughput. Routing tables select the output port that a given packet must take. The route decision is based on the * * * The input pipe is optional and may be inserted individually for each input port. It introduces a one-word-deep FIFO between the input controller and the crossbar and can help timing closure, although at the expense of one supplementary latency cycle. See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 322. As a further example the crossbar may have pipeline storage elements and the output controller contains a FIFO storage element “with as many words as there are date pipelined in the crossbar”:

'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	The crossbar implements datapath connection between inputs and outputs. It uses the connection matrix produced by the arbiter to determine which connections must be established. It is equivalent to a set of m muxes (one per output port), each having n inputs (one per input port). If necessary, the crossbar can be pipelined to enhance timing. The number of pipeline stages can be as high as $\max(n, m)$. The output controller constructs the output stream. It is also responsible for compensating crossbar latency. It contains a FIFO with as many words as there are data pipelined in the crossbar. FIFO flow control is internally managed with a credit mechanism. Although FIFO is typically empty, should the output port become blocked, it contains enough buffering to flush the crossbar. When necessary for timing reasons, a pipeline stage can be introduced at the output of the controller. <i>Id.</i> at 323. The buffering and pipeline stages are shown in the following depiction of the router architecture of the Arteris NoC:

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Qualcomm Accused Instrumentalities¹

11.3.3.2 Routing

The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address

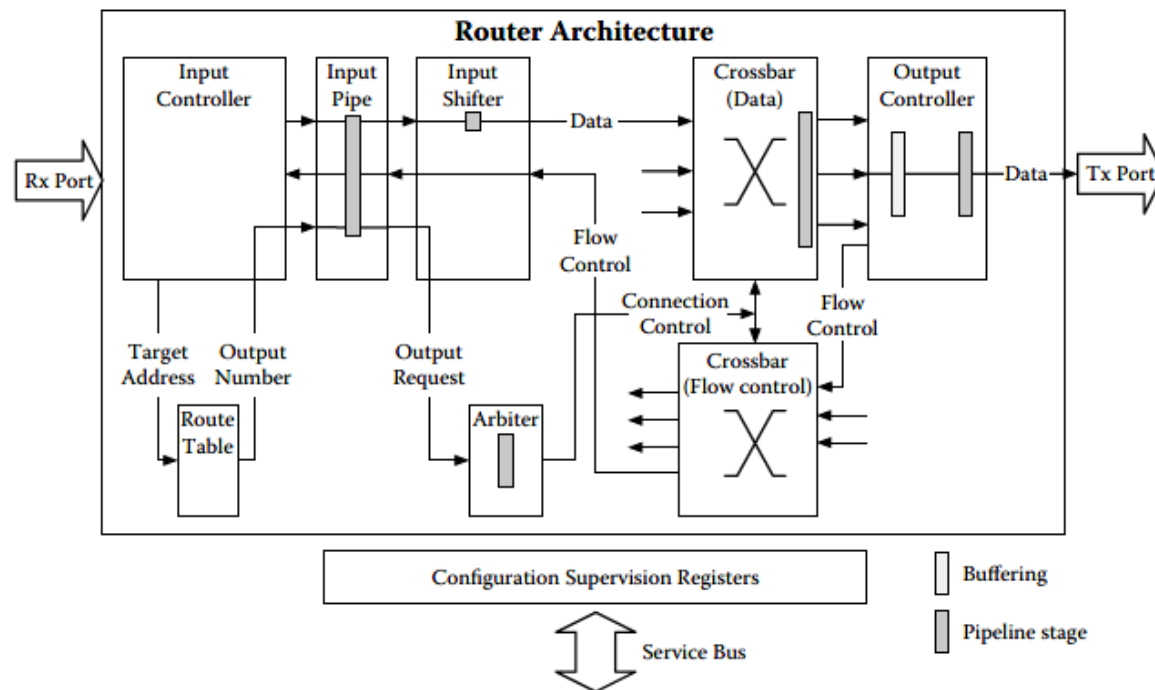
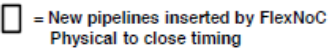
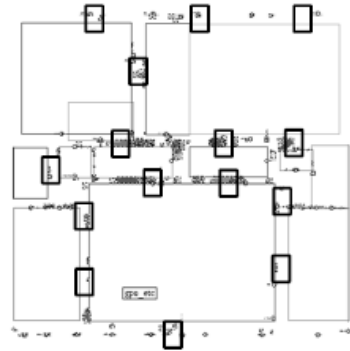


FIGURE 11.6
Packet transportation unit: Router architecture.

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'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	<i>Id.</i> at 320. As another example, the “fwdPipe” parameter “introduces a true pipeline register on the forward signals” and “inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path”: get frequency, process, or floor plan. The opportunity to break long paths is present on most MINI transmission ports, and is controlled through a parameter named fwdPipe: when set, this parameter introduces a true pipeline register on the forward signals, and effectively breaks the forward path. The parameter inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path. <i>Id.</i> at 323-324. As another example, pipelines may be automatically inserted by the Arteris NoC to close timing:

'2893 Patent Claim	Qualcomm Accused Instrumentalities ¹
	Adding Pipelines Automatically ○ Evaluate all timing arcs in the NoC interconnect ○ Distance and logic depth dictate number of pipeline stages ○ Placement of the NoC units is predicted by FlexNoC   Copyright © 2015 Arteris 14 Using SoC Interconnect IPs to Improve Physical Layout, http://mpsoc-forum.org/archive/2015/slides/45B-Charles%20Janac.pdf, at slide 14. As a further illustration, the Arteris NoC includes pipelining for distance spanning when traveling “~6mm” has a propagation delay of “~400ps/mm”, requiring at least “2400ps to span the Distance”; thus requiring “at least 3 pipeline stages and 4 clock cycles to meet timing.”

'2893 Patent Claim

Qualcomm Accused Instrumentalities¹

Wire Delays – Can't Cross a Chip in 1 Clock Cycle

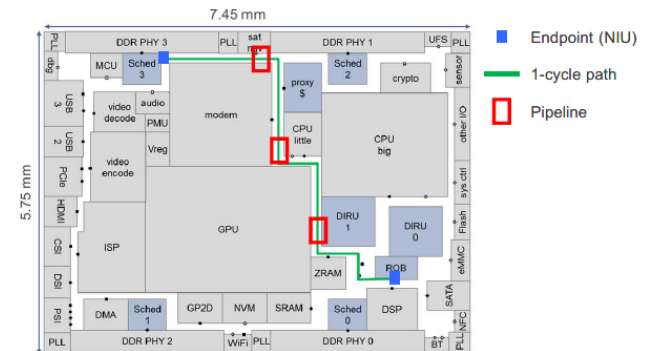
PHYSICAL DISTANCE DICTATES THE NUMBER OF PIPELINE STAGES



Clock Cycles

- Interconnect Frequency: 1.2GHz = 833ps
- Distance to travel = ~6mm
- Propagation delay = ~400ps/mm in 16nm FinFET; Needs 2400ps to span the distance
- Requires at least 3 pipeline stages and 4 clock cycles to meet timing

Large 14nm FinFET SoC may have >6,000 pipelines with 6K factorial pipeline combinations and 60 timing parameters – Too much for human comprehension!



ARTERIS^{IP}

ISPD 2018, 28 March 2018

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See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 3.