

EXHIBIT 7

PART 1

**UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION**

NETWORK SYSTEM TECHNOLOGIES, LLC,	)	
	)	
Plaintiff,	)	
	)	
v.	)	
	)	
QUALCOMM INCORPORATED;	)	Civil Action No. 1:22-cv-1331
QUALCOMM TECHNOLOGIES, INC.;	)	
ARTERIS, INC.,	)	JURY TRIAL DEMANDED
	)	
Defendants.	)	
	)	
	)	

DECLARATION OF DR. ERIK CHMELAR

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I, Dr. Erik Chmelar, declare as follows:

I. INTRODUCTION

1. I am an independent consultant. I am over eighteen years of age and I would be competent to testify as to the matters set forth herein if I am called upon to do so.

2. I have been engaged by Plaintiff Network System Technologies, LLC (“NST”) as an expert in this case regarding U.S. Patent No. 7,366,818 (the “’818 patent”), U.S. Patent No. 7,373,449 (the “’449 Patent”), U.S. Patent No. 7,594,052 (the “’052 Patent”), U.S. Patent No. 7,769,893 (the “’9893 Patent”), U.S. Patent No. 8,072,893 (the “’2893 Patent”), and U.S. Patent No. 8,086,800 (the “’800 Patent”) (collectively, the “Asserted Patents”) (Dkt. 1, Exhibits 1–6.).

3. This declaration is based on the information currently available to me. To the extent that additional information becomes available, I reserve the right to continue my investigation and study, which may include a review of documents and information that may be produced, as well as testimony from depositions that have not yet been taken.

4. I reserve the right to supplement this declaration in the event that Defendants in this case clarify their claim construction positions, or provide supplemental evidence, including expert testimony, in support of their proposed claim constructions.

5. I am being compensated for my time in the amount of \$600 per hour. I have no financial interest in NST or the Asserted Patents, and my compensation is not contingent upon the substance of my declaration, any statements or opinions made, or the outcome of this matter.

II. BACKGROUND AND EXPERIENCE

6. In 2000, I received a B.S. degree in Electrical Engineering from Michigan Technological University with the highest distinction (summa cum laude). In 2001, I received an M.S. degree in Electrical Engineering from Stanford University, with a focus on computer

networks (EE284 Introduction to Computer Networks, EE384A Internet Protocols, EE384S Network Architectures, and EE384S Multimedia Networks). In 2004, I received a Ph.D. degree in Electrical Engineering from Stanford University, with a primary focus on very large-scale integrated (VLSI) systems that culminated in a dissertation entitled “The Test and Diagnosis of Field-programmable Gate Arrays, advised by Dr. Edward J. McCluskey, and with conclusion of a secondary focus on computer networks (EE384X Packet Switch Architectures). While studying at Stanford University from 2000–2004, I taught undergraduate and graduate level courses as a Teaching Assistant (EE284 Introduction to Computer Networks, EE384A Internet Protocols and Standards, Digital Design Laboratory EE121, and E40 Introduction to Electronics), and I was employed as a Research Assistant in the Center for Reliable Computing. In 2011, I received a second B.S. degree in Chemical Physics from Saginaw Valley State University in 2011 with the highest distinction (summa cum laude).

7. During my undergraduate and graduate studies, I was additionally employed at several product-technology companies. From 1999–2002, I was employed as a Manufacturing Engineer at Cisco Systems, Inc, where I oversaw functional testing of layer-2 and layer-3 network switches and determined root-cause failures thereof. During the summers of 2002 and 2003, I was employed as a Product Test Engineer intern at Xilinx, Inc., where I researched and developed software tools to detect and diagnose physical hardware defects in FPGAs.

8. After earning my Ph.D., I was employed at LSI Corp. (now Broadcom, Inc.) from 2004–2012 as a Staff Software Engineer in the Advanced Technology Development department, where I conducted R&D for very large-scale integrated (VLSI) systems and serializer-deserializer (SerDes) circuits for high-speed data communications, for which I was granted approximately 20 U.S. patents. During this period of employment at LSI Corp., I also taught at

several Universities. From 2006–2008, I was a consulting Assistant Professor in the Electrical Engineering and Computer Science department at Stanford University, where I advised PhD students in the Center for Reliable Computing on the test and reliability of VLSI systems, and created and taught a PhD-level course on clock and data recovery (CDR) for digital communications (EE391 Clock and Data Recovery Architectures). From 2009–2012, I was an Adjunct Professor in the Electrical and Computer Engineering department at Saginaw Valley State University, where I taught several undergraduate courses in data communications and computer hardware (ECE455 Data Communications, ECE368 Computer Engineering, ECE368L Computer Engineering Lab, ECE216 Digital Circuits, and ECE216L Digital Circuits Lab).

9. From 2012–2015, I was employed at Stryker Instruments as a Senior Principal Engineer in the Advanced Development department, where I conducted and supervised R&D of computationally intelligent medical instruments and surgical technologies, and I delivered working prototypes for bio-photonic devices and boundary-constraint surgical robotics.

10. From 2015–2018, I was employed at Interdigital, Inc. as a Senior Manager of Innovation Partners, where I conducted and supervised R&D of 5th generation wireless (5G) network-enabled technologies including the Internet of Things, connected/autonomous vehicles, and augmented/virtual reality infrastructure, and I managed scientists and engineers to create over 100 new-invention disclosures for patent protection.

11. From 2019–present, I have provided consulting services to a major patent-licensing corporation as a Technical Expert in the areas of semiconductor circuits, microchips, and data communications. My consulting services have included determining whether and how specific patent claims within the aforementioned areas read on various products or product features. I analyze patents, technical specifications, product white papers, and product marketing

materials to produce detailed claim charts used by attorneys to formulate infringement opinions and licensing decisions. I have also performed technology market analysis and developed detailed technology landscapes and roadmaps in the aforementioned areas.

12. I have written technical publications dating back to 2003 on topics in the areas of semiconductor circuits, microchips, and data communications. I have written technical articles published in peer reviewed professional journals, trade journals, and proceedings of peer-reviewed conferences. I have presented at several technical symposia and technical conferences on topics in the aforementioned areas.

13. I am or have been a member or senior member of several professional organizations, including the Institute of Electrical & Electronic Engineers (IEEE), the Association for Computing Machinery (ACM), the American Society of Mechanical Engineers (ASME), the International Society of Optics & Photonics (SPIE), and the American Chemical Society (ACS).

14. I served as a Program Evaluator for the Accreditation Board of Engineering and Technology (ABET) from 2013–2018. As a Program Evaluator, I was responsible for determining ABET accreditation for university engineering programs categorized as Electrical Engineering programs and Computer Engineering programs.

15. I served as an Industry Mentor for National Science Foundation (NSF) I-Corps program in 2013, and served as an Instructor for the same in 2015. In these roles, I provided industry and technical guidance to engineers, inventors, and entrepreneurs launching technology startups.

16. I hold approximately 30 U.S. Patents, many of which concern technologies in the areas of semiconductor circuits, microchips, and data communications.

17. Additional details on my background and experience can be found in my *curriculum vitae*, attached hereto as **Appendix 1**.

III. LEGAL STANDARDS APPLIED IN MY DECLARATION

18. I have been asked to give expert opinions and technical advice on the meaning of certain terms found in the claims of the Asserted Patents.

19. My opinions are limited to what I believe a person of ordinary skill in the art (“POSITA”) would have understood with respect to the claims of the Asserted Patents.

20. I have studied the Asserted Patents, including the detailed description, drawings, and claims. A listing of all documents that I have reviewed and/or relied upon in formulating my opinions herein can be found attached hereto as **Appendix 2**.

21. I am informed and understand that claim construction is a matter of law, and will therefore be decided by the Court.

22. I am informed and understand that the specification, which includes the claims, is the single best guide as to the meaning of claim terms.

23. I am informed and understand that the relevant inquiry in claim construction is the question of how a POSITA would have understood the claim terms at the time of the invention, in light of the patent specification and prosecution history, and a POSITA is deemed to have read the claim terms in the context of the entire patent and its prosecution history.

24. I understand that one of ordinary skill in the art is presumed to be a person with at least a particular level of skill and knowledge in a certain field or industry, who is capable of understanding and practicing the technology described in the patent at issue. This person is assumed to have ordinary, not extraordinary, skill.

25. I understand that, in assessing the level of ordinary skill, one may consider several factors, including: (1) the education level of the inventor; (2) the education level of active workers in the field; (3) the types of problems encountered in the art; (4) prior art solutions to these problems; (5) the rate of innovation in the field; and (6) the sophistication of the technology.

26. Based on the foregoing, it is my opinion that a POSITA is an individual having at least: a Bachelor of Science (or equivalent) degree in electrical engineering, computer engineering, or a related field, and 2–3 years of work experience in very large-scale integrated (VLSI) systems, such as application-specific integrated circuits (ASICs), application-specific standard parts (ASSPs), system-on-chip (SoC), or field-programmable gate arrays (FPGAs), and has an understanding of on-chip interconnection networks.

IV. TECHNICAL BACKGROUND

27. A network-on-chip (NoC) is a data communication network on a microchip. In some ways, NoCs are like traditional computer networks, such as local area networks (LANs) and/or wide area networks (WANs). For example, both traditional computer networks and NoCs interconnect devices or components: traditional computer networks commonly interconnect discrete devices, such as computers, printers, servers, and so on, whereas NoCs commonly interconnect integrated components, such as processors, cores, caches, memories, input/output (I/O) interfaces, peripherals, and so on. The components interconnected by a NoC are typically integrated on a very large-scale integrated (VLSI) circuit, such as a system-on-chip (SoC).

28. An SoC is an integrated circuit in which most or all components of a system are integrated, including memories, processors, high-speed I/O interfaces, and dedicated application-specific logic. *See, e.g.,* NEIL WESTE & DAVID HARRIS, CMOS VLSI DESIGN: A CIRCUITS AND

SYSTEMS PERSPECTIVE 29 (4th ed. 2010) (**Exhibit A**); *see also* JAN RABAEY, ANANTHA CHANDRAKASAN & BORIVOJE NIKOLIC, DIGITAL INTEGRATED CIRCUITS: A DESIGN PERSPECTIVE 380–381, 395, 487 (2d ed. 2003) (**Exhibit B**). By the early 2000s, certain limitations of statically wired interconnections between components of an SoC were known, and as a result, NoCs were already emerging. *See, e.g., Exhibit B*, 487–488, *see also* William J. Dally & Brian Towles, *Route Packets, Not Wires: On-Chip Interconnection Networks*, PROC. 38TH DESIGN AUTOMATION CONF., 684, 684–689 (2001) (**Exhibit C**). Using a NoC, on-chip communication can be achieved by applying techniques and approaches that have made large-scale communications and networking systems around the world operate reliably and correctly. **Exhibit B**, 487. Rather than considering on-chip interconnections as point-to-point wires, they can be abstracted as communication channels over which to transmit data within a “quality-of-service” setting. *See Exhibit B*, 487 (citing M. Sgroi et al., *Addressing the System-on-a-Chip Interconnect Woes Through Communication-Based Design*, PROC. 38TH DESIGN AUTOMATION CONF., 667, 667–672 (2001)).

29. Before describing details of a NoC, it is important to describe how components can be interconnected in an SoC that does not implement a NoC. Interconnections, sometimes called interconnects, traces, wires, and signal lines, are electrical connections between a first component and a second component. Interconnects that carry similar signals are grouped together into buses, for example interconnects that carry address signals are grouped into an address bus and interconnects that carry data signals are grouped into a data bus. *See* JOHN F. WAKERLY, DIGITAL DESIGN: PRINCIPLES AND PRACTICES 358 (4th ed. 2005) (**Exhibit D**). A bus can be considered a direct interconnection between components (e.g., the path between a first component and a second component is always the same), where the interconnection may be

dedicated or shared. A dedicated bus comprises point-to-point interconnection between components, typically between two components. A shared bus comprises interconnections that can be shared between many components, and requires some type of bus arbitration to resolve conflicts when multiple components attempt to access the shared bus simultaneously.

30. There are several types of bus arbitration methods for shared buses, including centralized and distributed (sometimes called decentralized). In centralized arbitration, a single device, known as a bus controller or bus arbiter, is responsible for managing access to the bus. In distributed arbitration, components compete for access to the bus by sending a request signal to the bus arbiter and waiting for a grant signal. In some distributed arbitration methods, e.g., decentralized, each component has its own priority level, and the component with the highest priority is given access to the bus. A component capable of originating a bus transaction (e.g., requesting control of the bus) is a master component, and a component that cannot originate a bus transaction (e.g., only listens on the bus for communications intended for it) is a slave component. *See, e.g., Dkt. 1, Exhibit 1*, 3:63–65. In large and/or complex SoCs, such shared buses interconnecting master devices and slave devices via bus arbitration may not be sufficiently scalable nor provide enough bandwidth. *See* FAYEZ GEBALI, HAYTHAM ELMILIGI & MOHAMED WATHEQ EL-KHARASHI, NETWORKS-ON-CHIPS: THEORY AND PRACTICE 310 (2009) (**Exhibit E**).

31. In particular, with increasing quantities of components integrated in SoCs, increasing transistor densities, and increasing clock frequencies, it becomes very difficult to operate all the components synchronously within a same clock domain. This creates a need for a modular approach, where the processing system of the SoC comprises a plurality of relatively independent, complex modules. In conventional processing systems, the system modules usually

communicate with each other via a shared bus as described above. But as the number of modules increases, shared-bus communication is no longer practical at least because: (1) the large number of modules creates too high of an electrical load on the shared bus, and (2) the shared bus forms a communication bottleneck because only one component can control the bus at a time.

Consequently, some SoCs implement shared buses that utilize crossbar switches, also called crossbars, cross-point switch, matrix switch, or switch matrix, to achieve higher throughput, with STBus, IBM CoreConnect, and ARM AMBA being several examples of bus standards that may utilize crossbars. See **Exhibit E**, 310. A crossbar has a plurality of input lines and output lines that form a crossed pattern of intersecting lines between which a connection may be established by closing a switch located at a given intersection. An n -input, m -output crossbar, i.e., an $n \times m$ crossbar, is the equivalent to a set of m multiplexers (one per output port), each having n inputs (one per input port). See **Exhibit E**, 323. However, a shared bus that utilizes crossbars still has disadvantages. For example, the physical implementation of complex SoCs require large, complex crossbars that are difficult to place-and-route during physical design on the SoC in the areas between the components that implement functional logic of the SoC. See Kurt Schuler, *Busses, Crossbars and NoCs: The 3 Eras of SoC Interconnect History*, ARTERISIP (Oct. 22, 2010, 12:12 P.M.), <https://www.arteris.com/blog/bid/49081/busses-crossbars-and-nocs-the-3-eras-of-soc-interconnect-history> (**Exhibit F**). An on-chip communication network, e.g., a NoC, is an effective way to overcome some of the aforementioned disadvantages. See, e.g., **Dkt. 1**, **Exhibit 1**, 1:16–36.

32. A NoC interconnect paradigm radically changes the on-chip communication compared to direct interconnects, such as buses or switches. This is because of the multi-hop nature of a network, where components are not directly connected, but separated by one or more

network nodes. This is in contrast with buses, where components are directly connected as described above. Several implications of this change include arbitration methods (which can no longer be centralized), and communication properties (e.g., ordering, flow control, and so on). *See, e.g., Dkt. 1, Exhibit 1*, 3:36–46. In an SoC that implements a NoC, certain design-specific wiring structures of the SoC, typically the longer “global” wires that interconnect components, are replaced with a general-purpose on-chip communication network. *See Exhibit C, see also, e.g., Dkt. 1, Exhibit 1*, 1:37–50. Instead of connecting these top-level modules by routing dedicated wires, they are connected to a network that routes packets between them. *See Exhibit C*. In so doing, these network-connect modules, or components, can be thought of as “network clients” that communicate with each other through communication channels of a network that provide one or more levels of service, e.g., as may be achieved by various communication properties. *See Exhibit C*.

33. The 2001 paper by Dally and Towles provides a basic example of a NoC implementation. *See Exhibit C*. It describes dividing a chip into 16 “tiles,” where each tile comprises client logic, such as processors, DSPs, peripheral controllers, memory subsystems, and so on. The client logic within a tile (i.e., nearby logic) may communicate via direct interconnections, but client logic in different tiles (i.e., far-apart logic) must communicate only over the network. In other words, there are no top-level (global) bus-based interconnections, only interconnections provided by the network. Figure 1 of **Exhibit C** is reproduced below. *See Exhibit C*, Sec. 2.

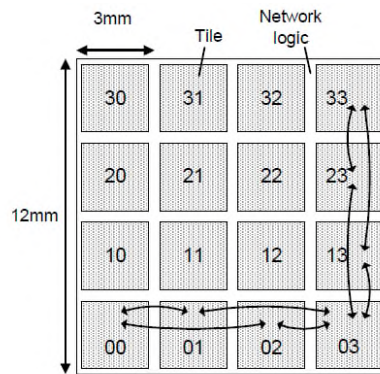


Figure 1 Partitioning the die into module tiles and network logic

34. Each tile interfaces with the network over an input port that is used to insert packets into the network and an output port over which the network delivers packets to the tile (where input and output here refer to packets going in and out of the network, not the tile). Each packet includes a virtual channel field that specifies which virtual channel it may be routed on, to provide different levels of service, and route field to specify a route through the network, i.e., the hops taken from source tile to destination tile. Such a port interface can present a simple and reliable level of service to the network clients. See **Exhibit C**, Sec. 2.1.

35. Logic local to the network clients can layer higher level services on top of this interface. For example, this local logic could present a memory read/write service, a flow-controlled data stream, or a logical wire to the client. Local logic can also provide a translation from a destination node to a route. See **Exhibit C**, Sec. 2.2.

36. The router needed at each tile consists of five input controllers (one for each direction and one for input from the tile) and five output controllers. The router for each tile is distributed across the four edges of a tile with the input and output controller for a given direction (e.g., west) located on that edge of the tile. Figure 2 of **Exhibit C**, reproduced below,

shows the west input controller and its connection to four output controllers (one for each of the other directions and one for the tile). See **Exhibit C**, Sec. 2.3.

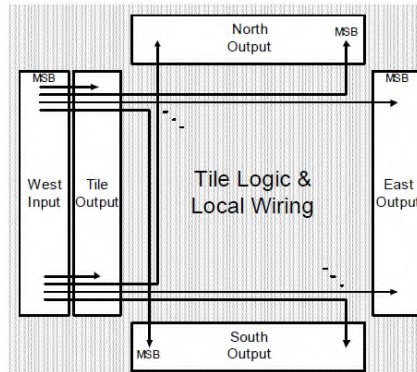


Figure 2 West input connections to output controllers

37. Details of an input controller and output controller are shown in Figure 3 of **Exhibit C**, reproduced below. Each input controller has an input buffer and input state logic for each virtual channel. When a head flit (flow control digit, e.g., part of a packet) arrives at each tile, the input controller strips the next entry off the route field and uses these two bits to select one of four output ports. The flit then arbitrates with the other virtual channels on that input port and, if it wins the arbitration, is forwarded to the output port. This arbitration and forwarding takes place in parallel with allocating a virtual channel and checking available buffer space to reduce latency. The output port provides a single stage of buffering for each input port connection. The flits in these buffers arbitrate for the link to the input controller on the next tile. Credits for buffer allocation are piggybacked on flits travelling in the reverse direction. See **Exhibit C**, Sec. 2.3.

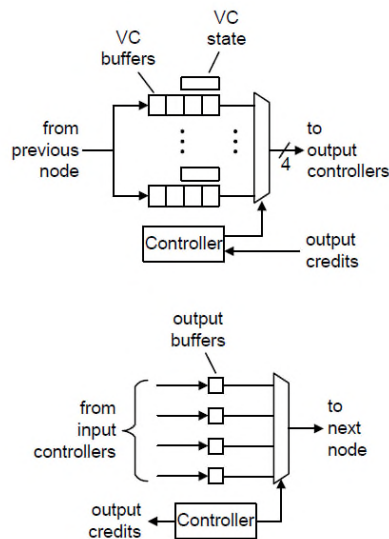


Figure 3 Input (top) and output controllers

38. As indicated earlier, the communication between the modules (e.g., components, network clients, etc.) are performed over connections. **Dkt. 1, Exhibit 1**, 6:36–38; *see also* **Dkt. 1, Exhibit 2**, 8:17–18; **Dkt. 1, Exhibit 3**, 4:53–55; **Dkt. 1, Exhibit 4**, 4:56–58; **Dkt. 1, Exhibit 6**, 5:16–18. The specification passages for each of the five Asserted Patents that utilize the claim term “connection” further indicate that the channels between modules have a set of connection properties. *See id.* Some examples of connection properties, which are sometimes called communication properties, are provided below.

The connection properties may include ordering (data transport in order), flow control (a remote buffer is reserved for a connection, and a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data), throughput (a lower bound on throughput is guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data), transmission termination, transaction completion, data correctness, or data delivery.

Dkt. 1, Exhibit 1, 6:48–56; *see also* **Dkt. 1, Exhibit 2**, 8:62–9:3; **Dkt. 1, Exhibit 3**, 4:64–5:5; **Dkt. 1, Exhibit 4**, 5:3–11; **Dkt. 1, Exhibit 6**, 5:27–35.

39. With such connection properties, on-chip networks are typically able to provide varying levels of communication service, which may be referred to as a quality of service (QoS) levels. “The QoS is a very important feature in the interconnect infrastructures because it

provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic.” **Exhibit E**, 315. Traffic here refers to a flow of data between a first module and a second module, for example, a series of data packets transmitted from the first module to the second module. With QoS, different traffic classes can be supported. **Exhibit E** describes four classes:

- Real time and low latency (RTLL)—Traffic flows that require the lowest possible latency.
- Guaranteed throughput (GT)—Traffic flows that must maintain their throughput over a relatively long time interval.
- Guaranteed bandwidth (GBW)—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval.
- Best effort (BE)—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

Exhibit E, 316.

40. The Asserted Patents disclose various inventions related to the systems described above. A high-level and noncomprehensive characterization of each patent is provided below.

41. U.S. Patent 7,366,818 discloses an integrated circuit including an on-chip network where the interfaces between modules and the network are able to drop data, for example, as a way to implement certain connection properties. (**Dkt. 1, Exhibit 1.**)

42. U.S. Patent 7,373,449 discloses an integrated circuit including an on-chip network where resource managers of the chip are configured to provide a communication channel between modules that have connection properties, where connection properties between different communication channels are independently configurable. (**Dkt. 1, Exhibit 2.**)

43. U.S. Patent 7,594,052 discloses an integrated circuit including an on-chip network where the interfaces between modules and the network are configured to map between a requested communication service and specific connection properties. (**Dkt. 1, Exhibit 3.**)

44. U.S. Patent 7,769,893 discloses an integrated circuit including an on-chip network where the interfaces between the modules and the network are configured to translate between different address formats for the modules. (**Dkt. 1, Exhibit 4.**)

45. U.S. Patent 8,072,893 discloses an integrated circuit including an on-chip network where data storage elements are introduced on certain slower communication channels to introduce a delay to resynchronize the slower channels with other channels. (**Dkt. 1, Exhibit 5.**)

46. U.S. Patent 8,086,800 discloses an integrated circuit including an on-chip network where interconnect utilization is improved by buffers that prevent data from entering the network until an optimal amount of data is available for transmission on the network. (**Dkt. 1, Exhibit 6.**)

V. CLAIM CONSTRUCTION

47. I am informed and understand that claims 1–7 of the '818 patent; claims 10–16 of the '449 patent; claim 6 of the '052 patent; claims 4–11 of the '9893 patent; claim 10 of the '2893 patent; and claim 12 of the '800 patent are all in dispute.

48. I am informed and understand that the following claim terms of the Asserted Patents are in dispute:

No.	Claim Term	Appears In
1	“connection”	'818 patent: claim 1 '449 patent: claims 10, 13–16 '052 patent: claim 6 '9893 patent: claims 4–11 '800 patent: claim 12
2	“dropping means (DM) for dropping data exchanged by said first and second module (M, S) / a first dropping means (DM) for dropping data / said dropping means (DM)”	'818 patent: claims 1, 3, 5

3	“resource manager determining whether a target connection with the desired connection properties is available”	’449 patent: claims 10, 14, 15
4	“communication manager”	’449 patent: claim 10
5	“interconnect means”	’052 patent: claims 1, 6, 7
6	“arranging . . . the first and the second information comprising said issued message as a single address”	’9893 patent: claim 4
7	“each data package comprising N data elements”	’2893 patent: claim 10
8	“data package”	’2893 patent: claim 1
9	“data storage elements”	’2893 patent: claim 1
10	“optimal amount of data”	’800 patent: claim 12
11	“optimal moment for sending the data in said first wrapper or said second wrapper”	’800 patent: claim 12
12	“first determination unit” / “second determination unit”	’800 patent: claim 12
13	“said first wrapper” / “said second wrapper”	’800 patent: claim 12
14	“wrapper”	’800 patent: claim 12

See Dkt. 77 (Defendants’ Joint Opening Claim Construction Brief (“Opening Br.”)).).

49. In my opinion, a POSITA would understand these terms to have the meanings as described below.

A. “connection”

50. I understand that NST contends this term means “one or more communication channels.”

51. I understand that Defendants contend this term means “one or more channels, each having a set of connection properties, between a first module and at least one second module, that are created before use and closed after use.”

52. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

53. The term “connection” is used in asserted claims of five of the six Asserted Patents (’818 Patent, ’449 Patent, ’052 Patent, ’9893 Patent, and ’800 Patent). Each of these five patents provides a characterization of “connection,” reproduced below, which is consistent between all five patents and with NST’s construction of the term. Included below each characterization is an excerpt of how the term “connection” is used in the relevant asserted claim or claims of the respective patent, where each use is consistent with the use of the term in the respective specification and with NST’s proposed construction of the term.

’818 Patent—

- **Specification:** “A connection is considered as a set of channels, each having a set of connection properties, between a first module and at least one second module.”

Dkt. 1, Exhibit 1, 6:36–38.

- **Claims:** “[P]roviding at least one connection between a first and at least one second module (M, S), . . .” **Dkt. 1, Exhibit 1, 12:7–9 (claim 1).**

’449 Patent—

- **Specification:** “Said connections comprises a set of communication channels each having a set of connection properties.” **Dkt. 1, Exhibit 2, 8:17–18.**
- **Claims:** “Method for exchanging messages in an integrated circuit comprising a plurality of modules, the messages between the modules being exchanged over connections via a network, . . . comprising the steps of: . . . the target connection between the first and second module being established based on the available

properties of said communication channels of said connection.” **Dkt. 1, Exhibit 2**, 19:21–20:6 (claim 10).

’052 Patent—

- **Specification:** “A connection is considered as a set of channels, each having a set of connection properties, between a first module and at least one second module.” **Dkt. 1, Exhibit 3**, 4:53–55.
- **Claims:** “Method . . . wherein at least one first of said processing modules (M) requests at least one communication service to at least one second processing module (S) . . . [the method] comprising the steps of: . . . enabling a connection based communication having a set of connection properties, . . . mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties . . .” **Dkt. 1, Exhibit 3**, 10:7–30 (claim 6).

’9893 Patent—

- **Specification:** “A connection is considered as a set of channels, each having a set of connection properties, between a first module and at least one second module.” **Dkt. 1, Exhibit 4**, 4:56–58.
- **Claims:** “[M]essages between the plurality of modules being exchanged via a network wherein a message issued by an addressing module M comprises: . . . a connection identifier identifying two or more message receiving modules S . . .” **Dkt. 1, Exhibit 4**, 12:41–48 (claim 4).
- **Claims:** “The method according to claim 5, wherein a connection comprises a set of channels, each channel having a set of connection properties between said

addressing module M and at least one message receiving module.” **Dkt. 1,**

Exhibit 4, 13:7–10 (claim 6).

’800 Patent—

- **Specification:** “A connection is considered as a set of channels, each having a set of connection properties, between a first module and at least one second module.” **Dkt. 1, Exhibit 6,** 5:16–18.
- **Claims:** “[P]rovide a communication connection between the first processing module and the second processing module, . . .” **Dkt. 1, Exhibit 6,** 11:56–58 (claim 12).

What is not provided in all five patents is support for additional functional steps provided in Defendants’ proposed construction, specifically, that connections “are created before use and closed after use.” For example, Defendants’ Joint Opening Claim Construction Brief concedes in footnote 5 on page 7 that only four of the five patents contain the passage Defendants rely on as support for the additional language in Defendants’ proposed construction:

The connections according to the embodiments of the invention must be first created or established with the desired properties before being used. . . . After usage, connections are closed, which leads to freeing the resources occupied by that connection.

Dkt. 1, Exhibit 1, 10:24–33; *see also* **Dkt. 1, Exhibit 2,** 10:62–11:3; **Dkt. 1, Exhibit 4,** 10:34–42; **Dkt. 1, Exhibit 3,** 5:44–49¹. The ’800 Patent does not include the above passage, or even a similar passage. Rather, the ’800 Patent includes just one reference to establishing a connection, which is part of a conditional phrase, which does not use the words “created” or “closed,” and which does not disclose or suggest terminating a connection after use: “[a]lternatively, the

¹ The language on the ’052 patent is slightly different than that of the other cited patents.

optimal burst length **may be** determined dynamically (1) every time a connection is set up for transferring data over the network” **Dkt. 1, Exhibit 6**, 6:56–58 (emphasis added). It is therefore my opinion that a POSITA, reading the asserted claims that use the term “connection” in the context of every respective Asserted Patent, would not understand the term “connection” to include the additional functional steps that Defendants proposed.

54. Defendants’ Joint Opening Claim Construction Brief (Dkt. 77) and Defendants’ Declaration of Dr. Marwan Hassoun (Dkt. 77-1) dedicate many pages each discussing “connection-oriented service” and “connectionless service,” where said brief and said declaration synonymize “connection based” and “connection-oriented.” Opening Br. At 8-11, Dkt 77-1 at 17-22. While a POSITA would understand one or more distinctions between connection-oriented service and connectionless service, these distinctions are inapposite for understanding the meaning of “connection” as it is used in the Asserted Patents.

55. For example, the specification of the ’818 Patent states “[i]n another alternative embodiment of the invention, the **transaction completion can be implemented in systems which are not connection based, as such a system is equivalent to a system with a single connection.**” **Dkt. 1, Exhibit 1**, 11:28–31. First, this passage states a system that is not connection-based is equivalent to a system with a single connection, thereby dispelling a notion that only connection-based systems can have a connection. Second asserted claim 1 of the ’818 patent recites:

[a]n integrated circuit comprising . . . a network (N; RN) arranged for **providing at least one connection** . . . wherein said **connection supports transactions** [and] wherein the dropping of data and therefore **the transaction completion can be controlled** by the interface means.

Dkt. 1, Exhibit 1, 12:5–25 (claim 1) (emphasis added). To reiterate, the integrated circuit of claim 1: (1) includes a network that *provides a connection*; and (2) and *implements transaction*

completion. As explained above, the specification of the '818 Patent states “transaction completion can be implemented in systems that are *not* connection based.” **Dkt. 1, Exhibit 1**, 11:29–30. Therefore, whether a system is connection-based is immaterial; the touchstone is whether the system uses connections. Indeed, Defendants’ Joint Opening Claim Construction Brief appears to conflate systems that do not use connections with systems that are connection based:

The patents also explain that certain aspects of the invention can be used in systems that **do not use connections**. '818 patent at 11:28-31 (In another alternative embodiment of the invention, the transaction completion can be implemented in systems **which are not connection based**”); '052 patent at 8:47-51 (“[T]he above described mapping is relevant for communication protocols **which do not include the notion of connection**”).

Opening Br. At 11 (emphasis in original). To be clear, “not connection based” is different than not using connections. Similarly, “notion of connection” is different than a connection and/or using a connection. Defendants’ and Dr. Hassoun’s reliance on inapposite “telephone system” and “postal service” analogies, (Dkt. 77-1 at ¶ 8) does not compel a different conclusion.

56. As explained earlier, the specifications of the Asserted Patents characterize a connection as a set of communication channels. See **Dkt. 1, Exhibit 1**, 6:36–38; **Dkt. 1, Exhibit 2**, 8:17–18; **Dkt. 1, Exhibit 3**, 4:53–55; **Dkt. 1, Exhibit 4**, 4:56–58; **Dkt. 1, Exhibit 6**, 5:16–18. NST’s proposed construction for “connection” is “one or more communication channels.” THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS (7th ed. 2000) provides the following definitions for “communication,” “channel,” and “communication channel”:

Communication:

- (1) (data transmission) (electric systems) (telecommunications) The transmission of information from one point to another by means of electromagnetic waves.
- (2) The flow of information from one point, known as the source, to another, the receive.

Channel:

- (A) (electric communication) A single path for transmitting electric signals, usually in distinction from other parallel paths. (B) (electric communication) A band of frequencies. Note: The word “path” is to be interpreted in a broad sense to include separation by frequency division or time division. The term “channel” may signify either a one-way path, providing transmission in one direction only, or a two-way path, providing transmission in two directions. (EEC/PE) [119], 599-1985. The Authoritative Dictionary of IEEE Standards Terms (7th ed. 2000)
- (10) A logically independent data path between two Functions. Multiple channels can be used to reach different Functions or to represent independent instances of inter-unit communication. (C/MM) 1212.1-1993
- (15) A single flow path for digital data or an analog signal, usually in distinction from other parallel paths. An IEEE 1451.2 channel provides a path for a single commodity or logical state, either real or virtual, using a single data model and a single set of physical units. (IM/ST) 1451.2-1997
- (17) A physical or logical communication link to a single transducer or to a group of transducers considered as a single transducer. (IM/ST) 1451.1-1999

Communication Channel:

- A facility that permits signaling between terminals.

57. Other authoritative sources provide similar definitions. What is clear from these definitions is that a communication channel is a channel for the transmission of information (e.g., data), and the channel can include physical and virtual aspects. A POSITA understands that a physical aspect of a channel may include a physical medium, such as a wire. *See, e.g., Dkt. 1, Exhibit 1*, 2:47–48 (“Luckily, on-chip wires provide a reliable communication medium, . . .”); *see also Dkt. 1, Exhibit 2*, 2:46–47. Further, a POSITA understands that a virtual aspect of a channel may include a virtual-circuit configuration of a connection-oriented service. *See, e.g., Dkt. 77-1 at ¶ 46* (“IEEE 100 Authoritative Dictionary of IEEE Standard Terms Seventh Edition . . . includes the following definition[] for “connection-oriented service” Connection-

Oriented Service: A kind of delivery service where different **virtual circuit configurations are used to transmit messages.**” (emphasis added)). Note that “[i]n the virtual circuit approach, a preplanned route is established before any packets are sent.” WILLIAM STALLINGS, DATA & COMPUTER COMMUNICATIONS P. 307 (6th ed. 1999) (**Exhibit K**). Thus, NST’s proposed construction of “connection” as “one or more communication channels” is consistent with all asserted claims and all respective specifications including references to “connection-oriented” or “connection based” in the specifications, without requiring inclusion of additional functional steps proposed by Defendants. NST’s proposed construction does not “seek[] to untether this term from the actual invention disclosed in the patents. . . . [nor] require[] nothing more than a wire, . . .” Opening Br. At 10.

58. Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

B. “dropping means (DM) for dropping data exchanged by said first and second module (M, S) / a first dropping means (DM) for dropping data / said dropping means (DM)”

59. I understand that NST contends “dropping means” means “circuit configured to drop messages,” and the remaining language should be afforded its plain and ordinary meaning (not subject to Section 112 ¶ 6). If the Court holds that Section 112 ¶ 6 applies, I understand that NST proposes the following construction: the function for claim 1 is “drop data exchanged by said first and second module,” the function for claim 3 is the function for claim 1 plus “create an error message if data is dropped,” and the function for claim 5 is the function for claim 3 plus “send said error message to said first module,” and the structure is “circuit.”

60. I understand that Defendants contend this term is subject to Section 112 ¶ 6. I understand that Defendants further contend the function for claim 1 is “dropping data exchanged

by said first and second module (M, S),” the function for claim 3 is the function for claim 1 plus “creating an error message if data is dropped,” and the function for claim 5 is the function for claim 3 plus “sending said error message to said first module (M),” and the structure is indefinite.

61. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

62. I understand that NST and Defendants have stipulated “integrated circuit” means “interconnected circuitry on a chip.” Opening Br. At 6. In my opinion, this meaning is consistent with how a POSITA reading the Asserted Patents would understand this term, and it is consistent with authoritative extrinsic sources, for example, THE NEW IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONICS TERMS, (5th ed. 1993), which defines an “integrated circuit” as “[a] combination of interconnected circuit elements inseparably associated on or within a continuous substrate.” **Exhibit I**; *see also* **Exhibit G**. The ’818 Patent describes the dropping means as being comprised in an integrated circuit. Accordingly, the dropping means is interconnected circuitry of the integrated circuit, i.e., the dropping means is a circuit, as explained below.

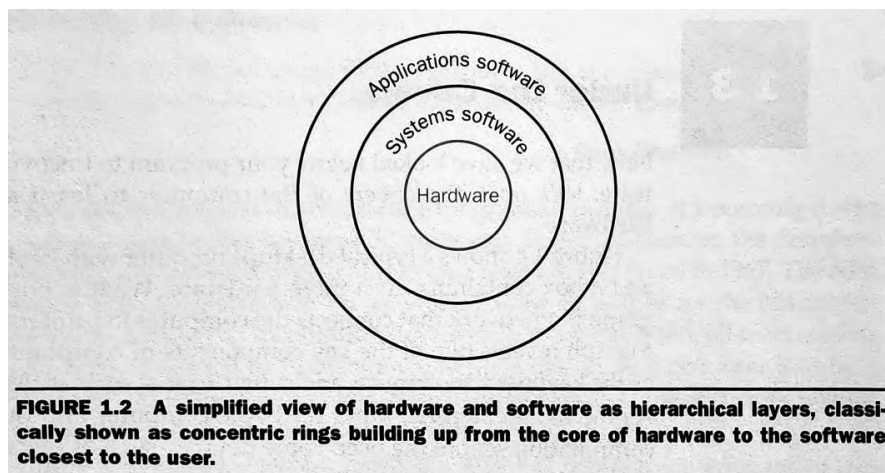
63. First, the specification of the ’818 Patent states “[s]aid **integrated circuit** comprises at least one dropping means” **Dkt. 1, Exhibit 1**, Abstract (emphasis added); *see also* **Dkt. 1, Exhibit 1**, 5:27–28. Because an integrated circuit is interconnected circuitry on a chip, a POSITA would understand that the dropping means comprised in an integrated circuit discloses that the dropping means is interconnected circuitry of the integrated circuit, i.e., the dropping means is a circuit.

64. Second, the specification of the '818 Patent states “[a]ccording to an aspect of the invention, **an integrated circuit comprising at least one interface means** ANIP, PNIP for managing the interface between a module M, S and the network N, RN is provided, **wherein said interface means ANIP, PNIP comprises a first dropping means . . .**” **Dkt. 1, Exhibit 1**, 5:37–41. Because an integrated circuit is interconnected circuitry on a chip, a POSITA would understand that the interface means comprised in an integrated circuit discloses that the interface means is interconnected circuitry of the integrated circuit, i.e., the interface means is a circuit. This is confirmed by a passage in the '818 Patent stating the “interface means ANIP, PNIP is **adapted to store received error messages.**” **Dkt. 1, Exhibit 1**, 5:65–66 (emphasis added). For the interface means to store messages, it must comprise storage circuitry such as flip-flops, latches, registers, random-access memory (RAM), and so on. Thus, a POSITA would understand that the dropping means comprised in the interface means discloses that the dropping means is circuitry of the interface means, i.e., the dropping means is a circuit.

65. Third, the specification of the '818 Patent states before the claims section that “[i]n the device claim enumerating several means, several of these **means can be embodied by one and the same item of hardware.**” **Dkt. 1, Exhibit 1**, 11:41–43 (emphasis added). A POSITA understands the term “hardware” to mean physical circuitry. For example, the DICTIONARY OF COMPUTER AND INTERNET TERMS (7th ed. 2000) defines hardware as “the physical elements of a computer system; the computer equipment as opposed to the programs or information stored in the machine.” (**Exhibit M**). This term is often used in contrast with the term “software,” which a POSITA understands as describing instructions for execution by computer hardware, e.g., by physical circuitry like a processor (sometimes called a central processing unit (CPU)). For example, the DICTIONARY OF COMPUTER AND INTERNET TERMS (7th

ed. 2000) defines software as “programs that tell a computer what to do. The term contrasts with *hardware*, which refers to the actual physical machines that make up a computer system.”

(emphasis in original) (**Exhibit M**). The figure below shows a simplified hierarchical view of the hardware-software interface, with hardware at the core and software on the periphery for execution by the core. DAVID PATTERSON AND JOHN HENNESSEY, *COMPUTER ORGANIZATION & DESIGN* § 1, P. 9 (2nd ed. 1998) (**Exhibit N**).



66. From the '818 Patent, “FIG. 2 shows a system on chip . . . compris[ing] two modules, namely a master M and a slave S module, a router network RN, and two network interfaces ANIP, PNIP between the modules and the router network RN. . . . The active network interface ANIP as well as the passive network interface PNIP comprise a dropping manager DM, respectively.” **Dkt. 1, Exhibit 1**, 7:23–48. In the '818 Patent, a dropping means DM is sometimes called a dropping manager DM, and a network interface is sometimes called an interface means. FIG. 2 is reproduced below.

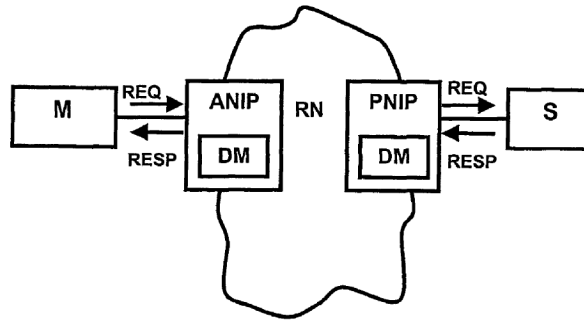


FIG.2

67. As indicated in the passage and figure immediately above, each network interface is disposed *between* a respective module and the router network, suggesting that the network interface is circuitry on a datapath between the respective module and the router network. This is confirmed at least because the interface means can store messages sent to a module. **Dkt. 1, Exhibit 1**, 5:60–66. (“[S]aid dropping means DM are adapted to send said error message to said first module M [and the] interface means ANIP, PNIP is adapted to store received error messages.”). Similarly, the dropping means is also circuitry on the datapath between the respective module and the router network for at least the same reason, and more specifically, at least because the dropping means is adapted to create, send, receive, and drop messages. **Dkt. 1, Exhibit 1**, 5:51 (“[D]ropping means DM are adapted to create an error message . . .”); **Dkt. 1, Exhibit 1**, 5:56–59 (“[D]ropping means DM are adapted to send said error message to a first dropping means DM. Hence, error messages are send [sic] to the dropping means in the interface means.”); **Dkt. 1, Exhibit 1**, 5:61–62 (“[D]ropping means DM are adapted to send said error message to said first module M.”); **Dkt. 1, Exhibit 1**, 7:48–51 (“These dropping managers DM are responsible for the dropping of data or messages [sic], i.e. only the network interfaces are able to drop data or messages.”).

68. A POSITA understands that messages or data that are created, sent, received, and/or dropped by the dropping means comprise electrical signals, e.g., voltages and/or currents, that are physically manipulated by the dropping means to effectuate the creating, sending, receiving, and dropping of these messages or data. A POSITA further understands that the electrical signals of the messages or data of the systems-on-chip (SoCs) described in the '818 patent can be represented, or abstracted, by binary digits, or “bits,” which can take on a value of logic-0 (commonly a low voltage level) or logic-1 (commonly a high voltage level).

Digital logic hides the pitfalls of the analog world by mapping the infinite set of real values for a physical quantity into two subsets corresponding to just two possible numbers or *logic values*—0 and 1. Thus, digital logic circuits can be analyzed and designed functionally, using switching algebra, tables, and other abstract means to describe the operation of well-behaved 0s and 1s in a circuit. A logic value, 0 or 1, is often called a *binary digit*, or *bit*.

JOHN F. WAKERLY, DIGITAL DESIGN: PRINCIPLES AND PRACTICES 80 (4th ed. 2005) (emphasis in original) (**Exhibit D**).

69. A POSITA therefore understands how to design and build circuitry adapted to create, send, receive, store, and/or drop messages or data in an SoC, for example:

- create a message by injecting electrical charge (high voltage) to represent logic-1 bits of the message and remove electrical charge (low voltage) to represent logic-0 bits of the message;
- send a message by modulating high and low voltages on a wire corresponding to the bits of the message;
- receive a message by detecting the high and low voltages corresponding to the bits of the message;
- store a message by storing in storage circuitry the electrical charges (high and low voltages) corresponding to the bits of the message; and

- drop a message by discarding to an electrical ground the electrical charges (high and low voltages) corresponding to the bits of the message.

70. Footnote 6 of Defendants' Joint Opening Claim Construction Brief suggests that "the dropping means need not be a circuit; rather, the dropping functions can be implemented as software or firmware operated by general purpose hardware in the integrated circuit. Hassoun Decl. at ¶63."). Opening Br. at 12. However, this is not suggested by the '818 Patent at least because there is no mention of software or firmware anywhere in the '818 patent, and moreover, a POSITA would not recognize software or firmware operated by general purpose hardware as "as a solution to the interconnect problem in highly-complex chips [at least because] NoCs help resolve the electrical problems in new deep-submicron technologies, as they structure and manage global wires." See **Dkt. 1, Exhibit 1**, 1:37–41. Networks-on-chip (NoCs) comprise circuitry that is designed and built specifically to provide data communication within the chip:

Networks on chip (NoC) have received considerable attention recently as a solution to the interconnect problem in highly-complex chips. The reason is twofold. First, NoCs help resolve the electrical problems in new deep-submicron technologies, as they structure and manage global wires. At the same time they share wires, lowering their number and increasing their utilization. NoCs can also be energy efficient and reliable and are scalable compared to buses. Second, NoCs also decouple computation from communication, which is essential in managing the design of billion-transistor chips. NoCs achieve this decoupling because they are traditionally designed using protocol stacks, which provide well-defined interfaces separating communication service usage from service implementation.

Dkt. 1, Exhibit 1, 1:37–50. Indeed, the '818 Patent dispels the notion of including a processor (which is a general-purpose hardware for executing software or firmware²) in a network interface of an on-chip network, where the dropping means are comprised in the network interface. **Dkt. 1, Exhibit 1**, 2:22–25. ("Including a dedicated processor in a network interface is **not feasible on**

² The '818 Patent mentions MIPS as an example of a processor (**Dkt. 1, Exhibit 1**, 3:4–5), where MIPS is a well-known reduced instruction set computer (RISC) processor.

chip, as the size of the network interface will become comparable to or larger than the IP³ to be connected to the network.”) (emphasis added).

71. Given the totality of evidence, it is my opinion that the correct understanding that a POSITA would have of “dropping means,” as used in the Asserted Patents, is the meaning provided by NST of “circuit configured to drop messages.”

72. I understand the Court may determine this term should be construed under 35 U.S.C. § 112 ¶ 6, means-plus-function. In this event, it is my opinion that NST’s proposed structure for this term with respect to claims 1, 3, and 5, of “circuit” is correct and Defendants’ proposed structure for this term with respect to claims 1, 3, and 5, as indefinite (no structure disclosed), is not correct. In my opinion, the functions proposed by NST and Defendants for this term with respect to claims 1, 3, and 5 are substantially the same but for differences in verb tense and Defendant’s inclusion of abbreviations “(M,S)” and “(M)” after instances of the word “module.”

73. First, independent claim 1 of the ’818 Patent recites “an integrated circuit comprising at least one dropping means (DM) for dropping data exchanged by said first and second module (M, S), . . .” **Dkt. 1, Exhibit 1**, 12:6–18. In other words, the function of the dropping means is to drop data exchanged by the first and second modules. Indeed, the specification directly supports this function, describing “an integrated circuit comprising at least one interface means ANIP, PNIP . . . , wherein said interface means ANIP, PNIP comprises a first dropping means DM for dropping data.” **Dkt. 1, Exhibit 1**, 5:37–42.

³ “The modules as described in FIGS. 1 and 2 can be so-called intellectual property blocks IPs (computation elements or memories, but not interconnection elements) that interact with network at said network interfaces NI.” **Dkt. 1, Exhibit 1**, 10:11–18.

74. Claims 3 and 5 of the '818 Patent provide further limitation on the dropping means, where claim 3 recites “said dropping means (DM) are adapted to create an error message if data is dropped,” (**Dkt. 1, Exhibit 1**, 12:29–31) and claim 5 recites “said dropping means (DM) are adapted to send said error message to said first module (M)” (**Dkt. 1, Exhibit 1**, 12:36–38). The specification directly supports these limitations, as well as others, as indicated below.

According to still a further aspect of the invention, said dropping means DM are adapted to create an error message if data is dropped. Therefore, a source of said data is informed of the dropping of the data, so that it can re-send said data later on, which will be part of another transaction.

Dkt. 1, Exhibit 1, 5:50–54.

According to still a further aspect of the invention, said dropping means DM are adapted to send said error message to said first module M. The error messages are directly send [sic] to the first module.

Dkt. 1, Exhibit 1, 5:60–63.

75. Thus, in my opinion, the function of the “dropping means” under 35 U.S.C. § 112 ¶ 6, with respect to claim 1, is to “drop data exchanged by said first and second module.” In my opinion, the function of the “dropping means” under 35 U.S.C. § 112 ¶ 6, with respect to claim 3, is the function according to claim 1 plus to “create an error message if data is dropped.” In my opinion, the function of the “dropping means” under 35 U.S.C. § 112 ¶ 6, with respect to claim 5, is the function according to claim 1 plus to “send said error message to said first module.”

76. As explained earlier in this section, a POSITA would recognize the structure of the dropping means to be a circuit. *Supra* ¶¶ 62–71.

77. Thus, it is my opinion that if the Court determines this term should be construed under 35 U.S.C. § 112 ¶ 6, then the correct understanding that a POSITA would have of this term as used in the Asserted Patents is the meaning provided by NST.

C. “resource manager determining whether a target connection with the desired connection properties is available”

78. I understand that NST contends “resource manager” means “circuit that manages network resources,” and the remaining language should be afforded its plain and ordinary meaning.

79. I understand that Defendants contend this term means “resource manager determining whether a connection between modules with desired properties is available to be opened and is not an arbiter prioritizing which port of a switching device is to be utilized.”

80. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

81. I understand that NST and Defendants have stipulated “integrated circuit” means “interconnected circuitry on a chip.” Opening Br. at 6. In my opinion, this meaning is consistent with how a POSITA reading the Asserted Patents would understand this term, and it is consistent with authoritative extrinsic sources, for example, THE NEW IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONICS TERMS, (5th ed. 1993), which defines an “integrated circuit” as “[a] combination of interconnected circuit elements inseparably associated on or within a continuous substrate.” **Exhibit I**; *see also* **Exhibit G**. The ’449 patent describes the resource manager as being comprised in an integrated circuit. Accordingly, the resource manager is interconnected circuitry of the integrated circuit, i.e., the resource manager is a circuit, as explained below.

82. Recall that a system-on-chip and a system-on-silicon are examples of integrated circuits in which most or all components of a system are integrated, including memories, processors, high-speed I/O interfaces, and dedicated application-specific logic. *See, e.g., Exhibit*

A, 29; *see also* **Exhibit B**, 380–381, 395, 487. This is consistent with the use of these terms in the ’449 Patent, for example:

Systems on silicon show a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions. This is enabled by the increasing density with which **components can be integrated on an integrated circuit**. At the same time the clock speed at which circuits are operated tends to increase too. The higher clock speed in combination with the increased density of components has reduced the area which can operate synchronously within the same clock domain. . . . A communication network forms an effective way to overcome these disadvantages.”

Dkt. 1, Exhibit 2, 1:15–35 (emphasis added); *see also* **Dkt. 1, Exhibit 1**, 1:16–36; **Dkt. 1, Exhibit 3**, 1:14–32; **Dkt. 1, Exhibit 4**, 1:14–34; **Dkt. 1, Exhibit 6**, 1:14–32.

The following embodiments relate to **systems on chip, i.e. a plurality of modules on the same chip** communicate with each other via some kind of interconnect.

Dkt. 1, Exhibit 2, 8:43–45 (emphasis added).

83. First, the specification of the ’449 Patent states “FIG. 3 shows a system on chip [that] comprises a communication manager CM and a resource manager RM.” **Dkt. 1, Exhibit 2**, 9:66–10:3. Because a system-on-chip (SoC) is an integrated circuit, and an integrated circuit is interconnected circuitry on a chip, a POSITA would understand that the resource manager comprised in an SoC integrated circuit discloses that the resource manager is interconnected circuitry of the integrated circuit, i.e., the resource manager is a circuit.

84. Second, the specification of the ’449 Patent states that “[a]ccording to an aspect of the invention, said **integrated circuit comprises . . . at least one resource managing means RM for managing the resources of the network N.**” **Dkt. 1, Exhibit 2**, 7:35–39 (emphasis added). In the ’449 patent, the resource manager RM is sometimes called the resource managing means RM. FIG. 3 is reproduced below.

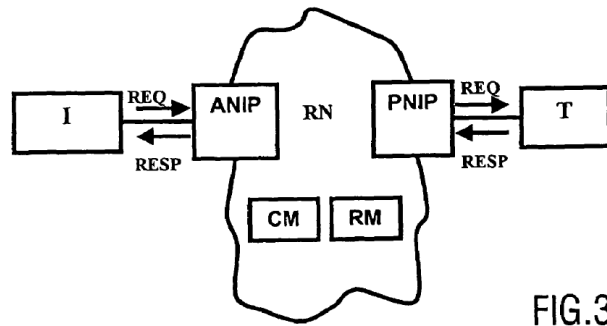


FIG.3

85. Because an integrated circuit is interconnected circuitry on a chip, a POSITA would understand that the resource manager comprised in an integrated circuit discloses that the resource manager is interconnected circuitry of the integrated circuit, i.e., the resource manager is a circuit.

86. Third, the specification of the '449 Patent states that "FIG. 3 shows a system on chip [wherein] the communication manager CM and **the resource manager RM are arranged in the router network RN, but they can also be arranged in one or some of the network interfaces NI.**" Dkt. 1, Exhibit 2, 9:66–10:6 (emphasis added). The '449 Patent states in several places that the network, or router network, and the network interface means are comprised in an integrated circuit, as indicated below.

An **integrated circuit comprising** a plurality of processing modules (M; I; S; T) and **a network (N; RN)** arranged for providing at least one connection between a first and at least one second module is provided.

Dkt. 1, Exhibit 2, Abstract (emphasis added).

The invention relates to an **integrated circuit having** a plurality of processing modules and **a network** arranged for providing connections between processing modules and a method for exchanging messages in such an integrated circuit.

Dkt. 1, Exhibit 2, 1:7–11(emphasis added).

Therefore, and **integrated circuit comprising** a plurality of processing modules M; I; S; T and a **network N; RN** arranged for providing at least one connection between a first and at least one second module is provided.

Dkt. 1, Exhibit 2, 7:15–18 (emphasis added).

According to still a further aspect of the invention, said **integrated circuit comprises at least one network interface means N1**, associated to each of said modules, for managing the communication between said modules and said network N.

Dkt. 1, Exhibit 2, 8:7–11 (emphasis added).

FIG. 2 shows a **system on chip** according to a second embodiment. **The system comprises** two modules, namely an initiator I and a target T, **a router network RN, and two network interfaces ANIP, PNIP** between the modules and the router network RN.

Dkt. 1, Exhibit 2, 9:17–21 (emphasis added).

87. Thus, a POSITA would understand that the resource manager comprised in either the network or the interface means discloses that the resource manager is circuitry of the integrated circuit that comprises the network or the interface means, i.e., the resource manager is a circuit.

88. Fourth, the specification of the '449 Patent refers to the “resource manager” that is recited in claims 10, 14, and 15 as either the “resource manager” or the “resource managing means” in the specification.

According [sic] to an aspect of the invention, said integrated circuit comprises at least one communication managing means CM for managing the communication between different modules; and at least one resource managing means RM for managing the resources of the network N.

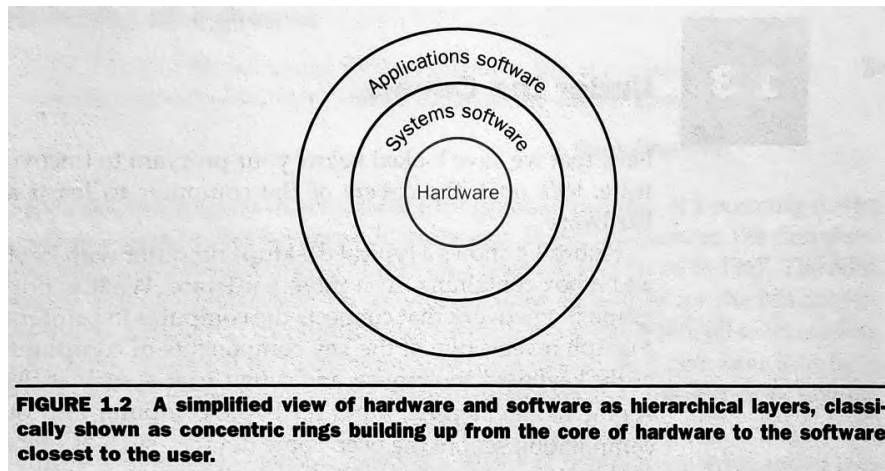
Dkt. 1, Exhibit 2, 7:35–39.

According to a further aspect of the invention, said first module M; I issues a request for a connection to at least one of said second modules to said communication managing means CM. Said communication managing means CM forwards the request for a connection with communication channels each having a specific set of connection properties to said resource managing means (RM). Said resource

managing means RM determines whether the requested connection based on said communication channels with said specific connection properties is available, and responds the availability of the requested connection to said communication managing means CM.

Dkt. 1, Exhibit 2, 7:40–51.

89. The specification of the '449 Patent states before the claims section that “[i]n the device claim enumerating several means, several of these **means can be embodied by one and the same item of hardware.**” **Dkt. 1, Exhibit 2**, 18:23–25 (emphasis added). A POSITA understands the term “hardware” to mean physical circuitry. For example, the DICTIONARY OF COMPUTER AND INTERNET TERMS (7th ed. 2000) defines hardware as “the physical elements of a computer system; the computer equipment as opposed to the programs or information stored in the machine.” (**Exhibit M**). This term is often used in contrast with the term “software,” which a POSITA understands as describing instructions for execution by computer hardware, e.g., by physical circuitry like a processor (sometimes called a central processing unit (CPU)). For example, the DICTIONARY OF COMPUTER AND INTERNET TERMS (7th ed. 2000) defines software as “programs that tell a computer what to do. The term contrasts with *hardware*, which refers to the actual physical machines that make up a computer system.” (emphasis in original) (**Exhibit M**). The figure below shows a simplified hierarchical view of the hardware-software interface, with hardware at the core and software on the periphery for execution by the core. DAVID PATTERSON AND JOHN HENNESSEY, COMPUTER ORGANIZATION & DESIGN § 1, p. 9 (2nd ed. 1998) (**Exhibit N**).



90. Based on the above evidence, it is my opinion that a POSITA would understand the resource manager to be a circuit.

91. Turning now to the “manages network resources” part of NST’s proposed construction for this term, the ’449 Patent describes the resource manager (sometimes called the “resource managing means”) as being configured to manage network resources. *See, e.g., Dkt. 1, Exhibit 2*, 7:38–39 (“at least one resource managing means RM for managing the resources of the network N.”).

92. First, independent claim 10 of the ’449 Patent recites “a method . . . comprising the steps of: . . . the resource manager determining whether a target connection with the desired connection properties is available; [and] the resource manager responding with the availability of the target connection to the communication manager.” **Dkt. 1, Exhibit 2**, 19:21–20:3. The specification describes these steps, for example:

“The communication manager CM request a connection with a set of properties between two modules from the resource manager RM, after receiving the request REQ from the active network interface ports ANIP, i.e. the properties of a connection, e.g. throughput, flow control, are to be requested when asking for a connection setup. **The resource manager RM allocates the necessary resources and enquires if such a connection based on these resources is possible.**”

* * *

After enquiring of the available connection properties, **the resource manager RM reserves the available connection i.e. the required resources, and responds to the communication manager CM which connection is available**, i.e. which connection properties or the required resources thereof are available for the desired channels.”

Dkt. 1, Exhibit 2, 10:19–26; 10:41–46 (emphasis added).

93. Claims 14 and 15 of the ’449 Patent provide further limitation on the resource manager, where claim 14 recites “the resource manager determining whether the target connection with the desired connection properties is available based on reading of a centralized or distributed property table comprising properties associated with the network,” (**Dkt. 1, Exhibit 2**, 20:15–19) and claim 15 recites “the resource manager reserving the target connection after determining whether the target connection with the desired connection properties is available.” (**Dkt. 1, Exhibit 2**, 20:20–23). The specification also supports these limitations, as indicated below.

The allocation of the resources can be preformed [sic] in two ways. First, **the resource manager RM may contain a property table with entries for all the different properties of the channels and connections. Alternatively, one central property table can be provided containing all different properties of the network, i.e. the table can either be central or distributed.**”

Dkt. 1, Exhibit 2, 10:34–40 (emphasis added).

After enquiring of the available connection properties, the resource manager RM reserves the available connection i.e. the required resources, . . .”

Dkt. 1, Exhibit 2, 10:41–44.

94. The functions of the resource manager described above are summarized below.

- Allocating resources for a connection.
- Enquiring if a connection based on these resources is possible.
- Reserving required resources.
- Notifying the CM of available required resources (e.g., connection properties).

- Maintaining a property table for connections.

95. Each of these steps is an example of managing network resources. Thus, it is my opinion that the correct understanding that a POSITA would have of “resource manager,” as used in the Asserted Patents, is the meaning provided by NST of “circuit that manages network resources.”

96. I understand that NST contends the second part of the term, “determining whether a target connection with the desired connection properties is available,” should be afforded its plain and ordinary meaning.

97. I understand that Defendants contend that this term means “determining whether a connection between modules with desired properties is available to be opened and is not an arbiter prioritizing which port of a switching device is to be utilized.”

98. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this part of the term as used in the Asserted Patents.

99. As shown by the evidence and explanations above, the resource manager is a circuit, and the resource manager is configured to manage network resources. *See, e.g., Dkt. 1, Exhibit 2*, 7:38–39 (“at least one resource managing means RM for managing the resources of the network N.”). The ’449 Patent describes several management functions of the resource manager RM, several examples of which are listed below. Indeed, the first three examples describe management functions that directly relate to the function described in the claim term “resource manager *determining whether a target connection with the desired connection properties is available.*” Consequently, a POSITA would understand a plain and ordinary meaning of this term as used in the Asserted Patents.

Said resource managing means RM determines whether the requested connection based on said communication channels with said specific

connection properties is available, and responds the availability of the requested connection to said communication managing means CM.

Dkt. 1, Exhibit 2, 7:46–51 (emphasis added).

The **resource manager RM allocates the necessary resources and enquires if such a connection based on these resources is possible** [where] the resource manager RM may contain a property table with entries for all the different properties of the channels and connections.

Dkt. 1, Exhibit 2, 10:24–37 (emphasis added).

After enquiring of the available connection properties, the resource manager RM reserves the available connection i.e. the required resources, and responds to the communication manager CM which connection is available, i.e. which connection properties or the required resources thereof are available for the desired channels.

Dkt. 1, Exhibit 2, 10:41–46 (emphasis added).

Otherwise, the resource manager RM sets the connection properties, and establishes a connection with accepted properties between said initiator and target modules. After said two modules I, T have performed the transactions as requested by the initiator module, the communication manager CM issues a request to said resource manager RM to reset the connection or the connection properties.

Dkt. 1, Exhibit 2, 10:55–61.

100. The Defendants contend that additional meaning should be given to the term “resource manager determining whether a target connection with the desired connection properties is available” that goes beyond the plain and ordinary meaning, specifically, “[whether a target connection with the desired properties is available] to be opened and is not an arbiter prioritizing which port of a switching device is to be utilized.” For the rest of the appended language, I understand Defendants contend this additional meaning is based on the prosecution history of the ’449 patent. However, the prosecution history does not justify the Defendants’ contention.

101. During prosecution, Examiner rejected claim 10 (then claim 7) based on a cited reference, Emerson (U.S. Patent Application No. 10/303,589; U.S. Publication No. 2004/0103230), that discloses an arbiter that the Examiner equated to the resource manager of the '449 patent. **Exhibit J** (Prosecution History of U.S. Patent No. 7,373,449), 12–13, 17–20. Applicant responded to the Office Action by arguing the following:

The Arbiter 112 of Emerson does not disclose or suggest . . . the resource manager determining whether the at least one connection with the communication channels is available based on the connection properties being available . . . , the resource manager determining whether a target connection with the desired connection properties is available, and the resource manager responding with the availability of the target connection to the communication manager.

Exhibit J, 13.

102. Concurrently, Applicant amended claim 10 (then claim 7) to include limitations concerning the resource manager in light of the missing features from Emerson, as highlighted in yellow in the excerpt taken from Applicant's Office Action Response shown below. **Exhibit J**, 9–10.

7. (Currently Amended) Method for exchanging messages in an integrated circuit comprising a plurality of modules, the messages between the modules being exchanged over connections via a network, wherein said connections comprises a set of communication channels each having a set of connection properties, any communication channel being independently configurable, wherein said connection through the network supports transactions comprising at least one of outgoing messages from the first module to the second module and return messages from the second module to the first module and further comprising the steps of:

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PATENT
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the first module issuing a request for a connection with the second module to a communication manager, wherein the request comprises desired connection properties associated with the sets of communication channels;
the communication manager forwarding the request to a resource manager;
the resource manager determining whether a target connection with the desired connection properties is available;
the resource manager responding with the availability of the target connection to the communication manager; and
the target connection between the first and second module being established based on the available properties of said communication channels of said connection.

103. The next correspondence from the Office was a Notice of Allowance, in which Examiner explains the reason for allowance as follows (where then claim 7 is issued claim 10 of the '449 Patent).

The following is an Examiner's statement of reasons for the indication of allowable subject matter: **Claims 1, 7, are allowable over the prior art of record because the prior arts, cited in its entirety, or in combination, do not teach wherein the resource manager determines whether the at least one connection with the communication channels is available based on the connection properties being available.**

Exhibit J, 6 (emphasis added).

104. Nothing in Applicant's remarks, Applicant's claim amendment, or Examiner's reasons for allowable subject matter concern whether the resource manager "is not an arbiter prioritizing which port of a switching device is to be utilized." To be clear, Applicant did not disclaim scope based on "an arbiter prioritizing which port of a switching device is to be utilized" because Applicant did not distinguish the resource manager from the arbiter thereby.

105. Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

D. “communication manager”

106. I understand that NST contends “communication manager” means “circuit that manages communication between modules” (not subject to Section 112 ¶ 6). If the Court holds that Section 112 ¶ 6 applies, I understand that NST proposes the following construction: the function is “forward a request for a connection to the resource manager,” and the structure is “circuit.”

107. I understand that Defendants contend that this term is subject to Section 112 ¶ 6. Defendants further contend the function is “receiving a request for a connection from the first module, forwarding the request to a resource manager, and receiving the availability of the target connection from the resource manager,” and the structure is indefinite.

108. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

109. I understand that NST and Defendants have stipulated “integrated circuit” means “interconnected circuitry on a chip.” Opening Br. at 6. In my opinion, this meaning is consistent with how a POSITA reading the Asserted Patents would understand this term, and it is consistent with authoritative extrinsic sources, for example, THE NEW IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONICS TERMS, (5th ed. 1993), which defines an “integrated circuit” as “[a] combination of interconnected circuit elements inseparably associated on or within a continuous substrate.” **Exhibit I**; *see also* **Exhibit G**. The ’449 Patent describes the resource manager as being comprised in an integrated circuit. Accordingly, the resource manager is interconnected circuitry of the integrated circuit, i.e., the resource manager is a circuit, as explained below.

110. Recall that a system-on-chip and a system-on-silicon are examples of integrated circuits in which most or all components of a system are integrated, including memories,

processors, high-speed I/O interfaces, and dedicated application-specific logic. *See, e.g., Exhibit A*, 29; *see also Exhibit B*, 380–381, 395, 487. This is consistent with the use of these terms in the '449 Patent, for example:

Systems on silicon show a continuous increase in complexity due to the ever increasing need for implementing new features and improvements of existing functions. This is enabled by the increasing density with which **components can be integrated on an integrated circuit**. At the same time the clock speed at which circuits are operated tends to increase too. The higher clock speed in combination with the increased density of components has reduced the area which can operate synchronously within the same clock domain. . . . A communication network forms an effective way to overcome these disadvantages.”

Dkt. 1, Exhibit 2, 1:15–35 (emphasis added); *see also Dkt. 1, Exhibit 1*, 1:16–36; **Dkt. 1, Exhibit 3**, 1:14–32; **Dkt. 1, Exhibit 4**, 1:14–34; **Dkt. 1, Exhibit 6**, 1:14–32.

The following embodiments relate to **systems on chip, i.e. a plurality of modules on the same chip** communicate with each other via some kind of interconnect.

Dkt. 1, Exhibit 2, 8:43–45 (emphasis added).

111. First, the specification of the '449 Patent states “FIG. 3 shows a system on chip [that] comprises a communication manager CM and a resource manager RM.” **Dkt. 1, Exhibit 2**, 9:66–10:3. Because a system-on-chip (SoC) is an integrated circuit, and an integrated circuit is interconnected circuitry on a chip, a POSITA would understand that the communication manager comprised in an SoC integrated circuit discloses that the communication manager is interconnected circuitry of the integrated circuit, i.e., the communication manager is a circuit.

112. Second, the specification of the '449 Patent states that “[a]ccording to an aspect of the invention, said **integrated circuit comprises at least one communication managing means CM for managing the communication between different modules, . . .**” **Dkt. 1, Exhibit 2**, 7:35–38 (emphasis added). In the '449 Patent, the communication manager CM is sometimes called the communication managing means CM. FIG. 3 is reproduced below.

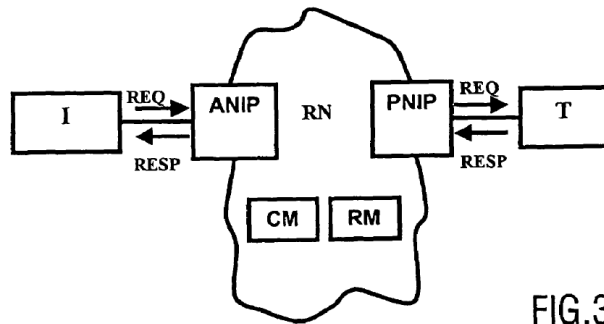


FIG.3

113. Because an integrated circuit is interconnected circuitry on a chip, a POSITA would understand that the communication manager comprised in an integrated circuit discloses that the communication manager is interconnected circuitry of the integrated circuit, i.e., the communication manager is a circuit.

114. Third, the specification of the '449 Patent states that "FIG. 3 shows a system on chip [wherein] **the communication manager CM and the resource manager RM are arranged in the router network RN, but they can also be arranged in one or some of the network interfaces NI.**" Dkt. 1, Exhibit 2, 9:66–10:6 (emphasis added). The '449 Patent states in several places that the network, or router network, and the network interface means are comprised in an integrated circuit, as indicated below.

An **integrated circuit comprising** a plurality of processing modules (M; I; S; T) and a **network (N; RN)** arranged for providing at least one connection between a first and at least one second module is provided.

Dkt. 1, Exhibit 2, Abstract (emphasis added).

The invention relates to an **integrated circuit having** a plurality of processing modules and a **network** arranged for providing connections between processing modules and a method for exchanging messages in such an integrated circuit.

Dkt. 1, Exhibit 2, 1:7–11(emphasis added).

Therefore, and **integrated circuit comprising** a plurality of processing modules M; I; S; T and a **network N; RN** arranged for providing at least one connection between a first and at least one second module is provided.

Dkt. 1, Exhibit 2, 7:15–18 (emphasis added).

According to still a further aspect of the invention, said **integrated circuit comprises at least one network interface means N1**, associated to each of said modules, for managing the communication between said modules and said network N.

Dkt. 1, Exhibit 2, 8:7–11 (emphasis added).

FIG. 2 shows a **system on chip** according to a second embodiment. **The system comprises** two modules, namely an initiator I and a target T, **a router network RN, and two network interfaces ANIP, PNIP** between the modules and the router network RN.

Dkt. 1, Exhibit 2, 9:17–21 (emphasis added).

115. Thus, a POSITA would understand that the communication manager comprised in either the communication or the interface means discloses that the communication manager is circuitry of the integrated circuit that comprises the network or the interface means, i.e., the communication manager is a circuit.

116. Fourth, the specification of the '449 Patent refers to the “communication manager” that is recited in claim 10 as either the “communication manager” or the “communication managing means” in the specification.

According [sic] to an aspect of the invention, said integrated circuit comprises at least one communication managing means CM for managing the communication between different modules; . . .

Dkt. 1, Exhibit 2, 7:35–38.

According to a further aspect of the invention, said first module M; I issues a request for a connection to at least one of said second modules to said communication managing means CM. Said communication managing means CM forwards the request for a connection with communication channels each having a specific set of connection properties to said resource managing means (RM). Said resource managing means RM determines whether the requested connection based on said communication channels with said specific connection properties is available, and responds the availability of the requested connection to said communication managing means CM.

Dkt. 1, Exhibit 2, 7:40–51.

According to a still further aspect of the invention, said communication managing means CM rejects establishing a connection based on the available connection properties when the available connection properties are not sufficient to perform the requested connection between said first and second module.

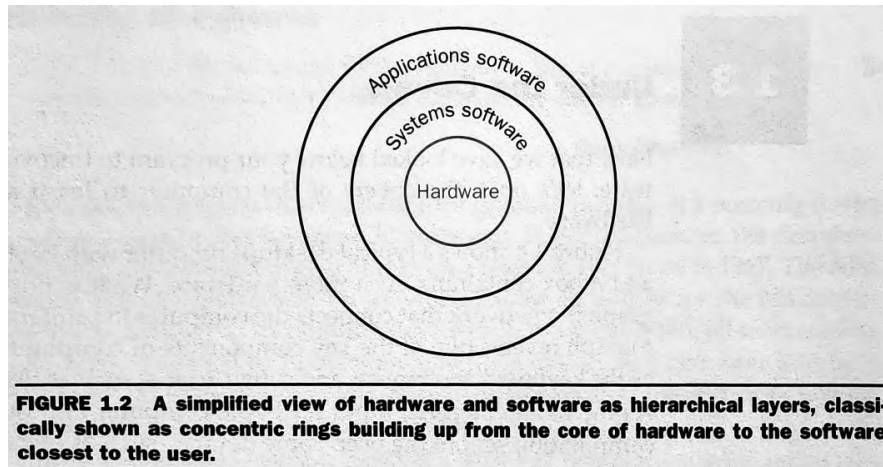
Dkt. 1, Exhibit 2, 7:56–61.

According to a further aspect of the invention, said communication managing means CM issues a request to reset the connection between said first and second module, when said modules have successfully performed their transactions, so that the network resources can be used again for other connections.

Dkt. 1, Exhibit 2, 8:1–6.

117. The specification of the '449 Patent states before the claims section that “[i]n the device claim enumerating several means, several of these **means can be embodied by one and the same item of hardware.**” **Dkt. 1, Exhibit 2**, 18:23–25 (emphasis added). A POSITA understands the term “hardware” to mean physical circuitry. For example, the DICTIONARY OF COMPUTER AND INTERNET TERMS (7th ed. 2000) defines hardware as “the physical elements of a computer system; the computer equipment as opposed to the programs or information stored in the machine.” (**Exhibit M**). This term is often used in contrast with the term “software,” which a POSITA understands as describing instructions for execution by computer hardware, e.g., by physical circuitry like a processor (sometimes called a central processing unit (CPU)). For example, the DICTIONARY OF COMPUTER AND INTERNET TERMS (7th ed. 2000) defines software as “programs that tell a computer what to do. The term contrasts with *hardware*, which refers to the actual physical machines that make up a computer system.” (emphasis in original) (**Exhibit M**). The figure below shows a simplified hierarchical view of the hardware-software interface, with hardware at the core and software on the periphery for execution by the core. DAVID PATTERSON

AND JOHN HENNESSEY, COMPUTER ORGANIZATION & DESIGN § 1, p. 9 (2nd ed. 1998) (**Exhibit N**).



118. Based on the above evidence, it is my opinion that a POSITA would understand the communication manager to be a circuit.

119. Turning now to the “manages communication between modules” part of NST’s proposed construction for this term, the ’449 Patent describes the communication manager (sometimes called the “communication managing means”) as being configured to manage communication between modules. *See, e.g., Dkt. 1, Exhibit 2*, 7:36–38 (“[A]t least one communication managing means CM for managing the communication between different modules, . . .”).

120. First, independent claim 10 of the ’449 Patent recites a “[m]ethod . . . comprising the steps of: . . . the first module issuing a request for a connection with the second module to a communication manager, . . . the communication manager forwarding the request to a resource manager; [and] the resource manager responding with the availability of the target connection to the communication manager, . . .” **Dkt. 1, Exhibit 2**, 19:21–20:2. Each of these steps are

examples of managing communications between modules. The specification describes these steps, for example:

The communication manager CM request a connection with a set of properties between two modules from the resource manager RM, after receiving the request REQ from the active network interface ports ANIP, i.e. the properties of a connection, e.g. throughput, flow control, are to be requested when asking for a connection setup. The resource manager RM allocates the necessary resources and enquires if such a connection based on these resources is possible. After enquiring of the available connection properties, the resource manager RM reserves the available connection i.e. the required resources, and responds to the communication manager CM which connection is available, i.e. which connection properties or the required resources thereof are available for the desired channels.”

Dkt. 1, Exhibit 2, 10:19–46 (emphasis added).

121. Thus, it is my opinion that the correct understanding that a POSITA would have of “communication manager,” as used in the Asserted Patents, is the meaning provided by NST of “circuit that manages communication between modules.”

122. I understand the Court may determine this term should be construed under 35 U.S.C. § 112 ¶ 6, means-plus-function. In this event, it is my opinion that NST’s proposed function and structure are correct and Defendants’ proposed functions and structure are not correct.

123. In my opinion, the function of the “communication manager” under 35 U.S.C. § 112 ¶ 6, with respect to claim 10, is to “forward a request for a connection to a resource manager,” and the corresponding structure is a “circuit.” A detailed explanation is below.

124. First, independent claim 10 of the ’449 Patent recites a “[m]ethod . . . comprising the steps of: . . . the first module issuing a request for a connection with the second module to a communication manager, . . . the communication manager forwarding the request to a resource manager; [and] the resource manager responding with the availability of the target connection to

the communication manager, . . .” **Dkt. 1, Exhibit 2**, 19:21–20:2. The specification describes these steps, for example:

The communication manager CM request a connection with a set of properties between two modules from the resource manager RM, after receiving the request REQ from the active network interface ports ANIP, i.e. the properties of a connection, e.g. throughput, flow control, are to be requested when asking for a connection setup. The resource manager RM allocates the necessary resources and enquires if such a connection based on these resources is possible. After enquiring of the available connection properties, **the resource manager RM reserves the available connection i.e. the required resources, and responds to the communication manager CM which connection is available**, i.e. which connection properties or the required resources thereof are available for the desired channels.”

Dkt. 1, Exhibit 2, 10:19–46 (emphasis added).

125. However, of those three steps recited in claim 10, only the step of “the communication manager forwarding the request to a resource manager” is an explicit step taken by the communication manager. The first and third steps describe steps explicitly taken by the first module and the resource manager, respectfully. Thus, in my opinion, the function of the “communication manager” under 35 U.S.C. § 112 ¶ 6, with respect to claim 10, is to “forward a request for a connection to a resource manager.”

126. As explained earlier in this section, a POSITA would recognize the structure of the communication manager to be a circuit *Supra* ¶¶ 109–118.

127. Thus, it is my opinion that if the Court determines this term should be construed under 35 U.S.C. § 112 ¶ 6, then the correct understanding that a POSITA would have of this term as used in the Asserted Patents is the meaning provided by NST.

E. “interconnect means”

128. I understand that NST contends this term means “multi-hop interconnection between modules separated by one or more network nodes.” If the Court holds that Section 112 ¶

6 applies, I understand NST proposes the following construction: the function is “coupling said plurality of processing modules (M, S),” and the structure is “circuit.”

129. I understand that Defendants contend this term is subject to Section 112 ¶ 6. I understand that Defendants further contend the function is “coupling said plurality of processing modules (M, S),” and the structure is “bus, switch, point-to-point wire, or network.”

130. I understand that NST and Defendants have stipulated “network” means “multi-hop interconnection between modules separated by one or more network nodes.” Opening Br. at 6. This is relevant to the construction of “interconnect means” because the ’052 Patent uses the terms “interconnect means (N)” and “network N” interchangeably, which is shown below.

131. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

132. At the time of the invention, on-chip networks were just emerging as an intersection of computer networks and microchip design. *See, e.g., Exhibit C*, § 1 (“We propose replacing design-specific global on-chip wiring with a general-purpose on-chip interconnection network.”).

133. Also, at the time of invention, computer networks and other off-chip networks were well-known and understood. For example, as explained in the specification of the ’052 Patent, “issues like out-of order transactions, higher latencies, and end-to-end flow control . . . have been already the subject of research in the field of local and wide area networks (computer networks) and as an interconnect for parallel machine interconnect networks.” **Dkt. 1, Exhibit 3**, 1:56–62; *see also* **Dkt. 1, Exhibit 1**, 1:59–65; **Dkt. 1, Exhibit 2**, 1:58–64; **Dkt. 1, Exhibit 4**, 1:57–63; **Dkt. 1, Exhibit 6**, 56–62. Engineers and/or researchers with backgrounds in computer networks tended to approach and describe on-chip networks from the perspective of computer

networks, e.g., LANs and WANs. Thus, “interconnect means” may have been an apt term for some of these engineers and/or researchers to describe an on-chip network, since they were already using the term “network” for off-chip networks. On the other hand, some engineers and/or researchers may have focused too heavily on the “interconnect” portion of “interconnect means,” and inadvertently narrowed its scope to direct interconnects, such as shared buses.

134. Also, at the time of invention, direct interconnections for enabling communication between modules (e.g., IP blocks or components) within a very large-scale integrated (VLSI) system, such as shared buses and switches, were well known and understood. For example, as explained in the '818 Patent, “[a]n outline [of] the differences of NoCs [(networks-on-chip)] and buses will be given below. We refer mainly to buses as direct interconnects, because currently they are the most used on-chip interconnect. Most of the bus characteristics also hold for other direct interconnects (e.g., switches).” **Dkt. 1, Exhibit 1**, 3:47–51; *see also* **Dkt. 1, Exhibit 2**, 3:58–62. Engineers and/or researchers with backgrounds in microchip design tended to approach and describe on-chip networks from the perspective of shared buses and switches, e.g., clusters of wires or interconnects. Thus, “interconnect means” may have been an apt term for these engineers and/or researchers to describe an on-chip network, since they were already using the term “interconnects” for on-chip wires. On the other hand, some engineers and/or researchers may have focused too heavily on the “interconnect” portion of “interconnect means,” and inadvertently narrowed its scope to direct interconnects, such as shared buses.

135. As a result of the different approaches and varying ways to describe an on-chip network in the fields of computer networks and microchip design, at the time of invention, “interconnect means,” as it is used in the Asserted Patents, lacked a strictly consistent plain and ordinary meaning. However, based on the intrinsic evidence, the interconnect means does not

describe only a direct interconnection, e.g., a shared bus; rather, it describes an indirect interconnection, e.g., a network, as explained below.

136. First, in the '052 Patent, the label “N” indicates a network portion in several figures, and the label “N” is associated with both the terms “network N” and “interface means (N)” in the specification and claims (recall claim 6 recites steps that describe “an interconnect means (N).”).

137. In the '052 Patent, “FIG. 1 shows a network on chip according to a first embodiment.” **Dkt. 1, Exhibit 3**, 5:6–7; *see also* 4:30–31. FIG. 1 is reproduced below, with annotation in yellow.

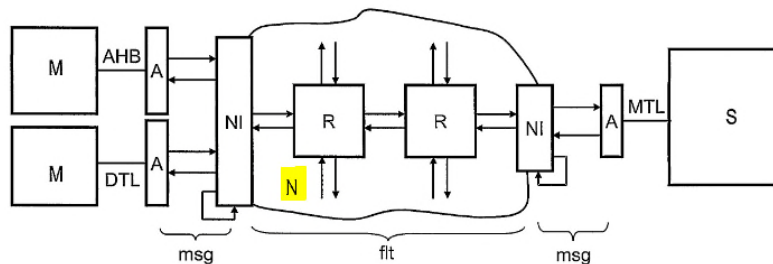


FIG.1

138. According to the description of FIG 1, the portion labeled “N” between the network interfaces corresponds to a network having a plurality of routers for transporting data packets:

The network N may be comprised of a plurality of interconnected network routers R. The routers R can be randomly connected amongst themselves (multiple links between routers are also possible) and to the network interfaces (i.e., there are no topology constraints). The routers R transport packets of data from one network interface NI to another. Such a packet consists of one or more flits, where a flit is the minimal transmission unit.

Dkt. 1, Exhibit 3, 5:24–31 (emphasis added).

139. In the '052 Patent, “FIG. 4 shows a basic representation of a block diagram of a network on chip according to a further embodiment.” **Dkt. 1, Exhibit 3**, 4:37–39; *see also* 8:7–8.

FIG. 4 is reproduced below, with annotation in yellow.

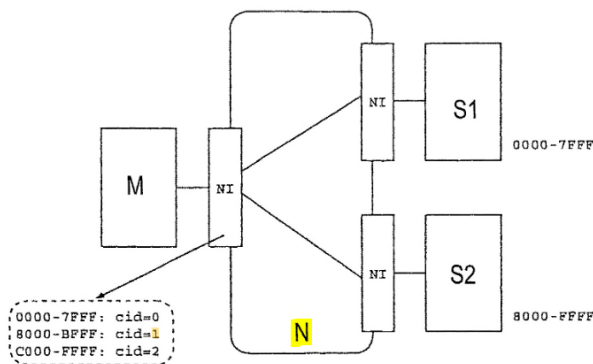


FIG.4

140. According to the description of FIG. 4, “[t]he network on chip comprises a master M and two slaves S1, S2 each being connected to a network via a network interface NI, respectively.” **Dkt. 1, Exhibit 3**, 8:9–12. Although FIG. 4 does not illustrate routers in the network N, this can be reasonably expected at least because “FIG. 4 shows a **basic block diagram of a network on chip for illustrating the operation of the mapping of IP block communication via address ranges to connections.**” **Dkt. 1, Exhibit 3**, 8:7–9 (emphasis added). In other words, FIG. 4 is provided for illustrating the mapping operation of the network interfaces, not for illustrating a topology of the network. Indeed, the description following FIG. 1, explicitly states “there are no topology constraints.” **Dkt. 1, Exhibit 3**, 5:27–28.

141. According to FIGS. 1 and 4 and the descriptions cited above, the network N interconnects modules (M to S in FIG. 1 and M to S1, S2 in FIG. 4). The specification ascribes the same function to the interconnect means, which several examples cited below. Thus, at least

for this reason, a POSITA would understand that the network N and the interconnect means (N) describe the same thing.

Furthermore, an interconnect means (N) is provided for coupling said plurality of processing modules (M, S) and for enabling a connection based communication having a set of connection properties.

Dkt. 1, Exhibit 3, Abstract.

The invention relates to an integrated circuit having a plurality of processing modules and an interconnect means for coupling said plurality of processing modules.

Dkt. 1, Exhibit 3, 1:7–8.

At least one network interface is associated to said at least one first of said processing modules for controlling the communication between said at least one first of said plurality of processing modules and said interconnect means.

Dkt. 1, Exhibit 3, 3:18–22.

Said plurality of processing modules are coupled by an interconnect means and enabling a connection based communication having a set of connection properties.

Dkt. 1, Exhibit 3, 3:51–54.

Furthermore, an interconnect means is provided for coupling said plurality of processing modules and for enabling a connection based communication having a set of connection properties.

Dkt. 1, Exhibit 3, 4:1–4.

142. There is additional evidence in the '052 Patent indicating that the network N and the interconnect means (N) describe the same thing. Specifically, the “interconnect means (N) is provided for coupling said plurality of processing modules (M, S) **and for enabling a connection based communication having a set of connection properties.**” **Dkt. 1, Exhibit 3, Abstract** (emphasis added); *see also* 3:15–18; 3:51–54; 4:1–4. As explained in the '052 Patent:

“At the transport layer of said network, the communication between the modules may be performed over connections. A connection is considered as a set of channels, each having a set of connection properties, between a first module and at

least one second module. . . . The connection properties may include ordering (data transport in order), flow control (a remote buffer is reserved for a connection, and a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data), throughput (a lower bound on throughput is guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data), transmission termination, transaction completion, data correctness, priority, or data delivery.”

Dkt. 1, Exhibit 3, 4:50–5:5.

“The connections may comprise the following services, or connection properties: 1) data integrity, 2) transaction ordering, 3) transaction completion, 4) connection flow control, and 5) connection throughput, latency, and jitter. A connection can request any combination of these properties (e. g. a throughput guarantee, flow control, but no transaction ordering).”

Dkt. 1, Exhibit 3, 6:13–19.

143. A POSITA would understand that a connection-based communication, which may include the connection properties listed above, is a known attribute of networks, and a POSITA would further understand that a connection-based communication, which may include the connection properties listed above, is not normally associated with direct interconnections, such as shared buses. Consequently, because the interconnection means described in the ’052 Patent enables a connection-based communication, a POSITA would understand the “interconnection means” to describe a network comprising indirect interconnections between modules, not a direct interconnection between modules. In other words, the POSITA would understand that the network N and the interconnect means (N) describe the same thing.

144. And as detailed earlier, the network N of FIG. 1 explicitly includes interconnected routers R for transporting data packets, consistent with “the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes.” **Dkt. 1, Exhibit 3, 2:33–36.** Thus, a network N is a “multi-hop interconnection between modules separated by one or more network nodes.” Consequently, because “interconnect means”

and “network” describe the same thing, then “interconnect means” is a “multi-hop interconnection between modules separated by one or more network nodes.”

145. Thus, it is my opinion that the correct understanding that a POSITA would have of “interconnect means,” as used in the Asserted Patents, is the meaning provided by NST of a “multi-hop interconnection between modules separated by one or more network nodes.”

F. “arranging . . . the first and the second information comprising said issued message as a single address”

146. I understand that NST contends this term means “arranging ... the first and second information comprised in said issued message as a single address.”

147. I understand that Defendants contend this term is indefinite.

148. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

149. Asserted claim 4 of the ’9893 Patent recites that “a **message** issued by an addressing module M **comprises: first information . . . and second information.**” Dkt. 1, Exhibit 4, 12:41–51 (emphasis added). A POSITA understands this to mean, quite plainly, that the message includes the first information and the second information. The full passage from claim 4 is reproduced below.

A method for exchanging messages in an integrated circuit comprising a plurality of modules, the messages between the plurality of modules being exchanged via a network wherein **a message issued by an addressing module M comprises: first information** indicative of a location of an addressed message receiving module S within the network and is comprised of (1) a connection identifier identifying two or more message receiving modules S and (2) an identifier of a passive network interface means associated with the addressed message receiving module S, **and second information** indicative of a particular location within the addressed message receiving module S, such as a memory, or a register address, the method including the steps of: . . .”

Dkt. 1, Exhibit 4, 12:39–54 (emphasis added).

150. Indeed, the specification of the '9893 patent describes the same arrangement of first information and second information comprised in a message from a module, as shown in the following passages.

[A] **message issued by a master module comprises first information** indicative for a location of a slave (addressed) module within the network, **and second information** indicative for a location within the addressed module.

Dkt. 1, Exhibit 4, Abstract (emphasis added).

Messages from a module are redirected by the nodes to one or more other nodes. To that end **the message comprises first information** indicative for the location of the addressed module(s) within the network. **The message may further include second information** indicative for a particular location within the module, such as a memory, or a register address.”

Dkt. 1, Exhibit 4, 3:16–22 (emphasis added).

[A] **message issued by a first module M comprises first information** indicative for a location of an addressed module within the network, **and second information** indicative for a location within the addressed module S.

Dkt. 1, Exhibit 4, 3:46–49 (emphasis added).

[A] **message issued by a module M comprises first information** indicative for a location of an addressed module S within the network, **and second information** indicative for a location within the addressed module S.

Dkt. 1, Exhibit 4, 4:19–23 (emphasis added).

151. Given the extensive evidence in the specification that the first information and the second information is comprised in the message, a POSITA would readily recognize the typographical error in which an incorrect verb form, “comprising,” is used instead of “comprised in” in the claim term at issue, “arranging . . . the first and second information **comprising** said issued message as a single address” (emphasis added). Further, a POSITA would recognize the incongruity of the first information and the second information comprising the message. Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in

the Asserted Patents, is the meaning provided by NST, “arranging . . . the first and second information **comprised in** said issued message as a single address” (emphasis added).

152. However, Defendants’ Joint Opening Claim Construction Brief contends this claim term is indefinite because a POSITA would not understand the word “arranging” as it is used in the ’9893 Patent.

A POSITA would not know what the patent means by “arranging” two pieces of information into “a single address.” Hassoun Decl. at ¶87. A POSITA would not know what type of data manipulation (if any) was required for “arranging” two pieces of information into a single address. *Id.* They also would not know what the boundaries of “single address” were.

Opening Br. at 24-25.

153. It is my opinion that this contention is inconsistent with the definition of the relevant POSITA provided in Defendants’ Declaration of Dr. Marwan Hassoun, which is reproduced below.

[T]he relevant POSITA for the Accused Patents would typically have had at least either a Master’s degree in Electrical Engineering, or a related field, as well as at least three years of work experience in the field of SoC design, or a Bachelor’s degree in Electrical Engineering, or related field, as well as at least five years of work experience in the field of SoC design. This POSITA would have had an understanding of SoC interconnects. They would also have a working understanding of the concepts of large-scale networks.

Dkt 77-1 at 5-6.

154. A person who has the stated education level and work experience of Defendants’ POSITA would readily understand how to arrange two units of information as a single address. The word “arrange” means to combine, to order, to group, to assemble, to adapt, and so on. *See, e.g.,* <https://www.thesaurus.com/browse/arrange>. Thus, arranging the first and second information as a single address that is consistent with the addressing characteristics of a particular on-chip network may include, for example, one or more operations that are well-

known to a person who has the stated education level and work experience of Defendants' POSITA, such as concatenation, addition, subtraction, integer multiplication, XOR, indexing a look-up table, and so on. For example, the single address may simply require concatenating the first and second information, or it may require adding the first and second information modulo $2^{(\text{number of bits in an address field for the single address})}$.

155. A person who has the stated education level and work experience of Defendants' POSITA would also readily understand "what the boundaries of 'single address' were." See Opening Br. at 5-6. For example, a quantity of bits in an address field of a message to be sent via a particular on-chip network is a conspicuous bound on a length of the single address. A person who has the stated education level and work experience of Defendants' POSITA would readily understand how to arrange the first and second information as a single address that would fit within the address field of the message, for example, via well known operations such as modulo, truncation, hash, and so on.

156. Defendants' Declaration of Dr. Marwan Hassoun alleges that uses of the word "arrange" in the specification of the '9893 Patent in contexts other than "arranging . . . the first and the second information comprising said issued message as a single address" increase the alleged uncertainty in the meaning of the claim term. Dkt. 77-1 at 39–40. A POSITA reading the Asserted Patents, as discussed above, would not find term "arranging" to add uncertainty.

157. Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

G. “each data package comprising N data elements”

158. I understand that NST incorporates its definition for the term “data package,” contends that “data elements” are groups of data, and contends that the remaining language should be afforded its plain and ordinary meaning.

159. I understand that Defendants contend this term means “every data package communicated by the network stations has a fixed size of N data elements.”

160. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

161. The specification of the ’2893 Patent describes a data communication network of an integrated circuit that is configured to communicate data packages, where each data package comprises N data elements.

According to an aspect of the invention, there is provided an integrated circuit a plurality of functional blocks and a **data communication network** comprising a plurality of network stations being interconnected via a plurality of communication channels **for communicating data packages** between the functional blocks, **each data package comprising N data elements including a data element comprising routing information for the network stations**, N being an integer of at least two,
...

Dkt. 1, Exhibit 5, 1:65–2:6 (emphasis added).

162. FIGS. 3 and 5 of the ’2893 Patent, reproduced below, show examples of data packages comprising 3 data elements, where data elements of a given data package are transferred by the data communication network in different clock cycles.

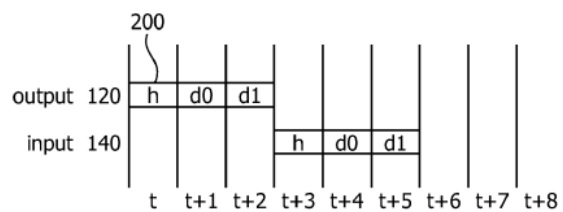


FIG. 2

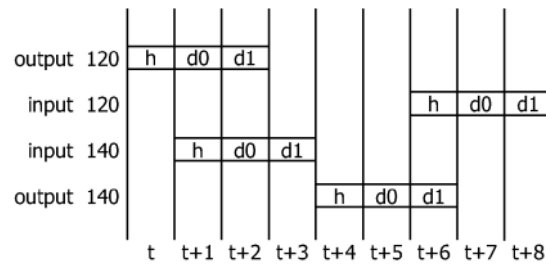


FIG. 4

163. The data packages contain data, i.e., information, for example, routing information. *See, e.g., Dkt. 1, Exhibit 5*, 2:22–26 (“The routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package, e.g. the first data element (i.e. a header), although other data elements may (also) contain such information.” (parentheses in original)). Put simply, a data element is a group of data. This is consistent with NST’s contention that “data elements” are groups of data.

164. The full claim term at issue is “each data package comprising N data elements.” A POSITA would readily recognize that data elements are groups of data as explained above, and a POSITA would understand the remaining language of this term according to its plain and ordinary meaning as used in the specification and the claims. In particular, the specification of the ’2893 Patent states “[t]he word ‘comprising’ does not exclude the presence of elements or steps other than those listed in a claim.” *Dkt. 1, Exhibit 5*, 10:16–18. Thus, the term “each data package comprising N data elements” means that each data package comprises N, or more than N, data elements, i.e., at least N data elements. I understand that the Applicant could have used a closed-ended phrase, such as “consisting of,” to signify that each data package has exactly N data elements. Indeed, in the specification of the ’2893 Patent, the Applicant chose to use this closed-ended phrase when referring to the data packages depicted in FIG. 4. *Dkt. 1, Exhibit 5*, 7:58–61 (“This is explained in more detail in FIG. 4, where a data package **consisting of data**

elements h, d0 and d1 is sent from data router 120 to data router 140 and back again in the network of IC 10 as shown in FIG. 3.” (emphasis added)).

165. Defendants contend that every data package must have exactly N data elements, which Defendants state as follows.

Claim 10 also requires that each of the data packages have N data elements, where ‘N’ is ‘an integer.’ . . . As such, ‘N’ would be superfluous were it not a fixed value for all the data packages because if the data packages have variable sizes (i.e., some packages sized ‘N’ data elements, some sized ‘N+1’ or ‘N+2’ data elements), the limitation ‘each data package comprising N data elements’ would effectively be read out of the claim. Hassoun Decl. at ¶95.

Opening Br. At 26. It is my opinion that this reading of the ’2893 Patent is overly narrow.

166. The disclosed invention is based on maintaining a correct periodicity between network stations, where data packages having N data elements take N clock cycles to transfer between the network stations, and the network stations expect routing information every N cycles.

The invention is based on the realization that the correct operation of the network relies on the maintenance of the correct periodicity between the network stations. Because the data packages have a fixed size of N data elements, the communication of a complete package between two network stations takes N clock cycles, or N handshake driven data transfers in case of an asynchronous implementation of the network. . . . Since a network station expects routing information to arrive periodically (i.e. after every N cycles), the introduction of a delay on the first communication channel (which typically is the slowest channel of the network) matching such a period, i.e. by delaying the whole data package rather than a single data element, the delayed data package is received by the receiving network station during the appropriate period, e.g. clock cycle.

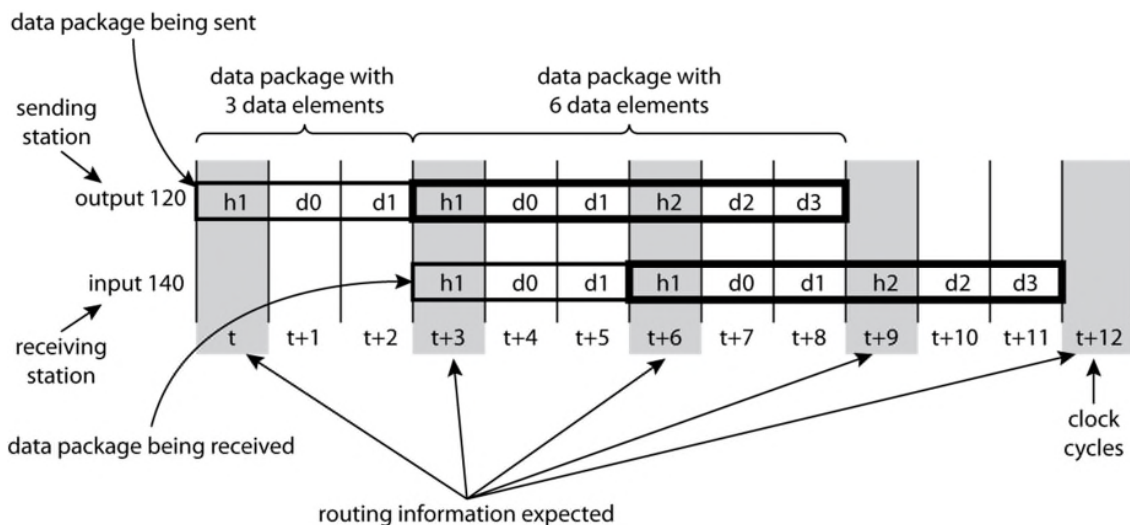
Dkt. 1, Exhibit 5, 2:15–22.

167. The specification of the ’2893 Patent explains that “[t]he routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package, e.g. the first data element (i.e. a header), **although other data elements may (also) contain such information.**” **Dkt. 1, Exhibit 5, 2:22–26** (emphasis added)

(parentheses in original). In other words, routing information contained in a data package may be included in any data element that is transferred in any cycle, and moreover, the routing information contained in a data package may be included in multiple data elements. Indeed, the specification is unambiguous on this point, explicitly stating that “[a]t least one of the N data elements in a package, e.g. the first data element, comprises routing instructions for the destination network station.” **Dkt. 1, Exhibit 5**, 4:53–56 (emphasis added). Thus, a network station must be able to evaluate routing information (e.g., routing instructions) in any cycle.

168. According to an implementation of the ’2893 Patent, “a network station expects routing information to arrive periodically (i.e. after every N cycles).” **Dkt. 1, Exhibit 5**, 2:26–28; *see also Dkt. 1, Exhibit 5*, 6:40–43 (“The data routers 110, 120, 130, 140 are all configured to periodically evaluate the content of a received data package, that is after every N clock cycles for a data package having a size N data elements.”). However, this does not mean that every data package must contain exactly N data elements as Defendants contend. For example, a data package having 2N data elements, where the first data element and the (N+1)th data element each contain routing information, easily satisfies the routing-information periodicity expectation of the network stations of this implementation. In general, any data package having $n*N$ data elements, where $n > 1$, that includes routing information in every $(1+i*N)^{th}$ data element, where $i > 0$, satisfies the routing-information periodicity expectation of the network stations of this implementation.

169. A simple example showing a transfer of two data packages is depicted below, where a first data package that is transferred has 3 data elements and a second data package that is transferred has 6 data elements. Routing information is provided in data elements labeled h1 and h2; therefore, the network stations receive routing information during the expected cycles.



170. As demonstrated above, different data packages can have different quantities of data elements while satisfying the routing-information periodicity expectation of the network stations of this implementation. Put simply, not every data package must contain exactly N data elements, and therefore, “each data package comprising N data elements” does not mean “every data package comprising N data elements.”

171. Given the totality of evidence, it is my opinion that the correct understanding that a POSITA would have of “each data package comprising N data elements,” as used in the Asserted Patents, is the meaning provided by NST, where “data elements” are groups of data and the remaining language should be afforded its plain and ordinary meaning. Specifically, the word “comprising” means “at least” and the phrase “each data package” means “a given data package,” not “every data package.”

H. “data package”

172. I understand that NST contends this term means “fixed-size arrangement of data.”

173. I understand that Defendants refer to their proposed construction for “each data package comprising N data elements.”

174. In my opinion, NST's proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

175. Asserted claims 10 of the '2893 Patent describes a data package as something capable of being communicated via a communication channel and which comprises an integer $N \geq 2$ of data elements:

a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels **for communicating data packages** between the functional blocks, **each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, . . .**

Dkt. 1, Exhibit 5, 10:30–36; 12:23–29 (emphasis added).

176. First, that the data package can be communicated between functional blocks indicates the data package comprises data rather than, for example, circuit elements. The specification of the '2893 Patent states the data package can be sent, received, and stored, confirming that the data package comprises data. **Dkt. 1, Exhibit 5**, 4:62–63 (“the data routers can send a stored data package to its next destination”); **Dkt. 1, Exhibit 5**, 6:54–55 (“data router 120 starts sending the data package upon its complete receipt”). Thus, a POSITA would understand that the data package comprises data.

177. Next, that the data package comprises a plurality (an integer $N \geq 2$) of data elements indicates the data of the data package is arranged in data elements. The specification and figures of the '2893 Patent depict such an arrangement. **Dkt. 1, Exhibit 5**, 7:58–61 (“This [phase shifted routing] is explained in more detail in FIG. 4, where a data package consisting of data elements h, d0 and d1 is sent from data router 120 to data router 140 and back again in the network of IC 10 as shown in FIG. 3.” (emphasis added)). FIG. 3 is reproduced below, depicting several data packages each including three data elements.

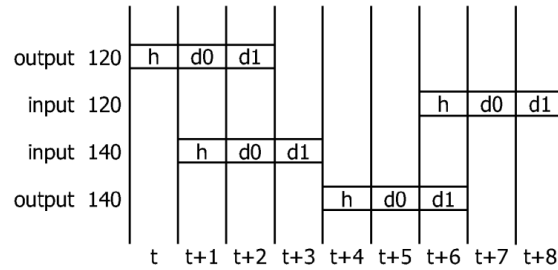


FIG. 4

178. The specification of the '2893 Patent explains that data elements contain data, i.e., information, such as “routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package, e.g. the first data element (i.e. a header), although other data elements may (also) contain such information.” **Dkt. 1, Exhibit 5**, 2:22–26. Thus, a POSITA would understand that the data package is an arrangement of data elements, and the data elements contain data, meaning the data package is an arrangement of data.

179. Finally, asserted claim 10 of the '2893 Patent recites “each data package comprising N data elements . . . N being an integer of at least two, . . .” **Dkt. 1, Exhibit 5**, 10:33–36; 12:27–29. Support for this can be found in the specification in numerous locations. *See, e.g.*, **Dkt. 1, Exhibit 5** (“Each data package includes N data elements . . . , N being an integer of at least two.”); **Dkt. 1, Exhibit 5**, 1:3–6 (“[E]ach data package comprising N data elements . . . , N being an integer of at least two, . . .”); **Dkt. 1, Exhibit 5**, 2:17–18 (“[T]he data packages have a fixed size of N data elements, . . .”). The specification of the '2893 Patent states that N corresponds to the size of the data package. **Dkt. 1, Exhibit 5**, 57–58 (“[W]ith N corresponding to the size of a data package, . . .”). Thus, a POSITA would understand that N is fixed for each data package, and each data package has a fixed size.

180. Based on the above discussion and evidence, it is my opinion that a POSITA would understand that: (1) a data package comprises data; (2) the data comprised in a data package is arranged in data elements; and (3) a data package has a fixed size. In other words, a data package is a “fixed-size arrangement of data.” Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

I. “data storage elements”

181. I understand that NST contends this term means “array of one or more elements that store data.”

182. I understand that Defendants contend this term means “each being a structure that stores one data element.”

183. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

184. Asserted claim 10 of the ’2893 Patent claims “[a] method of designing an integrated circuit comprising . . . a data communication network . . . ; the method comprising the acts of: . . . inserting M*N data storage elements into the data communication network, . . .” **Dkt. 1, Exhibit 5**, 12:22–39. I understand that NST and Defendants have stipulated that an integrated circuit is “interconnected circuitry on a chip.” Because the data communication network recited in claim 10 is comprised in the integrated circuit, the data communication network is circuitry of the integrated circuit. And because the data storage elements are comprised in the data communication network (i.e., circuitry of the integrated circuit), the data storage elements are also circuitry of the integrated circuit. Accordingly, a data storage element is a circuit.

185. The specification of the '2893 Patent describes a data storage element as being configured to store data. **Dkt. 1, Exhibit 5**, 8:1–3 (“At T=t, data element h is received by data storage element 160 in the first subchannel 152, which stores the data element h . . .”). Further, the specification of the '2893 Patent explains that a data storage element may be a single latch, and a plurality of data storage elements may be a pipeline of latches or buffers or flip-flops or as asynchronous FIFO buffers. **Dkt. 1, Exhibit 5**, 1:42 (“[A] data storage element such as a latch . . .”); **Dkt. 1, Exhibit 5**, 6:24–27 (“The data storage elements 160 may be a pipeline or a buffer of latches or flipflops, and may be implemented using synchronous or asynchronous storage elements.”); **Dkt. 1, Exhibit 5**, 8:54–55 (“[I]mplementing the M*N data storage elements 160 as asynchronous FIFO buffers.”). A POSITA understands the terms “pipeline” and “buffer” connote a sequence, series, or array, where in this situation, the pipeline or buffer of latches or flip-flops is a sequence, series, or array of memory circuit elements such as latches or flip-flops. This is depicted at least in FIGS. 1, 3, and 5 of the '2893 Patent, reproduced below with the data storage elements annotated in yellow.

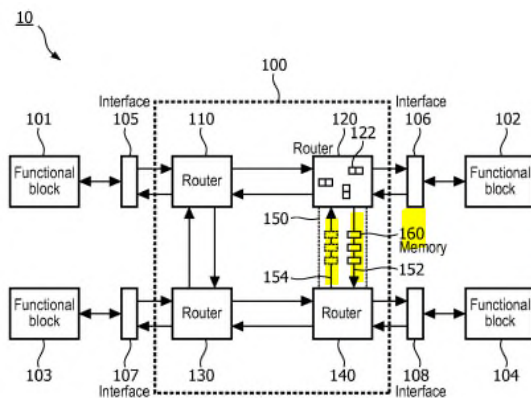


FIG. 1

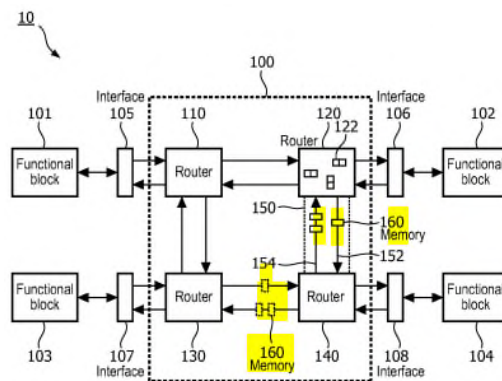
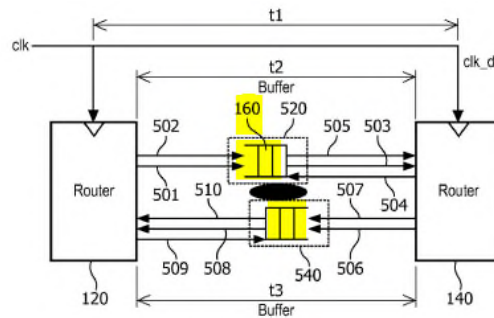


FIG. 3



186. Based on the above discussion and evidence, it is my opinion that a POSITA would understand that: (1) a data storage element is a circuit; (2) a data storage element stores data; and (3) data storage elements can be arranged in a sequence, series, or array. Accordingly, the plural, “data storage elements,” is “an array of one or more elements that store data.” Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents is the meaning provided by NST.

187. I understand that Defendants contend “data storage elements” means “each being a structure that stores one data element.” While this may be true in some implementations of the claimed invention, a POSITA would recognize contrary implementations, as explained below.

188. Asserted claim 10 of the ’2893 Patent recites “inserting $M \times N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel.” **Dkt. 1, Exhibit 5**, 12:38–41.

Defendants’ Joint Claim Construction Brief contends the following:

This corresponds to the “ N data elements” in each data package recited earlier in the claim and creates a mathematical relationship between the number of data elements (N), the number of data storage elements ($M \times N$), and the number of cycles of delay caused by the data storage elements ($M \times N$). Hassoun Decl. at ¶106. **If a data storage element stores more than one data element, this mathematical relationship would be lost.**

Opening Br. at 31 (emphasis added).

189. The quoted passages of the asserted claims do indeed each establish a mathematical relationship, but it is explicitly that the aggregate number of data storage elements ($M*N$) equals the aggregate number of cycles of delay ($M*N$) that are introduced. To be more rigorous, (1) the quantity of data storage elements equals $M*N$; (2) the quantity of cycles of delay equals $M*N$; and (3) the quantity of data storage elements equals the quantity of cycles of delay.⁴ These relationships can be readily satisfied when some of the data storage elements store more data than is contained in a single data element while other data storage elements store less data than is contained in a single data element, as long as the aggregate $M*N$ data storage elements introduce an aggregate delay of $M*N$ cycles. For example, let there be $M*N=20$ data storage elements numbered 1-20, where data storage elements 1-5 cause a delay of 4 cycles, data storage elements 6-10 cause a delay of 6 cycles, and data storage elements 11-20 cause a delay of 10 cycles, such that the aggregate number of cycles of delay, 4 cycles + 6 cycles + 10 cycles = 20 cycles (i.e., $M*N=20$ cycles of delay). This is just one example of many that satisfy asserted claim 10.

190. In a discussion concerning clock skew, the specification of the '2893 Patent states "[i]n such a scenario, the FIFO buffer 509 **must** be capable of storing more than $M*N$ data elements to avoid the loss of data stored in the FIFO buffer 509. This **can** be realized by adding one or more data storage elements to the $M*N$ data storage elements as overwrite protection." **Dkt. 1, Exhibit 5**, 9:46–51 (emphasis added). Adding one or more data storage elements is one way of avoiding the loss of data, as indicated by a sufficient condition, "can," instead of a necessary condition, like "must." Another way of avoiding the loss of data is, for example, for

⁴ Defendants' Joint Opening Claim Construction Brief and Defendants' Declaration of Dr. Marwan Hassoun mention an existence of "a mathematical relationship between the number of data elements (N), the number of data storage elements ($M*N$), and the number of cycles of delay caused by the data storage elements ($M*N$)," but neither document appears to explicitly divulge the alleged mathematical relationship.

one or more of the M*N data storage elements to be capable of storing more data than is contained in a single data element.

191. Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

J. “optimal amount of data”

192. I understand that NST contends this term should be afforded its plain and ordinary meaning.

193. I understand that Defendants contend this term is indefinite.

194. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

195. The ’800 Patent teaches an invention whose object is improving—indeed, optimizing—interconnect utilization in a network, where the improvement is achieved by buffering data until conditions for an optimal transfer are satisfied, as detailed in the following passages of the ’800 Patent.

It is therefore an object of the invention to provide an integrated circuit, a method for buffering as well as a data processing system with **an improved interconnect utilization.**

Dkt. 1, Exhibit 6, 3:35–37 (emphasis added).

According to a preferred aspect of the invention at least one of said first and second wrapper means comprise **a determination unit BLDU for determining the optimal first or second amount of data to be buffered in said first or second wrapper means before said data is transferred** according to the communication properties of said communication between said first and second processing module. Accordingly, the packet size of the data transferred over the interconnect can be adapted according to the properties of the actual communication **and thereby the utilization of the interconnect can be improved.**

Dkt. 1, Exhibit 6, 4:18–28 (emphasis added).

The invention is based on the idea to **buffer data until the buffered data is sufficiently large to be transferred optimally over an interconnect means in a packet**. The larger a packet is, the smaller is the amount of packet headers and therefore the overhead is reduced and **the interconnect is utilized more efficiently**. **The data is only transferred when sufficient data for an optimal packet size has been buffered even when data can be sent earlier**. The data is only transferred from the buffer when the conditions for an optimal transfer are satisfied.

Dkt. 1, Exhibit 6, 4:49–57 (emphasis added).

As in the first embodiment, the **wrapper means WM1, WM2 serve to buffer data to be sent over the network N until the conditions for an optimal transfer are satisfied**.

Dkt. 1, Exhibit 6, 6:15–17 (emphasis added).

The first and second wrapper means WM1, WM2 are **adapted to immediately transfer the buffered data when the first or second unbuffer-flag is set in the first or second unbuffer-flag unit UBF1, UBF2, respectively**. By providing this possibility to flush the buffered data a deadlock caused by data being buffered can be prevented. **In such case, all data being buffered are transferred as fast as possible without waiting for a packet size to suit the optimal burst length for the network N**.

Dkt. 1, Exhibit 6, 6:22–30 (emphasis added).

The flushing of the buffered data may also be achieved by a first or second unbuffer signal received by the first or second wrapper means WM1, WM2. Therefore, **if the first or second wrapper means WM1, WM2 receives an unbuffer signal, the data currently buffered are transferred as fast as possible, i.e. without waiting for the optimal burst length to be acquired**.

Dkt. 1, Exhibit 6, 6:31–36 (emphasis added).

The **data is buffered until the buffered data reach an optimal packet size such that the buffered data can be transferred over the network**. If the amount of buffered data has not yet reached the optimal packet size, none of the data is transferred over the network N even if transferring a smaller packet size is possible.

Dkt. 1, Exhibit 6, 7:23–28 (emphasis added).

The requests and responses are **aggregated in bursts with a length optimal for the particular interconnect**. As in the case of a request like a write, **the buffering can be prevented with an unbuffered flag to the response part of the**

transaction. Hence, all responses or requests pending and including the current one are transferred as fast as possible without being buffered to form an optimal burst length for the interconnect.

Dkt. 1, Exhibit 6, 7:44–51 (emphasis added).

196. Several things are clear from the above excerpts: (1) buffering of data improves and/or optimizes interconnect utilization (**Dkt. 1, Exhibit 6**, 3:35–37, 4:49–57, 6:15–17, 7:23–28, 7:44–51); (2) the optimal amount of data to be buffered can be based on communication properties of a communication (**Dkt. 1, Exhibit 6**, 4:18–28); and (3) the optimal amount of data to be buffered can be specific to a particular interconnect (**Dkt. 1, Exhibit 6**, 7:44–51). In other words, an optimal amount of data to be buffered may not be fixed or constant; rather, it may be according to communication properties and/or interconnect characteristics, i.e., based on certain conditions of a connection. This is typical for engineering optimization, for example, optimizing power consumption of a SoC, optimizing throughput of a CPU, optimizing manufacturing yield of an integrated circuit, and so on. A solution for each of these optimizations depends on properties and characteristics of the system, and the solution varies as the properties and characteristic vary. For example, relevant properties and characteristics for the above example optimizations may include:

- Power consumption of an SoC: supply voltage (e.g., 1.2V, 1.8V, etc.); semiconductor technology node (e.g., 90 nm, 20 nm, etc.); cooling method (e.g., passive heat sink, water cooled, etc.); data processed by the SoC (e.g., sparse matrices; real-time video, etc.); number representations (e.g., integer, floating point, etc.); and so on.
- Throughput of a CPU: instruction set architecture (e.g., reduced instruction set architecture (RISC), complex instruction set architecture (CISC), very long instruction word (VLIW), etc.); instruction length (e.g., 32-bit, 64-bit, etc.); applications executing

by the CPU (e.g., mathematical computations, 3D graphics, etc.); clock frequency (e.g., 500 MHz, 2 GHz, etc.); cache size (e.g., 1 megabyte, 100 megabytes, etc.); and so on.

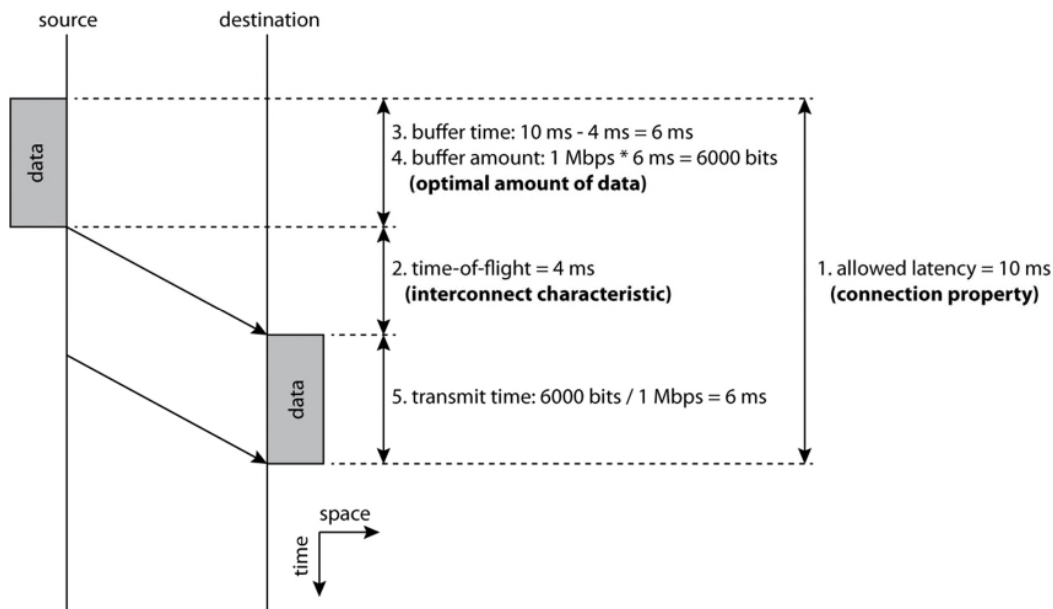
- Manufacturing yield of an integrated circuit: semiconductor technology node (e.g., 90 nm, 20 nm, etc.); types of circuits (e.g., analog, digital, mixed signal, etc.); die size (e.g., 2x2 mm, 20x20 mm, etc.); number of metal interconnect layers (e.g., 7 layers, 13 layers, etc.); types of transistors (e.g., MOSFETs, FinFETs, etc.); and so on.

197. To continue this comparison, consider the throughput of a CPU, where throughput may be, for example, the number of integer operations executed per second. An optimal throughput, e.g., a highest throughput of the CPU, depends on the considered properties and characteristics of the CPU, which may include instruction set architecture, instruction length, applications executed by the CPU, clock frequency, and cache size. This is analogous to the optimal interconnect utilization disclosed in the '800 Patent, e.g., a highest utilization of the interconnects, and depends on the considered properties and characteristics of the interconnects, which may include "ordering (data transport in order), flow control (a remote buffer is reserved for a connection, and a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data), throughput (a lower bound on throughput is guaranteed), latency (upper bound for latency is guaranteed), the lossiness (dropping of data), transmission termination, transaction completion, data correctness, priority, or data delivery."

Dkt. 1, Exhibit 6, 5:28–35 (listing connection properties). And as explained in the specification of the '800 Patent, an optimal amount of data to be buffered is an amount that optimizes interconnect utilization according to the connection properties. In the above CPU analogy, an optimal amount of data to be cached is an amount that optimizes CPU throughput according to

the properties and characteristics of the CPU. A POSITA therefore understands the optimal amount of data by its plain and ordinary meaning.

198. Given the connection properties of a connection, a POSITA would understand how to determine an optimal amount of data to be buffered with the objective of optimizing interconnect utilization. For example, if a 1 Mbps connection with a time-of-flight delay of 4 ms has a connection property that the maximum allowable latency is 10 ms, then an optimal amount of data to buffer (ignoring header data) would be the amount of data that could be transferred in $10 - 4 = 6$ ms, i.e., $(1 \text{ Mbps}) * (6 \text{ ms}) = 6000$ bits. A space-time diagram for this example is shown below.



199. The above simplistic example could be expanded to include, for example, a throughput connection property, where transmission time slots could be taken into account; a lossiness connection property, where dropping of data could be taken into account; a flow control connection property, where remote buffer space could be taken into account; data correctness, where error detection and/or correction codes could be taken into account, and so

on. A POSITA reading claim 12 of the '800 Patent, in light of the specification, would understand these connection properties and the characteristics of the interconnects, and how to determine an optimal amount of data to be buffered according to these properties and characteristics, i.e., an amount that is optimal under the conditions. This is the plain and ordinary meaning.

200. Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

K. “optimal moment for sending the data in said first wrapper or said second wrapper”

201. I understand that NST incorporates its definition for the term “wrapper,” and contends the remaining language should be afforded its plain and ordinary meaning.

202. I understand that Defendants contend this term is indefinite.

203. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

204. Claim 12 of the '800 Patent recites that a “determination unit is further configured to **determine an optimal moment for sending the data** in said first wrapper or said second wrapper **according to communication properties** of the communication between the master and the slave, . . .” **Dkt. 1, Exhibit 6** (emphasis added). Although the exact term “optimal moment” is not used in the specification, the specification discloses the meaning of an optimal moment in terms of a transmission moment. “Besides the optimal burst length determination, also **the transmission moment** may be determined in a similar way by the first and second determination means BLDU1, BLDU2.” **Dkt. 1, Exhibit 6**, 7:4–6 (emphasis added). A POSITA understands that transmission refers to “the data to be transmitted.” See **Dkt. 1, Exhibit 6**, 3:14, Accordingly, the transmission moment is the moment to transmit the data. Several examples of

determining the transmission moment based on communication properties are provided in the specification, which are underlined in the below passage.

Besides the optimal burst length determination, also **the transmission moment may be determined in a similar way** by the first and second determination means BLDU1, BLDU2. **For a guaranteed throughput GT connection, data should wait for one of the slots reserved for its connection.** Using a “flush”-like signal/flag may force the sending of the data in advance. Alternatively, **for a best effort BE connection, a round robin arbitration across connections in the NI can be used.** A “flush”-like signal may force a temporarily higher priority for a connection.

Dkt. 1, Exhibit 6, 7:4–14 (emphasis added).

205. Throughput is a communication property that includes guaranteed throughput (GT), which provides a lower bound on throughput, and best effort (BE), which does not provide a lower bound on throughput. *See, e.g., Dkt. 1, Exhibit 6*, 5:31–32 (“[T]hroughput (a lower bound on throughput is guaranteed), . . .”); *see also Dkt. 1, Exhibit 2*, 11:48–50 (“[B]est effort (i.e. no throughput guarantees) . . .”). Indeed, throughput is one of the communication properties available for determining an optimal moment for sending the data in Claim 12, which is emphasized in the below excerpt.

[W]herein at least one of the first determination unit and the second determination unit is further configured to **determine an optimal moment for sending the data in said first wrapper or said second wrapper according to communication properties** of the communication between the master and the slave, wherein the communication properties include ordering of data transport, flow control including when a remote buffer is reserved for a connection, then a data producer will be allowed to send data only when it is guaranteed that space is available for the produced data at the remote buffer, **throughput where a lower bound on throughput is guaranteed**, latency where an upper bound for latency is guaranteed, lossiness including dropping of data, transmission termination, transaction completion, data correctness, priority, and data delivery.

Dkt. 1, Exhibit 6, 12:16–32 (claim 12) (emphasis added).

206. A POSITA would understand an “optimal moment for sending the data in said first wrapper or said second wrapper” in terms of engineering optimization a same way that a

POSITA would understand an “optimal amount of data” to be buffered—as a moment for sending the data in the first wrapper or the second wrapper with the objective of optimizing interconnect utilization, where the optimal moment is determined according to the connection properties. Some examples concerning these connection properties are provided in the section on the “optimal amount of data,” such as a latency connection property, where time-of-flight could be taken into account; a throughput connection property, where transmission time slots could be taken into account; a lossiness connection property, where dropping of data could be taken into account; a flow control connection property, where remote buffer space could be taken into account; data correctness, where error detection and/or correction codes could be taken into account, and so on. A POSITA reading claim 12 of the '800 Patent, in light of the specification, would understand these connection properties and the characteristics of the interconnects, and how to determine an optimal moment for sending the data in said first wrapper or said second wrapper according to these properties and characteristics, i.e., a moment that is optimal under the conditions. This is the plain and ordinary meaning.

207. Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

L. “first determination unit” / “second determination unit”

208. I understand that NST incorporates its definition for the term “determination unit” (as “circuit that makes determinations based on stored or received information”) and contends the remaining language should be afforded its plain and ordinary meaning. If the Court holds that Section 112 ¶ 6 applies, I understand that NST proposes the following construction: the function of the “first determination unit” is “determine a first optimal amount of data to be buffered by the first memory,” the function of the “second determination unit” is “determine a second optimal

amount of data to be buffered by the second memory,” and for at least one of the first determination unit and the second determination unit, the function is “determine an optimal moment for sending the data in said first wrapper or said second wrapper,” and the structure is “circuit.”

209. I understand that Defendants contend this term is subject to Section 112 ¶ 6. I understand that Defendants further contend the function is “determining a first/second optimal amount of data to be buffered by the first/second memory,” and for at least one of the first determination unit and the second determination unit, “determining an optimal moment for sending data,” and the structure is indefinite.

210. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

211. I understand that NST and Defendants have stipulated “integrated circuit” means “interconnected circuitry on a chip.” Opening Br. at 6. In my opinion, this meaning is consistent with how a POSITA reading the Asserted Patents would understand this term, and it is consistent with authoritative extrinsic sources, for example, THE NEW IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONICS TERMS, (5th ed. 1993), which defines an “integrated circuit” as “[a] combination of interconnected circuit elements inseparably associated on or within a continuous substrate.” **Exhibit I**; see also **Exhibit G**. The ’800 Patent describes the determination unit as being comprised in an integrated circuit. Accordingly, the determination unit is interconnected circuitry of the integrated circuit, i.e., the determination unit is a circuit, as explained below.

212. Asserted claim 12 of the ’800 Patent claims “[a]n integrated circuit comprising: . . . a plurality of interconnect modules including a first interconnect module and a second

interconnect module. . . , the first interconnect module further including a first determination unit [and] the second interconnect module further including a second determination unit, . . .” **Dkt. 1, Exhibit 6**, 11:44–12:5. Because an integrated circuit is interconnected circuitry on a chip, a POSITA would understand that the first and second determination units comprised in an integrated circuit discloses that the first and second determination units are interconnected circuitry of the integrated circuit, i.e., the first and second determination units are circuits.

213. The description of the determination unit in the specification of the ’800 Patent is consistent with the determination unit as recited in claim 12.

According to a preferred aspect of the invention at least one of said first and second wrapper means comprise a **determination unit BLDU for determining the optimal first or second amount of data to be buffered in said first or second wrapper means** before said data is transferred according to the communication properties of said communication between said first and second processing module.

Dkt. 1, Exhibit 6, 4:18–24 (emphasis added).

214. The specification of the ’800 Patent uses the term “determination unit” and “determination means” interchangeably, labeling both as “BLDU.” Several examples are reproduced below.

In addition, a **first and second determination means BLDU1, BLDU2** are arranged in the network interfaces NI associated to the slave S and the master M, respectively. The **first and second determination units BLDU1, BLDU2** serve to determine the optimal burst length for transferring data over the network N according to the current communication or connection properties.

Dkt. 1, Exhibit 6, 6:47–53 (emphasis added).

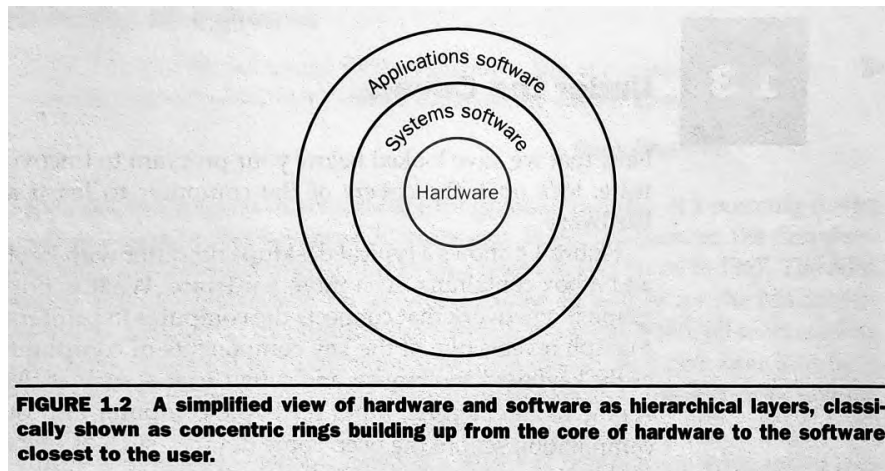
The determination of the optimal burst length may be performed based on information stored in the **determination units BDLU 1, 2 . . .**

Dkt. 1, Exhibit 6, 6:62–64 (emphasis added).

Besides the optimal burst length determination, also the transmission moment may be determined in a similar way by the **first and second determination means BLDU1, BLDU2**.

Dkt. 1, Exhibit 6, 7:4–6 (emphasis added).

215. The specification of the '800 Patent states before the claims section that “[i]n the device claim enumerating several means, several of these **means can be embodied by one and the same item of hardware.**” **Dkt. 1, Exhibit 6**, 8:34–36 (emphasis added). A POSITA understands the term “hardware” to mean physical circuitry. For example, the DICTIONARY OF COMPUTER AND INTERNET TERMS (7th ed. 2000) defines hardware as “the physical elements of a computer system; the computer equipment as opposed to the programs or information stored in the machine.” (**Exhibit M**). This term is often used in contrast with the term “software,” which a POSITA understands as describing instructions for execution by computer hardware, e.g., by physical circuitry like a processor (sometimes called a central processing unit (CPU)). For example, the DICTIONARY OF COMPUTER AND INTERNET TERMS (7th ed. 2000) defines software as “programs that tell a computer what to do. The term contrasts with *hardware*, which refers to the actual physical machines that make up a computer system.” (emphasis in original) (**Exhibit M**). The figure below shows a simplified hierarchical view of the hardware-software interface, with hardware at the core and software on the periphery for execution by the core. DAVID PATTERSON AND JOHN HENNESSEY, COMPUTER ORGANIZATION & DESIGN § 1, p. 9 (2nd ed. 1998) (**Exhibit N**).



216. Indeed, the specification of the '800 Patent indicates physical circuitry of the determination unit because the determination unit is configured to store information. **Dkt. 1, Exhibit 6**, 6:62–64 (“The determination of the optimal burst length may be performed based on **information stored in the determination units BDLU 1, 2** or on information received from the network N or IP blocks.” (emphasis added)). For the determination unit, which is comprised in an integrated circuit, to store information, the determination unit must comprise storage circuitry, such as flip-flops, latches, registers, random-access memory (RAM), and so on. Regarding the immediately above passage from the '800 Patent, Defendants’ Joint Opening Claim Construction Brief contends “the specification states that optimal burst length ‘may be’ performed based on information stored or received (i.e., it is optional).” Opening Br. at 43. However, this passage does not say that the determination may be performed based on information *that may be* stored in the determination units. In other words, the passage does not appear to suggest that storage of the information in the determination units is optional.

217. Based on the above evidence, it is my opinion that a POSITA would understand the determination unit is a circuit.

218. As recited in asserted claim 12, a determination unit is configured to determine an optimal amount of data to be buffered and an optimal moment for sending the data in a wrapper. **Dkt. 1, Exhibit 6**, 11:66–12:19 (“[F]irst determination unit is configured to determine a first optimal amount of data to be buffered . . . , the second determination unit is configured to determine a second optimal amount of data to be buffered . . . , at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper” (reciting claim 12)). In other words, a determination unit is configured to make determinations, including determining an optimal amount of data and an optimal moment for sending data.

219. Indeed, the specification of the ’800 Patent states the first and second determination units determine an optimal burst length. **Dkt. 1, Exhibit 6**, 6:59–53 (“The first and second determination units BLDU1, BLDU2 serve to determine the optimal burst length for transferring data over the network N according to the current communication or connection properties.”). Further, the specification of the ’800 Patent states “[t]he determination of the optimal burst length may be performed based on information stored in the determination units BDLU 1, 2 or on information received from the network N or IP blocks.” **Dkt. 1, Exhibit 6**, 6:62–64. In other words, a determination unit can determine a burst length based on stored or received information. Accordingly, a POSITA would understand that the determination unit makes determinations based on stored or received information.

220. The remaining language of this claim term, i.e., “first” and “second,” would be easily understood by a POSITA as indicating distinct determination units according to the plain and ordinary meaning of that language. Thus, it is my opinion that the correct understanding that

a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

221. I understand the Court may determine this term should be construed under 35 U.S.C. § 112 ¶ 6, means-plus-function. In this event, it is my opinion that NST's proposed structure for this term of "circuit" is correct and Defendants' proposed structure for this term as indefinite is incorrect. The proposed functions provided by both NST and Defendants are identical but for minor differences in formatting and verb tense.

222. As explained earlier in this section, a POSITA would recognize the structure of a determination unit to be a circuit *Supra* ¶¶ 211–217. Thus, it is my opinion that if the Court determines this term should be construed under 35 U.S.C. § 112 ¶ 6, then the correct understanding that a POSITA would have of this term as used in the Asserted Patents is the meaning provided by NST.

M. "said first wrapper" / "said second wrapper"

223. I understand that NST contends this term means "said first memory" / "said second memory."

224. I understand that Defendants contend this term is indefinite.

225. In my opinion, NST's proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

226. The issue alleged by Defendants is that "said first wrapper" and "said second wrapper" recited in claim 12 lack antecedent basis, and therefore, these terms are indefinite. I understand that "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig*

Instruments, Inc., 572 U.S. 898, 901 (2014). In my opinion, the alleged lack of antecedent basis of said first wrapper and said second wrapper would not fail to inform a POSITA, with reasonable certainty, the scope of the invention.

227. Asserted claim 12 of the '800 Patent recites, in relevant part, "a first memory for buffering first data . . . , a second memory for buffering second data . . . wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper" **Dkt. 1, Exhibit 6**, 11:62–19 (claim 12). In fact, the first memory is the only element in claim 12 described as buffering first data, and the second memory is the only element in claim 12 described as buffering second data, where a POSITA understands buffering to mean storing temporarily. Thus, it would be apparent to a POSITA just from the language of the claim that said first wrapper refers to the first memory and said second wrapper refers to the second memory. A reading of the specification of the '800 Patent would confirm that conclusion. For example, the specification discloses that a wrapper buffers data according to the following passages.

A first wrapper means associated to said second processing module

Dkt. 1, Exhibit 6, 3:41–43.

[A] second wrapper means is associated to the first processing module for buffering data

Dkt. 1, Exhibit 6, 3:54–56.

[E]ven if less than the first and second amount of data is buffered in said first and second wrapper means

Dkt. 1, Exhibit 6, 4:1–2.

[E]ven if less than the first and second amount of data is buffered in said first and second wrapper means

Dkt. 1, Exhibit 6, 4:7–8.

[A]t least one of said first and second wrapper means comprise a determination unit BLDU for determining the optimal first or second amount of data to be buffered in said first or second wrapper means

Dkt. 1, Exhibit 6, 4:18–22.

A second wrapper means associated to said second processing module buffers data

Dkt. 1, Exhibit 6, 4:41–43.

The wrapper means WM2, WM1, are responsible for buffering any data sent from the master M and the slave S over the network N. In particular, the two wrapper means WM1, WM2 buffer data coming from the master M or the slave S, respectively, until a certain amount of data is buffered.

Dkt. 1, Exhibit 6, 5:60–64.

[T]he wrapper means WM1, WM2 serve to buffer data to be sent over the network N until the conditions for an optimal transfer are satisfied.

Dkt. 1, Exhibit 6, 6:4–14.

The flushing of the buffered data may also be achieved by a first or second unbuffer signal received by the first or second wrapper means WM1, WM2. Therefore, if the first or second wrapper means WM1, WM2 receives an unbuffer signal, the data currently buffered are transferred as fast as possible, i.e. without waiting for the optimal burst length to be acquired.

Dkt. 1, Exhibit 6, 6:31–38.

228. Defendants provide two alternative meanings for said first wrapper and said second wrapper. First, Defendants contend that “[t]he terms ‘said first wrapper’ and ‘said second wrapper’ could be referring to the previously-recited ‘first interconnect module’ and ‘second interconnect module.’ Hassoun Decl. at ¶136.” Opening Br. at 44. Defendants argue that the wrapper may transfer data. Opening Br. at 44. However, Defendants concede that “the transferring function in claim 12 is performed by the first and second interconnect modules.”

Opening Br. at 44. Indeed. Nothing in claim 12 suggests that said first wrapper or said second wrapper perform a transferring function. Next, Defendants contend that “‘said first wrapper’ and ‘said second wrapper’ could be referring to a previously-unrecited structure, such as an interface structure. Hassoun Decl. at ¶137.” Opening Br. at 45. Defendants argue that wrappers have interface functionality and refer to extrinsic evidence for wrappers that convert between module protocols and interconnect protocols. Opening Br. at 45. But nothing in claim 12 suggests that said first wrapper or said second wrapper convert between module protocols and interconnect protocols.

229. Neither of the alternative meanings proffered by Defendants arise from the description of said first wrapper or said second wrapper as described in claim 12. Rather, a POSITA would understand that said first wrapper refers to the first memory and said second wrapper refers to the second memory.

230. Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

N. “wrapper”

231. I understand that NST contends this term means “memory.”

232. I understand Defendants contend this term is indefinite.

233. In my opinion, NST’s proposed construction is the correct understanding that a POSITA would have of this term as used in the Asserted Patents.

234. Asserted claim 12 of the ’800 Patent recites, in relevant part, “a first memory for buffering first data . . . , a second memory for buffering second data . . . wherein at least one of the first determination unit and the second determination unit is further configured to determine an optimal moment for sending the data in said first wrapper or said second wrapper” **Dkt.**

1, Exhibit 6, 11:62–19 (claim 12). In fact, the first memory is the only element in claim 12 described as buffering first data, and the second memory is the only element in claim 12 described as buffering second data, where a POSITA understands buffering to mean storing temporarily. Thus, it would be apparent to a POSITA just from the language of the claim that said first wrapper refers to the first memory and said second wrapper refers to the second memory, and therefore, that “wrapper” means “memory.” A reading of the specification of the ’800 Patent would confirm that conclusion. For example, the specification discloses that a wrapper buffers data according to the following passages.

A first wrapper means associated to said second processing module

Dkt. 1, Exhibit 6, 3:41–43.

[A] second wrapper means is associated to the first processing module for buffering data

Dkt. 1, Exhibit 6, 3:54–56.

[E]ven if less than the first and second amount of data is buffered in said first and second wrapper means

Dkt. 1, Exhibit 6, 4:1–2.

[E]ven if less than the first and second amount of data is buffered in said first and second wrapper means

Dkt. 1, Exhibit 6, 4:7–8.

[A]t least one of said first and second wrapper means comprise a determination unit BLDU for determining the optimal first or second amount of data to be buffered in said first or second wrapper means

Dkt. 1, Exhibit 6, 4:18–22.

A second wrapper means associated to said second processing module buffers data

Dkt. 1, Exhibit 6, 4:41–43.

The wrapper means WM2, WM1, are responsible for buffering any data sent from the master M and the slave S over the network N. In particular, the two wrapper means WM1, WM2 buffer data coming from the master M or the slave S, respectively, until a certain amount of data is buffered.

Dkt. 1, Exhibit 6, 5:60–64.

[T]he wrapper means WM1, WM2 serve to buffer data to be sent over the network N until the conditions for an optimal transfer are satisfied.

Dkt. 1, Exhibit 6, 6:4–14.

The flushing of the buffered data may also be achieved by a first or second unbuffer signal received by the first or second wrapper means WM1, WM2. Therefore, if the first or second wrapper means WM1, WM2 receives an unbuffer signal, the data currently buffered are transferred as fast as possible, i.e. without waiting for the optimal burst length to be acquired.

Dkt. 1, Exhibit 6, 6:31–38.

235. Thus, it is my opinion that the correct understanding that a POSITA would have of this term as used in the Asserted Patents, is the meaning provided by NST.

I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct. This declaration is executed this 16th day of November, 2023.

A handwritten signature in black ink, appearing to read "Erik Chmelar". The signature is fluid and cursive, with the first name "Erik" and last name "Chmelar" clearly distinguishable.

Dr. Erik Chmelar

Appendix 1

ERIK CHMELAR

(650) 533-7952 | echmelar@yahoo.com

Subject matter expert in semiconductor hardware and software with over two decades of experience developing, implementing, and protecting advanced technologies including digital and mixed-signal systems, high-speed serial communications, 5G/wireless telecommunications, and smart medical devices.

CREDENTIALS**EDUCATION —**

- | | |
|---|-----------|
| • JD, Intellectual Property , Univ. Michigan Law School, Ann Arbor, MI | 2015-2017 |
| • MBA, Management , Western Michigan Univ., Kalamazoo, MI | 2012-2013 |
| • BS, Chemical Physics , Saginaw Valley State Univ., University Center, MI | 2008-2011 |
| • PhD, Electrical Engineering , Stanford Univ., Stanford, CA | 2002-2004 |
| Dissertation: "Test and Diagnosis of Field-programmable Gate Arrays." | |
| • MS, Electrical Engineering , Stanford Univ., Stanford, CA | 2000-2001 |
| • BS, Electrical Engineering , Michigan Technological Univ., Houghton, MI | 1997-2000 |

LICENSES AND CERTIFICATIONS —

- | | |
|--|------------|
| • Agile Certified Practitioner (PMI-ACP, PMI) | 2015-pres. |
| • Certified Project Management Professional (PMP, PMI) | 2014-pres. |
| • Licensed Professional Engineer (PE, State of Michigan LARA) | 2010-pres. |
| • Licensed Patent Agent/Attorney (State Bar of Michigan, USPTO) | 2007-pres. |

EXPERIENCE

Technical Expert, Semiconductor Hardware/Software, Midland, MI 08/2007-pres.

- Serve as a technical expert witness for litigation in court and inter partes review (IPRs)
- Mine and analyze patent portfolios and develop assertion strategies for non-practicing entities (NPEs)
- Recent technology areas include memory, programmable hardware, microcontrollers, and AI devices

Senior Counsel, Young Basile Hanlon & MacFarlane, PC, Troy, MI 06/2023-pres.

- Draft and prosecute patent applications in a variety of semiconductor, software, and related arts
- Draft legal opinions for non-infringement, invalidity, and freedom-to-operate (FTO)
- Interview inventors, harvest inventions, and manage patent portfolios

Senior Associate, Dilworth IP, New Haven, CT 10/2020-06/2023

- Drafted and prosecuted patent applications in a variety of semiconductor, software, and related arts
- Drafted legal opinions for non-infringement, invalidity, freedom-to-operate (FTO), and export controls
- Interview inventors, harvest inventions, manage patent portfolios, and create technology landscapes

Senior Associate, Murphy, Bilak & Homiller, PLLC., Cary, NC 01/2020-06/2020

- Prosecuted patent applications for industry-leading wireless and semiconductor corporations
- Drafted approx. 100 office-action responses for complex 5G technologies
- Routinely referenced ETSI 3GPP specifications for prosecution of standard essential patents (SEPs)

Senior Manager, Innovation Partners, InterDigital, Inc., Wilmington, DE 09/2015-10/2018

- Created patent portfolios for 5G, IoT, connected/autonomous vehicles, and augmented/virtual reality
- Managed scientists and engineers to create over 100 new invention disclosures / patent applications
- Forged research partnerships with commercial and academic organizations to develop patent portfolios

Co-founder, Managing Member, Dera Industries LLC., Midland, MI 05/2016-07/2017

- Developed and productized the award-winning One-Tie™ re-usable tie strap consumer product
- Achieved \$1 million in annual sales prior to licensing the intellectual property

Senior Principal Engineer, Adv. Dev., Stryker Corp., Kalamazoo, MI 02/2012-03/2015

- Supervised R&D of disruptive medical instruments and surgical technologies
- Formalized new business opportunities, developed budgets and timelines, and staffed project teams
- Collaborated with several top-tier universities to bring necessary expertise into the organization
- Delivered working prototypes for biophotonic devices and boundary-constraint surgical robotics

Staff SW Engineer, Adv. Tech. Dev., LSI Corp. (Broadcom), Milpitas, CA 07/2004-01/2012

- Conducted R&D for very large scale integrated (VLSI) and serializer-deserializer (SerDes) circuits
- Granted approx. 20 patents for physical (PHY) interfaces, SerDes, and VLSI test architectures
- Made cutting-edge contributions in SerDes and test that were implemented in customer designs

Adjunct Professor, ECE Dept., SVSU, University Center, MI 01/2009-01/2012

- Taught courses in digital circuits, computer architecture and organization, and data communications

Consulting Assistant Professor, EE/CS Dept., Stanford University, Stanford, CA 09/2006-08/2008

- Advised PhD students on the test and reliability of VLSI circuits
- Created and taught a PhD-level course on clock and data recovery (CDR) for digital communications

Product Test Engineer, Xilinx, Inc., Los Gatos, CA (PhD. Intern, two summers) 06/2002-09/2003

- Engineered tools to detect and diagnose defects in FPGAs, which reduced diagnosis time by 75%

Manufacturing Engineer, Cisco Systems, Inc., San Jose, CA 11/1999-04/2002

- Oversaw functional testing of layer-2/3 network switches and determined root-cause failures

SERVICE AND MENTORING

Admissions Representative, Univ. Michigan Law School, Ann Arbor, MI 2018

- Advised prospective law students at 30 law fairs and forums

Instructor, National Science Foundation, Western Michigan Univ. I-Corps, Kalamazoo, MI 2015

- Taught Lean Startup and Business Canvas fundamentals to a cohort of 30 entrepreneurs

Engineering Program Evaluator, Accred. Board of Eng. & Tech. (ABET), Baltimore, MD 2013-2014

- Evaluated electrical engineering and computer engineering university educational programs

Industry Mentor, National Science Foundation, Univ. Michigan I-Corps, Ann Arbor, MI 2013

- Mentored teams of medical-device entrepreneurs participating in the I-Corps program

Industry Mentor, Western Michigan Univ., Starting Gate Accelerator, Kalamazoo, MI 2013

- Mentored entrepreneurs participating in the university startup-accelerator program

SELECT PROFICIENCIES

- | | |
|--|--|
| • Hardware – Verilog, VHDL, ASICs, FPGAs | • Software – C/C++, Perl, Java, MatLab |
| • Engineering – COMSOL, ANSYS | • CAD – SolidWorks, AutoCAD, Blender |

Select US Patents

US11446109B2, “Metal detection system for use with medical waste container,” issued 2022-09-23.

US11389556B2, “Sterilization container capable of providing an indication regarding whether or not surgical instruments sterilized in the container were properly sterilized,” issued 2022-07-19.

US11357877B2, “Sterilization enclosure for surgical instruments,” issued 2022-06-14.

US\$ 11225996B1, “Dual hook clasp,” issued 2022-01-18.

US11002308B2, “Hook device with opposing jaws,” issued 2021-05-11.

US11000341B2, “Metal detection system for use with medical waste container,” issued 2021-05-11.

US10994906B2, “Easy-to-remove cable tie,” issued 2021-05-04.

US10731698B2, “Hook device with rotatable opposing jaws,” issued 2020-08-04.

US10604317B2, “Reusable tie strap with multiple apertures,” issued 2020-03-31.

US10258706B2, “Sterilization container capable of providing an indication regarding whether or not surgical instruments sterilized in the container were properly sterilized,” issued 2019-04-16.

US10010636B2, “Sterilization container capable of providing an indication regarding whether or not surgical instruments sterilized in the container were properly sterilized,” issued 2018-07-03.

US9292644B2, “Row based analog standard cell layout design and methodology,” issued 2016-03-22.

US9087157B2, “Low-loss transmission line TDM communication link and system,” issued 2015-07-21.

US9014313B2, “Error signature analysis for data and clock recovery in a communication system,” issued 2015-04-21.

US8982941B2, “Predictive selection in a fully unrolled decision feedback equalizer,” issued 2015-03-17.

US8929497B2, "Dynamic deskew for bang-bang timing recovery in a communication system," issued 2015-01-06.

US8923382B2, "Tap adaptation with a fully unrolled decision feedback equalizer," issued 2014-12-30.

US8615062B2, "Adaptation using error signature analysis in a communication system," issued 2013-12-24.

US8527912B2, "Digitally obtaining contours of fabricated polygons," issued 2013-09-03.

US8432250B2, "Process variation based microchip identification," issued 2013-04-30.

US8121186B2, "Systems and methods for speculative signal equalization," issued 2012-02-21.

US7956790B2, "Systems and methods for synchronous, retimed analog to digital conversion," issued 2011-07-05.

US7973692B2, "Systems and methods for synchronous, retimed analog to digital conversion," issued 2011-06-07.

US7779320B2, "Low power scan shifting with random-like test patterns," issued 2010-08-17.

US7696915B2, "Analog-to-digital converter having reduced number of activated comparators," issued 2010-04-13.

US7656340B2, "Systems and methods for pipelined analog to digital conversion," issued 2010-02-02.

US7656339B2, "Systems and methods for analog to digital conversion," issued 2010-02-02.

US7328386B2, "Methods for using checksums in X-tolerant test response compaction in scan-based testing of integrated circuits," issued 2008-02-05.

US7293312B2, "Multipurpose skateboard tool," issued 2007-11-13.

US7210083B2, "System and method for implementing postponed quasi-masking test output compression in integrated circuit," issued 2007-04-24.

US7206983B2, "Segmented addressable scan architecture and method for implementing scan-based testing of integrated circuits," issued 2007-04-17.

US7093842B2, "Skateboard truck assembly," issued 2006-08-22.

US6979142B1, "Retractable tip mechanical pencil assembly," issued 2005-12-27.

US6920621B1, "Methods of testing for shorts in programmable logic devices using relative quiescent current measurements," issued 2005-07-19.

Select Publications

- E. Chmelar, “Error signature analysis (ESA) receiver architecture for data communication,” DesignCon, 2012.
- E. Chmelar and C. Ito, “Mostly digital SerDes (MDS): a comprehensive low power receiver architecture,” DesignCon, 2012.
- I. Park, D. Lee, E. Chmelar, and E. McCluskey, “Inconsistent fails due to limited tester timing accuracy,” Proc. 26th VLSI Test Symp., 2008.
- A. Al-Yamani, N. Devta-Prasanna, E. Chmelar, M. Grinchuk, and A. Gunda, “Scan test cost and power reduction through systematic scan reconfiguration,” IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 26, pp. 907–918, 2007.
- A. Al-Yamani, E. Chmelar, and M. Grinchuk, “Segmented addressable scan architecture,” Proc. 23rd VLSI Test Symp., 2005.
- E. Chmelar, “Minimizing the number of test configurations for FPGAs,” Int. Conf. Computer Aided Design, 2004.
- E. Chmelar, “The test and diagnosis of FPGAs,” Ph.D. thesis, Stanford University, 2004.
- E. Chmelar and S. Toutounchi, “FPGA bridging fault detection and location via differential IDDQ,” Proc. 22nd VLSI Test Symp., 2004.
- E. Chmelar, “Subframe multiplexing: FPGA manufacturing test time reduction,” CRC TR-04-01, 2004.
- E. Chmelar, “Subframe multiplexing for FPGA manufacturing test,” Proc. Int. Symp. FPGAs, 2004.
- E. Chmelar, “FPGA interconnect delay fault testing,” Proc. Int. Test Conf., pp. 1239–1247, 2003.

Select Professional Organizations

State Bar of Michigan
Member (2018-pres.)

Project Management Institute
Certified Agile Practitioner (2014-pres.)
Certified Project Management Professional (2015-pres.)

Association for Computing Machinery
Member (2018-2019)

Accreditation Board of Engineering and Technology
Program Evaluator (2013-2018)

Institute of Electrical & Electronic Engineers
Senior Member (2004-2018)

American Chemical Society
Member (2013-2016)

National Science Foundation I-Corps
Instructor (2015)
Industry Mentor (2013)

American Society of Mechanical Engineers
Member (2014-2015)

International Society of Optics & Photonics
Member (2015)

Appendix 2

Declaration of Dr. Erik Chmelar

List of Materials Considered

- Local Patent Rule 4-3 Joint Claim Construction and Prehearing Statement (Dkt. 49)
- U.S. Patent No. 7,366,818 (“818 patent”) (**Dkt. 1, Exhibit 1**)
- U.S. Patent No. 7,373,449 (“449 patent”) (**Dkt. 1, Exhibit 2**)
- U.S. Patent No. 7,594,052 (“052 patent”) (**Dkt. 1, Exhibit 3**)
- U.S. Patent No. 7,769,893 (“9893 patent”) (**Dkt. 1, Exhibit 4**)
- U.S. Patent No. 8,072,893 (“2893 patent”) (**Dkt. 1, Exhibit 5**)
- U.S. Patent No. 8,086,800 (“800 patent”) (**Dkt. 1, Exhibit 6**)
- NEIL WESTE & DAVID HARRIS, CMOS VLSI DESIGN: A CIRCUITS AND SYSTEMS PERSPECTIVE 29 (4th ed. 2010) (**Exhibit A**)
- JAN RABAEY, ANANTHA CHANDRAKASAN & BORIVOJE NIKOLIC, DIGITAL INTEGRATED CIRCUITS: A DESIGN PERSPECTIVE 380–381, 395, 487–488 (2d ed. 2003) (**Exhibit B**)
- William J. Dally & Brian Towles, *Route Packets, Not Wires: On-Chip Interconnection Networks*, PROC. 38TH DESIGN AUTOMATION CONF., 684, 684–689 (2001) (**Exhibit C**)
- JOHN F. WAKERLY, DIGITAL DESIGN: PRINCIPLES AND PRACTICES 358 (4th ed. 2005) (**Exhibit D**)
- FAYEZ GEBALI, HAYTHAM ELMILIGI & MOHAMED WATHEQ EL-KHARASHI, NETWORKS-ON-CHIPS: THEORY AND PRACTICE 310 (2009) (**Exhibit E**)
- Kurt Schuler, *Busses, Crossbars and NoCs: The 3 Eras of SoC Interconnect History*, ARTERISIP (Oct. 22, 2010, 12:12 P.M.), <https://www.arteris.com/blog/bid/49081/busses-crossbars-and-nocs-the-3-eras-of-soc-interconnect-history> (**Exhibit F**)
- IEEE 100: THE AUTHORITATIVE DICTIONARY OF IEEE STANDARDS TERMS (7th ed. 2000) (**Exhibit G**)
- THE COMPUTER GLOSSARY (Alan Freedman ed., 8th ed. 1998) (**Exhibit H**)
- THE NEW IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONICS TERMS (5th ed. 1993) (**Exhibit I**)
- Prosecution History of U.S. Patent No. 7,373,449 (**Exhibit J**)

- WILLIAM STALLINGS, DATA & COMPUTER COMMUNICATIONS § 1.2, p. 307 (6th ed. 1999) (**Exhibit K**)
- WEBSTER'S NEW WORLD DICTIONARY OF COMPUTER TERMS (5th ed. 1994) (**Exhibit L**)
- DICTIONARY OF COMPUTER AND INTERNET TERMS (Douglas Downing, et al., 7th ed. 2000) (**Exhibit M**)
- DAVID PATTERSON AND JOHN HENNESSEY, COMPUTER ORGANIZATION & DESIGN § 1, p. 9 (2nd ed. 1998) (**Exhibit N**)