

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED and
SAMSUNG ELECTRONICS CO., LTD.
Petitioners

v.

NETWORK SYSTEM TECHNOLOGIES, LLC
Patent Owner

Patent No. 8,072,893

Inter Partes Review No. IPR2024-00355

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	RELATED MATTERS	2
A.	The Samsung Litigation	2
B.	The Qualcomm Litigation	2
C.	The TI Litigation	3
D.	Other Litigations.....	3
III.	OVERVIEW OF THE ‘2893 PATENT	3
IV.	THE ‘2893 PATENT’S PROSECUTION HISTORY	5
V.	LEVEL OF SKILL IN THE RELEVANT FIELD OF ART	7
VI.	CLAIM CONSTRUCTION	7
A.	The Disputed District Court Constructions.....	8
B.	Agreed District Court Constructions.....	9
VII.	THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION PURSUANT TO 35 U.S.C. § 314(A) IN VIEW OF THE PARALLEL DISTRICT COURT PROCEEDING.....	10
A.	The Board Has Discretion to Deny Institution.....	10
B.	Parallel District Court Proceedings Will Determine the Issues Raised in the Petition Before the Board.....	13
C.	The First Factor is Neutral	15
D.	The Second Factor Favors Denial	15
E.	The Third Factor Favors Denial	18
F.	The Fourth Factor Should Favor Denial or Only Marginally Favors Institution.....	20
G.	The Fifth Favor Favors Denial	22
H.	The Sixth Factor Favors Denial	22
VIII.	PETITIONERS HAVE NOT ESTABLISHED ANY CLAIM IS UNPATENTABLE.....	22
A.	Ground 1: Purported Anticipation by Bertozzi (Claims 1-3, 6-7,	

and 10)	23
B. Ground 2: Purported Obviousness over Bertozzi Alone or in View of Jantsch or Duato (Claims 1–3, 6–7, and 10)	32
C. Ground 3: Purported Obviousness over Dielissen in View of Hassoun (Claims 1–3, 6, 7, 9 and 10)	35
D. Ground 4: Purported Obviousness over Grounds 1–3 Further in View of Sullam (Claim 8)	50
IX. CONCLUSION.....	50

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Allergan, Inc. v. Sandoz Inc.</i> , 796 F.3d 1293 (Fed. Cir. 2015)	32
<i>Apple Inc. v. Fintiv, Inc.</i> , IPR2020-00019, Paper 11 (Mar. 20, 2020)	<i>passim</i>
<i>Apple Inc. v. Fintiv, Inc.</i> , IPR2020-00019, Paper 15 (May 13, 2020).....	11, 15
<i>Apple Inc. v. Iancu</i> , No. 5:20-cv-06128-EJD (N.D. Cal.).....	13
<i>Application of Ratti</i> , 270 F.2d 810 (CCPA 1959)	35
<i>Arctic Cat Inc. v. Bombardier Recreational Prod. Inc.</i> , 876 F.3d 1350 (Fed. Cir. 2017)	30, 32
<i>Cisco Sys., Inc. v. Estech Sys., Inc.</i> , IPR2021-00329, Paper 13 (PTAB July 6, 2021)	19
<i>CommScope Technologies, LLC v. Dali Wireless Inc.</i> , IPR2022-01242, Paper 23 (Feb. 27, 2023)	11, 22
<i>Dolby Labs., Inc. v. Intertrust Techs. Corp.</i> , IPR2020-01106, Paper 12 (PTAB Jan. 5, 2021)	19
<i>E-One, Inc. v. Oshkosh Corp.</i> , IPR2019-00161, Paper 16 (PTAB May 15, 2019)	17, 18
<i>Harmonic Inc. v. Avid Tech., Inc.</i> , 815 F.3d 1356 (Fed. Cir. 2016)	10
<i>Merck Sharp & Dohme B.V. v. Warner Chilcott Co., LLC</i> , 711 F. App'x 633 (Fed. Cir. 2017)	34

<i>Network System Technologies, LLC v. Qualcomm Inc. et al.</i> , No. 2:22-cv-01331-DAE (W.D. Tex.).....	<i>passim</i>
<i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:22-cv-00481-JRG (E.D. Tex.)	<i>passim</i>
<i>Network System Technologies, LLC v. Texas Instruments, Inc.</i> , No. 2:22-cv-00482-RWS (E.D. Tex.).....	<i>passim</i>
<i>NHK Spring Co., Ltd. v. Intri-Plex Technologies, Inc.</i> , IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018).....	16, 17, 18
<i>Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.</i> , 68 F.3d 1013 (Fed. Cir. 2017)	7-8
<i>Oil States Energy Servs. LLC v. Green’s Energy Grp., LLC</i> , 138 S. Ct. 1365 (2018).....	10
<i>OpenSky Indus., LLC v. VLSI Tech. LLC</i> , IPR2021-01064, Paper 102 (PTAB Oct. 4, 2022).....	11, 12
<i>Polaris Indus., Inc. v. Arctic Cat, Inc.</i> , 882 F.3d 1056 (Fed. Cir. 2018)	33
<i>Trivascular, Inc. v. Samuels</i> , 812 F.3d 1056 (Fed. Cir. 2016)	34

Statutes

5 U.S.C. § 553.....	12
35 U.S.C. § 102(b)	6
35 U.S.C. § 103(a)	6
35 U.S.C. § 314.....	10, 13, 16, 18

Regulations

37 C.F.R. § 42.207	1
--------------------------	---

LISTING OF EXHIBITS

Exhibit No.	Description
2001	Declaration of Dr. Erik Chmelar
2002	<i>Curriculum vitae</i> of Dr. Erik Chmelar
2003	Neil Weste & David Harris, CMOS VLSI DESIGN: A CIRCUIT AND SYSTEMS PERSPECTIVE (4th ed. 2010)
2004	Jan Rabaey, Anantha Chandrakasan & Borivoje Nikolic, DIGITAL INTEGRATED CIRCUITS: A DESIGN PERSPECTIVE (2nd ed. 2003)
2005	William J. Dally & Brian Towles, <i>Route Packets, Not Wires: On-Chip Interconnection Networks</i> , PROC. 38TH DESIGN AUTOMATION CONF. (2001)
2006	John F. Wakerly, DIGITAL DESIGN: PRINCIPLES AND PRACTICES (4th ed. 2005)
2007	Fayez Gebali, Haytham Elmiligi & Mohamed Watheq El-Kharashi, NETWORKS-ON-CHIPS: THEORY AND PRACTICE (2009)
2008	Kurt Shuler, <i>Busses, Crossbars and NoCs: The 3 Eras of SoC Interconnect History</i> , ARTERISIP (Oct. 22, 2010), https://www.arteris.com/blog/busses-crossbars-and-nocs-the-3-eras-of-soc-interconnect-history/
2009	Kurt Shuler, <i>The SoC Interconnect Fabric: A Brief History</i> , ARTERISIP (Aug. 6, 2013), https://www.arteris.com/blog/the-soc-interconnect-fabric-a-brief-history/
2010	William Stallings, DATA & COMPUTER COMMUNICATIONS (6th ed. 1999)
2011	L.P. Carloni, N.E. McMillan, & Sangiovanni-Vincentelli, "Theory of Latency-Insensitive Design," <i>IEEE Trans. On CAD of ICs and Systems</i> , vol. 20, no. 9, (Sep. 2001)
2012	United States District Courts — National Judicial Caseload Profile
2013-2016	RESERVED

Exhibit No.	Description
2017	U.S. Patent No. 7,373,449
2018-2020	RESERVED
2021	Docket Control Order, <i>Network System Technologies, LLC v. Texas Instruments Incorporated</i> , Civil Action No. 2:22-cv-00482-RWS (E.D. Tex.), Dkt. 49 (Apr. 28, 2023)
2022	Claim Construction Order, <i>Network System Technologies, LLC v. Texas Instruments Incorporated</i> , Civil Action No. 2:22-cv-00482-RWS (E.D. Tex.), Dkt. 150 (Jan. 3, 2024)
2023-2026	RESERVED
2027	Complaint, <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al.</i> , Civil Action No. 2:22-cv-00481-JRG (E.D. Tex.), Dkt. 1 (Dec. 19, 2022)
2028	Docket Control Order, <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al.</i> , Civil Action No. 2:22-cv-00481-JRG (E.D. Tex.), Dkt. 59 (Jun. 16, 2023)
2029-2032	RESERVED
2033	P.R. 4-3 Claim Construction and Prehearing Statement, <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd.</i> , Civil Action No. 2:22-cv-00482-RWS (E.D. Tex.), Dkt. 91 (Jan. 9, 2024)
2034	Plaintiff Network System Technologies, LLC's Opening Claim Construction Brief, <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd.</i> , Civil Action No. 2:22-cv-00482-RWS (E.D. Tex.), Dkt. 100 (Feb. 20, 2024)
2035	Defendant Samsung Electronics Co., Ltd.'s Responsive Claim Construction Brief, <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd.</i> , Civil Action No. 2:22-cv-00482-RWS (E.D. Tex.), Dkt. 112 (March 12, 2024)
2036	Plaintiff Network System Technologies, LLC's Reply Construction Brief, <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd.</i> , Civil Action No. 2:22-cv-00482-

Exhibit No.	Description
	RWS (E.D. Tex.), Dkt. 116 (March 19, 2024)
2037	Complaint, <i>Network System Technologies, LLC v. Qualcomm Incorporated et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.) Dkt. 1 (Dec. 19, 2022)
2038	First Amended Complaint, <i>Network System Technologies, LLC v. Qualcomm Incorporated et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.) Dkt. 57 (Aug. 7, 2023)
2039	Second Amended Scheduling Order, <i>Network System Technologies, LLC v. Qualcomm Incorporated et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.) Dkt. 80 (Oct. 23, 2023)
2040	Defendants' Joint Opening Claim Construction Brief, <i>Network System Technologies, LLC v. Qualcomm Incorporated et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.), Dkt. 77 (Oct. 12, 2023)
2041	Plaintiff Network System Technologies, LLC's Responsive Claim Construction Brief, <i>Network System Technologies, LLC v. Qualcomm Incorporated et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.), Dkt. 81 (Nov. 16, 2023)
2042	Defendants' Joint Reply Claim Construction Brief, <i>Network System Technologies, LLC v. Qualcomm Incorporated et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.), Dkt. 83 (Nov. 30, 2023)
2043	Plaintiff Network System Technologies, LLC's Sur-Reply Claim Construction Brief, <i>Network System Technologies, LLC v. Qualcomm Incorporated et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.), Dkt. 86 (Dec. 14, 2023)
2044	Defendants' Supplemental Claim Construction Brief, <i>Network System Technologies, LLC v. Qualcomm Incorporated et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.), Dkt. 105 (Mar. 1, 2024)
2045	Plaintiff Network System Technologies, LLC's Supplemental Claim Construction Brief, <i>Network System Technologies, LLC v.</i>

Exhibit No.	Description
	<i>Qualcomm Incorporated et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.), Dkt. 106 (Mar. 1, 2024)
2046-2049	RESERVED
2050	Defendants' Invalidity and Ineligibility Contentions And Disclosures Pursuant to Patent Rule 3-3 Cover Pleading, <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd., et al.</i> , Civil Action No. 2:22-cv-00481-JRG (E.D. Tex.) (July 11, 2023)
2051	Defendants' Invalidity and Ineligibility Contentions Cover Pleading, <i>Network System Technologies, LLC v. Qualcomm Incorporated, et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.) (Sep. 22, 2023)
2052	Joint Claim Construction Statement, <i>Network System Technologies, LLC v. Qualcomm Incorporated, et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.), Dkt. 87 (Dec. 18, 2023)
2053	Exhibit E-5 to Defendants' Invalidity Contentions, <i>Network System Technologies, LLC v. Qualcomm Incorporated, et al.</i> , Civil Action No. 1:22-cv-1331-DAE (W.D. Tex.) (Sep. 22, 2023)
2054	Exhibit E-5 to Defendants' Invalidity Contentions, <i>Network System Technologies, LLC v. Samsung Electronics Co., Ltd., et al.</i> , Civil Action No. 2:22-cv-00481-JRG (E.D. Tex.) (July 11, 2023)

Network System Technologies, LLC (“NST” or “Patent Owner”) submits this preliminary response under 37 C.F.R. § 42.207 to the Petition for *Inter Partes* Review (“Petition”) of U.S. Patent No. 8,072,893 (“the ‘2893 Patent”), filed by Qualcomm Incorporated (“Qualcomm”) and Samsung Electronics Co., Ltd. (“Samsung”) (collectively, “Petitioners”).

I. INTRODUCTION

Patent Owner respectfully requests that the Board deny institution. The Board should exercise its discretion to deny institution pursuant to 35 U.S.C. § 314(a) in light of co-pending litigation between Petitioners and Patent Owner in the Eastern and Western District of Texas involving the ‘2893 patent. The Samsung litigation is set for trial prior to the time of a final written decision, and claim construction will be fully briefed and argued before an institution decision. The Qualcomm litigation is expected to be set for trial prior to the time of a final written decision, and claim construction has been fully briefed and argued. On balance, the factors set forth in the Board’s precedential *Fintiv* decision weigh in favor of denying discretion.

Further, Petitioners have not demonstrated a reasonable likelihood of success on the merits. Petitioners have failed to show that a key limitation is present in each of the independent claims for each of the presented grounds. The same limitations were the basis for allowance during examination of the application that became the ‘2893 Patent.

Accordingly, Patent Owner respectfully submits that institution should be denied.

II. RELATED MATTERS

As summarized below, the '2893 Patent is asserted in five pending district court proceedings in the Eastern District of Texas and Western District of Texas.

A. The Samsung Litigation

As of this Response, claims 1 and 10 of the '2893 Patent are asserted against Petitioner in *Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00481-JRG (E.D. Tex.) (hereinafter, "the Samsung Litigation"). A jury trial is scheduled for October 28, 2024. EX2028, 1.

The parties filed a Joint Claim Construction and Prehearing Statement with disputed and agreed claim constructions for the '2893 Patent on January 10, 2024. EX2033. Patent Owner's Opening Claim Construction Brief was filed February 20, 2024 (EX2034), Petitioner's Responsive Claim Construction Brief was filed March 12, 2024 (EX2035), and Patent Owner's Reply Claim Construction Brief was filed March 19, 2024 (EX2036). EX2028, 3. A *Markman* hearing is scheduled for April 9, 2024. EX2028, 3.

B. The Qualcomm Litigation

As of this Response, claim 10 of the '2893 Patent is asserted in *Network System Technologies, LLC v. Qualcomm Inc. et al.*, No. 2:22-cv-01331-DAE (W.D.

Tex.) (hereinafter, “the Qualcomm Litigation”). There is no trial date yet, but it is expected to be in early 2025. *See* EX2039. The parties completed claim construction briefing (EX2040-EX2045) and conducted a *Markman* hearing on December 21, 2023. EX2039, 6.

C. The TI Litigation

As of this Response, claim 10 of the ‘2893 Patent is asserted in *Network System Technologies, LLC v. Texas Instruments, Inc.*, No. 2:22-cv-00482-RWS (E.D. Tex.) (hereinafter, “the TI Litigation”). A jury trial is scheduled for November 4, 2024. EX2021. The court issued a *Markman* order on January 3, 2024 construing several terms in the ‘2893 Patent (“the TI Order”). EX2022; *Infra*, § VI.

D. Other Litigations

As of this Response, the ‘2893 Patent is asserted in *Network System Technologies, LLC v. Lenovo Group Ltd.*, No. 2:23-cv-00167-JRG (E.D. Tex.), *Network System Technologies, LLC v. Ford Motor Co.*, No. 2:23-cv-00440-DAE (W.D. Tex.), *Network System Technologies, LLC v. OnePlus Technology (Shenzhen) Co., Ltd.*, 2:23-cv-00520 (E.D. Tex.). These cases are currently stayed.

III. OVERVIEW OF THE ‘2893 PATENT

The ‘2893 Patent describes an integrated circuit that includes functional blocks and a data communication network. EX1001, Abstract; EX2001, ¶¶69, 73-73. The data communication network, also referred to as a network on chip (NoC)

facilitates flexible communication limits the amount of wires required in the integrated circuits. EX1001, 1:19:22; EX2001, ¶69. This network comprises network stations interconnected via communication channels, enabling the communication of data packages between the functional blocks. EX1001, Abstract; EX2001, ¶69. The network stations comprise data routers and network interfaces, with each data router connected to a functional block via a network interface. EX1001, Abstract; EX2001, ¶69.

The '2893 Patent identifies that “[a] problem associated with communication channels ... is that the clock speed at which the [integrated circuit] can operate may be determined by the slowest communication channel, i.e. the channel exhibiting the largest data transfer delay.” EX1001, 1:34–38; EX2001, ¶69.

The '2893 Patent teaches that “[t]o avoid having to limit the communication speed, e.g. the clock speed, of the data communication network 100 in accordance with the delay characteristics of the communication channel 150 between two network stations ... [the] communication channel ... is equipped with $M*N$ data storage elements to introduce a delay of $M*N$ cycles into the communication channel, with N corresponding to the size of a data package.” EX1001, 5:49–58; EX2001, ¶70. The '2893 Patent also teaches that “[e]ach data package comprising N data elements including a data element comprising routing information for the network stations.” EX1001, 1:65-2:6; EX2001, ¶70. This allows for “an increase of

the maximum communication frequency of the data network 100 at the expense of the introduction of a delay of a single data package, i.e. the number of clock cycles it takes to communicate such a data package, on the slow communication channel.” EX1001, 5:58-62; EX2001, ¶70.

The '2893 Patent also details a method for designing an integrated circuit with such a data communication network. EX2001, ¶75. This involves identifying communication channels with delays exceeding predefined thresholds and inserting M*N data storage elements to introduce the necessary delays, thereby optimizing the communication network's performance. EX1001, 3:34-53; EX2001, ¶75.

The '2893 Patent thus discloses “an integrated circuit including an on-chip network where data storage elements are introduced on certain slower communication channels to introduce a delay to resynchronize the slower channels with other channels.” EX2001, ¶71. This technology allows for flexible, efficient data communication within integrated circuits, enhancing their performance and reliability in processing and transferring large amounts of data across different functional blocks.

IV. THE '2893 PATENT'S PROSECUTION HISTORY

The '2893 Patent granted from U.S. Application No. 11/912,175 (“the '175 application”). EX1001, cover. During the examination of the '175 application, the Examiner initially rejected then pending claims 1–3, 6, and 10 based on 35 U.S.C.

§103(a), over U.S. Patent 7,362,763 (Wybenga) in view of U.S. Patent 7,197,009 (Dispensa). EX1002, 125-133.

In response, the applicant made stylistic modifications to the claims without altering the subject matter of the claims. EX1002, 144, 152-157; EX2001, ¶76. The applicant submitted that the office action conceded that Wybenga fails to disclose the claimed “M*N data storage elements, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel.” EX1002, 159-160. Additionally, the applicant argued that Dispensa's teaching that the “delay variation is the difference between the delay of link 411 and the delay of link 412” does not “disclose or suggest any storage elements, let alone disclosing or suggesting any ‘network comprising M*N data storage elements, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel.’” EX1002, 160.

Subsequently, the Examiner issued an Office Action on January 12, 2011, rejecting claims 1-3, 6, and 9 under 35 U.S.C. § 102(b) by U.S. Patent Publication No. 2002/0087716 (Mustafa), and claim 10 under 35 U.S.C. § 103(a) over Mustafa in view of U.S. Patent Publication No. 2004/019709 (Selvaggi). EX1002, 169-185.

In response, the applicant amended claim 10 to recite: “in response to the identifying act, inserting M*N data storage elements into the data communication network, M being a positive integer, for introducing a delay of M*N cycles on the

first communication channel.” EX1002, 194, 200-201. Applicant argued that neither Mustafa or Selvaggi, alone or in combination, “disclose or suggest introducing any delay, let alone ... **in response to identifying** that the first communication channel has a data transfer delay exceeding a predefined threshold, **inserting** M*N data storage elements into the data communication network for introducing a delay of M*N cycles on the first communication channel.” EX1002, (emphasis added), 205.

The Examiner, upon reviewing the amendments and arguments, allowed the ‘175 application, leading to the issuance of the ‘2893 Patent. EX1002, 211-220, 238.

V. LEVEL OF SKILL IN THE RELEVANT FIELD OF ART

With respect to the ‘2893 patent, Patent Owner applies the following identification of a person of ordinary skill in the art (“POSITA”) adopted by the District Court in the TI Litigation: “a POSITA would have at least a Bachelor’s degree in electrical engineering, computer engineering, or a related field, and as at least two years of work experience in the field of SoC [(“system-on-chip”)] and NoC [(“Network-on-Chip”)] technologies.” EX2022, 18; EX2001, ¶38.

VI. CLAIM CONSTRUCTION

Patent Owner submits that claim construction is not necessary at this time for the Board to find that Petitioners did not meet their burden for institution. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Although Petitioners identify several claim terms at issue in pending district

court litigation, Petitioners state that “[they] do not believe the Board needs to resolve those disputes to decide the issues raised by this *inter partes* review challenge.” Petition, 9-10. Patent Owner agrees but reserves the right to seek constructions of these terms in litigation and in this *inter partes* review, and to further respond to any constructions that the Petitioners submit. Nevertheless, Patent Owner identifies several claim terms and their proposed constructions in pending district court litigations below relating to the ‘2893 Patent.

A. The Disputed District Court Constructions

1. “each data package comprising N data elements” (claims 1, 7, and 10)

Term	Samsung/Qualcomm District Court Construction	NST District Court Construction
“each data package comprising N data elements”	“every data package communicated by the network stations has a fixed size of N data elements”	“data package” means “fixed-size arrangement of data,” “data elements” means “groups of data,” and the remaining language should be afforded its plain and ordinary meaning.

EX2052, 5; EX2033, Appendix 2, p. 6 (p. 14).

2. “data storage elements” (claims 1, 3, 7, and 10)

Term	Qualcomm District Court Construction	NST District Court Construction
“data storage elements”	“each being a structure that stores one data element”	“Array of one or more elements that store data”

EX2052, 5. Samsung did not propose a construction for “data storage elements” in the district court case. EX2033.

B. Agreed District Court Constructions

1. The preamble of claim 10

In the Qualcomm Litigation and Samsung Litigation, the parties agreed that the preamble of claim 10 should be construed as limiting. EX2052, 1; EX2033, Appendix 1, p. 4 (p. 8). The same construction was adopted by the district court in the TI Litigation. See EX2022, 19.

2. “network” (claims 1, 2, 7, 9, and 10)

In both the Qualcomm Litigation and Samsung Litigation, the parties agreed that “network” should be construed as “multi-hop interconnection between modules separated by one or more network nodes.” EX2052, 1; EX2033, Appendix 1, p. 1 (p. 5). The same construction was adopted by the district court in the TI Litigation. See EX2022 58.

3. “integrated circuit” (claims 1-3, 6, 7, 9, and 10)

In both the Qualcomm Litigation and Samsung Litigation, the parties agreed that the term “integrated circuit” should be construed as “interconnected circuitry on a chip.” EX2052, 2; EX2033, Appendix 1, pp. 1-2 (pp. 5-6). The district court in the TI Litigation construed “integrated circuit” as “a combination of interconnected

circuit elements inseparably associated on or within a continuous substrate.”

EX2022, 59.

VII. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION PURSUANT TO 35 U.S.C. § 314(A) IN VIEW OF THE PARALLEL DISTRICT COURT PROCEEDING

A. The Board Has Discretion to Deny Institution

The Board is granted the discretion to decline to institute *inter partes* review whenever it deems the circumstances warrant doing so. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“the PTO is permitted, but never compelled, to institute an IPR proceeding”); *see also* 35 U.S.C. § 314(a); *Oil States Energy Servs. LLC v. Green’s Energy Grp., LLC*, 138 S. Ct. 1365, 1371 (2018) (“The decision whether to institute *inter partes* review is committed to the Director’s discretion.”). The Board has declined to institute in cases where a parallel district court trial would determine the issues *before* the requested Board trial, rendering the review cumulative.

The Board considers the following set of six nonexclusive factors to determine on a case-by-case basis whether to deny institution based on a parallel proceeding:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;

3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, dated June 21, 2022 (available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf) (“Interim Guidance”); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5-6 (Mar. 20, 2020) (precedential) (hereinafter, “*Fintiv*”); *see also Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 (PTAB May 13, 2020) (informative) (applying the *Fintiv* factors and denying institution) (hereinafter, “*Fintiv II*”).

Where *Fintiv* factors 1-5 favor discretionary denial, a Petitioner must meet a higher standard for institution; they must present a compelling, meritorious, challenge to the patentability of at least one claim. *CommScope Technologies, LLC v. Dali Wireless Inc.*, IPR2022-01242, Paper 23 at 4-5 (Feb. 27, 2023) (“In circumstances where, however, the Board's analysis of *Fintiv* factors 1–5 favors denial of institution, the Board shall then assess compelling merits.”), *OpenSky*

Indus., LLC v. VLSI Tech. LLC, IPR2021-01064, Paper 102, 49 (PTAB Oct. 4, 2022)

("[A] compelling-merits challenge is a higher standard than the reasonable likelihood required for the institution of an IPR under 35 U.S.C. § 314(a).") A "[c]ompelling, meritorious challenges are those in which the evidence, if unrebutted at trial, would plainly lead to a conclusion that one or more claims are unpatentable by a preponderance of the evidence." *Id.*, p. 50. "A challenge can only 'plainly lead to a conclusion that one or more claims are unpatentable' if it is highly likely that the petitioner would prevail with respect to at least one challenged claim." *Id.*, p. 50. For the reasons discussed above, Petitioner has not presented a compelling challenge to the patentability of at least one claim. *Supra*, §VI-VII.

Patent Owner respectfully asserts that the Interim Guidelines are improper because the *Fintiv* instructions were issued in violation of the notice-and-comment rulemaking set forth in 5 U.S.C. § 553(b). Under the APA, the Director may adopt substantive rules only through notice-and-comment rulemaking. *See* 5 U.S.C. § 553. In particular, Patent Owner respectfully submits that the Interim Guidelines statement that a *Sotera* stipulation alone (factor 4) is sufficient for discretionary denial is improper and inconsistent with the statute. *See* Interim Guidelines, pp. 7-8. Patent Owner also respectfully submits that the compelling evidence standard (factor 6) is also improper and inconsistent with the statute. *See* Interim Guidelines, pp. 3-5.

The legality of the Interim Guidelines is currently being challenged in *Apple Inc. v. Iancu*, No. 5:20-cv-06128-EJD (N.D. Cal.). The Federal Circuit has remanded the case to the district court to review the specific issue of whether the Interim Guidelines were issued without compliance with notice-and-comment rulemaking requirements under the APA. The parties in that case are currently awaiting the district court's opinion on cross-motions for summary judgment, which is expected to address the merits of this remaining challenge to the Interim Guidelines. If the district court finds that Interim Guidelines were issued in violation of the APA's notice-and-comment procedures, it could invalidate or limit the application of the Interim Guidelines in these IPR proceedings.

In light of these concerns and the ongoing *Apple Inc. v. Iancu* case, Patent Owner respectfully requests that the Board refrain from relying on the Interim Guidelines in its decision on whether to institute IPR in this case. Instead, Patent Owner respectfully submits the Board should focus its analysis on the statutory requirements for institution set forth in 35 U.S.C. § 314. Nevertheless, should the Board choose to apply the Interim Guidelines, Patent Owner maintains that the factors outlined in the rule favor denying institution in this case.

B. Parallel District Court Proceedings Will Determine the Issues Raised in the Petition Before the Board

Contrary to the Petitioners' assertions that the district court proceedings are relatively early (Petition, 83), they are currently at a relatively advanced stage.

Claim 10 of the '2893 patent is currently asserted in co-pending litigation between Patent Owner and Petitioner Qualcomm in Federal District Court in the parallel Qualcomm litigation. EX2038, 37-38. The case was initiated on December 19, 2022. EX2037, 103. Infringement contentions were served May 26, 2023; Invalidity contentions were served September 22, 2023; and, the *Markman* hearing was held on December 21, 2023. EX2039, 2-3, 6. The Court's claim construction order is imminent. Fact discovery will be nearly complete by the time for entry of the Institution Decision. *Id.*, 6. Expert discovery will be complete by October 18, 2024. *Id.*, 7. All dispositive motions will be filed by November 18, 2024. *Id.*, 7. Although no trial date is determined yet, the trial is expected to be completed nearly two months before a final written decision. *Id.*, 8; EX2012, 35.

Claims 1 and 10 of the '2893 patent are currently asserted in co-pending litigation between Patent Owner and the Petitioner Samsung in Federal District Court in the parallel Samsung litigation. EX2027, 25-26. The case was initiated on December 19, 2022. *Id.*, 103. Infringement contentions were served May 16, 2023; invalidity contentions were served July 7, 2023; and, Markman briefing has been complete with the Markman hearing scheduled April 9, 2024, less than two weeks after the deadline for filing this preliminary response. EX2028, 3. Expert discovery will be nearly complete by the time for entry of the Institution Decision. *Id.*, 3. Additionally, dispositive motions will be fully briefed by August 5, 2024. *Id.*, 1.

Trial is currently scheduled for October 28, 2024 for the Samsung Litigation, which will pre-date the Board's final written decision by nearly eight months. Petition, 83. EX2028, 1. EX2012, 37. The Petitioners argue, without any evidence or basis, that the trial date is not set in stone and could easily change. *Id.* Indeed, the federal trial statistics for the Eastern District of Texas confirm that the time to trial for the Samsung Litigation will pre-date the Board's final written decision by nearly eight months. Interim Guidance, 2, 8-9; EX2012, 35. The federal trial statistics for the Western District of Texas confirm that the time to trial for the Qualcomm litigation will pre-date the Board's final written decision by nearly two months. EX2012, 37.

C. The First Factor is Neutral

The first *Fintiv* factor is at least neutral because the Petitioners have not requested a stay. *Fintiv II*, Paper 15 at 12 (determining that Factor 1 is neutral when neither party has requested a stay and the issue has not been addressed in the case by the district court.) Further, the Petitioners do not indicate that they would seek a stay if the Petition was instituted. Petition, 82-83.

D. The Second Factor Favors Denial

In this case, the Board will decide whether to institute an IPR on or before June 28, 2024 and its final written decision will be due around June 28, 2025. 35 U.S.C. § 314(b). However, the Samsung Litigation trial will be complete around

November 4, 2024, more than seven months in advance of a final written decision.

EX2028, 1. The Qualcomm Litigation trial is expected to be complete months before a final written decision based on the current scheduling. EX2039, 8. Further, the median time to trial in the Eastern District of Texas for similar cases is 21.4 months. EX2012, 35. The median time to trial in the Western District of Texas for similar cases is 28.3 months. EX2012, 37. This timeline is consistent with the governing Scheduling Orders. There is no reason for the Board to hold proceedings that would duplicate those in the district court and that would take longer to complete. The Board's scarce resources should be deployed instead where they can increase efficiency and provide the faster alternative proceeding contemplated by the AIA.

The Board's precedential decision in *NHK Spring* recognized that the Board can and should deny institution in its discretion under Section 314(a) when, as here, earlier completion of parallel district court litigation of the same issues would moot the “objective of the AIA . . . to provide an effective and efficient alternative to district court litigation.” See, e.g., *NHK Spring Co., Ltd. v. Intri-Plex Technologies, Inc.*, IPR2018-00752, slip op. at 20 (PTAB Sept. 12, 2018) (Paper 8) (Precedential) (quotations omitted).

In *NHK Spring*, the Board denied institution in part because of the duplicative nature and the advanced stage of a parallel district court proceeding. IPR2018-00752, Paper 8 at 19-20 (explaining that “the advanced state of [a] district court

proceeding is an additional factor that weighs in favor of denying the Petition under §314(a).”). The *NHK Spring* petitioner “assert[ed] the same prior art and arguments” in a parallel district court proceeding, which was “nearing its final stages” and was scheduled to complete a jury trial about five to six months before a final written decision from the Board would have been due. *Id.* The district court and the Board were also applying the same claim construction standard. *Id.*, 6-7. The Board explained that “instituting a trial under the facts and circumstances ...would be an inefficient use of Board resources,” and would not be consistent with “an objective of the AIA ...to provide an effective and efficient alternative to district court litigation.” *Id.*, 20.

Additionally, in *E-One, Inc. v. Oshkosh Corp.*, the Board observed the same factual circumstances as were present in *NHK Spring*, and denied institution. IPR2019-00161, Paper 16 at 4, 6-9 (PTAB May 15, 2019). The Board looked at whether “a district court proceeding involving the same patent was scheduled to go to trial before a final decision would have been due in the Board proceeding, and the Board proceeding would involve the same claim construction standard, the same prior art references, and the same arguments as in the district court.” *Id.*, 6.

Just as in *NHK Spring* and *E-One*, the parallel district court proceeding here (i) is between the same parties, (ii) will apply the same claim construction standard, (iii) is currently considering the same or significantly overlapping claim construction

issues and invalidity challenges, and (iv) will likely go to trial months before the Board's statutory deadline.

Under these facts and circumstances, which were also present and were dispositive in *NHK Spring* and *E-One*, institution of a duplicative parallel (and trailing) *inter partes* review proceeding would be an inefficient and wasteful use of the Board's limited resources. As in those cases, the Board should deny institution in its discretion under Section 314(a). This will allow the identical art and arguments to continue to be litigated and determined in district court, where substantial resources have already been expended and the district court stands ready to decide the issues urged here. Institution of an *inter partes* review here cannot provide the "effective and efficient alternative to district court litigation" contemplated by the AIA. *NHK Spring*, IPR2018-00752, Paper 8 at 20.

E. The Third Factor Favors Denial

The third factor concerns "the amount and type of work already completed in the parallel litigation by the court and the parties and the time of the institution decision." *Fintiv*, Paper 11 at 9. The focus of this factor is on "the actual investment by the district court and the parties" "at the time [the PTAB] decide[s] whether to institute this proceeding." *Dolby Labs., Inc. v. Intertrust Techs. Corp.*, IPR2020-01106, Paper 12 at 14 (PTAB Jan. 5, 2021). Petitioners address only the work performed as of the filing of the Petition. Petitioners do not address the investment

by the District Court and the parties by the time the Board issues its institution decision. As discussed above, a significant investment in the district court proceedings has already taken place. *Supra*, §VII.B.

The third *Fintiv* factor also considers the Petitioner's diligence: if "the petitioner did not file the petition expeditiously, such as at or around the same time that the patent owner responds to the petitioner's invalidity contentions, or even if the petitioner cannot explain the delay in filing its petition, these facts have favored denial." *Fintiv*, Paper 11 at 11-12. The Petitioners do not explain why they waited one year after the Samsung Litigation and Qualcomm Litigation were initiated to file the Petition. Petition, 77-79; *Cisco Sys., Inc. v. Estech Sys., Inc.*, IPR2021-00329, Paper 13 at 11 (PTAB July 6, 2021) (8-month delay between complaint and IPR petition favored denial). Nor do the Petitioners explain why they waited more than 5 months after serving initial invalidity contentions in the Samsung Litigation and 3 months after serving initial invalidity contentions in the Qualcomm Litigation to file the Petition. *Id.*

The Court is expected to issue its claim construction order imminently in the Qualcomm Litigation. EX2039, 6. The Court has scheduled its *Markman* hearing in the Samsung Litigation for April 9, 2024, which is prior to the Board's deadline for issuing the institution decision. EX2028, 3. There will thus be significant investment

in the parallel proceedings by the Court and the parties before the institution decision deadline.

Further, the Scheduling Orders demonstrate that trial of the Samsung Litigation will be eight months and the trial of the Qualcomm Litigation will likely be at least two months in advance of the final written decision statutory deadline. EX2028, 1; EX2039, 8; EX2012, 35, 37. An enormous amount of resources will have been invested in the parallel litigations before the Board issues a final written decision.

Thus, this factor favors denial.

F. The Fourth Factor Should Favor Denial or Only Marginally Favors Institution

The “concerns of inefficiency and the possibility of conflicting decisions [are] particularly strong” where a petition “includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding.” *Fintiv* at 12. Here, the Petition includes substantially the same claims, arguments, and evidence as has been presented in the district court litigations. Claims 1, 10 of the '2893 Patent have been asserted in the Samsung Litigation. EX2027, 25-26. Claim 10 of the '2893 Patent has been asserted in the Qualcomm Litigation. EX2038, 37-38. Claims 1-3 and 6-10 have been raised in the Petition. Petition, 3-4. Petitioner Samsung's initial invalidity contentions allege invalidity on the basis of at least Bertozzi which is also relied on as the main reference in this petition for the

grounds 1, 2, and 4. EX2050, *see e.g.*, pp. 56-60. Petitioner Qualcomm's initial invalidity contentions allege invalidity on the basis of at least Bertozzi which is also relied on as the main reference in this petition for the grounds 1, 2, and 4, and Jantsch and Duato, which are also relied on as the references in this petition for the grounds 2 and 4. EX2051, *see e.g.*, pp. 16, 81-86. In fact, Petitioner submitted claim charts for those references in its district court invalidity contentions that duplicate the substance of the Petition. EX2053; EX2054. Substantially the same art and arguments were raised and are being litigated in the district court. This weighs in favor of denying the Petition.

Although the Petitioners purport to stipulate that it will not pursue the specific grounds raised in the Petition or could have been reasonably raised if Institution is granted, the Petitioners have not filed the stipulation or otherwise formalized the stipulation. Petition, 82. Further, in the Samsung Litigation, opening expert reports are due June 3, 2024, prior to the deadline for the Board's Institution Decision, and rebuttal expert reports are due July 1, 2024, days after that deadline. EX2028, 3. Similarly, in the Qualcomm Litigation, all fact discovery will be complete by July 11, 2024, and opening expert reports are due August 9, 2024, days after the Board's Institution Decision. EX2039, 6-7. That is, the parties will have expended significant resources in the District Court Litigations on substantially similar

invalidity arguments before the stipulation becomes effective. This reduces the benefit of the so-called *Sotera* stipulation and increases inefficiency.

G. The Fifth Factor Favors Denial

Both the Petitioners and Patent Owner are parties to the parallel district court litigations, which further weighs against institution. *Fintiv*, Paper 11 at 13-14.

H. The Sixth Factor Favors Denial

Fintiv factors 1-5 favor discretionary denial or remain neutral. Many of the issues in the Petition (or substantially the same issues) will be decided in the district court litigations and these issues will likely be decided prior to the time a final written decision would be rendered. The Petitioners have not demonstrated a substantial likelihood of success as to any challenged claim and has not met its statutory burden for institution. The Petitioners have therefore not presented compelling evidence of unpatentability. The Petition should therefore be discretionarily denied. *CommScope Technologies, LLC*, IPR2022-01242, Paper No. 23, p. 4-5. In these circumstances, efficiency and the integrity of the system are best served by denying institution. *Fintiv*, Paper 11 at 6.

VIII. PETITIONERS HAVE NOT ESTABLISHED ANY CLAIM IS UNPATENTABLE

For the reasons set forth below, the Board should deny institution because Petitioners have not met their burden of showing that any claim of the '2893 Patent is unpatentable.

A. Ground 1: Purported Anticipation by Bertozzi (Claims 1-3, 6-7, and 10)

In Ground 1, Petitioners allege that claims 1-3, 6-7, and 10 are anticipated by Bertozzi. *See* Petition, 10-36.

1. Bertozzi Fails to Anticipate Claim 10

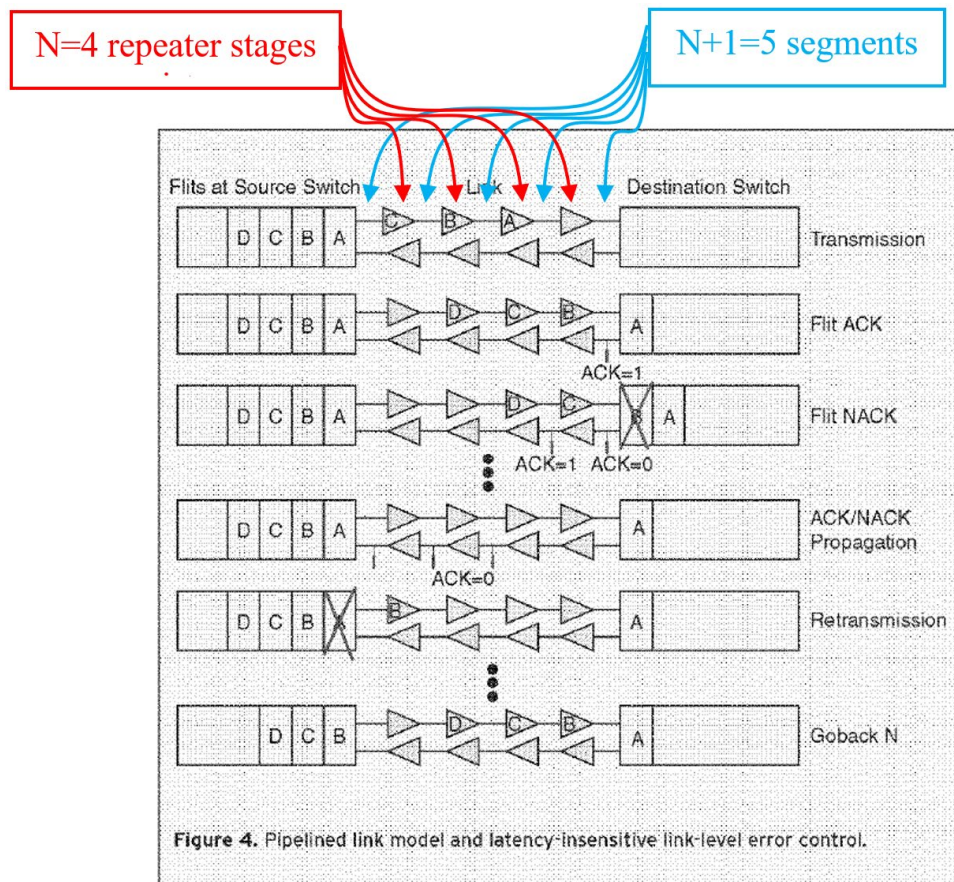
Claim 10 of the '2893 Patent claims a method of designing an integrated circuit that includes inserting a quantity of data storage elements ($M*N$) that is based on a specific quantity of data elements (N) in a data package. The quantity of data storage elements ($M*N$) is a function of the quantity of data elements (N). *See* EX2001, ¶89; EX1001, claim 10, 12:22–42.

Petitioners contend that Bertozzi discloses this limitation. Petition, 24-27. Petitioners rely primarily on Figure 4 of Bertozzi and paragraphs 135-142 of Dr. Mowry's declaration. Petitioners' argument fails. EX2001, ¶¶89-100. Bertozzi does not disclose this limitation. *Id.*

Bertozzi focuses on overcoming an interconnect-delay problem by pipelining interconnects and segmenting wires into lengths based on desired clock frequencies, not on the quantity of data elements in a data package. EX1005, 24; EX2001, ¶90. In Bertozzi, the insertion of repeaters is to partition links into segments or pipeline stages based on timing requirements rather than the data elements' quantity in a data package. *Id.* This fundamental distinction underscores that Bertozzi does not disclose the insertion quantity of ($M*N$) data storage elements is based on (or

correlates with) the data elements' quantity (N) in a data package, a critical aspect of Claim 10. EX2001, ¶¶89-100.

FIG. 4 of Bertozzi (reproduced below and annotated in color) illustrates an example of inserting four pipeline registers (i.e., repeater stages) into a link. EX2001, ¶90.



EX1005, FIG. 4

The four registers partition the link into five segments (the integration of N repeater stages within a link results in the partitioning of the link into N+1 segments). EX2001, ¶90; *see also* EX1005, 25 (“an ACK is propagated back to the source, and after N clock cycles (where N is the link length expressed in terms of number of

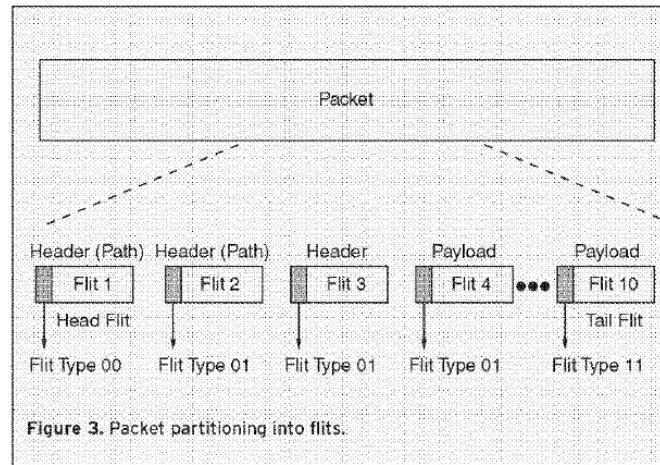
repeater stages)”); *see also* EX1005, 26 (“the flit has to propagate across the link (N cycles), . . . the ACK/NACK signal has to be propagated back (N cycles)”)

The Petition and Dr. Hassoun rely on this figure; however, the Petition and Dr. Hassoun mischaracterize it. *See, e.g.*, Petition, 25-26 (“In Figure 4, Bertozzi discloses inserting 8 repeaters (M*N data storage elements, where M=2, and N=4) into a link”); EX2001, ¶¶91-93. FIG. 4 of Bertozzi illustrates “[a] solution to the interconnect-delay problem consist[ing] of pipelining interconnects” where “*multiple outstanding flits* propagate across the link.” EX1005, 24 (emphasis added); EX2001, ¶93. FIG. 4 of Bertozzi illustrates N=4 repeater stages on the link from the source switch to the destination switch and N=4 repeater stages on the link from the destination switch to the source switch. *See* EX1005, 25-26; EX2001, ¶93. Bertozzi describes “a solution to overcome the interconnect-delay problem consists of pipelining interconnects [34, 35]. Wires can be partitioned into segments (or relay stations, which have a function similar to the one of latches in a pipelined datapath) whose length satisfies pre-defined timing requirements.” EX1005, 24 (brackets in original); EX2001, ¶98. Bertozzi explains that “[b]ased on the clock speed target and link routing, the number of pipeline stages for each link is also determined.” EX1005, 29; EX2001, ¶91. Bertozzi further explains that “[s]witch-to-switch links are subdivided into basic segments whose length can be tailored to the desired clock

frequency that needs to be achieved in the design.” EX1005, 24; EX2001, ¶91. A POSITA would understand that Bertozzi discloses that the quantity of repeater stages inserted onto a link is a function of (or correlates with) a desired length of each segment. EX2001, ¶91. Bertozzi does not disclose or suggest that the quantity of repeater stages (e.g., data storage elements) inserted onto a link (e.g., channel) is a function of (or correlates with) the quantity of flits (e.g., data elements) in a packet (e.g., data package). EX2001, ¶91.

The Petition conclusively and erroneously states that “a POSA would in any event at once envisage that the example of the fixed-length packets taught by Bertozzi corresponds to a data package having four flits A, B, C, D (each one a data element) as shown in Figure 4.” Petition at 19. That statement is unsupported by the disclosure in Bertozzi. EX2001, ¶92.

Bertozzi does not disclose or suggest that the multiple outstanding flits shown in FIG. 4 are indeed included a single packet comprising 4 flits. EX2001, ¶94. For example, the outstanding four flits may constitute a portion of a single packet, such as four flits from the 10-flit packet illustrated in FIG. 3 of Bertozzi (reproduced below), where only four flits have been illustrated for simplicity. EX2001, ¶94.



EX1005, FIG. 3

FIG. 3 of Bertozzi is the only place in Bertozzi that depicts a complete packet, and it consists of three header flits, six payload flits, and one tail flit (which is also considered a payload flit). EX2001, ¶94 Dr. Hassoun opines “[a] POSA would understand that this [FIG. 3] is a general illustration of the partitioning procedure of a packet.” EX1003, ¶121, n. 3. Bertozzi’s Figure 3 confirms that the flits in FIG. 4 are not the complete packet. Based on the “general illustration of the partitioning procedure” shown in Figure 3, a four-flit packet would consist of three header flits and one tail flit. EX2001, ¶ 94. A POSITA would understand that this would be a rather useless packet with practically no payload, and therefore Dr. Hassoun’s interpretation is highly unlikely. EX2001, ¶94. Alternatively, the outstanding four flits may belong to multiple packets, such as the last two flits of an earlier packet and the first two flits of a later packet. In fact, Bertozzi refers to the flits in FIG. 4 simply as “[m]ultiple outstanding flits.” EX1005, 25; EX2001, ¶94.

Bertozzi simply does not disclose or suggest any correlation between the number of repeater stages depicted in FIG. 4 and the number of flits illustrated in the same figure. EX2001, ¶95. Furthermore, it does not suggest that the number of repeater stages integrated into a link is determined by the number of flits contained within a packet as required by the claim 10 of the '2893 Patent. EX2001, ¶95.

Therefore, Bertozzi does not disclose or suggest “in response to the identifying act, **inserting $M*N$ data storage elements** into the data communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel” (emphasis added), where the preamble recites “**each data package compris[es] N data elements,**” as required by claim 10 (emphasis added). EX2001, ¶96.

Moreover, the purpose behind why the quantity ($M*N$) of data storage elements is a function of the quantity of data elements (N) in a data package in claim 10 is to ensure that network stations receive routing information within predefined evaluation cycles, a specificity not addressed or contemplated by Bertozzi. EX2001, ¶97. The '2893 Patent recites that “[s]ince a network station expects routing information to arrive periodically (i.e. after every N cycles), the introduction of a delay on the first communication channel (which typically is the slowest channel of the network) matching such a period.” *See* EX1001, 6:51–53; *see also id.*, 6:51–53 (“it is essential that the headers of the data packages do not arrive at any data router

110, 120, 130, 140 outside such an evaluation clock cycle.”); *see also id.*, 7:31–34 (“This ensures that the correct phase relation between clock cycle and routing information evaluation is maintained throughout the whole data communication network 100.”) EX2001, ¶97.

However, Bertozzi discloses that the switches utilized in Xpipes must operate correctly *regardless* of the quantity of repeater stages on a link. EX1005, 24 (“A solution to overcome the interconnect-delay problem consists of pipelining interconnects [34, 35]. . . . This requires the system to be composed of modules whose behavior does not depend on the latency of input communication channels [34].” (brackets in original); EX1005, 25 (“Switch operation is latency insensitive, in that correct operation is guaranteed for arbitrary link pipeline depth.”). EX2001, ¶98; *see also* EX2011 (cited by EX1005), 1065 (“[T]he latency-insensitive design methodology is to be able to ‘pipeline’ a communication channel by inserting an arbitrary amount of memory elements. In the framework of our theory, this operation corresponds to adding some particular processes, called relay stations, to the given system.”). Bertozzi’s approach, which allows for the operation of switches irrespective of the number of repeater stages and emphasizes latency insensitivity, diverges from the ’2893 Patent’s goal of aligning data package delivery with routing information evaluation cycles. EX2001, ¶98. This distinction demonstrates that

Bertozzi's disclosures neither anticipate nor render obvious the invention claimed in the '2893 Patent. *Id.*

Accordingly, the solution disclosed by Bertozzi teaches away from this routing-periodicity requirement described in the '2893 Patent by elaborating that the switches *must* operate correctly for *any arbitrary quantity of repeater stages on a link*, i.e., for routing information that arrives at a destination switch in any cycle rather than in only predefined evaluation cycles. EX1005, 24; EX2001, ¶98. A reference teaches away where a POSITA “would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.” *Arctic Cat Inc. v. Bombardier Recreational Prod. Inc.*, 876 F.3d 1350, 1360 (Fed. Cir. 2017) (quoting *Allergan, Inc. v. Sandoz Inc.*, 796 F.3d 1293, 1305 (Fed. Cir. 2015)).

For at least these additional reasons, Bertozzi does not disclose or suggest “in response to the identifying act, **inserting M*N data storage elements** into the data communication network, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel” (emphasis added), where the preamble recites “**each data package compris[es] N data elements**,” as required by claim 10 (emphasis added). EX2001, ¶100.

2. Bertozzi Fails to Anticipate Claim 1

The Petition alleges that Bertozzi discloses at least the limitation “the data communication introducing a delay of $M*N$ cycles on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold” of claim 1 for the same reasons as independent claim 10. *See* Petition, 28-34. Thus, Petitioners’ analysis of Claim 1 fails for the same reasons as Claim 10. EX2001, ¶101.

3. Bertozzi Fails to Anticipate Claim 7

The Petition alleges that Bertozzi discloses at least limitation “the data communication network further comprising $M*N$ data storage elements, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel” for the same reasons as independent claim 10. *See* Petition, 28-34. Thus, Petitioners’ analysis of claim 7 fails for the same reasons as independent Claim 10. EX2001, ¶102.

4. Bertozzi Fails to Anticipate the Dependent Claims

The dependent claims are not anticipated by Bertozzi for at least the same reasons that the independent claims from which they depend are not anticipated by Bertozzi.

B. Ground 2: Purported Obviousness over Bertozzi Alone or in View of Jantsch or Duato (Claims 1–3, 6–7, and 10)

In Ground 2, Petitioners allege that claims 1–3, 6–7, and 10 are rendered obvious over Bertozzi alone or in view of Jantsch or Duato. *See* Petition, 37-47.

In Ground 2, the Petition argues that Bertozzi, Jantsch, and Duato render limitation “in response to the identifying act, inserting $M \times N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel” (where the preamble recites “each data package compris[es] N data elements”) obvious for the same reasons discussed in Ground 1. *See* Petition, 38-41. Thus, Bertozzi alone or in view of Jantsch or Duato fail to render obvious independent Claim 1 for at least the same reasons as independent Claim 10. EX2001, ¶104.

A POSITA would not modify Bertozzi or combine Bertozzi with Jantsch and Duato because Bertozzi teaches away from the modification and/or combination. EX2001, ¶105. A reference teaches away where a POSITA “would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.” *Arctic Cat Inc. v. Bombardier Recreational Prod. Inc.*, 876 F.3d 1350, 1360 (Fed. Cir. 2017) (quoting *Allergan, Inc. v. Sandoz Inc.*, 796 F.3d 1293, 1305 (Fed. Cir. 2015)). “[E]ven if a reference is not found to teach away, its statements regarding preferences are relevant to a finding regarding whether a skilled artisan would be motivated to

combine that reference with another reference.” *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 (Fed. Cir. 2018).

Petitioners rely on paragraph 180 of Dr. Hassoun's Declaration to support its obviousness theory. Petition, 40. Paragraph 180 states that “it was well-known that synchronization of certain networks and types of communications require packets to arrive at network stations ‘at precisely scheduled time slots’,” and provides seven pages of inapposite discussion about such synchronization. EX2001, ¶105. As I discussed above, Bertozzi states that the switches utilized in Xpipes must operate correctly for data packets arriving at any time slot, not just for precisely scheduled time slots. EX2001, ¶105; EX1005, 24 (“A solution to overcome the interconnect-delay problem consists of pipelining interconnects [34, 35]. . . . This requires the system to be composed of modules whose behavior does not depend on the latency of input communication channels [34].” (brackets in original) (citing Carloni, EX2011); EX1007, 25 (“Switch operation is latency insensitive, in that correct operation is guaranteed for arbitrary link pipeline depth.”); *see also* EX2011, 1065 (“[T]he latency-insensitive design methodology is to be able to ‘pipeline’ a communication channel by inserting an arbitrary amount of memory elements. In the framework of our theory, this operation corresponds to adding some particular processes, called relay stations, to the given system.”). A POSITA would therefore understand that the solution disclosed by Bertozzi is not merely silent about ensuring

that packets arrive at switches at precisely scheduled time slots, e.g., that the switches receive routing information of only during predefined evaluation cycles, but Bertozzi explicitly teaches away from this because the switches must operate correctly for any arbitrary quantity of repeater stages on a link, i.e., for routing information that arrives at a destination switch in any cycle rather than in only predefined evaluation cycles. EX2001, ¶105.

Several Federal Circuit decisions are instructive as to why Bertozzi's teaching away is fatal to Petitioners' proposed combination. For example, in *Merck Sharp & Dohme B.V. v. Warner Chilcott Co., LLC*, the Federal Circuit held that the challenged claims were non-obvious "[b]ecause [the primary reference] criticizes the use of one compartment to deliver both compounds, the person of ordinary skill would not be motivated to modify [the primary reference] to make a one-compartment ring." 711 F. App'x 633, 637 (Fed. Cir. 2017). In *Trivascular, Inc. v. Samuels*, the Federal Circuit found that it would not be obvious "to substitute the recessed barbs of [the primary reference] with the protuberances of [the secondary reference], since TriVascular's proposed substitution would destroy the basic objective of the [invention]." 812 F.3d 1056, 1068 (Fed. Cir. 2016); *see also Application of Ratti*, 270 F.2d 810, 813 (CCPA 1959) (no motivation to combine because combination "would require a substantial reconstruction and redesign of the

elements shown in [the prior art reference] as well as a change in the basic principles under which [that reference's] construction was designed to operate”).

C. Ground 3: Purported Obviousness over Dielissen in View of Hassoun (Claims 1–3, 6, 7, 9 and 10)

In Ground 3, Petitioners allege that claims 1–3, 6, 7, 9 and 10 are rendered obvious over Dielissen in view of Hassoun. *See* Petition, 47-77.

1. Dielissen in View of Hassoun Fails to Render Obvious Claim 10

a. The Combination Fails to Disclose “in response to the identifying act, inserting $M \times N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel”

Petitioners acknowledge that Dielissen does not disclose “identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold” and “in response to the identifying act, inserting $M \times N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel,” where the preamble recites “each data package compris[es] N data elements” as recited in claim 10 of the '2893 Patent. EX1001, Claim 10, 12:22–42. Petition, 61. Instead, Petitioners turn to Hassoun for these limitations. However, no combination of Hassoun, Dielissen, or any other reference discloses or suggests this claim limitation. EX2001, ¶¶107-114.

First, Dielissen is silent about the claim element “identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold” recited in independent Claim 10. Dielissen describes some aspects of the Æthereal NoC. EX2001, ¶108; EX1007 (Dielissen) at 1 (“[W]e present the Æthereal NoC.”). Dielissen states that “[f]or the current Æthereal network, the flit size is chosen [to be] 3 to optimize the data clock frequency and control frequency.” EX1007, 2. Dielissen’s FIG. 4 (reproduced below) shows this example data packet. EX2001, ¶108.

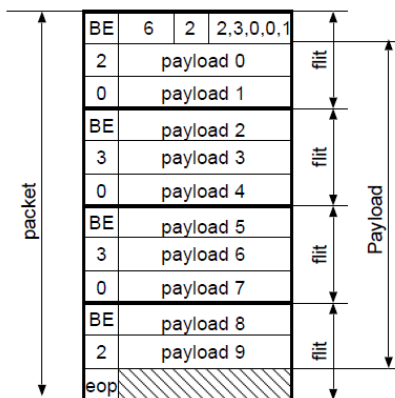


Figure 4. BE-packet example

Dielissen is also silent about “long wires, global wires, channel delays, channels having transfers delay exceeding predefined delay threshold, or an insertion or even existence of any data storage elements (e.g., pipeline registers, pipeline stages, repeaters, repeater stages, etc.) in the network to introduce a delay on a channel.” EX2001, ¶107. Dielissen does not disclose or suggest any need or desire to find a path with the minimum delay, at least because the selection of a flit

size of three had already optimized the data and control frequencies for the Æthereal NoC. Dielissen at 2 (“For the current Æthereal network, the flit size is chosen [to be] 3 to optimize the data clock frequency and control frequency.”). EX2001, ¶108.

Second, Hassoun discloses an algorithm designed to locate a registered buffered routing path with the minimum delay from source to sink. EX2001, ¶109; *see* EX1011, 247 (“The actual ‘Fast Path’ algorithm finds a minimum delay path for a net while simultaneously exploring all buffering and routing solutions.”); *see also* EX1011, 248 (“The Fast Path algorithm finds the minimum delay source-to-sink buffered routing path.”). Hassoun discloses “extend[ing] the [Fast Path] algorithm to handle additional synchronization elements such as registers, relay stations, and MCFIFOs” on the path. EX1011, 247; EX2001, ¶109. Illustrations of the Fast Path and Registered Buffered Path algorithms are depicted in Figures 1 and 4 of Hassoun below, respectively, annotated in red. EX2001, ¶109.

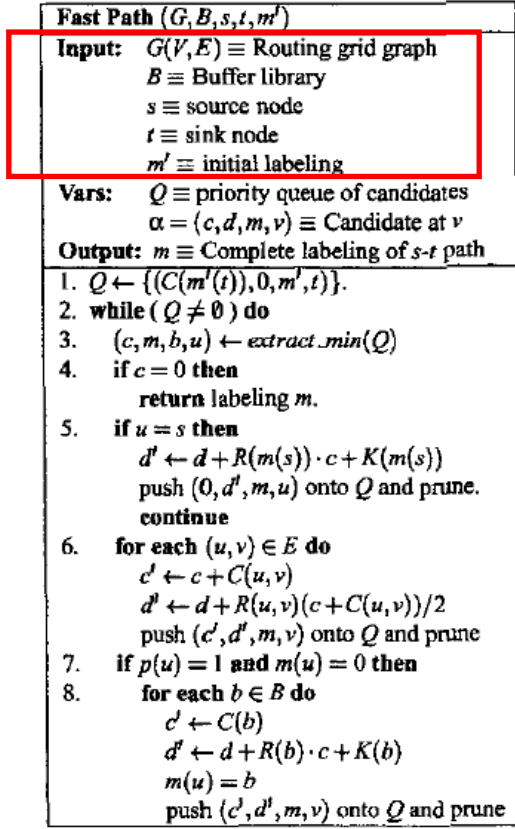


Figure 1. The Fast Path algorithm.

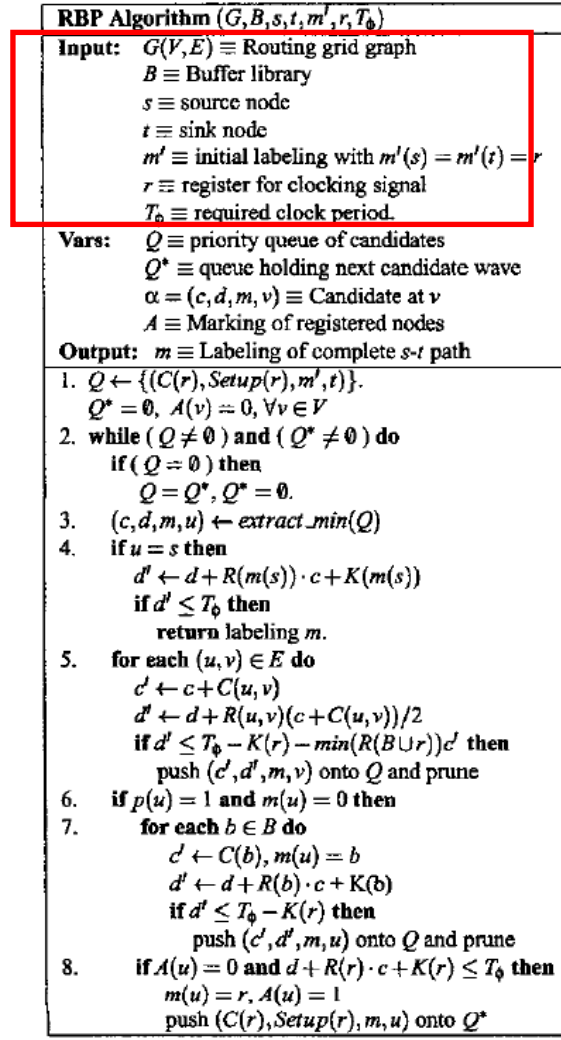


Figure 4. The Registered Buffered Path algorithm.

EX1011, Figures 1 and 4

The inputs for the Fast Path algorithm, as shown in Figure 1 and highlighted in red, consist of a routing grid path $G(V, E)$, a buffer library B , a source node s , a sink node t , and an initial labeling m' . EX2001, ¶110; EX1011, Figure 1. The Registered Buffered Path algorithm, depicted in Figure 4 and also highlighted in red, takes the same inputs as the Fast Path algorithm but adds registers r and a required clock period T_ϕ . EX2001, ¶110; EX1011, Figure 4. Notably absent from both

algorithms, particularly the Registered Buffered Path algorithm, is “any indication or suggestion that a size or length of a data packet it utilized as an input (e.g., any information indicating that a data package comprises N data elements).” EX2001, ¶110. This omission is due to the fact that neither algorithm accounts for the size or length of data packets. EX2001, ¶110. Indeed, the only changes made to the Fast Path algorithm to create the Registered Buffered Path algorithm consists only of the registers and a required clock period. *Id.*

Contrary to the Petitioners' allegation that “the obvious combination of Dielissen's integrated circuit designed for data packages with three data elements (N=3) with Hassoun's teaching of identifying a data transfer delay exceeding a predetermined delay threshold and then inserting three data storage elements in a communication link,” Hassoun FIG. 2 simply discloses an example routing that is arbitrarily illustrated with some quantity (three) of registers. EX2001, ¶111; Petition, 65. FIG. 2 of Hassoun “shows an example of a buffered-register path on a grid graph,” which is reproduced below and annotated in red. EX1011, 249; EX2001, ¶111.

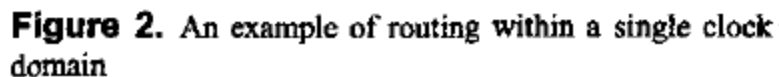


Figure 2 depicts three registers (annotated in red) on the path from source *s* to sink *t*. EX2001, ¶111. However, Hassoun is silent as to the rationale behind choosing the three registers in this example. EX2001, ¶111. Moreover, since both the Fast Path and the Registered Buffered Path algorithms do not take into account the size or length of data packets, there is no basis for a POSITA to infer any relationship between the number of three registers depicted in Hassoun's Figure 2 and the number of flits within a data packet, contrary to the Petition suggests. Petition, 65; EX2001, ¶¶111-112. The arbitrary number of registers shown in Hassoun's Figure 2 lacks any concrete association with the flits or words disclosed in Dielissen's data packet. EX2001, ¶112. Furthermore, Petitioners have not presented any rationale or evidence to establish a linkage between these disparate elements. EX2001, ¶112.

Thus, Diellisen in view of Hassoun fails to teach or suggest “in response to the identifying act, inserting $M*N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel” (emphasis added), where the preamble recites “each data package compris[es] N data elements,” as required by claim 10. EX2001, ¶114.

b. A POSITA Would Not Combine Dielissen and Hassoun

Further, there is no motivation to combine Dielissen and Hassoun, or any other reference cited by the Petition. EX2001, ¶113. Petitioners have failed to show that a POSITA would have had a reasonable expectation that the combination of Dielissen and Hassoun would have succeeded. *Id.* The Petition indicates that Dielissen does not disclose at least inserting $M*N$ data storage elements into the network (where N is the quantity of data elements in a data package) and that relies on Hassoun for (at least) this limitation. *Id.* However, as discussed above, neither the Fast Path algorithm nor the Registered Buffered Path algorithm disclosed by Hassoun takes into account the packet or flit length when calculating their outputs (the alleged $M*N$ data storage elements), which are critical for establishing a minimum-delay path. *Id.*

Consequently, any modification of Dielissen to include Hassoun's teachings cannot succeed because Hassoun's Fast Path algorithm or Registered Buffered Path algorithm do not produce their outputs (the alleged $M*N$ data storage elements)

according to a packet length or a flit length (the alleged N data elements of a data package). EX2001, ¶113.

A POSITA would not combine Dielissen and Hassoun as set forth in the petition. EX2001, ¶¶39-68, 113-116. NoCs were developed due to the drawbacks of buses and crossbars. EX2001, ¶55. NoC technology packetizes address and data information on the same wires, thereby allowing transactions to be sent over a smaller number of wires compared to prior interconnect solutions while maintaining high quality of service for each transmission. EX2001, ¶55. NoC technology also contributed to decreased die density by distributing the interconnect logic throughout the chip rather than having bridges as chokepoints.” *Id.*

Engineers at Koninklijke Philips Electronics (the original assignor of the ’2893 Patent) identified the same issues with existing interconnects and described the distinction between prior interconnects (e.g., buses and crossbars) and a multi-hop interconnect in patents related to network-on-chip technology in a related patent – U.S. Patent No. 7,373,449 (EX2017).

NoCs help resolve the electrical problems in new deep-submicron technologies, as they structure and manage global wires. At the same time they share wires, lowering their number and increasing their utilization. ... NoCs also decouple computation from communication, which is essential in managing the design of billion-transistor chips. NoCs achieve this decoupling because they are traditionally designed using protocol stacks, which provide well-defined interfaces separating communication service usage from service implementation.

EX2017, 1:38-49; EX2001, ¶56.

Moreover, using multi-hop interconnects “radically changes the communication when compared to direct interconnects, such as buses or switches.” EX2001, ¶¶44, 56; EX2017, 3:46–57 (“This is because of the multi-hop nature of a network, where communication modules are not directly connected, but separated by one or more network nodes. This is in contrast with the prevalent existing interconnects (i.e., buses) where modules are directly connected. The implications of this change reside in the arbitration (which must change from centralized to distributed), and in the communication properties (e.g., ordering, or flow control.)”). EX2001, ¶56.

Examples of differences between a multi-hop interconnect and a bus include: (1) media arbitration; (2) data routing; (3) data formatting; (4) latency; and (5) flow control for input buffers. EX2001, ¶57.

(1) Regarding media arbitration, “[i]n a bus, master modules request access to the interconnect, and the arbiter grants the access for the whole interconnect at once,” whereas in a NoC, “the arbitration is distributed, because it is performed in every router, and is based only on local information.” ’449 Patent, 5:25–42; EX2001, ¶57.

(2) Regarding data routing, “[f]or a bus, the command, address, and data are broadcasted on the interconnect. They arrive at every destination, of which one activates based on the broadcasted address, and executes the requested command,”

whereas in a NoC, “it is not feasible to broadcast information to all destinations, because it must be copied to all routers and network interfaces. This floods the network with data. The address is better decoded at the source to find a route to the destination module.” ’449 Patent, 5:43–54; EX2001, ¶58.

(3) Regarding data formatting, “[i]n modern bus interfaces the data format is defined by separate wire groups for the transaction type, address, write data, read data, and return acknowledgements/errors (e.g., VCI, OCP, AMBA, or CoreConnect),” whereas in a NoC, “there is typically no distinction between different kinds of data. Data is treated uniformly, and passed from one router to another.” EX2017, 6:8–25; EX2001, ¶59.

(4) Regarding latency

[L]atency is caused by two factors: (a) the access time to the bus, which is the time until the bus is granted, and (b) the latency introduced by the interconnect to transfer the data. For a bus, where the arbitration is centralized the access time is proportional to the number of masters connected to the bus. The transfer latency itself typically is constant and relatively fast, because the modules are linked directly. However, the speed of transfer is limited by the bus speed, which is relatively low. In a NoC, arbitration is performed at each router for the following link. The access time per router is small. Both end-to-end access time and transport time increase proportionally to the number of hops between master and slave. However, network links are unidirectional and point to point, and hence can run at higher frequencies than buses, thus lowering the latency. From a latency perspective, using a bus or a network is a trade off between the number of modules connected to the interconnect (which affects access time), the speed of the interconnect, and the network topology.

Multi-hop interconnects also differ from buses with respect to flow control for input buffers:

For buses, the source and destination are directly linked, and, destination can therefore signal directly to a source that it cannot accept data. This information can even be available to the arbiter, such that the bus is not granted to a transaction trying to write to a full buffer. In a NoC, however, the destination of a transaction cannot signal directly to a source that its input buffer is full. Consequently, transactions to a destination can be started, possibly from multiple sources, after the destinations input buffer has filled up. If an input buffer is full, additional incoming transitions are not accepted, and stored in the network. However, this approach can easily lead [sic] to network congestion, as the data could be eventually stored all the way to the sources, blocking the links in between.

EX2017, 6:48–62; EX2001, ¶61.

“NoC’s premises are different from off-chip networks, and, therefore, most of the network design choices must be reevaluated” because “[o]n-chip networks have different properties (e.g., tighter link synchronization) and constraints (e.g., higher memory cost) leading to different design choices, which ultimately affect the network services.” EX2017, 1:66–2:5; EX2001, ¶62. Another distinction between an on-chip network compared to off-chip networks is that “[a]n off-chip network interface usually contains a dedicated processor to implement the protocol stack up to network layer or even higher, to relieve the host processor from the communication processing;” however, “[i]ncluding a dedicated processor in a

network interface is not feasible on chip, as the size of the network interface will become comparable to or larger than the IP to be connected to the network.”

EX2017, 2:16–25; EX2001, ¶62.

Further, data sent via a NoC may be subject to out-of-order arrival, diverse routing paths, and retransmission after dropping.

In a network, data sent from a source to a destination may arrive out of order due to reordering in networks nodes, following different routes, or retransmission after dropping. For off-chip networks out-of-order data deliver is typical. However, for NoCs where no data is dropped, data can be forced to follow the same path between a source and a destination (deterministic routing) with no reordering. This in-order data transportation requires less buffer-space, and reordering modules are no longer necessary.

EX2017, 3:8–17; EX2001, ¶63.

On-chip networks also differ from off-chip networks with respect to time-related guarantees.

Off-chip networks typically use packet switching and offer best-effort services. Contention can occur at each network node, making latency guarantees very hard to offer. Throughput guarantees can still be offered using schemes such as rate-based switching or deadline-based packet switching, but with high buffering costs. An alternative to provide such time-related guarantees is to use time-division multiple access (TDMA) circuits, where every circuit is dedicated to a network connection. Circuits provide guarantees at a relatively low memory and computation cost. Network resource utilization is increased when the network architecture allows any left-over guaranteed band width to be used by best-effort communication.

EX2017, 3:34–46; EX2001, ¶64.

On-chip networks can also provide more reliable communication compared to off-chip networks.

A consequence of the tight on-chip resource constraints is that the network components (i.e., routers and network interfaces) must be fairly simple to minimize computation and memory requirements. Luckily, on-chip wires provide a reliable communication medium, which can help to avoid the considerable overhead incurred by off-chip networks for providing reliable communication. Data integrity can be provided at low cost at the data link layer. However, data loss also depends on the network architecture, as in most computer networks data is simply dropped if congestion occurs in the network.

EX2017, 2:43–53; EX2001, ¶65.

On-chip networks also differ from off-chip networks because of their constraints and synchronization:

Typically, resource constraints are tighter on chip than off chip. Storage (i.e., memory) and computation resources are relatively more expensive, whereas the number of point-to-point links is larger on chip than off chip. Storage is expensive, because general-purpose on-chip memory, such as RAMS, occupy a large area. Having the memory distributed in the network components in relatively small sizes is even worse, as the overhead area in the memory then becomes dominant.

EX2017, 2:6–15; EX2001, ¶66.

Given the technical challenges, a POSITA would have been dissuaded from attempting to modify or combine different prior art to arrive at the respective claimed inventions. EX2001, ¶¶67-68.

Neither Dielissen, Hassoun, or any other reference cited by Petition or Dr. Hassoun provide any motivation to incorporate any specific teaching—i.e., the Registered Buffered Path algorithm of Hassoun—into the design or implementation of the NoC described by Dielissen. EX2001, ¶116. Dr. Mowry's opinions are conclusory and are untethered to Dielissen. EX2001, ¶115. Further, neither Dielissen, Hassoun, or any other reference cited by Dr. Hassoun identifies a specific problem in Dielissen that could be solved by incorporating the Registered Buffered Path algorithm of Hassoun into the design or implementation of the NoC described by Dielissen. EX2001, ¶116. It also would not be obvious to try incorporating the Registered Buffered Path algorithm of Hassoun into the design or implementation of the NoC described by Dielissen, and such combination would not succeed, because Hassoun's Registered Buffered Path algorithm does not utilize a size of a packet as an input to produce its output. EX2001, ¶116.

For at least the reasons described above, Dielissen in view of Hassoun does not disclose or render obvious at least the limitation of claim 10 of the '2893 Patent that recites “in response to the identifying act, **inserting M*N data storage elements into the data communication network**, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel” (emphasis added), where the preamble recites “**each data package compris[es] N data elements**” (emphasis added). EX2001, ¶¶107-116.

2. Dielissen in View of Hassoun Fails to Render Obvious Claim 1

The Petition alleges that Dielissen in View of Hassoun discloses at least the limitation “the data communication introducing a delay of $M*N$ cycles on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold” of claim 1 for the same reasons discussed for independent claim 10. See Petition, 68. Thus, Dielissen in view of Hassoun fails to render obvious independent Claim 1 for the same reasons as Claim 10. EX2001, ¶117.

3. Dielissen in View of Hassoun Fails to Render Obvious Claim 7

The Petition alleges that Dielissen in View of Hassoun discloses at least limitation “the data communication network further comprising $M*N$ data storage elements, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel” for the same reasons discussed for independent claim 10. See Petition, 68. Thus, Dielissen in view of Hassoun fails to render obvious independent Claim 7 for the same reasons as Claim 10. EX2001, ¶118.

4. Dielissen in View of Hassoun Fails to Render Obvious the Dependent Claims

The dependent claims are not obvious over Dielissen in view of Hassoun for at least the same reasons that the independent claims from which they depend are not obvious over Dielissen in view of Hassoun.

D. Ground 4: Purported Obviousness over Grounds 1–3 Further in View of Sullam (Claim 8)

In Ground 4, Petitioners allege that claim 8 is rendered obvious over Grounds 1–3 Further in View of Sullam. *See* Petition, 78. Claim 8 depends from claim 1 and is patentable for at least the same reasons as claim 1, as discussed above in relation to Grounds 1-3.

IX. CONCLUSION

For at least the foregoing reasons, the Petition should be denied as to each of the requested grounds. For brevity, Patent Owner may not have addressed all characterizations of the applied references and the challenged claims and reserves the right to do so should institution be granted. The absence of a response by Patent Owner to any of the arguments presented in the Petition or the associated expert declaration does not constitute a concession to those arguments. The fact that Patent Owner's Preliminary Response has focused on particular arguments does not constitute a concession that there are no other arguments for patentability of the challenged claims.

U.S. Patent No. 8,072,893
IPR2024-00355

Patent Owner's Preliminary Response

Respectfully submitted,

Dated: March 27, 2024

By: /Jennifer Hayes/
Jennifer Hayes
Reg. No. 50,845
Nixon Peabody LLP
300 South Grand Avenue,
Suite 4100,
Los Angeles, CA 90071-3151
Tel. 213-629-6179
Fax 866-781-9391

Lead Counsel for Patent Owner

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the foregoing Patent Owner's Preliminary Response is produced using a 14-point Times New Roman font and contains approximately 10,886 words, which is less than the 14,000 total words permitted by the U.S. Patent Trial and Appeal Board rules. Counsel relies on the word count of the computer program used to prepare the response on March 27, 2024.

Dated: March 27, 2024

By: /s/ Jennifer Hayes

Lead Counsel for Patent Owner

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing **Patent Owner's Preliminary Response** was served on March 27, 2024, by email:

J. Derek Vandenburg
Aaron W. Pederson
Nathan D. Louwagie
Ryan D. Rypka
Carlson Caspers Vandenburg & Lindquist, P.A.
225 South Sixth Street, Suite 4200
Minneapolis, MN 55402
dvandenburg@carlsoncaspers.com
apederson@carlsoncaspers.com
nlouwagie@carlsoncaspers.com
rrypka@carlsoncaspers.com

F. Christopher Mizzo, P.C.
KIRKLAND & ELLIS LLP
1301 Pennsylvania Ave., N.W.
Washington, D.C. 20004
Telephone: (202) 389-5000
Sasmung_NST_IPR@kirkland.com

Gregory S. Arovas, P.C.
Alan Rabinowitz
KIRKLAND & ELLIS LLP
601 Lexington Avenue
New York, NY 10022
Telephone: (212) 446-4800
Sasmung_NST_IPR@kirkland.com

Counsel for Petitioners

By: /s/ Jennifer Hayes

Lead Counsel for Patent Owner