

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED and
SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETWORK SYSTEM TECHNOLOGIES, LLC,
Patent Owner.

IPR2024-00355
Patent 8,072,893 B2

Before CHARLES J. BOUDREAU, JOHN R. KENNY, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

AMUNDSON, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Qualcomm Incorporated and Samsung Electronics Co., Ltd. (collectively “Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–3 and 6–10 in U.S. Patent No. 8,072,893 B2 (Exhibit 1001, “the ’893 patent”) under 35 U.S.C. §§ 311–319. Paper 1 (“Pet.”). Network System Technologies, LLC (“Patent Owner”) filed a Preliminary Response. Paper 7 (“Prelim. Resp.”). No further briefing was requested or authorized.

Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute an *inter partes* review. We may institute an *inter partes* review only if “the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). The “reasonable likelihood” standard is “a higher standard than mere notice pleading” but “lower than the ‘preponderance’ standard to prevail in a final written decision.” *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 13 (PTAB Dec. 20, 2019) (precedential).

After considering the Petition, the Preliminary Response, and the evidence of record, and for the reasons explained below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in proving the unpatentability of at least one claim challenged in the Petition. Hence, we deny the Petition and do not institute an *inter partes* review.

II. BACKGROUND

A. *Real Parties in Interest*

Petitioner identifies the following real parties in interest: Qualcomm Incorporated; Qualcomm Technologies, Inc.; Samsung Electronics Co., Ltd.;

Samsung Semiconductor, Inc.; Samsung Electronics America, Inc.; and Samsung Austin Semiconductor, LLC. Pet. 84; *see id.* at 85 n.14. Patent Owner identifies itself as the sole real party in interest. Paper 5, 2. The parties do not raise any issue about real parties in interest.

B. Related Matters

Petitioner and Patent Owner identify the following civil actions as related matters:

- *Network System Technologies, LLC v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00481 (E.D. Tex. filed Dec. 19, 2022) (the “Samsung litigation”);
- *Network System Technologies, LLC v. Texas Instruments Inc.*, No. 2:22-cv-00482 (E.D. Tex. filed Dec. 19, 2022) (the “TI litigation”);
- *Network System Technologies, LLC v. Qualcomm Inc. et al.*, No. 1:22-cv-01331 (W.D. Tex. filed Dec. 19, 2022) (the “Qualcomm litigation”);
- *Network System Technologies, LLC v. Lenovo Group Ltd.*, No. 2:23-cv-00167 (E.D. Tex. Apr. 11, 2023);
- *Network System Technologies, LLC v. Ford Motor Co.*, No. 2:23-cv-00440 (E.D. Tex. filed Sept. 26, 2023); and
- *Network System Technologies, LLC v. OnePlus Technology (Shenzhen) Co., Ltd.*, No. 2:23-cv-00520 (E.D. Tex. filed Nov. 14, 2023).

Pet. 84–85; Paper 5, 2.

Patent Owner identifies the following Board proceedings as related matters:

- *Samsung Electronics Co., Ltd. v. Network System Technologies, LLC*, IPR2024-00338 (Patent 7,373,449 B2);

- *Samsung Electronics Co., Ltd. v. Network System Technologies, LLC*, IPR2024-00339 (Patent 8,086,800 B2); and
- *Qualcomm Inc. and Samsung Electronics Co., Ltd. v. Network System Technologies, LLC*, IPR2024-00343 (Patent 7,594,052 B2).

Paper 5, 3.

C. The '893 Patent (Exhibit 1001)

The '893 patent, titled “Integrated Circuit with Data Communication Network and IC Design Method,” issued on December 6, 2011, from an application filed on April 20, 2006. Ex. 1001, codes (22), (45), (54). The patent names John Dielissen and Edwin Rijpkema as inventors. *Id.* at code (75). The patent states that the invention “relates to an integrated circuit having a plurality of functional blocks interconnected via a data communication network.” *Id.* at 1:5–7; *see id.* at code (57).

The '893 patent explains that “most integrated circuits (ICs) are very large scale integration (VLSI) circuits having a large number of features that typically implement a large number of functions” located in “discrete functional blocks, e.g. system on chip (SoC) architectures.” Ex. 1001, 1:8–13. But the “interconnect of the functional blocks poses a design challenge” due to “the high clock speeds of modern ICs” that facilitate “communicating large amounts of data between the functional blocks.” *Id.* at 1:13–18.

To (1) “facilitate flexible communication on the one hand” and (2) “limit the amount of wires required on the other hand,” ICs may “incorporate a data communication network, also referred to as a network on chip (NoC).” Ex. 1001, 1:19–22. NoCs “typically comprise a plurality of

network stations, each associated with a functional block, interconnected via communication channels, e.g. wires.” *Id.* at 1:22–25. The “plurality of network stations include a plurality of data routers and a plurality of network interfaces, each data router being coupled to a functional block via a network interface.” *Id.* at 1:25–28. Data traverses the network “in the form of packages that include a mixture of data and routing instructions for the network stations.” *Id.* at 1:28–30. To facilitate duplex (two-way) communication between network stations, “a pair of network stations is typically interconnected via at least a pair of communication subchannels.” *Id.* at 1:30–33.

The ’893 patent describes a problem “associated with communication channels, e.g. wires.” Ex. 1001, 1:34–35. Specifically, “the clock speed at which the IC can operate may be determined by the slowest communication channel, i.e. the channel exhibiting the largest data transfer delay.” *Id.* at 1:34–38.

According to the ’893 patent, conventional solutions that “introduce a data storage element such as a latch into the slowest data communication channel” cannot “straightforwardly be applied to ICs communicating data between the functional blocks via an integrated network, especially when the nature of the communicated data differs per clock cycle.” Ex. 1001, 1:47–50. In that type of network, a router “receives the routing data incorporated in the data packet during a predefined clock cycle.” *Id.* at 1:54–57. Delaying “the communication to that router over a slow communication channel by a clock cycle to speed up the rest of the network would cause the routing data to arrive outside the predefined clock cycle, causing erroneous behaviour of the network.” *Id.* at 1:57–61.

The '893 patent endeavors to address that deficiency and “improve the data communication speed of a network of an integrated circuit.” Ex. 1001, 1:62–64; *see id.* at 1:5–7, 1:65–2:14, 3:34–53, code (57). In particular, an “integrated circuit includes functional blocks and a data communication network having network stations interconnected via communication channels for communicating data packages between the functional blocks.” *Id.* at code (57); *see id.* at 1:66–2:3. “Each data package includes N data elements having a data element with routing information for the network stations, N being an integer of at least two.” *Id.* at code (57); *see id.* at 2:3–6, 4:53–56. “The network stations include data routers and network interfaces, where each of the data routers is coupled to a functional block via a network interface.” *Id.* at code (57); *see id.* at 2:6–9. “The data communication network includes first and second network stations interconnected through a first communication channel.” *Id.* at code (57); *see id.* at 2:9–11. “The network includes $M \times N$ data storage elements, M being a positive integer, for introducing a delay of $M \times N$ cycles on the first communication channel.” *Id.* at code (57); *see id.* at 2:11–14.

The '893 patent explains that the invention rests on “the realization that the correct operation of the network relies on the maintenance of the correct periodicity between the network stations.” Ex. 1001, 2:15–17. Because “the data packages have a fixed size of N data elements, the communication of a complete package between two network stations takes N clock cycles, or N handshake driven data transfers in case of an asynchronous implementation of the network.” *Id.* at 2:17–22. “The routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package, e.g. the first

data element (i.e. a header), although other data elements may (also) contain such information.” *Id.* at 2:22–26. Because “a network station expects routing information to arrive periodically (i.e. after every N cycles),” introducing a delay “on the first communication channel (which typically is the slowest channel of the network) matching such a period, i.e. by delaying the whole data package rather than a single data element, the delayed data package is received by the receiving network station during the appropriate period, e.g. clock cycle.” *Id.* at 2:26–33.

“Preferably, $M=1$ in order to minimize the number of required delay elements, which will minimize the delay introduced on the first communication channel.” Ex. 1001, 3:15–17.

The ’893 patent’s Figure 1 (reproduced below) depicts an integrated circuit (IC):

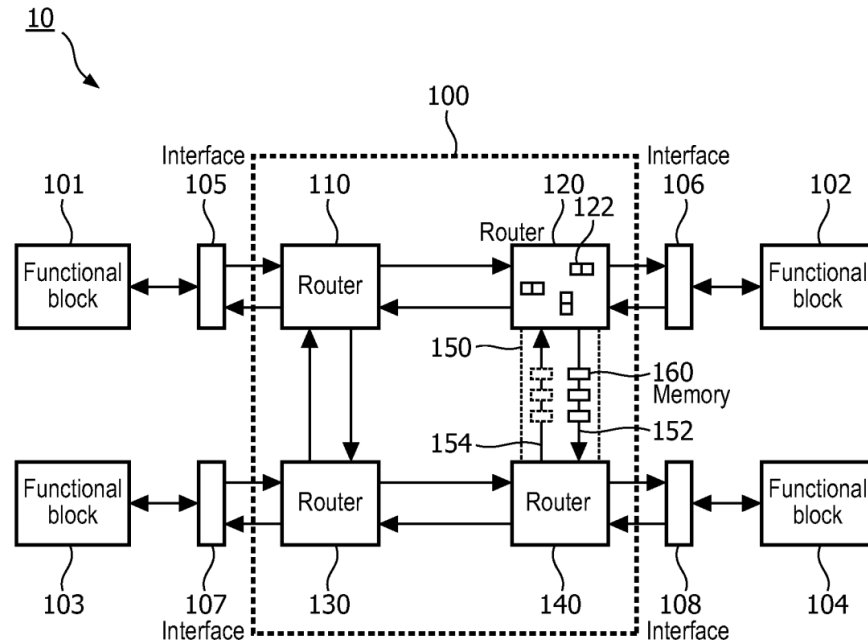


FIG. 1

Figure 1 illustrates IC 10 including the following components:

- data communication network 100;

- functional blocks 101, 102, 103, and 104, e.g., “processing units,” interconnected via data communication network 100;
- network interfaces 105, 106, 107, and 108 connected to functional blocks 101, 102, 103, and 104, respectively;
- data routers 110, 120, 130, and 140 connected to network interfaces 105, 106, 107, and 108, respectively;
- the data routers and respective network interfaces comprising “the network stations of the data communication network 100”;
- data communication channels 150, e.g., “one or more wires,” interconnecting data routers 110, 120, 130, and 140; and
- the data communication channel between data routers 120 and 140 comprising “a first subchannel 152 and a second subchannel 154.”

Ex. 1001, 4:25–33, 4:45–47, 5:5–10, Fig. 1.

Data communication network 100 allows “flexible communication of data streams between the functional blocks 101–104.” Ex. 1001, 4:48–50. “Typically, such a data stream comprises one [or] more data packages, with each data package comprising N data elements, with N being an integer having a value of at least 2.” *Id.* at 4:51–53. “At least one of the N data elements in a package, e.g. the first data element, comprises routing instructions for the destination network station.” *Id.* at 4:53–56. “Typically, the header of a first data package will comprise information about the destination of the data package as well as the service level of the data package, e.g. guaranteed bandwidth or best effort service.” *Id.* at 5:29–32.

In Figure 1, “the communication channel 150 between data routers 120 and 140 has been identified as the communication channel in the

network 100 exhibiting a data transfer delay exceeding a predetermined delay threshold.” Ex. 1001, 5:43–46; *see id.* at 9:54–60. To “avoid having to limit the communication speed, e.g. the clock speed, of the data communication network 100,” the communication channel 150 between data routers 120 and 140 is “equipped with $M*N$ data storage elements to introduce a delay of $M*N$ cycles onto the communication channel, with N corresponding to the size of a data package.” *Id.* at 5:49–58; *see id.* at 9:60–65. Inserting $M*N$ data storage elements allows increasing “the maximum communication frequency of the data network 100 at the expense of” introducing “a delay of a single data package, i.e. the number of clock cycles it takes to communicate such a data package, on the slow communication channel 150.” *Id.* at 5:54–62; *see id.* at 9:65–67.

In Figure 1, data communication network 100 is “arranged to communicate data packages with size $N=3$.” Ex. 1001, 5:63–64. “Other values of N are equally feasible.” *Id.* at 5:64–65. Subchannel 152 “of the slow communication channel 150 is extended with $N=3$ data storage elements 160,” with $M=1$ in that arrangement. *Id.* at 5:65–67. Optionally, subchannel 154 “of the slow communication channel 150 is also extended with $N=3$ data storage elements 160,” with $M=2$ in that arrangement. *Id.* at 5:67–6:2. “The data storage elements 160 may be a pipeline or a buffer of latches or flipflops, and may be implemented using synchronous or asynchronous storage elements.” *Id.* at 6:24–27.

The '893 patent's Figure 2 (reproduced below) depicts the timing of communication along a communication channel or subchannel with three data storage elements:

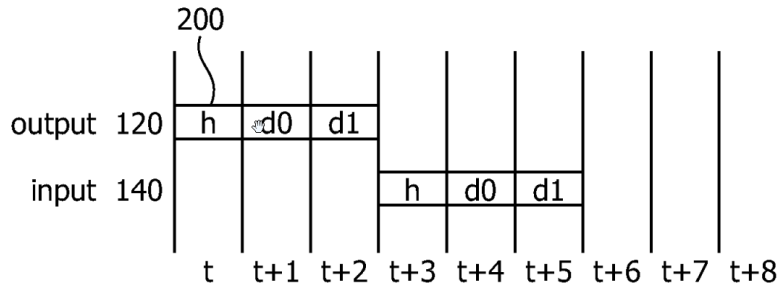


FIG. 2

Figure 2 illustrates the timing of a data package with three data elements (i.e., header element h, data element d0, and data element d1) “along the slow channel 150” in Figure 1 “extended with 3 data storage elements 160 on the first subchannel 152 interconnecting an output port of data router 120 with an input port of the data router 140.” Ex. 1001, 6:31–40, Figs. 1–2.

A data router employing wormhole routing, e.g., data router 120, provides header element h at clock cycle t, data element d0 at clock cycle t+1, and data element d1 at clock cycle t+2. Ex. 1001, 6:35–40, Fig. 2. The “presence of N=3 data storage elements 160 in the first subchannel 152 of the slow communication channel 150” causes data router 140 to receive a data element after N=3 clock cycles. *Id.* at 6:60–66, Fig. 2.

In Figure 1, the data routers are “all configured to periodically evaluate the content of a received data package” after “every N clock cycles for a data package having a size N data elements.” Ex. 1001, 6:40–44. In Figure 1, the data routers “perform this operation simultaneously, i.e. at the same clock cycle, which is clock cycle t plus every Nth clock cycle afterwards, i.e. at t+3, t+6 and so on, at which the arrival of a header h of a

new data package is expected.” *Id.* at 6:44–48. “Consequently, it is essential that the headers of the data packages do not arrive at any data router 110, 120, 130, 140 outside such an evaluation clock cycle.” *Id.* at 6:50–53.

D. The Challenged Claims

Petitioner challenges the following claims:

- independent claim 1 for an “integrated circuit”;
- claims 2, 3, 6, 8, and 9 that depend directly or indirectly from claim 1;
- independent claim 7 for an “integrated circuit”; and
- independent claim 10 for a “method of designing an integrated circuit.”

Pet. 3–4, 10–81.

Claims 1 and 10 exemplify the challenged claims and read as follows (with formatting added for clarity and with bracketed numbers and letters added for reference purposes):¹

1. [1.pre] An integrated circuit comprising:
 - [1.a] a plurality of functional blocks; and
 - [1.b] a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks,
 - [1.c] each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two,
 - [1.d] the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces,

¹ We use the same numbers and letters that Petitioner uses to identify the claim language. *See* Pet. 13–29, 88–89.

each of the data routers being coupled to a functional block via a network interface,

[1.e] the data communication network comprising a first network station and a second network station interconnected through a first communication channel,

[1.f] the data communication network further comprising $M*N$ data storage elements, M being a positive integer, the data communication introducing a delay of $M*N$ cycles on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold.

10. [10.pre] A method of designing an integrated circuit comprising

[10.pre.a] a plurality of functional blocks, and

[10.pre.b] a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks,

[10.pre.c] each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two,

[10.pre.d] the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface;

the method comprising the acts of:

[10.e] identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold; and

[10.f] in response to the identifying act, inserting $M*N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel.

Ex. 1001, 10:28–49, 12:22–41.

E. The Asserted References

For its challenges, Petitioner relies on the following references:

Name	Reference	Exhibit
Bertozzi	Davide Bertozzi & Luca Benini, <i>Xpipes: A Network-on-Chip Architecture for Gigascale Systems-on-Chip</i> , IEEE Circuits and Systems Magazine, Vol. 4, No. 2, 18–31 (September 2004) ²	1005
Jantsch	Axel Jantsch & Hannu Tenhunen eds., <i>Networks on Chip</i> , Kluwer Academic Publishers (2003)	1006
Dielissen	John Dielissen et al., <i>Concepts and Implementation of the Philips Network-on-Chip</i> , IP Based SoC Design 2003, Grenoble, France, 1–6 (November 2003)	1007
Duato	José Duato et al., <i>Interconnection Networks: An Engineering Approach</i> , IEEE Computer Society Press (1998)	1009
Hassoun	Soha Hassoun et al., <i>Optimal Buffered Routing Path Constructions for Single and Multiple Clock Domain Systems</i> , IEEE/ACM International Conference on Computer Aided Design, 247–53 (November 2002) ³	1011
Sullam	US 6,614,320 B1, issued September 2, 2003 (based on an application filed October 24, 2001)	1013

Pet. 3–4, 10–81.

Petitioner asserts that:

- (1) Bertozzi, Jantsch, Dielissen, Duato, and Hassoun qualify as prior art “under at least pre-AIA §§ 102(a)–(b)”;

² The acronym “IEEE” stands for “Institute of Electrical and Electronics Engineers.”

³ The acronym “ACM” stands for “Association for Computing Machinery.”

- (2) Sullam qualifies as prior art “under at least pre-AIA §§ 102(a)–(b), (e).”

Pet. 2–3; *see* 35 U.S.C. § 102(a), (b), (e) (2006).⁴

At this stage of the proceeding, Patent Owner does not dispute that each reference qualifies as prior art. *See, e.g.*, Prelim. Resp. 22–50.

F. The Asserted Challenges to Patentability

Petitioner asserts the following challenges to patentability:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–3, 6, 7, 10	102(a)–(b)	Bertozzi
1–3, 6, 7, 10	103(a)	Bertozzi
1–3, 6, 7, 10	103(a)	Bertozzi, Jantsch
1–3, 6, 7, 10	103(a)	Bertozzi, Duato
1–3, 6, 7, 9, 10	103(a)	Dielissen, Hassoun
8	103(a)	Bertozzi, Sullam
8	103(a)	Bertozzi, Jantsch, Sullam
8	103(a)	Bertozzi, Duato, Sullam
8	103(a)	Dielissen, Hassoun, Sullam

Pet. 3–4, 10–81.

G. Testimonial Evidence

To support its challenges, Petitioner relies on the declaration of Marwan Hassoun, Ph.D. (Exhibit 1003). Dr. Hassoun states, “I have been retained by” Petitioner as “an independent expert consultant in this

⁴ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 102 and § 103 effective March 16, 2013. Because the filing date of the challenged claims predates the AIA’s amendments to § 102 and § 103, this decision refers to the pre-AIA versions of § 102 and § 103.

proceeding.” Ex. 1003 ¶ 1. Dr. Hassoun also states, “In 1984 and 1988, I earned a master’s degree and a Ph.D., respectively, in Electrical Engineering from Purdue University with specialization in software and algorithms for computer-aided design of electronic circuits.” *Id.* ¶ 12.

Further, Petitioner relies on the declarations of Sylvia D. Hall-Ellis, Ph.D. (Exhibit 1021), Philippe Coeurdevey (Exhibit 1022), and Gordon MacPherson (Exhibit 1020, Exhibit 1023, and Exhibit 1024) to establish the authenticity and public availability of various publications that Petitioner cites as evidence of unpatentability.

To support its positions, Patent Owner relies on the declaration of Erik Chmelar, Ph.D. (Exhibit 2001). Dr. Chmelar states, “I have been retained on behalf of” Patent Owner as “an expert consultant.” Ex. 2001 ¶ 1. Dr. Chmelar also states, “In 2001, I received an M.S. degree in Electrical Engineering from Stanford University, with a focus on computer networks In 2004, I received a Ph.D. degree in Electrical Engineering from Stanford University, with a primary focus on very large-scale integrated (VLSI) systems” *Id.* ¶ 5.

Additionally, Petitioner cites Dr. Chmelar’s November 2023 declaration (Exhibit 1027) in the Qualcomm litigation when discussing claim construction. Pet. 9–10 (citing Ex. 1027 ¶ 164); *see infra* § IV.D.2.

III. DISCRETIONARY DENIAL IN VIEW OF PARALLEL LITIGATION

Under § 314(a), the Director possesses “broad discretion” in deciding whether to institute an *inter partes* review. *See* 35 U.S.C. § 314(a); *Saint Regis Mohawk Tribe v. Mylan Pharms. Inc.*, 896 F.3d 1322, 1327 (Fed. Cir. 2018). The Director is “permitted, but never compelled,” to institute an *inter*

partes review. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016). The Board decides whether to institute an *inter partes* review on the Director’s behalf. 37 C.F.R. § 42.4(a) (2023).

Based on *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential), Patent Owner argues that we should exercise our discretion under § 314(a) to deny institution in view of the Samsung litigation and the Qualcomm litigation. *See* Prelim. Resp. 10–22; *supra* § II.B. Petitioner argues that we should decline to exercise our discretion under § 314(a) to deny institution. *See* Pet. 82–84.

For the reasons explained below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in proving the unpatentability of at least one claim challenged in the Petition. *See infra* §§ IV.E–IV.I. Hence, we do not consider discretionary denial under § 314(a).

IV. PATENTABILITY ANALYSIS

A. Legal Principles: Anticipation

To “demonstrate anticipation, the proponent must show ‘that the four corners of a single, prior art document describe every element of the claimed invention.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Xerox Corp. v. 3Com Corp.*, 458 F.3d 1310, 1322 (Fed. Cir. 2006)). The prior-art document “must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Id.* (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Hence, a patent challenger cannot rely on portions from different, unrelated

embodiments in a prior-art document to demonstrate anticipation. *See id.* at 1369, 1371.

The “disclosure of a limited number of combination possibilities” may anticipate a claim. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 851 F.3d 1270, 1274 (Fed. Cir. 2017). Hence, a reference may anticipate “if that reference teaches that the disclosed components or functionalities may be combined and one of skill in the art would be able to implement the combination.” *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1344 (Fed. Cir. 2016). The “dispositive question regarding anticipation [is] whether one skilled in the art would reasonably understand or infer from the [reference’s] teaching” that it discloses every claim element arranged as in the claim. *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991); *see Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003).

We analyze the anticipation issues according to these principles.

B. Legal Principles: Obviousness

A patent may not be obtained “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). An obviousness analysis involves underlying factual inquiries including (1) the scope and content of the prior art; (2) differences between the claimed invention and the prior art; (3) the level of ordinary skill in the art; and (4) where in evidence, objective indicia of nonobviousness, such as commercial success, long-felt but unsolved needs,

and failure of others.⁵ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18, 35–36 (1966); *Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1047–48 (Fed. Cir. 2016) (en banc). When evaluating a combination of references, an obviousness analysis should address “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

We analyze the obviousness issues according to these principles.

C. Level of Ordinary Skill in the Art

Factors pertinent to determining the level of ordinary skill in the art include (1) the educational level of the inventor; (2) the type of problems encountered in the art; (3) prior-art solutions to those problems; (4) the rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the educational level of workers active in the field. *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–97 (Fed. Cir. 1983). Not all factors may exist in every case, and one or more of these or other factors may predominate in a particular case. *Id.* These factors are not exhaustive, but merely a guide to determining the level of ordinary skill in the art. *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007). Moreover, the prior art itself may reflect an appropriate skill level. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Petitioner asserts that a person of ordinary skill in the art at the time of the alleged invention would have had “at least either” (1) “a bachelor’s degree in electrical engineering, or related field, as well as at least five years of work experience in the field of SoC design” or (2) “a master’s degree in

⁵ The parties do not address objective indicia of nonobviousness. *See, e.g.*, Pet. 10–81; Prelim. Resp. 22–50.

electrical engineering, or a related field as well as at least three years of work experience in the field of SoC design.” Pet. 7–8. Petitioner also asserts that a skilled artisan would have had “an understanding of SoC interconnects, as well as the concepts of large-scale networks.” *Id.* at 8. Dr. Hassoun’s testimony supports Petitioner’s assertions. *See* Ex. 1003 ¶¶ 31–32.

Patent Owner asserts that a person of ordinary skill in the art at the time of the alleged invention would have had “at least a Bachelor’s degree in electrical engineering, computer engineering, or a related field, and as [sic] at least two years of work experience in the field of SoC [(‘system-on-chip’)] and NoC [(‘Network-on-Chip’)] technologies.” Prelim. Resp. 7 (second and third alterations by Patent Owner) (quoting Ex. 2022 (Claim Construction Order), 18). Patent Owner asserts that the district court in the TI litigation adopted this description of an ordinarily skilled artisan. *Id.*

Patent Owner proposes a somewhat lower level of ordinary skill in the art than Petitioner, i.e., “a Bachelor’s degree” and “two years of work experience” according to Patent Owner compared to either “a bachelor’s degree” and “five years of work experience” or “a master’s degree” and “three years of work experience” according to Petitioner. *See* Pet. 7–8; Prelim. Resp. 7.

For purposes of analysis, we adopt Petitioner’s description of an ordinarily skilled artisan because it comports with the technology and claims of the ’893 patent as well as the asserted prior art. For instance, “a master’s degree” and “three years of work experience” would have allowed someone to understand the ’893 patent as well as the asserted prior art. *See* Ex. 1003 ¶ 32.

Moreover, someone with a higher skill level will understand the technology at least as well as someone with a lower skill level. *See Innovention Toys, LLC v. MGA Entm't, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011); *Tokai Corp. v. Easton Enters., Inc.*, 632 F.3d 1358, 1369 (Fed. Cir. 2011). Hence, “it is generally easier to establish obviousness under a higher level of ordinary skill.” *Kinetic Concepts, Inc. v. Smith & Nephew, Inc.*, 688 F.3d 1342, 1366 (Fed. Cir. 2012).

We note that our analysis would not change if we adopted Patent Owner’s description of an ordinarily skilled artisan.

D. Claim Construction

1. GENERAL PRINCIPLES

We construe claim terms “using the same claim construction standard” that district courts use to construe claim terms in civil actions under 35 U.S.C. § 282(b). *See* 37 C.F.R. § 42.100(b). Under that standard, claim terms “are given their ordinary and customary meaning, which is the meaning the term would have to a person of ordinary skill in the art at the time of the invention.” *Power Integrations, Inc. v. Fairchild Semiconductor Int’l, Inc.*, 904 F.3d 965, 971 (Fed. Cir. 2018) (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc)). The meaning of claim terms may be determined by “look[ing] principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

2. DISPUTED CLAIM LANGUAGE

Petitioner explains that the parties in the Qualcomm litigation proposed competing constructions for the following language in the '893 patent's claims:

Term/Limitation	Patent Owner's Proposed Construction	Petitioner's Proposed Construction
"each data package comprising N data elements"	Patent Owner "incorporates its definition for the term 'data package,' 'data elements' are groups of data, and the remaining language should be afforded their plain and ordinary meanings."	"every data package communicated by the network stations has a fixed size of N data elements"
"data package"	"Fixed-size arrangement of data."	"See [Petitioner's] construction of 'each data package comprising N data elements' above."
"data storage elements"	"Array of one or more elements that store data."	"each being a structure that stores one data element"

Pet. 9; *see* Ex. 1025, 25–32;⁶ Ex. 1026, 24–28;⁷ Ex. 1028, 16–20;⁸
Ex. 2052, 6.⁹

Petitioner asserts that Patent Owner “has further clarified its constructions” for “data package” and “each data package comprising N data elements” by explaining that:

- (1) “the number of data elements in each data package traveling through the system ‘can vary between one data package and the next’”; and
- (2) “the term ‘each data package comprising N data elements’ means that each data package comprises N, or more than N, data elements, i.e., at least N data elements.”

Pet. 10 (quoting Ex. 1026, 25; Ex. 1027 ¶ 164). Petitioner also asserts that Patent Owner’s proposed construction for “each data package comprising N data elements” is “significantly broader” than Petitioner’s proposed construction. *Id.*

Additionally, Petitioner contends that the challenged claims are unpatentable under Patent Owner’s proposed constructions and Petitioner’s

⁶ For Exhibit 1025 (Defendants’ Joint Opening Claim Construction Brief), we cite to the page numbers of the brief rather than the page numbers that Petitioner applied to the exhibit.

⁷ For Exhibit 1026 (Network System Technologies, LLC’s Response to Defendants’ Joint Opening Claim Construction Brief), we cite to the page numbers of the brief rather than the page numbers that Petitioner applied to the exhibit.

⁸ For Exhibit 1028 (Defendants’ Joint Reply Claim Construction Brief), we cite to the page numbers of the brief rather than the page numbers that Petitioner applied to the exhibit.

⁹ For Exhibit 2052 (Joint Claim Construction Statement), we cite to the page numbers that Patent Owner applied to the exhibit, which are the same as the header page numbers.

proposed constructions. Pet. 9. Therefore, according to Petitioner, the Board does not need to explicitly construe any claim language to decide whether Petitioner satisfies the “reasonable likelihood” standard for instituting trial. *Id.* at 9–10.

Patent Owner asserts that the Board does not need to explicitly construe any claim language to “find that Petitioners did not meet their burden for institution.” Prelim. Resp. 7–8. But Patent Owner “reserves the right to seek constructions of these terms in litigation and in this *inter partes* review, and to further respond to any constructions” that Petitioner submits. *Id.* at 8.

Patent Owner does not dispute that its proposed construction for “each data package comprising N data elements” is “significantly broader” than Petitioner’s proposed construction. *See* Prelim. Resp. 7–10; Ex. 1026, 25; Ex. 1027 ¶ 164; Ex. 2034, 26.¹⁰

3. “EACH DATA PACKAGE COMPRISING N DATA ELEMENTS”

We agree with Petitioner that Patent Owner’s proposed construction for “each data package comprising N data elements” is “significantly broader” than Petitioner’s proposed construction. *See* Pet. 9–10; Ex. 1026, 25; Ex. 1027 ¶ 164; Ex. 2034, 26. To decide whether Petitioner satisfies the “reasonable likelihood” standard for instituting trial, we must determine the meaning of “each data package comprising N data elements.” Based on the current record, we agree with Petitioner that “each data package comprising N data elements” means “every data package communicated by the network stations has a fixed size of N data elements.”

¹⁰ For Exhibit 2034 (Plaintiff Network System Technologies, LLC’s Opening Claim Construction Brief), we cite to the header page numbers.

See, e.g., Pet. 9; Ex. 1025, 25–29; Ex. 1028, 16–18; Ex. 2035, 23–26;¹¹
Ex. 2040, 32–36;¹² Ex. 2042, 22–24.¹³

The claim language supports the conclusion that “each data package comprising N data elements” means “every data package communicated by the network stations has a fixed size of N data elements.” Ex. 1001, 10:28–49, 11:44–12:6, 12:22–41. Specifically, claims 1, 7, and 10 each recite “a data communication network . . . for communicating data packages between the functional blocks, each data package comprising N data elements . . . N being an integer of at least two.” *Id.* at 10:30–36, 11:46–52, 12:23–29. By its plain meaning, “each data package” refers to every one of the claimed “data packages” communicated by the claimed “data communication network.” For example, Black’s Law Dictionary (5th ed. 1979) defines “each” as “[a] distributive adjective pronoun, which denotes or refers to every one of the persons or things mentioned.” Ex. 3001, 4.

Also, allowing N to “vary between one data package and the next,” as Patent Owner contends, would render the claim language “each data package comprising N data elements” superfluous. *See* Ex. 1026, 25; Ex. 2034, 26. An interpretation rendering some portion of the claim language “void, meaningless, or superfluous” is “highly disfavored.” *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir. 2021). If the inventors wanted N to “vary between one data package and the next,” as Patent Owner

¹¹ For Exhibit 2035 (Samsung’s Responsive Claim Construction Brief), we cite to the header page numbers.

¹² For Exhibit 2040 (Defendants’ Joint Opening Claim Construction Brief), we cite to the header page numbers.

¹³ For Exhibit 2042 (Defendants’ Joint Reply Claim Construction Brief), we cite to the header page numbers.

contends, the inventors could have said “each data package comprising at least two data elements” instead of “each data package comprising N data elements . . . N being an integer of at least two.”

Additionally, claim 10 concerns a “method of designing an integrated circuit.” Ex. 1001, 12:22. Claim 10 recites “in response to the identifying act, inserting $M*N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel.” *Id.* at 12:38–41 (limitation 10.f). Allowing N to “vary between one data package and the next,” as Patent Owner contends, would prevent a skilled artisan from “inserting $M*N$ data storage elements into the data communication network” when “designing an integrated circuit.” *See* Ex. 1026, 25; Ex. 2034, 26. If N could “vary between one data package and the next,” a skilled artisan would not know how many data storage elements to insert to satisfy the $M*N$ requirement when “designing an integrated circuit” according to claim 10.

Claims 1 and 7 concern an “integrated circuit” instead of a “method of designing an integrated circuit” as covered by claim 10. Ex. 1001, 10:28, 11:44. But “when different claims of a patent use the same language,” the language should have the same meaning in each claim unless “otherwise compelled.” *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1119 (Fed. Cir. 2004); *see Wilson Sporting Goods Co. v. Hillerich & Bradsby Co.*, 442 F.3d 1322, 1328 (Fed. Cir. 2006). Here, we see nothing in the intrinsic evidence indicating that “each data package comprising N data elements” should have a different meaning in claims 1 and 7 than in claim 10.

The '893 patent's specification supports the conclusion that "each data package comprising N data elements" means "every data package communicated by the network stations has a fixed size of N data elements." *See, e.g.*, Ex. 1001, 2:15–33, 5:49–62, 6:31–53, Fig. 2. In particular, the specification explains that the invention rests on "the realization that the correct operation of the network relies on the maintenance of the correct periodicity between the network stations." *Id.* at 2:15–17. The specification also explains that "it is essential that the headers of the data packages do not arrive at any data router" outside an evaluation clock cycle because the data routers are "all configured to periodically evaluate the content of a received data package" at the same clock cycle after "every N clock cycles for a data package having a size N data elements." *Id.* at 6:40–48, 6:50–53.

According to the '893 patent's specification, "the data packages have a fixed size of N data elements." Ex. 1001, 2:17–18. Because "the data packages have a fixed size of N data elements, the communication of a complete package between two network stations takes N clock cycles, or N handshake driven data transfers in case of an asynchronous implementation of the network." *Id.* at 2:17–22. Further, the "routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package," e.g., in a header. *Id.* at 2:22–26. Because "a network station expects routing information to arrive periodically (i.e. after every N cycles)," introducing a delay "on the first communication channel (which typically is the slowest channel of the network) matching such a period, i.e. by delaying the whole data package rather than a single data element, the delayed data package is received by the

receiving network station during the appropriate period, e.g. clock cycle.”
Id. at 2:26–33; *see id.* at 5:49–62.

Inserting $M \times N$ data storage elements into a data communication channel to delay “the whole data package rather than a single data element” works only if “every data package communicated by the network stations has a fixed size of N data elements.” *See, e.g.*, Ex. 1001, 1:54–61, 2:15–33, 6:40–53. For instance, if some data packages had a size of $N+1$ data elements and some data packages had a size of $N+2$ data elements, routing information would not arrive periodically “after every N cycles,” and the network would not maintain “the correct periodicity between the network stations.”

As Patent Owner notes when arguing patentability, inserting $M \times N$ data storage elements into a data communication channel “ensure[s] that network stations receive routing information within predefined evaluation cycles.” Prelim. Resp. 28; *see infra* § IV.E.2(c)(ii). If some data packages had a size of $N+1$ data elements and some data packages had a size of $N+2$ data elements, that would conflict with the ’893 patent’s “goal of aligning data package delivery with routing information evaluation cycles.” *See* Prelim. Resp. 29; *infra* § IV.E.2(c)(ii).

The ’893 patent’s prosecution history does not conflict with the claim language or the patent’s specification. *See, e.g.*, Ex. 1002, 125–34 (July 22, 2010, Office action), 144–61 (Oct. 15, 2010, amendment), 169–85 (Jan. 12, 2011, Office action), 194–206 (Apr. 12, 2011, amendment), 211–20 (Aug. 8, 2011, notice of allowance).

Thus, based on the intrinsic evidence, “each data package comprising N data elements” means “every data package communicated by the network stations has a fixed size of N data elements.”

4. OTHER CLAIM LANGUAGE

“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.” *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); see *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Above, we addressed the meaning of “each data package comprising N data elements.” See *supra* § IV.D.3. Based on the current record, we determine that no other claim language requires an explicit construction to decide whether Petitioner satisfies the “reasonable likelihood” standard for instituting trial.

E. Alleged Anticipation by Bertozzi: Claims 1–3, 6, 7, and 10

Petitioner contends that claims 1–3, 6, 7, and 10 are unpatentable under § 102(a)–(b) as anticipated by Bertozzi. See Pet. 10–36. Patent Owner disputes Petitioner’s contentions. See Prelim. Resp. 23–31.

Below, we provide an overview of Bertozzi. Then, we consider the anticipation issues. For the reasons explained below, Petitioner does not establish sufficiently for purposes of institution that Bertozzi anticipates any of claims 1–3, 6, 7, and 10.

1. OVERVIEW OF BERTOZZI (EXHIBIT 1005)

Bertozzi is a paper titled “Xpipes: A Network-on-Chip Architecture for Gigascale Systems-on-Chip” by Davide Bertozzi and Luca Benini, published in the IEEE Circuits and Systems Magazine, Volume 4, Number 2

(September 2004). Ex. 1005, 1;¹⁴ Ex. 1020 ¶¶ 8–11; Ex. 1021 ¶¶ 56–63.

Bertozzi explains that the “integration of an entire system onto the same silicon die,” called System-on-Chip (SoC), “has become technically feasible as an effect of the increasing integration densities made available by deep sub-micron technologies.” Ex. 1005, 2.

Bertozzi describes conventional “shared communication resources” where (1) “an arbitration logic is needed for the serialization of bus access requests” and (2) “only one master at a time can drive the bus” as disadvantageous “when the level of SoC integration will exceed a dozen of cores.” Ex. 1005, 2. Also, “the connection of new blocks to a shared bus increases its associated load capacitance, resulting in more energy consuming bus transactions.” *Id.*

Bertozzi explains that a scalable communication infrastructure with “an on-chip packet-switched micro-network of interconnects,” called Network-on-Chip (NoC), “better supports the trend of SoC integration.” Ex. 1005, 2. The NoC architecture “envisions on-chip router (or switch)-based networks on which packetized communication takes place.” *Id.* With the NoC architecture, “[c]ores access the network by means of proper interfaces, and have their packets forwarded to destination through a multi-hop routing path.” *Id.*

¹⁴ For Exhibit 1005 (Bertozzi), we follow Petitioner’s practice and cite to the page numbers that Petitioner applied to the exhibit rather than the page numbers that appear in the original publication.

Bertozzi's Figure 1 (reproduced below) depicts an example of NoC architecture:

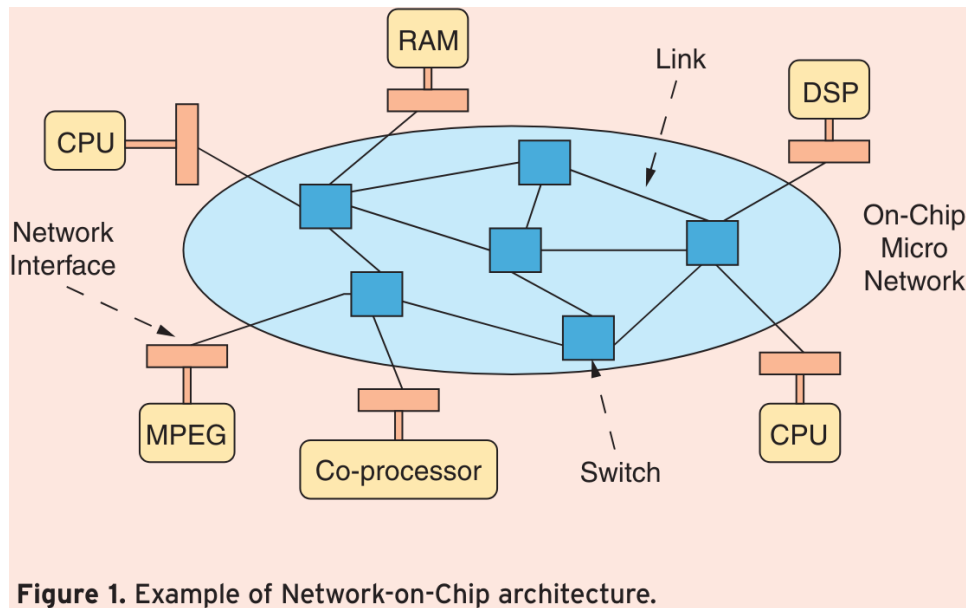


Figure 1 illustrates an SoC with a plurality of cores, such as co-processors, CPUs, DSPs, and RAM, connected through a plurality of network interfaces to an NoC with a plurality of switches/routers interconnected via a plurality of links for communicating packets.¹⁵ Ex. 1005, 2. The switches/routers “carry packets injected into the network to their final destination, following a statically defined or dynamically determined routing path,” e.g., using store-and-forward routing or wormhole routing. *Id.* at 5; *see id.* at 6.

Bertozzi explains that Xpipes includes “a library of soft macros (switches, network interfaces and links) that are design-time composable and tunable so that domain-specific heterogeneous architectures can be instantiated and synthesized.” Ex. 1005, 1, 13; *see id.* at 2, 11. An

¹⁵ The acronym “CPU” stands for “central processing unit.” The acronym “DSP” stands for “digital-signal processor.” The acronym “RAM” stands for “random-access memory.”

XpipesCompiler receives as inputs (1) a file with “information on the network architecture,” (2) routing tables for the network interfaces, and (3) the library of soft macros (switches, network interfaces and links). *Id.* at 12; *see id.* at 10 (Fig. 9). Then, the XpipesCompiler outputs “a SystemC hierarchical description, which includes all switches, links, network nodes and interfaces and specifies their connectivity.” *Id.* at 12; *see id.* at 10 (Fig. 9). That “description” can be (1) “compiled and simulated at the cycle-accurate and signal-accurate level” and/or (2) “fed to backend RTL synthesis tools for silicon implementation.”¹⁶ *Id.* at 12.

By enabling simulation at the cycle-accurate and signal-accurate level, Xpipes permits “comparison of the effects (in terms of area, power and performance) of mapping applications on customized domain-specific NoCs and regular mesh NoCs.” Ex. 1005, 12; *see id.* at 11 (Fig. 11).

Bertozzi describes data packetization as “a critical task for the network interface” that “has an impact on the communication latency, in addition to the latency of the communication channel.” Ex. 1005, 5. Also, messages “transmitted across the network are usually partitioned into fixed-length packets.” *Id.* Further, packets are “often broken into message flow control units called flits.” *Id.* “In the presence of channel width constraints, multiple physical channel cycles can be used to transfer a single flit.” *Id.*

The “packet preparation process consists of building the packet header, payload and packet tail.” Ex. 1005, 5. The packet header “contains the necessary routing and network control information (e.g., the source and destination address).” *Id.* The packet tail “indicates the end of a packet and

¹⁶ The acronym “RTL” stands for “register-transfer level.”

usually contains parity bits for error-detecting or error-correcting codes.” *Id.* During the building process, a network interface may spread the packet header “over a variable number of flits depending on the length of the path to the destination node.” *Id.* at 10; *see id.* at 9 (Fig. 8).

Bertozzi’s Figure 3 (reproduced below) depicts a packet partitioning procedure:

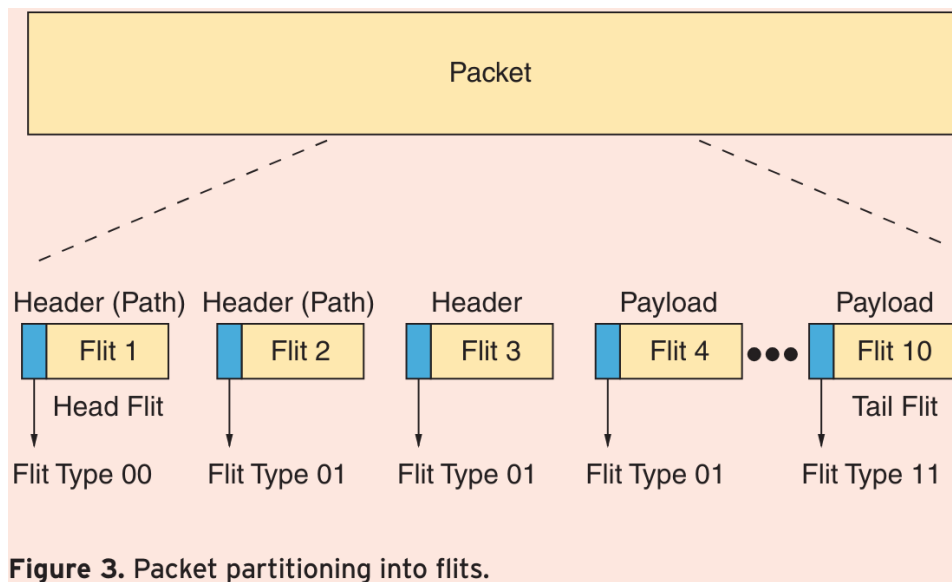


Figure 3 illustrates a packet partitioned into ten flits with (1) the head flit on the left identified as flit type 00, (2) the tail flit on the right identified as flit type 11, and (3) the flits between the head flit and the tail flit identified as flit type 01. Ex. 1005, 6. The flit type “allows to identify the head and the tail flit, and to distinguish between header and payload flits.” *Id.*

Among other design issues, Bertozzi identifies “global wire delays” that require “limiting the on-chip distance travelled by critical signals.” Ex. 1005, 3. As geometries shrink, “gate delay improves much faster than the delay in long wires.” *Id.* at 6. Hence, long wires may “determine the maximum clock rate, and hence performance, of the entire design.” *Id.*

A “solution to overcome the interconnect-delay problem consists of pipelining interconnects,” i.e., pipelining links in the NoC. Ex. 1005, 7. Specifically, switch-to-switch links are “subdivided into basic segments whose length can be tailored to the desired clock frequency that needs to be achieved in the design.” *Id.* Thus, “the system operating frequency is not bound by the delay of long links.” *Id.* The segments (relay stations or repeater stages) “have a function similar to the one of latches in a pipelined data path.” *Id.* at 6–7.

Pipelining links “with a flexible number of stages” decouples link throughput from link length. Ex. 1005, 1. The “number of pipeline stages for each link” is based on “the clock speed target and link routing.” *Id.* at 12. Further, “[i]f network switches are designed in such a way that their functional correctness depends on the flit arriving order and not on their timing, the input links of the switches can be different and of any length.” *Id.* at 7–8.

Additionally, as a trade-off between resource usage and implementation cost, Xpipes employs GO-BACK-N retransmission for error control. Ex. 1005, 7. GO-BACK-N retransmission differs from selective-repeat retransmission where “only those flits that are negatively acknowledged are retransmitted but more buffering resources are required at the destination switch.” *Id.*

With GO-BACK-N retransmission, a source switch transmits flits continuously to a destination switch and “does not wait for an ACK after sending a flit.” Ex. 1005, 7. The source switch receives a response (an ACK or a NACK) “after a round-trip delay” that depends on the link length *N* “expressed in terms of number of repeater stages.” *Id.* at 7–8. When the

source switch receives a NACK, the source switch “backs up to the flit that is negatively acknowledged and re-sends it in addition to the N succeeding flits that were transmitted during the round-trip delay.” *Id.* at 7. At the destination switch, “the N-1 received flits following the corrupted one are discarded regardless of whether they were received error-free or not.” *Id.*

Bertozzi’s Figure 4 (reproduced below) depicts a pipelined link between switches and GO-BACK-N retransmission:

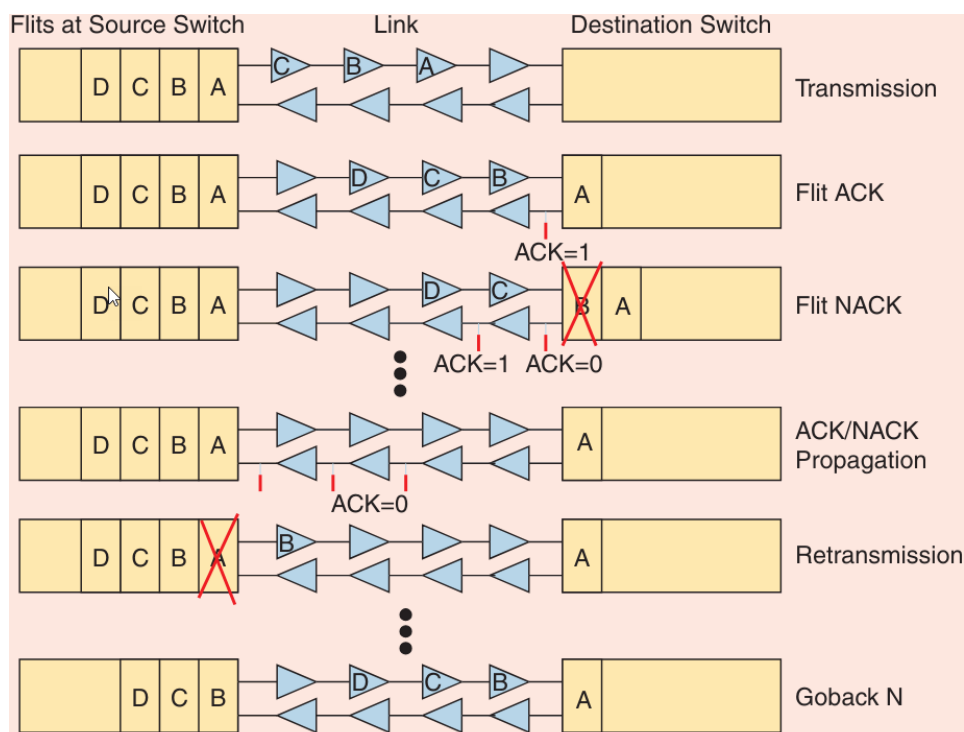


Figure 4. Pipelined link model and latency-insensitive link-level error control.

Figure 4 illustrates the following:

- a Source Switch on the left;
- a Destination Switch on the right;
- a link with four repeater stages in the direction from the Source Switch to the Destination Switch and four repeater stages in the direction from the Destination Switch to the Source Switch;

- a sequence of flits at the Source Switch with four of the flits labeled A, B, C, and D from right to left at the Source Switch;
- the Source Switch transmitting flits A, B, C, and D to the Destination Switch;
- the Destination Switch receiving flit A and returning an ACK (ACK=1);
- the Destination Switch receiving corrupt flit B and returning a NACK (ACK=0); and
- the Source Switch retransmitting flits B, C, and D after receiving the NACK.

See Ex. 1005, 7–8.

With a pipelined link between switches as shown in Figure 4, “[m]ultiple outstanding flits propagate across the link during the same clock cycle.” Ex. 1005, 7–8.

2. INDEPENDENT CLAIM 10

(a) Preamble 10.pre.a, 10.pre.b, 10.pre.c, and 10.pre.d

Claim 10’s preamble recites as follows:

A method of designing an integrated circuit comprising [10.pre.a] a plurality of functional blocks, and [10.pre.b] a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, [10.pre.c] each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, [10.pre.d] the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface.

Ex. 1001, 12:22–32.

Petitioner contends that Bertozzi discloses claim 10's preamble because Bertozzi discloses the following:

- (1) designing communication architectures for “highly integrated deep sub-micron SoCs” that are a “type of integrated circuit”;
- (2) an SoC with a plurality of cores, such as co-processors, CPUs, DSPs, and RAM;
- (3) an NoC for the SoC;
- (4) a plurality of network interfaces connecting the SoC's cores to the NoC;
- (5) the NoC includes a plurality of switches/routers interconnected via a plurality of links for communicating packets; and
- (6) fixed-length packets comprising N flits including (i) a header flit containing routing information, (ii) payload flits, and (iii) a tail flit.

Pet. 13–23; *see id.* at 10–13.

Petitioner maps the claimed “functional blocks” to the SoC's cores. Pet. 14–15. Petitioner maps the claimed “data communication network” to the NoC. *Id.* at 15–16. Petitioner maps the claimed “network stations” to the network interfaces and the switches/routers where a network interface and an associated switch/router together correspond to a “network station.” *Id.* Petitioner maps the claimed “communication channels” to the NoC's links between switches/routers. *Id.* at 15–16. Petitioner maps the claimed “data packages” to the packets traversing the links. *Id.* at 16–17. Petitioner maps the claimed “N data elements” in “each data package” to the multiple flits in each packet. *Id.* at 17–20.

To support its mappings, Petitioner provides an annotated and highlighted version of Bertozzi's Figure 1 as reproduced below (Pet. 22):

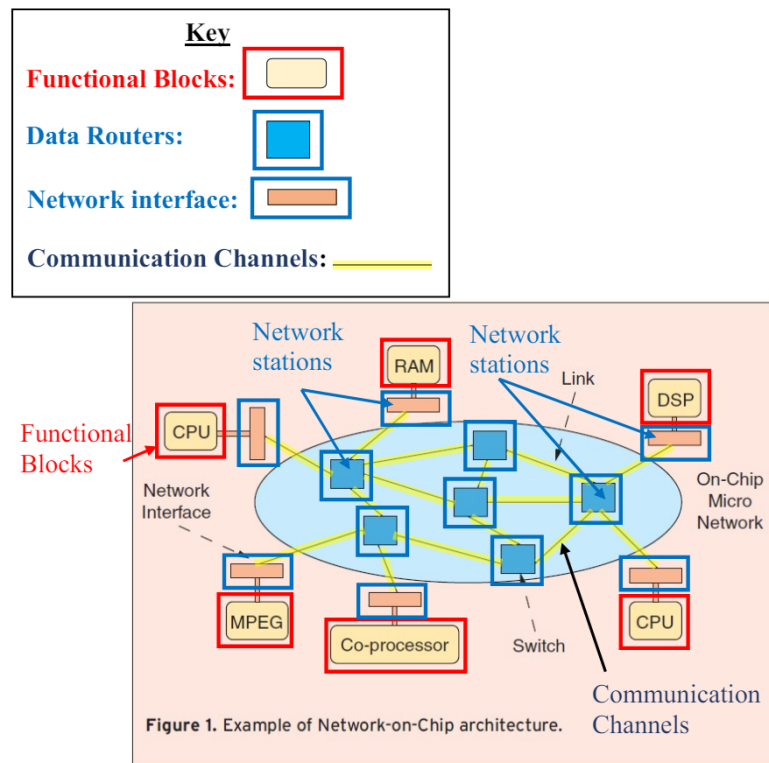


Figure 1 illustrates an SoC with a plurality of cores connected through a plurality of network interfaces to an NoC with a plurality of switches/routers interconnected via a plurality of links for communicating packets.

Ex. 1005, 2. The above annotated and highlighted version of Figure 1 includes the following annotations and highlighting:

- (1) red rectangles around cores identified by the red annotation “Functional Blocks”;
- (2) blue rectangles around network interfaces and switches/routers identified by the lighter blue annotation “Network stations”; and
- (3) yellow highlighting over the links for communicating packets identified by the darker blue annotation “Communication Channels.”

Pet. 22; *see* Ex. 1003 ¶ 128.

Patent Owner asserts that the parties in both the Samsung litigation and the Qualcomm litigation “agreed that the preamble of claim 10 should

be construed as limiting.” Prelim. Resp. 9 (citing Ex. 2052, 1; Ex. 2033, 8).¹⁷ At this stage of the proceeding, however, Patent Owner makes no arguments specific to claim 10’s preamble. *See, e.g., id.* at 23–30. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

Generally, a preamble does not limit a claim. *Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1346 (Fed. Cir. 2002). We need not decide whether claim 10’s preamble limits the claim because, based on the current record and for the reasons advanced by Petitioner and supported by Dr. Hassoun’s testimony, Petitioner establishes sufficiently that Bertozzi discloses claim 10’s preamble. *See* Pet. 13–23; Ex. 1003 ¶¶ 94, 96–121, 127–130.

(b) Limitation 10.e

Claim 10 recites “identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold.” Ex. 1001, 12:34–37 (limitation 10.e).

Petitioner contends that Bertozzi discloses limitation 10.e because Bertozzi describes:

- (1) “identifying links with a ‘link delay’ that exceeds ‘pre-defined timing requirements (e.g., the desired clock speed of the design)’”; and

¹⁷ For Exhibit 2033 (Local Patent Rule 4-3 Joint Claim Construction and Prehearing Statement), we cite to the page numbers that Patent Owner applied to the exhibit, which are the same as the header page numbers.

- (2) “using pipeline stages to break such long wires into ‘segments whose length can be tailored to the desired clock frequency.’”

Pet. 23–24 (quoting Ex. 1005, 7).

At this stage of the proceeding, Patent Owner makes no arguments specific to limitation 10.e. *See, e.g.*, Prelim. Resp. 23–30.

Based on the current record and for the reasons advanced by Petitioner and supported by Dr. Hassoun’s testimony, Petitioner establishes sufficiently that Bertozzi discloses limitation 10.e. *See* Pet. 23–24; Ex. 1003 ¶¶ 131–132.

(c) Limitation 10.f

Claim 10 recites “in response to the identifying act, inserting $M*N$ data storage elements into the data communication network, M being a positive integer, for introducing a delay of $M*N$ cycles on the first communication channel.” Ex. 1001, 12:38–41 (limitation 10.f).

(i) Petitioner’s Contentions

Petitioner contends that Bertozzi discloses limitation 10.f because Bertozzi describes “inserting ‘repeaters’ into the link to break it up into smaller segments or ‘pipeline stages’” and “repeaters (also called ‘relay stations’) function similarly to a latch in a pipelined data path, and that each stores a single flit (data element) at a time.” Pet. 24–25 (emphasis omitted) (citing Ex. 1003 ¶ 135; Ex. 1005, 7–8, 12, Fig. 4). Petitioner contends that Bertozzi’s Figure 4 discloses:

- (1) a four-flit packet with a fixed length where $N=4$;
- (2) a link between switches with eight repeaters (relay stations) corresponding to the claimed “data storage elements” where $M=2$; and

- (3) “inserting $M*N$ data storage elements . . . for introducing a delay of $M*N$ cycles on the first communication channel” according to limitation 10.f.

Id. at 18–19, 25–26 (alteration by Petitioner) (citing Ex. 1003 ¶¶ 77, 118–120, 135–142; Ex. 1005, Fig. 4); *see id.* at 38.

As support for its contentions, Petitioner provides an annotated excerpt from Bertozzi’s Figure 4 as reproduced below (Pet. 26):

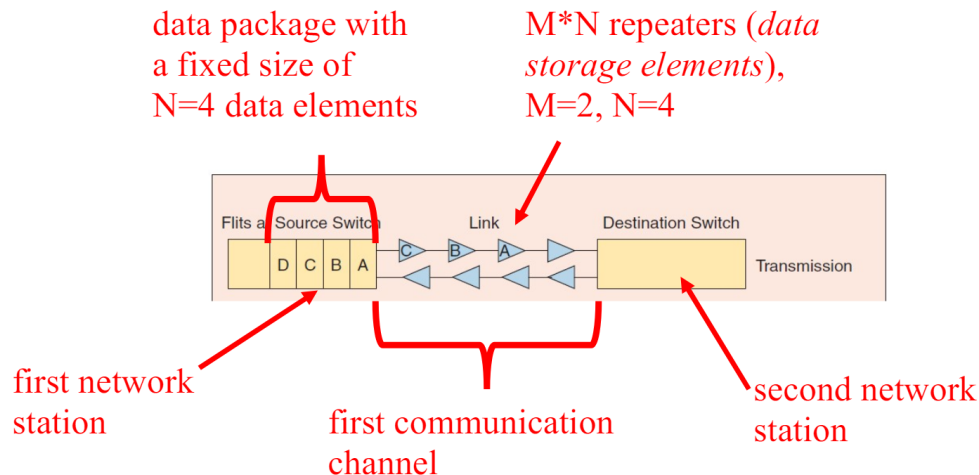


Figure 4 depicts a pipelined link between switches and GO-BACK- N retransmission. *See* Ex. 1005, 7–8. The above annotated excerpt from Figure 4 includes the following annotations:

- (1) the red annotation “first network station” identifying the Source Switch on the left;
- (2) the red annotation “second network station” identifying the Destination Switch on the right;
- (3) the red annotation “first communication channel” identifying the link between the Source Switch and the Destination Switch;
- (4) the red annotation “data package with a fixed size of $N=4$ data elements” identifying the four flits labeled A, B, C, and D at the Source Switch; and

- (5) the red annotation “M*N repeaters (*data storage elements*), M=2, N=4” identifying the eight repeaters (relay stations) in the link between the Source Switch and the Destination Switch.

Pet. 26 (emphasis in original); *see* Ex. 1003 ¶ 137.

According to Petitioner, “Figure 4 shows 8 total repeaters, divided equally between the path from the Source Switch to the Destination Switch and the path from the Destination Switch to the Source Switch.” Pet. 26. Petitioner asserts that “Bertozzi explains that each repeater causes a delay of one clock cycle.” *Id.* Petitioner also asserts that “the repeaters in Figure 4 introduce a delay of 8 cycles (M*N cycles, where M=2 and N=4).” *Id.* (emphasis omitted) (citing Ex. 1003 ¶¶ 137–139; Ex. 1005, 7–9).

Additionally, Petitioner contends that even if the four flits shown in Figure 4 are not a packet, an ordinarily skilled artisan would “at once envisage that the example of the fixed-length packets taught by Bertozzi corresponds to a data package having four flits A, B, C, D (each one a data element) as shown in Figure 4.” Pet. 19 (citing Ex. 1003 ¶¶ 118–120).

(ii) Patent Owner’s Contentions

Patent Owner disputes that Bertozzi discloses limitation 10.f. *See* Prelim. Resp. 23–30. In particular, Patent Owner contends that Bertozzi “does not disclose or suggest that the quantity of repeater stages (e.g., data storage elements) inserted onto a link (e.g., channel) is a function of (or correlates with) the quantity of flits (e.g., data elements) in a packet (e.g., data package).” *Id.* at 26 (citing Ex. 2001 ¶ 91); *see id.* at 28 (citing Ex. 2001 ¶ 95).

Patent Owner asserts that Bertozzi “focuses on overcoming an interconnect-delay problem by pipelining interconnects and segmenting

wires into lengths based on desired clock frequencies.” Prelim. Resp. 23 (citing Ex. 1005, 7; Ex. 2001 ¶ 90); *see id.* at 25. Patent Owner asserts that Bertozzi inserts repeater stages into links to “partition links into segments or pipeline stages based on timing requirements” where the length of each segment or stage “can be tailored to the desired clock frequency that needs to be achieved in the design.” *Id.* at 25–26 (quoting Ex. 1005, 7) (citing Ex. 2001 ¶ 91). Patent Owner asserts that an ordinarily skilled artisan would have understood that “the quantity of repeater stages inserted onto a link is a function of (or correlates with) a desired length of each segment.” *Id.* at 26 (citing Ex. 2001 ¶ 91).

Further, Patent Owner asserts that “the purpose behind why the quantity ($M \times N$) of data storage elements is a function of the quantity of data elements (N) in a data package in claim 10 is to ensure that network stations receive routing information within predefined evaluation cycles” to achieve the “goal of aligning data package delivery with routing information evaluation cycles.” Prelim. Resp. 28–29 (citing Ex. 2001 ¶¶ 97–98). According to Patent Owner, “Bertozzi teaches away from this routing-periodicity requirement” by “elaborating that the switches must operate correctly for any arbitrary quantity of repeater stages on a link, i.e., for routing information that arrives at a destination switch in any cycle rather than in only predefined evaluation cycles.” *Id.* at 30 (emphases omitted) (citing Ex. 1005, 7; Ex. 2001 ¶ 98).

Additionally, Patent Owner contends that Bertozzi depicts a complete packet only in Figure 3, in particular, a ten-flit packet containing “three header flits, six payload flits, and one tail flit (which is also considered a payload flit).” Prelim. Resp. 27 (citing Ex. 2001 ¶ 94). Patent Owner

contends that Bertozzi's Figure 4 does not disclose or suggest a four-flit packet. *Id.* at 26 (citing Ex. 2001 ¶ 94). Patent Owner explains that the four flits labeled A, B, C, and D in Figure 4 may constitute part of a larger packet, such as Figure 3's ten-flit packet, or alternatively parts of "multiple packets," such as "the last two flits of an earlier packet and the first two flits of a later packet." *Id.* at 26–27. According to Patent Owner, Bertozzi "does not disclose or suggest any correlation between the number of repeater stages depicted in FIG. 4 and the number of flits illustrated in the same figure." *Id.* at 28 (citing Ex. 2001 ¶ 95).

Further, Patent Owner asserts that Bertozzi's Figure 3 illustrates a "partitioning procedure" for packets. Prelim. Resp. 27. Based on Figure 3's "partitioning procedure," Patent Owner asserts that "a four-flit packet would consist of three header flits and one tail flit." *Id.* Patent Owner asserts that an ordinarily skilled artisan would have recognized that packet arrangement with "practically no payload" as "rather useless." *Id.* (citing Ex. 2001 ¶ 94). Patent Owner urges the Board to reject Petitioner's interpretation of the four flits labeled A, B, C, and D in Figure 4 as a four-flit packet. *See id.* at 26–27.

(iii) Analysis

Based on the current record, Petitioner does not establish sufficiently for purposes of institution that Bertozzi discloses limitation 10.f. *See* Pet. 24–26; Ex. 1003 ¶¶ 135–139; Ex. 2001 ¶¶ 89–96, 98–100. The claimed "data storage elements" encompass Bertozzi's repeater stages. *See* Ex. 2001 ¶ 91. The claimed "data communication network" encompasses Bertozzi's links. *See* Ex. 1003 ¶¶ 98, 128. Bertozzi does not disclose inserting M*N repeater stages into a link "for introducing a delay of M*N cycles" where M

is a positive integer and N is two or more and corresponds to a fixed number of “data elements” in “each data package” as required by claim 10.

Ex. 1005, 1, 6–8, 12; *see* Ex. 2001 ¶¶ 89–96, 98–100; *supra* § IV.D.3.

Instead, Bertozzi discloses inserting a “flexible number” of repeater stages into a link based on “the clock speed target and link routing” to “overcome the interconnect-delay problem.” Ex. 1005, 1, 7, 12; *see* Ex. 2001 ¶¶ 90–91. Specifically, switch-to-switch links are “subdivided into basic segments whose length can be tailored to the desired clock frequency that needs to be achieved in the design.” Ex. 1005, 7; *see* Ex. 2001 ¶ 91. Thus, “the system operating frequency is not bound by the delay of long links.” Ex. 1005, 7; *see* Ex. 2001 ¶ 91. Pipelining links “with a flexible number of stages” decouples link throughput from link length. Ex. 1005, 1. With suitably designed switches/routers, switch-to-switch links “can be different and of any length.” *Id.* at 7–8; *see* Ex. 2001 ¶¶ 92, 99.

Additionally, Petitioner maps the claimed “data packages” to Bertozzi’s packets and the claimed “data elements” to the flits in Bertozzi’s packets. *See, e.g.*, Pet. 16–20. Bertozzi’s Figure 3 illustrates a single packet partitioned into ten flits. Ex. 1005, 6; *see* Ex. 1003 ¶ 78; Ex. 2001 ¶ 94. Bertozzi does not disclose inserting $M \times 10$ repeater stages into a link “for introducing a delay of $M \times 10$ cycles” where M is a positive integer and 10 corresponds to the number of “data elements” in “each data package” as required by claim 10. *See, e.g.*, Ex. 1005, 1, 6–8, 12; Ex. 2001 ¶ 91. Bertozzi does not describe any correlation between the ten flits in Figure 3’s packet and the number of repeater stages inserted into a link. *See, e.g.*, Ex. 1005, 1, 6–7, 12; Ex. 2001 ¶ 91.

Bertozzi's Figure 4 depicts a pipelined link between switches and GO-BACK-N retransmission. Ex. 1005, 7–8; *see* Ex. 2001 ¶ 93. Figure 4 does not purport to show a packet's structure. *See* Ex. 1005, 7–8.

To depict a pipelined link between switches and GO-BACK-N retransmission, Figure 4 illustrates the following:

- a Source Switch on the left;
- a Destination Switch on the right;
- a link with four repeater stages in the direction from the Source Switch to the Destination Switch and four repeater stages in the direction from the Destination Switch to the Source Switch;
- a sequence of flits at the Source Switch with four of the flits labeled A, B, C, and D from right to left at the Source Switch;
- the Source Switch transmitting flits A, B, C, and D to the Destination Switch;
- the Destination Switch receiving flit A and returning an ACK (ACK=1);
- the Destination Switch receiving corrupt flit B and returning a NACK (ACK=0); and
- the Source Switch retransmitting flits B, C, and D after receiving the NACK.

See Ex. 1005, 7–8. Bertozzi does not indicate that the flits illustrated in Figure 4 constitute a single packet, let alone that the flits expressly labeled A, B, C, and D would be the only flits in that packet. *See, e.g., id.*; Ex. 2001 ¶¶ 93–94.

Indeed, Figure 4 shows five flits at the Source Switch, with the fifth, leftmost flit not labeled. Ex. 1005, 7. Thus, even if Bertozzi intended Figure 4 to illustrate a single packet at the Source Switch, that packet would

have at least five flits, not four flits as Petitioner contends. *See* Pet. 18–19; Ex. 1005, 7.

Additionally, Bertozzi describes the four flits labeled A, B, C, and D in Figure 4 as “[m]ultiple outstanding flits.” Ex. 1005, 8; *see* Ex. 2001 ¶¶ 93–95. In contrast to Figure 3’s ten flits illustrating a single packet, Figure 4’s “[m]ultiple outstanding flits” serve to exemplify GO-BACK-N retransmission where the Destination Switch receives flit A followed by corrupt flit B and then the Source Switch retransmits flits B, C, and D. *See* Ex. 1005, 7–8.

As Dr. Chmelar testifies, Bertozzi does not disclose that “the quantity of repeater stages shown in FIG. 4 has any relationship to the quantity of flits shown in FIG. 4.” Ex. 2001 ¶ 95. As Dr. Chmelar also testifies, an ordinarily skilled artisan most likely would have recognized Figure 4’s “[m]ultiple outstanding flits” as “a portion of a single packet,” i.e., a portion of Figure 3’s ten-flit packet. *Id.* ¶ 94.

Based on the current record, we disagree with Petitioner that an ordinarily skilled artisan would “at once envisage that the example of the fixed-length packets taught by Bertozzi corresponds to a data package having four flits A, B, C, D (each one a data element) as shown in Figure 4.” *See* Pet. 19. Bertozzi discloses that messages “transmitted across the network are usually partitioned into fixed-length packets” and that packets are “often broken into message flow control units called flits.” Ex. 1005, 5; *see* Ex. 2001 ¶ 92.

But Bertozzi does not disclose any limit on the number of flits in a packet. *See, e.g.*, Ex. 1005, 5–8. And Bertozzi does not disclose any limit on the number of repeater stages inserted into a link. *See, e.g., id.* at 1, 3,

6–8, 12; Ex. 2001 ¶¶ 92, 99. Nor does Bertozzi disclose that “the quantity of repeater stages inserted onto a link is a function of the quantity of flits in a packet.” Ex. 2001 ¶ 95. Instead, Bertozzi discloses that the number of repeater stages inserted into a link depends on “the clock speed target and link routing.” Ex. 1005, 7, 12; *see* Ex. 2001 ¶¶ 90–91. Hence, it would not have been immediately apparent to one of ordinary skill in the art to employ a four-flit packet in a network containing links like Figure 4’s link with four repeater stages in each direction between the Source Switch and the Destination Switch.

(d) Conclusion About Anticipation for Claim 10

Based on the current record and for the reasons discussed above, Petitioner does not establish sufficiently for purposes of institution that Bertozzi discloses limitation 10.f when, as Petitioner proposes and the Board agrees, “every data package communicated by the network stations has a fixed size of N data elements.” *See supra* §§ IV.D.2–IV.D.3, IV.E.2(c)(iii). Hence, Petitioner does not demonstrate a reasonable likelihood of proving that claim 10 is unpatentable under § 102(a)–(b) as anticipated by Bertozzi.

3. INDEPENDENT CLAIMS 1 AND 7

Claims 1 and 7 include limitations similar to limitation 10.f. *Compare* Ex. 1001, 12:38–41 (limitation 10.f), *with id.* at 10:42–49 (limitation 1.f), *and id.* at 11:58–62 (limitation 7.f).

Petitioner contends that Bertozzi discloses the limitations in claims 1 and 7 similar to limitation 10.f for the reasons Petitioner contends that Bertozzi discloses limitation 10.f. Pet. 28–29.

Patent Owner disputes that Bertozzi discloses the limitations in claims 1 and 7 similar to limitation 10.f for the reasons Patent Owner disputes that Bertozzi discloses limitation 10.f. Prelim. Resp. 31.

Based on the current record and for the reasons discussed above for limitation 10.f, Petitioner does not establish sufficiently for purposes of institution that Bertozzi discloses the limitations in claims 1 and 7 similar to limitation 10.f. *See supra* § IV.E.2(c)(iii). Hence, Petitioner does not demonstrate a reasonable likelihood of proving that claims 1 and 7 are unpatentable under § 102(a)–(b) as anticipated by Bertozzi.

4. DEPENDENT CLAIMS 2, 3, AND 6

Claims 2, 3, and 6 depend directly or indirectly from claim 1. Ex. 1001, 10:50–63, 11:42–43. Hence, claims 2, 3, and 6 incorporate all the limitations in claim 1. 35 U.S.C. § 112 ¶ 4 (2006).

Based on the current record and for the reasons discussed above for claim 1, Petitioner does not demonstrate a reasonable likelihood of proving that claims 2, 3, and 6 are unpatentable under § 102(a)–(b) as anticipated by Bertozzi. *See supra* § IV.E.3.

F. Alleged Obviousness over Bertozzi: Claims 1–3, 6, 7, and 10

Petitioner contends that claims 1–3, 6, 7, and 10 are unpatentable under § 103(a) as obvious over Bertozzi. *See* Pet. 37–47. Patent Owner disputes Petitioner’s contentions. *See* Prelim. Resp. 32–35.

Above, we provided an overview of Bertozzi. *See supra* § IV.E.1. Below, we consider the obviousness issues. For the reasons explained below, Petitioner does not establish sufficiently for purposes of institution that Bertozzi teaches the subject matter in any of claims 1–3, 6, 7, and 10.

1. INDEPENDENT CLAIMS 7 AND 10

For limitation 10.f and the similar limitation in claim 7, Petitioner relies on its arguments for the anticipation challenge based on Bertozzi to show how Bertozzi teaches the limitations. Pet. 38, 42. Based on the current record and for the reasons discussed above, we consider those arguments unavailing. *See supra* §§ IV.E.2(c)(iii), IV.E.3. Hence, based on the current record, Petitioner does not demonstrate a reasonable likelihood of proving that claims 7 and 10 are unpatentable under § 103(a) as obvious over Bertozzi.

2. INDEPENDENT CLAIM 1

Claim 1 recites “the data communication network further comprising $M*N$ data storage elements, M being a positive integer, the data communication introducing a delay of $M*N$ cycles on the first communication channel when the data communication network identifies the first communication channel as having a data transfer delay exceeding a predefined delay threshold.” Ex. 1001, 10:42–49 (limitation 1.f).

Petitioner contends that “it was well-known that certain networks require packets to arrive at network stations ‘at precisely scheduled time slots.’” Pet. 43 (quoting Ex. 1014, 11:27) (citing Ex. 1003 ¶ 180). Petitioner also contends that “in networks with precisely scheduled time slots, it was known to”:

- (1) “detect delay in a transmission channel (e.g., using ‘probe’ signals) that would result in a packet being received in an inappropriate time slot”; and
- (2) “use data storage elements like those described by Bertozzi to adjust the delay to be an ‘integral multiple of the packet transmission time’ (a delay of $M*N$ cycles) so that the packet arrives in an appropriate time slot.”

Id. at 43–44 (emphases omitted) (quoting Ex. 1014, 11:62) (citing Ex. 1003 ¶ 182).

Further, Petitioner asserts that an ordinarily skilled artisan “would have been motivated to implement this delay detection functionality in the SoC described by Bertozzi to provide an SoC with increased communication functionality” because “doing so would enable the SoC to service communications with precise timing constraints like audio and video data.” Pet. 44 (citing Ex. 1003 ¶ 183).

A “patent can be obvious in light of a single prior art reference if it would have been obvious to modify that reference to arrive at the patented invention.” *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361 (Fed. Cir. 2016). Based on the current record, Petitioner does not establish sufficiently for purposes of institution that Bertozzi teaches or suggests limitation 1.f or that an ordinarily skilled artisan would have modified Bertozzi to arrive at the patented invention.

Based on the current record and for the reasons discussed above for limitation 10.f in the anticipation challenge based on Bertozzi, Petitioner does not establish sufficiently for purposes of institution that Bertozzi teaches or suggests limitation 1.f. *See supra* § IV.E.2(c)(iii).

Further, even if an ordinarily skilled artisan would have been motivated to implement “delay detection functionality” in “the SoC described by Bertozzi,” as Petitioner asserts, Petitioner does not on this record show sufficiently that a skilled artisan would have arrived at the patented invention. *See* Pet. 43–45; Ex. 1003 ¶¶ 179–184. Specifically, Petitioner does not on this record show sufficiently how the “packet transmission time” relates to the “N data elements” in “each data package”

such that adjusting the delay to be an “integral multiple of the packet transmission time” equates to “introducing a delay of $M*N$ cycles” with “ $M*N$ data storage elements” as claimed. *See* Pet. 43–45; Ex. 1001, 10:42–49; Ex. 1003 ¶¶ 179–184.

As an example, a network may experience “poor performance because of localized congestion.” Ex. 1005, 3; *see id.* at 11; Ex. 1006, 42, 94–95;¹⁸ Ex. 1009, 19, 60, 95, 153, 165–68, 172, 175, 196, 223, 248;¹⁹ Ex. 1014, 8:1–3; Ex. 1036, 4:46–55; Ex. 2017, 2:51–53, 6:54–62. “Switches may have internal queues to handle congestion.” Ex. 1006, 9; Ex. 1018, 3. Depending on the level of network congestion, the “packet transmission time” will vary irregularly relative to the “ N data elements” in “each data package.” *See* Ex. 1005, 3, 11; Ex. 1006, 95; Ex. 1009, 19, 60, 95, 153, 165–68, 172, 175, 196, 223, 248. Based on the current record, adjusting the delay to be an “integral multiple of the packet transmission time” does not equate to “introducing a delay of $M*N$ cycles” with “ $M*N$ data storage elements” as claimed.

As another example, a heterogeneous SoC may have a “highly irregular” wire structure with “both short and extremely long switch-to-switch links.” Ex. 1005, 6; *see* Ex. 1003 ¶ 98. Depending on the wire length, the “packet transmission time” will vary irregularly relative to the “ N data elements” in “each data package.” *See* Ex. 1005, 3; *see also*

¹⁸ For Exhibit 1006 (Jantsch), we follow Petitioner’s practice and cite to the page numbers that Petitioner applied to the exhibit rather than the page numbers that appear in the original publication.

¹⁹ For Exhibit 1009 (Duato), we follow Petitioner’s practice and cite to the page numbers that Petitioner applied to the exhibit rather than the page numbers that appear in the original publication.

Ex. 1003 ¶¶ 212–213. Based on the current record, adjusting the delay to be an “integral multiple of the packet transmission time” does not equate to “introducing a delay of $M*N$ cycles” with “ $M*N$ data storage elements” as claimed.

As for Petitioner’s assertion that an ordinarily skilled artisan would have been motivated to implement “delay detection functionality” in “the SoC described by Bertozzi,” Bertozzi does not address the design of SoC building blocks such as “processors, co-processors, DSPs, dedicated hardware accelerators, memory blocks, I/O blocks, etc.” *See* Ex. 1005, 1–13; Pet. 44. Instead, Bertozzi describes NoC design using Xpipes. *See* Ex. 1005, 1–13.

In particular, an XpipesCompiler receives as inputs (1) a file with “information on the network architecture,” (2) routing tables for the network interfaces, and (3) the library of soft macros (switches, network interfaces and links). Ex. 1005, 12; *see id.* at 10 (Fig. 9). Then, the XpipesCompiler outputs “a SystemC hierarchical description, which includes all switches, links, network nodes and interfaces and specifies their connectivity.” *Id.* at 12; *see id.* at 10 (Fig. 9).

Petitioner does not explain how an ordinarily skilled artisan would have modified Xpipes to implement “delay detection functionality” in “the SoC described by Bertozzi.” *See* Pet. 43–45; Ex. 1003 ¶¶ 179–184.

For these reasons, Petitioner does not establish sufficiently for purposes of institution that Bertozzi teaches or suggests limitation 1.f or that an ordinarily skilled artisan would have modified Bertozzi to arrive at the patented invention. Hence, based on the current record, Petitioner does not

demonstrate a reasonable likelihood of proving that claim 1 is unpatentable under § 103(a) as obvious over Bertozzi.

3. DEPENDENT CLAIMS 2, 3, AND 6

Claims 2, 3, and 6 depend directly or indirectly from claim 1. Ex. 1001, 10:50–63, 11:42–43. Hence, claims 2, 3, and 6 incorporate all the limitations in claim 1. 35 U.S.C. § 112 ¶ 4.

Based on the current record and for the reasons discussed above for claim 1, Petitioner does not demonstrate a reasonable likelihood of proving that claims 2, 3, and 6 are unpatentable under § 103(a) as obvious over Bertozzi. *See supra* § IV.F.2.

G. Alleged Obviousness over Bertozzi and Either Jantsch or Duato: Claims 1–3, 6, 7, and 10

Petitioner contends that claims 1–3, 6, 7, and 10 are unpatentable under § 103(a) as obvious over Bertozzi and either Jantsch or Duato. *See* Pet. 37–47. Patent Owner disputes Petitioner’s contentions. *See* Prelim. Resp. 32–35.

Above, we provided an overview of Bertozzi. *See supra* § IV.E.1. Below, we provide overviews of Jantsch and Duato. Then, we consider the obviousness issues. For the reasons explained below, Petitioner does not establish sufficiently for purposes of institution that the combined disclosures in Bertozzi and either Jantsch or Duato teach the subject matter in any of claims 1–3, 6, 7, and 10.

1. OVERVIEW OF JANTSCH (EXHIBIT 1006)

Jantsch is a book titled “Networks on Chip” edited by Axel Jantsch and Hannu Tenhunen, published by Kluwer Academic Publishers in 2003. Ex. 1006, 1–3; Ex. 1021 ¶¶ 41–47. Jantsch addresses “design and

methodology issues” for NoCs and “hardware infrastructure,” such as “network topology, power management, fault tolerance, testing and clocking, among other topics.” Ex. 1006, 5.

Jantsch describes adapting “the concept of packet switched communication from computer networks to design on-chip networks” so that “the cores on the chip communicate among themselves by sending packets using a network of switches.” Ex. 1006, 47. According to Jantsch, however, “the geometrical and electrical conditions are very different when dealing with on chip communication as compared to devices connected by cables to Internet.” *Id.* at 56.

Jantsch identifies “the message sizes and variation in the message sizes” as a “major difference in the two networks.” Ex. 1006, 56. Jantsch explains that “the message size for on-chip communication is going to vary between 1 byte to a few thousand bytes, with an average being a number much smaller than 100.” *Id.* “Therefore, choosing a fixed packet size with a payload of eight will be efficient as compared to a variable packet size.” *Id.*

2. OVERVIEW OF DUATO (EXHIBIT 1009)

Duato is a book titled “Interconnection Networks: An Engineering Approach” by José Duato, Sudhakar Yalamanchili, and Lionel Ni, published by the IEEE Computer Society Press in 1998. Ex. 1009, 1–5; Ex. 1021 ¶¶ 48–55. Duato provides “a comprehensive treatment of interconnection networks from topology, through routing and flow control, to a discussion of the software layer.” Ex. 1009, 7. Duato addresses “issues that should be taken into account by the designer” and presents “a broad set of solutions proposed in the literature” for those issues. *Id.*

Duato describes flow control as “a synchronization protocol for transmitting and receiving a unit of information.” Ex. 1009, 32. “The unit of flow control refers to that portion of the message whose transfer must be synchronized.” *Id.* Each message “may be partitioned into fixed-length *packets*,” and packets “may be broken into message flow control units or *flits*.” *Id.* at 32–33 (emphases in original).

Duato explains that “it is easy to think of messages in terms of fixed-length packets.” Ex. 1009, 32. A “packet is forwarded across a physical channel or from the input buffers of a router to the output buffers.” *Id.* But “sufficient buffering must be provided so that a packet is either transferred in its entirety, or transmission is delayed until sufficient buffer space becomes available.” *Id.*

3. INDEPENDENT CLAIMS 1, 7, AND 10

“To the extent [Patent Owner] argues that Bertozzi does not disclose that every packet in its NoC has the same” fixed length, Petitioner asserts that fixed-length data packages “would have been obvious in view Duato or Jantsch” because Duato and Jantsch each teach “designing and using systems for fixed packet size.” Pet. 38 (citing Ex. 1003 ¶¶ 84–87, 165–176; Ex. 1006, 56; Ex. 1009, 32). Petitioner also asserts that an ordinarily skilled artisan “would have found it obvious to design, and for the integrated circuit disclosed by Bertozzi to use, data packages, each having a fixed-length of four data elements like the data package” identified as A, B, C, and D in Bertozzi’s Figure 4. *Id.* (emphases omitted).

Petitioner does not cite Jantsch or Duato as teaching limitation 10.f and the similar limitations in claims 1 and 7 when considering each reference alone or in combination with Bertozzi. *See* Pet. 38–47.

Based on the current record and for the reasons discussed above, Petitioner does not establish sufficiently for purposes of institution that Bertozzi teaches or suggests limitation 10.f and the similar limitations in claims 1 and 7. *See supra* §§ IV.E.2(c)(iii), IV.E.3, IV.F.1–IV.F.2. Additionally, Petitioner does not show how either Jantsch or Duato remedies the deficiencies in Bertozzi with respect to claims 1, 7, and 10. *See* Pet. 38–47. Hence, Petitioner does not demonstrate a reasonable likelihood of proving that claims 1, 7, and 10 are unpatentable under § 103(a) as obvious over Bertozzi and either Jantsch or Duato.

4. DEPENDENT CLAIMS 2, 3, AND 6

Claims 2, 3, and 6 depend directly or indirectly from claim 1. Ex. 1001, 10:50–63, 11:42–43. Hence, claims 2, 3, and 6 incorporate all the limitations in claim 1. 35 U.S.C. § 112 ¶ 4.

Based on the current record and for the reasons discussed above for claim 1, Petitioner does not demonstrate a reasonable likelihood of proving that claims 2, 3, and 6 are unpatentable under § 103(a) as obvious over Bertozzi and either Jantsch or Duato. *See supra* § IV.G.3.

H. Alleged Obviousness over Dielissen and Hassoun: Claims 1–3, 6, 7, 9, and 10

Petitioner contends that claims 1–3, 6, 7, 9, and 10 are unpatentable under § 103(a) as obvious over Dielissen and Hassoun. *See* Pet. 47–77. Patent Owner disputes Petitioner’s contentions. *See* Prelim. Resp. 35–49.

Below, we provide overviews of Dielissen and Hassoun. Then, we consider the obviousness issues. For the reasons explained below, Petitioner does not establish sufficiently for purposes of institution that the combined

disclosures in Dielissen and Hassoun teach the subject matter in any of claims 1–3, 6, 7, 9, and 10.

1. OVERVIEW OF DIELISSSEN (EXHIBIT 1007)

Dielissen is a paper titled “Concepts and Implementation of the Philips Network-on-Chip” by John Dielissen, Andrei Rădulescu, Kees Goossens, and Edwin Rijpkema, published at a workshop called IP Based SoC Design 2003 in November 2003. Ex. 1007, 1; Ex. 1022 ¶¶ 2–3. Dielissen describes the “Æthereal network on chip (NoC)” consisting of routers and network interfaces (NIs). Ex. 1007, 1. “The NIs are responsible for packetization/depacketization, for implementing the connections and services, and for offering a standard interface” to the “modules connected to the NoC.” *Id.* “The routers transport packets of data from one NI to another.” *Id.*

Dielissen's Figure 1 (reproduced below) depicts an example *Æ*thereal NoC:

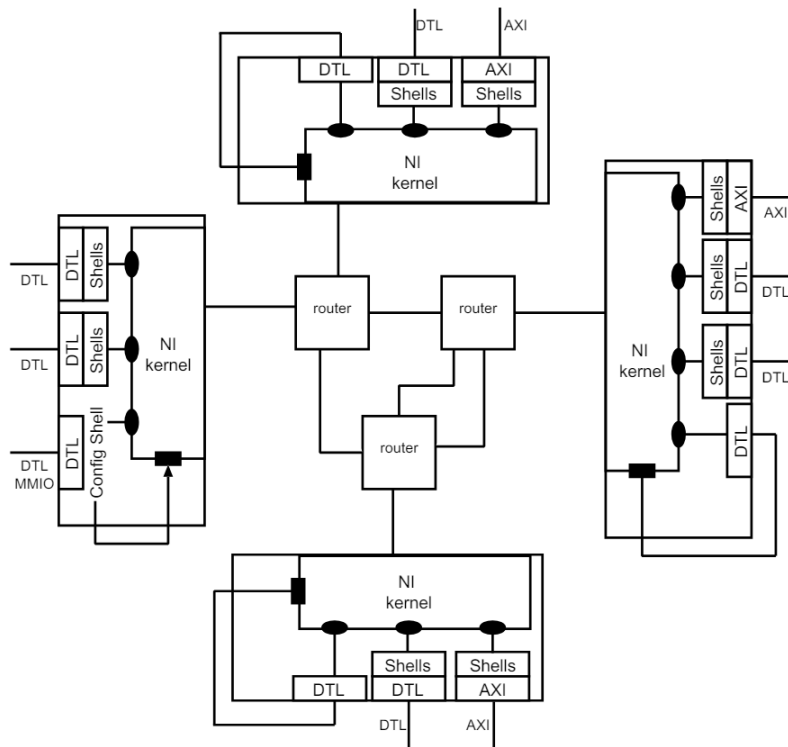


Figure 1. network example

Figure 1 illustrates an example *Æ*thereal NoC with three routers and four NIs where each NI includes a kernel and shells. Ex. 1007, 1–2. “The NI kernel provides the basic functionality, including arbitration between connections, ordering, end-to-end flow control, packetization, and a link protocol with the router.” *Id.* at 1; *see id.* at 3, 6. The NI shells implement “additional functionality,” such as “multicast and narrowcast connections,” and “adaptors to existing protocols.” *Id.* at 1; *see id.* at 3, 6.

The *Æ*thereal NoC allows for “differentiated traffic classes,” e.g., for best-effort (BE) data and guaranteed-throughput (GT) data. *See* Ex. 1007, 1–3, 6. To implement guarantees, the NoC employs a “time-division-multiplexed circuit-switching approach” where one or more circuits “are

created by reserving consecutive slots in consecutive routers/NIs.” *Id.* at 1; *see id.* at 6. For BE data, “no throughput guarantees are given.” *Id.* at 2.

By reserving consecutive slots for GT data, “no more than one GT data is scheduled at the same time on an output port of a router or NI.”

Ex. 1007, 2. “BE data is transferred on the slots that are not used by the GT data: either the slots are unreserved, or the slots are reserved, but not used.”

Id. “BE data can be delayed because of the higher priority GT data, or because of contention on the ports.” *Id.*

A “network packet is build [sic] up of one or more network flits” where the “flit is the minimal transmission unit.” Ex. 1007, 2. The “flit size is chosen 3” to “optimize the data clock frequency and control frequency.” *Id.* Packets “have a maximum length to avoid links being used exclusively by a packet/channel, leading to congestion.” *Id.* at 4.

Dielissen’s Figure 3 (reproduced below) depicts a flit format:

id	credit	qid	path
size	payload 0		
eop	payload 1		

Figure 3. Network flits

Figure 3 illustrates a flit with three words, i.e., the “flit size is chosen 3.”

Ex. 1007, 2–3.

The first flit in a packet includes a packet header as the first word and two payload words. Ex. 1007, 2. The next flits in the packet may include three payload words. *Id.* The last flit in the packet may include two payload words and an end-of-packet (eop) flag associated with the third word. *Id.*

A packet header includes the following information:

- (1) “the path on which the packet travels,” i.e., “a list of destination ports” for each of the routers on the path (“path” in Figure 3);
- (2) “remote queue id” for identifying “the queue of the remote network interface in which the data will be stored” (“qid” in Figure 3); and
- (3) “credit” data for tracking “empty buffer space” (“credit” in Figure 3).

Ex. 1007, 2–4.

Only “the first flit of a packet” includes a packet header. Ex. 1007, 2. Hence, “when packets consist of multiple flits, the overhead of the header is reduced.” *Id.*

Additionally, an “id” field in each flit identifies the “type of flit” as either a GT-flit or a BE-flit. Ex. 1007, 2–3. In the *Æthereal* NoC, schedulers and controllers prioritize GT-flits over BE-flits. *See id.* at 2–4. The “GT-flits are always scheduled for the next cycle.” *Id.* at 2. “After scheduling the GT-flits, the remaining destination ports can serve the BE-flits.” *Id.* at 3. The “BE-flits are scheduled to the remaining destination ports according a round-robin schedule.” *Id.* at 2; *see id.* at 6.

Further, a “size” field in each flit specifies the “amount of valid words in the flit.” Ex. 1007, 2.

Dielissen's Figure 4 (reproduced below) depicts an example packet:

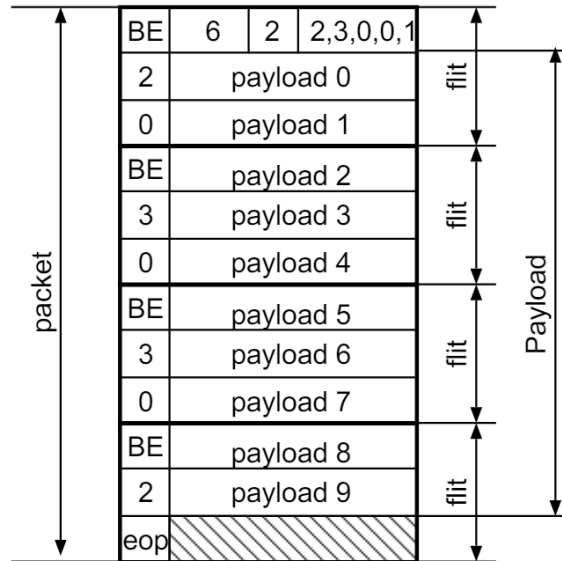


Figure 4. BE-packet example

Figure 4 illustrates an example BE-packet with four flits where each flit has three words and:

- (1) the first flit (i) includes a packet header as the first word, (ii) includes two payload words, and (iii) has the number “2” in the “size” field;
- (2) the second flit (i) lacks a packet header, (ii) includes three payload words, and (iii) has the number “3” in the “size” field;
- (3) the third flit (i) lacks a packet header, (ii) includes three payload words, and (iii) has the number “3” in the “size” field; and
- (4) the fourth flit (i) lacks a packet header, (ii) includes two payload words, (iii) has the number “2” in the “size” field, and (iv) has an eop flag associated with the third word.

Ex. 1007, 3. As shown in Figure 4, the example BE-packet includes ten payload words identified as payload 0 through payload 9. *Id.* at 2–3.

2. OVERVIEW OF HASSOUN (EXHIBIT 1011)

Hassoun is a paper titled “Optimal Buffered Routing Path Constructions for Single and Multiple Clock Domain Systems” by Soha Hassoun, Charles J. Alpert, and Meera Thiagarajan, published at the IEEE/ACM International Conference on Computer Aided Design in November 2002. Ex. 1011, 1;²⁰ Ex. 1024 ¶¶ 8–11. Hassoun explains that shrinking geometries and the increasing use of “IP (Intellectual Property) components,” e.g., “embedded processors and memories,” in SoCs present “new problems in routing and buffer insertion.” Ex. 1011, 1.

For instance, “cross-chip routing will require multiple clock cycles.” Ex. 1011, 1; *see id.* at 2. Also, a “shortest path for a signal between two chip components” may be “obstructed by IP blocks.” *Id.* at 1. Further, “if the IPs are clocked at different frequencies, as is the case with hard IP that often has a fixed clock period, then the signal route must cross from one time domain (of the sender) to another (that of the receiver) latched through the proper circuitry.” *Id.*

Hassoun “addresses two problems related to routing and buffering” in SoC designs. Ex. 1011, 1. First, for a single-clock-domain system, Hassoun seeks to provide “an optimal buffered-routing path” with synchronizer insertion and buffer insertion to “minimize the *cycle latency*, or equivalently, the total number of registers along the route.” *Id.* (emphasis in original); *see id.* at 2. Second, for a multiple-clock-domain system, Hassoun seeks to provide “an optimal routed path between two signals in different clock

²⁰ For Exhibit 1011 (Hassoun), we follow Petitioner’s practice and cite to the page numbers that Petitioner applied to the exhibit rather than the page numbers that appear in the original publication.

domains” by considering “simultaneous routing, buffer insertion, relay stations insertion, and MCFIFO insertion to achieve the minimum *time latency*.”²¹ *Id.* (emphasis in original). The MCFIFO “is the basic entity that establishes data communication between two modules operating at different frequencies.” *Id.* at 4.

For solving these problems, Hassoun identifies three algorithms: the Fast Path algorithm, the Registered-Buffered Path (RBP) algorithm, and the Globally Asynchronous, Locally Synchronous (GALS) algorithm. *See* Ex. 1011, 1–6. The Fast Path algorithm and the RBP algorithm relate to single-clock-domain systems. *Id.* at 2–4. The GALS algorithm relates to multiple-clock-domain systems. *Id.* at 4–6. The GALS algorithm differs from the RBP algorithm primarily because the GALS algorithm includes a step for “inserting MCFIFO elements.” *Id.* at 6.

The Fast Path algorithm “finds the minimum delay source-to-sink buffered routing path, while considering both physical obstacles (e.g., due to IP, memories, and other macro blocks) and wiring blockages (e.g., data path).” Ex. 1011, 2. The RBP algorithm adapts the Fast Path algorithm to consider candidate propagation “in waves of partial solutions wherein each wave corresponds to a different number of registers.” *Id.* at 3.

²¹ The acronym “MCFIFO” stands for “Multi-Clock First In, First Out.”

Hassoun's Figures 1 and 4 (reproduced below) depict the Fast Path algorithm and the RBP algorithm, respectively:

Fast Path (G, B, s, t, m') Input: $G(V, E) \equiv$ Routing grid graph $B \equiv$ Buffer library $s \equiv$ source node $t \equiv$ sink node $m' \equiv$ initial labeling Vars: $Q \equiv$ priority queue of candidates $\alpha = (c, d, m, v) \equiv$ Candidate at v Output: $m \equiv$ Complete labeling of s-t path 1. $Q \leftarrow \{(C(m'(t)), 0, m', t)\}$. 2. while ($Q \neq \emptyset$) do 3. $(c, m, b, u) \leftarrow \text{extract_min}(Q)$ 4. if $c = 0$ then return labeling m. 5. if $u = s$ then $d' \leftarrow d + R(m(s)) \cdot c + K(m(s))$ push $(0, d', m, u)$ onto Q and prune. continue 6. for each $(u, v) \in E$ do $c' \leftarrow c + C(u, v)$ $d' \leftarrow d + R(u, v)(c + C(u, v))/2$ push (c', d', m, v) onto Q and prune 7. if $p(u) = 1$ and $m(u) = 0$ then 8. for each $b \in B$ do $c' \leftarrow C(b)$ $d' \leftarrow d + R(b) \cdot c + K(b)$ $m(u) = b$ push (c', d', m, v) onto Q and prune	RBP Algorithm ($G, B, s, t, m', r, T_\phi$) Input: $G(V, E) \equiv$ Routing grid graph $B \equiv$ Buffer library $s \equiv$ source node $t \equiv$ sink node $m' \equiv$ initial labeling with $m'(s) = m'(t) = r$ $r \equiv$ register for clocking signal $T_\phi \equiv$ required clock period. Vars: $Q \equiv$ priority queue of candidates $Q^* \equiv$ queue holding next candidate wave $\alpha = (c, d, m, v) \equiv$ Candidate at v $A \equiv$ Marking of registered nodes Output: $m \equiv$ Labeling of complete s-t path 1. $Q \leftarrow \{(C(r), \text{Setup}(r), m', t)\}$. $Q^* = \emptyset, A(v) = 0, \forall v \in V$ 2. while ($Q \neq \emptyset$) and ($Q^* \neq \emptyset$) do if ($Q = \emptyset$) then $Q = Q^*, Q^* = \emptyset$. 3. $(c, d, m, u) \leftarrow \text{extract_min}(Q)$ 4. if $u = s$ then $d' \leftarrow d + R(m(s)) \cdot c + K(m(s))$ if $d' \leq T_\phi$ then return labeling m. 5. for each $(u, v) \in E$ do $c' \leftarrow c + C(u, v)$ $d' \leftarrow d + R(u, v)(c + C(u, v))/2$ if $d' \leq T_\phi - K(r) - \min(R(B \cup r))c'$ then push (c', d', m, v) onto Q and prune 6. if $p(u) = 1$ and $m(u) = 0$ then 7. for each $b \in B$ do $c' \leftarrow C(b), m(u) = b$ $d' \leftarrow d + R(b) \cdot c + K(b)$ if $d' \leq T_\phi - K(r)$ then push (c', d', m, u) onto Q and prune 8. if $A(u) = 0$ and $d + R(r) \cdot c + K(r) \leq T_\phi$ then $m(u) = r, A(u) = 1$ push $(C(r), \text{Setup}(r), m, u)$ onto Q^*
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Figure 1. The Fast Path algorithm.

Figure 4. The Registered Buffered Path algorithm.

Above on the left, Figure 1 illustrates pseudo-code for the Fast Path algorithm. Ex. 1011, 2. Above on the right, Figure 4 illustrates pseudo-code for the RBP algorithm. *Id.* at 4.

Hassoun explains that when cross-chip routing in a single-clock-domain system requires multiple clock cycles, “one must periodically clock

the signal by inserting synchronization elements (such as registers) along signal path.” Ex. 1011, 2–3. When solving the problem of determining “the minimum buffer-register path” from a source node s to a sink node t , an algorithm should at least find “a feasible buffer-register path from s to t such that the latency from s to t is minimized.” *Id.* at 3; *see id.* at 2.

Hassoun’s Figure 2 (reproduced below) depicts an example buffer-register path from a source node s to a sink node t in a single-clock-domain system:

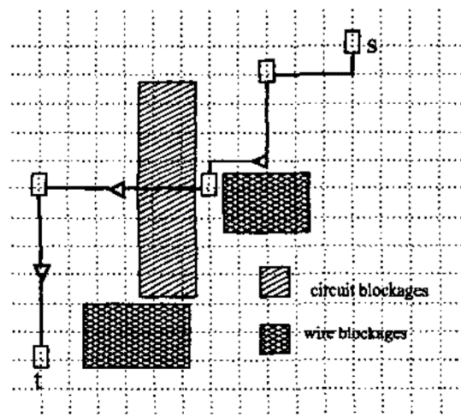


Figure 2. An example of routing within a single clock domain

Figure 2 illustrates a grid graph with circuit blockages and wire blockages and an example path from a source node s to a sink node t including three registers between the nodes. Ex. 1011, 3.

A “register releases its signal with clock cycle.” Ex. 1011, 3. In Figure 2, “[t]he s - t path has three registers between s and t ,” and traversing from s to t requires four clock cycles. *Id.*

3. INDEPENDENT CLAIM 10

Claim 10 recites “a data communication network comprising a plurality of network stations being interconnected via a plurality of

communication channels for communicating data packages between the functional blocks.” Ex. 1001, 12:23–26 (preamble 10.pre.b). Claim 10 also recites “each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two.” *Id.* at 12:27–29 (preamble 10.pre.c). Claim 10 further recites “in response to the identifying act, inserting M*N data storage elements into the data communication network, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel.” *Id.* at 12:38–41 (limitation 10.f).

(a) Petitioner’s Contentions

Petitioner contends that Dielissen teaches “data packages” according to claim 10 where “each data package compris[es] N data elements including a data element comprising routing information for the network stations, N being an integer of at least two.” Pet. 51–57. Specifically, Petitioner identifies the example four-flit packet in Dielissen’s Figure 4 where each flit has three words and the first word in the first flit includes a packet header. *Id.* at 54–55, 65. Petitioner maps the claimed “data packages” to the flits in that example four-flit packet. *Id.* at 54. Petitioner maps the claimed “N data elements” in “each data package” to the three words in each flit such that N=3 and has a fixed value. *Id.* at 54–55, 65.

To support its position, Petitioner provides an annotated version of Dielissen’s Figure 4 as reproduced below (Pet. 55):

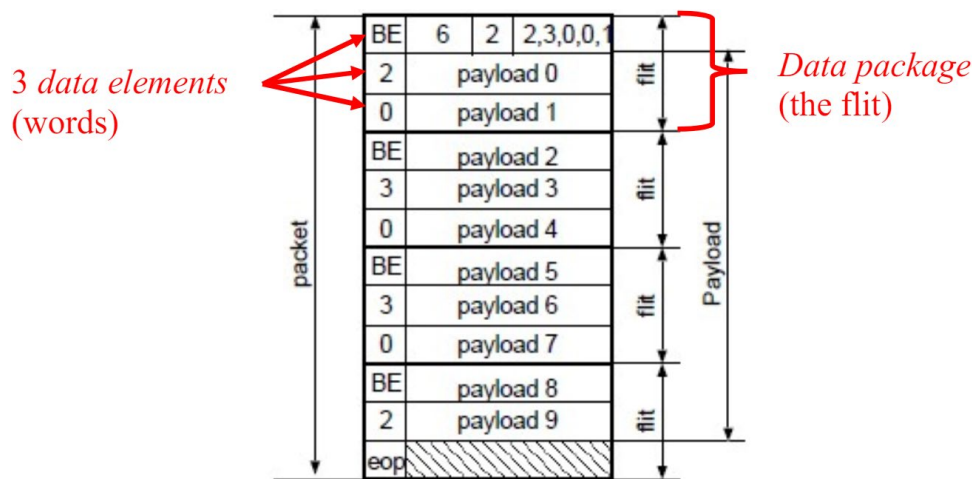


Figure 4 illustrates an example best-effort (BE) packet with four flits where each flit has three words and (a) the first word in the first flit includes a packet header, (b) the next ten words include payload information identified as payload 0 through payload 9, and (c) the last word in the last flit has an end-of-packet (eop) flag. Ex. 1007, 2–3. The above annotated version of Figure 4 includes the following annotations:

- (1) the red annotation “*Data package (the flit)*” identifying the first flit in the four-flit packet; and
- (2) the red annotation “*3 data elements (words)*” identifying the three words in the first flit.

Pet. 55 (emphases in original); *see* Ex. 1003 ¶ 202.

Claim 10 specifies that “each data package” includes “a data element comprising routing information for the network stations.” Ex. 1001, 12:27–29. Petitioner contends that “Dielissen discloses a data element comprising routing information for the network stations in the same way as” the ’893 patent. Pet. 55; *see id.* at 55–57.

Specifically, Petitioner asserts that “routing information” according to the ’893 patent includes “destination and required service type (e.g. best effort or guaranteed bandwidth).” Pet. 55 (quoting Ex. 1001, 2:22–24) (citing Ex. 1003 ¶ 203). Petitioner then cites the following disclosure in the ’893 patent about router memory operation relating to service level that allows interleaving data packages in different data streams over a single communication channel:

Typically, the header of a first data package will comprise information about the destination of the data package as well as the service level of the data package, e.g. guaranteed bandwidth or best effort service. The service level will be flagged by setting a bit in the appropriate memory element of the destination output port of the data router. For subsequent data packages having the same service level, the data router will know that these data packages belong to a data stream in progress because the appropriate bit has been stored in the associated memory element. The last data package of the data stream contains an indicator causing the data router to reset said bit.

Id. at 55–56 (citing Ex. 1001, 5:29–38); Ex. 1001, 5:29–40.

Petitioner asserts that Dielissen similarly discloses that:

- (1) “the first word of a packet is a packet header that contains the routing path, the packet id, and the flit type”; and
- (2) subsequent flits in the packet include (i) a flit-type field indicating “whether the flit is a guaranteed throughput or best effort” and (ii) “an end of packet (‘eop’) flag in the sideband information.”

Pet. 56 (citing Ex. 1003 ¶ 204; Ex. 1007, 2–3). According to Petitioner, the flit-type field “is like the service type” described in the ’893 patent, and the

one clock cycle on the channel.” Pet. 63 (citing Ex. 1003 ¶¶ 89, 211, 219; Ex. 1011, 3). Petitioner also contends that inserting three repeaters into the communication channel results in introducing a delay of three cycles on the communication channel. *Id.* (citing Ex. 1003 ¶¶ 89, 220).

In short, Petitioner asserts that the combined disclosures in Dielissen and Hassoun teach limitation 10.f because:

- (1) Dielissen teaches the claimed “data packages” with $N=3$ “data elements”;
- (2) Hassoun teaches the claimed “data storage elements” where $M=1$ and $N=3$; and
- (3) Hassoun teaches introducing a delay of $M*N$ cycles ($1*3=3$ cycles) on a communication channel.

Pet. 65 (citing Ex. 1001, 3:50–51; Ex. 1003 ¶ 225); *see id.* at 65–66.

According to Petitioner, an ordinarily skilled artisan “would have expected this known option” of introducing a delay according to Hassoun “to predictably improve Dielissen.” Pet. 66 (citing Ex. 1003 ¶ 225).

Further, Petitioner asserts that “it was known to adjust the ‘transmission delay between adjacent nodes to be equal to an integral number of packet transmission times’ allowing each node to know ‘when to expect the header’ of the packet.” Pet. 64 (quoting Ex. 1014, 6:58–60, 6:66) (citing Ex. 1003 ¶ 223). According to Petitioner, an ordinarily skilled artisan would have understood that:

- (1) the transmission time for a “data package” in Dielissen, i.e., a three-word flit, “would be the number of words in the flit, i.e., $N=3$ cycles”; and
- (2) adding “an integer multiple of 3 cycles of delay would thus require an integer multiple of 3 repeaters placed into the communication channel (i.e. 3 repeaters, 6 repeaters, or 9 repeaters, etc.).”

Id. (citing Ex. 1003 ¶¶ 223–224; Ex. 1007, 2).

(b) Patent Owner’s Contentions

Patent Owner disputes that the combined disclosures in Dielissen and Hassoun teach limitation 10.f. *See* Prelim. Resp. 35–48. In particular, Patent Owner contends that Dielissen discloses a packet with a flit size of three words chosen to “optimize the data clock frequency and control frequency.” *Id.* at 36 (quoting Ex. 1007, 2). Patent Owner contends that Dielissen “does not disclose or suggest any need or desire to find a path with the minimum delay, at least because the selection of a flit size of three had already optimized the data and control frequencies for the *Æthereal* NoC.” *Id.* at 36–37 (citing Ex. 1007, 2; Ex. 2001 ¶ 108).

Patent Owner asserts that Hassoun’s Fast Path algorithm and RBP algorithm lack “any indication or suggestion that a size or length of” a packet or flit provides an input “indicating that a data package comprises *N* data elements.” Prelim. Resp. 38–39, 41, 48 (citing Ex. 2001 ¶¶ 110, 113, 116). Patent Owner asserts that Hassoun’s algorithms do not account for the size or length of a packet or flit “when calculating their outputs (the alleged *M***N* data storage elements).” *Id.* at 39, 41, 48 (citing Ex. 2001 ¶¶ 110, 113, 116). Patent Owner also asserts that Hassoun’s algorithms “do not produce their outputs (the alleged *M***N* data storage elements) according to a packet length or a flit length (the alleged *N* data elements of a data package).” *Id.* at 41–42 (citing Ex. 2001 ¶ 113).

Further, Patent Owner asserts that Hassoun’s Figure 2 “simply discloses an example routing that is arbitrarily illustrated with some quantity (three) of registers.” Prelim. Resp. 39 (citing Ex. 2001 ¶ 111). Patent

Owner asserts that “Hassoun is silent as to the rationale behind choosing the three registers” in Figure 2. *Id.* at 40.

Additionally, Patent Owner contends that because Hassoun’s algorithms “do not take into account the size or length of” a packet or flit, there is no basis for an ordinarily skilled artisan “to infer any relationship between the number of three registers depicted in Hassoun’s Figure 2 and the number of flits within a data packet.” Prelim. Resp. 40 (citing Ex. 2001 ¶¶ 111–112). Patent Owner also contends that the “arbitrary number of registers shown in Hassoun’s Figure 2 lacks any concrete association with the flits or words disclosed in Dielissen’s data packet.” *Id.* (citing Ex. 2001 ¶ 112).

(c) Analysis

Based on the current record, Petitioner does not establish sufficiently for purposes of institution that the combined disclosures in Dielissen and Hassoun teach or suggest claim 10’s subject matter. *See* Pet. 50–67; Ex. 1003 ¶¶ 190–205, 209–226; Ex. 2001 ¶¶ 107–116. Initially, based on the current record, we disagree with Petitioner that Dielissen discloses “data packages” according to claim 10 where “each data package” comprises “N data elements including a data element comprising routing information for the network stations, N being an integer of at least two.” *See* Pet. 51–57.

According to the ’893 patent, “routing information” includes at least “destination” information. *See* Ex. 1001, 2:22–26, 4:53–56, 4:58–64, 5:29–32. Regarding “routing information,” the patent states, “The routing information, e.g. destination and required service type (e.g. best effort or guaranteed bandwidth) has a fixed position in the data package, e.g. the first data element (i.e. a header), although other data elements may (also) contain

such information.” *Id.* at 2:22–26; *see id.* at 5:29–32. The patent also states, “At least one of the N data elements in a package, e.g. the first data element, comprises routing instructions for the destination network station.” *Id.* at 4:53–56.

The “service type” or “service level” information in a data package does not indicate a route through a network or a destination. For instance, different data packages destined for different network nodes may have the same “service type” or “service level” information but different “destination” information. As a specific example, data package A destined for node X may have “guaranteed bandwidth” as the “service type,” and data package B destined for node Y may also have “guaranteed bandwidth” as the “service type.” *See* Ex. 1001, 3:31–33. Thus, the “service type” or “service level” information in a data package does not alone constitute “routing information.” *See* Ex. 1001, 2:22–26, 4:53–56, 4:58–64, 5:29–34.

Additionally, the ’893 patent distinguishes “routing information” from “service type” or “service level” information when explaining how a network station may interleave data packages “requiring different service levels” as follows:

Each network station may comprise a first memory element and a second memory element associated with a communication port of said network station, the first memory element being arranged to store routing information from a data package requiring a first service level associated with said communication port and the second memory element being arranged to store routing information from a data package requiring a second service level associated with said communication port. Such an implementation allows for the interleaving of packages requiring different service levels, e.g. best effort and guaranteed bandwidth service levels.

Ex. 1001, 3:23–33.

Dielissen’s Figure 4 illustrates an example BE-packet with four flits where each flit has three words and:

- (1) the first flit (i) includes a packet header as the first word, (ii) includes two payload words, and (iii) has the number “2” in the “size” field;
- (2) the second flit (i) lacks a packet header, (ii) includes three payload words, and (iii) has the number “3” in the “size” field;
- (3) the third flit (i) lacks a packet header, (ii) includes three payload words, and (iii) has the number “3” in the “size” field; and
- (4) the fourth flit (i) lacks a packet header, (ii) includes two payload words, (iii) has the number “2” in the “size” field, and (iv) has an eop flag associated with the third word.

Ex. 1007, 3.

Dielissen explains that a packet header includes “the path on which the packet travels,” i.e., “a list of destination ports” for each of the routers on the path. Ex. 1007, 2. Hence, a packet header in a Dielissen packet includes “routing information” according to the ’893 patent. *See* Ex. 1001, 2:22–26, 4:53–56, 4:58–64. But Dielissen also explains that only “the first flit of a packet” includes a packet header. Ex. 1007, 2.

Based on the current record, we disagree with Petitioner that (1) the flit-type field in a Dielissen packet contains “routing information” according to the ’893 patent and (2) an eop flag constitutes “routing information” according to the ’893 patent. *See* Pet. 55–57; Ex. 1003 ¶¶ 203–205.

Regarding the flit-type field in a Dielissen packet, Dielissen explains that an “id” field identifies the “type of flit” as either a GT-flit or a BE-flit to permit

prioritizing GT-flits over BE-flits. *See* Ex. 1007, 2–4. But identifying the “type of flit” as either a GT-flit or a BE-flit does not indicate a route through a network or a destination.

For instance, different flits destined for different network nodes may have the same flit type but different path information in the respective packet headers. So the information in the “id” field in a Dielissen packet does not alone constitute “routing information” according to the ’893 patent.

Although the *Æthereal* NoC may use the information in the “id” field together with a packet header’s path information to assist with output port selection, that does not mean that the information in the “id” field alone suffices as “routing information” according to the ’893 patent. *See* Ex. 1007, 2–4.

Moreover, based on the current record, Petitioner does not explain how an eop flag indicates a route through a network or a destination and, therefore, constitutes “routing information” according to the ’893 patent. *See* Pet. 55–57; Ex. 1003 ¶¶ 203–205.

Based on the current record, only the first flit in a Dielissen packet includes a packet header and “routing information” according to the ’893 patent. *See* Ex. 1001, 2:22–26, 4:53–56, 4:58–64; Ex. 1007, 2–4. The other flits in a Dielissen packet lack a packet header and “routing information” according to the ’893 patent. As Dielissen’s Figure 4 shows, the second, third, and fourth flits in the example four-flit packet lack a packet header and “routing information” according to the ’893 patent. Ex. 1007, 3. Hence, contrary to claim 10, the second, third, and fourth flits mapped to the claimed “data packages” lack “a data element comprising routing information for the network stations.”

As for the disclosure in the '893 patent about router memory operation relating to service level that allows interleaving data packages in different data streams over a single communication channel that Petitioner cites, that disclosure does not indicate that a claimed “data package” may lack “a data element comprising routing information for the network stations.” *See* Ex. 1001, 5:29–42; Pet. 55–56; *see also* Ex. 1001, 3:23–33. Instead, that disclosure describes setting a bit in an “appropriate memory element” in a router’s memory for data packages that “belong to a data stream in progress.” Ex. 1001, 5:29–38. That disclosure does not indicate that a router may determine what data packages “belong to a data stream in progress” without checking “destination” information in the data packages. *See id.* at 5:29–42; *see also id.* at 3:23–33.

As for Petitioner’s assertion that an ordinarily skilled artisan would have understood that the transmission time for a “data package” in Dielissen, i.e., a three-word flit, “would be the number of words in the flit, i.e., $N=3$ cycles,” we disagree that Dielissen’s three-word flits correspond to the claimed “data packages.” *See* Pet. 64. As discussed above in this section, only the first flit in a Dielissen packet includes a packet header and “routing information” according to the '893 patent. *See* Ex. 1001, 2:22–26, 4:53–56, 4:58–64; Ex. 1007, 2–4.

Additionally, based on the current record, the combined disclosures in Dielissen and Hassoun do not teach limitation 10.f when, as Petitioner proposes and the Board agrees, “every data package communicated by the network stations has a fixed size of N data elements.” *See supra* §§ IV.D.2–IV.D.3. Instead of seeking to “insert[] $M*N$ data storage elements into the data communication network” according to limitation 10.f, Hassoun’s Fast

Path algorithm and RBP algorithm seek to “minimize the *cycle latency*, or equivalently, the total number of registers along the route.” Ex. 1011, 1 (emphasis in original); *see id.* at 2.

Further, as Patent Owner asserts, Hassoun’s Fast Path algorithm and RBP algorithm lack “any indication or suggestion that a size or length of” a packet or flit provides an input “indicating that a data package comprises N data elements.” *See* Ex. 1011, 2–4; Ex. 2001 ¶¶ 109–110, 113, 116; Prelim. Resp. 38–39, 41, 48. As Patent Owner also asserts, Hassoun’s algorithms do not account for the size or length of a packet or flit “when calculating their outputs (the alleged M*N data storage elements).” *See* Ex. 1011, 2–4; Ex. 2001 ¶¶ 109–110, 113, 116; Prelim. Resp. 39, 41, 48. Because Hassoun’s algorithms do not account for the size or length of a packet or flit “when calculating their outputs (the alleged M*N data storage elements),” combining Hassoun’s teachings with Dielissen’s teachings does not yield the claimed invention. *See* Ex. 2001 ¶ 113.

As for Hassoun’s Figure 2 illustrating an example buffer-register path from a source node *s* to a sink node *t* in a single-clock-domain system with three registers between the nodes, “Hassoun provides no explanation as to why this routing example utilizes three registers.” Ex. 2001 ¶ 111; *see* Ex. 1011, 3. Because Hassoun’s algorithms do not account for the size or length of a packet or flit “when calculating their outputs (the alleged M*N data storage elements),” an ordinarily skilled artisan would have had “no reason to believe that the quantity of three registers” in Hassoun’s Figure 2 correlated to the quantity of flits in packet. Ex. 2001 ¶ 111. Based on the current record, Petitioner fails to show a logical connection between the

three registers in Hassoun’s Figure 2 and the three words in each flit in a Dielissen packet. *See* Pet. 61–67; Ex. 1003 ¶¶ 211–226; Ex. 2001 ¶ 112.

For these reasons, Petitioner does not demonstrate a reasonable likelihood of proving that claim 10 is unpatentable under § 103(a) as obvious over Dielissen and Hassoun.

4. INDEPENDENT CLAIMS 1 AND 7

Like claim 10, claims 1 and 7 recite “a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks.” Ex. 1001, 10:30–33 (limitation 1.b), 11:46–49 (limitation 7.b). Like claim 10, claims 1 and 7 also recite “each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two.” *Id.* at 10:33–36 (limitation 1.c), 11:49–52 (limitation 7.c). Additionally, claims 1 and 7 include limitations similar to limitation 10.f. *Compare id.* at 12:38–41 (limitation 10.f), *with id.* at 10:42–49 (limitation 1.f), *and id.* at 11:58–62 (limitation 7.f).

Petitioner contends that Dielissen discloses “data packages” according to claims 1 and 7 for the reasons Petitioner contends that Dielissen discloses “data packages” according to claim 10. Pet. 68. Petitioner contends that the combined disclosures in Dielissen and Hassoun teach the limitations in claims 1 and 7 similar to limitation 10.f for the reasons Petitioner contends that the combined disclosures teach limitation 10.f. *Id.* at 68–70.

Patent Owner disputes that Dielissen discloses “data packages” according to claims 1 and 7 for the reasons Patent Owner disputes that Dielissen discloses “data packages” according to claim 10. Prelim.

Resp. 49. Patent Owner disputes that the combined disclosures in Dielissen and Hassoun teach the limitations in claims 1 and 7 similar to limitation 10.f for the reasons Patent Owner disputes that the combined disclosures teach limitation 10.f. *Id.*

Based on the current record and for the reasons discussed above for claim 10, Petitioner does not establish sufficiently for purposes of institution that the combined disclosures in Dielissen and Hassoun teach claim 1's subject matter or claim 7's subject matter. *See supra* § IV.H.3(c). Hence, Petitioner does not demonstrate a reasonable likelihood of proving that claims 1 and 7 are unpatentable under § 103(a) as obvious over Dielissen and Hassoun.

5. DEPENDENT CLAIMS 2, 3, 6, AND 9

Claims 2, 3, 6, and 9 depend directly or indirectly from claim 1. Ex. 1001, 10:50–63, 11:42–43, 12:11–21. Hence, claims 2, 3, 6, and 9 incorporate all the limitations in claim 1. 35 U.S.C. § 112 ¶ 4.

Based on the current record and for the reasons discussed above for claim 1, Petitioner does not demonstrate a reasonable likelihood of proving that claims 2, 3, 6, and 9 are unpatentable under § 103(a) as obvious over Dielissen and Hassoun. *See supra* § IV.H.4.

I. Petitioner's Other Patentability Challenges: Claim 8

Petitioner contends that claim 8 is unpatentable under § 103(a) as obvious over each of the following combinations of references:

- Bertozzi and Sullam;
- Bertozzi, Jantsch, and Sullam;
- Bertozzi, Duato, and Sullam; and
- Dielissen, Hassoun, and Sullam.

Pet. 78–81. Patent Owner disputes Petitioner’s contentions. *See* Prelim. Resp. 50.

Claim 8 reads as follows (with formatting added for clarity):

8. The integrated circuit as claimed in claim 1, further comprising
a clock signal generator,
the plurality of network stations and the M*N data storage elements being responsive to the clock signal generator.

Ex. 1001, 12:7–10.

Petitioner cites Sullam as teaching “a clock signal generator” according to claim 8. Pet. 78, 80–81. Petitioner does not cite Sullam as teaching limitation 1.f when considering Sullam alone or in combination with the other references. *See id.* at 78–81.

Based on the current record and for the reasons discussed above, Petitioner does not establish sufficiently for purposes of institution that Bertozzi, alone or in combination with Jantsch or Duato, or the Dielissen-Hassoun combination discloses or suggests limitation 1.f. *See supra* §§ IV.E.3, IV.F.2, IV.G.3, IV.H.4. Additionally, Petitioner does not show how Sullam remedies the deficiencies in those other references with respect to claim 1. *See* Pet. 78–81. Hence, Petitioner does not demonstrate a reasonable likelihood of proving that claim 8 is unpatentable under § 103(a) as obvious over any asserted combination of references that includes Sullam.

V. CONCLUSION

After considering the Petition, the Preliminary Response, and the evidence of record, and for the reasons discussed above, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail

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in proving the unpatentability of at least one claim challenged in the Petition.
Hence, we deny the Petition and do not institute an *inter partes* review.

VI. ORDER

Accordingly, it is

ORDERED that the Petition is denied and no trial is instituted.

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For PETITIONER:

J. Derek Vandenburg
Aaron W. Pederson
Nathan D. Louwagie
Ryan D. Rypka
CARLSON CASPERS VANDENBURGH & LINDQUIST, P.A.
dvandenburg@carlsoncaspers.com
apederson@carlsoncaspers.com
nlouwagie@carlsoncaspers.com
rrypka@carlsoncaspers.com

F. Christopher Mizzo
Gregory S. Arovas
Alan M. Rabinowitz
KIRKLAND & ELLIS LLP
chris.mizzo@kirkland.com
greg.arovas@kirkland.com
alan.rabinowitz@kirkland.com

For PATENT OWNER:

Jennifer Hayes
Daniel S. Stringfield
Angelo J. Christopher
Hang Zheng
NIXON PEABODY LLP
jenhayes@nixonpeabody.com
dstringfield@nixonpeabody.com
achristopher@nixonpeabody.com
hzheng@nixonpeabody.com