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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371		ATTORNEY'S DOCKET NUMBER R2184.0495/P495
		U.S. APPLICATION NO. (if known, see 37 CFR 1.5) 10/579766 NEW
INTERNATIONAL APPLICATION NO. PCT/JP2005/017921	INTERNATIONAL FILING DATE 21 September 2005	PRIORITY DATE CLAIMED 30 September 2004

TITLE OF INVENTION
ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD

APPLICANT(S) FOR DO/EO/US
Takamitsu Yamada

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [x] This is a **FIRST** submission of items concerning a submission under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a submission under 35 U.S.C. 371.
3. [x] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [ ] The US has been elected (Article 31).
5. [x] A copy of the International Application as filed (35 U.S.C. 371 (c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [x] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [x] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [x] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [x] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [x] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [x] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A preliminary amendment.
14. [ ] An Application Data Sheet under 37 CFR 1.76.
15. [ ] A substitute specification.
16. [ ] A power of attorney and/or change of address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.2 and 37 CFR 1.821 – 1.825.
18. [ ] A second copy of the published International Application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).

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IPR2024-00356 (Cadence Design Systems, Inc. v. Semiconductor Design Technologies, LLC)
SDT00000045

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U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/579766 NEW	PCT/JP2005/017921	R2184.0495/P495

20. [x] Other items or information: Return Receipt Postcard
PCT Request
Written Opinion
International Search Report
Cover page of International Publication - (WO2006/035854)

The following fees have been submitted	CALCULATIONS	PTO USEONLY
21. [x] Basic national fee (37 CFR 1.492(a)) $300	$ 300.00	
22. [x] Examination fee (37 CFR 1.492(c)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... $0 All other situations $200	$ 200.00	
23. [x] Search fee (37 CFR 1.492(b)) If the written opinion of the ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... $0 Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority ..... $100 International Search Report prepared by an ISA other than the US and provided to the Office or previously communicated to the US by the IB ..... $400 All other situations $500	$ 400.00	
TOTAL OF 21, 22 and 23 =	$ 900.00	
[ ] Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing in compliance with 37 CFR 1.821(c) or (e) or computer program listing in an electronic medium) (37 CFR 1.492(j)). The fee is **$250** for each additional 50 sheets of paper or fraction thereof.		

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof (round up to a whole number)	RATE	
44 - 100 =	/50 =		x $250.00	$

Surcharge of **$130** for furnishing any of the search fee, examination fee, or the oath or declaration after the date of commencement of the national stage (37 CFR 1.492(h)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	15 - 20 =		x	0.00	
Independent claims	2 - 3 =		x	0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+		
			TOTAL OF ABOVE CALCULATIONS =	$ 900.00	
[ ] Applicant claims small entity status. See 37 CFR 1.27. Fees above are reduced by ½.					
			SUBTOTAL =	$ 900.00	
Processing fee of **$130.00** for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)).				$	
			TOTAL NATIONAL FEE =	$ 900.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 40.00	
				$	
			TOTAL FEES ENCLOSED =	$ 940.00	
			Amount to be refunded:	$	
			Amount to be charged	$	

DSMDB.2087001.1

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d. [x] Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed an granted to restore the International Application to pending status.

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DSMDB.2087001.1

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DESCRIPTION

ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD

TECHNICAL FIELD

The present invention relates to a technology that executes circuit verification of an LSI (large scale integration) and so on using a process based on a computer program, and a verifying technology for verifying so that design violation and missing verification do not exist in design data by converting a property of a circuit to be verified into an assertion description and inputting the assertion description to a simulator when the design data of a circuit in a RTL (register transfer level) are dynamically verified by the simulator; and in particular, an assertion generating system, a program thereof, a circuit verifying system, and an assertion generating method, in which the above technology is used.

The property to be discussed below is plain text that defines operations intended and expected in design data to be verified. For example, the property defines a relation between reception and response of a request signal and an approval signal in an arbiter circuit on time series constraint, and defines a regular state of the time series

constraint and circuit specifications to be forbidden. In addition, the property is an event to be monitored as a function coverage point which confirms whether a specific circuit sequence has been tested by a simulation. Property verification verifies whether a design description satisfies a predetermined property.

BACKGROUND ART

Recently, a system has been revised or a revised edition of a system has been published frequently, caused by missing verification of a corner case due to the complexity of a circuit and an increase of circuit size of a semiconductor integrated circuit, by missing confirmation of interface specifications among blocks allocated to plural designers due to group work, or by specification errors of a reusable core purchased from a third party.

These problems come from, for example, insufficient circuit verification or a test scenario that can extract bugs, which were not able to be formed because a corner case and core specifications of the third party were not understood sufficiently.

In order to solve these problems, an assertion verification technology, in which a property with respect to circuit specifications is converted into an assertion description and the assertion description is input to a

simulator (computer) for verification, and a function coverage report for showing a warning for assertion violation during the simulation and showing whether a specific circuit sequence has been tested by a simulator is given, has been proposed and has been recently put into use in actual designing.

An assertion is a note in which intention (in some cases, this shows property) of designing is written and is generally written by a comment sentence in a RTL. The intention is interpreted by a simulator during the verification, for example, an error log is generated in a case where a circuit to be verified operates differently from the intention. The intention of designing is, for example, an assumption and a precondition of circuit input, and in addition to these, expected operations when the conditions are satisfied.

The simulator checks the following two matters.

(1) Specific events such as an assumption and a precondition have occurred.

(2) Expected operations at that time complete normally.

From the above check (1), the assertion gives feedback of determining information as to whether a specific circuit function is confirmed by verification. Therefore, when the assertion is comprehensively installed

in a circuit to be verified, function coverage of the assertion can be obtained; consequently, its verification accuracy can be obtained quantitatively.

From the above check (2), the feedback to a verification debugging can be obtained by the assertion. For example, an assertion installed in a position, from which an influence caused by a circuit malfunction cannot be observed by external terminals, complements a malfunction state. In addition, when conditions such as an assumption and a precondition are satisfied in any stimulus, this expected operation is checked at any time. Therefore, for example, even when the stimulus is structured by a random system, self-collation with the expected operation, that is, comparison of expected values, can be executed. In addition, an assertion installed in a lower block is also effective in chip level verification.

The intention of designing may be described by a Verilog-HDL for verification being different from a RTL for logic synthesis; however, here, another assertion language is described.

At present, the most popular assertion language is a PSL (property specification language) described in Non-Patent Document 1. The PSL is an assertion language which will be given to IEEE from a standardization organization named Accellera, and is actually a standard

language. In the following, an actual example of an assertion description using the PSL is shown.

For example, it is assumed that the following design intention (property) for memory control is desired to monitored by verification.

1) read_n and write_n do not become Low at the same time

2) at the fall (negative) of write_n, enable_n is High

3) at the fall of read_n, enable_n is Low

The PSL description (assertion description) to be given to a simulator as an assertion for the intention is as follows.

```
// psl property memcont1 = never (!write_n && !read_n)
@(posedge clk) ;
// psl assert memcont1 ;
// psl property memcont2 = always (enable_n) @(negedge
write_n) ;
// psl assert memcont2 ;
// psl property memcont3 = always (!enable_n) @(negedge
read_n) ;
// psl assert memcont3 ;
```

All of "psl, property, never, assert, always" in the above PSL description (assertion description) are reserved words in the PSL. All rows start with "//" which shows a comment of the Verilog-HDL. In this, instead of using "//", all of the PSL descriptions can be closed with

"/**/".

The words "memcont1,2,3, !write_n && !read_n, posedge clk, enable_n, negedge write_n, !enable_n, negedge read_n" are descriptions by a user definition, and actual installed data names, that is, memory control signal names which appear in the RTL for defining the intention of 1) through 3) except for "memcont1,2,3".

In addition, "memcont1 though 3" are assertion names and are used for knowing an error log and a function coverage being given from the simulator as feedback.

The assertion description by the PSL has the following structural elements.

// psl property <an assertion name> =

<an event to be monitored> -> <expected operation when a condition is satisfied> @<a strobe condition> ;

// psl assert <an assertion name> ;

For example, in the assertion description of 1), "memcont1" is an assertion name, "!write_n && !read_n" is an event to be monitored, in this case, "never" is added in front of the event; therefore, it is monitored that the condition (event) in ( ) never becomes true. If "always" is added, it is monitored that the condition in ( ) is true. In addition, by "@(posedge clk)" which follows the above statement, it is defined that monitoring the condition is executed at every time of rising edges (positive edges).

"->" changes to "|=>" or "|->" depending on the time when the expected operation is started. In this, the above example does not accompany expected operations.

The part in ( ) except the strobe condition is described by the Verilog-HDL which returns Boolean values. The part in ( ) of the strobe condition has a description form of a sensitivity list described by an "always sentence" of the Verilog-HDL.

In the PSL, an event to be monitored can be defined, and each part of expected operations at the time when the condition is satisfied can define a sequence, that is, the changes of events and expected operations in plural cycles can be defined. An example is explained.

The intention of designing: When a clear start condition (m_task == 2'b00) is satisfied in a clearing process of a memory, in order to initialize all words (256 words), a writing operation is repeated 256 times. Here, one writing operation is completed by the operation of Low→High→High of write_n synchronized with a rise cycle (positive cycle) of clk.

The PSL description:

```
// psl sequence WRITE_PULSE = { !write_n; write_n;
write_n };
// psl property CLEAR_MEM_WRITE_N =
// always { m_task == 2'b00 } |=> { WRITE_PULSE [*256] }
```

```
// @(posedge clk) ;
// psl assert CLEAR_MEM_WRITE_N;
```

"sequence" defines a Low→High→High sequence of "write_n" by a macro-definition.

Here, it is the part of expected operations which follows "|=>" that is to be focused on. When "m_task == 2'boo", the expected operation is WRITE_PULSE, that is, it is expected that the sequence of Low→High→High being three cycles of write_n be repeated by 256 times.

However, in such an assertion verifying technology, for example, in a case where the assertion description language is written by a manual input when the specifications are defined, there is a possibility that a mistake may be made in the assertion itself. As a result, a report of the warning of the assertion violation and the function coverage obtained by the assertion verification cannot be fed back to prevent the system revision and the revised edition of the system. Further, this requires a verification period for debugging the assertion description language. Consequently, the verification efficiency becomes worse.

In other words, the major premise of the assertion verifying technology is that the circuit specifications and the assertion description match each other; however, there is no method to confirm the matching

before executing the simulation. Further, with respect to a complex finite state machine, it is difficult to describe a sequence of a comprehensive state transition by manual operation.

As conventional technologies with respect to the assertion verification, for example, there are technologies disclosed in Patent Document 1 and Patent Document 2.

In Patent Document 1, a technology, in which a state transition machine is modeled by a graph and a state transition path that satisfies the assertion is searched, is disclosed. Further, a technology to confirm the rightness of the assertion by only an analysis of this graph is disclosed. By the technologies, matching the circuit specifications with the assertion description can be confirmed.

However, in these technologies, with respect to the state transition machine which is made to be a graph, a model of the state transition machine which becomes a basic model is formed manually, or the state transition machine is extracted from design data formed by a description language of a RTL. Consequently, mixing a mistake in an object to be matched, that is, in the model of the state transition machine which should be the circuit specifications, cannot be avoided.

In addition, in Patent Document 2, a technology,

which generates an assertion for verifying a circuit by extracting a data transfer structure from design data of a RTL and expanding the data transfer structure into a graphic structure, is disclosed. However, in this technology, since the assertion which is the circuit specifications is extracted from the design data, matching the circuit specifications with the assertion description cannot be assured.

[Patent Document 1] Japanese Laid-Open Patent Application No. 2000-181933

[Patent Document 2] Japanese Laid-Open Patent Application No. 2000-142918

[Non-Patent Document 1] Property Specification Language Reference Manual Version 1.1 June 9, 2004, online, retrieved in September 14, 2004, from the Internet, URL: http://www.eda.org/vfv/docs/PSL-v1.1.pdf

Consequently, in the conventional technologies, matching the circuit specifications with the assertion description cannot be assured.

DISCLOSURE OF THE INVENTION

The object of the present invention is to solve the problems in the conventional technologies, for example, to enable high reliability and high efficiency in assertion verification for an LSI and so on.

In order to achieve the above object, according to the present invention, a property to be verified is automatically converted into an assertion description language, based on a visual state transition figure, a timing chart, and a process sequence chart used when a designer forms specifications of a circuit.

According to one aspect of the present invention, there is provided an assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit. The assertion generating system includes a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations; a first storing unit that stores the design data generated by the specification inputting unit; a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data; a second storing unit that stores the property generated by the property generating unit; and an assertion generating unit that converts the property into an assertion

description by reading the property generated by the property generating unit from the second storing unit. In addition, the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

According to another aspect of the present invention, there is provided a program that makes a computer function as the units of the assertion generating system.

According to another aspect of the present invention, there is provided a circuit verifying system. The circuit verifying system includes the assertion generating system and executes assertion verification of a semiconductor integrated circuit by using an assertion description generated by the assertion generating system.

According to another aspect of the present invention, there is provided an assertion generating method that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit by a computer which has a program. The assertion generating method includes a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations

and inputs the design data in storage; a property generating step that reads the design data generated at the specification inputting step from the storage and generates a property which verifies the specification of the semiconductor integrated circuit using the read design data and inputs the property in the storage; and an assertion generating step that reads the property generated at the property generating step from the storage and converts the property into an assertion description. In addition, the property generated by the property generating step is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

According to the present invention, since the assertion description of a property to be verified is automatically generated from electronic data of the state transition figure which is attached to the specifications, matching the circuit specification with the assertion is established. Therefore, work to be used for debugging the assertion can be reduced. In addition, since the generated assertion is a function coverage point generated by comprehensive search of paths of the state transition, after the verification, feedback that a path has not been tested can be obtained by a function coverage report; consequently, missing a test of a corner case can be

prevented. In addition, since the assertion description of a property to be verified is automatically generated from electronic data of a selection condition of timing charts and signals which are attached to the specifications, or electronic data of figures or a table form in which a process sequence is noted or defined, matching the circuit specification with the assertion is established. Therefore, work to be used for debugging the assertion can be reduced. In many cases, the selection condition of timing charts and signals which are attached to the specifications or the process sequence is an important assertion to be surely tested at the time of verification; however, since the assertion generated in the embodiment is an important property, a designer who does not know the specifications and the circuit functions sufficiently can execute verification by using the property. As a result, the number of times of revising the system caused by missing verification can be reduced.

These and other objects, features, and advantages of the present invention will become more apparent from the following detailed description of preferred embodiments given with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a structural

example of hardware of which an assertion generating system and a circuit verifying system according to the present invention consist;

FIG. 2 is a block diagram showing a first functional structure example of the assertion generating system and the circuit verifying system using the assertion generating system according to the present invention;

FIG. 3 is a diagram showing a memory content example of a graphic structure using in the assertion generating system according to the present invention;

FIG. 4 is a diagram showing a state transition figure and a graphic structure using in the assertion generating system according to the present invention;

FIG. 5 is a block diagram showing a second functional structure example of the assertion generating system according to the present invention;

FIG. 6 is a block diagram showing a third functional structure example of the assertion generating system according to the present invention;

FIG. 7 is a diagram showing a timing chart example used in the assertion generating system according to the present invention;

FIG. 8 is a diagram showing a structural body example for storing information with respect to signals defined on the timing chart and information with respect to

timing constraints for the signals using in the assertion generating system according to the present invention;

FIG. 9 is a diagram showing a memory content example of property information with respect to the timing chart shown in FIG. 7;

FIG. 10 is a block diagram showing a fourth functional structure example of the assertion generating system according to the present invention;

FIG. 11 is a diagram showing a structural example of a logic table of a full adder used in the assertion generating system according to the present invention;

FIG. 12 is a diagram showing a structural body example of one cell when the cell is expanded in a table in a memory;

FIG. 13 is a diagram showing a memory structural example of a sheet in which cell structural bodies shown in FIG. 12 are combined;

FIG. 14 is a diagram showing an example when the logic table of the full adder shown in FIG. 11 is expanded in the memory structural example shown in FIG. 13; and

FIG. 15 is a diagram showing a structural example of a process sequence in a table form used in the assertion generating system according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Next, referring to the drawings, embodiments of the present invention are explained in detail.

FIG. 1 is a block diagram showing a structural example of hardware of which an assertion generating system and a circuit verifying system according to the present invention consist. FIG. 2 is a block diagram showing a first functional structure example of the assertion generating system and the circuit verifying system using the assertion generating system according to the present invention. FIG. 3 is a diagram showing a memory content example of a graphic structure using in the assertion generating system according to the present invention. FIG. 4 is a diagram showing a state transition figure and a graphic structure using in the assertion generating system according to the present invention. FIG. 5 is a block diagram showing a second functional structure example of the assertion generating system according to the present invention. FIG. 6 is a block diagram showing a third functional structure example of the assertion generating system according to the present invention. FIG. 7 is a diagram showing a timing chart example used in the assertion generating system according to the present invention. FIG. 8 is a diagram showing a structural body example for storing information with respect to signals defined on the timing chart and information with respect to

timing constraints for the signals using in the assertion generating system according to the present invention. FIG. 9 is a diagram showing a memory content example of property information with respect to the timing chart shown in FIG. 7. FIG. 10 is a block diagram showing a fourth functional structure example of the assertion generating system according to the present invention. FIG. 11 is a diagram showing a structural example of a logic table of a full adder used in the assertion generating system according to the present invention. FIG. 12 is a diagram showing a structural body example of one cell when the cell is expanded in a table in a memory. FIG. 13 is a diagram showing a memory structural example of a sheet in which cell structural bodies shown in FIG. 12 are combined. FIG. 14 is a diagram showing an example when the logic table of the full adder shown in FIG. 11 is expanded in the memory structural example shown in FIG. 13. FIG. 15 is a diagram showing a structural example of a process sequence in a table form used in the assertion generating system according to the present invention.

In FIG. 1, the reference number 101 is storage composed of a memory, a hard disk, and so on; the reference number 102 is a CPU (central processing unit); the reference number 103 is an input unit composed of a keyboard, a mouse, and so on; the reference number 104 is a

display unit composed of a CRT (cathode ray tube), a LCD (liquid crystal display) and so on; the reference number 105 is a system bus, and a computer system is composed of the units 101 through 105 in which the units 101 through 104 are connected by the system bus 105.

The storage 101 stores functional descriptions of hardware not depending on architecture, and functions and means according to the present invention in feasible program formats which are read from recording media, from which a computer can read the programs, such as a CR-ROM (compact disc-read only memory), a DVD (digital video disc/digital versatile disc), and a FD (flexible disk). The CPU 102 executes the programs being stored in the storage 101, and executes processes of functions of the assertion generating system having the structure shown in FIG. 2.

A user interactively inputs commands to execute the programs that realize inputting and editing of the functional descriptions of hardware not depending on architecture and means of the present invention by using the input unit 103. The display unit 104 displays the functional descriptions of hardware not depending on architecture, and the progress and the results of the programs, which realize the means of the present invention, executed by the CPU 102.

FIG. 2 shows a basic structure of an assertion generating system 207 and a circuit verifying system using the assertion generating system 207 according to the present invention. First, a circuit specification to be specified in specifications is input from a graphical editor 201 by user operations, and the circuit specification input at the graphical editor 201 is stored in the storage 101 as specification electronic data 202. In this, as the graphical editor 201, a graphical editor such as a timing chart editor disclosed in, for example, Japanese Laid-Open Patent Application No. 1-309185 can be used.

Next, a syntax analyzer 203 reads the specification electronic data 202 being stored in the storage 101 and analyses the syntax, and a property extractor 204 extracts a property to be verified from the results of the syntax analysis.

An assertion generator 205 generates an assertion description language 206, which can be input to a simulator or a static property checker from the property extracted from the property extractor 204. The assertion description language 206 generated in such a manner is stored in the storage 101 and is input to a simulator, and verification is executed.

As mentioned above, according to the assertion

generating system of this example, when assertion verification, which verifies design data in which a property with respect to a specification of a semiconductor integrated circuit or a part of the specification of the semiconductor integrated circuit is described in an assertion description with design data of a circuit to be verified of the property, is executed by a simulator or a static verification tool, the graphical editor 201 generates the specification electronic data 202 (design data) by editing a specification of a finite state machine by a visual expression on a state transition table or a state transition figure. The syntax analyzer 203 analyses the circuit specification defined at the graphical editor 201 and the property extractor 204 extracts a property to be verified based on the design data, and the assertion generator 205 outputs this property in an assertion description.

Here, the design data (specification electronic data) formed at the graphical editor 201 are expanded into a graphic structure on the storage 101, and the property extractor 204 can refer to the graphic structure. Further, as the design data (specification electronic data) formed at the graphical editor 201, data, in which a process sequence of a circuit is shown in a timing chart or a time series figure by using a business tool that can edit a

table input or a figure, are included, in addition to the state transition table and the state transition figure.

FIG. 5 shows an example in which the state transition figure is used as the design data (specification electronic data) to be formed at the graphical editor 201. In FIG. 5, graphical information 501 that is the state transition figure exemplified in, for example, FIG. 4(a), is edited and formed by the graphical editor 201 and is stored in the storage 101 being a hard disk, a system memory, and so on.

The graphical information 501 includes visual information, that is, coordinate information and so on in which structural elements of the state transition figure are disposed, and the state transition figure expressed visually can be attached to specifications by printing out.

A graph search engine 502 has functions of the syntax analyzer 203 and the property extractor 204 shown in FIG. 2, and extracts a graphic structure exemplified in FIG. 4(b) from the state transition figure exemplified in FIG. 4(a), and temporarily stores the graphic structure in a system memory. In the extracted graphic structure, the structural elements of the state transition figure are formed as nodes, and the graph search engine 502 searches state transition paths. For example, the graph search engine 502 searches all state transition paths from an

initial state of the state transition machine, extracts the paths, and stores them in the storage 101 as a path database 503.

A property converter 504 converts the state transition paths extracted by the graph search engine 502 into an assertion description language 505 by referring to the path database 503. The assertion description language 505 converted at the property converter 504 is described, for example, as a function coverage point for confirming whether the assertion description language 505 has been tested at a simulator.

An example of the memory content of the graphic structure to be used at the graph search engine 502 is shown in FIG. 3. In FIG. 3, the reference number 301 is a structural body that stores information of each state in the state transition figure, and the reference number 302 is a structural body that stores information of arcs in the state transition figure. These structural bodies 301 and 302 mutually execute a pointer reference and form a graph in which the respective pointers are made to be nodes.

In FIG. 4, FIG. 4(a) shows an example of a state transition figure, and FIG. 4(b) shows a graphic structure formed from the state transition figure. The graph search engine 502 shown in FIG. 5 searches the state transition paths from the state transition figure shown in FIG. 4(a)

by using a path search in graph logic, for example, an algorithm of a shortest path search. As a result, the graphic structure shown in FIG. 4(b) is formed and the graphic structure is stored in the path database 503.

Next, an example of a state transition path to be stored in the path database 503 shown in FIG. 5 is shown by using the example shown in FIG. 4.

```
init ;
(GO) S1 ;
init ;
```

In this example, a path from "init" to "S1" is searched, and when "GO" is true, that is, is "1", the state transition path is formed.

In addition, an assertion description by PSL, which is generated by the property converter 504 in FIG. 5 (the assertion generator 205 in FIG. 2) from this state transition path, is shown as follows.

```
property init_to_S1 = always { state == init & GO} |=>
{ state == S1} ;
```

In case of a state transition machine, it is necessary that all states are visited in verification, in order to quantify the verification accuracy of important functions being keys of circuit functions. Whether each state of the state transition machine is visited can be determined by confirming the function coverage of state

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verification by cover syntax of PSL. In case of the example shown in FIG. 4, it is enough that only state names stored in nodes of a graph are made to be a list by a cover description of PSL.

In the following, the result is shown. In this, "state" is a state register name for holding the state at the time when a state transition machine is installed.

```
// psl cover ( state == init) ;
// psl cover ( state == S1) ;
```

Here, in a case where the graphical information 501 shown in FIG. 5 has information of a graphic structure with the coordinate information, as shown in FIG. 3 and FIG. 4(a), the graph search engine 502 directly refers to the graphic structure in the graphical information 501.

Next, referring to FIG. 6, another embodiment of the present invention is explained. In the embodiment shown in FIG. 6, timing chart information to be attached to specifications is extracted from timing chart electronic data 601, and the interrelation with respect to timing of a signal group to be verified is made to be an assertion description.

In FIG. 6, the reference number 602 is a timing chart reader that reads the timing chart electronic data 601, the reference number 603 is a timing property extractor that extracts an interrelation with respect to

timing of a signal group to be verified (timing chart information) and stores the interrelation in a timing chart database 604, and the reference number 605 is a property converter that reads the timing chart information from the timing chart database 604 and generates an assertion description language 606 that can be input to a simulator or a static property checker.

In this, the timing chart electronic data 601 can be data formed and edited by a timing chart editor (not shown), in this case, the timing chart reader 602 becomes a syntax analyzer for timing chart information formed and edited by the timing chart editor.

The memory content used by the timing property extractor 603 is shown in FIG. 8. In FIG. 8, the reference number 801 is a structural body that stores information with respect to signals defined on the timing chart, and the reference number 802 is a structural body that stores information with respect to timing constraint for the signals.

An example of the timing chart that is read by the timing chart reader 602 is shown in FIG. 7. In the example shown in FIG. 7, "ack" rises (becomes positive) during 2 to 5 cycles from the rise (positive) of "req" synchronized with "clk".

In the example shown in FIG. 7, the timing

constraint (property), in which the positive of "ack" must be received in the range of 2 to 5 of "clk" after the output signal of "req" becomes 1, is described.

The timing property extractor 603 shown in FIG. 6 extracts the timing information (property) to be verified by using signal attributes such as IN, OUT, and CK, and "pos" that means a rising condition, and interrelation with respect to timing of a signal group such as "<-" and "->" as keywords.

The timing chart information shown in FIG. 7 formed and edited by the not-shown timing chart editor is stored in hardware by being edited in, for example, the following list. In the following list, 1 through 3 rows show pins and input/output attributes, for example, a clock input, and 4 through 7 rows show waveform information. In the sixth row, a property, in which "ack" rises (becomes positive) during 2 to 5 cycles from the rise (positive) of "req" synchronized with "clk", is shown.

```
1 CK      clk;
2 IN      ack;
3 OUT     req;
4 {clk,req,ack}  = {1,0,0};
5 {clk,req,ack}  = {1,1,0};
6 {clk,req,ack}  = {1,0,0} [2:5];
7 {clk,req,ack}  = {1,0,1};
```

A memory content example of property information with respect timing expanded by this timing chart information is shown in FIG. 9.

Next, an example, in which a business tool capable of inputting a table and editing a figure is used for editing a logic table and a time series property of the above circuit, is explained.

FIG. 11 is a structural example in which a logic table of a full adder is input by Excel (a registered trademark) being spread sheet software of Microsoft Corp. NAME, CLOCK, CONDITION, and EXPECT shown in a bold type are reserved words when a table definition is executed, and show a property name, a clock name, a start condition of an assertion check, and expected operations when the assertion check is started, respectively.

In the next row of CONDITION and EXPECT, signal names are described, and under the names, logic values are entered. According to Excel, a sheet is composed of cells, a cell is a basic unit of a table, and the sheet can be output as an ASCII file by separating cells with ",".

In the case of FIG. 7, the signal name, the 1/2 pulse of clock, and so on are managed by cell, and after expanding in a memory, the cell structure is scanned and the memory content shown in FIG. 9 is obtained.

FIG. 12 is a structural body for expressing one

cell when a cell of Excel is expanded in a memory. Members of top, bottom, left, and right in this structural body respectively execute a pointer reference to up and down and left and right.

FIG. 13 is a diagram showing a structural example of a sheet in which structural bodies of the cells shown in FIG. 12 are combined. The reference number 1301 is a pointer showing a sheet, and is composed of "next" being a pointer reference of the next sheet and a member that executes a pointer reference for a header of a cell. The reference number 1302 is a pointer of a cell, and executes a pointer reference for up and down and left and right by using the members of top, bottom, left, and right. By the above method, scanning cells on the sheet can be easily executed, and the retrieval by the keywords such as NAME, CLOCK, CONDITION, and EXPECT and the interpretation of the logic table can be executed.

FIG. 14 shows a content example when the logic table of the full adder shown in FIG. 11 is expanded in the memory structure shown in FIG. 13.

In the following, a PSL description, which generates an assertion description from the logic table of the full adder shown in FIG. 11, is shown. In this, the table and the verification data (that is, assertion) can be easily linked by adding the row number of the table to the

structure of the assertion name. For example, on the first row, FADD_S_0__FADD_csv_line_5 is the assertion name, and line_5 corresponds to the row number of the table.

```
psl property FADD_S_0__FADD_csv_line_5 = always { !A & !B
& !CI} |-> { S === 1'b0} ;
psl property FADD_CO_0__FADD_csv_line_5 = always { !A & !B
& !CI} |-> { CO === 1'b0} ;
psl property FADD_S_1__FADD_csv_line_6 = always { !A & !B
& !CI} |-> { S === 1'b1} ;
psl property FADD_CO_1__FADD_csv_line_6 = always { !A & !B
& !CI} |-> { CO === 1'b0} ;
psl property FADD_S_2__FADD_csv_line_7 = always { !A & !B
& !CI} |-> { S === 1'b1} ;
psl property FADD_CO_2__FADD_csv_line_7 = always { !A & !B
& !CI} |-> { CO === 1'b0} ;
psl property FADD_S_3__FADD_csv_line_8 = always { !A & !B
& !CI} |-> { S === 1'b0} ;
psl property FADD_CO_3__FADD_csv_line_8 = always { !A & !B
& !CI} |-> { CO === 1'b1} ;
psl property FADD_S_4__FADD_csv_line_9 = always { !A & !B
& !CI} |-> { S === 1'b1} ;
psl property FADD_CO_4__FADD_csv_line_9 = always { !A & !B
& !CI} |-> { CO === 1'b0} ;
psl property FADD_S_5__FADD_csv_line_10 = always { !A & !B
& !CI} |-> { S === 1'b0} ;
```

```
psl property FADD_CO_5__FADD_csv_line_10 = always { !A & !B
& !CI} |-> { CO === 1'b1} ;
psl property FADD_S_6__FADD_csv_line_11 = always { !A & !B
& !CI} |-> { S === 1'b0} ;
psl property FADD_CO_6__FADD_csv_line_11 = always { !A & !B
& !CI} |-> { CO === 1'b1} ;
psl property FADD_S_7__FADD_csv_line_12 = always { !A & !B
& !CI} |-> { S === 1'b1} ;
psl property FADD_CO_7__FADD_csv_line_12 = always { !A & !B
& !CI} |-> { CO === 1'b1} ;
```

In FIG. 10, another embodiment of the present invention is explained. In this embodiment, a sequence to be attached to specifications is stored as table data 1001, a syntax analyzer 1002 expands a sequence which is defined in a table form on a system memory, a sequence extractor 1003 extracts a process sequence to be verified, and a property converter 1004 converts the sequence into an assertion description 1005.

An example of a process sequence to be verified is shown in FIG. 15. This example shows a property equal to that shown in FIG. 7. This example is also formed by Excel. The syntax analyzer 1002 and the sequence extractor 1003 resolves a sequence described in cells into time series, and the property converter 1004 generates an assertion description by using a SERE expanded regular

expression of PSL.

In the resolution of the sequence into time series, ";" in a character string is interpreted as behavior during one clock cycle. In FIG. 15, "0[*2:5]" uses a repetition expression of PSL, and means that a LOW period continues during 2 to 5 cycles. Further, since "0[*2:5];1;0" is described, "ack" shows behavior that a Low period continues during 2 to 5 cycles and after this High and Low follow.

In the following, an assertion description of PSL generated based on FIG. 15 is shown.

```
psl property reqack_ack_0__REQ_csv_line_5 = always { (rose)}
|-> {{ack === 1'b0}[*2:5];{ack === 1'b1};{ack === 1'b0};
```

Programs for which the CPU 102 shown in FIG. 1 executes process flows shown in FIGS. 5, 6, and 10 are recorded in a magnetic medium and so on in a feasible form and stored in the storage 101.

As explained by using FIGs. 1 through 15, the assertion generating system 207 according to the embodiment generates an assertion description that is used for assertion verification of a semiconductor integrated circuit. The graphical editor 201 (specification inputting unit) generates design data of the semiconductor integrated circuit by graphically editing a specification (finite state machine, process sequence) of the semiconductor

integrated circuit into a state transition table and a state transition figure or a timing chart and a time series figure based on user operations, forms the specification electronic data 202 by expanding the design data to a graphic structure, and causes the storage 101 to store the data. In addition, the syntax analyzer 203 and the property extractor 204 (property generating unit) read the specification electronic data 202 (design data) from the storage 101 and generate a property that verifies the specification of the semiconductor integrated circuit based on the design data. Further, the assertion generator 205 (assertion generating unit) converts the property into the assertion description language 206.

In this, in the graphical editor 201 (specification inputting unit), the design data of the semiconductor integrated circuit can be generated by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations. The assertion generator 205 converts the property into an assertion description; in which an assertion name composed of a table name or a table row number of the logic table or the state table edited at the graphical editor 201 (specification inputting unit), or an assertion name composed of a signal name or a state name in the logic table or the state table is added.

The circuit verification system according to the embodiment provides the assertion generating system 207 and executes assertion verification of the semiconductor integrated circuit by using the assertion description generated by the assertion generating system 207.

As mentioned above, according to the embodiments, since the assertion description of a property to be verified is automatically generated from electronic data of the state transition figure which is attached to the specifications, matching the circuit specification with the assertion is established. Therefore, work to be used for debugging the assertion can be reduced. In addition, since the generated assertion is a function coverage point generated by comprehensive search of paths of the state transition, after the verification, feedback that a path has not been tested can be obtained by a function coverage report; consequently, missing a test of a corner case can be prevented.

In addition, since the assertion description of a property to be verified is automatically generated from electronic data of a selection condition of timing charts and signals which are attached to the specifications, or electronic data of figures or a table form in which a process sequence is noted or defined, matching the circuit specification with the assertion is established. Therefore,

work to be used for debugging the assertion can be reduced. In many cases, the selection condition of timing charts and signals which are attached to the specifications or the process sequence is an important assertion to be surely tested at the time of verification; however, since the assertion generated in the embodiment is an important property, a designer who does not know the specifications and the circuit functions sufficiently can execute verification by using the property; as a result, the number of times of revising the system caused by missing the verification can be reduced.

While the present invention is described above with reference to specific embodiments shown in FIGs. 1 through 15, it should be apparent that the invention is not limited to these embodiments, but numerous modifications could be made thereto by those skilled in the art without departing from the basic concept and scope of the invention. For example, in the embodiments, programs which realize the property extractor 204, the assertion generator 205, and so on are stored in the storage 101 by using recording media such as a CD-ROM, a DVD, and a FD; however, the programs can be stored in the storage 101 by down loading via a network using a communication apparatus.

Further, in the embodiments, the assertion description is executed by using PSL, but can be executed

by using other languages.

This patent application is based on Japanese Priority Patent Application No. 2004-286042 filed on September 30, 2004.

CLAIMS

1. An assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit, comprising:

a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations;

a first storing unit that stores the design data generated by the specification inputting unit;

a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;

a second storing unit that stores the property generated by the property generating unit; and

an assertion generating unit that converts the property into an assertion description by reading the property generated by the property generating unit from the second storing unit, wherein

the property generated by the property generating

unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

2. The assertion generating system as claimed in claim 1, wherein

the property generating unit generates at least one or more properties, and

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations.

3. The assertion generating system as claimed in claim 1, wherein

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property.

4. The assertion generating system as claimed in claim 1, wherein

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property.

5. The assertion generating system as claimed in claim 4, wherein

the assertion generating unit converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or a signal name or a state name in the logic table or the state table edited by the specification inputting unit is added, and the property is the temporal property.

6. The assertion generating system as claimed in claim 1, wherein

the specification inputting unit is a business tool of spread sheet software and expands the design data into a graphic structure and inputs the graphic structure in the first storing unit.

7. A program that makes a computer function as the units of the assertion generating system as claimed in claim 1.

8. A circuit verifying system, comprising:

the assertion generating system as claimed in claim1, wherein

the circuit verifying system executes assertion verification of a semiconductor integrated circuit by using the assertion description generated by the assertion generating system.

9. An assertion generating method that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit by a computer which has a program, comprising:

a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations and inputs the design data in storage;

a property generating step that reads the design data generated at the specification inputting step from the storage and generates a property which verifies the

specification of the semiconductor integrated circuit using the read design data and inputs the property in the storage; and

an assertion generating step that reads the property generated at the property generating step from the storage and converts the property into an assertion description, wherein

the property generated by the property generating step is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

10. The assertion generating method as claimed in claim 9, wherein

the property generating step generates at least one or more properties, and

the specification inputting step generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations.

11. The assertion generating method as claimed in claim 9, wherein

the specification inputting step generates the

design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property.

12. The assertion generating method as claimed in claim 9, wherein

the specification inputting step generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property.

13. The assertion generating method as claimed in claim 12, wherein

the assertion generating step converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or a signal name or a state name in the logic table or the state table edited at the specification inputting step is added, and the property is the temporal property.

14. The assertion generating method as claimed in claim 9, wherein

the specification inputting step expands the design data into a graphic structure and inputs the graphic structure in the storage.

15. A manufacturing method of a semiconductor device, comprising:

a designing step that designs an integrated circuit having a predetermined function;

a simulating step that simulates the integrated circuit by using the assertion generated at the assertion generating method as claimed in claim 9; and

a manufacturing step that manufactures a semiconductor device based on specifications of the integrated circuit,

wherein

the semiconductor device in which design meeting specifications is confirmed is manufactured by that the integrated circuit is simulated by the assertion obtained at the assertion generating method as claimed in claim 9.

ABSTRACT

An assertion generating system is disclosed. In an assertion generating system 207, a graphical editor 201 generates design data of a semiconductor integrated circuit by graphically editing a specification (finite state machine, process sequence) of the semiconductor integrated circuit with the use of a state transition table and a state transition figure or by editing the process sequence into a timing chart and a time series figure based on user operations, and a syntax analyzer 203 and a property extractor 204 generate a property that verifies the specification of the semiconductor integrated circuit based on the design data. The assertion generator 205 converts the property into an assertion description language 206.

FIG.1

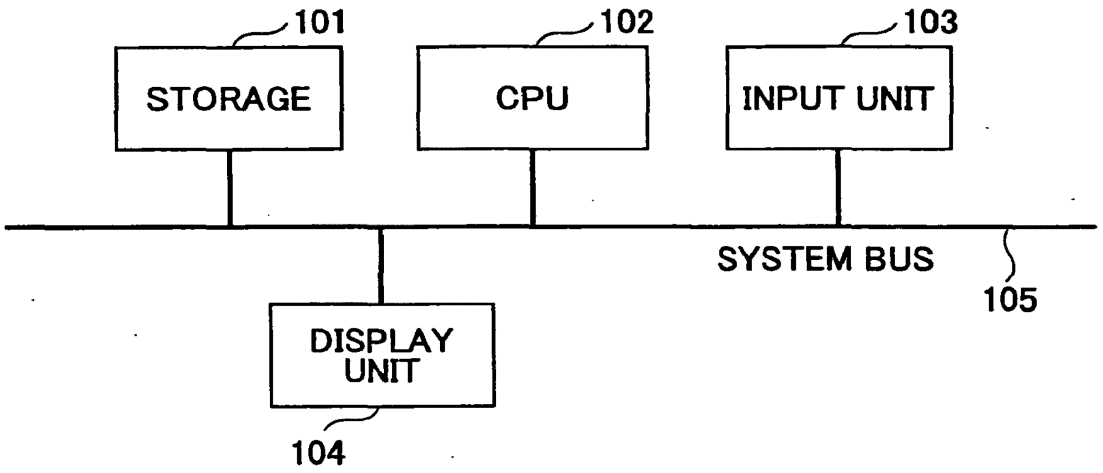
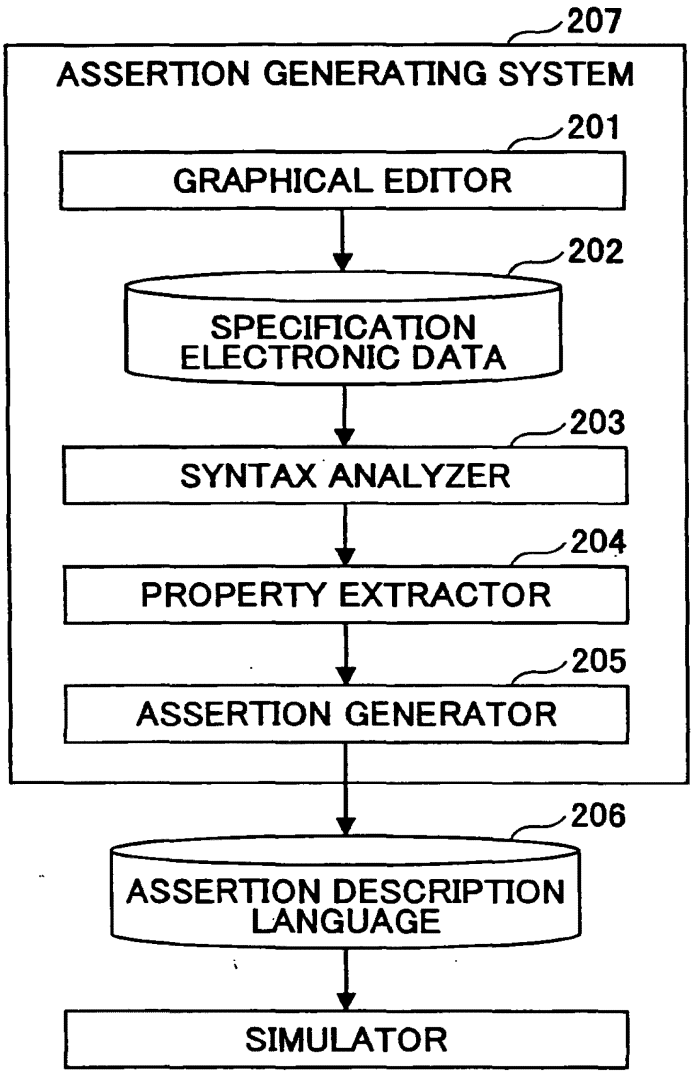
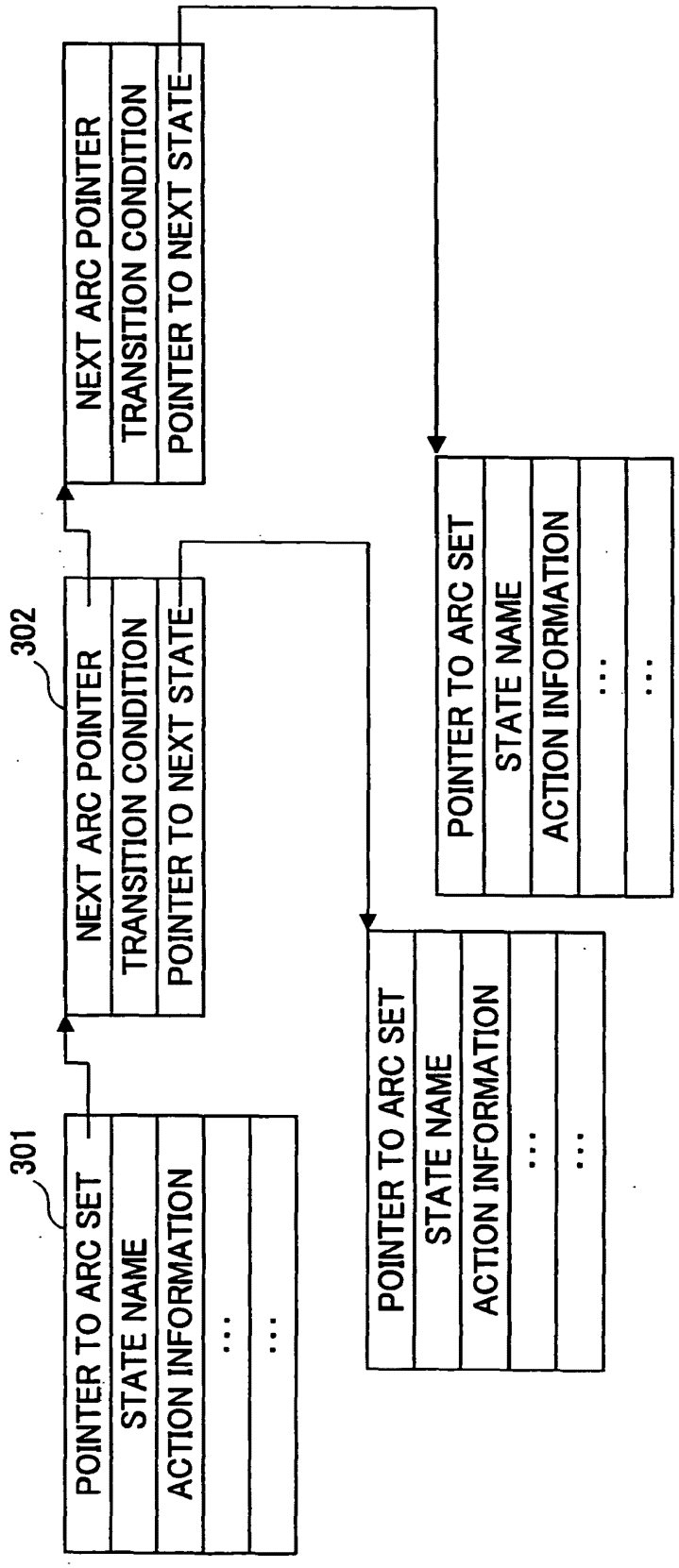

101
STORAGE
102
CPU
103
INPUT UNIT
SYSTEM BUS
105
DISPLAY UNIT
104

FIG.2


207
ASSERTION GENERATING SYSTEM
201
GRAPHICAL EDITOR
202
SPECIFICATION ELECTRONIC DATA
203
SYNTAX ANALYZER
204
PROPERTY EXTRACTOR
205
ASSERTION GENERATOR
206
ASSERTION DESCRIPTION LANGUAGE
SIMULATOR

SDT00000094

FIG.3



SDT00000095

FIG.4

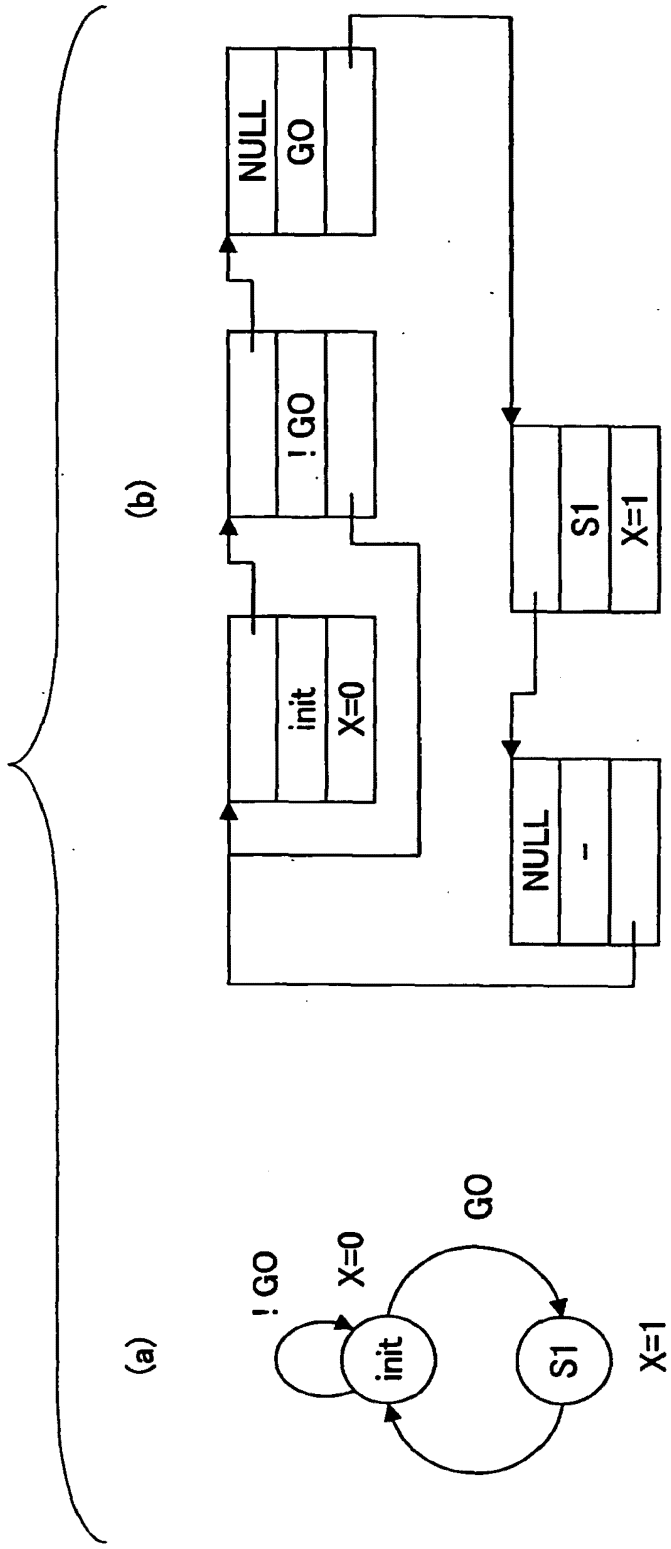


FIG.5

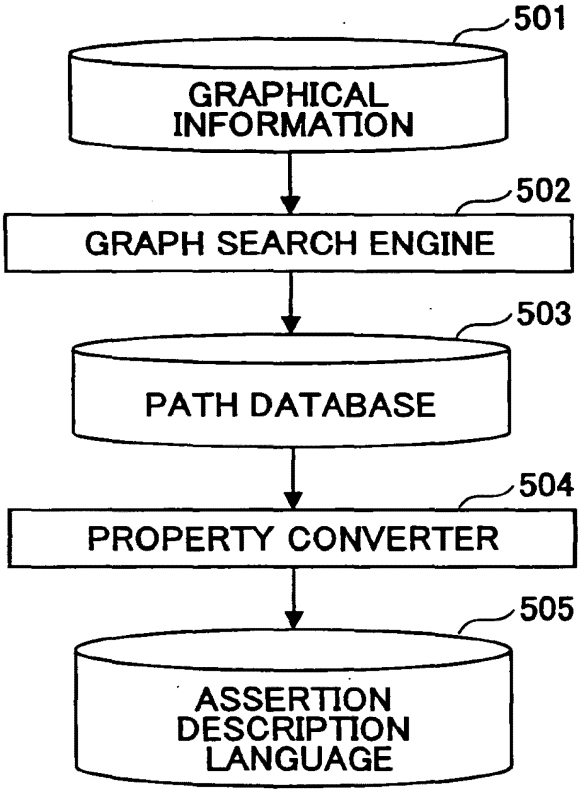

501
GRAPHICAL INFORMATION
502
GRAPH SEARCH ENGINE
503
PATH DATABASE
504
PROPERTY CONVERTER
505
ASSERTION DESCRIPTION LANGUAGE

FIG.6

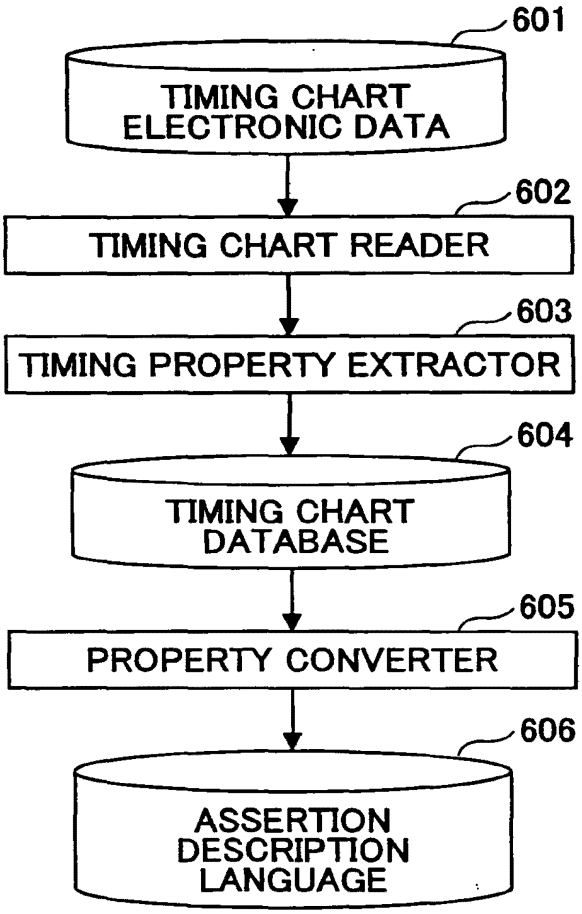

601
TIMING CHART ELECTRONIC DATA
602
TIMING CHART READER
603
TIMING PROPERTY EXTRACTOR
604
TIMING CHART DATABASE
605
PROPERTY CONVERTER
606
ASSERTION DESCRIPTION LANGUAGE

FIG.7

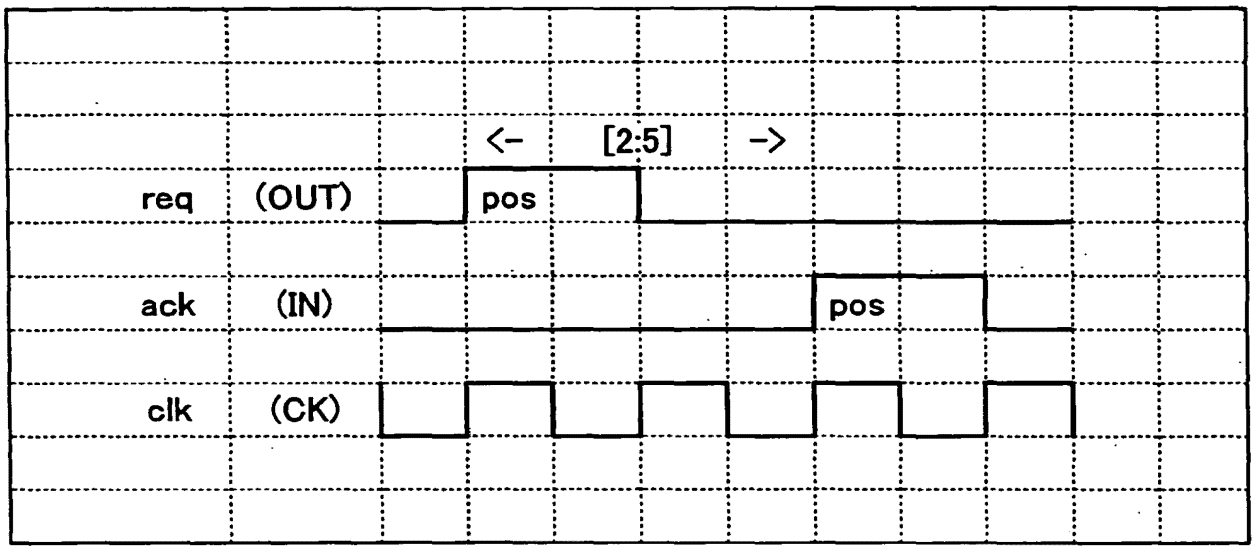

<-
[2:5]
->
req
(OUT)
pos
ack
(IN)
pos
clk
(CK)

FIG.8

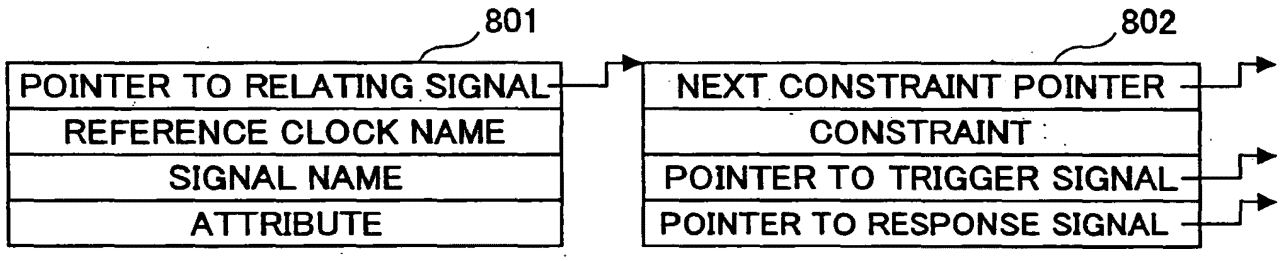

801
802
POINTER TO RELATING SIGNAL
REFERENCE CLOCK NAME
SIGNAL NAME
ATTRIBUTE
NEXT CONSTRAINT POINTER
CONSTRAINT
POINTER TO TRIGGER SIGNAL
POINTER TO RESPONSE SIGNAL

FIG.9

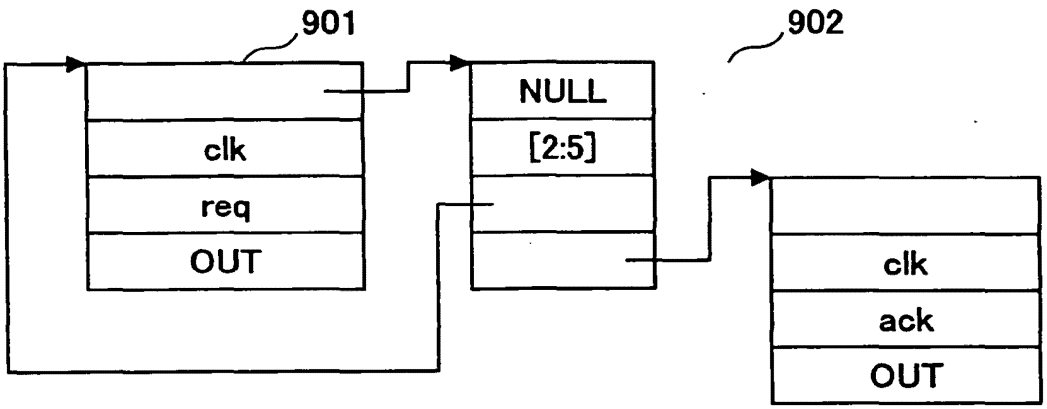

901
902
NULL
[2:5]
clk
req
OUT
clk
ack
OUT

FIG.10

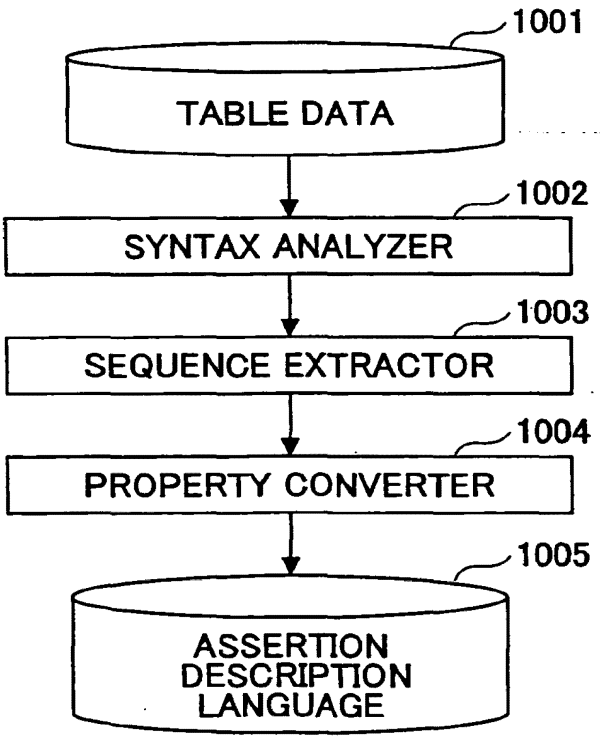

1001
TABLE DATA
1002
SYNTAX ANALYZER
1003
SEQUENCE EXTRACTOR
1004
PROPERTY CONVERTER
1005
ASSERTION DESCRIPTION LANGUAGE

FIG.11

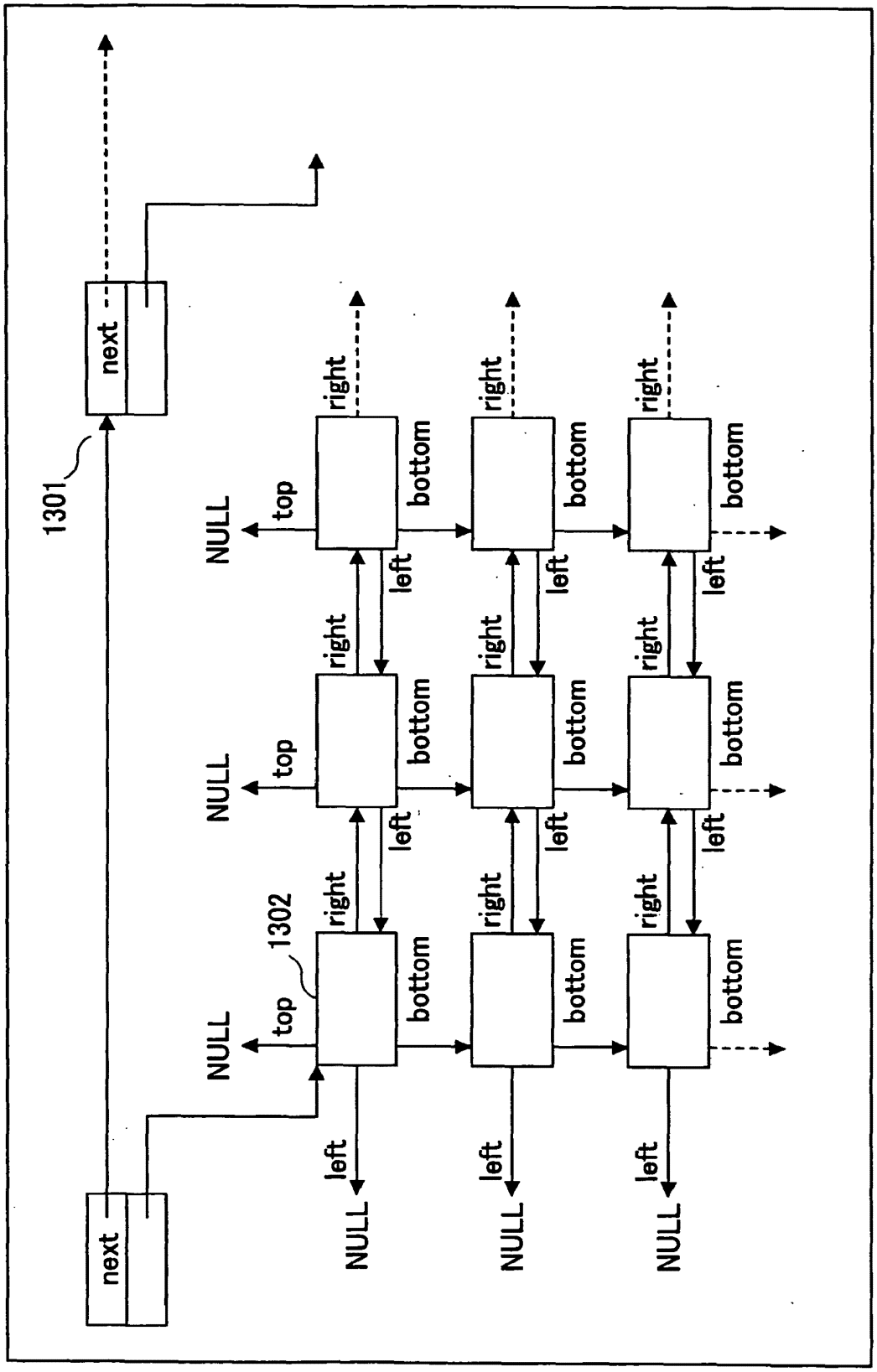
NAME	FADD			
CLOCK	posedge clk			
CONDITION	CONDITION	CONDITION	EXPECT	EXPECT
A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FIG.12

```
typedef struct piece {
    struct piece        *left, *right, *top, *bottom
    char*               str;

} Piece ;
```

FIG.13



SDT00000101

FIG.14

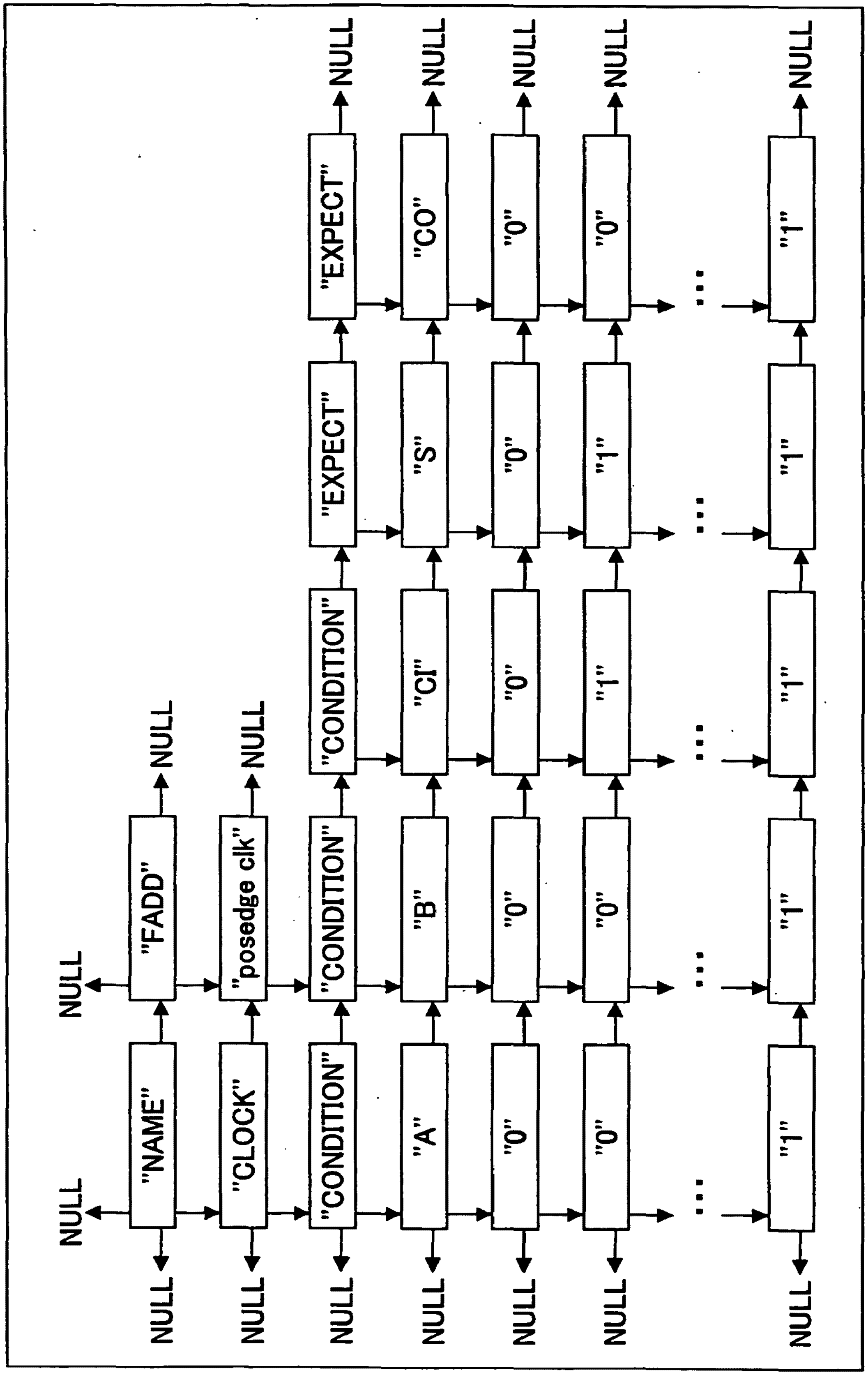

"NAME"
"FADD"
"CLOCK"
"posedge clk"
"CONDITION"
"CONDITION"
"CONDITION"
"EXPECT"
"EXPECT"
"A"
"B"
"CI"
"S"
"CO"
"0"
"1"
NULL

FIG.15

NAME	reqack
CLOCK	posedge clk
CONDITION	EXPECT
req	ack
rose	0[*2:5];1;0

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Declaration and Power of Attorney for Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

私は、以下に記名された発明者として、ここに下記の通り宣言する：

As a below named inventor, I hereby declare that:

私の住所、郵便の宛先そして国籍は、私の氏名の後に記載された通りである。

My residence, post office address, and citizenship are as stated next to my name.

下記の名称の発明について、特許請求範囲に記載され、且つ特許が求められている発明主題に関して、私は、最初、最先且つ唯一の発明者である（唯一の氏名が記載されている場合）か、或いは最初、最先且つ共同発明者である（複数の氏名が記載されている場合）と信じている。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD

上記発明の明細書はここに添付されているが、下記の箱がチェックされている場合は、この限りでない：

the specification of which is attached hereto unless the following box is checked:

☐ _____ の日に出願され、

☒ was filed on September 21, 2005

この出願の米国出願番号またはＰＣＴ国際出願番号は、

as United States Application Number or

PCT International Application Number

_____ であり、且つ

PCT/JP2005/017921 and was amended on

_____

_____ (if applicable).

の日に補正された出願（該当する場合）

私は、上記の補正によって補足された、特許請求範囲を含む上記明細書を検討し、且つ内容を理解していることをここに表明する。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編規則１．５６に定義されている、特許性について重要な情報を開示する義務があることを認める。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Cadence Design Systems, Inc. - Ex. 1002, Page 00060

SDT00000104

Japanese Language Declaration

（日本語宣言書）

私は、ここに、以下に記載した外国での特許出願または発明者証の出願、或いは米国以外の少なくとも一国を指定している米国法典第35編第365条(a)によるPCT国際出願について、同第119条(a)-(d)項又は第365条(b)項に基づいて優先権を主張するとともに、優先権を主張する本出願の出願日よりも前の出願日を有する外国での特許出願または発明者証の出願、或いはPCT国際出願については、いかなる出願も、下記の枠内をチェックすることにより示した。

I hereby claim foreign priority under Title 35, United States Code Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365 (a) of any PCT International application which designated at least one country other than the United States listed below and have also identified below, by checking the box, any foreign application for patent, or inventor's certificate, or PCT International application having a filing date before that of the application for which priority is claimed.

Prior Foreign Application(s)
外国での先行出願　Patent Application

Priority Not Claimed
優先権を主張なし

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願日／月／年)	
No. 2004-286042	Japan	30/September/2004	☐
			☐

私は、ここに、下記のいかなる米国仮特許出願についても、その米国法典第35編119条(e)項の利益を主張する。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)

私は、ここに、下記のいかなる米国出願についても、その米国法典第35編第120条に基づく利益を主張し、又米国を指定するいかなるPCT国際出願についても、その同第365条(c)に基づく利益を主張する。また、本出願の各特許請求の範囲の主題が、米国法典第35編第112条第1段に規定された態様で、先行する米国出願又はPCT国際出願に開示されていない場合においては、その先行出願の出願日と本国内出願日またはPCT国際出願日との間の期間中に入手された情報で、連邦規則法典第37編規則1．56に定義された特許性に関わる重要な情報について開示義務があることを承認する。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status Patented, Pending, Abandoned) (現況：特許許可、係属中、放棄)

私は、ここに表明された私自身の知識に係わる陳述が真実であり、且つ情報と信ずることに基づく陳述が、真実であると信じられることを宣言し、さらに、故意に虚偽の陳述などを行った場合は、米国法典第18編第1001条に基づき、罰金または拘禁、若しくはその両方により処罰され、またそのような故意による虚偽の陳述は、本出願またはそれに対して発行されるいかなる特許も、その有効性に問題が生ずることを理解した上で陳述が行われたことを、ここに宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Cadence Design Systems, Inc. - Ex. 1002, Page 00061

SDT00000105

Japanese Language Declaration
（日本語宣言書）

委任状：　私は本出願を審査する手続を行い、且つ米国特許商標庁との全ての業務を遂行するために、記名された発明者として、下記の弁護士及び／または弁理士を任命する。（氏名及び登録番号を記載すること）	POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number).*
All practitioners associated with Customer Number **24998**.	All practitioners associated with Customer Number **24998**.
書類送付先 Mark J. Thronson, Esq. DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP 2101 L Street NW Washington, DC 20037-1526	Send Correspondence to: Mark J. Thronson, Esq. DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP 2101 L Street NW Washington, DC 20037-1526
直通電話連絡先：（氏名及び電話番号） Mark J. Thronson, (202) 775-4742 (facsimile: (202) 887-0689)	Direct Telephone Calls to: *(name and telephone number)* Mark J. Thronson, (202) 775-4742 (facsimile: (202) 887-0689)

唯一または第一発明者氏名	Full name of sole or first inventor TAKAMITSU YAMADA
発明者の署名　日付 住所	Inventor's signature　Date Takamitsu Yamada May 8, 2006 Residence Kanagawa, Japan
国籍	Citizenship Japan
郵便の宛先	Post Office Address c/o RICOH COMPANY, LTD. 3-6, Nakamagome 1-chome, Ohta-ku, Tokyo 143-8555, Japan

第二共同発明者がいる場合、その氏名	Full name of second joint inventor, if any
第二共同発明者の署名　日付	Second inventor's signature　Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post Office Address

（第三以下の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

Cadence Design Systems, Inc. - Ex. 1002, Page 00062

SDT00000106

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

05/24/2006 LLANDGRA 00000001 10579766

01 FC:1631	300.00	OP
02 FC:1633	200.00	OP
03 FC:1642	400.00	OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 469-267/60033

10/579766
IAP12 Rec'd PCT/PTO 8 MAY 2006

Docket No.: R2184.0495/P495
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Takamitsu Yamada

Application No.: NEW | Confirmation No.: @@@

Filed: May 17, 2006 | Art Unit: N/A

For: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD | Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

MS PCT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

A summary/abstract translation of the non-English language references is enclosed.

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SDT00000108

Applicant has not submitted copies of each cited U.S. patent and U.S. patent application as required by 37 CFR 1.98(a)(2)(i), amended October 2004, as the U.S. Patent and Trademark Office has waived this requirement for all U.S. patent applications. Applicant submits herewith copies of foreign and non-patents in accordance with 37 CFR 1.98(a)(2).

A concise explanation of relevance of the items listed on form PTO/SB/08 is in the form of an English language copy of a Search Report from a foreign patent office, issued in a counterpart application, which refers to the relevant portions of the references.

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. R2184.0495/P495. A duplicate copy of this paper is enclosed.

Dated: May 17, 2006

Respectfully submitted,

By _____

Mark J. Thronson
Registration No.: 33,082
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
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Attorney for Applicant

10/579766
IAP12 Rec'd PCT/PTO 18 MAY 2006

PTO/SB/08a/b (07-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	NEW
Filing Date	May 17, 2006
First Named Inventor	Takamitsu Yamada
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	R2184.0495/P495

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	BA	JP-7-049887	02-21-1995			√
	BB	JP-2004-326650	11-18-2004			√
	BC	JP-2000-181933	06-30-2000			√
	BD	JP-2000-142918	05-23-2000			√

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	Property Specification Language Reference Manual Version 1.1, June 9, 2004	
	CB	TransEDA Announces Industry-First Property 1-15 Capture and Validation Product, [online], June 2, 2003, [retrieved on October 14, 2005], Retrieved from the Internet:<URL: http://www.transeda.com/news/view.php?id=54&s year=2003 > & <URL: http://www.transeda.com/news/languages/Japanese_54.doc >	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-049887
(43)Date of publication of application : 21.02.1995

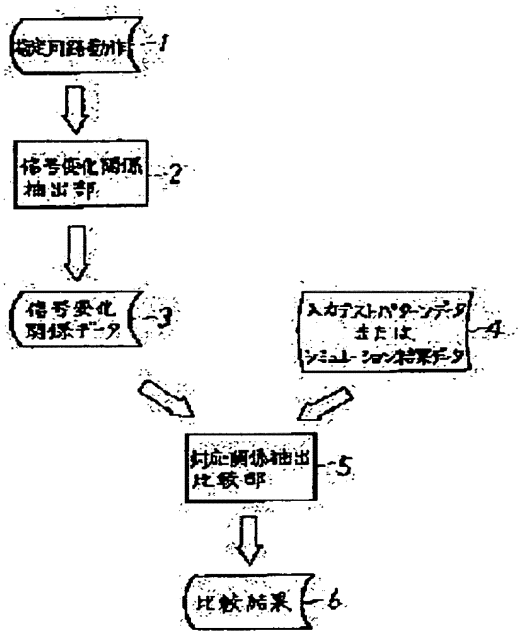
(51)Int.Cl. G06F 17/50

(21)Application number : 05-195706
(22)Date of filing : 06.08.1993

(71)Applicant : TOSHIBA CORP
(72)Inventor : TAKEI TSUTOMU

(54) LOGIC CIRCUIT VERIFICATION SYSTEM

(57)Abstract:
PURPOSE: To efficiently confirm operation by checking whether or not variation relation between the signal values of signals is satisfied for an input test pattern and a simulation result, or the input test pattern and an expected value.
CONSTITUTION: When a signal variation relation extraction part 2 partially specifies the dependency relation between an input/output signal and an internal signal as a verification item of specified circuit operation 1, this specification is converted as the variation relation between the signal values into internal data 3. A correspondence relation extraction and comparison part 5 retrieves variation relation between the signal values from the internal data 3 and the input test pattern of a simulator or simulation result data 4 to check whether or not the variation relation between the specified signal values depends upon the presence of data 4 on the input test pattern, expected value, or simulation result. Consequently, the operation can efficiently be confirmed by checking whether or not the variation relation between the signal values of the signals corresponding to the operation verification item is satisfied. Further, the comparison can be made while a margin is given to the time of signal variation.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

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SDT00000112

[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

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SDT00000113

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平7－49887

(43)公開日　平成７年(1995)２月21日

(51)Int.Cl.[6]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｇ０６Ｆ　17/50				
		7623－5L	Ｇ０６Ｆ　15/ 60	３６０　Ｄ

審査請求　未請求　請求項の数２　ＯＬ　（全 12 頁）

(21)出願番号　特願平5－195706

(22)出願日　平成５年(1993)８月６日

(71)出願人　000003078
株式会社東芝
神奈川県川崎市幸区堀川町72番地

(72)発明者　武井　勉
神奈川県川崎市幸区小向東芝町１番地　株式会社東芝研究開発センター内

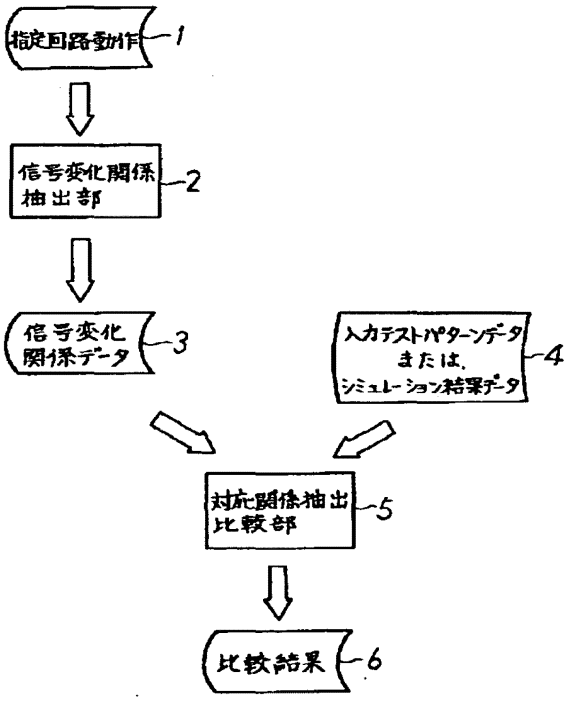
(74)代理人　弁理士　則近　憲佑

(54)【発明の名称】　論理回路検証方式

(57)【要約】

【構成】本発明は、このような従来の事情を鑑みてなされたものであり、第１の発明の目的は、動作検証項目を考えた時点で、入力信号，出力信号及び内部信号間の依存関係を部分的に表現し、入力テストパターン及びシミュレーション結果或いは入力テストパターン及び期待値に対して、信号間の信号値の変化関係が満たされているかを調べることにより効率的に動作確認を行える論理回路検証システムを提供することにある。また、第２の発明の目的は、シミュレーション結果同士、或いは、シミュレーション結果と期待動作信号変化を比較する場合に、一方の信号の信号変化の時刻に幅を持たせて比較することができることにより、期待動作との不一致を選択でき、効率的に動作確認を行える論理回路検証システムを提供することにある。

【効果】本発明によれば、効果的に動作確認が行える。



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【特許請求の範囲】
【請求項１】　入力信号、出力信号及び内部信号間の依存関係を部分的に表現し、それから信号間の信号値の変化関係を抽出し、入力テストパターン及びシミュレーション結果或いは入力テストパターン及び期待値に対して、該信号間の信号値の変化関係が満たされているかを調べることを特徴とする論理回路検証方式。
【請求項２】　２つのシミュレーション結果、或いは、シミュレーション結果と期待値を比較する場合に、両者の信号の信号変化の時刻に幅をもたせて比較することを特徴とする論理回路検証方式。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、論理回路システムの設計開発を行う際に用いる設計支援システムに関する。
【０００２】
【従来の技術】論理回路システムの設計開発をする場合に、機能論理シミュレータを用いて機能論理動作検証を行う。シミュレータによる検証では、論理回路システムのモデルを記述したハードウェア記述（Ｈａｒｄｗａｒｅ　ＤｅｓｃｒｉｐｔｉｏｎＬａｎｇｕａｇｅ記述）と入力テストパターンを与えてシミュレーションを行い、得られたシミュレーション結果の０，１等の信号変化を、０，１等のテキスト或いは波形として見ることによって、期待する正しい動作を行っているかを確認する。実際の論理回路システムのシミュレーション結果は非常に膨大になり、シミュレーション結果が期待どおりの動作を行っているかを確認する作業は非常に手間がかかる。この為に、予め、期待する動作として、出力信号などの注目する信号の信号変化を期待値として、入力テストパターンに対応して与えて、シミュレーション結果と比較する。また、回路の一部を修正してシミュレーションを再実行した場合は、以前のシミュレーション結果と回路修正後のシミュレーション結果の比較（例えば、テキストファイルの比較）を行うという作業が必要である。
【０００３】
【発明が解決しようとする課題】論理回路システムの動作検証をシミュレータなどで行う場合に、シミュレーション結果の０，１等の信号変化を見て、期待どおりの動作を行っているかを確認する作業で、見誤りが発生しやすく、作業に膨大な時間を要する問題があった。また、期待する動作として、出力信号などの注目する信号の０，１等の信号変化を、予め用意する作業でも、誤りが発生しやすく、作業に膨大な時間を要する問題があった。更に、作成する入力テストパターン自体に、動作検証項目として考えていた動作が含まれていないものを作成してしまうことがあり、その場合に、設計者が検証抜けに気付かないという問題もあった。更に、シミュレーション結果同士、或いは、シミュレーション結果と期待動作信号変化を比較する場合に、一方のシミュレーション結果のある信号の信号変化の時刻が、遅延やタイミングの変化により少し変わってしまった場合に、期待動作としては正しいが、テキストファイルの比較では、不一致となってしまい、不一致結果中のどの部分が論理的な誤りであるかを解析するのに膨大な時間を要する問題があった。
【０００４】そこで、本発明は、このような従来の事情を鑑みてなされたものであり、第１の発明の目的は、動作検証項目を考えた時点で、入力信号，出力信号及び内部信号間の依存関係を部分的に表現し、入力テストパターン及びシミュレーション結果或いは入力テストパターン及び期待値に対して、信号間の信号値の変化関係が満たされているかを調べることにより効率的に動作確認を行える論理回路検証システムを提供することにある。
【０００５】また、第２の発明の目的は、シミュレーション結果同士、或いは、シミュレーション結果と期待動作信号変化を比較する場合に、一方の信号の信号変化の時刻に幅を持たせて比較することができることにより、期待動作との不一致を選択でき、効率的に動作確認を行える論理回路検証システムを提供することにある。
【０００６】
【課題を解決するための手段】本技術は、上述した課題を達成するために、次のような手段を備えている。まず、第１の発明は、論理回路システムの回路動作として入力信号，出力信号及び内部信号間の依存関係を部分的に表現する手段を有し、該表現された信号間の依存関係から信号の値の変化関係を抽出する手段を有し、入力テストパターン或いは入力テストパターンと期待値或いは入力テストパターンと出力信号，内部信号を含むシミュレーション結果から、該‘信号の値の変化関係’を検索し、回路動作に対応する信号の値の変化関係が入力テストパターンに存在するかどうか調べる手段を有するか、或いは、回路動作に対応する信号の価の変化として、入力テストパターンの信号の値の変化関係とその時の入力信号，出力信号，内部信号の信号の値の変化関係が期待値或いはシミュレーション結果に存在するかどうか調べる手段を具備したものである。
【０００７】また、第２の発明は、２つのシミュレーション結果、或いは、シミュレーション結果と期待動作信号変化を比較する場合に、少なくとも一方の信号の信号変化の時刻に時間幅を指定する手段を有し、該時間幅を指定された信号の信号変化の時刻に幅を持たせて比較する手段を具備したものである。
【０００８】
【作用】本発明によれば、動作検証項目として、入力信号，出力信号及び内部信号間の依存関係を部分的に指定すると、該指定を信号値の変化関係として内部データに変換し、シミュレータの入力テストパターン或いはシミュレーション結果から該信号値の変化関係を検索し、指

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定された信号値の変化関係が入力テストパターン或いは期待値或いはシミュレーション結果に存在するかどうかを調べる手段を有することにより、動作検証項目に対応した信号間の信号値の変化関係が満たされているかを調べて、効率的に動作確認を行える。また、信号変化の時刻に幅をもたせて比較することができることにより、期待動作との不一致を選択でき、回路の論理的な誤り等を選択でき、効率的に動作確認を行える。

【０００９】

【実施例】以下に本発明の実施例を説明する。

第１の発明

図１は、第１の発明の論理検証システムに関する部分のシステム構成図の１例である。図１において、指定回路動作（１）は、設計者によって与えられる動作検証項目に対応した信号間の依存関係である。信号変化関係抽出部（２）は、指定回路動作（１）から信号変化関係を抽出する部分である。信号変化関係データ（３）は、信号変化関係抽出部（２）で抽出された信号変化関係を表す内部表現データである。データ（４）は、シミュレータの入力となる入力テストパターンデータまたは期待値またはシミュレータの出力であるシミュレーション結果データであり、各信号の変化時刻と変化値を持っている。対応関係抽出比較部（５）は、信号変化関係データ（３）と入力テストパターンデータ（４）より信号変化関係データ（３）で示された入力信号の信号変化関係が入力テストパターンデータ（４）の中に存在するかどうかを調べる、或いは、信号変化関係データ（３）とシミュレーション結果データ（４）より信号変化関係データ（３）で示された入力信号の信号変化関係に一致するものがシミュレーション結果データ（４）の中に存在するか否かを調べ、存在した場合には、信号変化関係データ（３）で示された入力信号，内部信号，出力信号の信号変化関係とシミュレーション結果データ（４）の信号変化関係が一致するかどうかを調べる。比較結果（６）は、対応関係抽出比較部（５）で比較された存在の有無，一致不一致の結果である。

【００１０】図２，図３，図４は、図１における指定回路動作（１）に相当する指定例の１例である。図２は、波形表示（７）を用いて回路動作を指定したものであり、入力端子の信号Ａが０から１に立ち上がった次の時点に、入力端子の信号Ｂが立ち上がり、その後に入力端子の信号Ｂが立ち下がり、入力端子の信号Ｂが立ち下がった次の時点に、出力端子の４ビットの信号ＤＯ（０ｔｏ３）が“００００”に変化する、ことを示している。ここで、信号変化の関係は、波形上に矢印で示された異なる信号間の因果関係，その時の信号の変化或いは信号の値（入力端子の信号Ａが０から１に立ち上がった次の時点に、入力端子の信号Ｂが立ち上がる。入力端子の信号Ｂが立ち下がった次の時点に、出力端子の信号ＤＯ（０ｔｏ３）が００００に変化する。）と、それに関係する信号自身の変化（入力端子の信号Ｂが立ち上がり、その後に入力端子の信号Ｂが立ち下がる。）で表されている。ここで、矢印に関連しない波形変化等は、回路動作のチェックの対象にはならない。図３は、使う動詞等が限定された言葉（８）を用いて、図２に示した波形の変化関係と同様のことを表現したものである。図４は、時相論理（９）を用いて図２，図３に示した信号の変化関係と同様のことを表現したものである。この他にも、信号の値と状態遷移図などを組み合わせて信号変化の関係を表現することができる。

【００１１】図５は、図１における対応関係抽出比較部（５）の処理フロー概略の１例である。先ず最初に、図１の信号変化関係（３）で示された信号に対応する、信号変化のデータを、図１の入力テストパターンデータ或いは期待値或いはシミュレーション結果データ（４）から取り出す（Ｓ１）。次に、該取り出した信号変化データに対して、該信号変化関係で示された信号の内の入力信号の変化関係に一致する部分を検索する（Ｓ２）。ここで、該検索で一致する部分が無かった場合は、指定された回路動作（信号変化関係）をシミュレーションする入力テストパターンに含まれていないことになる（Ｓ６）。一方、検索で一致する部分が存在した場合は、図５のステップＳ２で検索された、信号変化部分の期待値或いはシミュレーション結果の信号変化データに対して、図１の信号変化関係（３）で示された内部信号や出力信号の変化関係に一致するか一致しないかを調べる。そして、該一致不一致の判定と、その時のシミュレーション結果データにおける信号名，時刻，信号値と、信号変化関係で示された信号変化を出力する（図５のＳ３とＳ４）。図５のステップＳ２で検索される一致部分は複数ある場合がある、つまり、１つの（一連の）シミュレーション結果データ或いは期待値データの中に、信号変化関係で示された入力信号の変化関係に一致する部分が複数箇所ある場合があり、その場合は、各々の一致部分に対して行うために、次の入力信号の信号変化関係検索開始時刻を更新し（図５のステップＳ５）、図５のＳ３とＳ４とＳ５の処理を繰り返す。図６は図５のステップＳ２とステップＳ３の検索処理の処理フローである。また、図１の信号変化関係（３）で示された内部信号や出力信号の変化関係の指定が不充分である場合は、図５のステップＳ２で検索される一致部分に、余分なものまで検出されたりするが、その場合は、設計者が該信号変化関係に新たに関係を追加すると、余分なものは除外される。

【００１２】図７に、図１の信号変化関係（３）を表す内部表現データ（１０）の表現方法の概略の１例を示す。図７は、図２或いは図３或いは図４で示された信号変化関係を表したものである。

【００１３】図８は、図１のシミュレーション結果データ（４）のテキスト表示（１１）の１例である。図９

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は、図８に示したシミュレーション結果データの内部表現データ（１２）の表現方法の概略の１例の一部である。

【００１４】図１０は、図１の比較結果（６）、つまり、図５のステップＳ３で出力された結果のテキスト表示（１３）の１例である。図５での処理について、図７に示した信号変化関係と図９に示したシミュレーション結果の場合について、具体的に説明する。図７の信号変化関係データから関係する信号として、入力信号が２個、信号Ａと信号Ｂがあり、出力信号が１個、信号ＤＯ（０ｔｏ３）があることが解る。従って、図９のシミュレーション結果データから、関係する信号として、信号Ａ，信号Ｂ，信号ＤＯ（０ｔｏ３）の各信号変化データを取り出す。次に、図７の信号変化関係データから、入力信号の信号変化の関係を取り出す。図７では、信号Ａが１に変化し、次に、信号Ｂが１に変化し、次に信号Ｂが０に変化する、という関係が解る。この後に、信号Ｂの０への変化の次に信号ＤＯの００００への変化があるが、信号ＤＯは出力信号であるので、これは、期待される動作（シミュレーション結果或いは期待値が一致すべき動作）であると解る。この入力信号の関係に対応する部分を図９のシミュレーション結果データから検索する。図９のシミュレーション結果データの信号Ａの変化データより、信号Ａが１に変化するのが時刻３００であることが解る。そして、信号Ｂの変化データで、時刻３００の後で１に変化するデータとして、時刻４００に１に変化するのが解る。信号Ｂの変化データで、時刻４００の後の変化として、時刻６００に０に変化することが解る。従って、この場合、図７に示した入力信号の信号変化関係を満たすものが、図９のシミュレーション結果データの時刻３００から時刻６００に存在することが解る。ここで、信号Ｂの時刻６００の次の信号変化が時刻８００にあることが解り、シミュレーション結果データの一致判定範囲として時刻３００から時刻８００とする。もし、信号Ｂの時刻６００の変化が信号Ｂの変化の最後であったら、時刻３００から関係信号の最後の変化の時刻までを一致判定範囲とする。次に、先程の図７の信号変化関係データからの信号変化の関係の取り出しにおいて、期待される動作として、信号Ｂの０への変化の次に信号ＤＯの００００への変化があり、ここでの例ではこの関係のみである。この期待される動作の関係を図９のシミュレーション結果データの時刻３００から時刻８００の範囲で調べる。信号Ｂは時刻６００に０に変化しており、信号ＤＯは時刻７００に００００に変化しており、この場合、期待される動作、信号Ｂの０への変化の次に信号ＤＯの００００への変化、に一致していると判定する。

第２の発明

図１１は、第２の発明の論理検証システムに関する部分のシステム構成図の１例である。図１１において、データ（１４）は、シミュレーション結果或いはシミュレーションの期待動作として与えられた期待値のデータである。データ（１５）は、該符号１のシミュレーション結果とは別の、例えば、論理回路修正後の新たなシミュレーション結果である。結果比較部（１６）は、該符号１，該符号２のシミュレーション結果同士、或いは、シミュレーション期待値とシミュレーション結果との一致不一致を比較する部分である。表示部（１７）は、該符号３で比較した不一致部分を表示するための処理をする部分である。ディスプレイ（１８）は、該符号４で作成された不一致部分の表示を表示するものである。時間幅入力（１９）は、該表示される不一致部分に対して、時間幅を入力して、該符号１６、該符号１７で示した部分において不一致となる部分を絞り込むための、入力用キーボードである。

【００１５】図１２は、図１１の旧シミュレーション結果或いはシミュレーション期待値データ（１４）のテキスト表示（２０）の１例の一部分である。図１３は、図１１の新シミュレーション結果データ（１５）のテキスト表示（２１）の１例の一部分である。図１２，図１３に示したテキスト表示に対する内部表現データの表現方法は、例えば、第１の発明の図９に示したような方法で行う。

【００１６】図１４は、該図１２と該図１３に示したシミュレーション結果同士或いはシミュレーション期待値とシミュレーション結果を比較した結果の表示例（２２）である。図１４において、時刻５００の信号Ｃの値１と、時刻６００の信号ＤＯの値ＸＸＸＸが、不一致であり、信号の値が強調表示（反転表示）されている。時刻５１０と時刻６４０の各信号の値は一致しているが、時刻５００と時刻６００の不一致状況・原因を設計者が理解しやすいように表示している。

【００１７】図１５は、該図１４の結果において不一致となったものに対して、ある指定された時間幅の不一致は不一致としないようにして表示した１例（２３）である。ここで、不一致としない時間幅として、基準となるシミュレーション期待値或いはシミュレーション結果に対して、＋０，＋１５が指定された。従って、基準となる該図１２に示した信号変化に対して、＋１５時刻の間の信号変化の不一致は不一致とは見なされない。そこで、時刻５００から５１０の間の信号Ｃの不一致は不一致としては表示されず、時刻６００から６４０の間の信号ＤＯが（時刻６１５から６４０までが不一致となる）、不一致として表示される。このようにして、論理動作の異なるところ、或いは、論理動作は一致しているがディレイが無視できない程大きくなっている部分を抽出できる。

【００１８】図１２と図１３の信号変化関係のデータの場合について、具体的に説明する。図１２における信号変化関係で、信号Ｃの信号変化は、時刻０に値０，時刻

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５００に値１，時刻５５０に値０であり、信号ＤＯの信号変化は、時刻０にＸＸＸＸ，時刻６００に値０００００である。図１３における信号変化関係で、信号Ｃの信号変化は、時刻０に値０，時刻５１０に値１，時刻５５０に値０であり、信号ＤＯの信号変化は、時刻０に値ＸＸＸＸ，時刻６４０に値０００００である。先ず、時間幅を考慮しない場合の比較では、図１２の信号Ｃの時刻５００値１の変化に対して、図１３の信号Ｃの時刻５１０値１の変化と図１２の信号ＤＯの時刻６００値００００の変化に対して、図１３の信号ＤＯの時刻６４０値００００の変化が不一致となる。次に、時刻幅が指定されて、本例では、図１２の信号変化に対して時間幅＋１５以内に図１３の信号変化が一致している場合は、一致すると見なす。信号Ｃの場合は、時刻５００の値１と時刻５１０の値１の変化が不一致となったが、時間幅を考慮した時刻５００から５１５の間で値１で一致しているので一致と見なされる。信号ＤＯの場合は、時刻６００の値００００と時刻６４０の値００００の変化が不一致となり、時間幅を考慮した時刻６００から６１５の間で値が一致しないので不一致と見なされる。

【００１９】図１６は、該図１４の例の不一致となった信号に対応して、機能記述上の対応する文を強調表示（反転表示）（２４）した例である。図１７は、該図１５の例の不一致となった信号に対応して、論理接続記述上の対応する文を強調表示（反転表示）（２５）した例である。

【００２０】

【発明の効果】以上説明したように本発明によれば、論理回路システムの動作検証をシミュレータなどで行う場合に、シミュレーション結果の０，１等の信号変化を見て期待どおりの動作を行っているかを確認する作業、或いは、期待する動作として出力信号などの注目する信号の０，１等の信号変化を予め用意して比較する作業を、自動化することにより、誤りの発生や膨大な作業時間を削減できる。また、作成した入力テストパターンに、動作検証項目として考えていた動作が含まれていないことを見落とすことを減少させ、検証抜けを防止できる。これにより、設計検証の効率を向上させることができる。また、シミュレーション結果同士、或いは、シミュレーション結果と期待動作信号変化を比較する場合に、一方の信号の信号変化の時刻に幅を持たせて比較することができることにより、期待動作との不一致を選択でき、効率的に動作確認を行える。

【図面の簡単な説明】

【図１】　図１の発明の論理検証システムに関する部分のシステム構成図。

【図２】　波形表示を用いて回路動作を指定した指定例の１例を示す波形図。

【図３】　使う動詞等が限定された言葉を用いて、図２に示した波形の変化関係と同様のことを表現した図。

【図４】　時相論理を用いて図２，図３に示した信号の変化関係と同様のことを表現した図。

【図５】　図１における対応関係抽出比較部（５）の処理フロー概略の１例を示すフローチャート。

【図６】　対応関係抽出比較部のサブ処理フロー概略の１例であり、図５で示した検索処理の処理フローチャート。

【図７】　図１の信号変化関係（３）を表す内部表現データの表現方法の概略の１例を示す図。

【図８】　図１のシミュレーション結果データ（４）のテキスト表示の１例を示す図。

【図９】　図８に示したシミュレーション結果データの内部表現データの表現方法の概略の１例の一部を示す図。

【図１０】　図１の比較結果（６）、つまり、図６のステップＳ３で出力された結果のテキスト表示の１例を示す図。

【図１１】　第２の発明の論理検証システムに関する部分のシステム構成図。

【図１２】　図１１の旧シュミレーション結果或いはシミュレーション期待値データのテキスト表示の１例の一部分を示す図。

【図１３】　図１１の新シュミレーション結果データのテキスト表示の１例の一部分を示す図。

【図１４】　図１１と図１３に示したシミュレーション結果同士或いはシュミレーション期待値とシミュレーション結果を比較した結果の表示例を示す図。

【図１５】　図１４の結果において不一致となったものに対して、ある指定された時間幅の不一致は不一致としないようにして表示した１例を示す図。

【図１６】　図１５の例の不一致となった信号に対応して、機能記述上の対応する文を強調表示（反転表示）した例示図。

【図１７】　図１５の例の不一致となった信号に対応して、論理接続記述上の対応する文を強調表示（反転表示）した例示図。

【符号の説明】

１…設計者によって与えられる指定回路動作

２…指定回路動作（１）から信号変化関係を抽出する信号変化関係抽出部

３…信号変化関係抽出部（２）で抽出された信号変化関係を示す内部表現データ

４…シミュレータの入力となる入力テストパターンデータまたはシミュレーションの出力であるシミュレーション結果データ

５…信号変化関係データ（３）と入力テストパターンデータ或いはシミュレーション結果データ（４）より、信号変化関係データ（３）で示された入力信号の信号変化関係が入力テストパターンデータ（４）の中に存在するかどうか、或いは、信号変化関係データ（３）で示され

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た入力信号の信号変化関係に一致するものがシミュレーション結果データ（４）の中に存在するかどうかを調べ、存在した場合には、３の信号変化関係データで示された入力信号，内部信号，出力信号の信号変化関係と４のシミュレーション結果データの信号変化関係が一致するかどうかを調べる、対応関係抽出比較部

６…対応関係抽出比較部（５）で比較された存在の有無，一致不一致の結果表示

Ｓ１…関係する信号データ取り出し

Ｓ２…入力信号の信号変化関係の一致検索

Ｓ３…内部信号，出力信号の信号変化関係の一致検索

Ｓ４…検索結果の出力

Ｓ５…入力信号の信号変化関係検索開始時刻更新

Ｓ６…該当入力テストパターン無し

１４…シミュレーション結果或いはシミュレーションの期待動作として与えられた期待値のデータ

１５…シミュレーション結果とは別のシミュレーション結果

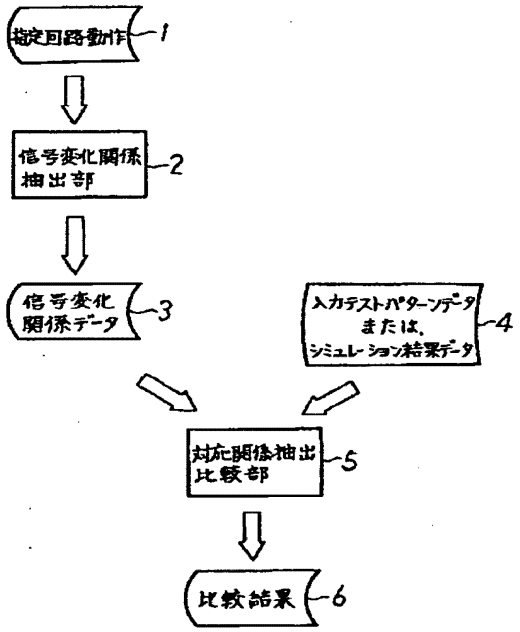
１６…シミュレーション結果同士、或いは、シミュレーション期待値とシミュレーション結果との一致不一致を比較する結果比較部

１７…結果比較部で比較した不一致部分を表示するための表示部

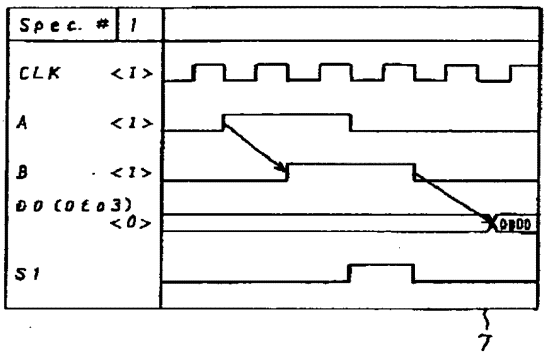
１８…表示部で作成された不一致部分の表示を表示するディスプレイ

１９…表示される不一致部分に対して、時間幅を入力して、結果比較部と表示部において不一致となる部分を絞り込むための、入力用キーボード

【図１】



【図２】



【図３】

Spec. #	
1	入力信号Aがたちあがった後に，入力信号Bが立ち上がり，入力信号Bが立ち上がった後に，出力信号D0が0000に変化する。

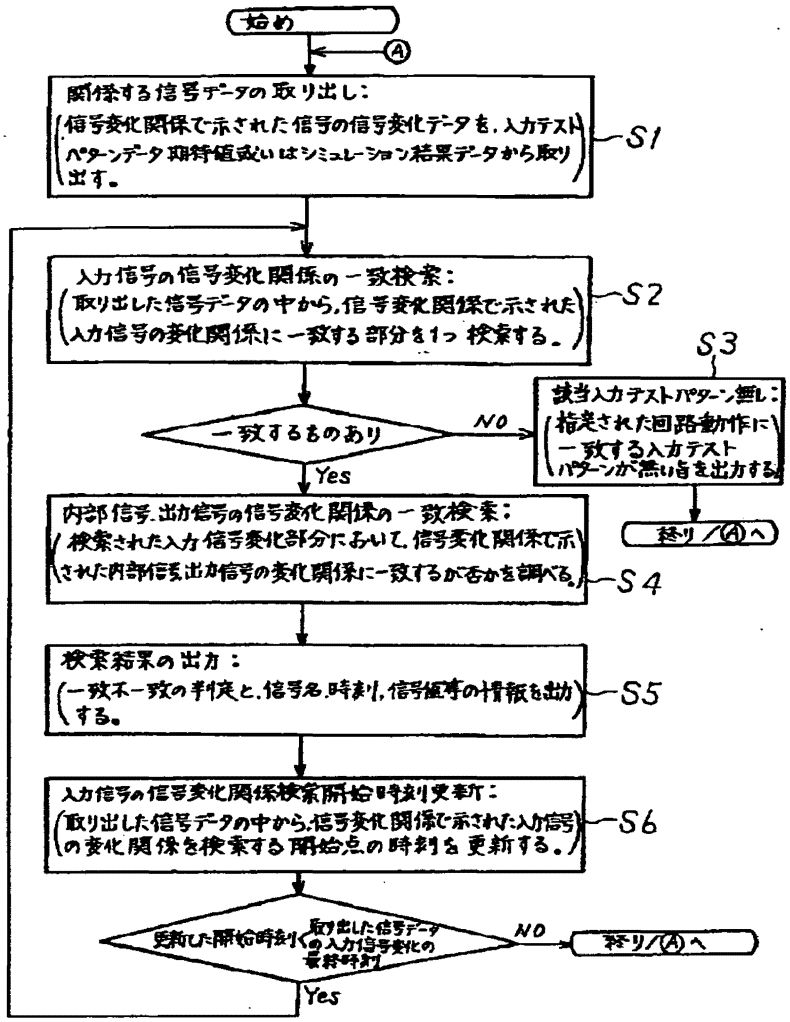
8

【図４】

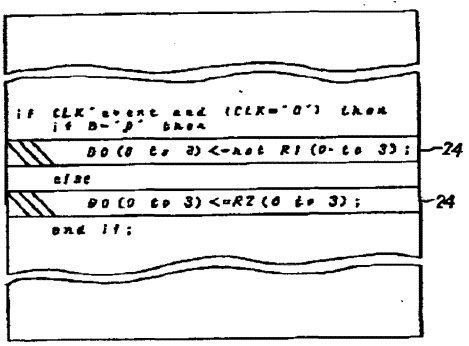
Spec. #	
1	(~A∧○A)→○(~B∧○B)，(~B∧○B)→○(B∧○(~B))，(B∧○(~B))→○(~D00∧~D01∧~D02∧~D03)；

9

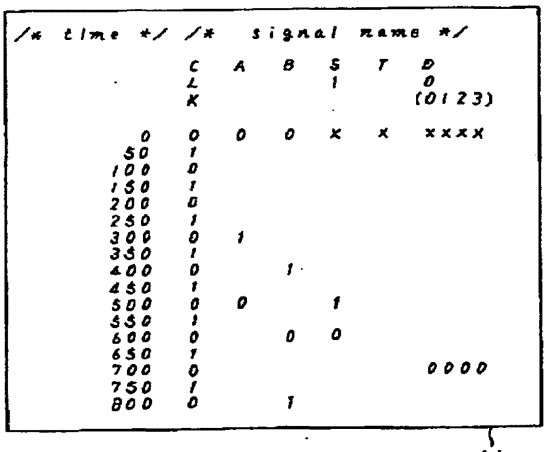
【図５】



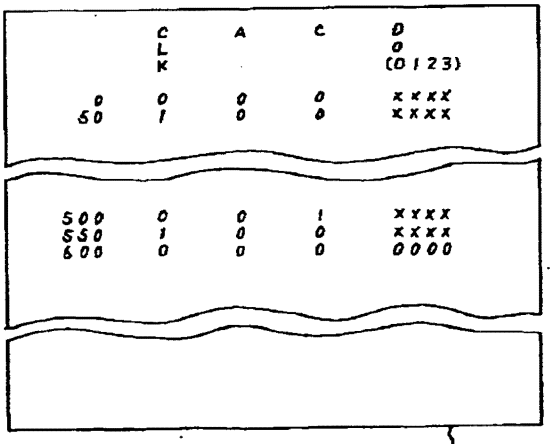
【図１６】



【図８】



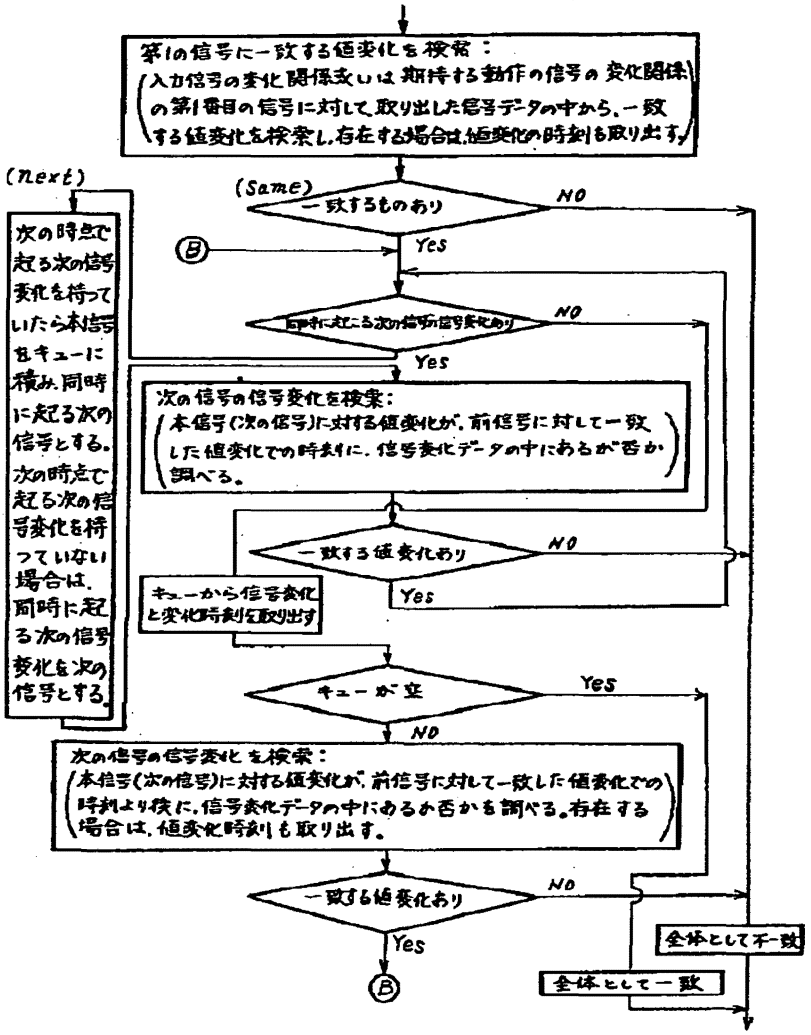
【図１２】



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【図６】



【図１４】

	CLK	A	C	D0 (0123)
500	0	0	1	XXXX
610	0	0	1	XXXX
600	0	0	0	XXXX
640	0	0	0	0000

22

【図１５】

	CLK	A	C	D0 (0123)
time width (+0, +15)				
600	0	0	0	XXXX
640	0	0	0	0000

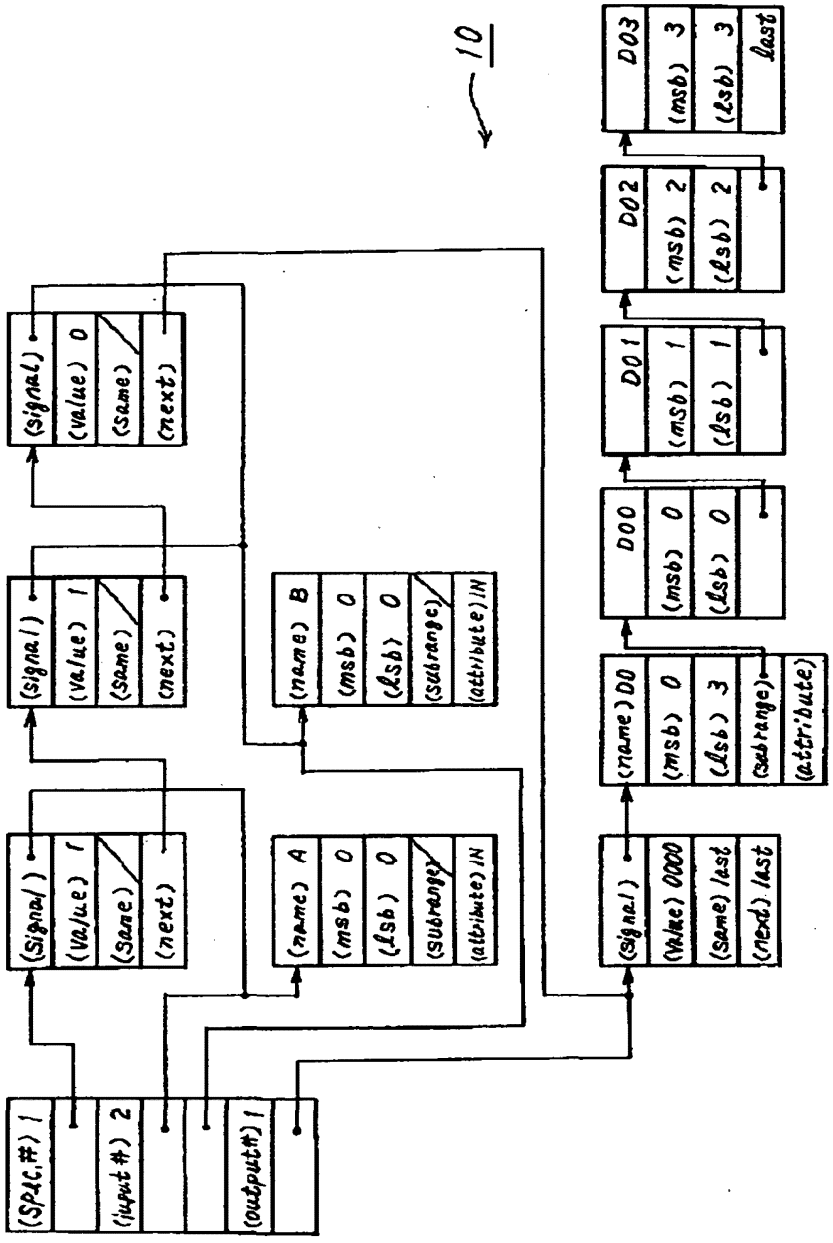
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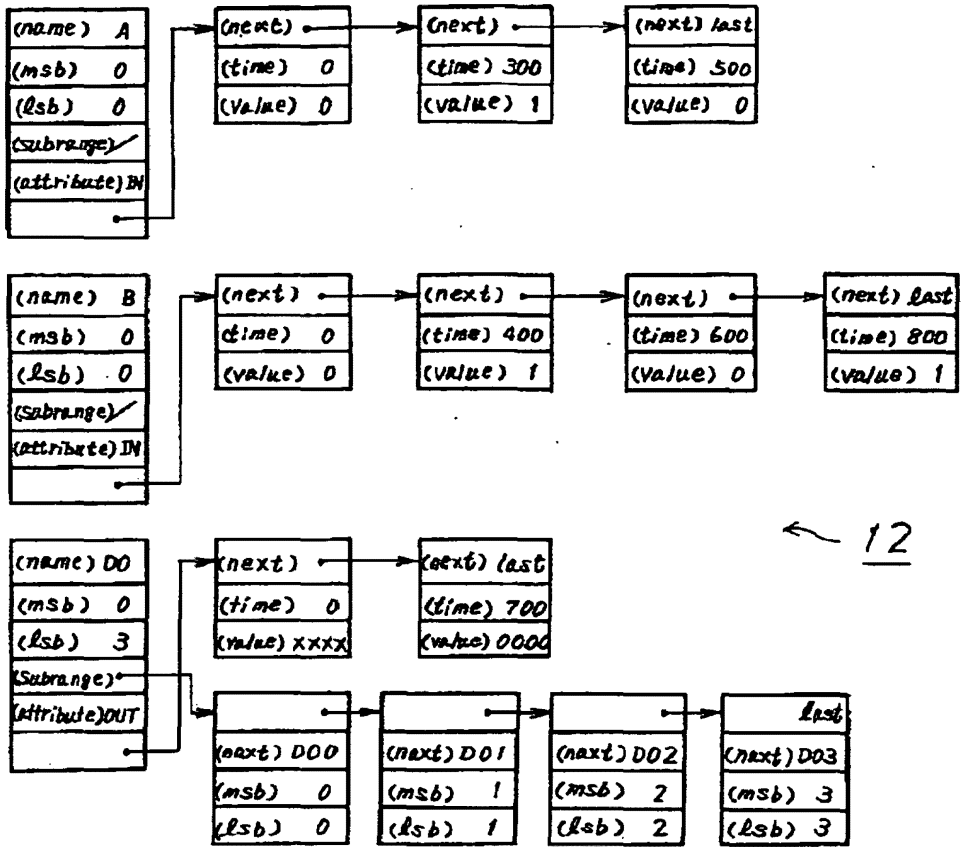
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【図7】

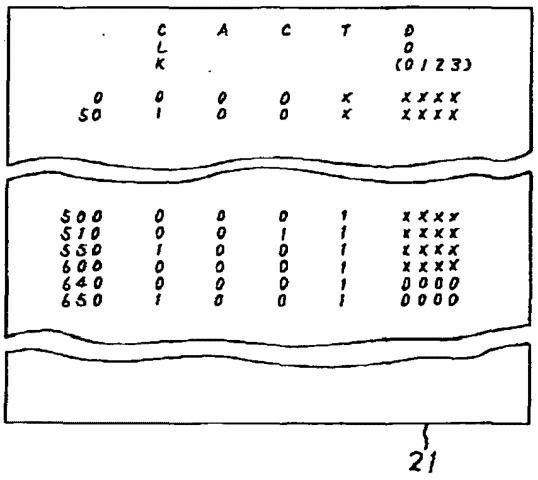


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【図９】

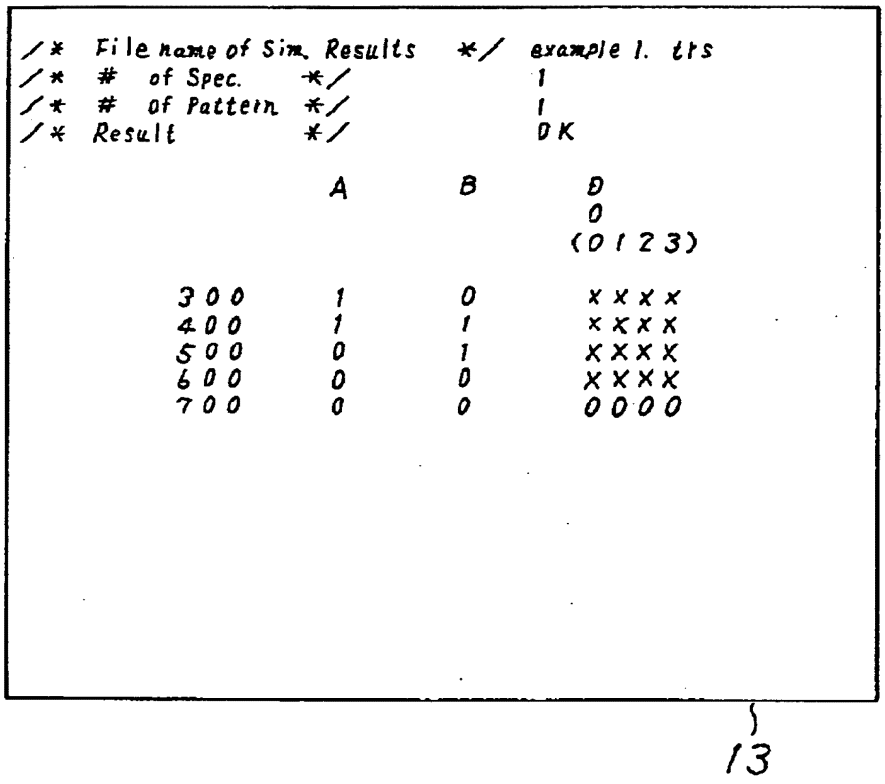


【図１３】

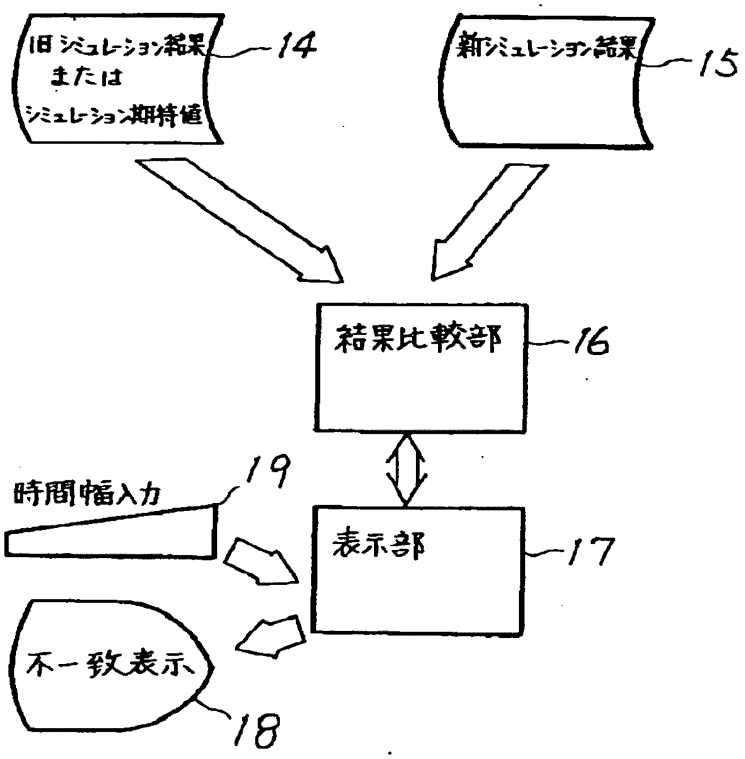


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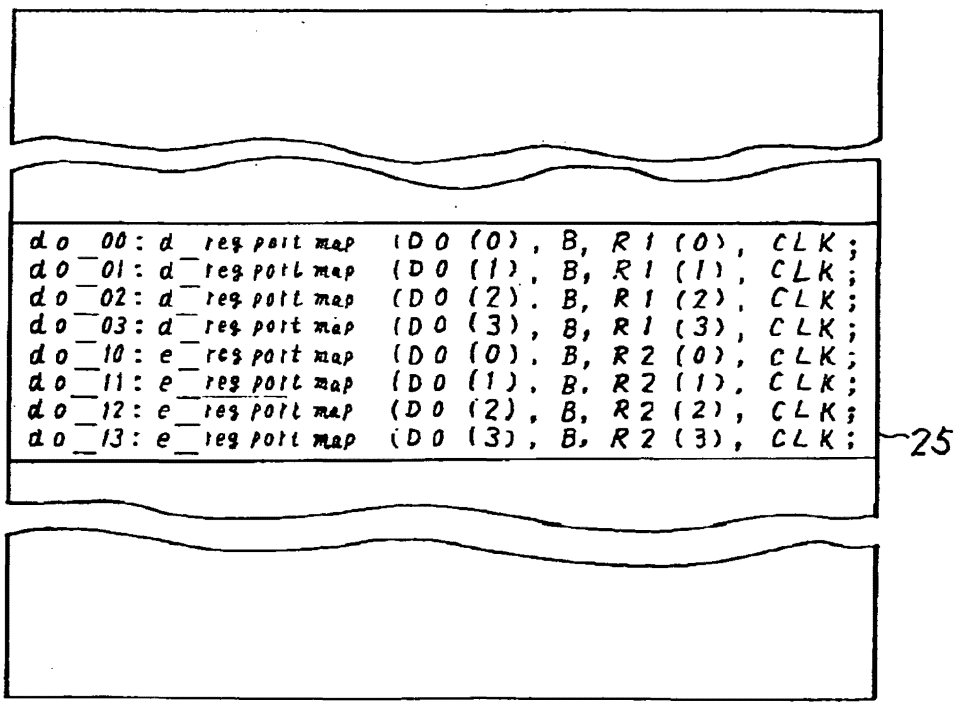
【図１０】


/* File name of Sim. Results */ example 1. trs
/* # of Spec. */ 1
/* # of Pattern */ 1
/* Result */ OK
A
B
D
0
(0 1 2 3)
300 1 0 xxxx
400 1 1 xxxx
500 0 1 XXXX
600 0 0 XXXX
700 0 0 0000
13

【図１１】



【図１７】



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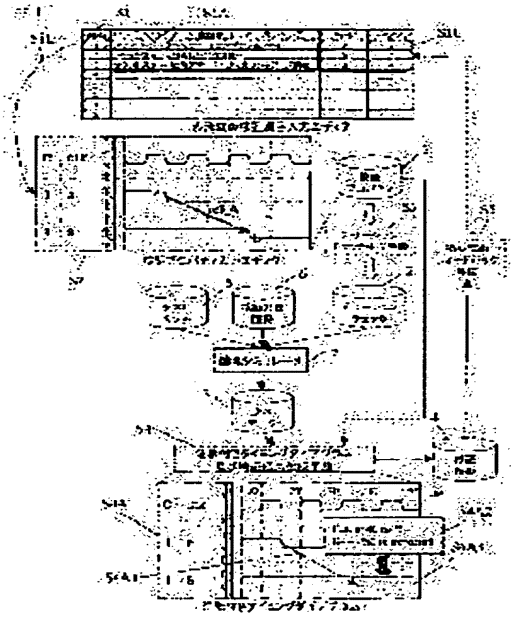
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(21)Application number : 2003-123402
(22)Date of filing : 28.04.2003

(71)Applicant : RENESAS TECHNOLOGY CORP
(72)Inventor : KAMATA TAKEROO

(54) LOGIC VERIFICATION PROGRAM AND RECORDING MEDIUM

(57)Abstract:
PROBLEM TO BE SOLVED: To improve the logic verification efficiency.
SOLUTION: The logic verification program allows a personal computer 100 to function as a verification item input editor (S1) which enables an input of a verification item in a natural language on a tabular display screen and to function as a verification result feedback means (S5) which enables the creation of a test report by feeding-back the verification result to the verification item input editor. The processing of the personal computer 100 reduces the time required for creating the test report as compared with the case of manual operation, and also reduces man-made mistakes due to the unnecessity for troublesome manual operations.



LEGAL STATUS

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	G06F	17/50	672C	

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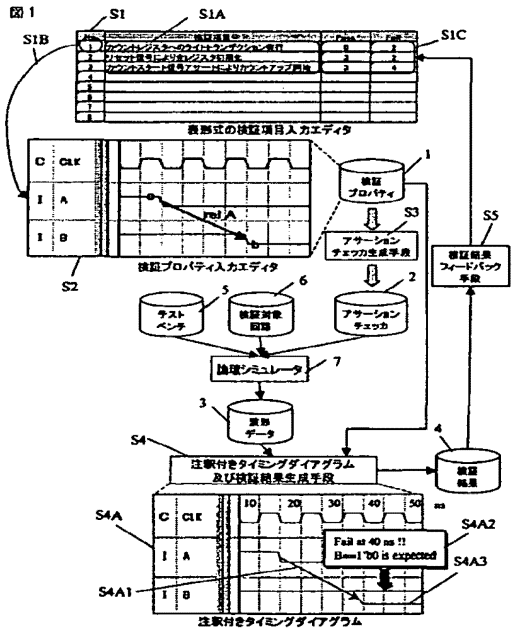
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Fターム(参考)　5B046 AA08　BA03　DA01　JA05

(54)【発明の名称】論理検証プログラム及び記録媒体

(57)【要約】
【課題】論理検証効率の向上を図る。
【解決手段】論理検証プログラムにより、パーソナルコンピュータ１００を、表形式の表示画面において検証項目の自然言語による入力を可能とする検証項目入力エディタ（Ｓ１）、検証結果を上記検証項目入力エディタにフィードバックすることでテストレポートの生成を可能とする検証結果フィードバック手段（Ｓ５）として機能させる。パーソナルコンピュータ１００での処理によれば、人手作業によってテストレポートを作成するのに比べて短時間で済むし、人手作業による煩雑な作業が不要とされることで人為的なミスも低減される。
【選択図】　図１



【特許請求の範囲】
【請求項１】
コンピュータを、表形式の表示画面において検証項目の自然言語による入力を可能とする検証項目入力エディタ、
検証結果を上記検証項目入力エディタにフィードバックすることでテストレポートの生成を可能とする検証結果フィードバック手段、として機能させることを特徴とする論理検証プログラム。
【請求項２】
コンピュータを、表形式の表示画面において検証項目の自然言語による入力を可能とする検証項目入力エディタ、
上記検証項目入力エディタにリンクされ、検証プロパティを検証言語で作成可能な検証プロパティ入力エディタ、
上記検証プロパティに基づいてアサーションチェッカを生成するアサーションチェッカ生成手段、
上記アサーションチェッカに基づく論理シミュレーションによって得られた波形データと上記検証プロパティとに基づいて注釈付きタイミングダイアグラム及び検証結果を生成するための注釈付きタイミングダイアグラム及び検証結果生成手段、
上記検証結果を上記検証項目入力エディタにフィードバックすることでテストレポートの生成を可能とする検証結果フィードバック手段、として機能させることを特徴とする論理検証プログラム。
【請求項３】
上記注釈付きタイミングダイアグラム及び検証結果生成手段は、上記検証プロパティに基づいて状態遷移グラフを生成するための状態遷移グラフ生成手段と、
上記状態遷移グラフと上記波形データとに基づいて注釈情報付き波形データ及び上記検証結果を得る状態遷移グラフトレース手段と、を含む請求項２記載の論理検証プログラム。
【請求項４】
請求項１乃至３の何れか１項記載の論理検証プログラムを記録したコンピュータ読み取り可能な記録媒体。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は、論理デバッグ技術、さらには、コンピュータによって実行可能な論理検証プログラム、及びその論理検証プログラムを記録したコンピュータ読み取り可能な記録媒体に関する。
【０００２】
【従来の技術】
論理回路等の設計工程においては、設計した論理回路の論理機能やタイミング等を検証するツールとして論理シミュレータや波形ビューアが用いられる。論理シミュレータでは、半導体素子の回路情報を記述したネットリストを半導体素子の仕様に合わせて作成したテストパターンを記述したテストベクタに基づいてシミュレーションが行われる。波形ビューアでは、上記シミュレーションの結果が波形表示される。波形ビューアでは、横軸を時間軸とし、縦軸方向に信号名を羅列し、各信号の時間的な変化を波形表示することが行われる。設計者は、この波形ビューアによる波形表示に基づいて、シミュレーション結果が仕様と一致しているかどうかを確認する。
【０００３】
波形表示を見やすくするための方法としては、例えば指定したトリガ信号の値の変化に従ってその表示色を変化し、トリガ信号の値の変化に依存して変化した信号線の値をトリガ信号と同色で表示することが知られている（例えば特許文献１参照）。
【０００４】
【特許文献１】

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特開平７－２１２４４号公報
【０００５】
【発明が解決しようとする課題】
波形表示ツールとしての波形ビューアによる波形表示に基づく論理検証においては、検証言語で記述した回路が満たすべき性質（以下、「検証プロパティ」という）の識別子と検証結果を表形式で表示し、検証プロパティを満たさなかったイベントを波形ビューア上で強調表示することができる。しかしながら、そのような波形表示ツールによれば、自然言語で検証項目を記述することができないため、テスト仕様書やテストレポートを別途、エディタ等で作成しなければならない。この結果、テスト仕様書、検証プロパティ、及びテストレポートの作成及び修正は全て人手によって行われる。また、テスト仕様書作成に用いるエディタに検証項目のバージョン管理機能がないため、更新履歴の作成を人手作業で行う必要がある。このように従来技術によれば、人手作業が多く、工数の増加及び人為的なミスを生じ易い。
【０００６】
さらに、タイミングチャート上でバグ原因を解析するする際は、シミュレーション結果が示すイベント間の論理的関係を正確に理解することが前提条件とされる。タイミングチャート上でイベント間の論理的関係を表現する手段として、従来から「注釈付きタイミングダイヤグラム（ａｎｎｏｔａｔｅｄ　ｔｉｍｉｎｇｄｉａｇａｍ）」が用いられてきた。検証エンジニアは、バグ原因解析の際に、上記注釈付きタイミングダイヤグラムを自分で脳裏で作成している。しかし、脳裏で作成できないほどイベント間の論理的関係が複雑な場合や、バグ原因を第三者に説明する必要がある場合、あるいは記録として残す場合には、波形表示ツール上のタイミングチャートを紙に印刷し、それにペンで注釈を書き加えることにより、イベント間の論理的関係をタイミングチャート上で視覚化する。しかし、その作業は煩雑であり、検証工数の増加を余儀なくされる。
【０００７】
本発明の目的は、論理検証の効率向上を図ることにある。
【０００８】
本発明の前記並びにその他の目的と新規な特徴は本明細書の記述及び添付図面から明らかになるであろう。
【０００９】
【課題を解決するための手段】
本願において開示される発明のうち代表的なものの概要を簡単に説明すれば下記の通りである。
【００１０】
すなわち、第１手段は、論理検証プログラムによって、コンピュータを、表形式の表示画面において検証項目の自然言語による入力を可能とする検証項目入力エディタ、検証結果を上記検証項目入力エディタにフィードバックすることでテストレポートの生成を可能とする検証結果フィードバック手段として機能させる。
【００１１】
上記第１手段によれば、コンピュータでの処理により表形式の検証項目入力エディタの表示画面に、検証結果がフィードバックされることでテストレポートが作成される。コンピュータでの処理によれば、人手作業による場合よりも短時間でテストレポートを作成することができる。また、上記テストレポートの作成において人手作業による煩雑な作業が省略されるため、人為的なミスも低減される。このことが、論理検証効率の向上を達成する。また、上記検証項目入力エディタは、検証項目の自然言語による入力を可能とすることで、検証項目の入力の容易化を達成する。
【００１２】
第２手段は、論理検証プログラムによって、コンピュータを、表形式の表示画面において検証項目の自然言語による入力を可能とする検証項目入力エディタ、上記検証項目入力エディタにリンクされ、検証プロパティを検証言語で作成可能な検証プロパティ入力エディ

タ、上記検証プロパティに基づいてアサーションチェッカを生成するアサーションチェッカ生成手段、上記アサーションチェッカに基づく論理シミュレーションによって得られた波形データと上記検証プロパティとに基づいて注釈付きタイミングダイアグラム及び検証結果を生成するための注釈付きタイミングダイアグラム及び検証結果生成手段、上記検証結果を上記検証項目入力エディタにフィードバックすることでテストレポートの生成を可能とする検証結果フィードバック手段として機能させる。

【００１３】

上記のようにタイミングチャート上でバグ原因を解析するする際は、シミュレーション結果が示すイベント間の論理的関係を正確に理解することが前提条件とされ、タイミングチャート上でイベント間の論理的関係を表現する手段として、従来から「注釈付きタイミングダイヤグラム」が用いられてきたが、その人手による作成作業は煩雑であり、検証工数の増加を余儀なくされる。

【００１４】

しかし、上記第２手段によれば、注釈付きタイミングダイヤグラム及び検証結果生成手段により、注釈付きタイミングダイヤグラムが作成され、上記検証結果を上記検証項目入力エディタにフィードバックすることでテストレポートが作成される。コンピュータでの処理によれば、人手による場合よりも、注釈付きタイミングダイヤグラムやテストレポートを短時間で作成することができる。また、注釈付きタイミングダイヤグラムやテストレポートの作成において人手作業にる煩雑な作業が省略されるため、人為的なミスも低減される。このことが、論理検証効率の向上を達成する。

【００１５】

上記注釈付きタイミングダイアグラム及び検証結果生成手段は、上記検証プロパティに基づいて状態遷移グラフを生成するための状態遷移グラフ生成手段と、上記状態遷移グラフと上記波形データとに基づいて注釈情報付き波形データ及び上記検証結果を得る状態遷移グラフトレース手段とを含んで構成することができる。

【００１６】

【発明の実施の形態】

図１０には、本発明にかかる論理検証プログラムが実行されるパーソナルコンピュータシステムが示される。

【００１７】

図１０に示されるパーソナルコンピュータシステム１００は、特に制限されないが、本発明にかかる論理検証プログラムを実行することで、論理検証のための各種機能を発揮するマイクロコンピュータ１０２と、外部との間で各種情報のやり取りを可能とする外部インタフェース１０１、上記マイクロコンピュータ１０２で実行される各種プログラムや各種データ等が格納されたハードディスク装置や、上記マイクロコンピュータ１０２での演算処理における作業領域などに使用される半導体記憶装置などを含む記憶装置１０４、上記マイクロコンピュータ１０２での演算結果や必要とされる各種情報を表示可能な表示装置１０３を含んで成る。また、上記マイクロコンピュータ１０２で実行されるプログラムは、プログラム提供者からネットワーク２００を介してパーソナルコンピュータシステム１００に送られる場合と、可搬型記憶媒体３００を介してパーソナルコンピュータシステム１００にロードされる場合とがある。本発明に係る論理検証プログラムは、ネットワーク２００を介して、あるいは可搬型記憶媒体３００を介して記憶装置１０４に格納される。上記可搬型記憶媒体３００には、フロッピィディスク、ＣＤ－ＲＯＭ、磁気ディスク、光ディスク、光磁気ディスクなどの各種ディスクが含まれる。ここで、上記記憶装置１０４や可搬型記憶媒体３００は、論理検証プログラムを記録したコンピュータ読み取り可能な記録媒体の一例とされる。

【００１８】

図１には、上記マイクロコンピュータ１０２において論理検証に関する所定のプログラムが実行されることで実現される論理検証ツールの全体的な構成例が示される。

【００１９】

図１に示される論理検証ツールは、特に制限されないが、検証項目入力エディタＳ１、検証プロパティ入力エディタＳ２、アサーションチェッカ生成手段Ｓ３、注釈付きタイミングダイヤグラム及び検証結果生成手段Ｓ４、検証結果フィードバック手段Ｓ５、及び論理シミュレータ７を含む。

【００２０】

上記検証項目入力エディタＳ１は、バージョン管理機能を備え、且つ、表形式で検証項目Ｓ１Ａの入力を可能とする。検証項目Ｓ１Ａの入力は、入力の容易化を図るため、自然言語で行うことができるようになっている。特に制限されないが、検証項目入力エディタＳ１によって入力された検証項目の例としては、「カウントレジスタへのライトトランザクション実行」、リセット信号により全レジスタ初期化」、「カウントスタート信号アサートによりカウントアップ開始」などを挙げることができる。

【００２１】

検証プロパティ入力エディタＳ２は、検証プロパティの入力を可能とする。検証プロパティ入力エディタＳ２は、検証項目にリンクしており（ＳＢ１）、この検証プロパティ入力エディタＳ２を用いて検証プロパティ１を検証言語で作成することができる。

【００２２】

アサーションチェッカ生成手段Ｓ３は、特定デザインがどのように振る舞うか、あるいは振る舞ってはいけないかをチェックするためのアサーションチェッカ２を上記検証プロパティ１に基づいて生成する。

【００２３】

論理シミュレータ７は、テストベンチ５、検証対象回路６、アサーションチェッカ２の各情報を読み込んで論理シミュレーションを実行する。そしてこの論理シミュレーションの結果として波形データ３が得られる。

【００２４】

注釈付きタイミングダイヤグラム及び検証結果生成手段Ｓ４は、上記波形データＳ４と上記検証プロパティ１とに基づいて検証結果４を生成するとともに、注釈付きタイミングダイヤグラムＳ４Ａを生成する。生成された検証結果生成された検証結果４は、テストレポート作成のため、検証結果フィードバック手段Ｓ５により上記検証項目入力エディタＳ１にフィードバックされる。

【００２５】

上記注釈付きタイミングダイヤグラムの表示画面は、実際のシミュレーション波形に、イベント間の論理的関係を示す注釈記号Ｓ４Ａ１、エラーメッセージＳ４Ａ２、及び波形の期待値Ｓ４Ａ３を含む。上記検証項目入力エディタＳ１の表示画面における検証結果Ｓ１Ｃと注釈付きタイミングダイヤグラムＳ４Ａはリンクしており、検証プロパティ１を満たす（Ｐａｓｓ）、それを満たさない（Ｆａｉｌ）項目を選択することにより、対応する注釈付きタイミングダイヤグラムが表示されるようになっている。

【００２６】

次に、上記論理検証ツールを更に詳細に説明する。

【００２７】

図２には、上記検証項目入力エディタＳ１の入力例が示される。図２に示される例では、上記検証項目入力エディタＳ１により、「信号Ａ立ち上がりの３サイクル後に信号Ｂが立ち上がる」という検証項目Ｓ１Ａが自然言語で記述されている。自然言語はパーソナルコンピュータシステム１００におけるキーボードを介して容易に入力することができる。

【００２８】

図３には、検証プロパティの生成及びアサーションチェッカの生成例が示される。

【００２９】

検証項目入力エディタＳ１にリンクしている検証プロパティ入力エディタＳ２を用いて検証プロパティが作成される。より詳細には、検証プロパティＳ２は、検証項目入力エディタＳ１の検証項目検証項目Ｓ１Ａにリンクしている。

【００３０】

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最初に検証プロパティを作成する場合は、例えばマウスなどの入力装置で検証項目Ｓ１Ａを選択することにより検証プロパティ入力エディタＳ２を起動させ、この検証プロパティ入力エディタＳ２に検証プロパティを入力する。一度検証プロパティを入力した後は、例えばマウスなどの入力装置で検証項目Ｓ１Ａを選択することにより、対応する入力済み検証プロパティを検証プロパティ入力エディタＳ２で確認出来る。リンク機構Ｓ１Ｂにより、検証項目と検証プロパティの対応が常に保証される。アサーションチェッカ生成手段Ｓ３に検証プロパティ１が入力されることにより、アサーションチェッカ生成手段Ｓ３においてアサーションチェッカが生成される。

【００３１】

図４には論理シミュレーションの実行及びその結果が示される。

【００３２】

テストベンチ５、検査対象回路２、及びアサーションチェッカを論理シミュレータＳ１で読み込み、論理シミュレーションを実行し、波形データ４を生成する。この波形データ４には、毎サイクルの時刻及びその時刻における信号値（Ａの信号値、Ｂの信号値）が格納されている。

【００３３】

図５には、注釈付きタイミングダイアグラム及び検証結果生成手段Ｓ４の構成例が示される。

【００３４】

注釈付きタイミングダイアグラム及び検証結果生成手段Ｓ４は、図５に示されるように、検証プロパティ１に基づいて状態遷移グラフ８を作成するための状態遷移グラフ生成手段Ｓ６と、この状態遷移グラフ生成手段Ｓ６によって生成された状態遷移グラフ８を波形データ３に基づいてトレースすることで注釈情報付き波形データ９及び検証結果４を得る状態遷移グラフトレース手段Ｓ７とを含む。波形ビューアＳ４Ａは、上記注釈付き波形データ９を読み込んで注釈付きタイミングダイヤグラムを生成する。

【００３５】

図６には、状態遷移グラフ生成手段Ｓ６による状態遷移グラフ生成の流れが示される。

【００３６】

タイミングチャート上の「ａ」は検証プロパティの前提条件を示し、「ｂ」は帰結を示している。検証プロパティ１は、各サイクルにおいて信号がとるべき値を示しており、その値をグラフの各アークに遷移条件として付加することで状態遷移グラフが形成される。「終了ステート」は、後述する状態遷移グラフのトレースの結果、検証プロパティを満たす場合に到達するステートを示している。フェイルステートは、後述する状態遷移グラフのトレースの結果検証プロパティを満たさない場合に到達するステートを示している。

【００３７】

図７には、上記状態遷移グラフトレース手段による注釈情報付き波形データ及び検証結果の生成の流れが示される。

【００３８】

状態遷移グラフのトレースは状態遷移グラフの開始ステートから開始される。波形データから毎サイクルの信号値を読み込み、状態遷移グラフの遷移条件と比較することにより、状態遷移のグラフをトレースすることができる。図７において、ステートにステート名（Ｒｉｓｅ（Ａ），Ｒｉｓｅ（Ｂ））が付されているものは、検証プロパティで定義されているイベントを示しており、上記ステートを通過したならば、当該ステートに到達した時刻、及び当該ステートから抜けた時刻がステート名と共に注釈情報付き波形データ書込まれる。本例では、時刻５０（ｎｓ）において、波形データの信号値Ｂの値が「０」、検証プロパティから期待される信号値が「１」であるため、フェイルステートに遷移している。フェイルステートに遷移したならば、もう一方のステートへの遷移条件である信号の期待値を取得する。この信号の期待値に基づいてフェイルした時刻における信号値が注釈付き波形データに書込まれる。フェイルステートに遷移したならば、フェイルしたプロパティ名、時刻、検証結果がファイルに書込まれる。

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【００３９】
図８には、注釈付き波形データに基づいて生成された注釈付きタイミングダイヤグラムが示される。検証結果に基づいてエラーメッセージ８０が表示される。また、注釈情報付き波形データに格納されている信号値の期待値に基づいて、期待される信号波形が実際の波形に重ねて表示される。注釈情報付き波形データに格納されているイベントの情報に基づいて、イベントの論理的関係を示す矢印記号８１が表示される。
【００４０】
図９には検証結果のフィードバックの様子が示される。
【００４１】
図９に示されるように、検証結果４が検証結果フィードバック手段Ｓ５により検証項目入力エディタＳ１にフィードバックされる。検証項目入力エディタＳ１において、パス（Ｐａｓｓ）項目には検証プロパティを満たした回数の合計（図９の例では「０」）が示され、フェイル（Ｆａｉｌ）項目には検証プロパティを満たさなかった回数の合計（図９の例では「１」）が表示される。
【００４２】
上記の例によれば、以下の作用効果を得ることができる。
【００４３】
（１）表形式の検証項目入力エディタＳ１の表示画面に、検証結果がフィードバックされることでテストレポートが作成される。パーソナルコンピュータ１００での処理は、人手作業によってテストレポートを作成するのに比べて短時間で済むし、上記テストレポートの作成において人手作業による煩雑な作業が省略されるため、人為的なミスも低減され、それによって論理検証効率の向上を達成することができる。
【００４４】
（２）タイミングチャート上でバグ原因を解析するする際は、シミュレーション結果が示すイベント間の論理的関係を正確に理解することが前提条件とされ、タイミングチャート上でイベント間の論理的関係を表現する手段として、従来から「注釈付きタイミングダイヤグラム」が用いられてきたが、その人手による作成作業は煩雑であり、検証工数の増加を余儀なくされる。これに対して、注釈付きタイミングダイヤグラム及び検証結果生成手段Ｓ４により、注釈付きタイミングダイヤグラムＳ４Ａが作成され、表形式の検証項目入力エディタＳ１の表示画面に検証結果がフィードバックされることでテストレポートが作成される。パーソナルコンピュータ１００での処理は、注釈付きタイミングダイヤグラムやテストレポートを人手作業によって作成するのに比べて短時間で済む。また、注釈付きタイミングダイヤグラムやテストレポートの作成において人手作業にる煩雑な作業が省略されるため、人為的なミスも低減され、それによって論理検証効率の向上を達成することができる。
【００４５】
（３）上記（１），（２）の作用効果により、ＩＰ購入側に対して、自社ＩＰコアの品質を定量的に示すことができる資料を提供することができる。
【００４６】
以上本発明者によってなされた発明を具体的に説明したが、本発明はそれに限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。
【００４７】
例えば論理シミュレータは、図１に示される論理検証ツールとは別プログラムとして提供することができる。また、注釈付きタイミングダイアグラムにおける注釈には、矢印記号のみならず、直線や曲線あるいは破線などの各種線、各種記号列や文字列が含まれる。
【００４８】
以上の説明では主として本発明者によってなされた発明をその背景となった利用分野であるパーソナルコンピュータシステムに適用した場合について説明したが、本発明はそれに限定されるものではなく、ワークステーション等にも適用することができる。
【００４９】

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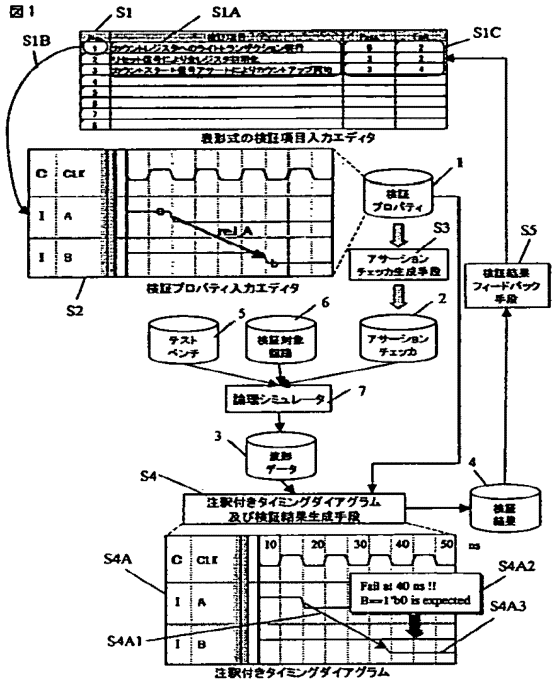
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【発明の効果】
本願において開示される発明のうち代表的なものによって得られる効果を簡単に説明すれば下記の通りである。
【００５０】
すなわち、コンピュータでの処理により、注釈付きタイミングダイヤグラムやテストレポートを速やかに作成することができ、また、人手作業にる煩雑な作業が省略されることで人為的なミスの低減を図ることができるため、論理検証効率の向上を図ることができる。
【図面の簡単な説明】
【図１】本発明にかかる論理検証プログラムによって実現される論理検証ツールの全体的な構成例ブロック図である。
【図２】上記論理検証ツールに含まれる検証項目入力エディタにおける入力例の説明図である。
【図３】上記論理検証ツールによる検証プロパティやアサーションチェッカの生成に関する説明図である。
【図４】上記論理検証ツールにおける論理シミュレーションの実行及びその結果の説明図である。
【図５】上記論理検証ツールに含まれる「注釈付きタイミングダイアグラム及び検証結果生成手段」の構成例説明図である。
【図６】上記論理検証ツールに含まれる状態遷移グラフ生成手段による状態遷移グラフ生成の説明図である。
【図７】上記論理検証ツールに含まれる状態遷移グラフトレース手段による注釈情報付き波形データ及び検証結果の生成説明図である。
【図８】注釈付き波形データに基づいて生成された注釈付きタイミングダイヤグラムの説明図である。
【図９】上記論理検証ツールにおける検証結果のフィードバック説明図である。
【図１０】本発明にかかる論理検証プログラムが実行されるパーソナルコンピュータシステムの構成例ブロック図である。
【符号の説明】
１００　パーソナルコンピュータシステム
１０１　外部インタフェース
１０２　マイクロコンピュータ
１０３　表示装置
１０４　記憶装置
２００　ネットワーク
３００　可搬型記憶媒体
Ｓ１　検証項目入力エディタ
Ｓ２　検証プロパティ入力エディタ
Ｓ３　アサーションチェッカ生成手段
Ｓ４　検証結果生成手段
Ｓ５　検証結果フィードバック手段

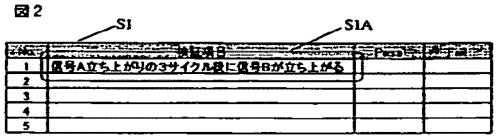
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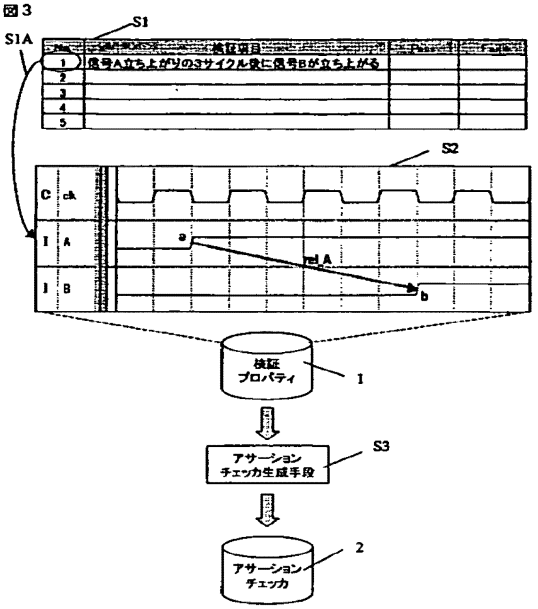
【図１】


図1
S1
S1A
S1B
S1C
表形式の検証項目入力エディタ
検証プロパティ入力エディタ
S2
検証プロパティ
S3
アサーションチェック生成手段
S5
検証結果フィードバック手段
テストベンチ
検証対象回路
アサーションチェック
論理シミュレータ
波形データ
S4
注釈付きタイミングダイアグラム及び検証結果生成手段
検証結果
S4A
S4A1
S4A2
S4A3
Fail at 40 ns !!
B==1'b0 is expected
注釈付きタイミングダイアグラム

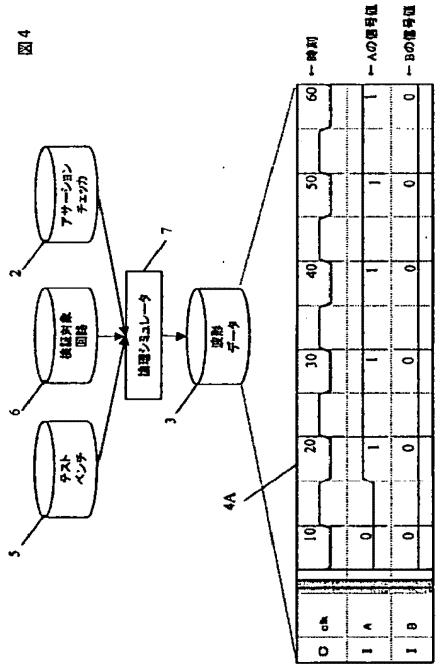
【図２】


図2
S1
S1A
検証項目
信号A立ちよがりの3サイクル後に信号Bが立ちよがる

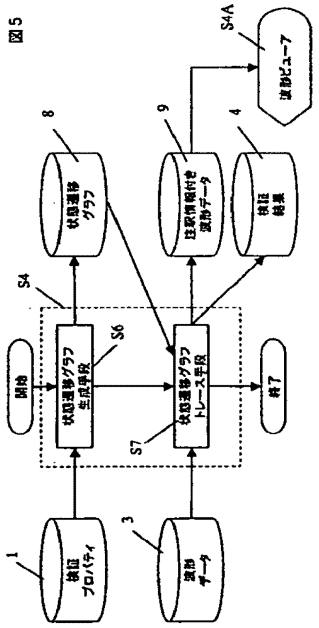
【図３】


図3
S1
S1A
検証項目
信号A立ちよがりの3サイクル後に信号Bが立ちよがる
S2
検証プロパティ
S3
アサーションチェック生成手段
アサーションチェック

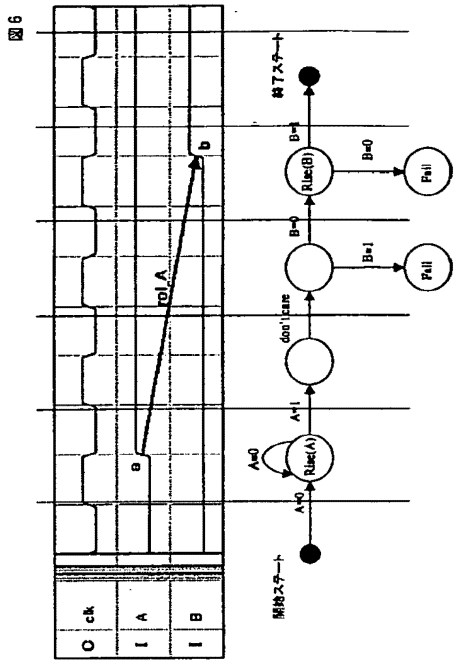
【図４】


図4
アサーションチェック
検証対象回路
テストベンチ
論理シミュレータ
波形データ
Aの信号値
Bの信号値

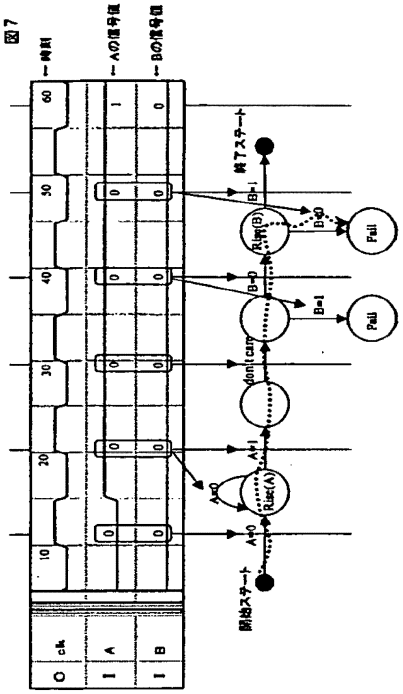
【図５】


図5
S4A
波形ビューア
状態遷移グラフ
注釈情報付き波形データ
検証結果
S4
状態遷移グラフ生成手段
S6
状態遷移グラフトレース手段
S7
開始
終了
検証プロパティ
波形データ

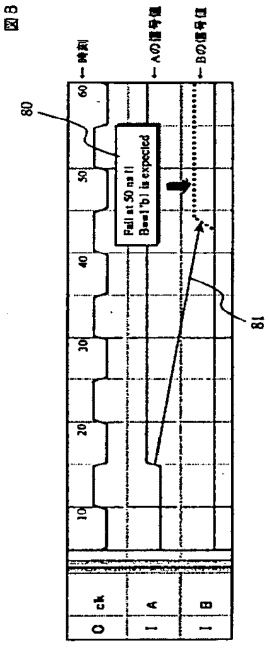
【図６】



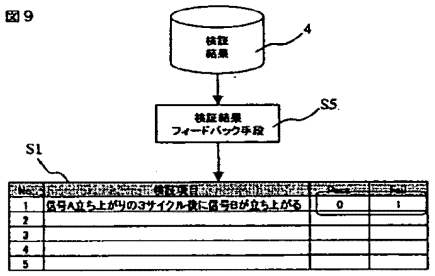
【図７】



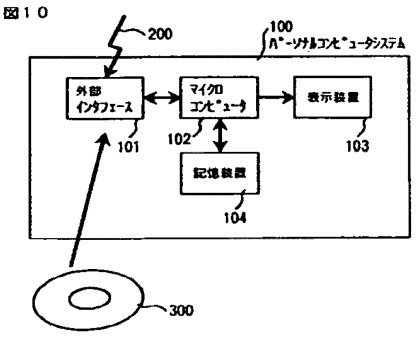
【図８】



【図９】



【図１０】



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PATENT ABSTRACTS OF JAPAN

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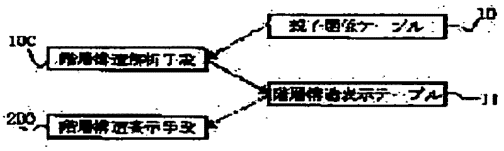
(51)Int.Cl. G06F 17/30
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H04L 12/44

(21)Application number : 10-361607
(22)Date of filing : 18.12.1998

(71)Applicant : NEC CORP
(72)Inventor : ARAI TSUNEHISA

(54) HIERARCHICAL STRUCTURE PREPARATION METHOD AND DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a hierarchical structure preparation method capable of efficiently preparing/displaying the entire hierarchical structure in an order from a highest level based on a master/slave relation table among respective stations in a communication system constituted of one master station B and N slave stations.
SOLUTION: This hierarchical structure preparation device for preparing and displaying the hierarchical structure of plural elements provided with master/slave relation is provided with a hierarchical structure analysis means 100 for referring to the master/slave relation table 10 for indicating the master/slave relation among the respective elements and preparing and outputting a hierarchical structure display table 11 provided with at least information for specifying whether or not the respective elements are master elements, the information for specifying whether or not they are the master element of the highest order, the information for specifying the slave elements of the respective master elements and the information for specifying the other slave elements in the same hierarchy of the respective slave elements and a hierarchical structure display means 200 for referring to the hierarchical structure display table 11 and preparing and displaying the entire hierarchical structure of the respective elements.



LEGAL STATUS

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[Patent number] 3277906

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(43)公開日　平成12年６月30日(2000.6.30)

(51)Int.Cl.'	識別記号	FI		テーマコード'(参考)
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17/50		15/60	604G	5B075
H04L 12/44			650A	5K033
		H04L 11/00	340	

審査請求　有　請求項の数５　ＯＬ　（全７頁）

(21)出願番号　特願平10－361607

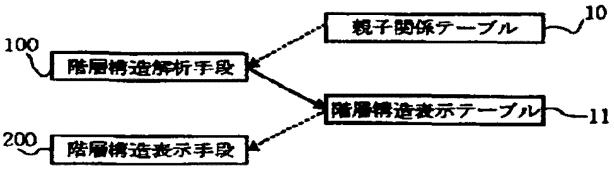
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Ｆターム(参考)　5B046 AA01 KA08
5B075 ND35 NK54 PQ02 PQ15
5K033 AA03 CB11 DA01 DA16 DA19
DB12 DB14 EA07 EC04

(54)【発明の名称】　階層構造作成方法及び装置

(57)【要約】
【課題】１つの親局Ｂ、Ｎ個の子局で構成される通信システムにおいて、各局間の親子関係テーブルをもとに全体の階層構造を最上位レベルから順に効率よく作成・表示できる階層構造作成方法を提供する。
【解決手段】親子関係を有する複数の要素の階層構造を作成及び表示する階層構造作成装置であって、各要素間の親子関係を表す親子関係テーブル１０を参照して、少なくとも各要素が親要素であるかどうかを特定する情報、最上位の親要素であるかどうかを特定する情報、各親要素の子要素を特定する情報、及び各子要素の同一階層における他の子要素を特定する情報を含んで構成される階層構造表示テーブル１１を作成して、出力する階層構造解析手段１００と、階層構造表示テーブル１１を参照して、各要素全体の階層構造を作成、表示する階層構造表示手段２００とを備えている。



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【特許請求の範囲】
【請求項１】　親子関係を有する複数の要素の階層構造を作成及び表示する階層構造作成方法であって、
各要素間の親子関係を表す親子関係テーブルを参照して、少なくとも各要素が親要素であるかどうかを特定する情報、最上位の親要素であるかどうかを特定する情報、各親要素の子要素を特定する情報、及び各子要素の同一階層における他の子要素を特定する情報を含んで構成される階層構造表示テーブルを作成して、出力する階層構造解析過程と、
階層構造表示テーブルを参照して、各要素全体の階層構造を作成、表示する階層構造表示過程とを有していることを特徴とする階層構造作成方法。
【請求項２】　階層構造表示テーブルが、１または複数の配列変数から構成されていることを特徴とする請求項１記載の階層構造作成方法。
【請求項３】　前記複数の配列変数は、前記各情報を配列変数の要素番号と、要素の値の大きさと、要素の値の符号とを所定の値とすることによって特定するものであることを特徴とする請求項１又は２に記載の階層構造作成方法。
【請求項４】　前記親子関係を有する複数の要素が、１又は複数の親局と、Ｎ個（Ｎは自然数）の子局で構成される通信システムにおける各局に対応するものであることを特徴とする請求項１～３のいずれか１項に記載の階層構造作成方法。
【請求項５】　親子関係を有する複数の要素の階層構造を作成及び表示する階層構造作成装置であって、
各要素間の親子関係を表す親子関係テーブルを参照して、少なくとも各要素が親要素であるかどうかを特定する情報、最上位の親要素であるかどうかを特定する情報、各親要素の子要素を特定する情報、及び各子要素の同一階層における他の子要素を特定する情報を含んで構成される階層構造表示テーブルを作成して、出力する階層構造解析手段と、
階層構造表示テーブルを参照して、各要素全体の階層構造を作成、表示する階層構造表示手段とを備えることを特徴とする階層構造作成装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、移動体通信システム等における複数の親局と子局の各局間の個々の親子関係を表すテーブルから、複数の親局および子局全体での階層構造を作成および表示するための階層構造作成方法及び装置に関する。
【０００２】
【従来の技術】従来の階層構造作成方法として、例えば移動体通信システム等における複数の親局と子局の各局間の１対１の親子関係を示す複数のデータを有する親子関係テーブルをもとに、親局から順に子局の親子関係をサーチして階層構造を作成するようにしたものがある。この方法によると子局をサーチするたびに親子関係テーブルを始めからサーチすることになり、特に局数Ｎが多いと親子関係テーブルをサーチする回数（平均Ｎ＊Ｎ／２）が増え、階層構造を表示するスピードが悪化する。
【０００３】また、ある子局に対して、最上位局がその子局の親局以外にあるかどうかを判定するには、親子関係テーブルで親局側になっている局を１局ずつその局がさらに他の局の子局になっていないかどうかを調べる必要がある。
【０００４】また、例えば、１つの親局Ｂと、Ｎ個の子局（中継局Ｒまたは端局Ｔ）で構成される通信システムにおいて、各局間の親子関係を示す親子関係テーブルをもとに全体の階層構造を作成・表示しようとした場合、このシステムでは実際には親局Ｂ以外は最上位局にならないが、親子関係テーブルのデータが足りないときには、例えば親局Ｂではなく、中継局Ｒが表示上では最上位局になることがある。すなわち、本来１つであるべき最上位局が複数表示されることになる。
【０００５】また、通信システムの監視装置に通信システムの階層構造表示をさせる場合、通常、最上位局から順番に局を表示していかないとエラーになり表示を行うことができないので、表示の際にも最上位局を特定するための処理が必要となる。
【０００６】
【発明が解決しようとする課題】上記の事情に鑑み、本発明は、例えば、１つの親局Ｂ、Ｎ個の子局（中継局Ｒ，端局Ｔ）で構成される通信システムにおいて、各局間の親子関係テーブルをもとに全体の階層構造を最上位レベルから順に効率よく作成・表示できる階層構造作成方法及び装置を提供することを目的とする。すなわち、本発明は、例えば１つの親局Ｂ、Ｎ個の子局（中継局Ｒ，端局Ｔ）で構成される通信システムにおいて、階層構造を作成・表示する際に、親子関係テーブルを１局ごとに毎回サーチすることなくすべての親子関係を１回のサーチで参照でき、かつ親局以外の最上位局を１回のサーチで把握し、全体の階層構造を最上位レベルから順に効率よく作成・表示することができる階層構造作成方法及び装置を提供することを目的とする。
【０００７】
【課題を解決するための手段】上記課題を解決するため、請求項１記載の階層構造作成方法は、親子関係を有する複数の要素の階層構造を作成及び表示する階層構造作成方法であって、各要素間の親子関係を表す親子関係テーブルを参照して、少なくとも各要素が親要素であるかどうかを特定する情報、最上位の親要素であるかどうかを特定する情報、各親要素の子要素を特定する情報、及び各子要素の同一階層における他の子要素を特定する情報を含んで構成される階層構造表示テーブルを作成して、出力する階層構造解析過程と、階層構造表示テーブ

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ルを参照して、各要素全体の階層構造を作成、表示する階層構造表示過程とを有していることを特徴としている。

【０００８】また、請求項２記載の発明は、階層構造表示テーブルが、１または複数の配列変数から構成されていることを特徴としている。また、請求項３記載の発明は、前記複数の配列変数が、前記各情報を配列変数の要素番号と、要素の値の大きさと、要素の値の符号とを所定の値とすることによって特定するものであることを特徴としている。また、請求項４記載の発明は、前記親子関係を有する複数の要素が、１又は複数の親局と、Ｎ個（Ｎは自然数）の子局で構成される通信システムにおける各局に対応するものであることを特徴としている。

【０００９】また、請求項５記載の発明は、親子関係を有する複数の要素の階層構造を作成及び表示する階層構造作成装置であって、各要素間の親子関係を表す親子関係テーブルを参照して、少なくとも各要素が親要素であるかどうかを特定する情報、最上位の親要素であるかどうかを特定する情報、各親要素の子要素を特定する情報、及び各子要素の同一階層における他の子要素を特定する情報を含んで構成される階層構造表示テーブルを作成して、出力する階層構造解析手段と、階層構造表示テーブルを参照して、各要素全体の階層構造を作成、表示する階層構造表示手段とを備えることを特徴としている。

【００１０】

【発明の実施の形態】以下、図面を参照して本発明の実施の形態について説明する。なお、以下の例は、本発明を移動体通信システムに適用した場合のものであるが、本発明の適用範囲は移動体通信システムに限られるものではなく、親子関係を有している複数の要素から階層構造を作成する場合であれば、一般に、他のすべてのシステムに対して適宜応用することが可能である。

【００１１】図１は本発明による階層構造作成装置の一実施形態を示すブロック図である。図１に示す実施形態では、階層構造解析手段１００が、各局間の個々の親子関係を示すデータを複数有する親子関係テーブル１０を参照して、階層構造を表示する際に中間的なデータとして使用される階層構造表示テーブル１１を作成・出力し、階層構造表示手段２００が、階層構造表示テーブル１１をもとに、最終的に階層構造を作成・表示する。ここで、各手段は、例えば、１つまたは複数の親局Ｂと、Ｎ個の子局（中継局Ｒ，端局Ｔ）で構成される通信システムにおける各局またはその通信システムの監視装置内のＣＰＵ（中央処理装置）と記憶装置等の周辺装置と、それらを用いて実行されるソフトウェアによって実現される。また、各テーブルは、記憶装置に格納される複数のデータから形成される。なお、階層構造解析手段１００と階層構造表示手段２００は、必ずしも同一装置内に設けられている必要はなく、例えば通信回線を介して接続されていてもよい。

【００１２】図２は階層構造解析手段１００の動作フローチャート、図３は階層構造表示手段２００の動作のフローチャートを示している。また図４は、親子関係テーブル１０の例を示している。

【００１３】図４に示す親子関係テーブル１０は、テーブルの右に示す階層構造を持つ複数の局１～７の各局間の個々の親子関係を示す複数のデータを有して構成されている。この場合、親子関係テーブル１０は、テーブルの各行が各局間における各親子関係に対応している。各行（あるいは各項目）をなす複数のデータは、行番号を示す“Ｎｏ”（後述する図５の変数ｊに対応）、各親子関係における親局を示す“上位局ＮＯ”と、子局を示す“局ＮＯ”からの３つである。例えば、行Ｎｏ．＝１は、局１が親局で、局４が子局となる親子関係４１を示し、行Ｎｏ．＝３は、局４が親局で、局２が子局となる親子関係４２を示している。

【００１４】図５は、階層構造解析手段１００が図２に示す動作フローチャートに従って、図４の親子関係テーブル１０から図１に示す階層構造表示テーブル１１を出力する過程における各変数の変化を示す階層構造解析動作図である。図５において、変数ｊは図２のステップ１０３とステップ１１２の間で１ずつ増加する変数ｊに対応し、１から、図４の親子関係テーブル１０の項目数Ｍ＝５までの値をとる。配列変数Ｒ(i)およびＬ(i)（ｉ＝１～Ｎ：ただしＮは局数）は、初期値をそれぞれ８および０として、図２のステップ１０３とステップ１１２間における各処理で変数ｊの変化に応じて変化し、最終的に階層構造表示テーブル１１を形成する各データとなる。図５では、各変数Ｒ(i)および変数Ｌ(i)の内容が変化したところで変化後の数値を表示している。すなわち、例えば、Ｒ(1)はｊ＝１の処理で－１に変化し、またＲ(4)はｊ＝１の処理で一度０に変化し、再びｊ＝３の処理で３に変化している。

【００１５】図５に示す階層構造表示テーブル１１を形成する一方の配列Ｒ(i)は、その値の大きさと正または負の符号とを予め定めた値とすることによって、局ｉが親局すなわちいずれかの局を子局とする局であるかどうか（図５に示す場合ではＲ(i)が０または初期値８以外の値のとき親局を意味する。）、局ｉが親局である場合に局ｉが最も上位の親局すなわち最上位局であるかどうか（図５に示す場合には０または初期値８以外の値でありかつ負の値のとき）、および局ｉが親局である場合にその値Ｒ(i)の絶対値｜Ｒ(i)｜によって、その子局のうちで親子関係テーブル１０内で最小の項目番号に設定されている局の局ＮＯに対応する値が配列Ｌ(i)内の配列Ｌ(｜Ｒ(i)｜)に格納されていることを示している。

【００１６】なお、図５に示す場合、局ｉが下位に子局を持たない子局であるときにはＲ(i)に０が設定されている。また図５には該当局はないが、本実施形態では、

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局ｉが親子関係テーブル１０に含まれていないときには、Ｒ(i)に初期値８が格納されることになる。

【００１７】図５に示す例では、階層構造表示テーブル１１は、Ｒ(1)、Ｒ(4)、Ｒ(5)にそれぞれ－１，３，－４が格納されているので、図４に示すように局１，４，５が親局であり、かつ局１，５が最上位局であることを示すとともに、さらに、局１の最初の子局の局番号４が変数Ｌ(1)に、局４の最初の子局の局番号２（ただし符号は負）が変数Ｌ(3)に、そして、局５の最初の子局の局番号３（ただし符号は負）が変数Ｌ(4)に格納されていることを示している。また、他の配列変数Ｒ(2)，Ｒ(3)，Ｒ(6)，Ｒ(7)には０が格納されているので、局２，３，６，７が階層構造に存在している子局であることを示している。

【００１８】他方、階層構造表示テーブル１１を形成するもう一方の配列Ｌ(i)は、親子関係テーブル１０に含まれているすべての子局の局ＮＯに対応するデータを、親子関係テーブル１０の項目番号と同一の要素番号を有する要素として、当該項目に設定されている局ＮＯと同一の絶対値を有し、正または負の符号を有する整数として有し、その符号の正負によって、当該子局がその子局の親局と同一の局を親局とする他の子局が存在するかどうか、すなわち同一階層に他の子局が存在するかどうかを示している。すなわち、図５に示す例では、配列Ｌ(i)の各要素として、親子関係テーブル１０の項目番号ｉに設定されている子局の局ＮＯに等しい絶対値を持ち、親子関係テーブル１０の項目番号（ｉ－１）に同一階層の子局が存在する場合には符号を正とする整数が（Ｌ(2)，Ｌ(5)）、存在しない場合は符号を負とする整数が（Ｌ(1)，Ｌ(3)，Ｌ(4)）、それぞれ格納されている。ただし、親子関係テーブル１０に対応する項目番号ｉが存在しない場合（図５ではＬ(6)，Ｌ(7)）には、初期値が格納されている。

【００１９】なお、階層構造表示テーブル１１を形成する各配列に設定される値は上記の設定に限定されるものではなく、例えば、初期値の値を変更したり、正負の符号を逆にする等、適宜変更が可能である。

【００２０】次に、図１に示す実施形態の各構成の動作について、階層構造解析手段１００、解析構造表示手段２００の順に説明する。

【００２１】（１）階層構造解析手段１００の動作

図２のフローチャートのもとづき、図４および図５を用いて動作を説明する。なお、処理の前に図４の親子関係テーブル１０はあらかじめ上位局ＮＯで番号の若い順でソートされているものとする。また、局ＮＯに重複はないものとする。

【００２２】まず始めに、階層構造表示テーブル１０用の変数Ｒ(i)とL(i)を初期化する（ｉ＝１からＮおよびｉ＝０からＮ）（ステップ１０１）。ここではＲ(i)にＮ＋１が代入され（Ｎは局数）、Ｌ(i)に０が代入される。

【００２３】次に、作業用変数ｉｕ（上位局ＮＯの保存用）を初期化（＝Ｎ＋１）する（ステップ１０２）。次に、ステップ１０３からステップ１１２までの各手順をｊ＝１からＭまで繰り返す（Ｍは親子関係テーブルの項目数）。

【００２４】まず、ステップ１０４で、親子関係テーブル１０のｊ番めのデータを参照し、局ＮＯを変数ｋに、そして上位局ＮＯを変数ｉに、それぞれ代入する。次に、ステップ１０５で、変数ｋとｉを比較し、等しければステップ１１１へ処理を飛ばし、等しくなければステップ１０６へ処理を進める。ステップ１０６では、変数ｉと変数ｉｕを比較し、等しくなければステップ１０７ａへ処理を進め、等しければステップ１０９へ処理を進める。

【００２５】ステップ１０７ａではＲ(i)の値をチェックし、Ｒ(i)＝０であればＲ(i)に＋ｊを代入し（ステップ１０７ｂ）、Ｒ(i)＝Ｎ＋１であればＲ(i)に－ｊを代入する（ステップ１０７ｃ）。次に、ステップ１０８でＬ(j)に－ｋを代入し、ステップ１１０ａへ処理を進める。一方、ステップ１０９では、Ｌ(j)に＋ｋを代入し、ステップ１１０ａへ処理を進める。

【００２６】ステップ１１０ａでは、変数Ｒ(k)の値をチェックし、Ｒ(k)＝Ｎ＋１であればＲ(k)に０を代入し（ステップ１１０ｂ）、Ｒ(k)＜０であればＲ(k)にＲ(k)の絶対値を代入する（ステップ１１０ｃ）。そして、ステップ１１１で、変数ｉｕに変数ｉの値を代入する（ｉｕに上位局ＮＯをセーブする）。

【００２７】これらの処理により、階層構造解析手段２００は、図４の親子関係テーブルを入力しながら変数ｊを１からＭ（＝５）まで変化させ、ステップ１０４からステップ１１１までの処理を通るごとに、図５に示すように変数R(i)、L(i)に各値を設定し、最終的に図５の階層構造表示テーブル１１を作成して出力する。

【００２８】なお、図２において、ステップ１０７ａ～１０７ｃからなる処理１０７では、その時点の上位局（上位局ＮＯ＝ｉ）が、以前の処理（ステップ１１０ｂ）で既に下位局として処理されていた場合には、変数Ｒ(i)に、子局の局ＮＯ（－ｋ）を格納する変数Ｌ（ｊ）の配列要素番号ｊの正の値を設定し（ステップ１０７ｂ）、以前にまだ処理されていなかった場合には（値が初期値のままであった場合には）、最上位の親局として、変数Ｒ(i)に、変数Ｌ（ｊ）の配列要素番号ｊの負の値を設定している（ステップ１０７ｃ）。また、ステップ１１０ａ～１１０ｃからなる処理１１０では、その時点の局ＮＯ＝ｋの局が、以前にまだ処理されていなかった場合には、変数Ｒ(k)に親局ではない子局であることを示す０を設定し（ステップ１１０ｂ）、以前に最上位の親局として値が設定されていた場合（ステップ１０７ｃ）には、変数Ｒ(k)の値を最上位ではない親局

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を示す正の値に変更している（ステップ１１０ｃ）。

【００２９】（２）階層構造表示手段２００の動作

次に、図３のフローチャートにもとづき、図６を用いて階層構造表示手段２００の動作について説明する。図６は階層構造表示手段２００が階層構造表示テーブル１１から階層構造を表示する処理の過程を示す階層構造表示動作図である。

【００３０】図３に示すように、図１に示す階層構造表示手段２００は、主ルーチン（ステップ２０１～２０４）において、階層構造表示テーブル１１を参照しながら、変数ｑをｑ＝１からＮまでＲ(ｑ)をチェック（ステップ２０２）しながら変化させ、ステップ２０１～２０４の処理を繰り返し実行し、Ｒ(ｑ)が負であればステップ２０３で関数Ｔｒｅｅ（ｑ，ｑ）を呼び出す処理を行う。

【００３１】関数Ｔｒｅｅ（ｐ，ｑ）では、変数ｐと変数ｑが比較され（ステップ３０１ａ）、ｐ＝ｑであれば変数ｑが最上位局として表示され（ステップ３０１ｂ）、変数ｐと変数ｑが等しくなければ、変数ｑが変数ｐの配下の局として表示される（ステップ３０１ｃ）。このステップ３０１ａ～３０１ｃの処理によって階層構造を表示する部分の処理３０１が構成されている。

【００３２】次に、ステップ３０２で、変数ｊに変数ｑが代入されるとともに、変数ｉに階層構造表示テーブル１１における配列変数Ｒ(ｊ)の絶対値が代入される。ステップ３０３では、変数ｋに階層構造表示テーブル１１における配列変数Ｌ(ｉ)の絶対値が代入され、次いで、変数ｋの値がチェックされ（ステップ３０４ａ）、ｋ＝０であればステップ３０５へ処理が進められ、ｋ≠０であれば変数ｊ，ｋを引数として関数Ｔｒｅｅ（ｊ，ｋ）が再帰的に呼び出されて実行される（ステップ３０４ｂ）。ここで、ステップ３０４ａ～３０４ｃからなる処理３０４では、ｋすなわち変数Ｌ(ｉ)が０でない場合、つまり、同一階層にさらに呼び出すべき下位局が存在する場合に、関数Ｔｒｅｅを呼び出す処理が行われている。

【００３３】そして、ステップ３０５では、変数ｉが１だけ増分され、ステップ３０６で変数ｋ＞０かつ変数Ｌ(ｉ)＞０の条件が成立すればステップ３０３へ戻り、同一の変数ｊすなわち同一の親局に対する他の子局に対して処理３０４による関数Ｔｒｅｅの呼出処理が行われる。

【００３４】これらの処理により、階層構造表示手段２００は、図５に示す階層構造表示テーブル１１から図６の階層構造表示動作図に示す様に、階層構造表示テーブル１１を始めからサーチすることなく１本の経路をたどって図４の階層構造を効率よく作成・表示する。

【００３５】ここで、図６の階層構造表示動作図について詳細に説明する。図６は、階層構造表示手段２００が、図５に示す階層構造表示テーブル１１を参照しながら、図４の階層構造を表示する際の処理過程を示すものである。図３のフローチャートでは、まず、変数ｑが１のときに、関数Ｔｒｅｅ（１，１）が呼び出され、局ＮＯ＝１が最上位局として表示される（図６の符号６０１）。次に、関数Ｒ(1)が参照されて、関数Ｒ(1)の値に基づいてＬ(1)＝－４の絶対値を引数ｋとして（６０２）、関数Ｔｒｅｅ（１，４）が実行され（６０３）、局ＮＯ＝４が局ＮＯ＝１の下位局として表示される。次に、関数Ｒ(4)が参照されて、Ｌ(3)＝－２の絶対値を引数ｋとして（６０４）、関数Ｔｒｅｅ（４，２）が実行され（６０５）、局ＮＯ＝２が局ＮＯ＝４の下位局として表示される。

【００３６】関数Ｔｒｅｅ（４，２）では、変数Ｒ(2)＝０＝ｉとなることから、変数Ｌ(0)＝０＝ｋとなり、関数Ｔｒｅｅ（４，２）が終了し（６０６）、次に、引数ｋをＬ(1)の絶対値（＝４）からＬ(1+1)＝Ｌ(2)の絶対値（＝７）に代えて（６０７）、関数Ｔｒｅｅ（１，７）が呼び出される（６０８）。そして、局ＮＯ＝７が局ＮＯ＝１の下位局として表示される。ここで、Ｒ(7)＝０なので、ｋ＝０となり、関数Ｔｒｅｅ（１，７）が終了し（６０９）、さらに、Ｌ(2+1)＝Ｌ(3)＝－２なので（６１０）、関数Ｔｒｅｅ（１，１）内の処理が終了する（６１１）。

【００３７】次に、主ルーチンのステップ２０３から関数Ｔｒｅｅ（５，５）が実行され、局ＮＯ＝５が最上位局として表示される（６１２）。次に、関数Ｒ(5)が参照されて、Ｌ(4)＝－３の絶対値を引数ｋとして（６１３）、関数Ｔｒｅｅ（５，３）が実行され（６１４）、局ＮＯ＝３が局ＮＯ＝５の下位局として表示される。関数Ｔｒｅｅ（５，３）では、変数Ｒ(3)＝０となることから、変数Ｌ(0)＝ｋ＝０となり、関数Ｔｒｅｅ（５，３）が終了し（６１５）、次に、引数ｋをＬ(4)の絶対値（＝３）からＬ(4+1)＝Ｌ(5)の絶対値（＝６）に代えて（６１６）、関数Ｔｒｅｅ（５，６）が呼び出される（６１７）。そして、局ＮＯ＝６が局ＮＯ＝５の下位局として表示される。ここで、Ｒ(6)＝０なので、ｋ＝０となり、関数Ｔｒｅｅ（５，６）が終了し（６１８）、さらに、Ｌ(5+1)＝Ｌ(6)＝０なので（６１９）、関数Ｔｒｅｅ（５，５）内の処理が終了する（６２０）。

【００３８】以上のようにして、図４に示すような階層構造が表示される。

【００３９】なお、本発明は、上記の実施形態に限定されるものではなく、例えば親子関係情報が局ＮＯ．１～ＮＯ．Ｎの局ですべてそろっていなくても実現することができる。

【００４０】また、上記実施形態では、階層構造表示テーブル１１を異なる２つの変数名を持つ配列変数Ｒと配列変数Ｌとから構成するようにしているが、階層構造表示テーブル１１の構成方法はこれに限定されるものでは

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ない。例えば、配列変数Ｒと配列変数Ｌを、それぞれ２つの配列変数Ｒ１，Ｒ２および配列変数Ｌ１，Ｌ２に分割し、変数Ｒ１と変数Ｌ１とが変数Ｒと変数Ｌの値の絶対値の情報を持ち、変数Ｒ２と変数Ｌ２とが変数Ｒと変数Ｌの正負の符号の情報を持つようにすれば、４つの変数名を持つ配列変数から上記と同等の階層構造表示テーブルを構成することができる。あるいは、階層構造表示テーブル１１を１つの配列変数から構成し、その要素番号の奇数を配列変数Ｒに、偶数を配列変数Ｌに割り当てるようにしたり、もしくは所定のオフセット値を設定して、オフセット値を付加するかしないかによって配列変数Ｒと配列変数Ｌと同等の構成を得るようにすることによっても、上記と同等の階層構造表示テーブルを構成することができる。

【００４１】

【発明の効果】以上説明したように、本発明によれば、各要素間の親子関係を表す親子関係テーブルから一旦、少なくとも各要素が親要素であるかどうかを特定する情報、最上位の親要素であるかどうかを特定する情報、各親要素の子要素を特定する情報、及び各子要素の同一階層における他の子要素を特定する情報を含んで構成される階層構造表示テーブルを作成し、これを参照して各要素全体の階層構造を作成、表示するようにしたので、階層構造を最上位レベルから効率よく作成・表示できる。

【図面の簡単な説明】

【図１】　本発明による階層構造作成装置の一実施形態を示すブロック図である。

【図２】　図１に示す階層構造解析手段１００の動作フローチャートである。

【図３】　図１に示す階層構造表示手段２００の動作のフローチャートである。

【図４】　図１に示す親子関係テーブル１０の一例およびその例による階層構造を示す図である。

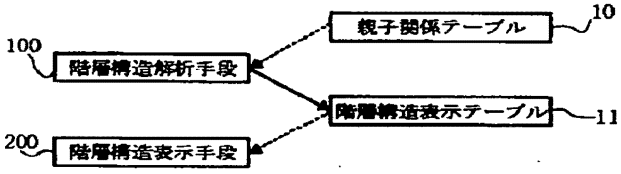
【図５】　図１に示す階層構造解析手段１００が図２に示す動作フローチャートに従って、図４の親子関係テーブル１０から階層構造表示テーブル１１を出力する過程における各変数の状態変化を示す階層構造解析動作図である。

【図６】　図１に示す階層構造表示手段２００が階層構造表示テーブル１１から階層構造を表示する過程の流れを示す階層構造表示動作図である。

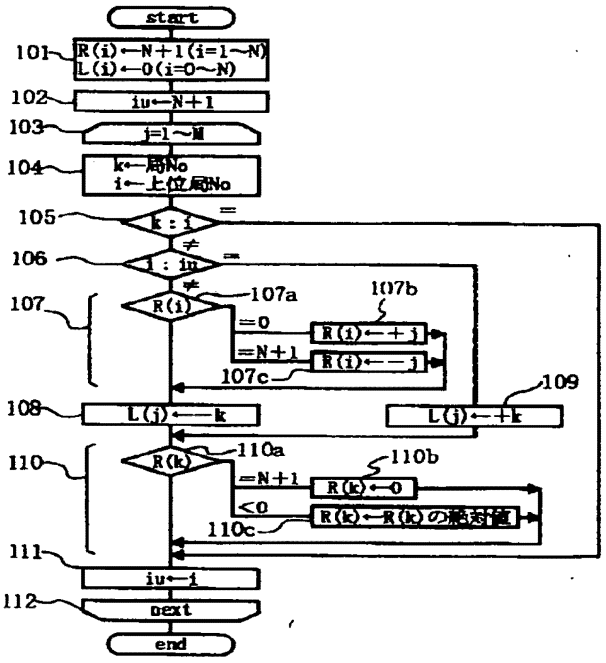
【符号の説明】

１０　親子関係テーブル
１１　階層構造表示テーブル
１００　階層構造解析手段
２００　階層構造表示手段

【図１】



【図２】

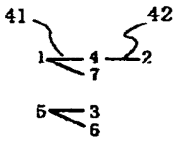


【図４】

10：親子関係テーブル

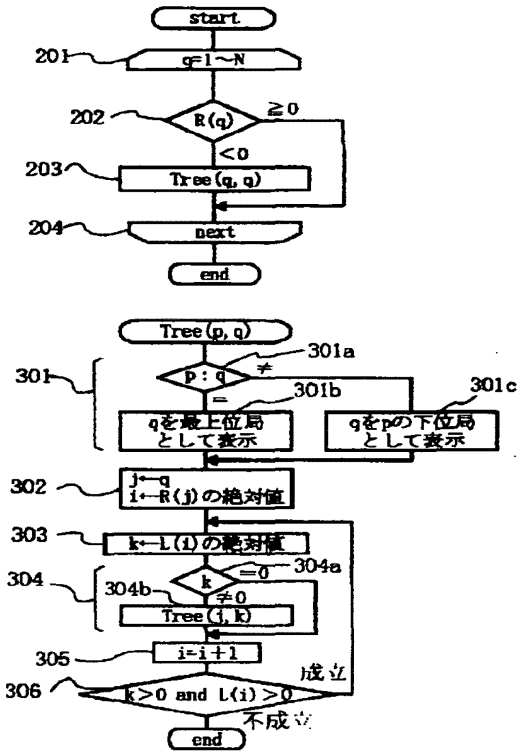
No(j)	上位局No	局No
1	1	4
2	1	7
3	4	2
4	5	3
5	5	6

階層構造



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【図３】



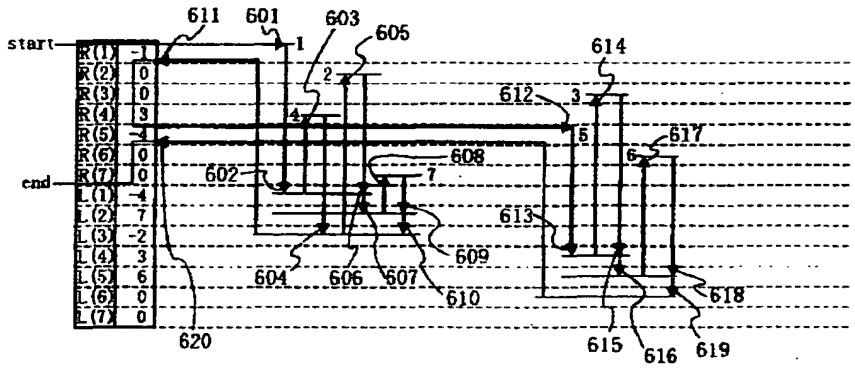
【図５】

11：階層構造表示テーブル

N＝7(局数)
M＝5(親子関係テーブルの項目数)

	初期	1	2	3	4	5	
R(1)	8	-1					-1
R(2)	8			0			0
R(3)	8				0		0
R(4)	8	0		3			3
R(5)	8				-4		-4
R(6)	8					0	0
R(7)	8		0				0
L(1)	0	-4					-4
L(2)	0		7				7
L(3)	0			-2			-2
L(4)	0				-3		-3
L(5)	0					6	6
L(6)	0						0
L(7)	0						0

【図６】



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PATENT ABSTRACTS OF JAPAN

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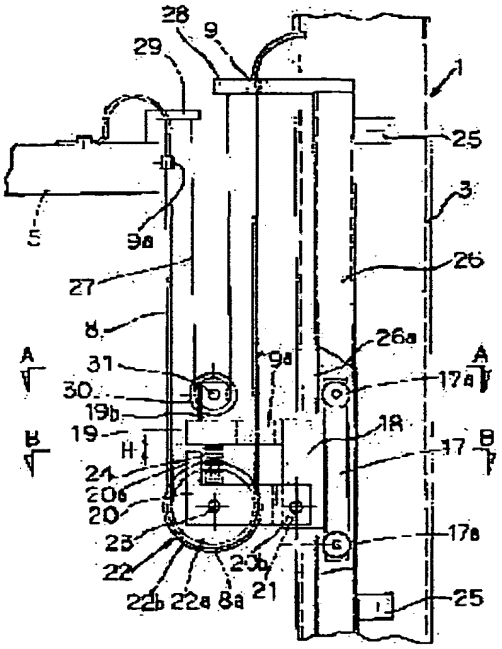
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AMADA HIROYUKI
KOSUGE YUICHI

(54) POWER SUPPLY SYSTEM FOR CRANE IN AUTOMATED WAREHOUSE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent a power supply cable from deflecting without applying an excessive load to the cable, and to prevent the cable from being disconnected.
SOLUTION: In a power supply system for a crane in an automated warehouse, including a pair of masts 3, a cargo bed 5 moved up and down along the masts 3, a power supply cable 8 fixed at its one to the heightwise middle part of the mast 3 and at its the other end to the cargo bed 5, and having is intermediate part drooped down so as to form a U-like curved part 8a, a guide rail 26 laid in parallel with the masts 3, an elevating frame 17 arranged to the guide rail 26 so as to be elevatable, and a constraining wheel 22 attached to the elevating frame 17 and wound thereon the curved part 8a of the cable 8, the constraining wheel 22 is attached to a swingable frame 20 pivotally supported to the elevating frame 20, and the elevating frame 17 is suspended by means of a wire rope 27 fixed at its one end to a hightwise substantially middle position of the mast 3, and at its the other end to the cargo bed 5, through the intermediary of a rope sheave 30.



LEGAL STATUS

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[Patent number]

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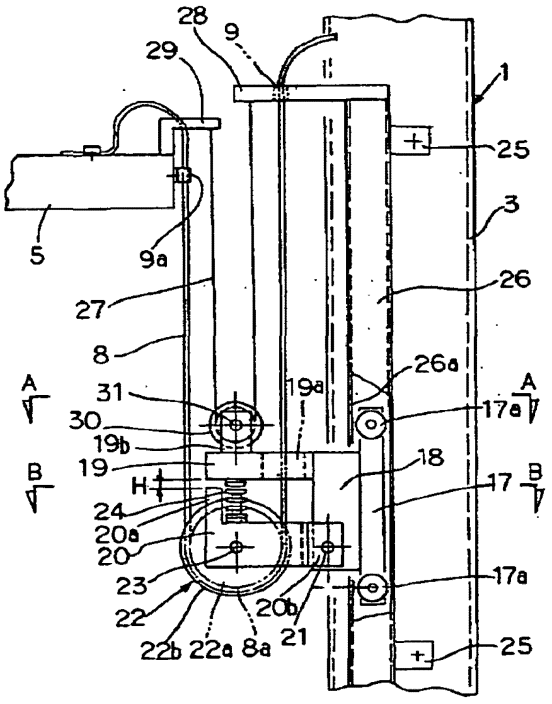
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弁理士　島村　芳明

最終頁に続く

(54)【発明の名称】　自動倉庫用クレーンの給電装置

(57)【要約】
【課題】　給電ケーブルに過大な荷重を掛けないで給電ケーブルの振れを防止するとともに、給電ケーブルの線の切断を防止するようにする。
【解決手段】　一対のマスト３と、該マスト３に沿って昇降する荷台５と、一端をマスト３の高さ方向の中間部に固定するとともに、他端を荷台５に固定して中間が垂下してＵ字状の屈曲部８ａを形成した給電ケーブル８と、マスト３に平行に設けたガイドレール２６と、該ガイドレール２６に昇降可能に配設した昇降フレーム１７と、該昇降フレーム１７に取り付けられ、上記給電ケーブル８の屈曲部８ａが巻き掛けられた拘束輪２２とを有してなる自動倉庫用クレーンの給電装置であって、上記拘束輪２２は上記昇降フレーム１７に枢支された揺動フレーム２０に取り付けられており、昇降フレーム１７は一端をマスト３の高さ方向のほぼ中間部に固定し、他端を荷台５に固定したワイヤロープ２７によりロープシーブ３０を介して吊り下げるようにしてなる。



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【特許請求の範囲】
【請求項１】　一対のマストと、該マストに沿って昇降する荷台と、一端をマストの高さ方向の中間部に固定するとともに、他端を荷台に固定して中間が垂下してＵ字状の屈曲部を形成した給電ケーブルと、マストに平行に設けたガイドレールと、該ガイドレールに昇降可能に配設した昇降フレームと、該昇降フレームに取り付けられ、上記給電ケーブルの屈曲部が巻き掛けられた拘束輪とを有してなる自動倉庫用クレーンの給電装置であって、上記拘束輪は上記昇降フレームに枢支された揺動フレームに取り付けられており、昇降フレームは一端をマストの高さ方向のほぼ中間部に固定し、他端を荷台に固定したワイヤロープによりロープシーブを介して吊り下げるようにしてなることを特徴とする自動倉庫用クレーンの給電装置。
【請求項２】　前記揺動フレームの先端側上面とロープシーブ支持材下面との間に、給電ケーブルに張力を付与する弾性体を配設した請求項１記載の自動倉庫用クレーンの給電装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、自動倉庫用クレーンの給電装置に係り、特に自動倉庫用クレーンの荷台へ給電するための給電装置に関するものである。
【０００２】
【従来の技術】自動倉庫は、倉庫内に設けられた多数の棚を有する棚列の前面に沿って走行する自動倉庫用クレーンによって入出庫台と棚との間で荷物の受け渡しをして荷物の入出庫を行うようにしたものである。
【０００３】図４は従来の倉庫用クレーンおよび棚列の概要を示す正面図である。図５は図４のＣ－Ｃ矢視図であり、図６は図４のＤ－Ｄ矢視図である。図４ないし図６において、１は自動倉庫用クレーン（以下「クレーン」という。）である。クレーン１は、走行車輪２ａを有する下部フレーム２と、下部フレーム２上に立設した一対のマスト３と、このマスト３の上端に設けたガイドローラ４ａを有する上部フレーム４と、一対のマスト３に沿って昇降する荷台５とから構成されている。
【０００４】クレーン１は、走行路１１に沿って左右に設けられた棚列１４の間に位置し、棚列１４の前面に沿って床面１０上に敷設した走行レール１２上を、上部フレーム４に設けられたガイドローラ４ａを介して上部ガイドレール１３に案内されて移動する。また、クレーン１は、機上制御盤７に内蔵されたコンピュータに指示を与えることによって、入出庫台１６と棚列１４の棚１４ａとの間を移動して所定位置で停止するとともに、荷台５を所定の棚１４ａまで昇降し、荷台５上に設けた移載装置６により荷物１５の受け渡しを行うようになっている。荷台５は上部フレーム４に設けられた図示しない巻上装置に巻き掛けられたワイヤロープによって吊り下げられてマスト３に案内されて昇降する。
【０００５】荷台５には、棚列１４の棚１４ａまたは入出庫台１６との間で荷物１５の受け渡しをする移載装置（フォーク装置）６が設けられている。また、荷台５には移載装置６の他に図示しない各種の位置検出センサ等の制御用機器が設けられている。８はこれら移載装置６や制御用機器に給電するための給電ケーブルである。７は下部フレーム２上に設けられた機上制御盤である。
【０００６】給電ケーブル８は、荷台５が下限位置から上限位置まで昇降できるだけの長さを有しており、その中間は荷台５の側面とマスト３の高さ方向のほぼ中間に留金具９，９ｂによってそれぞれ固定されている。また、給電ケーブル８は、マスト３の留金具９と荷台５の留金具９ａとの間で中間が垂下してＵ字状の屈曲部８ａを形成し、マスト３に沿ってＵ字状に吊り下げられて屈曲部８ａは常に最下端に位置するようになっていて屈曲部８ａは自由状態になっている。
【０００７】なお、給電ケーブル８には、帯状のケーブルによって形成されたものや複数のケーブルによって形成されたものがある。
【０００８】近年、倉庫スペースの有効利用を図り、作業の効率化を図るため、棚列の高さを従来のものより高くするとともに、クレーンの移動や荷台の昇降の際の速度を従来のものより速くするようにしている。
【０００９】このため、給電ケーブル８のＵ字状の屈曲部８ａは自由状態になっているので、クレーン１の移動方向に対して左右方向に大きく振れて、棚１４ａの支柱や格納してある荷物１５に引っ掛けて損傷したり、極端な場合には切断してしまう恐れがある。また、給電ケーブルは移送用ドラムに巻いて現地に搬送されることが多いが、そのため、現地でクレーンに取り付けたときドラムの巻き癖が残り、真っ直ぐに垂れ下がらず、給電ケーブルはあらかじめドラムから巻き戻し、引き延ばして巻き癖取りをした後に取り付けなければならない。
【００１０】このような事態を防止するため、給電ケーブル８が振れて棚１４ａの支柱や格納してある荷物１５に接触したり、引っ掛けないようにするための技術が提案されている（特開平９－１５６８７３）。
【００１１】図７および図８は、特開平９－１５６８７３に示された倉庫設備用クレーンにおける給電ケーブルの張力付与装置の図で、図７はその一部拡大側面図であり、図８は図７のＥ－Ｅ矢視図である。なお、図４ないし図６で説明したものと共通の部分は、同じ符号を付して説明する。図７および図８において、クレーン１のマスト３には、マスト３と平行に水平断面がＣ溝形状のガイドレール２６が複数のブラケット２５を介して固定されている。ガイドレール２６は、その開口部２６ａを給電ケーブル８側に向け、かつ、給電ケーブル８と所定の間隔を保つように設けられている。５はマスト３に案内されて昇降する荷台である。給電ケーブル８は、留金具

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９ａにより荷台５のマスト３対向面とマスト３の高さ方向のほぼ中間に固定され、マスト３の留金具９との間では中間が垂下してＵ字状の屈曲部８ａを形成している。なお、これらの点は、図４に示すクレーンと実質的に同じである。

【００１２】１７は昇降フレームで、その高さ方向の中間部に給電ケーブル８側に突出するように固定された水平部材１７ｂによりＴ字状に形成されており、その上下端部に配設したガイドローラ１７ａによりガイドレール２６に嵌入され、ガイドレール２６に案内されて昇降するようになっている。

【００１３】昇降フレーム１７の水平部材１７ｂの先端には二叉状のクレビス部１７ｃが一体に形成されており、クレビス部１７ｃ内には両端にフランジ２２ｂを有する拘束輪２２がピン２３により回転可能に枢支されている。２２ａは拘束輪２２のドラム部である。

【００１４】拘束輪２２のドラム部２２ａに給電ケーブル８のＵ字状の屈曲部８ａが巻き掛けられ、拘束輪２２および昇降フレーム１７の重量を給電ケーブル８に掛けて給電ケーブル８に下方に向けて荷重を与えるようになっている。

【００１５】このように、上記給電ケーブルの張力付与装置によれば、給電ケーブル３は、拘束輪２２によって下方に向けて荷重を与えられており、かつ、拘束輪２２および昇降フレーム１７は、ガイドレール２６に案内されているので、クレーン移動の際、クレーン１の急速な加減速が行われても、給電ケーブル８の屈曲部８ａが拘束されて振れることがない。

【００１６】

【発明が解決しようとする課題】しかしながら、上記特開平９－１５６８７３に示された倉庫設備用クレーンにおける給電ケーブルの張力付与装置では、給電ケーブルに拘束輪や昇降フレームなどの重量を作用させて給電ケーブルの振れを防止しているが、拘束輪や昇降フレームなどの重量を重くし過ぎると、給電ケーブルの線が切断するなどのトラブルが発生したりする一方、軽くし過ぎると拘束輪が給電ケーブルの慣性に負けて上下動してしまうという問題がある。

【００１７】本発明は、上記のような問題点を解決するために創案したもので、給電ケーブルに過大な荷重を掛けず、クレーンを移動する際や荷台を昇降する際に、クレーンの急速な加減速が行われても給電ケーブルの振れを防止し、かつ、給電ケーブルの線の切断を防止するとともに、給電ケーブルの巻き癖取り作業をなくして現地作業時間の短縮を図るようにした自動倉庫用クレーンの給電装置を提供することを目的とするものである。

【００１８】

【課題を解決するための手段】本発明によれば、一対のマストと、該マストに沿って昇降する荷台と、一端をマストの高さ方向の中間部に固定するとともに、他端を荷台に固定して中間が垂下してＵ字状の屈曲部を形成した給電ケーブルと、マストに平行に設けたガイドレールと、該ガイドレールに昇降可能に配設した昇降フレームと、該昇降フレームに取り付けられ、上記給電ケーブルの屈曲部が巻き掛けられた拘束輪とを有してなる自動倉庫用クレーンの給電装置であって、上記拘束輪は上記昇降フレームに枢支された揺動フレームに取り付けられており、昇降フレームは一端をマストの高さ方向のほぼ中間部に固定し、他端を荷台に固定したワイヤロープによりロープシーブを介して吊り下げるようにしてなる自動倉庫用クレーンの給電装置が提供される。

【００１９】本発明の好ましい実施形態によれば、前記揺動フレームの先端側上面とロープシーブ支持材下面との間に、給電ケーブルに張力を付与する弾性体を配設している。

【００２０】次に本発明の作用について説明する。昇降フレームは、一端をマストの高さ方向のほぼ中間部に固定し、他端を荷台に固定したワイヤロープによりロープシーブを介して吊り下げられている。昇降フレームには揺動フレームが枢支されており、給電ケーブルのＵ字状の屈曲部は、この揺動フレームに取り付けられた拘束輪のドラム部に巻き掛けられている。昇降フレームは、その上下端部に設けたガイドローラによってマストに平行に設けたガイドレールに案内されて昇降するので、水平方向への動きはほとんどない。昇降フレームは、一端をマストの高さ方向のほぼ中間部に固定し、他端を荷台に固定したワイヤロープによりロープシーブを介して吊り下げるようにしているので、給電ケーブルに過大な荷重を掛けず、クレーンの移動する際や荷台の昇降する際に、クレーンの急速な加減速が行われても給電ケーブルが振れないようにすることができ、かつ、給電ケーブルの巻き癖取り作業をなくして現地作業時間の短縮を図ることができる。

【００２１】また、昇降フレームをワイヤロープによって吊り下げるとともに、昇降フレームに枢支された揺動アームとロープシーブ支持材との間に、弾性体（ばね）を配設して給電ケーブルに拘束輪の重量に加えてばねの弾発力による張力を付与するようにしているので、弾発力を調整することにより給電ケーブルに過大な荷重を掛けることがない。

【００２２】

【本発明の実施の形態】以下、本発明の好ましい一実施形態について、図面を参照して説明する。図１は自動倉庫用クレーンの給電装置の側面図である。図２は図１のＡ－Ａ矢視図であり、図３は図１のＢ－Ｂ矢視図である。なお、これらの図において、図４ないし図８で説明したものと共通の部分については同じ符号を付して説明し、重複する説明は省略する。

【００２３】図１ないし図６に示すように、自動倉庫用クレーンの給電装置は、一対のマスト３と、このマスト

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３に沿って昇降する荷台５と、一端をマスト３の高さ方向の中間部に固定するとともに、他端を荷台５に固定して中間が垂下してＵ字状の屈曲部８ａを形成した給電ケーブル８と、マスト３に平行に設けたガイドレール２６と、このガイドレール２６に昇降可能に配設した昇降フレーム１７と、この昇降フレーム１７に取り付けられ、上記給電ケーブル８の屈曲部８ａが巻き掛けられた拘束輪２２とを有しており、上記拘束輪２２は上記昇降フレーム１７に枢支された揺動フレーム２０に取り付けられており、昇降フレーム１７は一端をマスト３の高さ方向のほぼ中間部に固定し、他端を荷台５に固定したワイヤロープ２７によりロープシーブ３０を介して吊り下げるようにしている。

【００２４】昇降フレーム１７は、その高さ方向の中間部に給電ケーブル８側に突出するように固定されたアーム１８によりＴ字状に形成されており、その上下端部に配設したガイドローラ１７ａによりガイドレール２６に嵌入され、ガイドレール２６に案内されて昇降するようになっている。ガイドレール２６は、複数のブラケット２５を介してマスト３に平行に固定されている。２６ａはガイドレール２６の開口部である。昇降フレーム１７は、一端をマスト３の高さ方向のほぼ中間部に設けたアーム２８に固定し、他端を荷台５に設けたアーム２９に固定したワイヤロープ２７によりロープシーブ３０を介して吊り下げるようにしている。昇降フレーム１７のアーム１８の上部には、給電ケーブル８を挿通させるための開口１９ａを有する平板状のロープシーブ支持材１９が固定されており、その上面に設けた突起１９ｂにピン３１を介してロープシーブ３０が枢支されている。また、アーム１８の下部には、水平断面がコ字状の揺動フレーム２０が後端に設けた突起２０ｂを介してピン２１により上下動可能に枢支されている。この揺動フレーム２０のコ字状部内には、ドラム２２ａとその両端にフランジ２２ｂを有する拘束輪２２がピン２３により回転可能に枢支されている。拘束輪２２は、そのドラム部２２ａに給電ケーブル８のＵ字状の屈曲部８ａを巻き掛けている。２４はコ字状の揺動フレーム２０の上面とロープシーブ支持材１９の下面との間に配設した弾性体（ばね）で、揺動フレーム２０を常に下方に押し下げるようにしており、拘束輪２２を介して給電ケーブル８に下方に向けて荷重を与えるようになっている。また、コ字状の揺動フレーム２０の両先端には、上方に突出した突起２０ａが固定されており、通常は突起２２ａの上面とロープシーブ支持材１９の下面との間に隙間Ｈを設けるようにしていて、揺動フレーム２０がばね２４に抗して上方に回転しても拘束輪２２がロープシーブ支持材１９に衝突しないようになっている。

【００２５】給電ケーブル８は、一端を荷台５に留金具９ａにより固定して垂下し、拘束輪２２に巻き掛け、ロープシーブ支持材１９の開口１９ａを挿通して引き上げられ、ワイヤロープ固定用アーム２８に留金具９により固定され、先端は図示しない機上制御盤に接続される。なお、給電ケーブル８は複数のケーブルによって形成されている。

【００２６】次に本実施形態の作用について説明する。昇降フレーム１７は、一端をマスト３の高さ方向のほぼ中間部に固定し、他端を荷台５に固定したワイヤロープ２７によりロープシーブ３０を介して吊り下げられている。昇降フレーム１７には揺動フレーム２０が枢支されており、給電ケーブル８のＵ字状の屈曲部８ａは、この揺動フレーム２０に取り付けられた拘束輪２２のドラム部２２ａに巻き掛けられている。昇降フレーム１７は、その上下端部に設けたガイドローラ１７ａによってマスト３に平行に設けたガイドレール２６に案内されて昇降するので、水平方向への動きはほとんどない。昇降フレーム１７は、一端をマスト３の高さ方向のほぼ中間部に固定し、他端を荷台５に固定したワイヤロープ２７によりロープシーブ３０を介して吊り下げるようにしているので、給電ケーブル８に過大な荷重を掛けず、クレーン１の移動する際や荷台５の昇降する際に、クレーン１の急速な加減速が行われても給電ケーブル８が振れないようにすることができ、かつ、給電ケーブル８の巻き癖取り作業をなくして現地作業時間の短縮を図ることができる。

【００２７】また、昇降フレーム１７をワイヤロープ２７によって吊り下げるとともに、昇降フレーム１７に枢支された揺動アーム２０とロープシーブ支持材１９との間に、弾性体（ばね）２４を配設して給電ケーブル８に張力を付与するようにしているので、給電ケーブル８に過大な荷重を掛けることがない。

【００２８】本発明は、上記実施形態に限定されるものではなく、たとえば、昇降フレームに枢支した揺動フレームを、ピンに替えてスライド部材により水平に昇降可能に設けてもよいなど本発明の要旨を逸脱しない範囲で種々の変更が可能である。

【００２９】

【発明の効果】以上述べたように、本発明によれば、給電ケーブルに拘束輪や昇降フレームなどの重量を作用させるとともに、昇降フレームをワイヤロープによりロープシーブを介して吊り下げて給電ケーブルに過大な荷重を掛けないようにしているので、給電ケーブルの振れを防止することができるとともに、給電ケーブルの線を切断したり、拘束輪が給電ケーブルの慣性に負けて上下動してしまうのを防止することができ、かつ、給電ケーブルの巻き癖取り作業をなくして現地作業時間の短縮を図ることができるなど優れた効果を奏する。

【図面の簡単な説明】

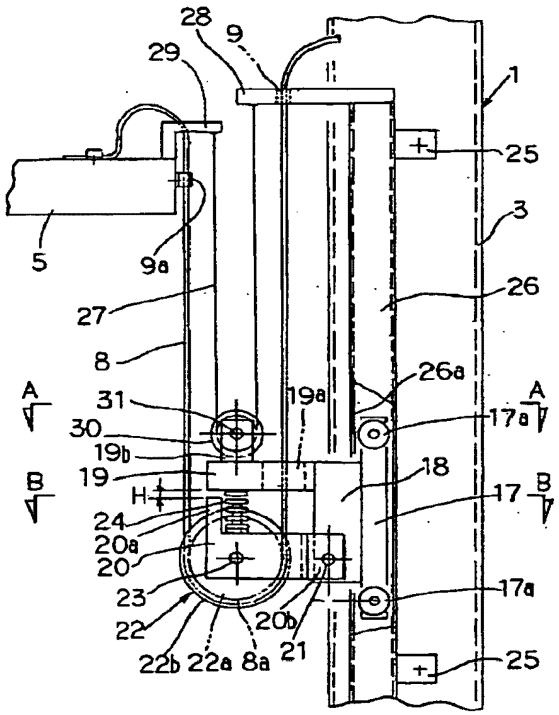
【図１】本発明の自動倉庫用クレーンの給電装置の正面図ある。

【図２】図１のＡ－Ａ矢視図である。

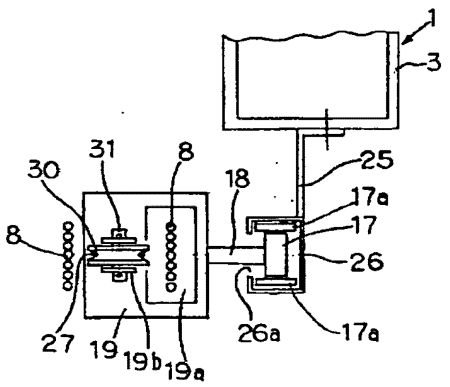
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【図３】図１のＢ－Ｂ矢視図である。
【図４】従来の自動倉庫用クレーンおよび棚列の概要を示す側面図である。
【図５】図４のＣ－Ｃ矢視図である。
【図６】図４のＤ－Ｄ矢視図である。
【図７】特開平９－１５６８７３に示された倉庫設備用クレーンにおける給電ケーブルの張力付与装置の一部拡大側面図である。
【図８】図７のＥ－Ｅ矢視図である。
【符号の説明】
１　倉庫用クレーン
２　下部フレーム
２ａ　走行車輪
３　マスト
４　上部フレーム
４ａ　ガイドローラ
５　荷台
６　移載装置
８　給電ケーブル
８ａ　給電ケーブルの屈曲部
１０　床面
１１　走行路
１２　走行レール
１３　上部ガイドレール
１４　棚列
１５　荷
１６　入出庫台
１７　昇降フレーム
１７ａ　ガイドローラ
１８　水平アーム
１９　ロープシーブ支持材
１９ａ　開口部
１９ｂ，２０ａ，２０ｂ　突起
２０　揺動フレーム
２１，２３，３１　ピン
２２　拘束輪
２２ａ　ドラム
２２ｂ　フランジ
２４　弾性体（ばね）
２５　ブラケット
２６　ガイドレール
２７　ワイヤロープ
２８，２９　ワイヤロープ固定用アーム
３０　ロープシーブ

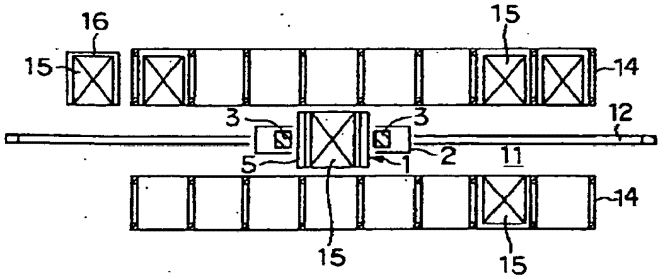
【図１】



【図２】

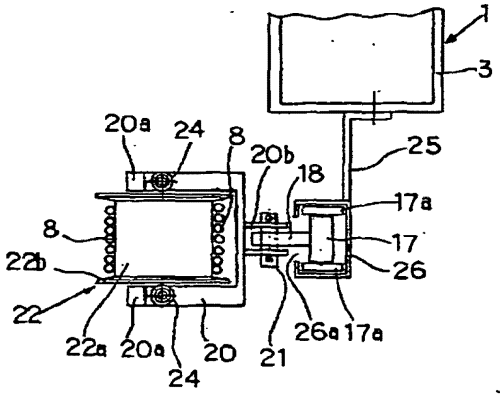


【図５】

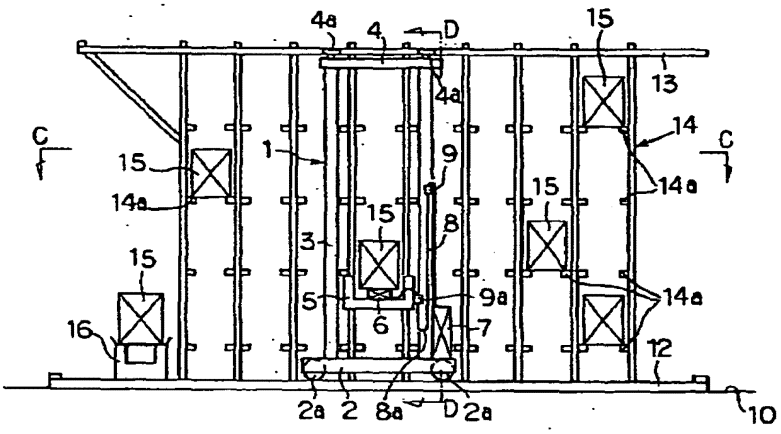


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SDT00000155

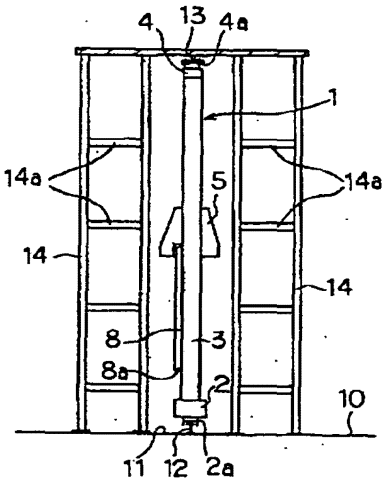
【図３】



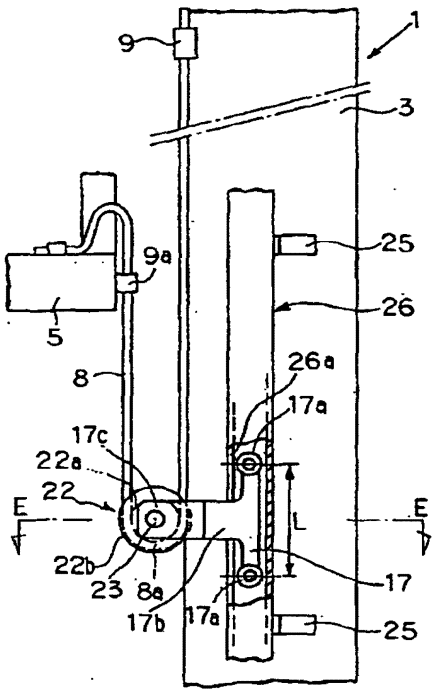
【図４】



【図６】

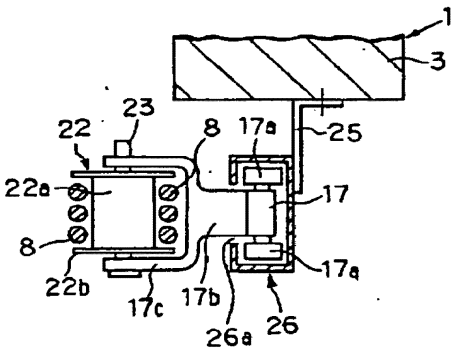


【図７】



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【図８】



フロントページの続き

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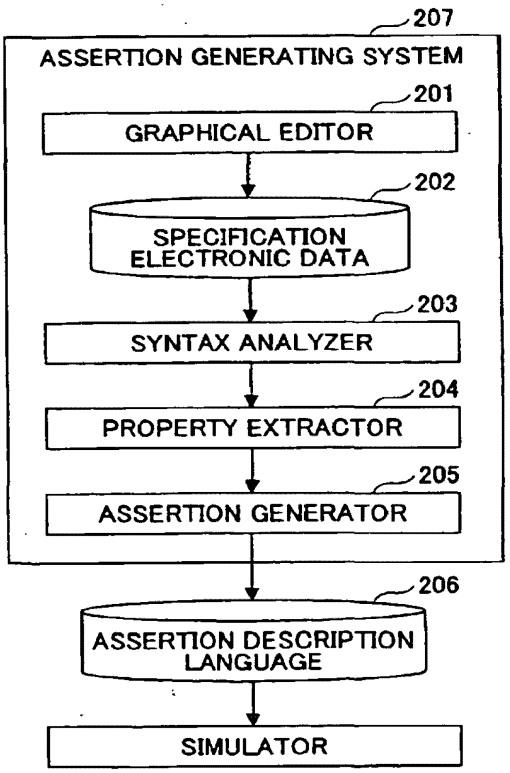
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[Continued on next page]

(54) Title: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD



(57) Abstract: An assertion generating system is disclosed. In an assertion generating system 207, a graphical editor 201 generates design data of a semiconductor integrated circuit by graphically editing a specification (finite state machine, process sequence) of the semiconductor integrated circuit with the use of a state transition table and a state transition figure or by editing the process sequence into a timing chart and a time series figure based on user operations, and a syntax analyzer 203 and a property extractor 204 generate a property that verifies the specification of the semiconductor integrated circuit based on the design data. The assertion generator 205 converts the property into an assertion description language 206.

WO 2006/035854 A1

European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

— *with international search report*

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
ITOH, Tadahiko

32nd Floor, Yebisu Garden Place Tower, 20 -3, Ebisu 4-chome, Shibuya -ku, Tokyo 1506032 Japan

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	08.11.2005
Applicant's or agent's file reference	**FOR FURTHER ACTION** See paragraph 2 below
R05160PCT	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/JP2005/017921	21.09.2005	30.09.2004

International Patent Classification (IPC) or both national classification and IPC
Int.Cl.[7] ***G06F17/50*** (2006. 01)

Applicant
RICOH COMPANY, LTD.

1. This opinion contains indications relating to the following items:
   - ☑ Box No. I Basis of the opinion
   - ☐ Box No. II Priority
   - ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - ☐ Box No. IV Lack of unity of invention
   - ☑ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - ☐ Box No. VI Certain documents cited
   - ☐ Box No. VII Certain defects in the international application
   - ☐ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

   If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

   If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

   For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Date of completion of this opinion	14.10.2005
Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office	HAYAKAWA, Manabu
3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Telephone No. +81-3-3581-1101 Ext. 3531

5H 9652

Form PCT/ISA/237 (cover sheet) (April 2005)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2005/017921

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☑ the international application in the language in which it was filed

   ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material

   ☐ on paper

   ☐ in electronic form

   c. time of filing/furnishing

   ☐ contained in the international application as filed

   ☐ filed together with the international application in electronic form

   ☐ furnished subsequently to this Authority for the purposes of search

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

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SDT00000161

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2005/017921

Box No. V **Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-15	YES
	Claims		NO
Inventive step (IS)	Claims		YES
	Claims	1-15	NO
Industrial applicability (IA)	Claims	1-15	YES
	Claims		NO

2. Citations and explanations:

D1. JP 7-49887 A (TOSHIBA CORP.) 1995.02.21, abstract, paragraph 0009-0013, Fig. 1-7 family none

D2: TransEDA Announces Industry-First Property Capture and Validation Product, [online], 2003.06.02, [retrieved on 2005.10.14], Retrieved from the Internet:<URL: http://www.transeda.com/news/view.php?id=54&syear=2003 >
& <URL: http://www.transeda.com/news/languages/Japanese_54.doc >

The subject matter of claim 1-15 does not appear to involve an inventive step in view of the D1 cited in the ISR and the D2 cited in the same.

Form PCT/ISA/237 (Box No. V) (April 2005)

Document made available under the Patent Cooperation Treaty (PCT)

International application number: PCT/JP2005/017921

International filing date: 21 September 2005 (21.09.2005)

Document type: Certified copy of priority document

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Number: 2004-286042
Filing date: 30 September 2004 (30.09.2004)

Date of receipt at the International Bureau: 28 October 2005 (28.10.2005)

Remark: Priority document submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b)



World Intellectual Property Organization (WIPO) - Geneva, Switzerland
Organisation Mondiale de la Propriété Intellectuelle (OMPI) - Genève, Suisse

日 本 国 特 許 庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出 願 年 月 日 Date of Application:	２００４年　９月３０日
出 願 番 号 Application Number:	特願２００４－２８６０４２
パリ条約による外国への出願に用いる優先権の主張の基礎となる出願の国コードと出願番号 The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is	ＪＰ２００４－２８６０４２
出 願 人 Applicant(s):	株式会社リコー

２００５年１０月１２日

特許庁長官
Commissioner,
Japan Patent Office

中嶋 誠

Cadence Design Systems, Inc. - Ex. 1002, Page 00120

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【提出日】　平成16年 9月30日
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【国際特許分類】　G06F 17/30
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　【連絡先】　担当
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　【包括委任状番号】　9808799

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【書類名】特許請求の範囲
【請求項１】
半導体集積回路のアサーション検証に用いるアサーション記述を生成するアサーション生成システムであって、
ユーザ操作に基づき上記半導体集積回路の仕様をグラフィカルに編集して当該半導体集積回路の設計データもしくは仕様書及び仕様書確認用のドキュメントを生成する仕様入力手段と、
該仕様入力手段で生成した設計データを記憶する第１の記憶手段と、
該第１の記憶手段から上記仕様入力手段が生成した設計データを読み出し、該設計データを元に、上記半導体集積回路の仕様に関して検証すべきプロパティを生成するプロパティ生成手段と、
該プロパティ生成手段で生成したプロパティを記憶する第２の記憶手段と、
該第２の記憶手段から上記プロパティ生成手段が生成したプロパティを読み出し、該プロパティをアサーション記述に変換するアサーション生成手段と
を有することを特徴とするアサーション生成システム。
【請求項２】
請求項１に記載のアサーション生成システムであって、
上記仕様入力手段は、
ユーザ操作に基づき上記半導体集積回路の仕様を状態遷移表もしくは状態遷移図で編集して当該半導体集積回路の設計データを生成する手段を有することを特徴とするアサーション生成システム。
【請求項３】
請求項１に記載のアサーション生成システムであって、
上記仕様入力手段は、
ユーザ操作に基づき上記半導体集積回路の処理シーケンスをタイミングチャートもしくは時系列に図示して編集し、当該半導体集積回路の設計データを生成する手段を有することを特徴とするアサーション生成システム。
【請求項４】
請求項１から請求項３のいずれかに記載のアサーション生成システムであって、
上記仕様入力手段は、
ユーザ操作に基づき上記半導体集積回路の仕様を論理テーブルもしくは状態テーブルで編集して、当該半導体集積回路の設計データを生成する手段を有することを特徴とするアサーション生成システム。
【請求項５】
請求項４に記載のアサーション生成システムであって、
上記アサーション手段は、
上記仕様入力手段で編集した論理テーブルもしくは状態テーブルのテーブル名あるいはテーブルの行番号、または、当該論理テーブルもしくは状態テーブルにおける信号名あるいは状態名で構成されたアサーション名を付加されたアサーション記述に変換することを特徴とするアサーション生成システム。
【請求項６】
請求項１から請求項５のいずれかに記載のアサーション生成システムであって、
上記仕様入力手段は、
上記設計データをグラフ構造に展開し、上記第１の記憶手段に出力することを特徴とするアサーション生成システム。
【請求項７】
コンピュータを、請求項１から請求項６のいずれかに記載のアサーション生成システムにおける各手段として機能させるためのプログラム。
【請求項８】
請求項１から請求項６のいずれかに記載のアサーション生成システムを具備し、該アサー

ション生成システムで生成したアサーション記述を用いて半導体集積回路のアサーション検証を行うことを特徴とする回路検証システム。

【請求項９】

半導体集積回路のアサーション検証に用いるアサーション記述を、プログラムされたコンピュータによって生成するアサーション生成方法であって、

ユーザ操作に基づき上記半導体集積回路の仕様をグラフィカルに編集して当該半導体集積回路の設計データを生成して記憶装置に入力する仕様入力手順と、

上記記憶装置から上記仕様入力手順で生成した設計データを読み出し、該設計データを元に、上記半導体集積回路の仕様に関して検証すべきプロパティを生成して記憶装置に入力するプロパティ生成手順と、

上記記憶装置から上記プロパティ生成手順で生成したプロパティを読み出し、該プロパティをアサーション記述に変換するアサーション生成手順と

を有することを特徴とするアサーション生成方法。

【請求項１０】

請求項９に記載のアサーション生成方法であって、

上記仕様入力手順では、

ユーザ操作に基づき上記半導体集積回路の仕様を状態遷移表もしくは状態遷移図で編集して当該半導体集積回路の設計データを生成することを特徴とするアサーション生成方法。

【請求項１１】

請求項９に記載のアサーション生成方法であって、

上記仕様入力手順では、

ユーザ操作に基づき上記半導体集積回路の処理シーケンスをタイミングチャートもしくは時系列に図示して編集し、当該半導体集積回路の設計データを生成することを特徴とするアサーション生成方法。

【請求項１２】

請求項９から請求項１１のいずれかに記載のアサーション生成方法であって、

上記仕様入力手順では、

ユーザ操作に基づき上記半導体集積回路の仕様を論理テーブルもしくは状態テーブルで編集して、当該半導体集積回路の設計データを生成することを特徴とするアサーション生成方法。

【請求項１３】

請求項１２に記載のアサーション生成方法であって、

上記アサーション手順では、

上記仕様入力手順で編集した論理テーブルもしくは状態テーブルのテーブル名あるいはテーブルの行番号、または、当該論理テーブルもしくは状態テーブルにおける信号名あるいは状態名で構成されたアサーション名を付加されたアサーション記述に変換することを特徴とするアサーション生成方法。

【請求項１４】

請求項９から請求項１３のいずれかに記載のアサーション生成方法であって、

上記仕様入力手順では、

上記設計データをグラフ構造に展開して上記記憶装置に記憶することを特徴とするアサーション生成方法。

【書類名】明細書
【発明の名称】アサーション生成システムと回路検証システムおよびプログラムならびにアサーション生成方法
【技術分野】
【０００１】
本発明は、コンピュータのプログラムに基づく処理により、ＬＳＩ（Large Scale Integration、大規模集積回路）等の回路検証を行う技術に係わり、特に、レジスタ転送レベルの設計データをシミュレータでダイナミックに検証するときに、検証対象回路のプロパティをアサーション記述してシミュレータに加味させることで設計違反や検証漏れを確認するようにした検証技術に関するものである。
【０００２】
ここで言うプロパティとは、検証対象の設計品に意図・期待される動作を定義する平叙文（プレーン・テキスト）であり、例えば、アービタ回路における要求信号と承認信号の受信や応答の関係を時系列制約で定義したり、時系列制約の正当状態や、禁止される回路仕様を定義したりするものである。その他、特定の回路シーケンスがシミュレーションでテストされたかどうかを確認する機能カバレッジ・ポイントとして監視すべきイベントとされる。設計記述（デザイン）が所定のプロパティを満たしているかどうかを検証することをプロパティ検証という。
【背景技術】
【０００３】
近年、半導体集積回路においては回路規模の増大化と複雑さのためにコーナーケースの検証漏れや、グループワークのために複数の設計者へ設計担当を割り振った際の各担当ブロック間のインターフェース仕様の確認漏れ、あるいは、第三者から購入した再利用可能なコアの誤仕様などが原因でシステムの改定や改版がしばしば発生している。
【０００４】
これらの問題の要因は、十分に回路検証が出来ていなかったか、もしくはコーナーケースや第三者のコアの仕様を十分に理解できていないためにバグを抽出し得るテストシナリオを作成できなかった、などがある。
【０００５】
これらのことを背景に、検証用に回路仕様に関するプロパティをアサーション記述してシミュレータ（コンピュータ）に与え、シミュレーション中のアサーション違反の警告や、特定の回路シーケンスがシミュレーションでテストされたかどうかを示す機能カバレッジ・レポートを提供するようにしたアサーション検証技術が提案され、最近では実設計に適用され始めてきた。
【０００６】
アサーションは設計の意図(これをプロパティと指すこともある)を記した注釈であって、通常はＲＴＬ（Register Transfer Level）中にコメント文で記述する。検証期間中はシミュレータによってその意図が解釈され、例えば検証対象の回路がその意図とは異なる動作へ陥った場合はエラー・ログが生成される。ここでの設計の意図とは、例えば回路入力の仮定や前提条件であるほか、それらの条件が満たされた場合に期待する動作といったものを指す。
【０００７】
シミュレータは以下の二つのことをチェックする。
（１）仮定や前提条件といった特定のイベントが発生したかどうか
（２）そのときの期待動作が正しく完了するかどうか
【０００８】
上記（１）のチェックから、アサーションは特定の回路機能が検証で確認されたかどうかの判定材料をフィードバックする。よってアサーションを検証対象回路へ網羅的に埋め込んでおけばアサーションの被服率（機能カバレッジと呼ぶ）が得られ、これをもって検証精度を定量化できる。

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【０００９】
上記（２）のチェックから、アサーションによって検証デバッグへのフィードバックが得られる。例えば、回路の不具合の影響が外部端子で観測困難であるところへ埋め込まれたアサーションは不具合の状況を補足する。また、いかなるスティミュラス（Stimulus）においても仮定や前提条件などの条件が満されるときはいつでもこの期待動作がチェックされる。よって例えばスティミュラスがランダムな系列で構成されていたとしても期待動作との自己照合、すなわち期待値比較が実施される。また、下位ブロックに埋め込まれたアサーションはチップレベル検証においても同様に有効である。
【００１０】
これらの設計の意図は論理合成向けＲＴＬと区別された検証向けのVerilog-HDLで記述できるかも知れないが、ここでは別のアサーション言語について述べる。
【００１１】
現在、最も普及しているのが非特許文献１に記載のＰＳＬ（Property Specification Language）である。ＰＳＬはAcceleraという標準化規格団体によってIEEEへの寄贈が進行中のアサーション言語であり、事実上の標準言語である。以下、ＰＳＬによるアサーション記述の具体例を示す。
【００１２】
例えば、メモリ制御に関して次のような設計の意図（プロパティ）を検証で監視したいとする。
１）read-nとwrite-nは、同時にLowにはならない
２）write-nの立ち下がりで、enable-nはHighである
３）read-nの立ち下がりで、enable-nはLowである
【００１３】
これらをアサーションとしてシミュレータへ渡すためのＰＳＬ記述（アサーション記述）は以下の通りである。
【００１４】

```
// psl property memcont1 = never (!write-n && !read-n) @(posedge clk) ;
// psl assert memcont1 ;
// psl property memcont2 = always (enable-n) @(negedge write-n) ;
// psl assert memcont2 ;
// psl property memcont3 = always (!enable-n) @(negedge read-n) ;
// psl assert memcont3 ;
```

【００１５】
上記ＰＳＬ記述（アサーション記述）の内の「psl、property、never、assert、always」は全てＰＳＬの予約語である。全ての行はVerilog-HDLのコメントであることを示す「//」で開始する。尚、「//」に代えて「/**/」でＰＳＬの記述全体を閉じても良い。
【００１６】
また、上記ＰＳＬ記述（アサーション記述）の内の「memocont1、2、3、!write-n&&!read-n、posedge clk、enable-n、negedge write-n、!enable-n、negedge read-n」はユーザ定義の記述であって、「memocont1、2、3」以外は上記１）～３）の意図を定義するための具体的な実装データ名、すなわちＲＴＬ中に出現するメモリ制御信号名である。
【００１７】
また、memcont1～3はアサーション名であって、シミュレータからフィードバックされるエラー・ログや機能カバレッジの識別に使用される。
【００１８】
ＰＳＬによるアサーション記述は次の構成要素をとる。
【００１９】

```
// psl property <アサーション名> =
      <監視すべきイベント>  -> <条件が満たされたときの期待動作>
       @<ストローブ条件>;
```

// psl assert <アサーション名>;

【００２０】

例えば１）のアサーションであれば「memcont」がアサーション名、(!write-n && !read-n) が監視すべきイベントであって、この場合は先にneverが付加されている事により（ ）内の条件が決して真とならないことを監視する（仮にalwaysが付加される場合は（ ）内の条件が真であることがチェックされる）。これに続く@(posedge clk)によって条件の監視がclkの立ち上がりエッジのたびに行われることを定義している。「->」は何時、期待動作が開始されるかによって「|=>」、「|->」へ変化する。なお、上記の例は期待動作を付随していない。

【００２１】

ストローブ条件以外の各パートの（ ）内はブーリアンを返すVerilog-HDLの式で記述する。ストローブ条件の（ ）内はVerilog-HDLのalways文で記述するセンシティビティリストの記述形式をとる。

【００２２】

ＰＳＬは監視すべきイベントと、その条件が満たされたときの期待動作の各パートのそれぞれはシーケンスを、すなわち複数サイクルに渡るイベントの変化や期待動作といったものが定義できる。次の例を見てみる

【００２３】

・設計の意図：メモリのクリア処理では、クリア開始条件(m-taskが2'b00)が成立したならば、全ワード(２５６ワード)の初期化のための書込み操作が２５６回だけ継続される。ここで、一回の書込みはclkの立ち上がりサイクルに同期したwrite-nのLow→High→Highの動作で完了する。

【００２４】

・ＰＳＬ記述

```
// psl sequence WRITE-PULSE = { !write-n; write-n; write-n };
// psl property CLEAR-MEM-WRITE-N =
// always { m-task == 2'b00 } |=> { WRITE-PULSE [*256] }
// @(posedge clk);
// psl assert CLEAR-MEM-WRITE-N;
```

【００２５】

sequenceはwrite-nのLow→High→Highといったシーケンスをマクロ定義している。

ここで注目したいのは「|=>」に続く期待動作のパートである。m-task == 2'b00 であれば、WRITE-PULSE、すなわちwrite-nのLow→High→Highといった３サイクルにまたがるシーケンスが２５６回分、継続することを期待している。

【００２６】

しかし、このようなアサーション検証技術においては、例えば、仕様を定義する時に手入力でアサーション記述言語を書いた場合、アサーション自体にミスが混入してしまう可能性がある。その結果、アサーション検証によって得られたアサーション違反の警告や機能カバレッジのレポートと言うものはシステムの改定や改版を防ぐためのフィードバックとはな成り得ず、さらにはアサーション記述言語のデバッグのための検証期間を要してしまい、結果的に検証効率が悪くなってしまう。

【００２７】

すなわち、回路仕様とアサーション記述との整合性が一致していることがアサーション検証技術の大前提であるが、シミュレーションを実施するのに先んじてその整合性を確認する手立てがない。また、複雑な有限状態機械に関しては、人手によって網羅的な状態遷移のシーケンスを記述すること自体が困難である。

【００２８】

このようなアサーション検証に関しての従来技術としては、例えば、特許文献１および特許文献２に記載の技術がある。

【００２９】

特許文献１においては、状態遷移機械をグラフでモデル化し、アサーションを満たすべき状態遷移経路の探索に関する技術が示されている。また、このグラフの解析によってのみアサーションの正当性を確認する技術が示されている。これにより、回路仕様とアサーション記述との整合性を確認することができる。

【００３０】

しかし、この技術では、グラフ化する状態遷移機械は、人手で、基礎となる状態遷移機械のモデルを作成するか、もしくは、レジスタ転送レベルの記述言語で作成された設計データから抽出するようにしている。そのため、整合性一致の対象自体、すなわち、回路仕様であるべき状態遷移機械のモデルへのミスの混入は否めない。

【００３１】

また、特許文献２においては、レジスタ転送レベルの設計データからデータ転送の構造を抽出してグラフ構造へ展開し、対象回路に関して検証すべきアサーションを生成する技術が記載されている。しかし、この技術では、回路仕様であるアサーションが設計データから抽出されるので、回路仕様とアサーション記述との整合性一致は保証されない。

【００３２】

【特許文献１】特開２０００－１８１９３３号公報

【特許文献２】特開２０００－１４２９１８号公報

【非特許文献１】「Property Specification Language Reference Manual Version 1.1 June 9, 2004」、［online］、［平成１６年９月１４日検索］、インターネット<URL : http://http://www.eda.org/vfv/docs/PSL-v1.1.pdf

【発明の開示】

【発明が解決しようとする課題】

【００３３】

解決しようとする問題点は、従来の技術では、回路仕様とアサーション記述との整合性一致は保証されない点である。

【００３４】

本発明の目的は、これら従来技術の課題を解決し、例えばＬＳＩ等に対するアサーション検証の高信頼化および高効率化を可能とすることである。

【課題を解決するための手段】

【００３５】

上記目的を達成するため、本発明では、操作者が回路の仕様書を作成するときに使用した視覚的な状態遷移図やタイミングチャート、および、処理のシーケンス図等をもとにして、検証すべきプロパティを自動的にアサーション記述言語へ変換することを特徴とする。

【発明の効果】

【００３６】

本発明によれば、例えば仕様書に添付される状態遷移図の電子データから、検証すべきプロパティのアサーション記述を自動的に生成するので、回路仕様とアサーションとの整合性が一致する。これにより、アサーションのデバッグに費やす作業が削除できる。また、生成したアサーションは、状態遷移の経路を網羅的に探索して生成した機能カバレッジ・ポイントであるので、検証の後、どの経路がテストされていないかを機能カバレッジ・レポートからフィードバックでき、コーナーケースのテスト漏れを防ぐことができる。また、例えば仕様書に添付するタイミングチャートや信号の選択条件、あるいは処理のシーケンスを注釈もしくは定義した図形もしくは表形式の電子データから、検証すべきプロパティのアサーション記述を自動的に生成するので、回路仕様とアサーションとの整合性が一致する。これにより、アサーションのデバッグに費やす作業が削除できる。特に、仕様書に添付するタイミングチャートや信号の選択条件、または処理のシーケンスというのは検証時に必ずテストされなければならないほど重要なアサーションであることが多く、生成したアサーションは重要プロパティであり、仕様書や回路機能を熟知しない設計者がキー・プロパティを使って検証作業を行うことができ、最終的に検証漏れによるシステムの

改版率を低減させることが可能である。

【発明を実施するための最良の形態】

【００３７】

以下、図を用いて本発明を実施するための最良の形態例を説明する。

【００３８】

図１は、本発明に係わるアサーション生成システムおよび回路検証システムを構成するハードウェアの構成例を示すブロック図であり、図２は、本発明に係わるアサーション生成システムの第１の機能構成例およびそれを用いた回路検証システムの構成例を示すブロック図、図３は、本発明に係わるアサーション生成システムで用いられるグラフ構造のメモリイメージ例を示す説明図、図４は、本発明に係わるアサーション生成システムで用いられる状態遷移図とそのグラフ構造例を示す説明図、図５は、本発明に係わるアサーション生成システムの第２の機能構成例を示すブロック図、図６は、本発明に係わるアサーション生成システムの第３の機能構成例を示すブロック図、図７は、本発明に係わるアサーション生成システムで用いられるタイミングチャート例を示す説明図、図８は、本発明に係わるアサーション生成システムで用いられるタイミングチャート上で定義される信号に関する情報および当該信号に対するタイミング制約に関する情報を格納するための構造体例を示す説明図、図９は、図７におけるタイミングチャートに関するプロパティ情報のメモリイメージ例を示す説明図、図１０は、本発明に係わるアサーション生成システムの第４の機能構成例を示すブロック図、図１１は、本発明に係わるアサーション生成システムで用いられるフルアダーの論理テーブルの構成例を示す説明図、図１２は、表（テーブル）におけるセルをメモリ上に展開するときの１個のセルを表すための構造体例を示す説明図、図１３は、図１２におけるセルを表す構造体を組み合わせてシートを構成したときのイメージ例を示す説明図、図１４は、図１１におけるフルアダーの論理テーブルを図１３のメモリ構造へ展開したときのイメージ例を示す説明図、図１５は、本発明に係わるアサーション生成システムで用いられる処理シーケンスの表形式での構造例を示す説明図である。

【００３９】

図１において、１０１はメモリもしくはハードディスク等からなる記憶装置、１０２はＣＰＵ（Central Processing Unit、中央処理装置）、１０３はキーボードやマウスなどからなる入力装置、１０４はＣＲＴ（Cathode Ray Tube）やＬＣＤ（Lquid Crystal Display）等からなる表示装置、１０５はシステムバスであり、システムバス１０５で各装置１０１～１０４を接続することでコンピュータシステムを構成している。

【００４０】

記憶装置１０１では、アーキテクチャに依存しないハードウエア機能記述や本発明に係わる各機能・手段を、ＣＤ－ＲＯＭ（Compact Disc-Read Only Memory）やＤＶＤ（Digital Video Disc/Digital Versatile Disc）あるいはＦＤ（Flexible Disk）等のコンピュータ読み取り可能な記録媒体から読み取られた実行可能なプログラムの形式で格納する。ＣＰＵ１０２は、記憶装置１０１に記憶されたプログラムを実行することで、図２に示す構成のアサーション生成システムにおける各機能としての処理を実行する。

【００４１】

入力装置１０３を用いて、ユーザは、アーキテクチャに依存しないハードウエア機能記述の入力・編集や本発明の各手段を実現したプログラムの実行命令を対話的に入力する。そして、表示装置１０４において、アーキテクチャに依存しないハードウエア機能記述の表示や、ＣＰＵ１０２による本発明の各手段を実現したプログラムの実行経過や実行結果を表示する。

【００４２】

図２においては、本発明に係るアサーション生成システム２０７およびそれを用いた回路検証システムの基本構成を示しており、まず、グラフィカルエディタ２０１において、ユーザ操作により、仕様書に明記すべき回路仕様が入力され、このグラフィカルエディタ２０１で作成された仕様書は、電子データ２０２として、記憶装置１０１に記憶される。

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尚、グラフィカルエディタ２０１としては、例えば、特開平１－３０９１８５号公報に記載のタイミングチャート・エディタ等のグラフィカルエディタを用いることができる。

【００４３】

次に、構文解析器２０３により、記憶装置１０１に記憶された電子データ２０２を読み出して構文解析し、この構文解析結果から、プロパティ抽出器２０４により、検証すべきプロパティを抽出する。

【００４４】

そして、アサーション生成器２０５において、プロパティ抽出器２０４で抽出したプロパティから、シミュレータや静的プロパティチェッカへ入力可能なアサーション記述言語２０６を生成する。このようにして生成されたアサーション記述言語２０６は、記憶装置１０１に格納され、シミュレータに入力され、検証が行われる。

【００４５】

このように、本例のアサーション生成システムでは、半導体集積回路や半導体集積回路の一部分の仕様に関するプロパティをアサーション記述した設計データと当該プロパティの対象回路の設計データとをシミュレータ、もしくは静的検証ツールで検証するアサーション検証を行うに際に、グラフィカルエディタ２０１において、有限状態機械の仕様を、状態遷移表や状態遷移図による視覚的表現で編集して仕様書電子データ（設計データ）を生成し、このようにグラフィカルエディタ２０１において定義した回路仕様に関し、構文解析器２０３およびプロパティ抽出器２０４において、当該設計データを基に検証すべきプロパティを生成し、アサーション生成器２０５において、このプロパティをアサーション記述によって出力する。

【００４６】

尚、グラフィカルエディタ２０１で作成された設計データ（仕様書電子データ）はメモリ上でグラフ構造に展開され、プロパティ生成抽出器２０４によって参照可能となっている。また、グラフィカルエディタ２０１で作成される設計データ（仕様書電子データ）には、状態遷移表や状態遷移図の他に、表入力や図形を編集可能なビジネスツールを用いて回路の処理シーケンスをタイミングチャートや時系列に図示したものも適用できる。

【００４７】

図５においては、グラフィカルエディタ２０１で作成される設計データ（仕様書電子データ）として「状態遷移図」を適用する際の例を示している。本図５において、グラフィカル情報５０１は、例えば図４（ａ）に例示される状態遷移図であり、グラフィカルエディタによって編集、作成され、システムメモリ、もしくはハードディスク等の記憶装置に格納されている。

【００４８】

また、このグラフィカル情報５０１は、視覚的情報、すなわち状態遷移図の各構成要素を配置したときの座標情報などを含んでおり、視覚的に表示された状態遷移図はプリントアウトして仕様書に添付できるようになっている。

【００４９】

グラフ探索エンジン５０２は、図２における構文解析器２０３とプロパティ抽出器２０４の機能を有し、グラフィカル情報５０１としての図４（ａ）に例示する状態遷移図から、図４（ｂ）に例示するグラフ構造を抽出し、システムメモリ上に展開する。抽出したグラフは状態遷移図の各構成要素をノードとして構成されており、グラフ探索エンジン５０２は、状態遷移の経路を探索する。例えば、状態遷移機械の初期状態からのあらゆる遷移パスを探索し、それらを抽出し、経路データベース（図中「経路ＢＤ」と記載）５０３として、システムメモリに展開、もしくはハードディスク上に格納する。

【００５０】

そして、プロパティ変換器５０４は、経路データベース５０３を参照して、グラフ探索エンジン５０２で探索した状態遷移パスをアサーション記述言語５０５へ変換する。このプロパティ変換器５０４での変換後のアサーション記述言語５０５は、例えば、シミュレーションでテストされたかどうかを確認するための機能カバレッジ・ポイントとして記述

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される。

【００５１】

グラフ探索エンジン５０２で使用するグラフ構造のメモリイメージを、図３に示す。この図３において、３０１は状態遷移図中の各状態に関する情報を保持するための構造体であり、３０２は状態遷移図中のアークに関する情報を保持するための構造体である。これらの構造体３０１，３０２は、相互にポインタ参照しており、それぞれのポインタをノードとしたグラフを構成する。

【００５２】

図４においては、図４（ａ）に状態遷移図の例を示し、それから生成されるグラフ構造を図４（Ｂ）に示す。図５のグラフ探索エンジン５０２の処理は、図４（ａ）に示す状態遷移図に対して、グラフ理論における経路探索、例えば最短経路探索のアルゴリズムなどを利用して状態遷移経路を探索するようにしている。その結果として、図４（ｂ）に示すグラフ構造が生成され、経路データベース５０３に格納される。

【００５３】

以下に、図４の例を用いて、図５の経路データベース５０３に格納されうる状態遷移パスを例示す。

【００５４】

```
Init ;
(G0) S1 ;
init ;
```

【００５５】

この例では、initからS1への経路が探索されており、しかもそれは「G0」が真、すなわち「１」である場合に、その状態遷移パスが成立することを表している。

【００５６】

また、この状態遷移パスから、図５のプロパティ変換器５０４（図２におけるアサーション生成器２０５）にり生成されるアサーション記述をＰＳＬで以下に例示する。

【００５７】

```
property init-to-S1 = always { state == init & G0} |=> { state == S1};
```

【００５８】

状態遷移機械の場合、検証で全ての状態を訪問したか、と言ったことも回路機能の鍵となる重要機能の検証精度の定量化のために必要となる。状態遷移機械の各状態が訪問されたかとうかはＰＳＬのcover構文で状態の検証の被服率を確認すればよい。図４の例であれば、グラフのノードに格納された状態名をＰＳＬのcover記述でリスト生成するだけでよい。

【００５９】

以下にその結果を示す。ここでstateは状態遷移機械の実装時に状態を保持するための状態レジスタ名である。

【００６０】

```
// psl cover ( state == init);
// psl cover ( state == S1);
```

【００６１】

尚、図５におけるグラフィカル情報５０１が、座標情報と共に、図３および図４（ｂ）に示すように、グラフ構造に関する情報を併せ持つようにした場合、グラフ探索エンジン５０２は、直接、グラフィカル情報５０１内のグラフ構造を参照する。

【００６２】

次に、図６を用いて他の実施例を説明する。本図６に示す例では、仕様書に添付すべきタイミングチャートの電子データ６０１からタイミングチャート情報を抽出し、検証すべき信号群のタイミングに関する相互関係をアサーション記述するようにしている。

【００６３】

図６において、６０２はタイミングチャートの電子データ６０１を読みとるタイミング

チャート読み取り器、６０３は検証すべき信号群のタイミングに関する相互関係（タイミングチャート情報）を抽出してタイミングチャートデータベース（ＤＢ）６０４に格納するタイミング・プロパティ抽出器、６０５はタイミングチャートデータベース（ＤＢ）６０４からタイミングチャート情報を読み出してシミュレータや静的プロパティチェッカへ入力可能なアサーション記述言語６０６を生成するプロパティ変換器である。

【００６４】

尚、タイミングチャートの電子データ６０１は、タイミングチャート・エディタで作成・編集されたものでよく、その場合のタイミングチャート読み取り器６０２は、タイミングチャート・エディタで作成・編集されたタイミングチャート情報の構文解析器で構成される。

【００６５】

タイミング・プロパティ抽出器６０３で使用するメモリイメージを図８に示す。本図８において、８０１はタイミングチャート上で定義される信号に関する情報を格納するための構造体であって、８０２は前記信号に対して相互にタイミング制約に関する情報を格納するための構造体である。

【００６６】

タイミングチャート読み取り器６０２で読み取るタイミングチャートの具体例を図７に示す。本図７に示す例では、clkに同期してreqの立ち上がりから２～５サイクルの間にackが立ち上がることを示している。

【００６７】

このように、図７の例では「reqの出力信号が１になった後、clkの２～５クロックの範囲でackの立ち上がりを受信しなければならない」というタイミング制約（プロパティ）が描かれている。

【００６８】

そして、図６のタイミング・プロパティ抽出器６０３は、IN,OUT,CKなどの信号属性や、立ち上がり条件を意味する「pos」、「<-」、「->」のような信号群のタイミングに関する相互関係をキーワードにして検証すべきタイミング情報（プロパティ）を抽出する。

【００６９】

この結果、図７に示すタイミングチャート・エディタで作成・編集されたタイミングチャート情報は、例えば、以下のリストに編集されハードウエアに格納される。ここでは、１～３行目はピンと、例えばクロック入力であるとか入出の属性を宣言している。４～７行目は波形情報である。このうち６行目は「clkに同期してreqの立ち上がりから２～５サイクルの間にackが立ち上がる」というプロパティが示されている。

【００７０】

```
1  CK      clk;
2  IN      ack;
3  OUT     req;
4  {clk,req,ack} = {1,0,0};
5  {clk,req,ack} = {1,1,0};
6  {clk,req,ack} = {1,0,0}[2:5];
7  {clk,req,ack} = {1,0,1};
```

【００７１】

このタイミングチャート情報リストをもとに展開されたタイミングに関するプロパティ情報のメモリイメージを、図９に例示する。

【００７２】

次に、上述した回路の論理テーブルや時系列プロパティの編集に、表入力や図形の編集可能なビジネスツールを用いる例を説明する。

【００７３】

図１１は、フルアダーの論理テーブルをマイクロソフト社の表入力ツールであるＥｘｃｅｌ（登録商標）で入力したものである。太字で示したNAME,CLOCK,CONDITION,EXPECTは

表定義する際の予約語であって、それぞれプロパティ名、クロック名、アサーション・チェックの開始条件、アサーション・チェックが開始されたときの期待動作を表す。

【００７４】

また、CONDITION,EXPECTのすぐ下の欄は信号名であり、その下には論理値が続いている。このＥｘｃｅｌ（登録商標）によれば表の一こまを「セル」という基本単位で面（シートと呼ばれる）を構成しており、各セルを「,」で区切ったASCIIファイルで出力可能である。

【００７５】

図７の場合は、信号名やクロックの１／２パルス等をセルで管理し、いったんメモリ上へ展開した後にセルの構成を走査して、図９に示すメモリイメージへ展開するようにした。

【００７６】

図１２は、Ｅｘｃｅｌ（登録商標）のセルをメモリ上に展開するときの１個のセルを表すための構造体である。この構造体のtop,bottom,left,rightのメンバは、それぞれセルの上下、左右をポインタ参照する。

【００７７】

図１３は、図１２のセルを表す構造体を組み合わせてシートを構成したときのイメージ図である。１３０１はシートを示すポインタであって、次のシートのポインタ参照であるnextとセルのヘッダをポインタ参照するメンバで構成している。１３０２はセルのポインタであって、top,bottom,left,rightのメンバで上下、左右をポインタ参照している。こうしておけばシート上のセルの走査がメモリ上で容易に可能であり、NAME,CLOCK,CONDITION,EXPECTといったキーワードによる検索と論理テーブルの解釈が可能である。

【００７８】

図１４には、図１１のフルアダーの論理テーブルを図１３のメモリ構造へ展開したときのイメージを示している。

【００７９】

また、以下に、図１１で示したフルアダーの論理テーブルからアサーション記述を生成したＰＳＬ記述を示す。ここでは、アサーション名の構成に表の行番号を含ませることで表と検証データ（すなわちアサーション）とが容易にリンクできるようにしている。例えば１行目であればFADD-S-0--FADD-csv-line-5がアサーション名であって、このうちline-5は表の行番号に相当している。

【００８０】

```
psl property FADD-S-0--FADD-csv-line-5 = always {!A & !B & !CI} |-> {S === 1'b0}
;
psl property FADD-CO-0--FADD-csv-line-5 = always {!A & !B & !CI} |-> {CO === 1'b
0};
psl property FADD-S-1--FADD-csv-line-6 = always {!A & !B & CI} |-> {S === 1'b1};
psl property FADD-CO-1--FADD-csv-line-6 = always {!A & !B & CI} |-> {CO === 1'b0
};
psl property FADD-S-2--FADD-csv-line-7 = always {!A & B & !CI} |-> {S === 1'b1};
psl property FADD-CO-2--FADD-csv-line-7 = always {!A & B & !CI} |-> {CO === 1'b0
};
psl property FADD-S-3--FADD-csv-line-8 = always {!A & B & CI} |-> {S === 1'b0};
psl property FADD-CO-3--FADD-csv-line-8 = always {!A & B & CI} |-> {CO === 1'b1}
;
psl property FADD-S-4--FADD-csv-line-9 = always {A & !B & !CI} |-> {S === 1'b1};
psl property FADD-CO-4--FADD-csv-line-9 = always {A & !B & !CI} |-> {CO === 1'b0
};
psl property FADD-S-5--FADD-csv-line-10 = always {A & !B & CI} |-> {S === 1'b0};
psl property FADD-CO-5--FADD-csv-line-10 = always {A & !B & CI} |-> {CO === 1'b1
```

```
};
psl property FADD-S-6--FADD-csv-line-11 = always {A & B & !CI} |-> {S === 1'b0};
psl property FADD-CO-6--FADD-csv-line-11 = always {A & B & !CI} |-> {CO === 1'b1
};
psl property FADD-S-7--FADD-csv-line-12 = always {A & B & CI} |-> {S === 1'b1};
psl property FADD-CO-7--FADD-csv-line-12 = always {A & B & CI} |-> {CO === 1'b1}
;
```

【００８１】

図１０において、本発明に係わる他の実施例を示す。この例では仕様書に添付すべきシーケンスを表データ１００１として格納しており、構文解析器１００２によって、表形式で定義されたシーケンスをシステムメモリ上に展開し、シーケンス抽出器１００３によって、検証すべき処理のシーケンスを抽出し、プロパティ変換器１００４によって、アサーション記述１００５へ変換するようにしている。

【００８２】

表形式による処理のシーケンスの例を図１５に示す。この例は図７と同じプロパティを示している。この例もＥｘｃｅｌ（登録商標）で作成されている。構文解析器１００２やシーケンス抽出器１００３は、セル内に記述されたシーケンスを時系列に分解し、プロパティ変換器１００４において、ＰＳＬのSERE拡張正規表現でアサーション記述を生成するようにしている。

【００８３】

シーケンスの時系列への分解は、文字列内の「；」をクロックの1サイクル間の振る舞いとして解釈する。また、図１５に示す「0[*2:5]」はＰＳＬの繰り返し表現を用いており、Low期間が２～５サイクル間だけ継続することを意味している。また、「ack」は「0[*2*5];1;0」と記されているので、「ack」はLow期間が２～５サイクル間だけ継続し、その後、High,Lowと続く振る舞いであることを示している。

【００８４】

以下に、図１５を元に生成されたＰＳＬのアサーション記述を示す。

【００８５】

```
psl property reqack-ack-0--REQ-csv-line-5 =
    always {{rose)} |-> {{ack === 1'b0}[*2:5];{ack === 1'b1};{ack === 1'b0}};
```

【００８６】

尚、図５と図６および図１０に示された各処理フローを、図１におけるＣＰＵ１０２が実行するためのプログラムは、実行可能な形式で磁気メディア等に記録され、図１の記憶装置１０１に格納される。

【００８７】

以上、図１～図１５を用いて説明したように、本例のアサーション生成システム２０７は、半導体集積回路のアサーション検証に用いるアサーション記述を生成するものであって、グラフィカルエディタ（仕様入力手段）２０１により、ユーザ操作に基づき半導体集積回路の仕様（有限状態機械、処理シーケンス）を、状態遷移表や状態遷移図、あるいは、タイミングチャートや時系列図形で、グラフィカルに編集して当該半導体集積回路の設計データを生成し、グラフ構造に展開して仕様書電子データ２０２とし、記憶装置に記憶し、構文解析器２０３およびプロパティ抽出器２０４（プロパティ生成手段）により、仕様書電子データ（設計データ）を記憶装置から読み出し、この設計データを元に、半導体集積回路の仕様に関して検証すべきプロパティを生成し、そして、アサーション生成器（アサーション生成手段）２０５により、当該プロパティをアサーション記述言語２０６に変換する。

【００８８】

尚、グラフィカルエディタ（仕様入力手段）２０１では、ユーザ操作に基づき半導体集積回路の仕様を論理テーブルもしくは状態テーブルで編集して、当該半導体集積回路の設計データを生成することでも良い。そして、アサーション生成器２０５は、グラフィカル

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エディタ（仕様入力手段）２０１で編集した論理テーブルもしくは状態テーブルのテーブル名あるいはテーブルの行番号、または、当該論理テーブルもしくは状態テーブルにおける信号名あるいは状態名で構成されたアサーション名を付加されたアサーション記述に変換する。

【００８９】

また、本例の回路検証システムは、このようなアサーション生成システム２０７を具備し、このアサーション生成システムで生成したアサーション記述を用いて半導体集積回路のアサーション検証を行う。

【００９０】

このように、本例では、仕様書に添付する状態遷移図の電子データから、検証すべきプロパティのアサーション記述を自動的に生成するようにしたので、回路仕様とアサーションとの整合性が一致する。そのためアサーションのデバッグに費やす作業が削除できる。また生成されたアサーションは状態遷移の経路を網羅的に探索されて生成された機能カバレッジ・ポイントであるので、検証の後、どの経路がテストされていないかを機能カバレッジ・レポートからフィードバックでき、コーナー・ケースのテスト漏れを防ぐことが出来る。

【００９１】

また、仕様書に添付するタイミングチャートや信号の選択条件、または処理のシーケンスを注釈もしくは定義した図形もしくは表形式の電子データから、検証すべきプロパティのアサーション記述を自動的に生成するようにしたので、回路仕様とアサーションとの整合性が一致する。そのためアサーションのデバッグに費やす作業が削除できる。また仕様書に添付するタイミングチャートや信号の選択条件、または処理のシーケンスというのは検証時に必ずテストされなければならないほど重要なアサーションであることが多いが、本例で生成されるアサーションは重要プロパティであり、仕様書や回路機能を熟知しない設計者がキー・プロパティを使って検証作業を行うことができ、最終的に検証漏れによるシステムの改版率を低減させることができる。

【００９２】

尚、本発明は、図１～図１５を用いて説明した例に限定されるものではなく、その要旨を逸脱しない範囲において種々変更可能である。例えば、本例では、プロパティ抽出器２０４やアサーション生成器２０５等を構成するプログラムは、ＣＤ－ＲＯＭ（Compact Disc-Read Only Memory）やＤＶＤ（Digital Video Disc/Digital Versatile Disc）あるいはＦＤ（Flexible Disk）等の記録媒体から記憶装置１０１にインストールする構成としているが、このようなプログラムのインストールに関しては、通信装置を介してネットワーク経由でプログラムをダウンロードしてインストールすることでも良い。

【００９３】

また、本例では、ＰＳＬでのアサーション記述を例に説明したが、他のアサーション記述にも適用可能である。

【図面の簡単な説明】

【００９４】

【図１】本発明に係わるアサーション生成システムおよび回路検証システムを構成するハードウェアの構成例を示すブロック図である。

【図２】本発明に係わるアサーション生成システムの第１の機能構成例およびそれを用いた回路検証システムの構成例を示すブロック図である。

【図３】本発明に係わるアサーション生成システムで用いられるグラフ構造のメモリイメージ例を示す説明図である。

【図４】本発明に係わるアサーション生成システムで用いられる状態遷移図とそのグラフ構造例を示す説明図である。

【図５】本発明に係わるアサーション生成システムの第２の機能構成例を示すブロック図である。

【図６】本発明に係わるアサーション生成システムの第３の機能構成例を示すブロッ

ク図である。

【図７】本発明に係わるアサーション生成システムで用いられるタイミングチャート例を示す説明図である。

【図８】本発明に係わるアサーション生成システムで用いられるタイミングチャート上で定義される信号に関する情報および当該信号に対するタイミング制約に関する情報を格納するための構造体例を示す説明図である。

【図９】図７におけるタイミングチャートに関するプロパティ情報のメモリイメージ例を示す説明図である。

【図１０】本発明に係わるアサーション生成システムの第４の機能構成例を示すブロック図である。

【図１１】本発明に係わるアサーション生成システムで用いられるフルアダーの論理テーブルの構成例を示す説明図である。

【図１２】表（テーブル）におけるセルをメモリ上に展開するときの１個のセルを表すための構造体例を示す説明図である。

【図１３】図１２におけるセルを表す構造体を組み合わせてシートを構成したときのイメージ例を示す説明図である。

【図１４】図１１におけるフルアダーの論理テーブルを図１３のメモリ構造へ展開したときのイメージ例を示す説明図である。

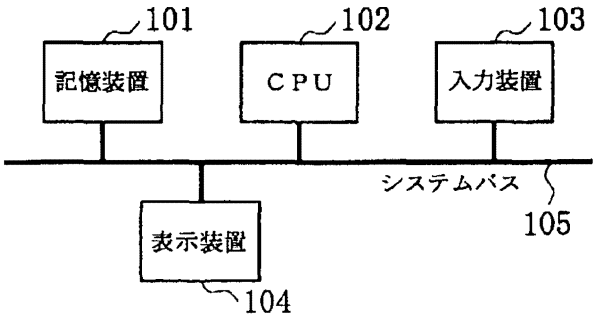
【図１５】本発明に係わるアサーション生成システムで用いられる処理シーケンスの表形式での構造例を示す説明図である。

【符号の説明】

【００９５】

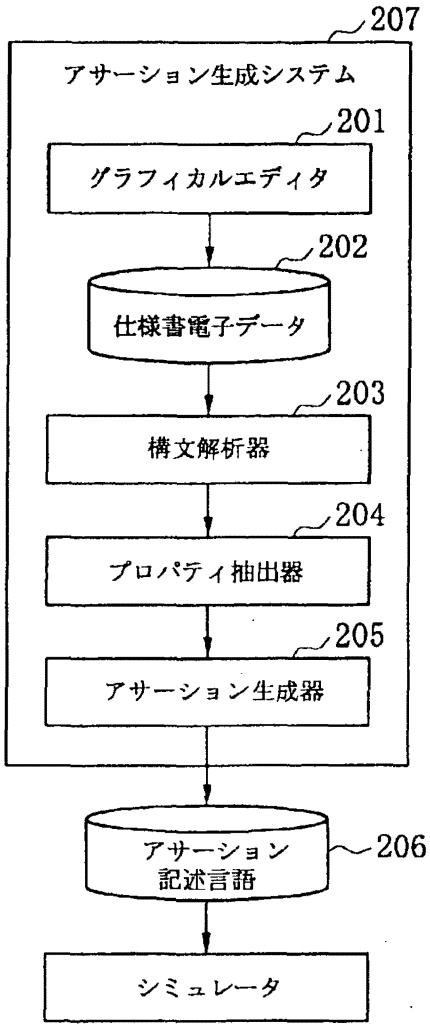
１０１：記憶装置、１０２：ＣＰＵ、１０３：入力装置、１０４：表示装置、１０５：システムバス、２０１：グラフィカルエディタ、２０２：電子データ、２０３：構文解析器、２０４：プロパティ抽出器、２０５：アサーション生成器、２０６：アサーション記述言語、３０１：構造体（アークの集合へのポインタ）、３０２：構造体（Ｎｅｘｔアーク・ポインタ）、５０１：グラフィカル情報、５０２：グラフ探索エンジン、５０３：経路データベース（ＤＢ）、５０４：プロパティ変換器、５０５：アサーション記述言語、６０１：タイミングチャート電子データ、６０２：タイミングチャート読み取り器、６０３：タイミング・プロパティ抽出器、６０４：タイミングチャートデータベース（ＤＢ）、６０５：プロパティ変換器、６０６：アサーション記述言語、８０１：構造体（関連信号へのポインタ）、８０２：構造体（Ｎｅｘｔ制約ポインタ）、１００１：表データ、１００２：構文解析器、１００３：シーケンス抽出器、１００４：プロパティ変換器、１００５：アサーション記述言語、１３０１：ポインタ（シートを示す）、１３０２：ポインタ（セル）。

【書類名】図面
【図１】

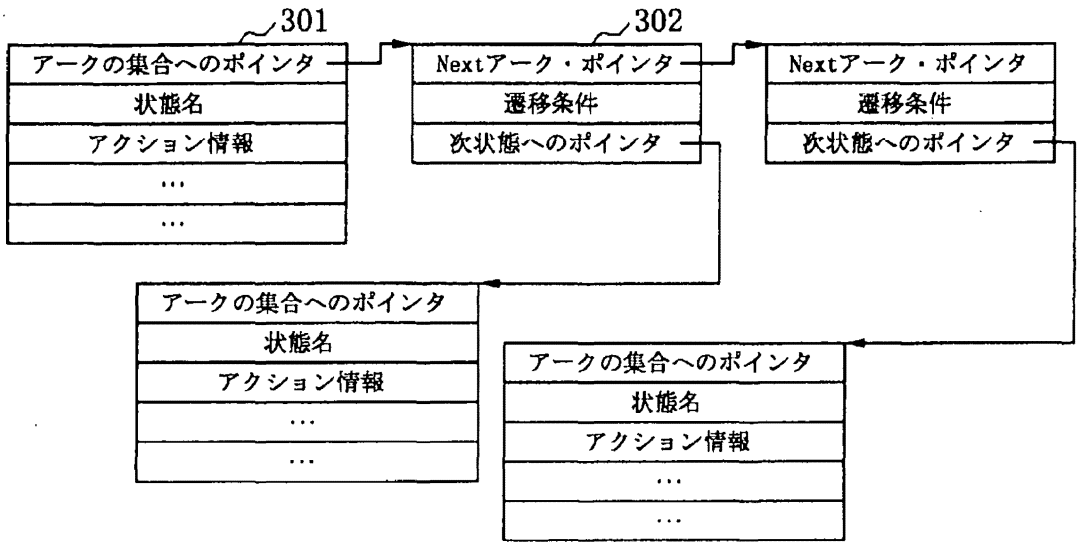


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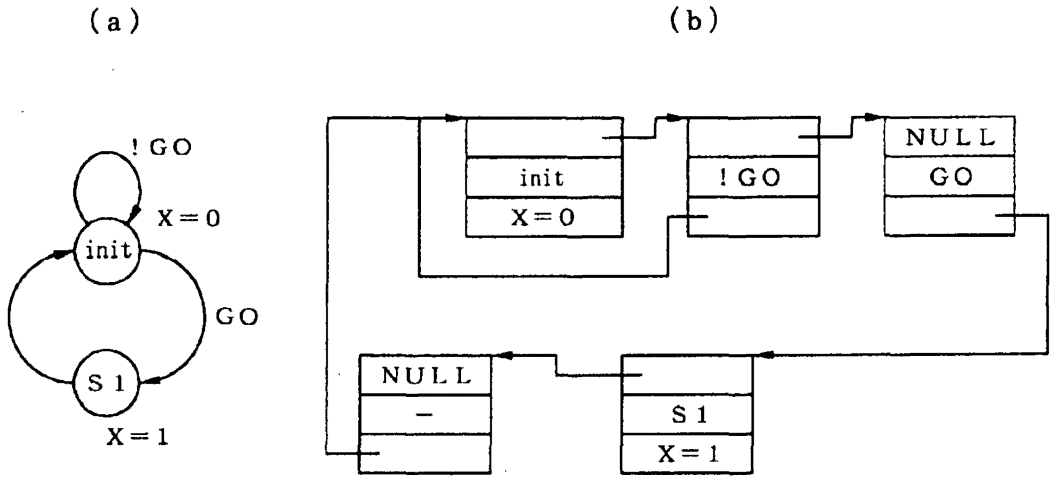
【図２】


207
アサーション生成システム
201
グラフィカルエディタ
202
仕様書電子データ
203
構文解析器
204
プロパティ抽出器
205
アサーション生成器
アサーション
記述言語
206
シミュレータ

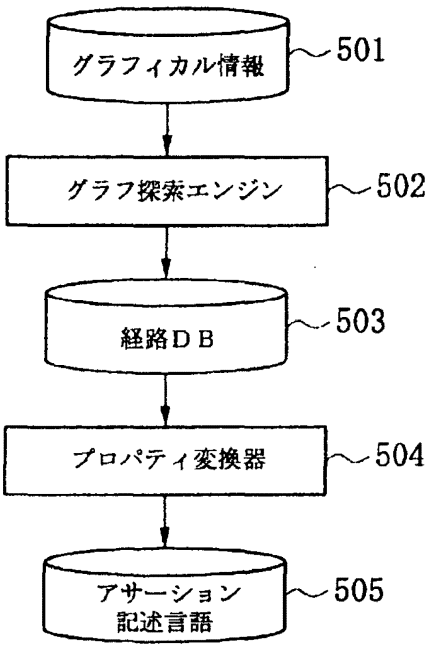
【図３】


301
302
アークの集合へのポインタ
状態名
アクション情報
…
…
Nextアーク・ポインタ
遷移条件
次状態へのポインタ
Nextアーク・ポインタ
遷移条件
次状態へのポインタ
アークの集合へのポインタ
状態名
アクション情報
…
…
アークの集合へのポインタ
状態名
アクション情報
…
…

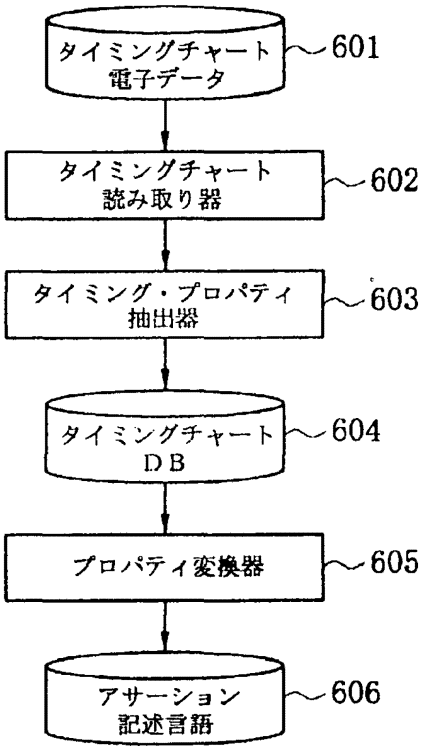
【図４】


(a)
(b)
! GO
X＝0
init
GO
S 1
X＝1
init
X＝0
! GO
NULL
GO
NULL
–
S 1
X＝1

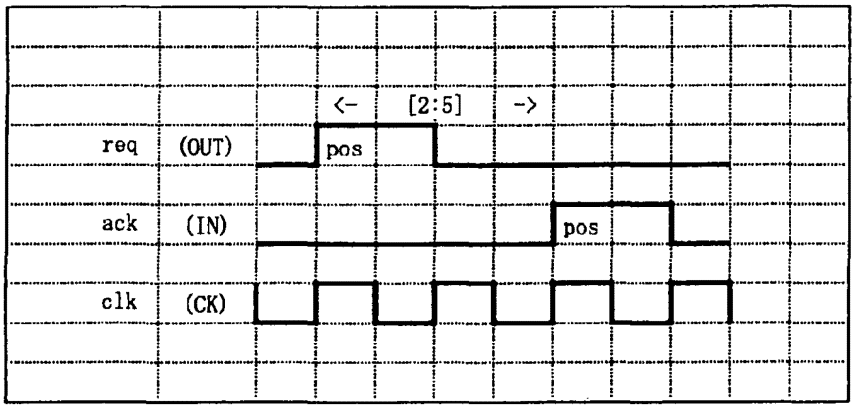
【図５】


グラフィカル情報
501
グラフ探索エンジン
502
経路ＤＢ
503
プロパティ変換器
504
アサーション
記述言語
505

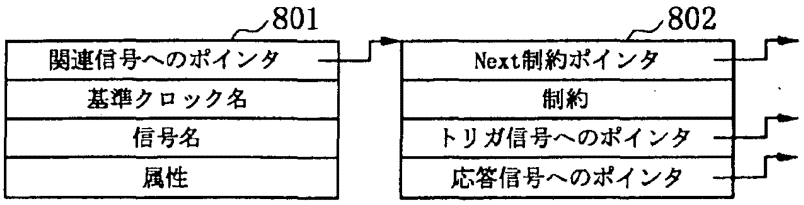
【図６】


タイミングチャート
電子データ
601
タイミングチャート
読み取り器
602
タイミング・プロパティ
抽出器
603
タイミングチャート
DB
604
プロパティ変換器
605
アサーション
記述言語
606

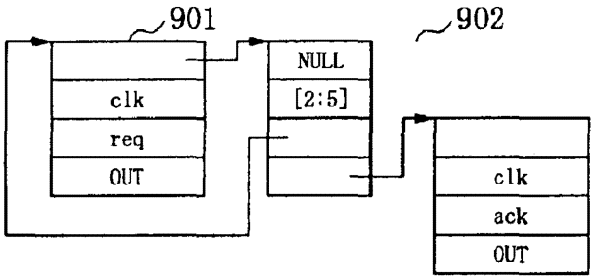
【図７】


<-
[2:5]
->
req
(OUT)
pos
ack
(IN)
pos
clk
(CK)

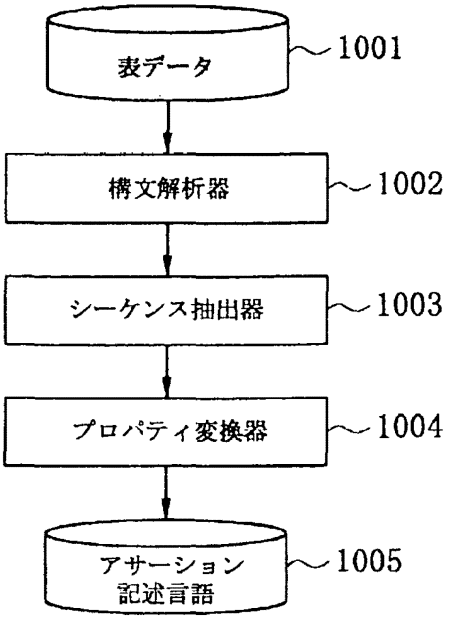
【図８】


801
802
関連信号へのポインタ
基準クロック名
信号名
属性
Next制約ポインタ
制約
トリガ信号へのポインタ
応答信号へのポインタ

【図９】


901
902
clk
req
OUT
NULL
[2:5]
clk
ack
OUT

【図１０】



【図１１】

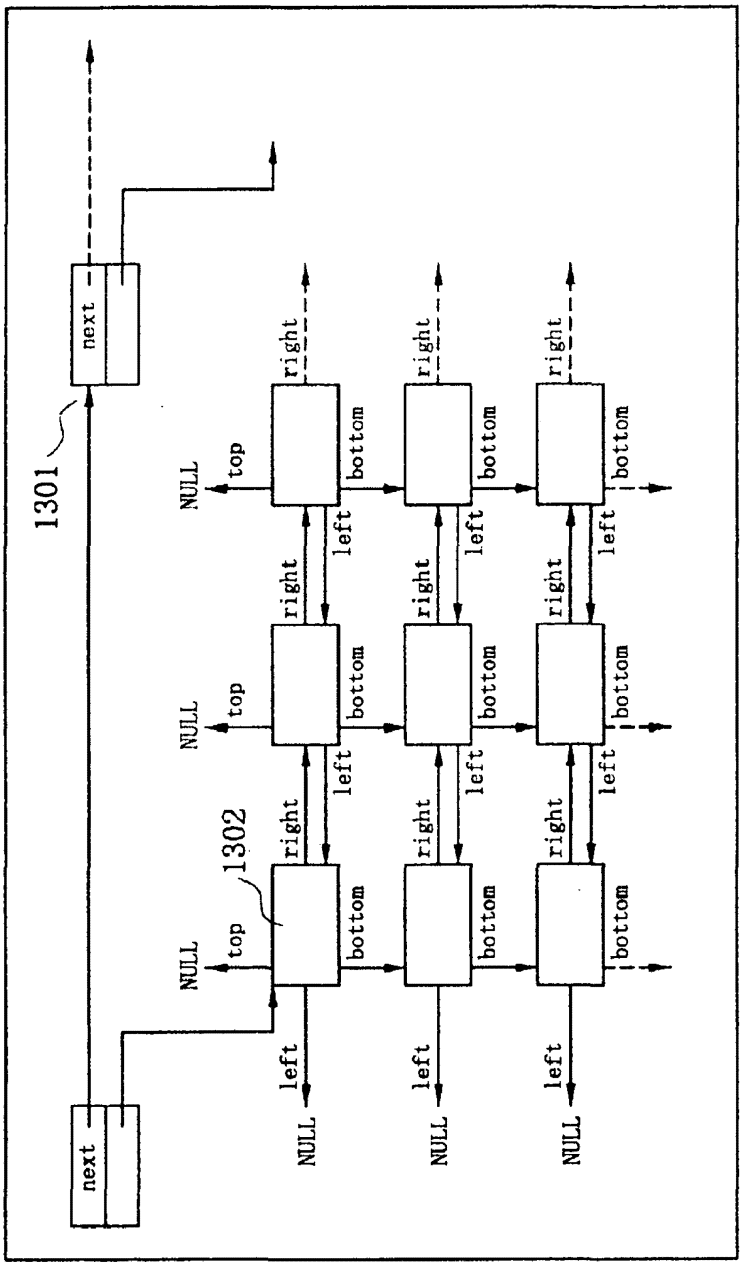
NAME	FADD			
CLOCK	posedge clk			
CONDITION	CONDITION	CONDITION	EXPECT	EXPECT
A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

【図１２】

```
typedef struct piece {
    struct piece        *left, *right, *top, *bottom
    char*               str;

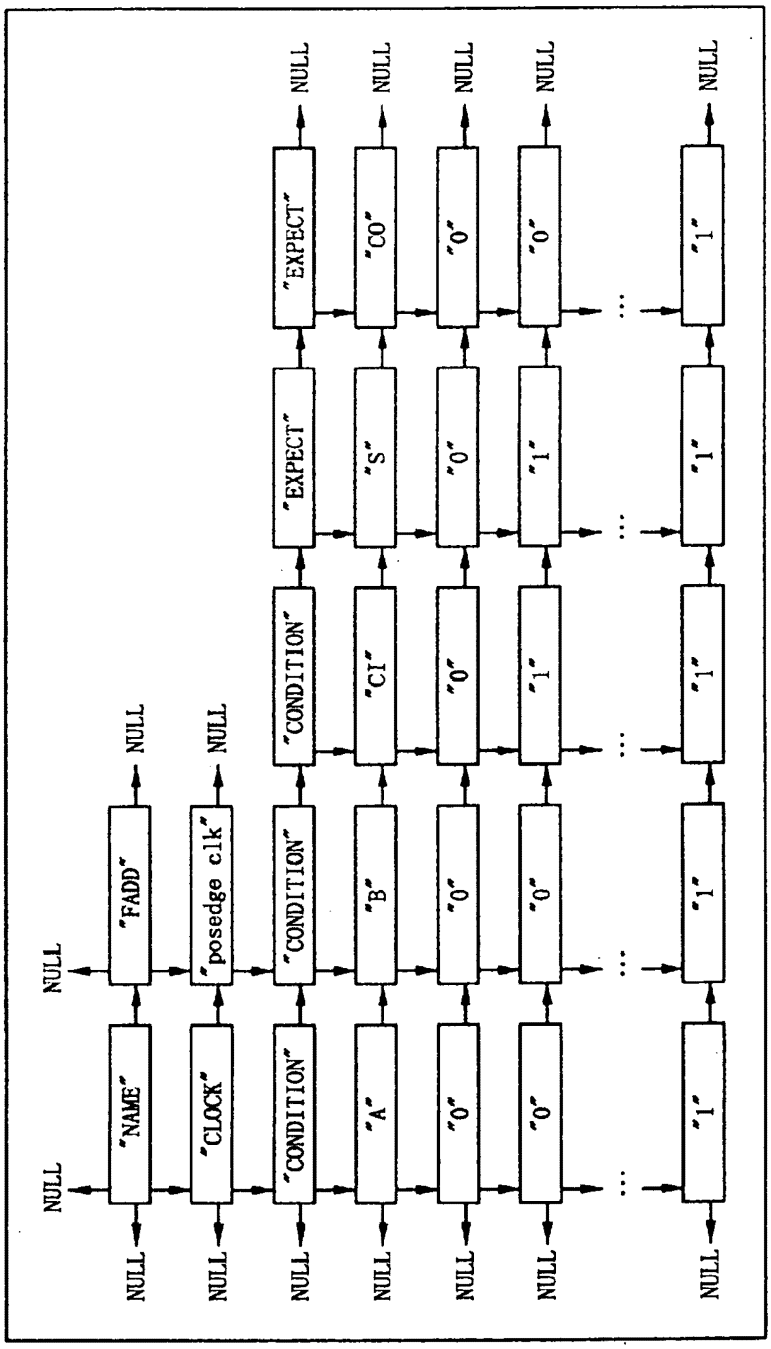
} Piece ;
```

【図１３】



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【図１４】


NULL
"NAME"
"CLOCK"
"CONDITION"
"A"
"0"
"0"
"1"
NULL
NULL
"FADD"
"posedge clk"
"CONDITION"
"B"
"0"
"0"
"1"
NULL
NULL
"CONDITION"
"CI"
"0"
"1"
"1"
NULL
NULL
"EXPECT"
"S"
"0"
"1"
"1"
NULL
NULL
"EXPECT"
"CO"
"0"
"0"
"1"
NULL

【図１５】

NAME	reqack
CLOCK	posedge clk
CONDITION	EXPECT
req	ack
rose	0[*2:5];1;0

【書類名】要約書
【要約】
【課題】　従来の技術では、回路仕様とアサーション記述との整合性一致は保証されないとの課題を解決し、例えばＬＳＩ等に対するアサーション検証の高信頼化および高効率化を可能とする。
【課題を解決するための手段】
【解決手段】　本例のアサーション生成システム２０７は、グラフィカルエディタ（仕様入力手段）２０１により、ユーザ操作に基づき半導体集積回路の仕様（有限状態機械、処理シーケンス）を、状態遷移表や状態遷移図あるいはタイミングチャートや時系列図形で、グラフィカルに編集して当該半導体集積回路の設計データ（仕様書電子データ２０２）を生成し、構文解析器２０３およびプロパティ抽出器２０４からなるプロパティ生成手段により、設計データを元に、半導体集積回路の仕様に関して検証すべきプロパティを生成し、アサーション生成器２０５により、当該プロパティをアサーション記述言語２０６に変換する。
【選択図】　図２

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出願人履歴

０００００６７４７
20020517
住所変更

東京都大田区中馬込１丁目３番６号
株式会社リコー

PATENT APPLICATION FEE DETERMINATION RECORD

Effective December 8, 2004

Application or Docket Number: 10/579766

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)	SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
			RATE	FEE		RATE	FEE
U.S. NATIONAL STAGE FEES							
BASIC FEE	SMALL ENT. = $ 150	LARGE ENT. = $ 300	BASIC FEE		OR	BASIC FEE	300
EXAMINATION FEE	Satisfies PCT Article 33(1)-(4) = $ 50 / $ 100	All other situations = $ 100 / $ 200	EXAM. FEE			EXAM. FEE	200
SEARCH FEE	U.S. is ISA = $ 50 / $ 100 ALL other countries = $ 200 / $ 400	ALL other situations = $ 250 / $ 500	SEARCH FEE			SEARCH FEE	400
FEE FOR EXTRA SPEC. PGS.	minus 100 =	/ 50 =	X $ 125 =			X $ 250 =	
TOTAL CHARGEABLE CLAIMS	15 minus 20 =	*	X $ 25 =		OR	X $ 50 =	
INDEPENDENT CLAIMS	3 minus 3 =	*	X $ 100 =		OR	X $ 200 =	
MULTIPLE DEPENDENT CLAIM PRESENT ☐			+ $ 180 =		OR	+ $ 360 =	
			TOTAL		OR	TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
AMENDMENT A	Total	*	Minus	**	=	X $ 25 =		OR	X $ 50 =	
	Independent	*	Minus	***	=	X $ 100 =		OR	X $ 200 =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐					+ $ 180 =		OR	+ $ 360 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE	ADDITIONAL FEE	OR	RATE	ADDITIONAL FEE
AMENDMENT B	Total	*	Minus	**	=	X $ 25 =		OR	X $ 50 =	
	Independent	*	Minus	***	=	X $ 100 =		OR	X $ 200 =	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐					+ $ 180 =		OR	+ $ 360 =	
						TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '20', enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than '3', enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET (FOR USE WITH FORM PTO-875)	SERIAL NO. 10/579766	FILING DATE
	APPLICANT(S)	

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
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TOTAL IND.	3					
TOTAL DEP.	12					
TOTAL CLAIMS	15					

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
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PTO - 1360 (REV. 11/04)

U.S. DEPARTMENT of COMMERCE
Patent and Trademark Office

DO/ EO WORKSHEET

Fred Smith, Patent Application Specialist/ National Stage Division

U.S. Appl. No. 10/579766 International Appl. No. PCT/JP2005/017921

Application filed by : ☐ 20 months ☑ 30 months

WIPO PUBLICATION INFORMATION :

Publication No.: WO2006/035854 Publication Language : ☐ English ☐ German ☐ Japanese ☐ Chinese ☐ Korean ☐ French ☐ Spanish ☐ Russian ☐ Other : _____

Publication Date : 6 Apr 2006 Not Published : ☐ U.S. only designated ☐ EP request Published : ☑ EP request

INTERNATIONAL APPLICATION PAPERS IN THE APPLICATION FILE :

- ☑ International Application *(RECORD COPY)*
- ☐ Article 19 Amendments
- ☐ PCT/IPEA/409 IPER : ☐ EP ☐ JP ☐ SE ☐ AU ☐ US ☐ FR ☐ CN ☐ ES ☐ RU ☐ AT ☐ KR ☐ ___
- ☐ Annexes to 409
- ☑ PCT/ISA/237 : ☐ EP ☑ JP ☐ SE ☐ AU ☐ US ☐ FR ☐ CN ☐ ES ☐ RU ☐ AT ☐ KR ☐ ___
  - ☐ PCT/IPEA/409 or PCT/ISA/237 was NOT AVAILABLE at the time of paralegal review
- ☐ PCT/IB/306
- ☐ Request form PCT/RO/101
- ☑ PCT/ISA/210 - Search Report : ☐ EP ☑ JP ☐ SE ☐ AU ☐ US ☐ FR ☐ CN ☐ ES ☐ RU ☐ AT ☐ KR ☐ ___ ☐ NONE
- ☐ Search Report References
- ☑ Priority Document (s) No. 1
  - ☐ N/A
  - ☐ Priority Document was NOT AVAILABLE at the time of paralegal review
- ☐ Other : _____

RECEIPTS FROM THE APPLICANT *(other than checked above)* :

- ☐ Basic National Fee *(or authorization to charge)*
- ☑ Description 36 ☑ Claims 7 ☑ Abstract 1
- ☑ Drawing Figure(s) - (# of drwgs. 12)
- ☐ Translation of Article 19 Amendments ☐ entered ☐ not entered : ☐ not a page for page substitution ☐ replaced by Article 34 Amendment
- ☐ Annexes to 409 ☐ entered ☐ not entered : ☐ not a page for page substitution ☐ no translation ☐ other : _____
- ☐ Application Data Sheet
- ☐ Power of Attorney
- ☐ Change of Address
- ☐ Preliminary Amendment(s) Filed on : 1. ☐ same as 371 request date 2. _____ 3. _____
- ☑ Information Disclosure Statement(s) Filed on : 1. ☑ same as 371 request date 2. _____ 3. _____
- ☐ Assignment Document (forwarded to Assignment Branch)
- ☐ Assignee Statement Under 37 CFR 3.73(b)
- ☐ Assignee PG Publication Notice
- ☐ Substitute Specification Filed on : 1. ☐ same as 371 request date 2. _____ 3. _____
- ☐ Verified Small Status Statement
- ☑ Oath/ Declaration (executed)
- ☐ Oath/ Declaration ☐ unsigned ☐ no citizenship ☐ other
- ☐ DNA Diskette ☐ Sequence Listing
- ☐ Other : _____

NOTES : ☐ I.A. used as Specification ☐ Other :

35 U.S.C. 371 - Receipt of Request (PTO-1390)	mo. 5 / day 18 / yr. 2006
Date Acceptable Oath/ Declaration Received	☑ Same as 371 Req. Date; ☐ mo. / day / yr. 200
Date of Completion of requirements under 35 U.S.C. 371	☑ Same as 371 Req. Date; ☐ Same as OATH Date; ☐ mo. / day / yr. 200
Date of Completion of DO/ EO 903 - Notification of Acceptance	
Date of Completion of DO/ EO 905 - Notification of Missing Requirements	
Date of Completion of DO/ EO 909 - Notification of Abandonment	
Date of Completion of DO/ EO 916 - Notification of Defective Response	
Date of Completion of DO/ EO 922 - Notification to Comply w/ Requirements for Patent Applications Containing Nucleotide and/or Amino Acid Sequence Disclosures	

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PATENT & TRADEMARK OFFICE

ITW

Docket No.: R2184.0495/P495
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Takamitsu Yamada

Application No.: 10/579,766 — Confirmation No.: 3580

Filed: May 18, 2006 — Art Unit: Not Yet Assigned

For: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD — Examiner: Not Yet Assigned

STATUS INQUIRY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

It is respectfully requested that the attorney named below be advised of the status of the above-identified application. Please advise us of when we might expect to receive an Office Action from the Patent and Trademark Office.

Dated: November 26, 2007

Respectfully submitted,

By _____
Mark J. Thronson
Registration No.: 33,082
Ranga Sourirajan
Registration No.: 60,109
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicant

DSMDB-2356029

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
10/579,766	05/18/2006	2827	900	R2184.0495/P495	15	3

CONFIRMATION NO. 3580

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

FILING RECEIPT

OC000000027817979

Date Mailed: 01/22/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Takamitsu Yamada, Kanagawa, JAPAN;

Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP05/17921 09/21/2005

Foreign Applications

JAPAN 2004-286042 09/30/2004

If Required, Foreign Filing License Granted: 01/18/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 10/579,766**

Projected Publication Date: 05/01/2008

Non-Publication Request: No

Early Publication Request: No

Cadence Design Systems, Inc. - Ex. 1002, Page 00153

SDT00000197

Title

Assertion Generating System, Program Thereof, Circuit Verifying System, and Assertion Generating Method

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

Cadence Design Systems, Inc. - Ex. 1002, Page 00154

SDT00000198

the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Cadence Design Systems, Inc. - Ex. 1002, Page 00155

SDT00000199

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
10/579,766	Takamitsu Yamada	R2184.0495/P495

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

INTERNATIONAL APPLICATION NO.	
PCT/JP05/17921	
I.A. FILING DATE	PRIORITY DATE
09/21/2005	09/30/2004

CONFIRMATION NO. 3580
371 ACCEPTANCE LETTER

OC000000027817980

Date Mailed: 01/22/2008

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

05/18/2006	05/18/2006
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and (c)(4) REQUIREMENTS	DATE OF COMPLETION OF ALL 35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** *The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363).* Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Copy of the International Application filed on 05/18/2006
- Copy of the International Search Report filed on 05/18/2006
- Information Disclosure Statements filed on 05/18/2006
- Oath or Declaration filed on 05/18/2006
- Request for Immediate Examination filed on 05/18/2006
- U.S. Basic National Fees filed on 05/18/2006
- Priority Documents filed on 05/18/2006
- Specification filed on 05/18/2006
- Claims filed on 05/18/2006
- Abstracts filed on 05/18/2006
- Drawings filed on 05/18/2006

FORM PCT/DO/EO/903 (371 Acceptance Notice)

Cadence Design Systems, Inc. - Ex. 1002, Page 00156

SDT00000200

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

FREDERICK SMITH

Telephone: (703) 308-9140 EXT 210

FORM PCT/DO/EO/903 (371 Acceptance Notice)

Cadence Design Systems, Inc. - Ex. 1002, Page 00157

SDT00000201

Docket No.: R2184.0495/P495
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Takamitsu Yamada

Application No.: 10/579,766 | Confirmation No.: 3580

Filed: May 18, 2006 | Art Unit: 2827

For: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD | Examiner: Not Yet Assigned

REQUEST FOR CORRECTED FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant hereby requests that a corrected Filing Receipt be issued in the above-identified patent application. The official Filing Receipt received by Applicant, a copy of which is attached hereto, has an error in the number of independent claims. The current filing receipt incorrectly indicates that 3 independent claims were submitted. The correct number of claims should be listed as **2**.

Applicant additionally requests that all pertinent U.S. Patent and Trademark Office records relating to the subject application be changed to reflect this correction.

Cadence Design Systems, Inc. - Ex. 1002, Page 00158

SDT00000202

Dated: February 6, 2008

Respectfully submitted,

By _____

Mark J. Thronson
Registration No.: 33,082
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
10/579,766	05/18/2006	2827	900	R2184.0495/P495	15	3

CONFIRMATION NO. 3580

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

RECEIVED
JAN 23 2008
MJT/RS/FORM-DC
BY: 01/24/08

FILING RECEIPT

OC000000027817979

Date Mailed: 01/22/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Takamitsu Yamada, Kanagawa, JAPAN;

Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP05/17921 09/21/2005

Foreign Applications

JAPAN 2004-286042 09/30/2004

If Required, Foreign Filing License Granted: 01/18/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 10/579,766**

Projected Publication Date: 05/01/2008

Non-Publication Request: No

Early Publication Request: No

PREVIOUSLY DOCKETED

Title

Assertion Generating System, Program Thereof, Circuit Verifying System, and Assertion Generating Method

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

Cadence Design Systems, Inc. - Ex. 1002, Page 00161

SDT00000205

the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Cadence Design Systems, Inc. - Ex. 1002, Page 00162

SDT00000206

Electronic Acknowledgement Receipt

EFS ID:	2823064
Application Number:	10579766
International Application Number:	
Confirmation Number:	3580
Title of Invention:	Assertion Generating System, Program Thereof, Circuit Verifying System, and Assertion Generating Method
First Named Inventor/Applicant Name:	Takamitsu Yamada
Customer Number:	24998
Filer:	Mark J. Thronson/Jamie Alfaro
Filer Authorized By:	Mark J. Thronson
Attorney Docket Number:	R2184.0495/P495
Receipt Date:	06-FEB-2008
Filing Date:	18-MAY-2006
Time Stamp:	16:16:17
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	req.pdf	283443 931a7ec239c20219867fda2568436629c5a2cef6	no	5

Warnings:	
Information:	

Total Files Size (in bytes):	283443

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/579,766	05/18/2006	Takamitsu Yamada	R2184.0495/P495

CONFIRMATION NO. 3580

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC20006-5403

Title: Assertion Generating System, Program Thereof, Circuit Verifying System, and Assertion Generating Method

Publication No. US-2008-0104556-A1
Publication Date: 05/01/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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Pre-Grant Publication Division, 703-605-4283

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
10/579,766	05/18/2006	2825	900	R2184.0495/P495	15	2

CONFIRMATION NO. 3580

CORRECTED FILING RECEIPT

24998
DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

OC000000030080180

Date Mailed: 05/22/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Takamitsu Yamada, Kanagawa, JAPAN;

Power of Attorney: The patent practitioners associated with Customer Number 24998

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/JP05/17921 09/21/2005

Foreign Applications

JAPAN 2004-286042 09/30/2004

If Required, Foreign Filing License Granted: 01/18/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 10/579,766**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Cadence Design Systems, Inc. - Ex. 1002, Page 00166

SDT00000210

Title

Assertion Generating System, Program Thereof, Circuit Verifying System, and Assertion Generating Method

Preliminary Class

716

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Cadence Design Systems, Inc. - Ex. 1002, Page 00167

SDT00000211

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NOT GRANTED

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Cadence Design Systems, Inc. - Ex. 1002, Page 00168

SDT00000212

OIPE
MAY 27 2008
PATENT & TRADEMARK OFFICE
IAP58

Docket No.: R2184.0495/P495
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Takamitsu Yamada

Application No.: 10/579,766 Confirmation No.: 3580

Filed: May 18, 2006 Art Unit: 2827

For: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned (37 CFR 1.97(b)(3)).

Copies of European Search Report for EP-05-788142 and references cited therein are enclosed.

Cadence Design Systems, Inc. - Ex. 1002, Page 00169

SDT00000213

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. R2184.0495/P495.

Dated: May 27, 2008

Respectfully submitted,

By _____

Mark J. Thronson
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Used in Lieu of PTO/SB/08A/B
(Based on PTO 01-08 version)

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/579,766-Conf. #3580
Filing Date	May 18, 2006
First Named Inventor	Takamitsu Yamada
Art Unit	2827
Examiner Name	Not Yet Assigned
Attorney Docket Number	R2184.0495/P495

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	TASIRAN et al.; "Linking Simulation with Formal Verification at a Higher Level"; Synergies for Design Verification; IEEE Design & Test of Computers; Vol. 21, No. 6; Jun 2004; pp. 472-482.	
	CB	CHEN et al.; "Logic of Constraints: A Quantitative Performance and Functional Constraint Formalism"; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Vol. 23, No. 8; August 2004; pp. 1243-1255.	
	CC	DATTA et al.; "Assertion Based Verification Using HDVL"; Proceedings of the 17th International Conference on VLSI Design; Jan. 2004; pp. 319-325.	
	CD	PIXLEY et al.; "Functional Verification 2003: Technology, Tools and Methodology"; Proceedings 5th International Conference, IEEE; Vol. 1; Oct. 2003; pp. 1-5.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,766	05/18/2006	Takamitsu Yamada	R2184.0495/P495	3580

24998 7590 07/17/2008

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
SIEK, VUTHE	
ART UNIT	PAPER NUMBER
2825	
MAIL DATE	DELIVERY MODE
07/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/579,766	YAMADA, TAKAMITSU	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/18/06;5/27/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/579,766 filed on 5/18/06. Claims 1-15 remain pending in the application.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1 and 9 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention lacks patentable utility. Claims 1 and 9 a data structure per see without patentable utility. Claim 7 is non-statutory subject matter because a program without storing in a physical storage device executed by a computer processor, and excluding all kind carrier waves is non-statutory subject matter.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-15 is rejected under 35 U.S.C. 102(e) as being anticipated by Hekmatpour et al. (7,313,772 B2).

6. As to claims 1 and 9, Hekmatpour et al. teach an assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit,

comprising: a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations (examples are a design; design constructs; designs blocks shown in Fig. 2; assertion schemas stored in a database shown in Fig. 1; Fig. 10); a first storing unit that stores the design data generated by the specification inputting unit (examples are a design; design constructs; designs blocks shown in Fig. 2; Fig. 1, 10); a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data (example are assertion schemas stored in a database shown in Fig. 1; 10); a second storing unit that stores the property generated by the property generating unit (example are assertion schemas stored in a database shown in Fig. 1; Fig. 4, 10 and its description); and an assertion generating unit that converts the property into an assertion description by reading the property generated by the property generating unit from the second storing unit (Fig. 1; assertion generator may embed the assertions in the design HDL or provide them in a separate design module), wherein the property

generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data (at least see col. 9 lines 6-41; Fig. 1, 5 and its description).

7. As to claims 2 and 10, Hekmatpour et al. teach, wherein the property generating unit generates at least one or more properties, and the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations (Fig. 10).

8. As to claims 3 and 11, Hekmatpour et al. teach, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property (Fig. 10, 11).

9. As to claims 4 and 12, Hekmatpour et al. teach, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property (Fig. 2, 10).

10. As to claims 5 and 13, Hekmatpour et al. teach, wherein the assertion generating unit converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or

a signal name or a state name in the logic table or the state table edited by the specification inputting unit is added, and the property is the temporal property (Fig. 2, 10).

11. As to claims 6 and 14, Hekmatpour et al. teach, wherein the specification inputting unit is a business tool of spread sheet software and expands the design data into a graphic structure and inputs the graphic structure in the first storing unit (Fig. 1 shows a database; Fig. 2 shows design data; Fig. 10 shows assertion generation system).

12. As to claim 7, Hekmatpour et al. teach a program that makes a computer function as the units of the assertion generating system as claimed in claim 1 (Fig. 3-9 show a program).

13. As to claim 8, Hekmatpour et al. teach a circuit verifying system, comprising: the assertion generating system as claimed in claim 1, wherein the circuit verifying system executes assertion verification of a semiconductor integrated circuit by using the assertion description generated by the assertion generating system (Fig. 1, 10 and 11 show assertion system).

14. As to claim 15, Hekmatpour et al. teach a manufacturing method of a semiconductor device, comprising: a designing step that designs an integrated circuit having a predetermined function ; a simulating step that simulates the integrated circuit by using the assertion generated at the assertion generating method as claimed in claim 9; and a manufacturing step that manufactures a semiconductor device based on specifications of the integrated circuit, wherein the semiconductor device in which

design meeting specifications is confirmed is manufactured by that the integrated circuit is simulated by the assertion obtained at the assertion generating method as claimed in claim 9 (see claim 1 and 9 rejection; the limitations are known to be inherently in the art).

15. Claims 1-15 is rejected under 35 U.S.C. 102(e) as being anticipated by Mitra et al. (7,325,209 B2).

16. As to claims 1 and 9, Mitra et al. teach an assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit (see abstract, summary, Fig. 1-4), comprising: a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations (HDL design; Fig. 4); a first storing unit that stores the design data generated by the specification inputting unit (Fig. 4); a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data (Fig. 4); a second storing unit that stores the property generated by the property generating unit (Fig. 4); and an assertion generating unit that converts the property into an assertion description by reading the property generated by the property generating unit from the second storing unit (Fig. 4; translator or transformer), wherein the property generated by the property generating

unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data (Fig. 2-4).

17. As to claims 2 and 10, Mitra et al. teach, wherein the property generating unit generates at least one or more properties, and the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations (Fig. 1, 4).

18. As to claims 3 and 11, Mitra et al. teach, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property (Fig. 2-4).

19. As to claims 4 and 12, Mitra et al. teach, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property (Fig. 1-4).

20. As to claims 5 and 13, Mitra et al. teach, wherein the assertion generating unit converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or

a signal name or a state name in the logic table or the state table edited by the specification inputting unit is added, and the property is the temporal property (Fig. 1-4).

21. As to claims 6 and 14, Mitra et al. teach, wherein the specification inputting unit is a business tool of spread sheet software (known art) and expands the design data into a graphic structure and inputs the graphic structure in the first storing unit (Fig. 1-4).

22. As to claim 7, Mitra et al. teach a program that makes a computer function as the units of the assertion generating system as claimed in claim 1 (Fig. 1-4).

23. As to claim 8, Mitra et al. teach a circuit verifying system, comprising: the assertion generating system as claimed in claim 1, wherein the circuit verifying system executes assertion verification of a semiconductor integrated circuit by using the assertion description generated by the assertion generating system (Fig. 1-4).

24. As to claim 15, Mitra et al. teach a manufacturing method of a semiconductor device, comprising: a designing step that designs an integrated circuit having a predetermined function ; a simulating step that simulates the integrated circuit by using the assertion generated at the assertion generating method as claimed in claim 9; and a manufacturing step that manufactures a semiconductor device based on specifications of the integrated circuit, wherein the semiconductor device in which design meeting specifications is confirmed is manufactured by that the integrated circuit is simulated by the assertion obtained at the assertion generating method as claimed in claim 9 (Fig. 1-4; the limitations are known to be inherently in the art).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, A.U. 2825

Notice of References Cited	Application/Control No. 10/579,766	Applicant(s)/Patent Under Reexamination YAMADA, TAKAMITSU	
	Examiner Vuthe Siek	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,313,772	12-2007	Hekmatpour et al.	716/5
*	B	US-7,194,713	03-2007	Iwashita, Hiroaki	716/5
*	C	US-7,076,753	07-2006	Cerny et al.	716/5
*	D	US-7,325,209	01-2008	Mitra et al.	716/5
	E	US-			
	F	US-			
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FOREIGN PATENT DOCUMENTS

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	N					
	O					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	536	assert$3 near4 description	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:06
S2	90459	graphical near5 representation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S3	72207	state near machine	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S4	3159118	property or timing near constraint	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S5	472053	simulat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S6	11	S1 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:08
S7	0	S3 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:08
S8	3196	S3 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:08
S9	1384	S8 and S4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:10

S10	699	S9 and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:10
S11	25614	assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:11
S12	67	S10 and S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:11
S13	4490	(716/4,18).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:23
S14	2	graphical with assertion near3 description	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:38
S15	5886	(716/4,5,18).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:39
S16	40	graphical with assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:39
S17	11	S5 and S16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:40
S18	356	property with assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:49
S19	25	S2 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:49

S20	599479	graphic$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:52
S21	156	S18 and S20	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:52
S22	32	S3 and S21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:53
S23	358	property with assertioN	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/24 17:08
S24	456	assertioN near4 language	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/24 17:08
S25	60	S23 and S24	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/24 17:08

6/24/08 6:22:42 PM
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OIPE IAP58 MAY 27 2008 PATENT & TRADEMARK OFFICE

Used in Lieu of PTO/SB/08A/B
(Based on PTO 01-08 version)

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/579,766-Conf. #3580
Filing Date	May 18, 2006
First Named Inventor	Takamitsu Yamada
Art Unit	2827
Examiner Name	Not Yet Assigned
Attorney Docket Number	R2184.0495/P495

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	TASIRAN et al.; "Linking Simulation with Formal Verification at a Higher Level"; Synergies for Design Verification; IEEE Design & Test of Computers; Vol. 21, No. 6; Jun 2004; pp. 472-482.	
	CB	CHEN et al.; "Logic of Constraints: A Quantitative Performance and Functional Constraint Formalism"; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Vol. 23, No. 8; August 2004; pp. 1243-1255.	
	CC	DATTA et al.; "Assertion Based Verification Using HDVL"; Proceedings of the 17th International Conference on VLSI Design; Jan. 2004; pp. 319-325.	
	CD	PIXLEY et al.; "Functional Verification 2003: Technology, Tools and Methodology"; Proceedings 5th International Conference, IEEE; Vol. 1; Oct. 2003; pp. 1-5.	

Examiner Signature	/Vuthe Siek/	Date Considered	06/24/2008

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

DSMDB-2445952v01

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /V.S./

EFS-Web Receipt date: 05/18/2006

10579766 GAU: 2825

10/579766

IAP12 Rec'd PCT/PTO 18 MAY 2006

PTO/SB/08a/b (07-05)
Approved for use through 07/31/2006. OMB 0651-0031
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Substitute for form 1449A/B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	NEW
Filing Date	May 17, 2006
First Named Inventor	Takamitsu Yamada
Art Unit	N/A
Examiner Name	Not Yet Assigned SIEK, V.
Attorney Docket Number	R2184.0495/P495

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	BA	JP-7-049887	02-21-1995			√
	BB	JP-2004-326650	11-18-2004			√
	BC	JP-2000-181933	06-30-2000			√
	BD	JP-2000-142918	05-23-2000			√

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	Property Specification Language Reference Manual Version 1.1, June 9, 2004	
	CB	TransEDA Announces Industry-First Property 1-15 Capture and Validation Product, [online], June 2, 2003, [retrieved on October 14, 2005], Retrieved from the Internet:<URL: http://www.transeda.com/news/view.php?id=54&s year=2003 > & <URL: http://www.transeda.com/news/languages/Japanese_54.doc >	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	/Vuthe Siek/	Date Considered	06/24/2008

DSMDB.2086999 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /V.S./

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United States Patent and Trademark Office
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www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 3580

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/579,766	05/18/2006	~~365~~ 716	2825	R2184.0495/P495

APPLICANTS
Takamitsu Yamada, Kanagawa, JAPAN;

**** CONTINUING DATA ***************************
This application is a 371 of PCT/JP05/17921 09/21/2005

**** FOREIGN APPLICATIONS ***************************
JAPAN 2004-286042 09/30/2004

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
01/18/2008

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /VUTHE SIEK/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		JAPAN	12	15	2

ADDRESS

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403
UNITED STATES

TITLE

Assertion Generating System, Program Thereof, Circuit Verifying System, and Assertion Generating Method

FILING FEE RECEIVED		
900	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10579766	YAMADA, TAKAMITSU
	Examiner	Art Unit
	Vuthe Siek	2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/24/2008								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
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	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10579766	YAMADA, TAKAMITSU
	Examiner	Art Unit
	Vuthe Siek	2825

SEARCHED

Class	Subclass	Date	Examiner
716	4,5,18	6/24/08	VA

SEARCH NOTES

Search Notes	Date	Examiner
EAST ALL DATABASES (SEE SEARCH REPORT PRINTOUT)	6/24/08	VS

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

AMENDMENT TRANSMITTAL LETTER

Docket No. R2184.0495/P495			
Application No. 10/579,766-Conf. #3580	Filing Date May 18, 2006	Examiner Vuthe Siek	Art Unit 2825

Applicant(s): Takamitsu Yamada

Invention: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an Amendment in the above-identified application.

The fee has been calculated and is being transmitted as shown below.

CLAIMS AS AMENDED

	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	14	- 20 =	0	x 52.00	0
Independent Claims	4	- 3 =	1	x 220.00	220.00
Multiple Dependent Claims (check if applicable) ☐				390.00	0
Other fee (please specify):					0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					220.00

☒ Large Entity ☐ Small Entity

☐ No additional fee is required for this Amendment.

☐ Please charge Deposit Account No. _____ in the amount of $ _____.

☐ A check in the amount of $ _____ to cover the filing fee is enclosed.

☒ Payment by credit card. Form PTO-2038 is attached.

☒ The Director is hereby authorized to charge and credit Deposit Account No. 04-1073 as described below.

☒ Credit any overpayment.

☒ Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Dated: October 17, 2008

Mark J. Thronson
Attorney/Agent Reg. No.: 33,082

DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-4742

Docket No.: R2184.0495/P495
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Takamitsu Yamada

Application No.: 10/579,766 | Confirmation No.: 3580

Filed: May 18, 2006 | Art Unit: 2825

For: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD | Examiner: Vuthe Siek

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated July 17, 2008, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

Cadence Design Systems, Inc. - Ex. 1002, Page 00192

SDT00000236

AMENDMENTS TO CLAIMS

1. (Original) An assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit, comprising:

a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations;

a first storing unit that stores the design data generated by the specification inputting unit;

a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;

a second storing unit that stores the property generated by the property generating unit; and

an assertion generating unit that converts the property into an assertion description by reading the property generated by the property generating unit from the second storing unit, wherein

the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

2. (Original) The assertion generating system as claimed in claim 1, wherein

the property generating unit generates at least one or more properties, and

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations.

3. (Original) The assertion generating system as claimed in claim 1, wherein the specification inputting unit includes a design data generating unit that generates the design data of

the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property.

4. (Original) The assertion generating system as claimed in claim 1, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property.

5. (Original) The assertion generating system as claimed in claim 4, wherein the assertion generating unit converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or a signal name or a state name in the logic table or the state table edited by the specification inputting unit is added, and the property is the temporal property.

6. (Original) The assertion generating system as claimed in claim 1, wherein the specification inputting unit is a business tool of spread sheet software and expands the design data into a graphic structure and inputs the graphic structure in the first storing unit.

7. (Canceled)

8. (Currently amended) A circuit verifying system, comprising:

an assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit, comprising:

a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations;

a first storing unit that stores the design data generated by the specification inputting unit;

a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;

a second storing unit that stores the property generated by the property generating unit; and

an assertion generating unit that converts the property into an assertion description by reading the property generated by the property generating unit from the second storing unit, wherein

the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data; and

~~the assertion generating system as claimed in claim 1,~~ wherein the circuit verifying system executes assertion verification of [[a]] the semiconductor integrated circuit by using the assertion description generated by the assertion generating system.

9. (Original) An assertion generating method that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit by a computer which has a program, comprising:

a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations and inputs the design data in storage;

a property generating step that reads the design data generated at the specification inputting step from the storage and generates a property which verifies the specification of the semiconductor integrated circuit using the read design data and inputs the property in the storage; and

an assertion generating step that reads the property generated at the property generating step from the storage and converts the property into an assertion description, wherein

the property generated by the property generating step is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

10. (Original) The assertion generating method as claimed in claim 9, wherein

the property generating step generates at least one or more properties, and

the specification inputting step generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations.

11. (Original) The assertion generating method as claimed in claim 9, wherein the specification inputting step generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property.

12. (Original) The assertion generating method as claimed in claim 9, wherein the specification inputting step generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property.

13. (Original) The assertion generating method as claimed in claim 12, wherein the assertion generating step converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or a signal name or a state name in the logic table or the state table edited at the specification inputting step is added, and the property is the temporal property.

14. (Original) The assertion generating method as claimed in claim 9, wherein the specification inputting step expands the design data into a graphic structure and inputs the graphic structure in the storage.

15. (Currently amended) A manufacturing method of a semiconductor device, comprising:

a designing step that designs an integrated circuit having a predetermined function;

a simulating step that simulates the integrated circuit by using [[the]] an assertion generated [[at the]] by an assertion generating method ~~as claimed in claim 9~~; and

a manufacturing step that manufactures a semiconductor device based on specifications of the integrated circuit, and

~~the semiconductor device in which design meeting specifications is confirmed is manufactured by the integrated circuit is simulated by the assertion obtained at the assertion generating method as claimed in claim 9~~ wherein the assertion generating method comprises:

a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations and inputs the design data in storage;

a property generating step that reads the design data generated at the specification inputting step from the storage and generates a property which verifies the specification of the semiconductor integrated circuit using the read design data and inputs the property in the storage; and

an assertion generating step that reads the property generated at the property generating step from the storage and converts the property into an assertion description, wherein

the property generated by the property generating step is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

REMARKS

Claim 7 has been canceled, without prejudice. Claims 8 and 15 have been rewritten in independent form, and claim 15 has been further amended. The application as amended contains claims 1-6 and 8-15 – four independent claims and a total of fourteen claims. Please charge any deficiency in the fees to Deposit Account No. 04-1073. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Claims 1 and 9 are rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. The Office Action contends that claims 1 and 9 are directed to a "data structure per se." Reconsideration is respectfully requested.

Claim 1 is directed to a system which has physical elements, including the recited first and second storing units. Claim 1 is directed to the system, not to a program. The claim is not directed to a "data structure per se."

Claim 9 is directed to a method that has positive steps. Claim 9 is not directed to a program; it is not directed to a "data structure per se," and the Office Action provides no explanation to the contrary. See M.P.E.P. § 2106.01(I).

Claims 1-6 and 8-15 are rejected under 35 U.S.C. § 102 as being anticipated by Hekmatpour. Reconsideration is respectfully requested. Hekmatpour's filing date is May 24, 2005. Claims 1-6 and 8-15 should be entitled to the September 30, 2004 filing date of the Japanese priority application. An accurate English-language translation of the priority document is being submitted concurrently herewith. September 30, 2004 is prior to May 24, 2005. Therefore, the rejection based on Hekmatpour should be withdrawn.

Claims 1-6 and 8-15 are rejected under 35 U.S.C. § 102 as being anticipated by Mitra. Reconsideration is respectfully requested. Mitra has an effective U.S. filing date of either

November 17, 2005 or November 17, 2004, depending on what was disclosed in the corresponding provisional application. As noted above, claims 1-6 and 8-15 should be entitled to the September 30, 2004 filing date of the Japanese priority application. September 30, 2004 is prior to November 17, 2004. Therefore, the rejection based on Mitra should be withdrawn.

Allowance of the application with claims 1-6 and 8-15, as amended, is solicited.

Dated: October 17, 2008

Respectfully submitted,

By _____

Mark J. Thronson
Registration No.: 33,082
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
202-420-4742
Attorneys for Applicant

2825

I, Tadahiko Itoh, a Patent Attorney of Tokyo, Japan having my office at 32nd Floor, Yebisu Garden Place Tower, 20-3 Ebisu 4-Chome, Shibuya-Ku, Tokyo 150-6032, Japan do solemnly and sincerely declare that I am the translator of the attached English language translation and certify that the attached English language translation is a correct, true and faithful translation of Japanese Patent Application No. 2004-286042 to the best of my knowledge and belief.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Tadahiko ITOH
Patent Attorney
ITOH International Patent Office
32nd Floor,
Yebisu Garden Place Tower,
20-3 Ebisu 4-Chome, Shibuya-Ku,
Tokyo 150-6032, Japan

(Document Name)	Application for Patent
(Reference Number)	200402839
(Date of Submission)	September 30, 2004
(Destination)	Commissioner of Patent Office
(IPC)	G 06F 17/30
(Inventor)	
(Residence or Address)	c/o RICOH COMPANY, LTD. 3-6, Nakamagome 1-chome, Ohta-ku, Tokyo, Japan
(Name)	Takamitsu Yamada
(Applicant for Patent)	
(Identification Number)	000006747
(Name)	RICOH COMPANY, LTD.
(Attorney)	
(Identification Number)	100102587
(Patent Attorney)	
(Name)	Masayuki Watanabe
(Appointed Attorney)	
(Identification Number)	100077274
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CLAIMS

1. An assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit, comprising:

a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations;

a first storing unit that stores the design data generated by the specification inputting unit;

a property generating unit that generates a property to be verified with respect to the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;

a second storing unit that stores the property generated by the property generating unit; and

an assertion generating unit that converts the property into an assertion description by reading the property generated by the property generating unit from

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the second storing unit.

2. The assertion generating system as claimed in claim 1, wherein

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations.

3. The assertion generating system as claimed in claim 1, wherein

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations.

4. The assertion generating system as claimed in any one of claims 1 through 3, wherein

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing

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the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations.

5. The assertion generating system as claimed in claim 4, wherein

the assertion generating unit converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or a signal name or a state name in the logic table or the state table edited by the specification inputting unit is added.

6. The assertion generating system as claimed in any one of claims 1 through 5, wherein

the specification inputting unit loads the design data into a graphic structure and inputs the graphic structure in the first storing unit.

7. A program that makes a computer function as the units of the assertion generating system as claimed in any one of claims 1 through 6.

8. A circuit verifying system, comprising:

the assertion generating system as claimed in

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any one of claims 1 through 6, wherein

the circuit verifying system executes assertion verification of a semiconductor integrated circuit by using the assertion description generated by the assertion generating system.

9. An assertion generating method that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit by a computer which has a program, comprising:

a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations and inputs the design data in storage;

a property generating step that reads the design data generated at the specification inputting step from the storage and generates a property to be verified with respect to the specification of the semiconductor integrated circuit using the read design data and inputs the property in the storage; and

an assertion generating step that reads the property generated at the property generating step from the storage and converts the property into an assertion description.

10. The assertion generating method as claimed in claim 9, wherein

the property generating step generates at least one or more properties, and

the specification inputting step generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations.

11. The assertion generating method as claimed in claim 9, wherein

the specification inputting step generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations.

12. The assertion generating method as claimed in any one of claims 9 through 11, wherein

the specification inputting step generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table

based on user operations.

13. The assertion generating method as claimed in claim 12, wherein

the assertion generating step converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or a signal name or a state name in the logic table or the state table edited at the specification inputting step is added.

14. The assertion generating method as claimed in any one of claims 9 through 13, wherein

the specification inputting step loads the design data into a graphic structure and inputs the graphic structure in the storage.

TITLE OF THE INVENTION

ASSERTION GENERATING SYSTEM, CIRCUIT VERIFYING SYSTEM, PROGRAM THEREOF, AND ASSERTION GENERATING METHOD

TECHNICAL FIELD

The present invention relates to a technology that executes circuit verification of an LSI (large scale integration) and so on by using a process based on a

computer program; and in particular, a verifying technology in which design violation and missing verification are confirmed in design data by converting a property of a circuit to be verified into an assertion description and inputting the assertion description to a simulator when the design data of the circuit in a RTL (register transfer level) are dynamically verified by the simulator.

The property to be discussed below is a plain text that defines operations intended and expected in a design circuit to be verified. For example, the property defines a relation between reception and response of a request signal and an approval signal in an arbiter circuit on time series constraint, and defines a regular state of the time series constraint and circuit specifications to be forbidden. In addition, the property is an event to be monitored as a function coverage point which confirms whether a specific circuit sequence has been tested by a simulation. Property verification verifies whether a design description satisfies a predetermined property.

BACKGROUND ART

Recently, a system has been revised or a revised edition of a system has been published frequently,

caused by missing verification of a corner case due to the complexity of a circuit and an increase of circuit size of a semiconductor integrated circuit, by missing confirmation of interface specifications among blocks allocated to plural designers due to group work, or by specification errors of a reusable core purchased from a third party.

These problems come from, for example, insufficient circuit verification or a test scenario that can extract bugs, which were not able to be formed because a corner case and core specifications of the third party were not understood sufficiently.

In order to solve these problems, an assertion verification technology, in which a property with respect to circuit specifications is converted into an assertion description and the assertion description is input to a simulator (computer) for verification, and a function coverage report for showing a warning for assertion violation during the simulation and showing whether a specific circuit sequence has been tested by a simulator is provided, has been proposed and has been recently put into use in actual designing.

An assertion is a note in which intention (in some cases, this shows property) of designing is written and is generally written by a comment sentence in a RTL.

The intention is interpreted by a simulator during the verification, for example, an error log is generated in a case where a circuit to be verified operates differently from the intention. The intention of designing is, for example, an assumption and a precondition of circuit input, and in addition to these, expected operations when the conditions are satisfied.

The simulator checks the following two matters.

(1) Specific events such as an assumption and a precondition have occurred.

(2) Expected operations at that time complete normally.

From the above check (1), the assertion gives feedback of determining information as to whether a specific circuit function is confirmed by verification. Therefore, when the assertion is comprehensively installed in a circuit to be verified, function coverage of the assertion can be obtained; consequently, its verification accuracy can be obtained quantitatively.

From the above check (2), the feedback to a verification debugging can be obtained by the assertion. For example, an assertion installed in a position, from which an influence caused by a circuit malfunction cannot be observed by external terminals, complements a malfunction state. In addition, when conditions such as

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an assumption and a precondition are satisfied in any stimulus, this expected operation is checked at any time. Therefore, for example, even when the stimulus is structured by a random system, self-collation with the expected operation, that is, comparison of expected values, can be executed. In addition, an assertion installed in a lower block is also effective in chip level verification.

The intention of designing may be described by a Verilog-HDL for verification being different from a RTL for logic synthesis; however, here, another assertion language is described.

At present, the most popular assertion language is a PSL (property specification language) described in Non-Patent Document 1. The PSL is an assertion language which will be given to IEEE from a standardization organization named Accellera, and is actually a standard language. In the following, an actual example of an assertion description using the PSL is shown.

For example, it is assumed that the following design intention (property) for memory control is desired to be monitored by verification.

1) read_n and write_n do not become Low at the same time

2) at the fall of write_n, enable_n is High

3) at the fall of read_n, enable_n is Low

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The PSL description (assertion description) to be given to a simulator as an assertion for the intention is as follows.

```
// psl property memcont1 = never (!write_n && !read_n)
@(posedge clk) ;
// psl assert memcont1 ;
// psl property memcont2 = always (enable_n) @(negedge
write_n) ;
// psl assert memcont2 ;
// psl property memcont3 = always (!enable_n) @(negedge
read_n) ;
// psl assert memcont3 ;
```

All of "psl, property, never, assert, always" in the above PSL description (assertion description) are reserved words in the PSL. All rows start with "//" which shows a comment of the Verilog-HDL. In this, instead of using "//", all of the PSL descriptions can be closed with "/**/".

The words "memcont1,2,3, !write_n && !read_n, posedge clk, enable_n, negedge write_n, !enable_n, negedge read_n" are descriptions by a user definition, and actual installed data names, that is, memory control signal names which appear in the RTL for defining the intention of 1) through 3) except for "memcont1,2,3".

In addition, "memcont1 through 3" are assertion

names and are used for knowing an error log and a function coverage being given from the simulator as feedback.

The assertion description by the PSL has the following structural elements.

// psl property <an assertion name> =

<an event to be monitored> -> <expected operation when a condition is satisfied> @<a strobe condition> ;

// psl assert <an assertion name> ;

For example, in the assertion of 1), "memcont1" is an assertion name, "!write_n && !read_n" is an event to be monitored, in this case, "never" is added in front of the event; therefore, it is monitored that the condition in ( ) never becomes true (if "always" is added, it is monitored that the condition in ( ) is true). By "@(posedge clk)" which follows the above statement, it is defined that monitoring the condition is executed at every time of rising edges. "->" changes to "|=>" or "|->" depending on the time when the expected operation is started. In this, the above example does not accompany expected operations.

The inside of ( ) of each part except the strobe condition is described by the Verilog-HDL which returns Boolean values. The inside of ( ) of the strobe

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condition has a description form of a sensitivity list described by an "always sentence" of the Verilog-HDL.

In the PSL, an event to be monitored can be defined, and each part of expected operations at the time when the condition is satisfied can define a sequence, that is, the changes of events and expected operations in plural cycles can be defined. An example is explained.

The intention of designing: When a clear start condition (m_task == 2'b00) is satisfied in a clearing process of a memory, in order to initialize all words (256 words), a writing operation is repeated 256 times. Here, one writing operation is completed by the operation of Low→High→High of write_n synchronized with a rise cycle (positive cycle) of clk.

The PSL description:

```
// psl sequence WRITE_PULSE = { !write_n; write_n;
write_n };
// psl property CLEAR_MEM_WRITE_N =
// always { m_task == 2'b00 } |=> { WRITE_PULSE [*256] }
// @(posedge clk) ;
// psl assert CLEAR_MEM_WRITE_N;
```

"sequence" defines a Low→High→High sequence of "write_n" by a macro-definition.

Here, it is the part of expected operations which follows "|=>" that is to be focused on. When

"m_task == 2'boo", the expected operation is WRITE_PULSE, that is, it is expected that the sequence of Low→High→High being three cycles of write_n be repeated by 256 times.

However, in such an assertion verifying technology, for example, in a case where the assertion description language is written by a manual input when the specifications are defined, there is a possibility that a mistake may be made in the assertion itself. As a result, a report of the warning of the assertion violation and the function coverage obtained by the assertion verification cannot be fed back to prevent the system revision and the revised edition of the system. Further, this requires a verification period for debugging the assertion description language. Consequently, the verification efficiency becomes worse.

In other words, the major premise of the assertion verifying technology is that the circuit specifications and the assertion description match each other; however, there is no method to confirm the matching before executing the simulation. Further, with respect to a complex finite state machine, it is difficult to describe a sequence of a comprehensive state transition by manual operation.

As conventional technologies with respect to

the assertion verification, for example, there are technologies disclosed in Patent Document 1 and Patent Document 2.

In Patent Document 1, a technology, in which a state transition machine is modeled by a graph and a state transition path that satisfies the assertion is searched, is disclosed. Further, a technology to confirm the rightness of the assertion by only an analysis of this graph is disclosed. By the technologies, matching the circuit specifications with the assertion description can be confirmed.

However, in these technologies, the state transition machine which is made to be a graph manually forms a model of the state transition machine which becomes a basic model, or the state transition machine is extracted from design data formed by a description language of a RTL. Consequently, mixing a mistake in an object to be matched, that is, in the model of the state transition machine which should be the circuit specifications, cannot be avoided.

In addition, in Patent Document 2, a technology, which generates an assertion for verifying a circuit by extracting a data transfer structure from design data of a RTL and expanding the data transfer structure into a graphic structure, is disclosed. However, in this

technology, since the assertion which is the circuit specifications is extracted from the design data, matching the circuit specifications with the assertion description cannot be assured.

[Patent Document 1] Japanese Laid-Open Patent Application No. 2000-181933

[Patent Document 2] Japanese Laid-Open Patent Application No. 2000-142918

[Non-Patent Document 1] Property Specification Language Reference Manual Version 1.1 June 9, 2004, online, retrieved in September 14, 2004, from the Internet, URL: http://www.eda.org/vfv/docs/PSL-v1.1.pdf

Consequently, in the conventional technologies, matching the circuit specifications with the assertion description cannot be assured.

DISCLOSURE OF THE INVENTION

The object of the present invention is to solve the problems in the conventional technologies, for example, to enable high reliability and high efficiency in assertion verification for an LSI and so on.

In order to achieve the above object, according to the present invention, a property to be verified is automatically converted into an assertion description language, based on a visual state transition figure, a

timing chart, a process sequence chart, and so on used when a designer forms specifications of a circuit.

According to the present invention, since the assertion description of a property to be verified is automatically generated from electronic data of a state transition figure which is attached to the specifications, matching the circuit specification with the assertion is established. Therefore, work to be used for debugging the assertion can be reduced. In addition, since the generated assertion is a function coverage point generated by comprehensive search of paths of the state transition, after the verification, feedback that a path has not been tested can be obtained by a function coverage report; consequently, missing a test of a corner case can be prevented. In addition, since the assertion description of a property to be verified is automatically generated from a selection condition of timing charts and signals which are attached to the specifications, or electronic data of figures or a table form in which a process sequence is noted or defined, matching the circuit specification with the assertion is established. Therefore, work to be used for debugging the assertion can be reduced. Especially, in many cases, the selection condition of timing charts and signals which are attached to the specifications or the process sequence is an

important assertion to be surely tested at the time of verification; however, since the assertion generated in the embodiments is an important property, a designer who does not know the specifications and the circuit functions sufficiently can execute verification by using the key property; as a result, the number of times of revising the system caused by missing the verification can be reduced.

BEST MODE FOR CARRYING OUT THE INVENTION

Next, referring to the drawings, preferred embodiments of the present invention are explained in detail.

FIG. 1 is a block diagram showing a structural example of hardware of which an assertion generating system and a circuit verifying system according to the present invention consist. FIG. 2 is a block diagram showing a first functional structure example of the assertion generating system and the circuit verifying system using the assertion generating system according to the present invention. FIG. 3 is an explanatory diagram showing a memory content example of a graphic structure which is used in the assertion generating system according to the present invention. FIG. 4 is an explanatory diagram showing a state transition figure and

a graphic structure example which is used in the assertion generating system according to the present invention. FIG. 5 is a block diagram showing a second functional structure example of the assertion generating system according to the present invention. FIG. 6 is a block diagram showing a third functional structure example of the assertion generating system according to the present invention. FIG. 7 is an explanatory diagram showing a timing chart example which is used in the assertion generating system according to the present invention. FIG. 8 is an explanatory diagram showing a structural body example for storing information with respect to signals defined on the timing chart and information with respect to timing constraints for the signals which is used in the assertion generating system according to the present invention. FIG. 9 is an explanatory diagram showing a memory content example of property information with respect to the timing chart shown in FIG. 7. FIG. 10 is a block diagram showing a fourth functional structure example of the assertion generating system according to the present invention. FIG. 11 is an explanatory diagram showing a structural example of a logic table of a full adder which is used in the assertion generating system according to the present invention. FIG. 12 is an explanatory diagram showing a

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structural body example for showing one cell when the cell in a table is loaded in a memory. FIG. 13 is an explanatory diagram showing a content example when a sheet is formed by combining structural bodies showing the cells shown in FIG. 12. FIG. 14 is an explanatory diagram showing a content when the logic table of the full adder shown in FIG. 11 is loaded in the memory structure shown in FIG. 13. FIG. 15 is an explanatory diagram showing a structural example of a process sequence in a table form which is used in the assertion generating system according to the present invention.

In FIG. 1, the reference number 101 is storage composed of a memory, a hard disk, and so on; the reference number 102 is a CPU (central processing unit); the reference number 103 is an input unit composed of a keyboard, a mouse, and so on; the reference number 104 is a display unit composed of a CRT (cathode ray tube), a LCD (liquid crystal display) and so on; the reference number 105 is a system bus, and a computer system is composed of the units 101 through 105 in which the units 101 through 104 are connected by the system bus 105.

The storage 101 stores functional descriptions of hardware not depending on architecture, and functions and means according to the present invention in feasible program formats which are read from recording media, from

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which a computer can read the programs, such as a CR-ROM (compact disc-read only memory), a DVD (digital video disc/digital versatile disc), and a FD (flexible disk). The CPU 102 executes the programs being stored in the storage 101, and executes processes of functions of the assertion generating system having the structure shown in FIG. 2.

A user interactively inputs commands to execute the programs that realize inputting and editing of the functional descriptions of hardware not depending on architecture and means of the present invention by using the input unit 103. The display unit 104 displays the functional descriptions of hardware not depending on architecture, and the progress and the results of the programs, which realize the means of the present invention, executed by the CPU 102.

FIG. 2 shows a basic structure of an assertion generating system 207 and a circuit verifying system using the assertion generating system 207 according to the present invention. First, a circuit specification to be specified in specifications is input from a graphical editor 201 by user operations, and the circuit specification formed by the graphical editor 201 is stored in the storage 101 as specification electronic data 202. In this, as the graphical editor 201, a

graphical editor such as a timing chart editor disclosed in, for example, Japanese Laid-Open Patent Application No. 1-309185 can be used.

Next, a syntax analyzer 203 reads the specification electronic data 202 being stored in the storage 101 and analyses the syntax, and a property extractor 204 extracts a property to be verified from the results of the syntax analysis.

An assertion generator 205 generates an assertion description language 206, which can be input to a simulator or a static property checker, from the property extracted from the property extractor 204. The assertion description language 206 generated in such a manner is stored in the storage 101 and is input to a simulator, and verification is executed.

As mentioned above, according to the assertion generating system of this example, when assertion verification, which verifies design data in which a property with respect to a specification of a semiconductor integrated circuit or a part of the specification of the semiconductor integrated circuit is described in an assertion description with design data of a circuit to be verified of the property, is executed by a simulator or a static verification tool, the graphical editor 201 generates the specification electronic data

202 (design data) by editing a specification of a finite state machine by a visual expression on a state transition table or a state transition figure. With respect to the circuit specification defined at the graphical editor 201, the syntax analyzer 203 and the property extractor 204 generates a property to be verified based on the design data, and the assertion generator 205 outputs this property in an assertion description.

Here, the design data (specification electronic data) formed at the graphical editor 201 are expanded into a graphic structure on the memory, and the property extractor 204 can refer to the graphic structure. Further, as the design data (specification electronic data) formed at the graphical editor 201, data, in which a process sequence of a circuit is shown in a timing chart or a time series figure by using a business tool that can edit a table input or a figure, are included, in addition to the state transition table and the state transition figure.

FIG. 5 shows an example in which the state transition figure is used as the design data (specification electronic data) to be formed at the graphical editor 201. In FIG. 5, graphical information 501 is, for example, the state transition figure

exemplified in FIG. 4(a), and is edited and formed by the graphical editor 201 and is stored in the storage being a hard disk, a system memory, and so on.

The graphical information 501 includes visual information, that is, coordinate information and so on when structural elements of the state transition figure are disposed, and the state transition figure expressed visually can be attached to specifications by printing out.

A graph search engine 502 has functions of the syntax analyzer 203 and the property extractor 204 shown in FIG. 2, and extracts a graphic structure exemplified in FIG. 4(b) from the state transition figure exemplified in FIG. 4(a), and temporarily stores the graphic structure in a system memory. In the extracted graphic structure, the structural elements of the state transition figure are formed as nodes, and the graph search engine 502 searches state transition paths. For example, the graph search engine 502 searches all state transition paths from an initial state of the state transition machine, extracts the paths, and loads them in the system memory or stores them in the hard disk as a path database 503.

A property converter 504 converts the state transition paths searched by the graph search engine 502

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into an assertion description language 505 by referring to the path database 503. The assertion description language 505 converted at the property converter 504 is described, for example, as a function coverage point for confirming whether the assertion description language 505 has been tested at a simulator.

A memory content of the graphic structure to be used at the graph search engine 502 is shown in FIG. 3. In FIG. 3, the reference number 301 is a structural body that stores information of each state in the state transition figure, and the reference number 302 is a structural body that stores information of arcs in the state transition figure. These structural bodies 301 and 302 mutually refer to pointers and form a graph in which the respective pointers are made to be nodes.

In FIG. 4, FIG. 4(a) shows an example of a state transition figure, and FIG. 4(b) shows a graphic structure formed from the state transition figure. The graph search engine 502 shown in FIG. 5 searches the state transition paths from the state transition figure shown in FIG. 4(a) by using a path search in graph logic, for example, an algorithm of a shortest path search. As a result, the graphic structure shown in FIG. 4(b) is formed and the graphic structure is stored in the path database 503.

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Next, an example of a state transition path to which can be stored in the path database 503 shown in FIG. 5 is shown by using the example shown in FIG. 4.

```
init ;
(GO) S1 ;
init ;
```

In this example, a path from "init" to "S1" is searched, and when "GO" is true, that is, is "1", the state transition path is formed.

In addition, an assertion description by PSL, which is generated by the property converter 504 in FIG. 5 (the assertion generator 205 in FIG. 2) from this state transition path, is shown as follows.

```
property init_to_S1 = always { state == init & GO} |=>
{ state == S1} ;
```

In case of a state transition machine, it is necessary whether all states are visited in verification, in order to quantify the verification accuracy of important functions being keys of circuit functions. Whether each state of the state transition machine is visited can be determined by confirming the function coverage of state verification by cover syntax of PSL. In case of the example shown in FIG. 4, it is enough that only state names stored in nodes of a graph are made to be a list by a cover description of PSL.

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In the following, the result is shown. In this, "state" is a state register name for holding the state at the time when a state transition machine is installed.

```
// psl cover ( state == init) ;
// psl cover ( state == S1) ;
```

Here, in a case where the graphical information 501 shown in FIG. 5 has information with respect to a graphic structure with the coordinate information, as shown in FIG. 3 and FIG. 4(a), the graph search engine 502 directly refers to the graphic structure in the graphical information 501.

Next, referring to FIG. 6, another embodiment of the present invention is explained. In the embodiment shown in FIG. 6, timing chart information to be attached to specifications is extracted from timing chart electronic data 601, and the interrelation with respect to timing of a signal group to be verified is made to be an assertion description.

In FIG. 6, the reference number 602 is a timing chart reader that reads the timing chart electronic data 601, the reference number 603 is a timing property extractor that extracts an interrelation with respect to timing of a signal group to be verified (timing chart information) and stores the interrelation in a timing chart database 604, and the reference number 605 is a

property converter that reads the timing chart information from the timing chart database 604 and generates an assertion description language 606 that can be input to a simulator or a static property checker.

In this, the timing chart electronic data 601 can be data formed and edited by a timing chart editor, in this case, the timing chart reader 602 becomes a syntax analyzer for timing chart information formed and edited by the timing chart editor.

The memory content which is used by the timing property extractor 603 is shown in FIG. 8. In FIG. 8, the reference number 801 is a structural body that stores information with respect to signals to be defined on the timing chart, and the reference number 802 is a structural body that stores information with respect to timing constraint for the signals.

An actual example of the timing chart that is read by the timing chart reader 602 is shown in FIG. 7. In the example shown in FIG. 7, "ack" rises during 2 to 5 cycles from the rise of "req" synchronized with "clk".

In the example shown in FIG. 7, the timing constraint (property), in which the rise of "ack" must be received in the range of 2 to 5 of "clk" after the output signal of "req" becomes 1, is described.

The timing property extractor 603 shown in FIG.

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6 extracts the timing information (property) to be verified by using signal attributes such as IN, OUT, and CK, and "pos" that means a rising condition, and interrelation with respect to timing of a signal group such as "<-" and "->" as keywords.

The timing chart information shown in FIG. 7 formed and edited by the timing chart editor is stored in hardware by being edited in, for example, the following list. In the following list, 1 through 3 rows show pins and input/output attributes, for example, a clock input, and 4 through 7 rows show waveform information. In the sixth row, a property, in which "ack" rises during 2 to 5 cycles from the rise of "req" synchronized with "clk", is shown.

```
1 CK      clk;
2 IN      ack;
3 OUT     req;
4 {clk,req,ack} = {1,0,0};
5 {clk,req,ack} = {1,1,0};
6 {clk,req,ack} = {1,0,0} [2:5];
7 {clk,req,ack} = {1,0,1};
```

A memory content of property information with respect to timing loaded by this timing chart information is shown in FIG. 9.

Next, an example, in which a business tool

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capable of inputting a table and editing a figure is used for editing a logic table and a time series property of the above circuit, is explained.

FIG. 11 is a structural example in which a logic table of a full adder is input by Excel (a registered trademark) being spread sheet software of Microsoft Corp. NAME, CLOCK, CONDITION, and EXPECT shown in a bold type are reserved words when a table definition is executed, and show a property name, a clock name, a start condition of an assertion check, and expected operations when the assertion check is started, respectively.

In the right under row of CONDITION and EXPECT, signal names are described, and under the names, logic values are entered. According to Excel, a sheet is composed of cells, a cell is a basic unit of a table, and the sheet can be output as an ASCII file by separating cells with ",".

In the case of FIG. 7, the signal name, the 1/2 pulse of clock, and so on are managed by cell, and after loading in a memory, the cell structure is scanned and the memory content shown in FIG. 9 is obtained.

FIG. 12 is a structural body for expressing one cell when a cell of Excel is loaded in a memory. Members of top, bottom, left, and right in this structural body

respectively execute a pointer reference to up and down and left and right.

FIG. 13 is a diagram showing a structural example of a sheet in which structural bodies of the cells shown in FIG. 12 are combined. The reference number 1301 is a pointer showing a sheet, and is composed of "next" being a pointer reference of the next sheet and a member that executes a pointer reference for a header of a cell. The reference number 1302 is a pointer of a cell, and executes a pointer reference for up and down and left and right by using the members of top, bottom, left, and right. By the above method, scanning cells on the sheet can be easily executed in a memory, and the search by the keywords such as NAME, CLOCK, CONDITION, and EXPECT and the interpretation of the logic table can be executed.

FIG. 14 shows a content when the logic table of the full adder shown in FIG. 11 is loaded in the memory structure shown in FIG. 13.

In the following, a PSL description, which generates an assertion description from the logic table of the full adder shown in FIG. 11, is shown. In this, the table and the verification data (that is, assertion) can be easily linked by adding the row number of the table to the structure of the assertion name. For

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example, on the first row, FADD_S_0__FADD_csv_line_5 is the assertion name, and line_5 corresponds to the row number of the table.

```
psl property FADD_S_0__FADD_csv_line_5 = always {!A & !B
& !CI} |-> {S === 1'b0};
psl property FADD_CO_0__FADD_csv_line_5 = always {!A & !B
& !CI} |-> {CO === 1'b0};
psl property FADD_S_1__FADD_csv_line_6 = always {!A & !B
& !CI} |-> {S === 1'b1};
psl property FADD_CO_1__FADD_csv_line_6 = always {!A & !B
& !CI} |-> {CO === 1'b0};
psl property FADD_S_2__FADD_csv_line_7 = always {!A & !B
& !CI} |-> {S === 1'b1};
psl property FADD_CO_2__FADD_csv_line_7 = always {!A & !B
& !CI} |-> {CO === 1'b0};
psl property FADD_S_3__FADD_csv_line_8 = always {!A & !B
& !CI} |-> {S === 1'b0};
psl property FADD_CO_3__FADD_csv_line_8 = always {!A & !B
& !CI} |-> {CO === 1'b1};
psl property FADD_S_4__FADD_csv_line_9 = always {!A & !B
& !CI} |-> {S === 1'b1};
psl property FADD_CO_4__FADD_csv_line_9 = always {!A & !B
& !CI} |-> {CO === 1'b0};
psl property FADD_S_5__FADD_csv_line_10 = always {!A & !B
& !CI} |-> {S === 1'b0};
```

```
psl property FADD_CO_5__FADD_csv_line_10 = always {!A
& !B & !CI} |-> {CO === 1'b1};
psl property FADD_S_6__FADD_csv_line_11 = always {!A & !B
& !CI} |-> {S === 1'b0};
psl property FADD_CO_6__FADD_csv_line_11 = always {!A
& !B & !CI} |-> {CO === 1'b1};
psl property FADD_S_7__FADD_csv_line_12 = always {!A & !B
& !CI} |-> {S === 1'b1};
psl property FADD_CO_7__FADD_csv_line_12 = always {!A
& !B & !CI} |-> {CO === 1'b1};
```

In FIG. 10, another embodiment of the present invention is explained. In this embodiment, a sequence to be attached to specifications is stored as table data 1001, a syntax analyzer 1002 loads a sequence which is defined in a table form in a system memory, a sequence extractor 1003 extracts a sequence of a process to be verified, and a property converter 1004 converts the sequence into an assertion description 1005.

An example of a sequence of a process is shown in FIG. 15. This example shows a property equal to that shown in FIG. 7. This example is also formed by Excel. The syntax analyzer 1002 and the sequence extractor 1003 resolve a sequence described in cells into time series, and the property converter 1004 generates an assertion description by using a SERE expanded regular expression

of PSL.

In the resolution of the sequence into time series, ";" in a character string is interpreted as behavior during one clock cycle. In FIG. 15, "0[*2:5]" uses a repetition expression of PSL, and means that a LOW period continues during 2 to 5 cycles. Further, since "ack" is described as "0[*2:5];1;0", "ack" shows behavior that a Low period continues during 2 to 5 cycles and after this High and Low follow.

In the following, an assertion description of PSL generated based on FIG. 15 is shown.

```
psl property reqack_ack_0__REQ_csv_line_5 = always
{(rose)} |-> {{ack === 1'b0}[*2:5];{ack === 1'b1};{ack
=== 1'b0};
```

Programs which the CPU 102 shown in FIG. 1 executes process flows shown in FIGS. 5, 6, and 10 are recorded in a magnetic medium and so on in a feasible form and stored in the storage 101.

As explained by using FIGs. 1 through 15, the assertion generating system 207 according to the embodiment generates an assertion description that is used for assertion verification of a semiconductor integrated circuit. The graphical editor 201 (specification inputting unit) generates design data of the semiconductor integrated circuit by graphically

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editing a specification (finite state machine, process sequence) of the semiconductor integrated circuit into a state transition table and a state transition figure or a timing chart and a time series figure based on user operations, forms the specification electronic data 202 by expanding the design data to a graphic structure, and causes the storage to store the data. In addition, the syntax analyzer 203 and the property extractor 204 (property generating unit) read the specification electronic data (design data) from the storage and generate a property to be verified with respect to the specification of the semiconductor integrated circuit based on the design data. Further, the assertion generator 205 (assertion generating unit) converts the property into the assertion description language 206.

In this, in the graphical editor 201 (specification inputting unit), the design data of the semiconductor integrated circuit can be generated by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations. The assertion generator 205 generates an assertion description; in which an assertion name composed of a table name or a table row number of the logic table or the state table edited at the graphical editor 201 (specification inputting unit), or

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an assertion name composed of a signal name or a state name in the logic table or the state table is added.

The circuit verification system according to the embodiment provides the assertion generating system 207 and executes assertion verification of the semiconductor integrated circuit by using the assertion description generated by the assertion generating system 207.

As mentioned above, according to the embodiments, since the assertion description of a property to be verified is automatically generated from electronic data of the state transition figure which is attached to the specifications, matching the circuit specification with the assertion is established. Therefore, work to be used for debugging the assertion can be reduced.

In addition, since the generated assertion is a function coverage point generated by comprehensive search of paths of the state transition, after the verification, feedback that a path has not been tested can be obtained by a function coverage report; consequently, missing a test of a corner case can be prevented.

In addition, since the assertion description of a property to be verified is automatically generated from a selection condition of timing charts and signals which

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are attached to the specifications, or electronic data of figures or a table form in which a process sequence is noted or defined, matching the circuit specification with the assertion is established. Therefore, work to be used for debugging the assertion can be reduced.

In many cases, the selection condition of timing charts and signals which are attached to the specifications or the process sequence is an important assertion to be surely tested at the time of verification; however, since the assertion generated in the embodiment is an important property, a designer who does not know the specifications and the circuit functions sufficiently can execute verification by using the key property; as a result, the number of times of revising the system caused by missing the verification can be reduced.

While the present invention is described above with reference to specific embodiments shown in FIGs. 1 through 15, it should be apparent that the invention is not limited to these embodiments, but numerous modifications could be made thereto by those skilled in the art without departing from the basic concept and scope of the invention. For example, in the embodiments, programs which realize the property extractor 204, the assertion generator 205, and so on are stored in the

storage 101 by using recording media such as a CD-ROM, a DVD, and a FD; however, the programs can be stored in the storage 101 by down loading via a network using a communication apparatus.

Further, in the embodiments, the assertion description using PSL is explained; however, the embodiments can be applied to other assertion descriptions.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a structural example of hardware of which an assertion generating system and a circuit verifying system according to the present invention consist;

FIG. 2 is a block diagram showing a first functional structure example of the assertion generating system according to the present invention;

FIG. 3 is an explanatory diagram showing a memory content example of a graphic structure which is used in the assertion generating system according to the present invention;

FIG. 4 is an explanatory diagram showing a state transition figure and a graphic structure example which is used in the assertion generating system according to the present invention;

FIG. 5 is a block diagram showing a second functional structure example of the assertion generating system according to the present invention;

FIG. 6 is a block diagram showing a third functional structure example of the assertion generating system according to the present invention;

FIG. 7 is an explanatory diagram showing a timing chart example which is used in the assertion generating system according to the present invention;

FIG. 8 is an explanatory diagram showing a structural body example for storing information with respect to signals defined on a timing chart and information with respect to timing constraints for the signals which is used in the assertion generating system according to the present invention;

FIG. 9 is an explanatory diagram showing a memory content example of property information with respect to the timing chart shown in FIG. 7;

FIG. 10 is a block diagram showing a fourth functional structure example of the assertion generating system according to the present invention;

FIG. 11 is an explanatory diagram showing a structural example of a logic table of a full adder which is used in the assertion generating system according to the present invention;

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FIG. 12 is an explanatory diagram showing a structural body example of one cell when the cell in a table is loaded in a memory;

FIG. 13 is an explanatory diagram showing a content example when a sheet is formed by combining the structural bodies showing a cell shown in FIG. 12;

FIG. 14 is an explanatory diagram showing a content example when the logic table of the full adder shown in FIG. 11 is loaded in the memory structurer shown in FIG. 13; and

FIG. 15 is an explanatory diagram showing a structural example of a process sequence in a table form which is used in the assertion generating system according to the present invention.

DESCRIPTION OF REFERENCE NUMBERS

101: storage, 102: CPU, 103: input unit, 104: display unit, 105: system bus, 201: graphical editor, 202: specification electronic data, 203: syntax analyzer, 204: property extractor, 205: assertion generator, 206: assertion description language, 301: structural body (pointer to arc set), 302: structural body (next ark pointer), 501: graphical information, 502: graph search engine, 503: path database (DB), 504: property converter, 505: assertion description language, 601: timing chart

electronic data, 602: timing chart reader, 603: timing property extractor, 604: timing chart database (DB), 605: property converter, 606: assertion description language, 801: structural body (pointer to relating signal), 802: structural body (next constraint pointer), 1001: table data, 1002: syntax analyzer, 1003: sequence extractor, 1004: property converter, 1005: assertion description language, 1301: pointer (showing a sheet), and 1302: pointer (of a cell)

ABSTRACT

In order to solve a problem that matching a circuit specification with an assertion description is not assured in a conventional technology, the present invention enables to establish high reliability and high efficiency in assertion verification for an LSI and so on.

In an assertion generating system 207, a graphical editor (specification inputting unit) 201 generates design data (specification electronic data 202) of a semiconductor integrated circuit by graphically editing a specification (finite state machine, process sequence) of the semiconductor integrated circuit with the use of a state transition table and a state transition figure or a timing chart and a time series figure based on user operations, and a property generating unit composed of a syntax analyzer 203 and a property extractor 204 generates a property to be verified with respect to the specification of the semiconductor integrated circuit based on the design data. An assertion generator 205 converts the property into an assertion description language 206.

FIG. 2

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FIG.1

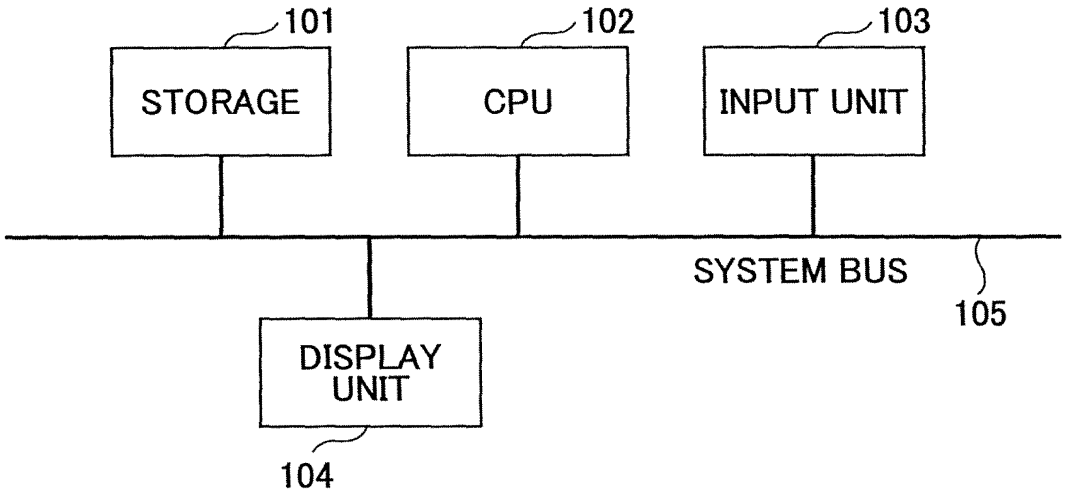

101
102
103
STORAGE
CPU
INPUT UNIT
SYSTEM BUS
105
DISPLAY UNIT
104

FIG.2

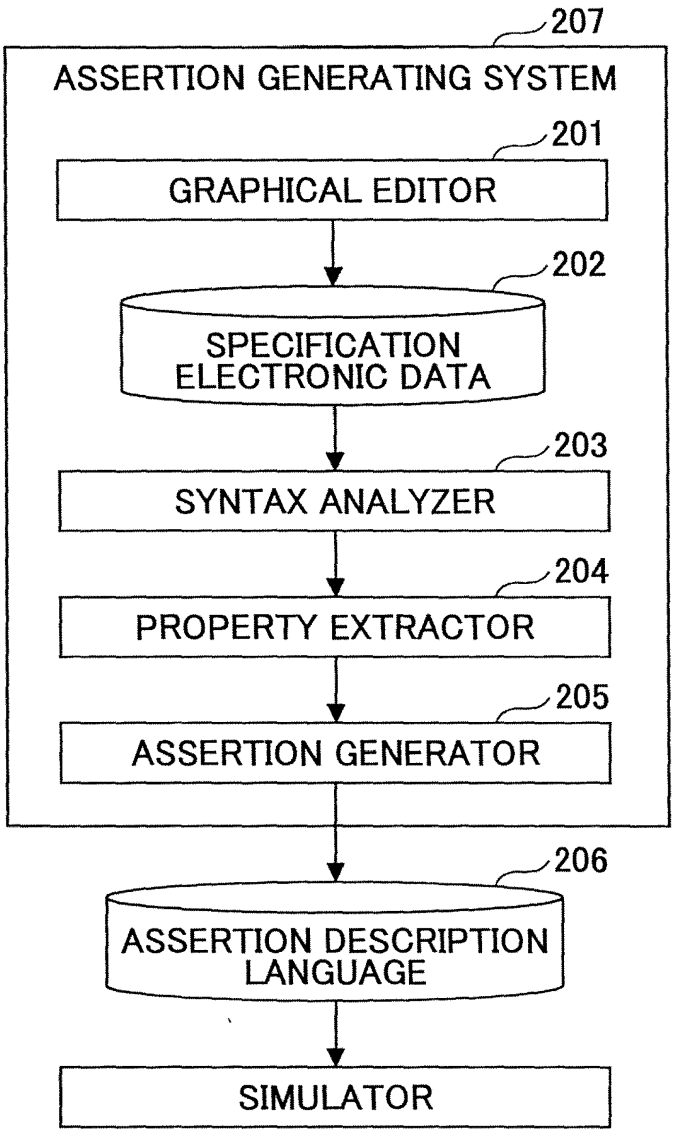

207
ASSERTION GENERATING SYSTEM
201
GRAPHICAL EDITOR
202
SPECIFICATION ELECTRONIC DATA
203
SYNTAX ANALYZER
204
PROPERTY EXTRACTOR
205
ASSERTION GENERATOR
206
ASSERTION DESCRIPTION LANGUAGE
SIMULATOR

FIG.3

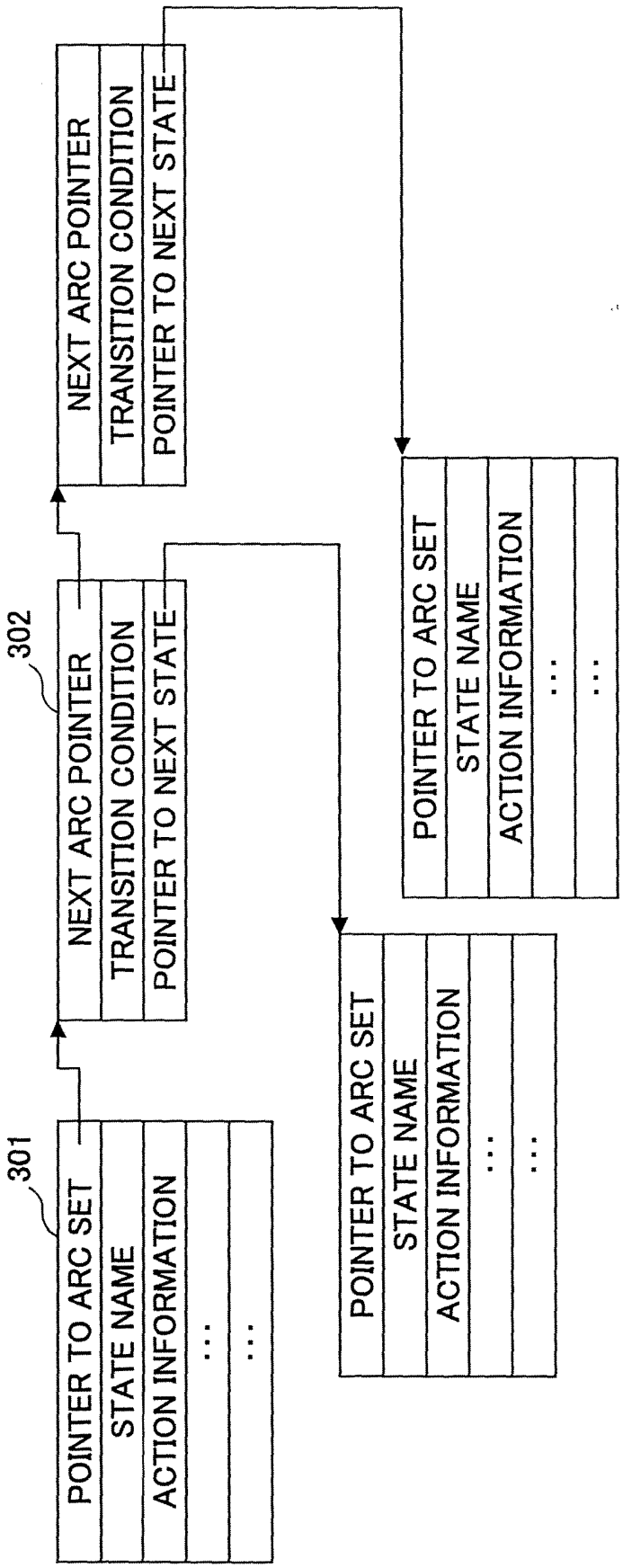

301
POINTER TO ARC SET
STATE NAME
ACTION INFORMATION
...
...
302
NEXT ARC POINTER
TRANSITION CONDITION
POINTER TO NEXT STATE
NEXT ARC POINTER
TRANSITION CONDITION
POINTER TO NEXT STATE
POINTER TO ARC SET
STATE NAME
ACTION INFORMATION
...
...
POINTER TO ARC SET
STATE NAME
ACTION INFORMATION
...
...

FIG.4

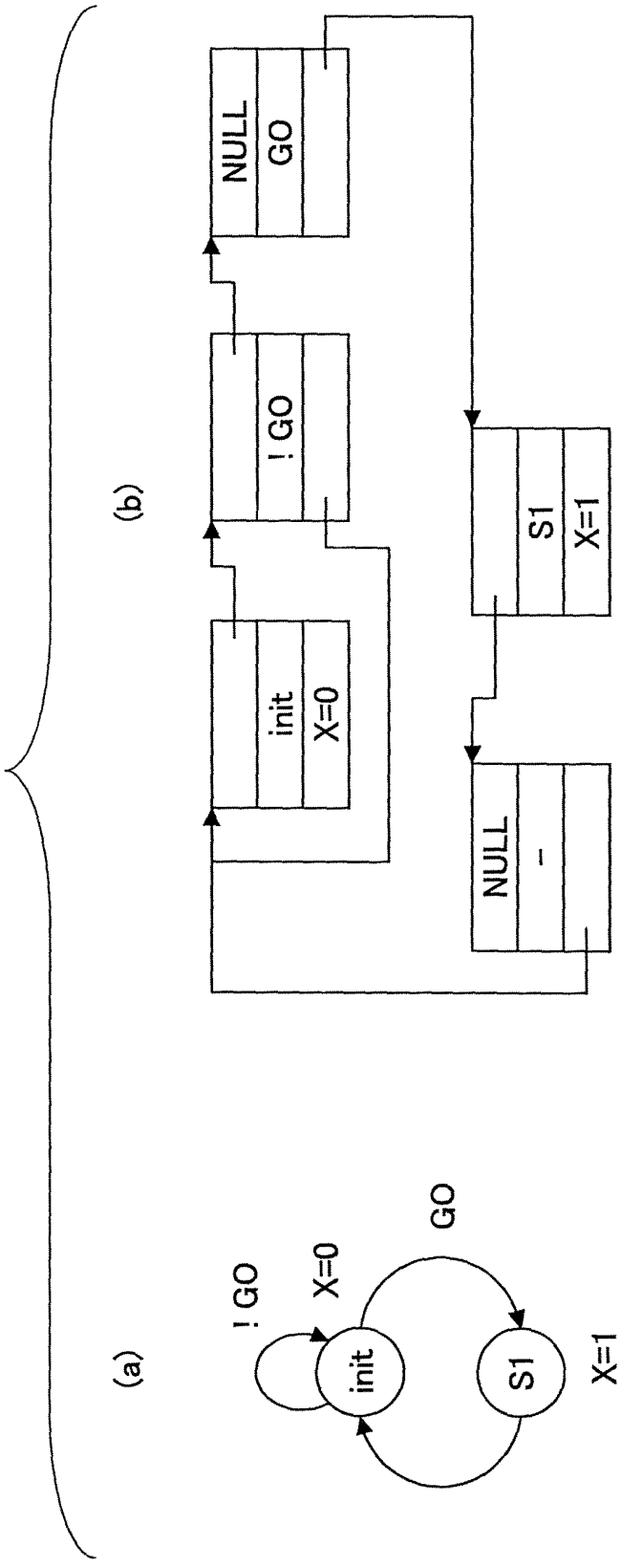


FIG.5

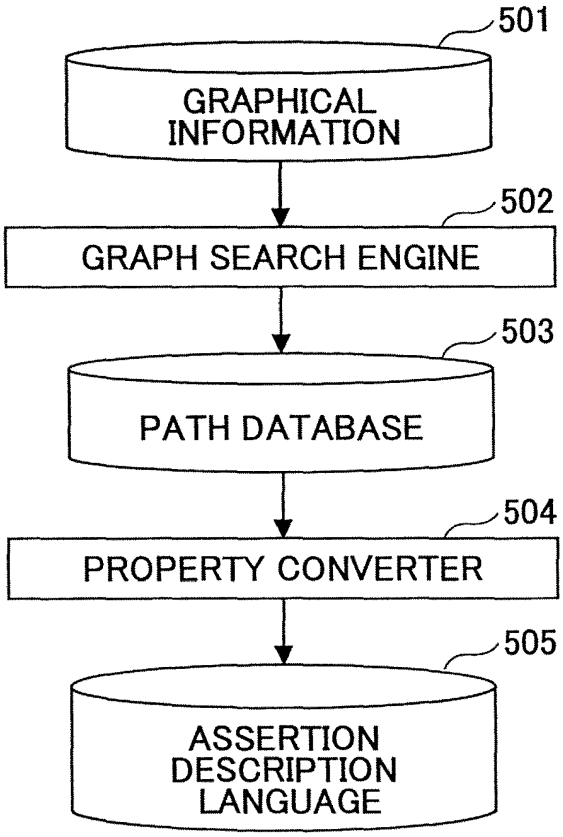

501
GRAPHICAL INFORMATION
502
GRAPH SEARCH ENGINE
503
PATH DATABASE
504
PROPERTY CONVERTER
505
ASSERTION DESCRIPTION LANGUAGE

FIG.6

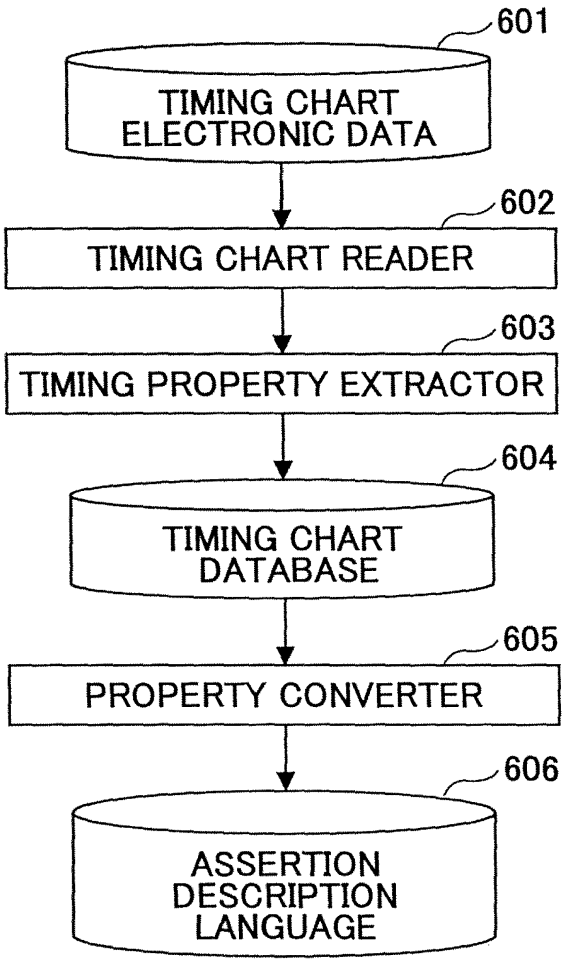

601
TIMING CHART ELECTRONIC DATA
602
TIMING CHART READER
603
TIMING PROPERTY EXTRACTOR
604
TIMING CHART DATABASE
605
PROPERTY CONVERTER
606
ASSERTION DESCRIPTION LANGUAGE

FIG.7

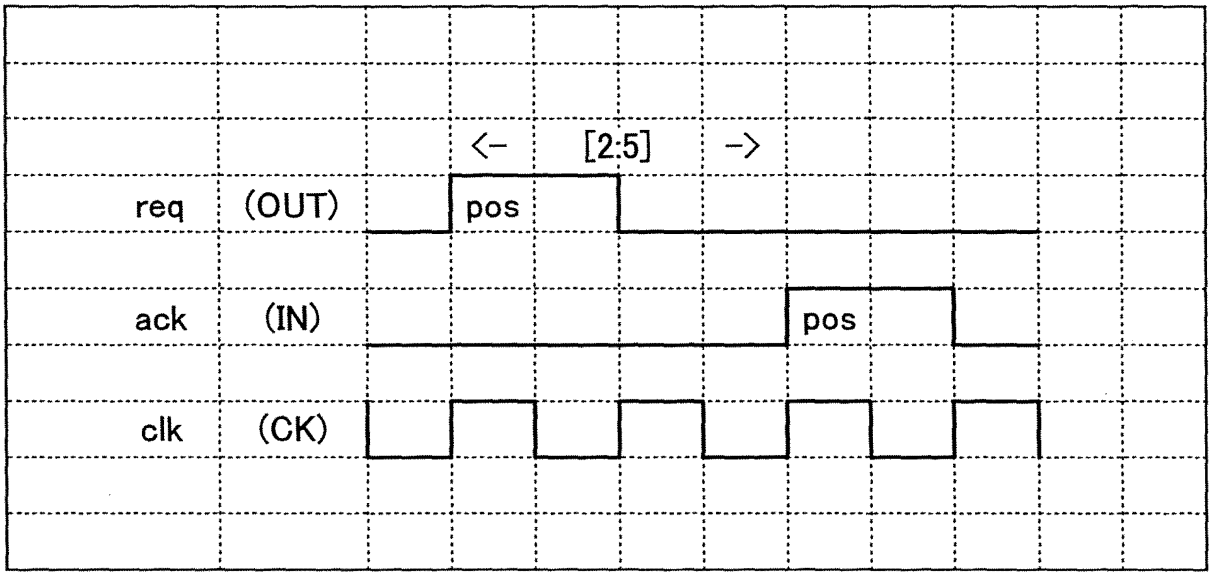

<-
[2:5]
->
req
(OUT)
pos
ack
(IN)
pos
clk
(CK)

FIG.8

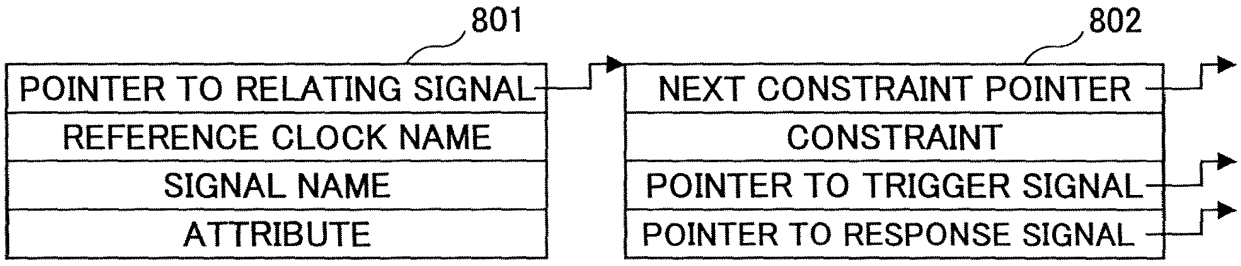

801
802
POINTER TO RELATING SIGNAL
REFERENCE CLOCK NAME
SIGNAL NAME
ATTRIBUTE
NEXT CONSTRAINT POINTER
CONSTRAINT
POINTER TO TRIGGER SIGNAL
POINTER TO RESPONSE SIGNAL

FIG.9

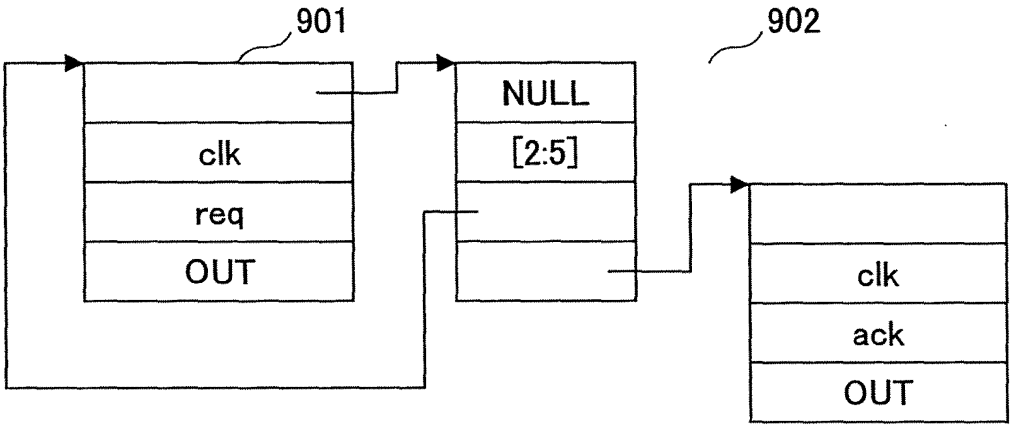
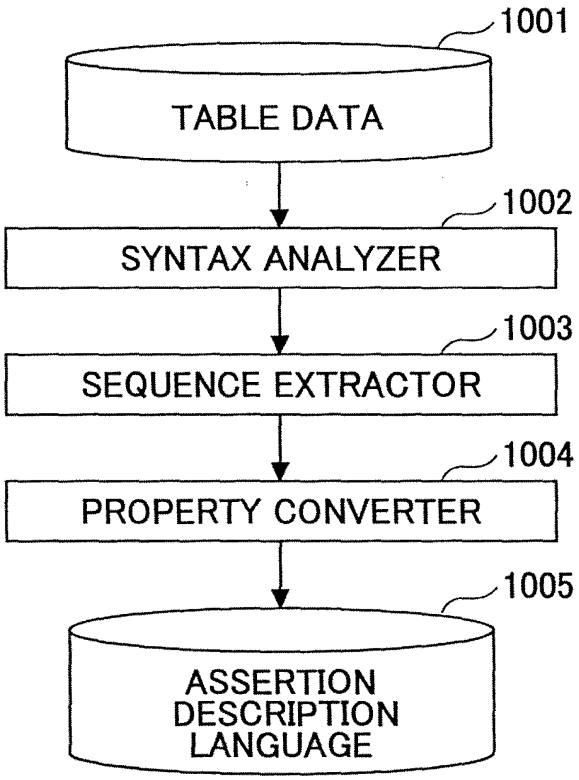


FIG.10



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FIG.11

NAME	FADD			
CLOCK	posedge clk			
CONDITION	CONDITION	CONDITION	EXPECT	EXPECT
A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FIG.12

```
typedef struct piece {
    struct piece        *left, *right, *top, *bottom
    char*               str;

} Piece ;
```

FIG.13

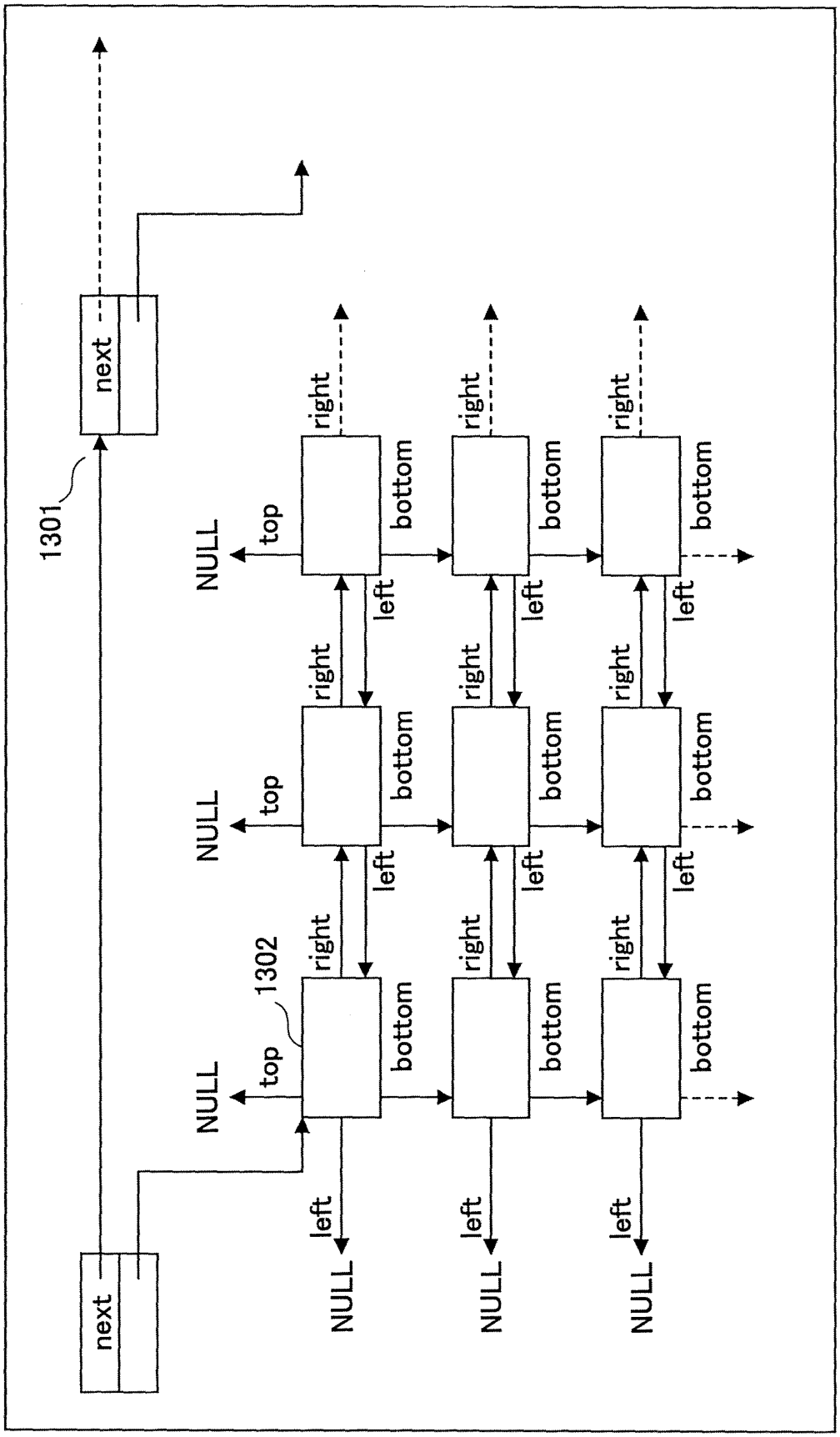


FIG.14

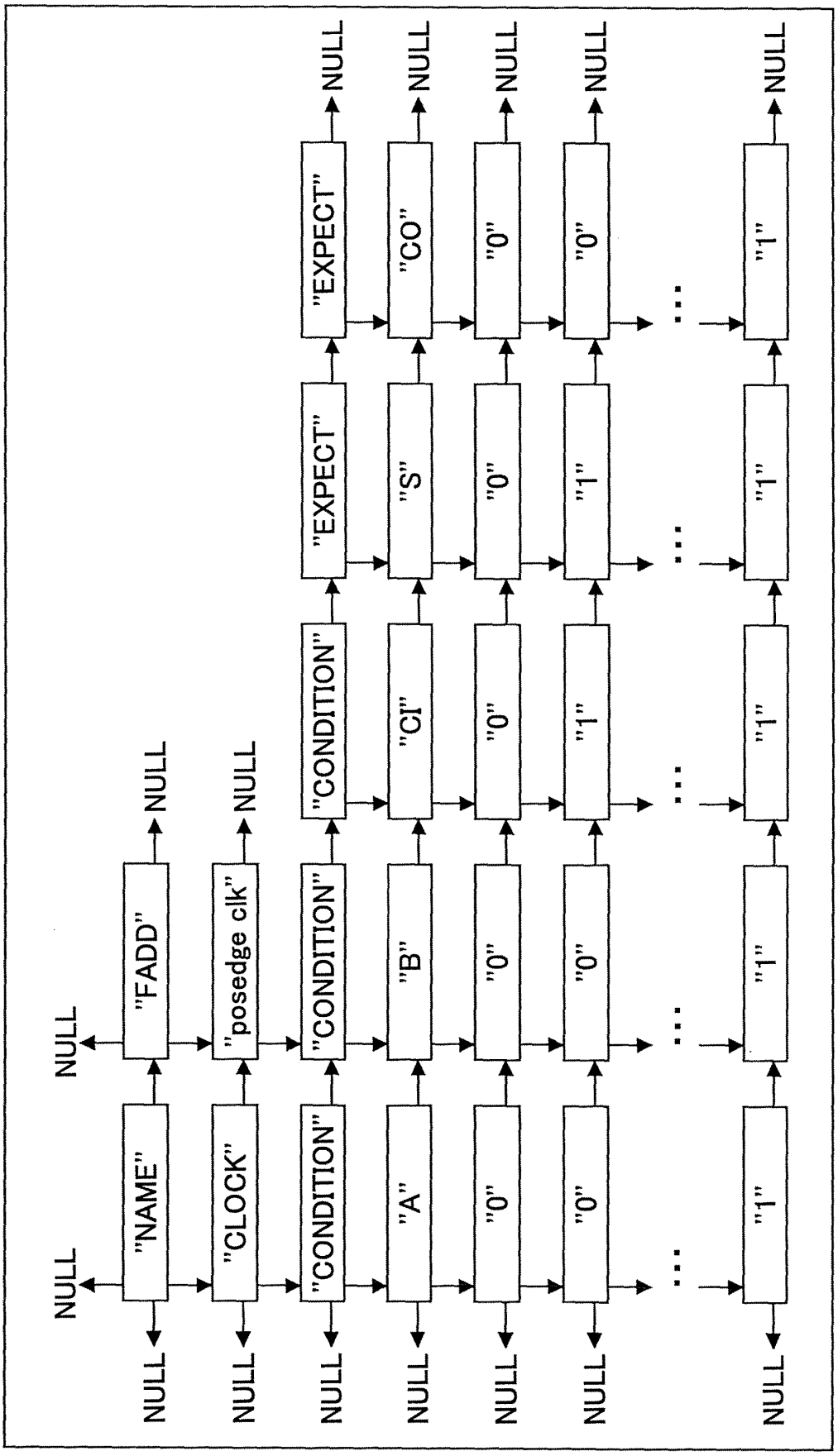

NULL
"NAME"
"CLOCK"
"CONDITION"
"A"
"0"
"0"
"1"
"1"
NULL
"FADD"
"posedge clk"
"CONDITION"
"B"
"0"
"0"
"1"
"1"
NULL
"CONDITION"
"CI"
"0"
"0"
"1"
"1"
NULL
"EXPECT"
"S"
"0"
"1"
"1"
NULL
"EXPECT"
"CO"
"0"
"0"
"1"
"1"
NULL

FIG.15

NAME	reqack
CLOCK	posedge clk
CONDITION	EXPECT
req	ack
rose	0[*2:5];1;0

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Electronic Patent Application Fee Transmittal

Application Number:	10579766
Filing Date:	18-May-2006
Title of Invention:	Assertion Generating System, Program Thereof, Circuit Verifying System, and Assertion Generating Method
First Named Inventor/Applicant Name:	Takamitsu Yamada
Filer:	Mark J. Thronson/robin lamalchaux
Attorney Docket Number:	R2184.0495/P495

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Independent claims in excess of 3	1614	1	220	220
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**220**

Electronic Acknowledgement Receipt

EFS ID:	4133013
Application Number:	10579766
International Application Number:	
Confirmation Number:	3580
Title of Invention:	Assertion Generating System, Program Thereof, Circuit Verifying System, and Assertion Generating Method
First Named Inventor/Applicant Name:	Takamitsu Yamada
Customer Number:	24998
Filer:	Mark J. Thronson/robin lamalchaux
Filer Authorized By:	Mark J. Thronson
Attorney Docket Number:	R2184.0495/P495
Receipt Date:	17-OCT-2008
Filing Date:	18-MAY-2006
Time Stamp:	13:42:22
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$220
RAM confirmation Number	7684
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		amdt.pdf	2873801 caaf42d8570c985b9c816ecc451170ce2b1c53d5	yes	65

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Amendment/Req. Reconsideration-After Non-Final Reject	1	2
Claims	3	7
Applicant Arguments/Remarks Made in an Amendment	8	9
Translation of Foreign Priority Documents	10	65

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	30409 a6d0ba750aa770b410bacb37e2763f560181ed81	no	2

Warnings:

Information:

Total Files Size (in bytes):	2904210

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
10/579,766	05/18/2006	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	10/17/2008	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***3	= 1	X $ =		OR	X $220=	220
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	220

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DEBRA a. SAVOY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,766	05/18/2006	Takamitsu Yamada	R2184.0495/P495	3580

24998 7590 12/17/2008

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
SIEK, VUTHE	
ART UNIT	PAPER NUMBER
2825	
MAIL DATE	DELIVERY MODE
12/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/579,766	YAMADA, TAKAMITSU	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/579,766 and amendment filed on //200. Claims 1-15 remain pending in the application.

Claim Objections

2. Claims 1 and 9 are objected to because of the following informalities: in the step of converting the property into an assertion description is suggested to automatically converting the property into an assertion description langue (see 0039) as regard to the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.

4. Claims 1-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The above claimed invention appears to be to an abstract idea than a practical application of the idea. The claimed invention does not result in an output transformation that provides a useful, concrete and tangible result. For example, the act of generating an assertion description [referred to assertion description language] clearly appears to be to an abstract idea than a practical application of the idea because such generated assertion description is not used nor transformed to another state that is useful to provide a concrete and tangible result. A tangible requirement does require that the claim must recite more than a 101 judicial exception, in that the process claim must set forth a practical application of that 101

judicial exception to produce a real-world result. In addition, the claimed invention lacks utility because it appears to be a data (generated assertion description). Since such data generated has not been used patentable utility is lacking. Therefore, the claimed invention appears non-statutory.

Allowable Subject Matter

5. Claims 1-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 101 and claim objection, set forth in this Office action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, A.U. 2825

Notice of References Cited	Application/Control No. 10/579,766	Applicant(s)/Patent Under Reexamination YAMADA, TAKAMITSU	
	Examiner Vuthe Siek	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,591,403	07-2003	Bass et al.	716/5
*	B	US-6,742,166	05-2004	Foster et al.	716/4
*	C	US-7,174,522	02-2007	Busch, Holger	716/5
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10579766	YAMADA, TAKAMITSU
	Examiner	Art Unit
	Vuthe Siek	2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/24/2008	12/12/2008							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10579766	YAMADA, TAKAMITSU
	Examiner	Art Unit
	Vuthe Siek	2825

SEARCHED			
Class	Subclass	Date	Examiner
716	4,5,18	6/24/08	VA

SEARCH NOTES		
Search Notes	Date	Examiner
EAST ALL DATABASES (SEE SEARCH REPORT PRINTOUT)	6/24/08	VS
UPDATED SEARCH (SEE PRINTOUT)	12/9/08	VS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	45	assert$3 with description with property	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:04
L2	562	assert$3 with verification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:04
L3	745	assert$3 with verify $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:04
L4	1139	2 or 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:04
L5	24	1 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:05
L6	929282	transition	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:32
L7	8	5 and 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:32
L8	6	translat$3 with property with assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:36
S1	536	assert$3 near4 description	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:06

S2	90459	graphical near5 representation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S3	72207	state near machine	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S4	3159118	property or timing near constraint	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S5	472053	simulat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S6	11	S1 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:08
S7	0	S3 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:08
S8	3196	S3 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:08
S9	1384	S8 and S4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:10
S10	699	S9 and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:10
S11	25614	assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:11

S12	67	S10 and S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:11
S13	4490	(716/4,18).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:23
S14	2	graphical with assertion near3 description	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:38
S15	5886	(716/4,5,18).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:39
S16	40	graphical with assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:39
S17	11	S5 and S16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:40
S18	356	property with assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:49
S19	25	S2 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:49
S20	599479	graphic$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:52
S21	156	S18 and S20	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:52

S22	32	S3 and S21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:53
S23	358	property with assertioN	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/24 17:08
S24	456	assertioN near4 language	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/24 17:08
S25	60	S23 and S24	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/24 17:08

12/9/08 5:40:13 PM
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Docket No.: R2184.0495/P495
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Takamitsu Yamada

Application No.: 10/579,766 | Confirmation No.: 3580

Filed: May 18, 2006 | Art Unit: 2825

For: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD | Examiner: V. Siek

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

INTRODUCTORY COMMENTS

In response to the Office Action dated December 17, 2008, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

AMENDMENTS TO THE CLAIMS

1. (Currently amended) An assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit, comprising:

a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations;

a computer readable storage device having a first storing unit that stores the design data generated by the specification inputting unit;

a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;

a second storing unit that stores the property generated by the property generating unit, wherein the second storing unit may or may not be a part of the computer readable storage device; and

an assertion generating unit that automatically converts the property into an assertion description if the property is to be verified during assertion verification by reading the property generated by the property generating unit from the second storing unit, wherein

the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

2. (Original) The assertion generating system as claimed in claim 1, wherein

the property generating unit generates at least one or more properties, and

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations.

3. (Original) The assertion generating system as claimed in claim 1, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property.

4. (Original) The assertion generating system as claimed in claim 1, wherein the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property.

5. (Original) The assertion generating system as claimed in claim 4, wherein the assertion generating unit converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or a signal name or a state name in the logic table or the state table edited by the specification inputting unit is added, and the property is the temporal property.

6. (Original) The assertion generating system as claimed in claim 1, wherein the specification inputting unit is a business tool of spread sheet software and expands the design data into a graphic structure and inputs the graphic structure in the first storing unit.

7. (Canceled)

8. (Currently amended) A circuit verifying system, comprising:

an assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit, comprising:

a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations;

a computer readable storage device having a first storing unit that stores the design data generated by the specification inputting unit;

a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;

a second storing unit that stores the property generated by the property generating unit, wherein the second storing unit may or may not be a part of the computer readable storage device; and

an assertion generating unit that automatically converts the property into an assertion description if the property is to be verified during assertion verification by reading the property generated by the property generating unit from the second storing unit, wherein

the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data; and

wherein the circuit verifying system executes assertion verification of the semiconductor integrated circuit by using the assertion description generated by the assertion generating system.

9. (Currently amended) A computer readable medium encoded with a program for causing a computer provided in an~~An~~ assertion generating system,~~method~~ that is capable of generating~~generates~~ an assertion description ~~which is used~~ for assertion verification of a semiconductor integrated circuit, to execute~~by a computer which has a program, comprising~~:

a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations and inputs the design data in storage;

a property generating step that reads the design data generated at the specification inputting step from the storage and generates a property which verifies the specification of the

semiconductor integrated circuit using the read design data and inputs the property in the storage; and

an assertion generating step that reads the property generated at the property generating step from the storage and automatically converts the property into an assertion description if the property is to be verified during assertion verification, wherein

the property generated by the property generating step is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

10. (Currently amended) The computer readable mediumassertion generating method as claimed in claim 9, wherein

the property generating step generates at least one or more properties, and

the specification inputting step generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations.

11. (Currently amended) The computer readable mediumassertion generating method as claimed in claim 9, wherein the specification inputting step generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property.

12. (Currently amended) The computer readable mediumassertion generating method as claimed in claim 9, wherein the specification inputting step generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property.

13. (Currently amended) The computer readable mediumassertion generating method as claimed in claim 12, wherein the assertion generating step converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or a signal name or a state name in the logic table or the state table edited at the specification inputting step is added, and the property is the temporal property.

14. (Currently amended) The computer readable mediumassertion generating method as claimed in claim 9, wherein the specification inputting step expands the design data into a graphic structure and inputs the graphic structure in the storage.

15. (Currently amended) A manufacturing method of a semiconductor device, comprising:

a designing step that designs an integrated circuit having a predetermined function;

a simulating step that simulates the integrated circuit by using an assertion generated by an assertion generating method; and

a manufacturing step that manufactures a semiconductor device based on specifications of the integrated circuit, and

wherein the assertion generating method comprises:

a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations and inputs the design data in storage;

a property generating step that reads the design data generated at the specification inputting step from the storage and generates a property which verifies the specification of the semiconductor integrated circuit using the read design data and inputs the property in the storage; and

an assertion generating step that reads the property generated at the property generating step from the storage and automatically converts the property into an assertion description if the property is to be verified during assertion verification, wherein

the property generated by the property generating step is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

Cadence Design Systems, Inc. - Ex. 1002, Page 00279

SDT00000323

REMARKS

Claims 1 and 8-15 have been amended. Claims 1-6 and 8-15 are pending in this application. Applicant reserves the right to pursue the original and other claims in this and other applications.

Claims 1 and 9 are objected to for informalities. Applicant submits that claims 1 and 9 have been amended to recite "automatically converts the property into an assertion description if the property is to be verified during assertion verification." Applicant respectfully submits that the objection be withdrawn and the claims allowed.

Claims 1-15 are rejected under 35 U.S.C. § 101 for being directed to non-statutory subject matter. This rejection is respectfully traversed and reconsideration is respectfully requested in light of the above amendments and the following remarks.

Applicant respectfully submits that Applicant's invention as claimed meets the requirements set forth in § 101. The text of the statute is provided below:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

35 U.S.C. § 101. With respect to a claimed process, the Supreme Court has held that "[a] claimed process is surely patent-eligible under § 101 if: (1) it is tied to a particular machine or apparatus, or (2) it transforms a particular article into a different state or thing." *In re Bilski*, 545 F.3d 943, 88 U.S.P.Q.2d 1385, 1391 (Fed. Cir. 2008) (en banc). Moreover, patent eligibility is determined based on the claim as a whole and not whether selected limitations constitute patent-eligible subject matter. *Id.* at 1394.

Applicant's invention relates to a technology that automatically generates an assertion description of a property which verifies the specification of a semiconductor integrated circuit. According to the Federal Circuit, a method is patent-eligible under § 101 if it is "tied to a particular

machine or apparatus," not counting any activity that is "insignificant" or "extra-solution." *In re Bilski*, at 1391, 1393, n.14. Claim 1 recites an assertion generating system comprising "a computer readable storage device having a first storing unit that stores the design data generated by the specification inputting unit." Thus, the generation of an assertion description by the assertion generating system of claim 1 is indeed "tied to a particular machine or apparatus." Moreover, storage of the design data by the computer readable storage device is a critical part of what is claimed as the stored design data is the input into the property generating unit that generates a property which verifies the specification based on the design data. As such, the assertion generating system of claim 1 is tied to at least one particular machine or apparatus in ways that are not insignificant and that are not extra-solution in nature. Therefore, claim 1 passes the first prong of the machine-or-transformation test.

Claim 8, as amended, recites limitations that are similar to those discussed above in connection with claim 1. Therefore, the § 101 rejection of claims 1 and 8 should be withdrawn.

Claim 9, as amended, is in the form approved in M.P.E.P. § 2106.01(I) ("a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory"). Thus, the § 101 rejection of claim 9 should be withdrawn.

Claim 15 recites a method of making a semiconductor device using an assertion description, the method comprising "a manufacturing step that manufacturers a semiconductor device based on specifications of the integrated circuit." The manufacturing step of claim 15 necessarily passes the second prong of the machine-or-transformation test because the claimed process "transforms a particular article into a different state or thing," namely, a semiconductor device. Therefore, the § 101 rejection of claim 15 should be withdrawn.

Claims 2-6 depend from claim 1 and claims 10-14 depend from claim 9. Accordingly, Applicant respectfully submits that claims 1-6 and 8-15 are in compliance with 35 U.S.C. § 101. Thus, Applicant requests that the rejection be withdrawn and the claims allowed. In view of the above, Applicant believes the pending application is in condition for allowance.

Dated: March 17, 2009

Respectfully submitted,

By_____

Mark J. Thronson
Registration No.: 33,082
Cathy Chen
Registration No.: 61,337
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicant

Electronic Acknowledgement Receipt

EFS ID:	4979643
Application Number:	10579766
International Application Number:	
Confirmation Number:	3580
Title of Invention:	Assertion Generating System, Program Thereof, Circuit Verifying System, and Assertion Generating Method
First Named Inventor/Applicant Name:	Takamitsu Yamada
Customer Number:	24998
Filer:	Mark J. Thronson/Madeline Baker
Filer Authorized By:	Mark J. Thronson
Attorney Docket Number:	R2184.0495/P495
Receipt Date:	17-MAR-2009
Filing Date:	18-MAY-2006
Time Stamp:	11:41:11
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Document.pdf	414925 6f6b4f0f5a4cc47c67cbb20aaacc6ab8b6e71b9e	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	10
Warnings:			
Information:			
	Total Files Size (in bytes):	414925	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☒ To be Mailed
10/579,766	05/18/2006	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	03/17/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/KATRINA HARLING/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	1	(assertion and specification and description and property and verification and convert$3 and graphic $4).clm.	US-PGPUB	OR	ON	2009/06/01 11:52
S1	536	assert$3 near4 description	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:06
S2	90459	graphical near5 representation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S3	72207	state near machine	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S4	3159118	property or timing near constraint	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S5	472053	simulat$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:07
S6	11	S1 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:08
S7	0	S3 and S6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:08

S8	3196	S3 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:08
S9	1384	S8 and S4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:10
S10	699	S9 and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:10
S11	25614	assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:11
S12	67	S10 and S11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:11
S13	4490	(716/4,18).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:23
S14	2	graphical with assertion near3 description	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:38
S15	5886	(716/4,5,18).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:39
S16	40	graphical with assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:39
S17	11	S5 and S16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:40

S18	356	property with assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:49
S19	25	S2 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:49
S20	599479	graphic$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:52
S21	156	S18 and S20	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:52
S22	32	S3 and S21	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/11 10:53
S23	358	property with assertioN	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/24 17:08
S24	456	assertioN near4 language	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/24 17:08
S25	60	S23 and S24	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/06/24 17:08
S26	45	assert$3 with description with property	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:04
S27	562	assert$3 with verification	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:04

S28	745	assert$3 with verify $3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:04
S29	1139	S27 or S28	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:04
S30	24	S26 and S29	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:05
S31	929282	transition	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:32
S32	8	S30 and S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:32
S33	6	translat$3 with property with assertion	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/12/09 17:36

6/1/09 11:53:25 AM
C:\ Documents and Settings\ vsiek\ My Documents\ EAST\ Workspaces\ 10579766.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10579766	YAMADA, TAKAMITSU
	Examiner	Art Unit
	Vuthe Siek	2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/24/2008	12/12/2008	06/01/2009						
1	1	✓	✓	=						
2	2	✓	✓	=						
3	3	✓	✓	=						
4	4	✓	✓	=						
5	5	✓	✓	=						
	6	✓	✓	-						
6	7	✓	✓	=						
7	8	✓	✓	=						
8	9	✓	✓	=						
9	10	✓	✓	=						
10	11	✓	✓	=						
11	12	✓	✓	=						
12	13	✓	✓	=						
13	14	✓	✓	=						
14	15	✓	✓	=						

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
10579766	YAMADA, TAKAMITSU
Examiner	**Art Unit**
Vuthe Siek	2825

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
716	4	G 0 6 F 17 / 50 (2006.0)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
716	5	18			

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
4	4														
5	5														
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6	7														
7	8														
8	9														
9	10														
10	11														
11	12														
12	13														
13	14														
14	15														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	14	
/Vuthe Siek/ Primary Examiner.Art Unit 2825	6/1/09	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2,3

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	10579766	YAMADA, TAKAMITSU
	Examiner	Art Unit
	Vuthe Siek	2825

SEARCHED

Class	Subclass	Date	Examiner
716	4,5,18	6/24/08	VA

SEARCH NOTES

Search Notes	Date	Examiner
EAST ALL DATABASES (SEE SEARCH REPORT PRINTOUT)	6/24/08	VS
UPDATED SEARCH (SEE PRINTOUT)	12/9/08	VS
SEE INTERFERENCE SEARCH REPORT PRINTOUT	6/1/09	VS

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner
716	4,5,18	6/1/09	VS

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

24998 7590 06/08/2009

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
SIEK, VUTHE	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/08/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,766	05/18/2006	Takamitsu Yamada	R2184.0495/P495	3580

TITLE OF INVENTION: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/08/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Cadence Design Systems, Inc. - Ex. 1002, Page 00293

SDT00000337

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24998 7590 06/08/2009

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,766	05/18/2006	Takamitsu Yamada	R2184.0495/P495	3580

TITLE OF INVENTION: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/08/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
SIEK, VUTHE	2825	716-004000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,766	05/18/2006	Takamitsu Yamada	R2184.0495/P495	3580

24998 7590 06/08/2009

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
SIEK, VUTHE	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/08/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 365 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 365 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Cadence Design Systems, Inc. - Ex. 1002, Page 00295

SDT00000339

Notice of Allowability	Application No.	Applicant(s)	
	10/579,766	YAMADA, TAKAMITSU	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *03/17/09*.

2. ☒ The allowed claim(s) is/are *1-6 and 8-15 (Renumbering per 37 CFR 1.126)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Vuthe Siek/
Primary Examiner, Art Unit 2825

DETAILED ACTION

1. This office action is in response to application 12/124,616 filed on 05/21/2008. Claims 1-6 and 8-15 remain pending in the application.

EXAMINER'S STATEMENT AS TO THE REASONS FOR ALLOWANCE

2. Claims 1-6 and 8-15 are allowed over the prior art of record.

3. The following is an examiner's statement of reasons for allowance: the prior art of record does not teach or fairly suggest a manufacturing method/computer readable storage medium encoded with a computer program/an assertion generating system comprising a graphical editor that graphically generates design data of a semiconductor integrated circuit by editing a specification; a property generating unit that generating a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by graphical editor; and assertion generating unit that automatically converts the property generating into an assertion description language if the property is to be verified during assertion verification by reading the property generated by the property generating unit and from the storage unit, wherein the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals or a least one or more signals in the design data. Note that a computer readable medium recited in the claims is refereed to a computer readable storage device that excludes any carrier waves or electromagnetic waves because they are non-statutory subject matter.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, Art Unit 2825

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
10579766	YAMADA, TAKAMITSU
Examiner	**Art Unit**
Vuthe Siek	2825

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
716	4	G 0 6 F 17 / 50 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
716	5	18			

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
4	4														
5	5														
6	6														
	7														
7	8														
8	9														
9	10														
10	11														
11	12														
12	13														
13	14														
14	15														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	14	
/Vuthe Siek/ Primary Examiner.Art Unit 2825	6/1/09	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2,3

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

24998 7590 06/08/2009

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,766	05/18/2006	Takamitsu Yamada	R2184.0495/P495	3580

TITLE OF INVENTION: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/08/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
SIEK, VUTHE	2825	716-004000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Dickstein Shapiro LLP
2 X
3 X

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Ricoh Company, Ltd.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Tokyo, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 1

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 04-1073 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 9/1/09

Typed or printed name Mark J. Thronson Registration No. 33,082

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	10579766
Filing Date:	18-May-2006
Title of Invention:	ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD
First Named Inventor/Applicant Name:	Takamitsu Yamada
Filer:	Ryan Holbrook Flax/Monick Lewis
Attorney Docket Number:	R2184.0495/P495

Filed as Large Entity

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	1	3	3
		Total in USD ($)		**1813**

Electronic Acknowledgement Receipt

EFS ID:	5994891
Application Number:	10579766
International Application Number:	
Confirmation Number:	3580
Title of Invention:	ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD
First Named Inventor/Applicant Name:	Takamitsu Yamada
Customer Number:	24998
Filer:	Ryan Holbrook Flax/Monick Lewis
Filer Authorized By:	Ryan Holbrook Flax
Attorney Docket Number:	R2184.0495/P495
Receipt Date:	01-SEP-2009
Filing Date:	18-MAY-2006
Time Stamp:	16:21:18
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1813
RAM confirmation Number	2585
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	R21840495.PDF	128561 c935b31338041cc17f66159d747df7d8eba29477	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	33871 bab82b33b84fae318735b0c2da4464054b0c77e4	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	162432		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,766	10/13/2009	7603636	R2184.0495/P495	3580

24998 7590 09/23/2009

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 365 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Takamitsu Yamada, Kanagawa, JAPAN;

Doc Code: PET.PTA.RCAL
Document Description: Request for Recalculation in view of Wyeth

PTO/SB/131 (01-10)
Approved for use through 02/28/2011. OMB 0651-0020
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR RECALCULATION OF PATENT TERM ADJUSTMENT IN VIEW OF *WYETH**

Attorney Docket Number: R2184.0495/P495	Patent Number: 7,603,636
Filing Date (or 371(b) or (f) Date): May 18, 2006	Issue Date: October 13, 2009
First Named Inventor: Takamitsu Yamada	
Title: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD	

PATENTEE HEREBY REQUESTS RECALCULATION OF THE PATENT TERM ADJUSTMENT (PTA) UNDER 35 USC 154(b) INDICATED ON THE ABOVE-IDENTIFIED PATENT. THE PATENTEE'S SOLE BASIS FOR REQUESTING THE RECALCULATION IS THE USPTO'S PRE-*WYETH* INTERPRETATION OF 35 U.S.C. 154(b)(2)(A).

Note: This form is only for requesting a recalculation of PTA for patents issued before March 2, 2010, if the sole basis for requesting the recalculation is the USPTO's pre-*Wyeth* interpretation of 35 U.S.C. 154(b)(2)(A). See Instruction Sheet on page 2 for more information.

Patentees are reminded that to preserve the right to review in the United States District Court for the District of Columbia of the USPTO's patent term adjustment determination, a patentee must ensure that he or she also takes the steps required under 35 U.S.C. 154(b)(3) and (b)(4) and 37 CFR 1.705 in a timely manner.

**Wyeth v. Kappos*, No. 2009-1120 (Fed. Cir., Jan. 7, 2010).

Signature Jennifer M. McCue	Date April 7, 2010
Name (Print/Typed) Jennifer M. McCue	Registration Number 55,440

Note: *Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below**.

[✓] *Total of 1 forms are submitted.

The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	7380415
Application Number:	10579766
International Application Number:	
Confirmation Number:	3580
Title of Invention:	ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD
First Named Inventor/Applicant Name:	Takamitsu Yamada
Customer Number:	24998
Filer:	Gianni Minutoli/Madeline Baker
Filer Authorized By:	Gianni Minutoli
Attorney Docket Number:	R2184.0495/P495
Receipt Date:	08-APR-2010
Filing Date:	18-MAY-2006
Time Stamp:	17:57:58
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for PTA recalculation in view of Wyeth	Document.pdf	57435 c49cae5b642bcabf40ee9316e868148ea7d7d73b	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	57435

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

Mail Date: 04/21/2010

Applicant	: Takamitsu Yamada	: DECISION ON REQUEST FOR
Patent Number	: 7603636	: RECALCULATION of PATENT
Issue Date	: 10/13/2009	: TERM ADJUSTMENT IN VIEW
Appliction No	: 10/579,766	: OF WYETH AND NOTICE OF INTENT TO
Filed	: 05/18/2006	: ISSUE CERTIFICATE OF CORRECTION
		:

The Request for Recalculation is **GRANTED** to the extent indicated.

The patent term adjustment has been determined to be **513** days. The USPTO will *sua sponte* issue a certificate of correction reflecting the amount of PTA days determined by the recalculation.

Prior to the issuance of the certificate of correction, the USPTO will afford patentee an opportunity to be heard and request reconsideration. Accordingly, patentee has **one month or thirty (30) days,** whichever is longer, to file a request for reconsideration of this patent term adjustment calculation. See 35 U.S.C. 154(b)(3)(B)(ii) and 37 CFR 1.322(a)(4). No extensions of time will be granted under 37 CFR 1.136.

Patentee should use document code PET.OP if electronically filing a request for reconsideration of this patent term adjustment calculation. The patentee must also include the information required by 37 CFR 1.705(b)(2) and the fee required by 37 CFR 1.18(e). If patentee does not file a timely request for reconsideration of this patent term adjustment calculation including the information required by 37 CFR 1.705(b)(2) and the fee required by 37 CFR 1.18(e), the USPTO will issue a certificate of correction reflecting the PTA determination noted above.

Patentee should be aware that in order to preserve the right to review in the United States District Court for the District of Columbia of the USPTO patent term adjustment determination, patentee must ensure that he or she also take the steps required under 35 U.S.C. 154(b)(4)(A) in a timely manner. Nothing in the request for recalculation should be construed as providing an alternative time frame for commencing a civil action under 35 U.S.C. 154(b)(4)(A).

Any questions concerning this decision should be directed to the Office of Patent Legal Administration at 571-272-7702.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,603,636 B2
APPLICATION NO. : 10/579766
DATED : October 13, 2009
INVENTOR(S) : Takamitsu Yamada

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

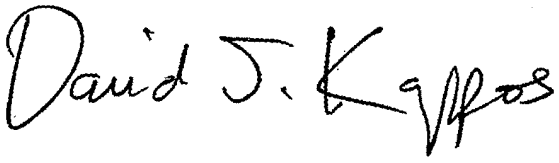
On the Title Page:

The first or sole Notice should read --

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 513 days.

Signed and Sealed this

Fifth Day of October, 2010



David J. Kappos
Director of the United States Patent and Trademark Office

PTO/SB/81A (12-08)
Approved for use through 09/30/2025. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Patent Number	7603636
Issue Date	October 13, 2019
First Named Inventor	TAKAMITSU YAMADA
Title	ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD
Attorney Docket No.	0823-03984

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: **27197**

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Inventor, having ownership of the patent.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____.

SIGNATURE of Inventor or Patent Owner

Signature	/Yi Lu/	Date	March 14, 2023
Name	Yi Lu	Telephone	
Title and Company	Authorized Signatory for Patent Matters of Semiconductor Design Technologies LLC		

NOTE: Signatures of all the inventors or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of _____ forms are submitted.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0035. Public burden for this form is estimated to average 15 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **If filing this completed form by mail, send to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013). https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf

Routine uses of the information in this record may include disclosure to: 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law; 2) a Federal, state, local, or international agency, in response to its request; 3) a contractor of the USPTO having need for the information in order to perform a contract; 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record; 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record; 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations; 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals; 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)); 9) the Office of Personnel Management (OPM) for personnel research purposes; and 9) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Additional Uses

Additional USPTO uses of the information in this record may include disclosure to: 1) the International Bureau of the World Intellectual Property Organization, if the record is related to an international application filed under the Patent Cooperation Treaty; 2) the public i) after publication of the application pursuant to 35 U.S.C. 122(b), ii) after issuance of a patent pursuant to 35 U.S.C. 151, iii) if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections, or an issued patent, or iv) without publication of the application or patent under the specific circumstances provided for by 37 CFR 1.14(a)(1)(v)-(vii); and/or 3) the National Archives and Records Administration, for inspection of records.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
10/579,766	**03/14/2023 07:47:51 PM ET**	**R2184.0495/P495**

Title of Invention

ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD

Application Information

APPLICATION TYPE	Utility - U.S. National Stage under 35 USC 371	PATENT #	7603636
CONFIRMATION #	3580	FILED BY	Yi Lu
PATENT CENTER #	61741397	FILING DATE	05/18/2006
CUSTOMER #	24998	FIRST NAMED INVENTOR	Takamitsu Yamada
INTL. APPLICATION #	-	INTL. FILING DATE	-
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Szymon Gurda

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
636- aia0096.pdf	3	Assignee showing of ownership per 37 CFR 3.73	201 KB
636-sb0081a.pdf	2	Power of Attorney	466 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
636- aia0096.pdf	D9D8B23311BAB4A0ED4397D9CF981AEA9463C5B4FD7681F62

	B552FCFF2F2B9CC3E4EF13A91E43901D972DF048A6451ECEE 8D951E931695C3165F49BFB0FCB9C3
636-sb0081a.pdf	0EEFFC2CE9559ABA7075AB0A4B5C027B63470CBC8B20E46F 521D6871FE6301E5B84957D3A69A9DCEDCEAA500072B183C C3CF1E2C0FBC01183DF598555BA03E5E

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: SEMICONDUCTOR DESIGN TECHNOLOGIES LLC

Application No./Patent No.: 7603636 Filed/Issue Date: October 13, 2009

Titled: ASSERTION GENERATING SYSTEM, PROGRAM THEREOF, CIRCUIT VERIFYING SYSTEM, AND ASSERTION GENERATING METHOD

SEMICONDUCTOR DESIGN TECHNOLOGIES LLC, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: TAKAMITSU YAMADA To: RICOH COMPANY, LTD.

   The document was recorded in the United States Patent and Trademark Office at

   Reel 017909, Frame 0731, or for which a copy thereof is attached.

2. From: RICOH COMPANY, LTD. To: SEMICONDUCTOR DESIGN TECHNOLOGIES LLC

   The document was recorded in the United States Patent and Trademark Office at

   Reel 062552, Frame 0702, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Szymon M. Gurda/	March 14, 2023
Signature	Date
Szymon M. Gurda	58451
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/579,766	05/18/2006	Takamitsu Yamada	R2184.0495/P495

CONFIRMATION NO. 3580

POA ACCEPTANCE LETTER

27197
MICHAEL J. CHERSKOV
SZYMON M. GURDA
903 COMMERCE DR
SUITE 310
OAK BROOK, IL 60523

OC000000137606305

Date Mailed: 03/21/2023

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/14/2023.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sltorres/

Cadence Design Systems, Inc. - Ex. 1002, Page 00319

SDT00000363

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/579,766	05/18/2006	Takamitsu Yamada	R2184.0495/P495

CONFIRMATION NO. 3580

POWER OF ATTORNEY NOTICE

24998
Blank Rome LLP
1825 Eye Street, NW
Washington, DC 20006-5403

OC000000137606303

Date Mailed: 03/21/2023

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/14/2023.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sltorres/

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SDT00000364