

**Exhibit A-2: Infringement of U.S. Patent No. 7,603,636 by Cadence Spectre Simulation Platform,  
Including Spectre Simulation, Xcelium Parallel Logic Simulator, Virtuoso ADE Product Suite, and Debug Suite**

Cadence directly infringes claims 1, 7, 8, and 13 under §271(a) by installing Spectre Simulation Platform software on computer-readable medium as part of a computer in an assertion generating system, and making and/or using the computer-readable medium. For example, Cadence installs the Spectre Simulation Platform software on computers it uses to test the functionality of the Spectre Simulation Platform software, as well as provide support to its customers. “The Cadence Global Customer Support team strives to provide flexible access to the expert support you need to successfully resolve any EDA challenge or technical issue. Whether it's fast access to our knowledgebase of solutions and technical documentation or direct collaboration between your team and Cadence technical experts, Cadence is committed to providing efficient technical support that fits your needs.” SDT00000687-689, [https://www.cadence.com/en\\_US/home/support/support-process.html](https://www.cadence.com/en_US/home/support/support-process.html). For purposes of this chart, “Spectre Simulation Platform” includes Spectre AMS Designer, Spectre FX, Spectre X, RF, Virtuoso ADE Integration, EM-IR, Xcelium Parallel Logic Simulator, Virtuoso ADE Product Suite, Debug Suite (also referred to as “Spectre Product(s)” or “Spectre”). The term “Spectre Simulation Platform” and any variants including, for example, “Spectre software,” “Spectre Product(s)” or “Spectre system” also includes any associated computer software and data, and any associated hardware, and processes and methods related thereto not specifically listed above.

Cadence indirectly infringes claims 1, 7, 8, and 13 under §271(b) by inducing its customers to make and/or use an assertion generating system by installing the Spectre Simulation Platform on customer-provided computer-readable media for generating assertion descriptions for validation of a semiconductor IC. SDT00000694-695, [https://www.cadence.com/en\\_US/home/tools/custom-ic-analog-rf-design/circuit-simulation/spectre-ams-designer.html](https://www.cadence.com/en_US/home/tools/custom-ic-analog-rf-design/circuit-simulation/spectre-ams-designer.html); SDT00000696-708, [https://www.cadence.com/content/dam/cadence-www/global/en\\_US/documents/training/learning-maps.pdf#page=4](https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/training/learning-maps.pdf#page=4). “Cadence® software is available through electronic distribution to customers with a current maintenance agreement and Cadence Online Support, or eDA-on-Tap website accounts. To stay up to date when selected product base and update releases are available, Cadence Online Support users may set up their Software Update Preferences. Software update notifications will provide an email containing the release information along with a link to an online order form.” SDT00000683-686, [https://www.cadence.com/en\\_US/home/support/software-downloads.html](https://www.cadence.com/en_US/home/support/software-downloads.html). See also SDT00000679-681, [https://www.cadence.com/en\\_US/home/support/computing-platform-support.html](https://www.cadence.com/en_US/home/support/computing-platform-support.html) (“Cadence works with our hardware platform partners to ensure that our products run on a variety of UNIX- and PC-based systems. For up-to-date information on operating system support, select the support matrix below. This matrix shows current Cadence® technology releases and the operating systems supported across UNIX and PC platforms.”)

Cadence indirectly infringes claim 14 under §271(b) by inducing its customers to use the Spectre Simulation Platform to perform the manufacturing method. Customers utilize the Spectre Simulation Platform to perform the manufacturing method to design and manufacture (including direct a fab to manufacture) a semiconductor integrated circuit. See, e.g., SDT00000709-712, [Spectre AMS Datasheet](#) at 710 (discussing meeting tapeout schedules for manufacturing integrated circuits). Cadence is a member of the TSMC EDA Alliance. “TSMC EDA Alliance, a key component of TSMC Open Innovation Platform® (OIP), reduces design barriers for customer's adoption of TSMC process technologies. By combining TSMC and EDA Alliance members R&D capability and resource, new generations of EDA solutions are enabled to be compliant to TSMC technology requirements.” SDT00000682, [https://www.tsmc.com/english/dedicatedFoundry/oip/eda\\_alliance](https://www.tsmc.com/english/dedicatedFoundry/oip/eda_alliance).

Cadence also indirectly infringes claims 1, 7, 8, 13, and 14 under §271(c) by contributing to the infringement by its customers. Customers directly infringe these claims for the same reasons stated above in connection with §271(b). The Spectre Simulation Platform is a material part of a computer provided in an assertion generation system for generating system for generating assertion descriptions for validation of a semiconductor IC. The portions of the Spectre Simulation Platform that map to claims 1, 7, 8, 13, and 14 have no substantial non-infringing uses.

| US7603636                                                                                                                                                                  | Spectre Simulation Platform                                                                                                                                                                                                                                               |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1[pre]. An assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit, comprising: | To the extent the preamble is limiting, a computer upon which Spectre Simulation Platform software is installed is an assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit. |

| US7603636                                                                                                                                                                                                                                                                        | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                                  | <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| [a] a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations; | <p>The Spectre system includes a specification inputting unit, including software and/or hardware that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations. Spectre generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit. Spectre allows users to graphically edit the specification of the semiconductor integrated circuit based on user operations.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

| US7603636 | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|           | <div data-bbox="600 164 1197 509"><p data-bbox="621 175 926 207"><b>Spectre AMS Designer</b></p><div data-bbox="617 232 1180 316"><div data-bbox="617 232 888 316">Spectre simulation</div><div data-bbox="909 232 1180 316">Xcelium Parallel Logic Simulator</div></div><div data-bbox="611 354 865 402">Supports an analog-centric design flow</div><div data-bbox="888 354 909 402">↕</div><div data-bbox="932 354 1176 402">Supports a digital-centric design flow</div><div data-bbox="600 427 1197 509"><div data-bbox="600 427 888 509">Virtuoso ADE Product Suite</div><div data-bbox="909 427 1197 509">Debug suite</div></div></div> <p data-bbox="648 561 1180 583"><i>Figure 2: One simulator supports either verification flow</i></p> <p data-bbox="590 607 1190 631">SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 710.</p> <p data-bbox="596 651 1203 886">Spectre AMS Designer is tightly integrated with the Virtuoso ADE Product Suite for mixed-signal block design. It uses native Analog Design Environment netlisting technologies to combine schematics and behavioral views, enabling users to independently manage the level of abstraction of each block. The entire design is configured using the hierarchy editor, which facilitates the viewing and design preparation of a complex mixed-signal design.</p> <p data-bbox="590 906 1190 930">SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 710.</p> <p data-bbox="596 956 1434 1045">Virtuoso Schematic Editor L is the design intent environment of the industry standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed-signal design.</p> <p data-bbox="590 1065 1379 1089">SDT00000713-733, <a href="#">Virtuoso Schematic Editor L and XL Data Sheet</a>.</p> |

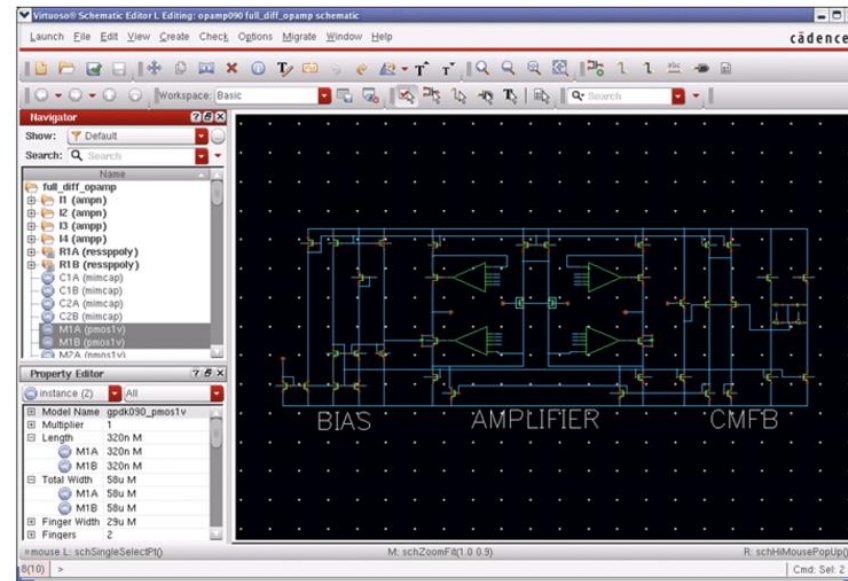


Figure 1: Virtuoso Schematic Editor L

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

Virtuoso Schematic Editor XL is the new design and constraint composition environment of the industry-standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed signal design.

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

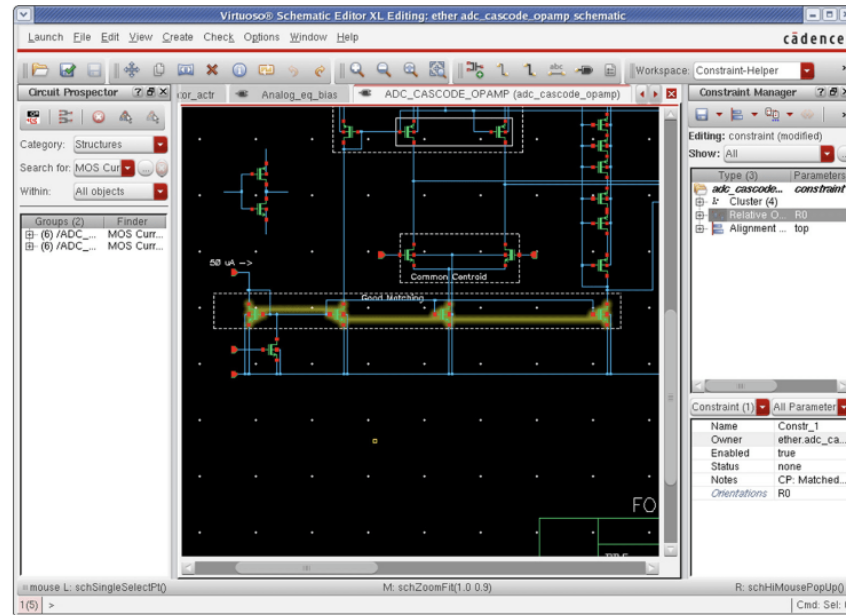


Figure 2: Virtuoso Schematic Editor XL common constraint environment

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to fully and accurately describe functionality of the Accused Products with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.

[b] a computer readable storage device having a first storing unit that stores the design data generated by the specification inputting unit;

The Spectre system includes a computer readable storage device having a first storing unit, including software and/or hardware that stores the design data generated by the specification inputting unit.

| US7603636                                                                                                                                                                                                                                                                     | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                               | <p><b>Design inputs</b></p> <ul style="list-style-type: none"> <li>▶ OpenAccess database</li> <li>▶ Verilog-AMS 2.0</li> <li>▶ VHDL-AMS 1076.1</li> <li>▶ Verilog (IEEE 1364-1995, IEEE 1364-2001 extensions)</li> <li>▶ VHDL (IEEE 1076-1987, IEEE 1076-1993, IEEE 1076.4-2000 [VITAL 2000])</li> <li>▶ Spectre and SPICE netlist formats</li> <li>▶ SystemVerilog (IEEE 1800)</li> <li>▶ Unified Power Format (UPF) or Common Power Format (CPF)</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                   |
| <p>[c] a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;</p> | <p>The Spectre system includes a property generating unit, including software and/or hardware that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data. The Spectre AMS feature of “capturing design intent” or “capturing power intent” verifies the specification.</p> <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting “PowerSmart” connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul> |

| US7603636                                                                                                                                                                                                                                                                              | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                                        | <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <p>[d] a second storing unit that stores the property generated by the property generating unit, wherein the second storing unit may or may not be a part of the computer readable storage device; and</p>                                                                             | <p>The Spectre system includes a second storing unit, including software and/or hardware that stores the property generated by the property generating unit, wherein the second storing unit may or may not be a part of the computer readable storage device.</p> <ul style="list-style-type: none"> <li>▸ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▸ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| <p>[e] an assertion generating unit that automatically converts the property into an assertion description if the property is to be verified during assertion verification by reading the property generated by the property generating unit from the second storing unit, wherein</p> | <p>The Spectre system includes an assertion generating unit, including software and/or hardware that automatically converts the property into an assertion description if the property is to be verified during assertion verification by reading the property generated by the property generating unit from the second storing unit. The Spectre AMS's assertions are generated from the properties that "captur[e] design intent" so that the assertions can be used to verify the design.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

| US7603636                                                                                                                                                                                                                         | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                   | <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| <p>[f] the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.</p> | <p>In Spectre, the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.</p> <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p>                                                                                                                                                                                                                                                                                                                                                                                              |

| US7603636                                                                                                                                                                     | <b><u>Spectre Simulation Platform</u></b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                               | <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                                    |
| <p>7. A circuit verifying system, comprising:</p>                                                                                                                             | <p>To the extent the preamble is limiting, a computer upon which Spectre software is installed is a circuit verifying system.</p> <ul style="list-style-type: none"> <li>▸ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▸ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> |
| <p>[a] an assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit, comprising:</p> | <p>The Spectre system includes an assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

| US7603636                                                                                                                                                                                                                                                                                 | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                                           | <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| <p>[a-1] a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations;</p> | <p>The assertion generating system of Spectre includes a specification inputting unit, including software and/or hardware that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations.</p> <div data-bbox="598 1029 1199 1377"> <p><b>Spectre AMS Designer</b></p> <pre> graph TD     subgraph Spectre_AMS_Designer [Spectre AMS Designer]         direction LR         S[Spectre simulation]         X[Xcelium Parallel Logic Simulator]     end     S --- DF1[Supports an analog-centric design flow]     X --- DF2[Supports a digital-centric design flow]     DF1 &lt;--&gt; DF2     DF1 --- V[Virtuoso ADE Product Suite]     DF2 --- D[Debug suite] </pre> </div> <p><i>Figure 2: One simulator supports either verification flow</i></p>                                                                                                                                                                                                                                                                                                                           |

SDT00000709-712, [Spectre AMS Datasheet](#) at 710.

Spectre AMS Designer is tightly integrated with the Virtuoso ADE Product Suite for mixed-signal block design. It uses native Analog Design Environment netlisting technologies to combine schematics and behavioral views, enabling users to independently manage the level of abstraction of each block. The entire design is configured using the hierarchy editor, which facilitates the viewing and design preparation of a complex mixed-signal design.

SDT00000709-712, [Spectre AMS Datasheet](#) at 710.

Virtuoso Schematic Editor L is the design intent environment of the industry standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed-signal design.

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

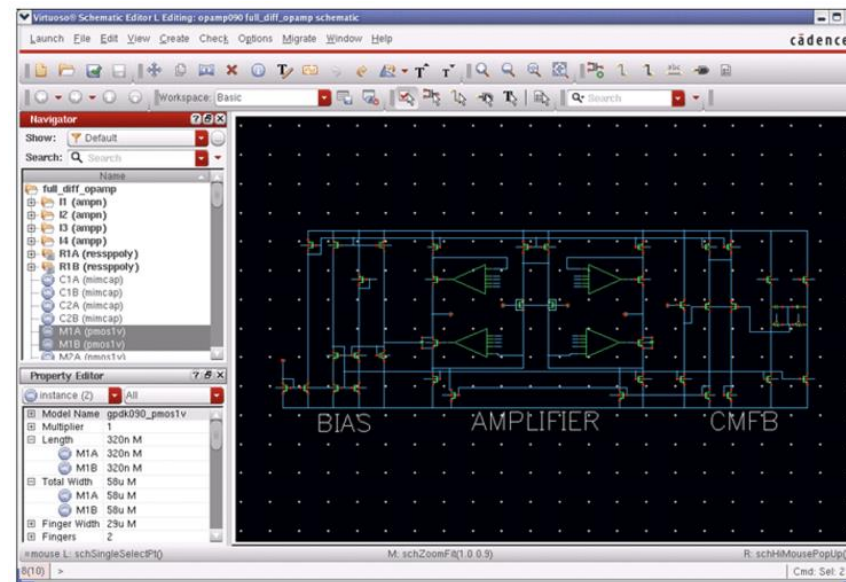
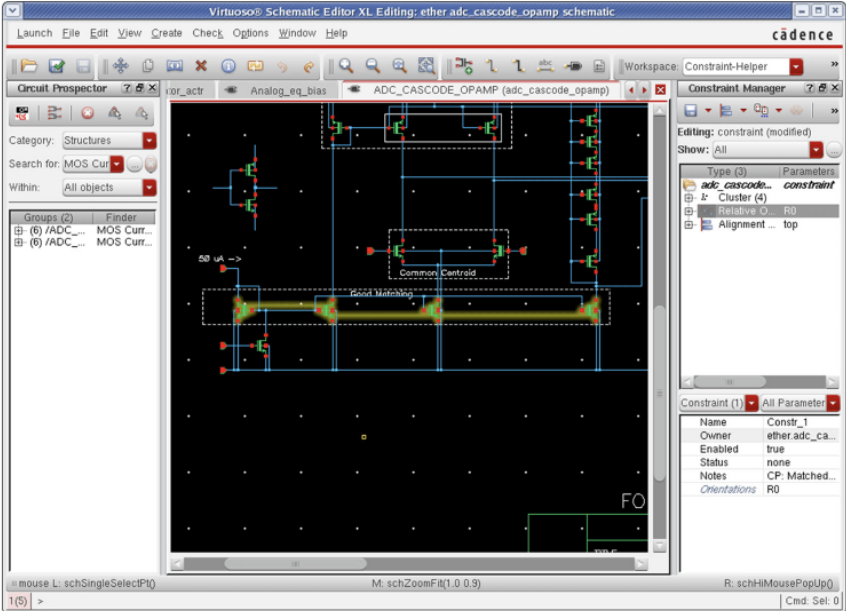


Figure 1: Virtuoso Schematic Editor L

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

Virtuoso Schematic Editor XL is the new design and constraint composition environment of the industry-standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed signal design.

| US7603636                                                                                                                                       | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                 | <p>SDT00000713-733, <a href="#">Virtuoso Schematic Editor L and XL Data Sheet</a>.</p>  <p>Figure 2: Virtuoso Schematic Editor XL common constraint environment</p> <p>SDT00000713-733, <a href="#">Virtuoso Schematic Editor L and XL Data Sheet</a>.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| [a-2] a computer readable storage device having a first storing unit that stores the design data generated by the specification inputting unit; | The assertion generating system of Spectre includes a computer readable storage device having a first storing unit that stores the design data generated by the specification inputting unit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

| US7603636                                                                                                                                                                                                                                                                       | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                                 | <p><b>Design inputs</b></p> <ul style="list-style-type: none"> <li>▶ OpenAccess database</li> <li>▶ Verilog-AMS 2.0</li> <li>▶ VHDL-AMS 1076.1</li> <li>▶ Verilog (IEEE 1364-1995, IEEE 1364-2001 extensions)</li> <li>▶ VHDL (IEEE 1076-1987, IEEE 1076-1993, IEEE 1076.4-2000 [VITAL 2000])</li> <li>▶ Spectre and SPICE netlist formats</li> <li>▶ SystemVerilog (IEEE 1800)</li> <li>▶ Unified Power Format (UPF) or Common Power Format (CPF)</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                                           |
| <p>[a-3] a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;</p> | <p>The assertion generating system of Spectre includes a property generating unit, including software and/or hardware that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data. The Spectre AMS feature of “capturing design intent” or “capturing power intent” verifies the specification.</p> <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting “PowerSmart” connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul> |

| US7603636                                                                                                                                                                                                                                                                                | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                                          | <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <p>[a-4] a second storing unit that stores the property generated by the property generating unit, wherein the second storing unit may or may not be a part of the computer readable storage device; and</p>                                                                             | <p>The assertion generating system of Spectre includes a second storing unit, including software and/or hardware that stores the property generated by the property generating unit, wherein the second storing unit may or may not be a part of the computer readable storage device.</p> <ul style="list-style-type: none"> <li>▸ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▸ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| <p>[a-5] an assertion generating unit that automatically converts the property into an assertion description if the property is to be verified during assertion verification by reading the property generated by the property generating unit from the second storing unit, wherein</p> | <p>The assertion generating system of Spectre includes an assertion generating unit, including software and/or hardware that automatically converts the property into an assertion description if the property is to be verified during assertion verification by reading the property generated by the property generating unit from the second storing unit. The Spectre AMS's assertions are generated from the properties that "captur[e] design intent" so that the assertions can be used to verify the design.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

| US7603636                                                                                                                                                                                                                      | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                | <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| [b] the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data; and | <p>In Spectre, the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.</p> <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p>                                                                                                                                                                                                                                                                                                                                                                                              |

| US7603636                                                                                                                                                                                                | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                          | <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <p>[c] wherein the circuit verifying system executes assertion verification of the semiconductor integrated circuit by using the assertion description generated by the assertion generating system.</p> | <p>In Spectre, the circuit verifying system executes assertion verification of the semiconductor integrated circuit by using the assertion description generated by the assertion generating system.</p> <ul style="list-style-type: none"> <li>▸ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▸ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| <p>8. A computer readable medium encoded with a program for causing a computer provided in an assertion generating system, that is capable of generating an assertion description</p>                    | <p>To the extent the preamble is limiting, a computer readable medium encoded with Spectre software satisfies this language. Spectre causes a computer provided in an assertion generating system to generate an assertion description.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

| US7603636                                                                     | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                               | <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| for assertion verification of a semiconductor integrated circuit, to execute: | <p>To the extent the preamble is limiting, Spectre performs assertion verification of a semiconductor integrated circuit.</p> <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                       |

| US7603636                                                                                                                                                                                                                  | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>[a-1] a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations and</p> | <p>The computer upon which Spectre is installed executes a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations.</p> <div data-bbox="600 266 1199 613"> <p>The diagram, titled 'Spectre AMS Designer', illustrates the integration of simulation and design tools. At the top, two boxes are shown: 'Spectre simulation' (blue) and 'Xcelium Parallel Logic Simulator' (green). Below these, a vertical double-headed arrow indicates bidirectional communication between two design flows: 'Supports an analog-centric design flow' on the left and 'Supports a digital-centric design flow' on the right. At the bottom, two more boxes are shown: 'Virtuoso ADE Product Suite' (orange) and 'Debug suite' (yellow). The 'Spectre simulation' box is connected to the 'Virtuoso ADE Product Suite' box, and the 'Xcelium Parallel Logic Simulator' box is connected to the 'Debug suite' box.</p> </div> <p><i>Figure 2: One simulator supports either verification flow</i></p> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 710.</p> <p>Spectre AMS Designer is tightly integrated with the Virtuoso ADE Product Suite for mixed-signal block design. It uses native Analog Design Environment netlisting technologies to combine schematics and behavioral views, enabling users to independently manage the level of abstraction of each block. The entire design is configured using the hierarchy editor, which facilitates the viewing and design preparation of a complex mixed-signal design.</p> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 710.</p> <p>Virtuoso Schematic Editor L is the design intent environment of the industry standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed-signal design.</p> <p>SDT00000713-733, <a href="#">Virtuoso Schematic Editor L and XL Data Sheet</a>.</p> |

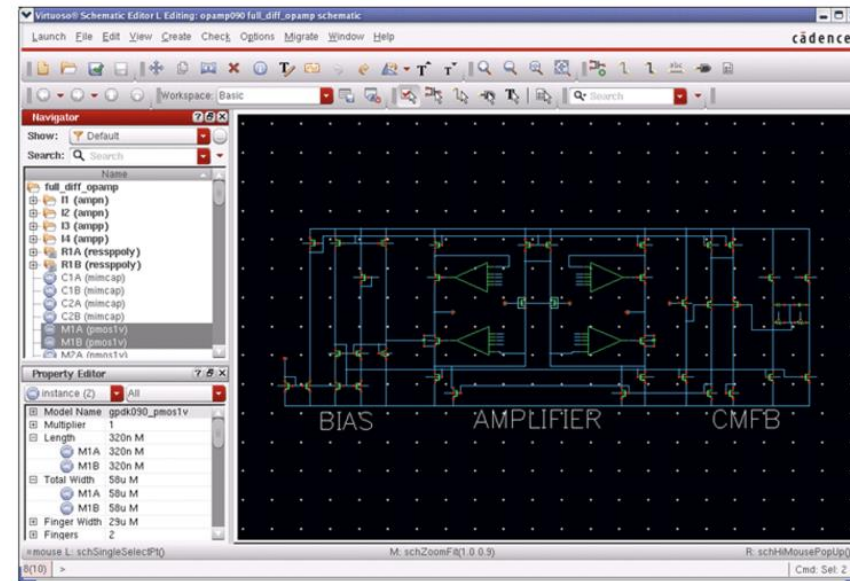


Figure 1: Virtuoso Schematic Editor L

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

Virtuoso Schematic Editor XL is the new design and constraint composition environment of the industry-standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed signal design.

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

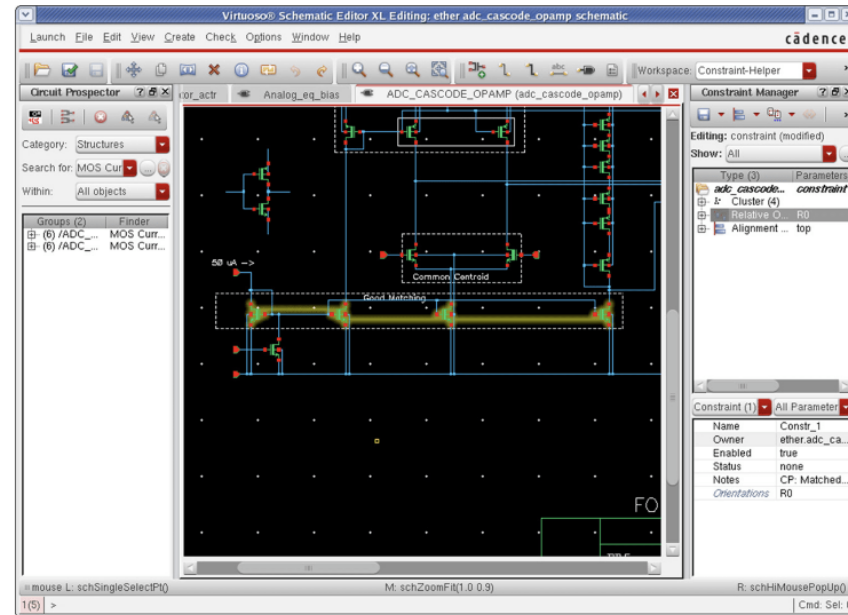


Figure 2: Virtuoso Schematic Editor XL common constraint environment

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.

[a-2] inputs the design data in storage;

As part of the specification inputting step, the computer upon which Spectre is installed inputs the design data in storage.

#### Design inputs

- ▶ OpenAccess database
- ▶ Verilog-AMS 2.0
- ▶ VHDL-AMS 1076.1
- ▶ Verilog (IEEE 1364-1995, IEEE 1364-2001 extensions)
- ▶ VHDL (IEEE 1076-1987, IEEE 1076-1993, IEEE 1076.4-2000 [VITAL 2000])
- ▶ Spectre and SPICE netlist formats
- ▶ SystemVerilog (IEEE 1800)
- ▶ Unified Power Format (UPF) or Common Power Format (CPF)

| US7603636                                                                                                                                 | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                           | <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| <p>[b-1] a property generating step that reads the design data generated at the specification inputting step from the storage and</p>     | <p>The computer upon which Spectre is installed executes a property generating step that reads the design data generated at the specification inputting step from the storage.</p> <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| <p>[b-2] generates a property which verifies the specification of the semiconductor integrated circuit using the read design data and</p> | <p>As part of the property generating step, the computer upon which Spectre is installed generates a property which verifies the specification of the semiconductor integrated circuit using the read design data. The Spectre AMS feature of "capturing design intent" or "capturing power intent" verifies the specification.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

| US7603636                                     | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                               | <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| [b-3] inputs the property in the storage; and | <p>As part of the property generating step, the computer upon which Spectre is installed inputs the property in the storage.</p> <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul>                                                                                                                                                                                                                                                                                                         |

| US7603636                                                                                                                                       | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                 | <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| <p>[c-1 ] an assertion generating step that reads the property generated at the property generating step from the storage and</p>               | <p>The computer upon which Spectre is installed executes an assertion generating step that reads the property generated at the property generating step from the storage. The Spectre AMS's assertions are generated from the properties that "captur[e] design intent" so that the assertions can be used to verify the design.</p> <ul style="list-style-type: none"> <li>▸ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▸ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Xcelium platform</p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| <p>[c-2] automatically converts the property into an assertion description if the property is to be verified during assertion verification,</p> | <p>As part of the assertion generating step, the computer upon which Spectre is installed automatically converts the property into an assertion description if the property is to be verified during assertion verification. The Spectre AMS's assertions are generated from the properties that "captur[e] design intent" so that the assertions can be used to verify the design.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

| US7603636                                                                                                                                                                                                                            | <b><u>Spectre Simulation Platform</u></b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                      | <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▶ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▶ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| [d-1] wherein the property generated by the property generating step is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data. | <p>Properties and assertions for describing the design include selection conditions with respect to state transitions, logic values, and signals in the design data.</p> <ul style="list-style-type: none"> <li>▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

| US7603636                                                                                       | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                 | <p>Xcelium platform</p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <p>14 [pre]. A manufacturing method of a semiconductor device, comprising:</p>                  | <p>To the extent the preamble is limiting, Spectre users perform a manufacturing method for manufacturing a semiconductor integrated circuit. Users produce and verify a semiconductor design using Spectre, and may direct a fab to perform the actual manufacturing steps.</p> <p>The Cadence® Spectre® AMS Designer provides an advanced mixed-signal simulation solution for the design and verification of analog, RF, memory, and mixed-signal silicon realization. It is integrated with the Cadence Virtuoso® full-custom environment as well as the Cadence Xcelium™ Parallel Logic Simulator. Spectre AMS Designer provides a single-simulation executable with flexible abstraction support through the standard mixed-signal languages (Verilog-AMS and VHDL-AMS), SystemVerilog, and/or SPICE-level models. As the bridge between the analog and digital domains, it enables users to choose the right analog solver for the right design or verification task. Designers can choose Spectre technologies for SPICE-accurate block-level analog and RF designs: Spectre Accelerated Parallel Simulator (APS), Spectre RF Option, Spectre X Simulator, and Spectre eXtensive Partitioning Simulator (XPS).</p> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 709.</p> |
| <p>[a] a designing step that designs an integrated circuit having a predetermined function;</p> | <p>Spectre users perform a designing step that designs an integrated circuit having a predetermined function.</p> <p>The Cadence® Spectre® AMS Designer provides an advanced mixed-signal simulation solution for the design and verification of analog, RF, memory, and mixed-signal silicon realization. It is integrated with the Cadence Virtuoso® full-custom environment as well as the Cadence Xcelium™ Parallel Logic Simulator. Spectre AMS Designer provides a single-simulation executable with flexible abstraction support through the standard mixed-signal languages (Verilog-AMS and VHDL-AMS), SystemVerilog, and/or SPICE-level models. As the bridge between the analog and digital domains, it enables users to choose the right analog solver for the right design or verification task. Designers can choose Spectre technologies for SPICE-accurate block-level analog and RF designs: Spectre Accelerated Parallel Simulator (APS), Spectre RF Option, Spectre X Simulator, and Spectre eXtensive Partitioning Simulator (XPS).</p> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 709.</p>                                                                                                                                                                |

| US7603636                                                                                                                                                                                                                                              | <u>Spectre Simulation Platform</u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                        | Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| [b] a simulating step that simulates the integrated circuit by using an assertion generated by an assertion generating method; and                                                                                                                     | <p>Spectre users perform a simulating step that simulates the integrated circuit by using an assertion generated by an assertion generating method.</p> <p>The Cadence® Spectre® AMS Designer provides an advanced mixed-signal simulation solution for the design and verification of analog, RF, memory, and mixed-signal silicon realization. It is integrated with the Cadence Virtuoso® full-custom environment as well as the Cadence Xcelium™ Parallel Logic Simulator. Spectre AMS Designer provides a single-simulation executable with flexible abstraction support through the standard mixed-signal languages (Verilog-AMS and VHDL-AMS), SystemVerilog, and/or SPICE-level models. As the bridge between the analog and digital domains, it enables users to choose the right analog solver for the right design or verification task. Designers can choose Spectre technologies for SPICE-accurate block-level analog and RF designs: Spectre Accelerated Parallel Simulator (APS), Spectre RF Option, Spectre X Simulator, and Spectre eXtensive Partitioning Simulator (XPS).</p> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 709.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| [c] a manufacturing step that manufactures a semiconductor device based on specifications of the integrated circuit, and                                                                                                                               | <p>Spectre users perform (or direct a foundry or fab to perform) a manufacturing step that manufactures a semiconductor device based on specifications of the integrated circuit.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| [d] wherein the assertion generating method comprises:                                                                                                                                                                                                 | Spectre users perform the assertion generating method, as described below.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| [d-1] a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations and inputs the design data in storage; | Spectre users perform a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations and inputs the design data in storage.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

| US7603636 | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|           | <div data-bbox="600 164 1197 509"><p data-bbox="621 175 926 207"><b>Spectre AMS Designer</b></p><div data-bbox="617 232 1180 316"><div data-bbox="617 232 888 316">Spectre simulation</div><div data-bbox="909 232 1180 316">Xcelium Parallel Logic Simulator</div></div><div data-bbox="611 354 865 402">Supports an analog-centric design flow</div><div data-bbox="888 354 1171 402">Supports a digital-centric design flow</div><div data-bbox="600 427 1197 509"><div data-bbox="600 427 888 509">Virtuoso ADE Product Suite</div><div data-bbox="909 427 1197 509">Debug suite</div></div></div> <p data-bbox="648 560 1178 583"><i>Figure 2: One simulator supports either verification flow</i></p> <p data-bbox="590 605 1190 631">SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 710.</p> <p data-bbox="596 649 1203 886">Spectre AMS Designer is tightly integrated with the Virtuoso ADE Product Suite for mixed-signal block design. It uses native Analog Design Environment netlisting technologies to combine schematics and behavioral views, enabling users to independently manage the level of abstraction of each block. The entire design is configured using the hierarchy editor, which facilitates the viewing and design preparation of a complex mixed-signal design.</p> <p data-bbox="590 904 1190 930">SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 710.</p> <p data-bbox="596 956 1434 1044">Virtuoso Schematic Editor L is the design intent environment of the industry standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed-signal design.</p> <p data-bbox="590 1065 1379 1091">SDT00000713-733, <a href="#">Virtuoso Schematic Editor L and XL Data Sheet</a>.</p> |

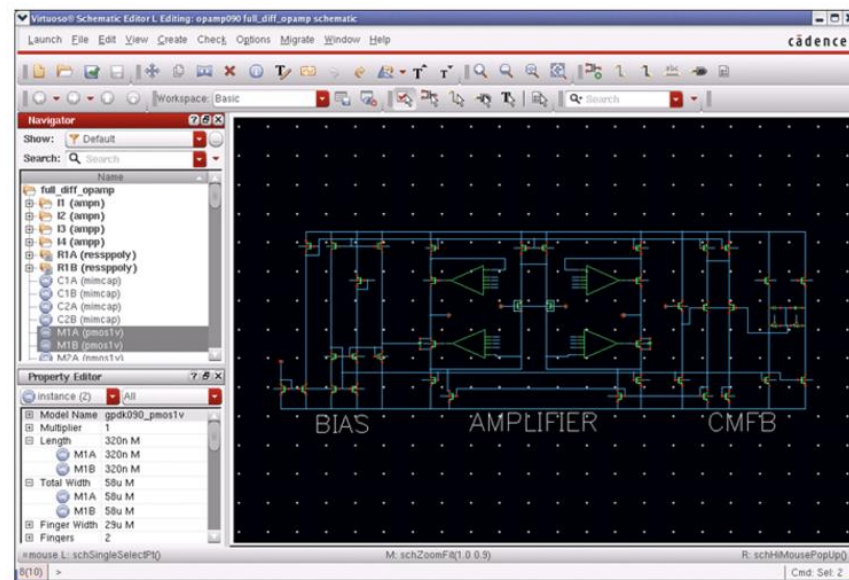


Figure 1: Virtuoso Schematic Editor L

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

Virtuoso Schematic Editor XL is the new design and constraint composition environment of the industry-standard Virtuoso custom design platform, the complete solution for front-to-back custom-analog, digital, RF, and mixed signal design.

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

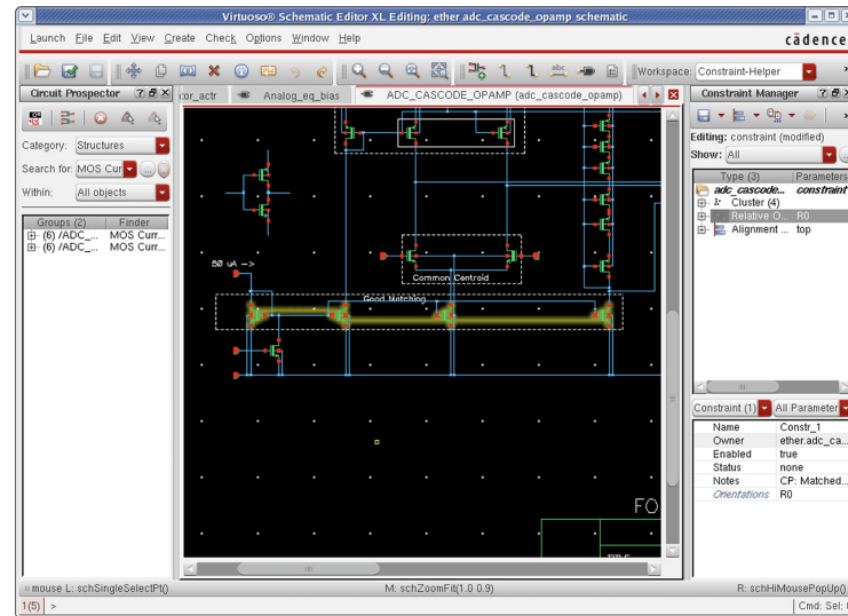


Figure 2: Virtuoso Schematic Editor XL common constraint environment

SDT00000713-733, [Virtuoso Schematic Editor L and XL Data Sheet](#).

Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.

[d-2] a property generating step that reads the design data generated at the specification inputting step from the storage and generates a property which verifies the specification of the semiconductor integrated circuit using the read design data and inputs the property in the storage; and

Spectre users perform a property generating step that reads the design data generated at the specification inputting step from the storage and generates a property which verifies the specification of the semiconductor integrated circuit using the read design data and inputs the property in the storage. The Spectre AMS feature of “capturing design intent” or “capturing power intent” verifies the specification.

- ▶ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.
- ▶ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting “PowerSmart” connect modules on key interfaces.

SDT00000709-712, [Spectre AMS Datasheet](#) at 711.

| US7603636                                                                                                                                                                                                                                                                   | Spectre Simulation Platform                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                                             | <p>Xcelium platform</p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <p>[d-3] an assertion generating step that reads the property generated at the property generating step from the storage and automatically converts the property into an assertion description if the property is to be verified during assertion verification, wherein</p> | <p>Spectre users perform an assertion generating step that reads the property generated at the property generating step from the storage and automatically converts the property into an assertion description if the property is to be verified during assertion verification. The Spectre AMS's assertions are generated from the properties that "captur[e] design intent" so that the assertions can be used to verify the design.</p> <ul style="list-style-type: none"> <li>▸ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▸ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Xcelium platform</p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |
| <p>[d-4] the property generated by the property generating step is a selection condition with respect to a state transition, a logic value of at least one</p>                                                                                                              | <p>With Spectre, the property generated by the property generating step is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

| US7603636                                                                   | <u>Spectre Simulation Platform</u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>or more signals, or at least one or more signals in the design data.</p> | <ul style="list-style-type: none"> <li>▸ Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.</li> <li>▸ Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p><b>Xcelium platform</b></p> <ul style="list-style-type: none"> <li>▸ SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)</li> <li>▸ Specman technology</li> </ul> <p>SDT00000709-712, <a href="#">Spectre AMS Datasheet</a> at 711.</p> <p>Cadence confidential information (e.g., product documentation, source code, etc.) may be necessary to describe functionality of the Accused Products fully and accurately with respect to this limitation and, accordingly, Plaintiff reserves the right to supplement these infringement contentions once such information is made available to Plaintiff.</p> |