

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE PATENT TRIAL AND APPEAL BOARD

---

CADENCE DESIGN SYSTEMS, INC.,  
Petitioner

v.

SEMICONDUCTOR DESIGN TECHNOLOGIES, LLC,  
Patent Owner

---

Case IPR2024-00356  
U.S. Patent No. 7,603,636

---

**DECLARATION OF JOHN E. BERG IN SUPPORT OF  
PATENT OWNER PRELIMINARY RESPONSE**

***Mail Stop "PATENT BOARD"***  
Patent Trial and Appeal Board  
U.S. Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

SDT EX2001  
Cadence Design Systems v. SDT  
IPR2024-00356

I, John Berg, declare:

**I. INTRODUCTION**

1. I have been retained by counsel for Patent Owner Semiconductor Design Technologies, LLC to provide opinions regarding the technology described in U.S. Patent No. 7,603,636 (“the ’636 patent”) and certain prior art references cited in connection with an IPR proceeding (IPR2024-00356) brought by Petitioner Cadence Design Systems, Inc., as outlined below.

2. I am being compensated at \$325 per hour. My compensation does not depend in any way on the outcome of this proceeding, my testimony, or opinions that I express.

3. In rendering my opinions, I considered the items discussed or listed herein, as well as my own knowledge and experiences in the field. My opinions here are limited to specific technical issues that are relevant in this preliminary stage of the proceeding. However, I reserve the right to amend or supplement my opinions in light of further documents, depositions, or discovery disclosures. I also reserve the right to submit an additional declaration in the event that the Board institutes review.<sup>1</sup>

---

<sup>1</sup> For purposes of this declaration, I have been asked to assume as true (1) the level of ordinary skill in the art proposed by Petitioner, *see* Pet., 11-12, and (2) the claim construction proposals suggested by Petitioner, *see* Pet., 12-14. I have not expressly taken any positions with respect to either issue, but reserve the right to do so in the event that the Board institutes review.

## **II. QUALIFICATIONS AND EXPERIENCE**

4. I am currently a consultant with Berg-Attenborough, Inc. I provide business, technical, and litigation advisory services to electronic and semiconductor companies. My experience includes 42 years of designing, fabricating, and selling semiconductor devices for leading semiconductor producers.

5. I received a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology in 1980. I then performed engineering and business graduate work in the fields of electrical engineering and management at Stanford University between 2002-2003.

6. From 1990 to 1998, I was Vice President of Technology Development at Zilog, Inc. (“Zilog”), a U.S. industry leader in semiconductor manufacturing. At Zilog, I managed both technology development and design teams that built Zilog’s then cutting-edge 200 mm wafer fabrication facility, designed Z8 microcontrollers, and engineered scaling of CMOS and embedded CMOS non-volatile memory technologies from 2 um to 0.25 um. Zilog built semiconductor products for commercial customers, industrial customers, and the U.S. Defense Department.

7. From 1998 to 2003, I was a Managing Director at Cypress Semiconductor (“Cypress”), where I managed a business unit that designed five new programmable logic chip product families. My work included designing,

fabricating, and selling programmable logic semiconductor devices in 250 nm, 180 nm, and 130 nm CMOS technologies. This included writing and reviewing circuit datasheets, and circuit specifications.

8. From 2003-2005, I developed automated manufacturing tools for the nano-imprint industry at Transfer Devices. This included specifying and ordering semiconductor products.

9. From 2005 to 2016, I was the Chief Technologist at American Semiconductor Inc. (“ASI”). At ASI, I developed and designed CMOS sensors and systems built using hybrid bonded wafers and multichip modules using 45 nm double-gate and 45 nm FINFET technology. My work included designing microcontrollers.

10. I am a named inventor on seventeen semiconductor-related patents issued by the United States Patent and Trademark Office:

| <b>U.S. Patent No.</b> | <b>Subject Matter</b>                                                                                            |
|------------------------|------------------------------------------------------------------------------------------------------------------|
| 8,913,402              | Triple-damascene interposer                                                                                      |
| 7,595,527              | Non-volatile electromechanical field effect devices and circuits using the same and methods of forming same      |
| 6,476,635              | Programmable number of metal lines and effective metal width along critical paths in a programmable logic device |
| 6,436,195              | Method of fabricating a MOS device                                                                               |
| 6,190,973              | Method of fabricating a high-quality thin oxide                                                                  |

| <b>U.S. Patent No.</b> | <b>Subject Matter</b>                                                                             |
|------------------------|---------------------------------------------------------------------------------------------------|
| 6,165,846              | Method of eliminating gate leakage in nitrogen annealed oxides                                    |
| 6,156,653              | Method of fabricating a MOS device                                                                |
| 5,978,127              | Light Phase Grating Device                                                                        |
| 5,631,180              | Method of fabricating high threshold metal oxide silicon read-only memory transistors             |
| 5,498,896              | High threshold metal oxide silicon read-only-memory transistors                                   |
| 5,389,565              | Method of fabricating high threshold metal oxide silicon read-only memory transistors             |
| 5,338,423              | Method of eliminating metal voiding in a titanium nitride/aluminum processing                     |
| 5,317,187              | Ti/TiN/Ti contact metallization                                                                   |
| 5,244,831              | Method of doping a polysilicon layer on a semiconductor wafer                                     |
| 5,240,880              | Ti/TiN/Ti contact metallization                                                                   |
| 4,895,520              | Method of fabricating a submicron silicon gate MOSFET, which has a self-aligned threshold implant |
| 4,824,803              | Multilayer metallization method for integrated circuits                                           |

11. A complete summary of my background, qualifications, and professional experience and affiliations is set forth in my curriculum vitae, which is attached as Appendix A.

### **III. THE '636 PATENT**

12. There are two important technical terms in the '636 patent which are not interchangeable: “properties” and “assertions.”

13. The '636 patent states:

The property to be discussed below is plain text that defines operations intended and expected in design data to be verified. For example, the property defines a relation between reception and response of a request signal and an approval signal in an arbiter circuit on time series constraint, and defines a regular state of the time series constraint and circuit specifications to be forbidden. In addition, the property is an event to be monitored as a function coverage point which confirms whether a specific circuit sequence has been tested by a simulation. Property verification verifies whether a design description satisfies a predetermined property.

EX1001, 1:19-29.

14. The '636 patent provides an example of how it extracts properties:

The syntax analyzer 203 analyses the circuit specification defined at the graphical editor 201 and the property extractor 204 extracts a property to be verified based on the design data. ...

EX1001, 8:16-20. Both a graphical user interface editor and an automated extraction system use the circuit specification to build the properties. Thus, properties are derived from specifications.

15. When validating the design of a complex, large-scale VLSI circuit, it is important to check “corner case(s)” and avoid “specification errors of a reusable core purchased from a third party.” EX1001, 1:34-45. Failing to do so can lead to problems such as “insufficient circuit verification or a test scenario that can extract

bugs,” which were well-known challenges in the industry at the time. EX1001, 1:41-45. As the ’636 patent states:

In order to solve these problems, an assertion verification technology, in which a property with respect to circuit specifications is converted into an assertion description and the assertion description is input to a simulator (computer) for verification, and a function coverage report for showing a warning for assertion violation during the simulation and showing whether a specific circuit sequence has been tested by a simulator is given, has been proposed and has been recently put into use in actual designing.

EX1001, 1:46-54.

16. An “assertion” in VLSI design is different than a property:

An assertion is a note in which intention (in some cases, this shows property) of designing is written and is generally written by a comment sentence in a RTL. The intention is interpreted by a simulator during the verification, for example, an error log is generated in a case where a circuit to be verified operates differently from the intention. The intention of designing is, for example, an assumption and a precondition of circuit input, and in addition to these, expected operations when the conditions are satisfied.

EX1001, 1:55-62.

17. In other words, properties are derived from the specification and are converted to assertions in standard VLSI designs. Properties and assertions are

different entities, both of which must be congruent with one another and the design specification. In fact, the '636 patent discloses an automated way of generating assertions from properties and the design specification: “The syntax analyzer 203 analyses the circuit specification defined at the graphical editor 201 and the property extractor 204 extracts a property to be verified based on the design data.” EX1001, 8:16-20. Both a graphical user interface editor and an automated extraction system use the circuit specification to build the properties.

#### **IV. GROUND 1 AND 4 (ABARBANEL + KOBAYASHI)**

18. Abarbanel uses RCTL language to specify properties. RCTL is an extension of the CTL (computational tree modeling) language that IBM used to define properties in its circuit designs:

The specification language RCTL, an extension of CTL, is defined by adding the power of regular expressions to CTL. In addition to being a more expressive and natural hardware specification language than CTL, a large family of RCTL formulas can be verified on-the-fly (during symbolic reachability analysis). On-the-fly model checking, as a powerful verification paradigm, is especially efficient when the specification is false and extremely efficient when the computation needed to get to a failing state is short. It is suitable for the inherently gradual design process since it detects a multitude of bugs at the early verification stages, and paves the way towards finding the more complex errors as the design matures. It is shown that for every erroneous finite computation, there is an RCTL formula that detects it

and can be verified on-the-fly. On-the-fly verification of RCTL formulas has moved model checking in IBM into a different class of designs inaccessible by prior techniques.

EX1023, Abstract.

19. Thus, RCTL is a modification of CTL that allows logic to be expressed as Boolean expressions. RCTL and CTL are different languages than Verilog and VHDL. Further, the prior art acknowledges that:

[a]nother major concern related to CTL model checking is the specification language. CTL is difficult to use for most users, and requires a new way of thinking about hardware design. The tree of computations is not a natural idea for most hardware designers which tend to think more in terms of a single computation. In addition, even the expert CTL user might have great difficulties expressing some properties in bare CTL.

EX1023, 1.

20. Abarbanel emphasizes the importance of and built its solution around the use of RCTL. Abarbanel emphasizes throughout its paper that RCTL provides a “conciseness,” “expressiveness,” and “ease of use” that is essential to Abarbanel’s verification solution:

- “RCTL includes a rich and useful set of CTL safety formulas and regular expressions.” EX1004, 1 n.1.

- “An equally important benefit of FoCs is the conciseness and expressiveness of RCTL formulas.” EX1004, 2.
- “The following example will demonstrate the conciseness and ease of use of RCTL for checker writing and the advantage of automatic checker generation.” EX1004, 3.
- “Thousands of FoCs checkers were written so far by virtue of the great ease of writing RCTL specifications and translating them into FoCs checkers.” EX1004, 4.
- “Our own experience has demonstrated that the simple, concise syntax and semantics of RCTL, coupled with online simulation checking, is highly useful to the verification teams with whom we work.” EX1004, 4.
- “In contrast [to Schlipf’s method that automatically translates state machines], our solution represents the specification as temporal logic formulas rather than state machines, for the sake of conciseness and readability.” EX1004, 5.

21. In other words, Abarbanel’s FoCs are designed specifically to process IC properties expressed in RCTL (and not in any other language or format) to harness the benefits that RCTL provides. Abarbanel does not simply treat RCTL as a convenient programming language that the authors just happened to select, but as an integral part of Abarbanel’s solution.

22. Abarbanel provides two examples of RCTL properties. The first property, “[i]f a transaction that starts with tag  $t$  has to send  $k$  bytes, then at the end of the transaction  $k$  bytes have been sent,” is expressed in RCTL as:

*forall k:* <sup>2</sup>  
 $\{*, start \ \& \ start\_tag=t \ \& \ to\_send=k, !end*, end \ \& \ end\_tag=t\} \rightarrow \{sent=k\}$

EX1004, 3. The second property, “a snoop event happens twice between read and write,” is expressed in RCTL as:

$\{*, read, \{!snoop*, snoop, !snoop*, snoop\} \ \& \ \{!write*\} \} \rightarrow \{cover\}$

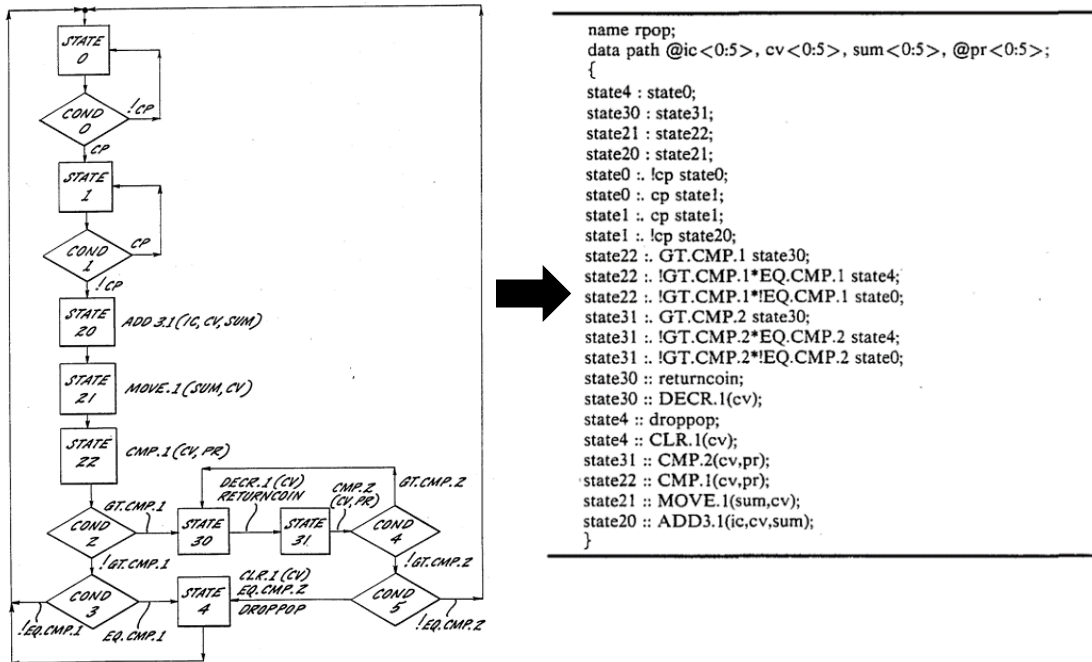
EX1004, 4.

23. Further, as Abarbanel makes clear, the implementation of the first example is “not trivial” and “involves spawning a new automation whenever a new value of  $k$  is encountered.” EX1004, 3, n.2.

24. Finally, Abarbanel discourages the use of state machine notation, in contrast to Schlipf and the ’636 patent: “[i]n contrast, our solution represents the specification as temporal logic formulas rather than state machines, for the sake of conciseness and readability.” EX1004, 5. Schlipf specifically uses finite-state machines: “We use only finite-state machine notation, which is familiar and intuitive to designers.” EX1029, 1.

25. Kobayashi’s “statelist” is “produced as output from the EDSIM program 20 and is used as an input to the PSCS program 30 (FIG. 3).” EX1005,

13:32-35. Kobayashi's statelist is a series of short, declarative statements that describe an IC's operational states, as well as conditions that trigger changes to such states.



EX1005, FIG. 10, 14:8-29.

26. Further, Kobayashi's "statelist" is "used by the PSCS program 30 to generate a netlist." EX1005, 7:2-3. As such, a POSA would understand the statelist as being the design itself, and the "statelist" contains state machines as Kobayashi uses the word "state" with "change" and "transition" throughout its disclosure. State conditions and state changes are terms frequently used to describe actions in a state machine. Thus, Kobayashi expresses state machines using its statelists.

27. To combine Kobayashi and Abarbanel, Kobayashi's statelist needs to be written in RCTL. Petitioner does not explain why or how a POSA would have

made the specific modification that Petitioner proposes (swapping Abarbanel's RCTL for Kobayashi's statelist/state machine), especially considering Abarbanel's emphasis on using RCTL and Abarbanel's discouraging state machine notation. To the extent Petitioner suggests translating Kobayashi's state machines into RCTL, Pet., 26-27, Petitioner fails to explain how or why that would have been accomplished.

28. RCTL and statelists are not interchangeable. Statelists identify states and state transitions, i.e., describe a state machine, whereas RCTL "includes a rich and useful set of CTL safety formulas and regular expressions." EX1004, 1 n.1. A POSA would not express a statelist in RCTL, especially because Abarbanel discourages state machine notation, nor would it be possible to use a statelist to characterize safety formulas and expressions as done in RCTL.

29. It would not be trivial to convert a statelist into RCTL. Most designers at the time had difficulty working with CTL and RCTL. In addition to dealing with the "for all k" property in RCTL and the exponential "spawning new automata" when a new "k" is created in Abarbanel's RCTL example, the prior art also mentions the designer's challenges as well: "However, CTL has one big drawback: although its syntax is very simple, its semantics are difficult to learn and master. Even an expert finds it difficult to understand formulas written by others." EX1024, 2.

30. Accordingly, modifying Abarbanel's FoCs to process a statelist, which is not written in RCTL, would eliminate the benefits that Abarbanel touts and is designed to achieve.

I declare under the penalty of perjury of the laws of the United States that the foregoing is true and correct. Executed in Palo Alto, California.

DATED: April 19, 2024

  
\_\_\_\_\_  
John Berg

22233261.1

# APPENDIX A

---

# JOHN BERG

---

• Palo Alto, California • 650.906.9657 • [johneberg2@gmail.com](mailto:johneberg2@gmail.com) •

---

## SUMMARY

As the Chief Technologist at American Semiconductor, Mr. Berg developed and designed CMOS sensors and systems built using bonded wafers and multichip modules using 45nm double-gate FET technology. Before joining ASI, Mr. Berg developed automated tools for the nano-imprint industry at Transfer Devices. Prior to Transfer Devices, Mr. Berg was a Managing Director at Cypress Semiconductor, where he managed a business unit that designed five new programmable logic chip product families in five years. Prior to Cypress, Mr. Berg was Vice President of Technology Development at Zilog, where he managed both technology development and design teams that built the company's 200mm wafer fabrication facility, designed Z8 microcontrollers, and engineered scaling of CMOS and embedded CMOS non-volatile memory technologies from 2um to 0.25um - the latter of which required co-development of CMP tools with the tool supplier. He received a Bachelor of Science degree in Physics from the Massachusetts Institute of Technology.

Mr. Berg has been an expert witness in semiconductor process development, silicon device physics, semiconductor design, CAD tools, lithography, semiconductor bonding including CMP, and business practices. He served as the plaintiff's expert witness in the Palmchip v. Ralink (Mediatek) microprocessor patent infringement. He was an expert witness for the plaintiff in Semi-Materials Co. Ltd. v. MEMC Pasadena Inc, in which he testified at jury trial twice and was deposed twice. In both cases, the plaintiff won, with more than \$19M being awarded to Mr. Berg's client. Mr. Berg also has testified in front of the US Patent Office in the re-examinations of three patents, all of which were successfully defended, and has been an expert in numerous IPR cases. He was deposed as a Cypress employee in Cypress Semiconductor v. Altera Corp., where Altera was sued for interference with contract, trade secret misappropriation, and unfair competition involving programmable logic devices. At Standard Microsystems, he did reverse engineering analysis on competitors' products; these analyses led to three successful licensing agreements with other semiconductor companies.

---

## PROFESSIONAL EXPERIENCE

### BERG-ATTENBOROUGH, INC.

SEPTEMBER 2010 - PRESENT

#### PRINCIPAL (2 EMPLOYEES)

Berg-Attenborough, Inc. is a consulting firm, which does technical consulting for Top 50 semiconductor companies and does expert witness work for patent and business issues.

#### *Key Achievements:*

- Developed wafer bonding and CMP for advanced photonics integrated circuit processing.
  - Fan-Out Wafer Level Packaging, FO-WLP consulting for Draper Laboratories
    - Successfully developed a 60+ chip multi-chip module including MPU, FPGA, DRAM, and FLASH.
    - Uncovered two temperature cycle reliability problems with the existing FO-WLP technology and instituted corrective actions to the process and design to eliminate these.
      - Modified interlayer dielectric and solder mask to correct die cracking
        - Problem uncovered by SEM and verified via SEM and reliability testing
      - Modified metal bus rules using Ansys and empirical data to ameliorate die cracking
-

## **PROFESSIONAL EXPERIENCE (CONT.)**

### **AMERICAN SEMICONDUCTOR, INCORPORATED**

**2005-2014**

#### **CHIEF TECHNOLOGIST (22 EMPLOYEES)**

American Semiconductor is fabricating radiation-hard CMOS products for military and aerospace customers.

##### ***Key Achievements:***

- Hands-on in-fab development the front-end & back-end full wafer scale process for an antenna array product, which resulted in a Top Supplier of the Year Award from Boeing. A low temperature substrate-to-substrate bonding technique was developed specifically for this product.
- Hands-on in-fab development of the company's double-gate FET process, and successful transfer of the company's double-gate FET CMOS process from university laboratory into a CMOS production facility. This included CMP, lithography, and etching processes.
- Design of MCU/analog RF/sensor/memory flexible system-on-chip reference products:
  - Products includes hardware and software/firmware for system control and security/encryption
  - Process development included direct low temperature and high temperature direct wafer-to-wafer bonding techniques with and without through silicon vias (TSV's) to reduce system form factor.
  - Flip-chip, ball-bond, and wire-bonding used to assemble product.

### **TRANSFER DEVICES, SANTA CLARA, CA**

**2004-2005**

#### **CHIEF OPERATING OFFICER (12 EMPLOYEES)**

Transfer Devices is a lithography start-up, which is commercializing technology developed in Professor Fabian Pease's laboratory at Stanford University.

##### ***Key Achievements:***

- Built a class 10 manufacturing clean room and delivered product to customers.
- Launched the ExaGlide 10r nano-patterning production tool development program
- Improved tool uptime from <10% to 95% and product yields from 50% to 99.9%

### **NANTERO, WOBURN, MA**

**2003-2004**

#### **VICE PRESIDENT, NEW PRODUCT DEVELOPMENT (50 EMPLOYEES)**

Nantero is developing non-volatile random-access memory using carbon nanotube switches.

##### ***Key Achievements:***

- Hired and led the design team that taped out a 4Mb non-volatile memory chip, which resulted in a radiation-hardened non-volatile memory technology.
-

## **PROFESSIONAL EXPERIENCE (CONT.)**

### **CYPRESS SEMICONDUCTOR, SAN JOSE, CA**

**1998-2002**

#### **MANAGING DIRECTOR, PROGRAMMABLE LOGIC (5500 EMPLOYEES)**

Cypress Semiconductor, a public company, is a broad line supplier of semiconductor components.

#### ***Key Achievements:***

- Program manager for Delta39K, 37K product lines, including hardware development, and software/firmware development on systems instantiated by customers.
- First Cypress multi-chip module product, using flip-chip and ball-bonding technologies.
- Hired, trained, and managed the ESD team at Cypress (3 technology and design engineers). Reduced the number of corporate ESD-related design errors from 50% to <5% by standardizing ESD design rules, testing and incorporating secondary breakdown into the ESD design, standardizing ESD design methodology, and instituting formal ESD design reviews into Cypress's design flow. Purchased test systems for in-house ESD testing.
- Integrated NAND FLASH IC and SRAM-based CPLD IC into 1<sup>st</sup> Cypress multichip module
- Developed and put into production the company's 0.25um BiCMOS and 0.18um SiGe HBT processes used for Datacommunications Products. Substantial materials and CMP work.
  - Provided PDK, CAD, and Device support.
- Increased revenues from \$38M to \$72M by increasing the number of PLD/FPGA product families to 6, including the Ultra37000, Delta39K, Quantum38K and PSI product families
- Designed CPLD products in TSMC's 0.13um technology which used copper interconnect.

### **ZILOG CORPORATION NAMPA, ID**

**1990-1998**

#### **VICE PRESIDENT, TECHNOLOGY DEVELOPMENT (1600 EMPLOYEES)**

Zilog was a pre-IPO company that successfully went public in 1991 and was later acquired by IXYS.

#### ***Key Achievements:***

- Trained and led the Nampa site's 15-person Design Department and 30-person Technology Development Department; delivered memory cells (SRAM, EEPROM, EPROM, NOR Flash), memory block compilers, and I/O cells for the company's design library for its system-on-chip and application-specific standard products.
  - Designed, built, and qualified the \$175M 200mm fabrication facility: 1<sup>st</sup> silicon yield.
    - 0.25um CMOS technology, including CMP, tungsten plugs, trench isolation, and low k dielectric. First dry-in/dry-out CMP metals and dielectric tools brought into production.
    - Solved the temperature cycle problem with the 200mm line within 90 days after initial observation. Solution involved modifying design rules for metallization and improved planarization.
  - Hired, trained, and led the design team that taped out 6 system-on-chip products per year for 8 years for the \$120M Z8 microcontroller business unit.
  - Worked with outside laboratories to ensure hardware design compliance to FCC's EMF/EMI requirements.
  - Modified design rules and design clocking scheme to improve 1<sup>st</sup> pass yields.
-

## **PROFESSIONAL EXPERIENCE (CONT.)**

**STANDARD MICROSYSTEMS CORPORATION, HAUPPAUGE, NY** **1980-1990**  
**ENGINEERING DIRECTOR (500 EMPLOYEES)**

Standard Microsystems was a public company in 1980, and later, was acquired by Microchip, Inc.

### ***Key Achievements:***

- Began career as a hands-on manufacturing CVD engineer working with Applied Materials deposition tools.
- Solved the company's Highly Accelerated Temperature/Humidity Stress Test (HAST) problem, that had been plaguing the company for five years, using optimizing thin film dopant concentration.
- Instituted DOE and six sigma process development practices in 1986.
- Hired, trained, and managed 26 sustaining and development engineers in the company's 2500 wpm wafer fab. Developed and transferred five 2um/sub-2um CMOS technologies into production.
- Reversed engineered Intel, TI, and National Semiconductor products to provide evidence of infringement against Standard Microsystem's patents. This included working with and coordinating external laboratories to provide deconstruction analysis.

---

## **EDUCATION**

|                  |                                                                                                                                 |                      |
|------------------|---------------------------------------------------------------------------------------------------------------------------------|----------------------|
| <b>2002-2003</b> | <b>STANFORD UNIVERSITY</b><br>M.S. Management, Graduate School of Business. Sloan Fellow.                                       | <b>PALO ALTO, CA</b> |
| <b>1998-2002</b> | <b>STANFORD UNIVERSITY</b><br>16 graduate credits in Electrical Engineering (GPA = 4.1) in circuit design                       | <b>PALO ALTO, CA</b> |
| <b>1975-1980</b> | <b>MASSACHUSETTS INSTITUTE OF TECHNOLOGY</b><br>BS Physics. Four-year National Merit Finalist and Scholar. Intercollegiate crew | <b>CAMBRIDGE, MA</b> |

---

## **PUBLICATIONS**

“MOS Transistor Technology from Planar to Nanowire Transistors,” Mantha, B. and Berg, J., Silicon Valley Engineering Council Journal, Volume 1, 2009, Pages 23-32.

“Substrate Bias Effects on Transiently Triggered Latchup in Bulk CMOS,” Chang, L. and Berg, J.; IEEE Transactions on Electron Devices, Volume 33, Issue 1, Jan. 1986 Pages 165 - 167

“A Derivative Method to Determine a MOSFET's Effective Channel Length and Width Electrically,” Chang, L. and Berg, J.; IEEE Electron Device Letters, Volume 7, Issue 4, Apr 1986 Pages 229 – 231.

“A Simplified Model to Predict the Linear Temperature Coefficient of a CMOS Inverter's Delay Time,” Chang, L., Khoa Vo and Berg, J.; IEEE Transactions on Electron Devices, Volume 34, Issue 8, Aug 1987 Pages 1834 – 1837.

---

## **CONFERENCE LEADERSHIP AND PRESENTATIONS**

Co-Chairman, 2007 IEEE San Francisco Bay Area Nanotechnology Symposium, July 2007.

“Rad-Hard Reconfigurable Bidirectional Level Shifter (ReBiLS) for NASA Space Applications in the Flexfet 0.18um SOI CMOS Technology,” K. DeGregorio, D. Wilson, S. Parke, J. Berg, M. Goldston, R. Hayhurst, D. Hackler 12th NASA Symposium on VLSI Design

Committee Member, Programmable Logic Sub-Committee, 2003 IEEE Solid State Circuits Conference, San Francisco, CA

“Measuring the Effective Channel Length of the Deep Submicron MOSFET and the Channel Broadening Effect,” S.H. Chung, Tim Carns, S.K. Lee, L. DeBruler, and J. Berg, Proceedings of the Thirteenth Biennial University/Government/Industry Symposium, IEEE Press, pp. 176-181, 1998.

---

### **PATENTS**

| <u>Patent Number</u> | <u>Title</u>                                                                                                     |
|----------------------|------------------------------------------------------------------------------------------------------------------|
| 8,913,402            | Triple-damascene interposer                                                                                      |
| 7,595,527            | Non-volatile electromechanical field effect devices and circuits and methods of forming same                     |
| 6,476,635            | Programmable number of metal lines and effective metal width along critical paths in a programmable logic device |
| 6,436,195            | Method of fabricating a MOS device                                                                               |
| 6,190,973            | Method of fabricating a high quality thin oxide                                                                  |
| 6,165,846            | Method of eliminating gate leakage in nitrogen annealed oxides                                                   |
| 6,156,653            | Method of fabricating a MOS device                                                                               |
| 5,978,127            | Light Phase Grating Device                                                                                       |
| 5,631,180            | Method of fabricating high threshold metal oxide silicon read-only-memory transistors                            |
| 5,498,896            | High threshold metal oxide silicon read-only-memory transistors                                                  |
| 5,389,565            | Method of fabricating high threshold metal oxide silicon read-only-memory transistors                            |
| 5,338,423            | Method of eliminating metal voiding in a titanium nitride/aluminum processing                                    |
| 5,317,187            | Ti/TiN/Ti contact metallization                                                                                  |
| 5,244,831            | Method of doping a polysilicon layer on a semiconductor wafer                                                    |
| 5,240,880            | Ti/TiN/Ti contact metallization                                                                                  |
| 4,895,520            | Method of fabricating a submicron silicon gate MOSFET, which has a self-aligned threshold implant                |
| 4,824,803            | Multilayer metallization method for integrated circuits                                                          |

---

### **PROFESSIONAL MEMBERSHIPS**

- National Science Foundation, Electronics & Nanotechnology Phase I & II SBIR Reviewer •
    - Gerson, Lehrman Group: Leader (Top 5%) Council member •
  - Chair Emeritus, and Founding Member, IEEE San Francisco Bay Area Nanotechnology Council •
    - IEEE National Chapter of the Year Award, 2013 •
    - Executive Committee Member, IEEE Santa Clara Valley Section •
    - Member, Silicon Valley Engineering Council Steering Committee •
      - Senior Member, IEEE •
      - Member, Sigma Xi •
    - Member, New York Academy of Science •
    - Chair, Vistage International 2010-2015 •
    - Security Clearance: Secret •
- 

### **SEMINARS, TUTORIALS & WORKSHOPS**

- ESD Association Tutorial: "Prevention of Electrostatic Discharge to Electronic Devices, Assemblies, and Systems." 1998 •
    - Juran Institute, "Juran Management Systems," 1989 •
-

**SOFTWARE**

**DESIGN TOOLS:**

**SYNOPSYS:** GALAXY DESIGN PLATFORM: DESIGN COMPILER, CUSTOM DESIGNER  
SE/DE/SDL, PRIMETIME, IC COMPILER, HSPICE, IC VALIDATOR, POWER  
COMPILER

**CADENCE:** AMS DESIGNER, ASSURA, SPECTRE, VIRTUOSO

**MENTOR GRAPHICS:** CALIBRE

**TCAD:**

**SILVACO:** ATHENA, ATLAS, VICTORY

**OTHER TOOLS:** VHDL, PYTHON, JSON, JMP, MATLAB, MICROSOFT OFFICE SUITE

---

**John Berg**  
Expert Witness History: 2010-2024  
[johneberg2@gmail.com](mailto:johneberg2@gmail.com)  
650-906-9657

- 2023** Steven A.W. De Jaray, Perienne De Jaray, and Darrell R. Oswald, Plaintiffs, v. Lattice Semiconductor Corporation, an Oregon- headquartered Delaware corporation, and John and Jane Does 1-20. Case No. #:19-cv-00086-SI.
- Expert Witness for De Jaray, Plaintiff
  - Two expert witness declarations written and submitted
  - Oral Deposition taken over four days.
  - Trial testimony given.
- 2021** Certain Semiconductor Devices, Wireless Infrastructure Equipment Containing the Same, and Components Thereof, ITC Inv. No. 337-TA-1254.
- Expert Witness for Ericsson, Defendant
  - Assisted counsel on invalidity contentions for the following patents: US Patent 9,018,697; US Patent 9,748,243; US Patent 9,761,719; US Patent 9,048,219
  - Assisted counsel on invalidity contentions for the following German patents: DE 20 2013 012 863 U1, and DE 11 2005 000 394 B4.
  - Worked with Ericsson in-house counsel and outside counsel in both U.S and Germany.
- 2020** Semiconductor Connections LLC v. Taiwan Semiconductor Manufacturing Company Limited & TSMC North America, No. 6:20-cv-109 (W.D. Texas)
- Expert Witness for TSMC, Defendant
  - Alleged patent infringement of US Patent 6,548,391
  - Assisted counsel in writing definitions for Markman hearing and writing invalidity contentions
- 2020** Taiwan Semiconductor Manufacturing Company, Limited ("TSMC") Matter Adverse to GlobalFoundries ("GFC")
- Provided technical information on advanced semiconductor processing to TSMC counsel.
- 2019** Samsung Electronics Co., LTD. v. Promos Technologies, Case IPR2019-00782
- Inter Partes Review of US 5,934,97
  - Expert Witness for Promos, Defendant
  - Technical expert witness declaration written and submitted
  - Oral Deposition taken

**John Berg**  
Expert Witness History: 2010-2024  
(cont.)

- 2019** Samsung Electronics Co., LTD. v. Promos Technologies, Case IPR2017-00032
- Inter Partes Review of US 6,099,386
  - Expert Witness for Promos, Defendant
  - Technical expert witness declaration written and submitted
  - Oral Deposition taken
- 2019** Micron Technology, Inc. v. United Microelectronics Corporation et al, No. 3:2017cv06932 - Document 139 (N.D. Cal.)
- Expert Witness for United Microelectronics Corporation, Defendant
  - Multiple technical expert witness declaration written on behalf of UMC.
- 2018** Shareholder Representatives Services, LLC v. Synaptics, Inc; JAMS Case No. 111001944
- Expert Witness for Synaptics, Defendant
  - Technical expert witness declaration written and submitted
- 2017** Home Semiconductor v. Samsung Electronics Co., Case :13-cv-02033-RGA
- Expert for Home Semiconductor, Plaintiff
  - Worked with Plaintiff Counsel on claim construction for multiple Samsung's processes to determine whether the Samsung processes infringe on Plaintiff's patent
- 2015** Palmchip, Inc. v. Ralink (Mediatek), Case number 112CV234653
- Plaintiff Witness in patent litigation suit
  - Three written Rule 132 declarations, Markman hearing and oral deposition; US District Court for the Southern District of California; settled prior to court date
- 2015** Unigen Corporation v. Nickel Electronics, LLC (a California LLC), Nickel Electronics, LLC (a Delaware LLC), and Robert Nicol
- Defendant Witness in trade secrets case
  - Two written Rule 132 declarations
- 2014** Ziptronix, Inc. v. Omnivision Technologies, Inc., Taiwan Semiconductor Manufacturing Company LTD., and TSMC North America Corp.,
- Expert Witness for TSMC
  - Six expert witness declarations written supporting IPR's for TSMC for six different Ziptronix wafer bonding patents. Patents involved in litigation, where TSMC was the Defendant.

**John Berg**  
Expert Witness History: 2010-2024  
(cont.)

- 2013** Ex Parte Re-examination: U.S. Patent 6,225,795
- Expert Witness for Volterra
  - Written expert witness declaration submitted
- 2011** Ex Parte Re-examination: U.S. Patent 7,405,443
- Expert Witness for Volterra
  - Written expert witness declaration submitted
  - Oral expert testimony on the stand in front of the 3-examiner tribunal at the USPTO in Arlington, Va.
- 2011** Ex Parte Re-examination: U.S. Patent 6,400,126
- Expert Witness for Volterra
  - Written expert witness declaration submitted
  - Oral expert testimony in front of a 3-examiner tribunal at the USPTO in Arlington Va.
- 2011** Ex Parte Re-examination: U.S. Patent 7,671,411
- Expert Witness for Volterra
  - Written Rule 132 declaration and oral expert testimony in front of a 3-examiner tribunal at the USPTO in Arlington Va.
- 2011** Semi-Materials Co., Ltd. v. MEMC Electronic Materials, Inc. et al. Case Number 4:06-cv-01426-FRB; Missouri Eastern District Court,
- Plaintiff Witness
  - Written declaration, oral deposition, and oral expert testimony on the witness stand in Federal District Court, Eastern District of Missouri
- 2010** Semi-Materials Co., Ltd. v. MEMC Electronic Materials, Inc. and MEMC Pasadena, Case number 4:08-cv-434 JCH, Missouri Eastern District Court,
- Plaintiff Witness
  - Written declaration, oral deposition, and oral expert testimony on the witness stand in Federal District Court, Eastern District of Missouri