

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CADENCE DESIGN SYSTEMS, INC.,
Petitioner,

v.

SEMICONDUCTOR DESIGN TECHNOLOGIES, LLC,
Patent Owner.

IPR2024-00356
Patent 7,603,636 B2

Before ST. JOHN COURTENAY III, GREGG I. ANDERSON, and
NATHAN A. ENGELS, *Administrative Patent Judges*.

ANDERSON, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Cadence Design Systems, Inc. (“Petitioner”) filed a Petition requesting *inter partes* review of claims 1–3, 7–10, and 13–14 (the “challenged claims”) of U.S. Patent No. 7,603,636 B2 (Ex. 1001, the “’636 patent”), Paper 1 (“Pet.”). Semiconductor Design Technologies, LLC (“Patent Owner”) filed a Patent Owner Preliminary Response. Paper 6 (“Prelim. Resp.”).

For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one claim. *See* 35 U.S.C. § 314(a) (*inter partes* review may not be instituted unless “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”). We therefore institute *inter partes* review as to all of the challenged claims of the ’636 patent and all of the asserted grounds of unpatentability. *See SAS Inst. Inc. v Iancu*, 138 S. Ct. 1348, 1356 (2018); 37 C.F.R. § 42.108 (a) (“When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”).

B. Related Proceedings

The parties identify the following district court proceeding involving the ’636 patent: *Semiconductor Design Technologies, LLC v. Cadence Design Systems, Inc.*, 3-23-cv-01001 (N.D. Cal.) (“District Court”). Pet. 84; Paper 4 (“Patent Owner’s Mandatory Notices”), 2.

C. Real Parties-in-Interest

Petitioner identifies itself, Cadence Design Systems, Inc., as the real party-in-interest. Pet. 84. Patent Owner identifies itself, Semiconductor Design Technologies, LLC, as the real party-in-interest. Paper 4, 1.

D. The '636 Patent

The '636 patent claims priority to an application that was filed under the Patent Cooperation Treaty on September 21, 2005. Ex. 1001 at code [22]. The '636 patent also claims priority to Japanese patent application JP 2004-286042 filed September 30, 2004. *Id.* at code [30].

1. Technical Background

The '636 patent relates to semiconductor technology for circuit verification in an LSI (large scale integration) circuit. Ex. 1001, 1:8–10. Verification is done to prevent design violation “by converting a property of a circuit to be verified into an assertion description and inputting the assertion description to a simulator when the design data of a circuit in a RTL (register transfer level) are dynamically verified by the simulator.” *Id.* at 1:10–16. An assertion generating system includes a program circuit verification “and an assertion generating method. *Id.* at 1:17–19.

“Property verification verifies whether a design description satisfies a predetermined property.” Ex. 1001, 1:28–29. A property “defines a relation between reception and response of a request signal and an approval signal in an arbiter circuit on time series constraint.” *Id.* at 1:22–24. A property also “defines a regular state of the time series constraint and circuit specifications to be forbidden.” *Id.* at 1:24–25. A property can be “an event to be

monitored as a function coverage point which confirms whether a specific circuit sequence has been tested by a simulation.” *Id.* at 1:26–29.

In assertion verification technology “a property with respect to circuit specifications is converted into an assertion description and the assertion description is input to a simulator (computer) for verification.” Ex. 1001, 1:46–49. A function coverage report shows a “warning for assertion violation during the simulation” and “whether a specific circuit sequence has been tested by a simulator is given, has been proposed and has been recently put into use in actual designing.” *Id.* at 1:50–54.

2. The Assertion Generation System of the '636 Patent

The problem the '636 patent attempts to solve is missing verification “due to the complexity of a circuit and an increase of circuit size of a semiconductor integrated circuit, by missing confirmation of interface specifications among blocks allocated to plural designers due to group work, or by specification errors of a reusable core purchased from a third party.” Ex. 1001, 1:34–40.

Figure 2 of the '636 patent is reproduced below.

FIG.2

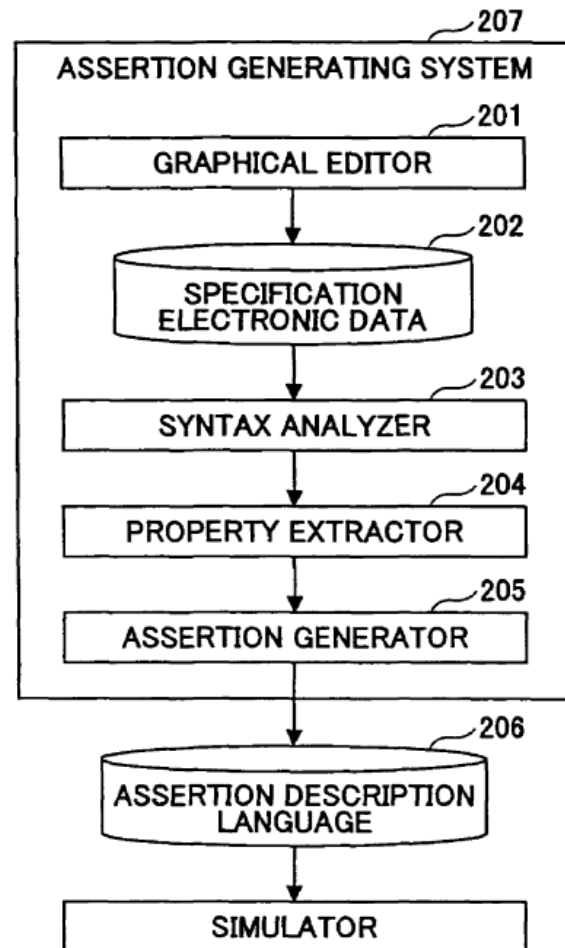


Figure 2 is a block diagram showing a first functional structure example of the assertion generating system and the circuit verifying system using the assertion generating system.

Ex. 1001, 6:1–3. As shown in Figure 2, “[a]n assertion generator 205 generates an assertion description language 206, which can be input to a simulator or a static property checker from the property extracted from the property extractor 204.” Ex. 1001, 7:65–8:1. “The assertion description language 206 generated in such a manner is stored in the storage 101 and is input to a simulator, and verification is executed.” *Id.* at 8:1–3.

The '636 patent thus describes an assertion generation system that includes a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations; a first storing unit that stores the design data generated by the specification inputting unit; a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data; a second storing unit that stores the property generated by the property generating unit; and an assertion generating unit that converts the property into an assertion description by reading the property generated by the property generating unit from the second storing unit. In addition, the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

Ex. 1001, 4:45–67.

E. Illustrative Claim

The Petition challenges claims 1–3, 7–10, 13, and 14, of which claims 1, 7, 8, and 14 are independent claims to, respectively, an assertion generating system, circuit verifying system, a computer readable medium, and manufacturing method. Claim 1 is illustrative of the claimed subject matter and reproduced below:

[1pre]¹ An assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit, comprising:

[1a] a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations;

[1b] a computer readable storage device having a first storing unit that stores the design data generated by the specification inputting unit;

[1c] a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;

[1d] a second storing unit that stores the property generated by the property generating unit, wherein the second storing unit may or may not be a part of the computer readable storage device; and

[1e] an assertion generating unit that automatically converts the property into an assertion description if the property is to be verified during assertion by reading the property generated by the property generating unit from the second storing unit, wherein

[1f] the property generated by the property generating unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

Ex. 1001, 13:29–57.

¹ Paragraph labeling in brackets is based on those provided by Petitioner. Pet. 87–93 (CLAIM APPENDIX).

F. References and Other Evidence

The Petition relies on the following references:

Name²	Reference	Copyright, Issue, or Publication Date	Exhibit(s)
Abarbanel	FoCs - Automatic Generation of Simulation Checkers from Formal Specifications, E.A. Emerson and A.P. Sistla (Eds.): CAV 2000, LNCS 1855, pp. 538-542	Copyright 2000	Ex. 1004
Kobayashi	U.S. Pat. 4,922,432	May 1, 1990	Ex. 1005
Narain	U.S. Pat. 6,651,228 B1	Nov. 18, 2003	Ex. 1006
Feyerabend	A Visual Formalism for Real Time Requirement Specifications. Pp. 156–168	1997 ³	Ex. 1007
McKeone	U.S. Pat. 6,957,413 B1	Oct. 18, 2005	Ex. 1008

Petitioner submits the Declaration of Soheil Ghiasi, Ph.D. Ex. 1003 (“Ghiasi Declaration”).

Patent Owner submits the Declaration of John E. Berg in Support of Patent Owner Preliminary Response. Ex. 2001 (“Berg Declaration”).

² First named author or inventor only.

³ Based on Ex. 1036 (“Declaration of Welmoed Spahr”), ¶¶ 1–9, 11–12; Ex. 1038 (“Declaration of Rachel J. Watters on Authentication of Publication”).

G. Asserted Grounds of Unpatentability

Petitioner asserts the challenged claims are unpatentable on the following grounds:

Grounds⁴	Claims Challenged	35 U.S.C. §⁵	References
1	1, 2, 7–9, 13	103	Abarbanel, Kobayashi
2	1, 2, 7–9, 13	103	Narain, Kobayashi
3	1, 3, 7, 8, 10, 13	103	Abarbanel, Feyerabend
4	14	103	Abarbanel, Kobayashi, McKeone
5	14	103	Narain, Kobayashi, McKeone
6	14	103	Abarbanel, Feyerabend, McKeone

See Pet. 5.

H. Overview of the Prior Art

1. Abarbanel (Ex. 1004)

Abarbanel addresses “the inefficient process of manual checker writing” by “automatically generating checkers from formal specifications.”

⁴ Grounds as listed at page 5 of the Petition.

⁵ Because the earliest application from which the ’895 patent claims priority was filed before March 16, 2013, the pre-AIA (“America Invents Act”) version of § 103 applies. Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011).

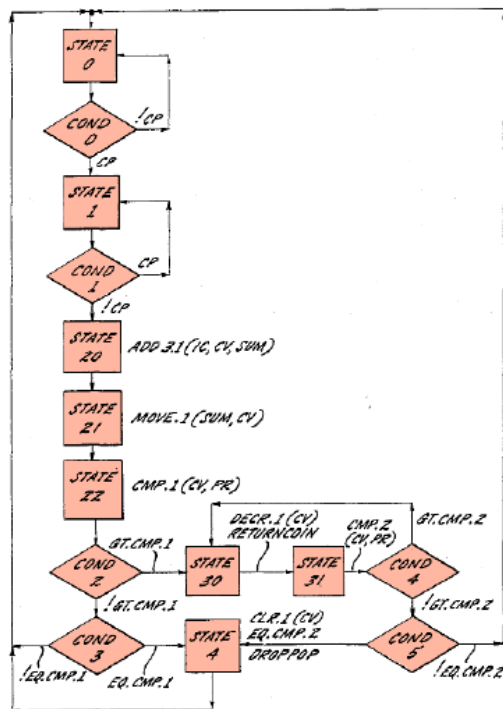
Ex. 1004, 538. Abarbanel takes RCTL^[6] properties as input and translates them into assertion descriptions (VHDL Checkers) for simulation and verification. *Id.* at 538–539. Abarbanel teaches translating properties into assertions for simulation/verification. *Id.* at 538.

2. Kobayashi (Ex. 1005)

Kobayashi generates a list of properties based on a flowchart. Ex. 1005, Abs., 6:68–7:3, 13:33–34. Kobayashi teaches IC design and verification. *Id.* at Abs. Kobayashi’s “EDSIM” program includes a “flowchart editor 21 for creating and editing flowcharts and a flowchart simulator 22 for simulation and verification of flowcharts.” *Id.* at 4:56–60. A PSCS (path synthesizer and cell selector) “generates a system controller, selects all other hardware cells, generates data and control paths, and generates a netlist describing all of this design information.” *Id.* at 4:63–64, 5:8–13.

In Appendix A, Kobayashi explains that the “EDSIM will generate an intermediate file, called a statelist, for each flowchart. Ex. 1005, 13:32–33. This file is then used by the PSCS program 30 to generate a netlist.” *Id.* at 7:2–3. Figure 10 of Kobayashi and an example of a statelist are reproduced below.

⁶ Regular CTL (RCTL) is a specification language which is an extension of the CTL programming language by adding the power of regular expression to CTL. Ex. 1023 (Beer, *On-the-Fly Model Checking of RCTL Formulas*, IBM Science and Technology, Haifa Research Laboratory), 185–186; *see also* Ex. 1003 ¶¶ 119–121 (CTL is “computational tree logic”).

~~Fig. 10.~~

```

name rpop;
data path @ic<0.5>, cv<0.5>, sum<0.5>, @pr<0.5>;
{
state4 : state0;
state30 : state31;
state21 : state22;
state20 : state21;
state0 :: lcp state0;
state0 :: cp state1;
state1 :: cp state1;
state1 :: lcp state20;
state22 :: GT.CMP.1 state30;
state22 :: !GT.CMP.1*EQ.CMP.1 state4;
state22 :: !GT.CMP.1*IEQ.CMP.1 state0;
state31 :: GT.CMP.2 state30;
state31 :: !GT.CMP.2*EQ.CMP.2 state4;
state31 :: !GT.CMP.2*IEQ.CMP.2 state0;
state30 :: returncoin;
state30 :: DECR.1(cv);
state4 :: droppop;
state4 :: CLR.1(cv);
state31 :: CMP.2(cv,pr);
state22 :: CMP.1(cv,pr);
state21 :: MOVE.1(sum,cv);
state20 :: ADD3.1(ic,cv,sum);
}

```

Side-by-side comparison of Kobayashi Figure 10 flowchart and statelist.

Id. at 14:8–29; *see also* Ex. 1003 ¶ 116 (reproducing above side-by-side comparison). The PSCS program generates the netlist defining “hardware components and their interconnection requirements. From this netlist the mask data for producing the integrated circuit can be directly produced using available VLSI CAD tools.” Ex. 1005, 14:1–6.

3. Narain (Ex.1006)

Narain’s verification methodology automatically translates express design intent (properties) into assertion descriptions to find design defects. Ex. 1006, Abs., 5:1–2, 9:55–11:43. With Narain’s teachings, “the designer is not required to manually code individual monitors for each property he/she would like to verify.” *Id.* at 3:15–28.

4. Feyerabend (Ex. 1007)

Feyerabend generates properties from timing waveform diagrams and translates them into formulas for verification. Ex.1007, 156–158.

Feyerabend teaches timing waveform diagrams and verification. *Id.* at 162.

5. McKeone (Ex. 1008)

McKeone teaches conventional semiconductor manufacturing. Ex. 1008, Abs. McKeone teaches IC manufacturing. *Id.* at 7:43–45, Fig. 4.

II. ANALYSIS OF THE CHALLENGED CLAIMS

A. Level of Ordinary Skill in the Art

Citing the Ghiasi Declaration, Petitioner contends a person of ordinary skill in the art of the '636 patent

would have a bachelor's degree in electrical engineering, computer engineering, computer science, or a similar field (collectively, the "Degree Areas") with at least two years of experience in IC design and verification, or a master's degree in the Degree Areas with a specialization in semiconductor IC design and verification. A person with less education but more relevant practical experience may also meet this standard. Pet. 11 (citing Ex. 1003 ¶¶ 56–57).

Further, a person of ordinary skill in the art would have had the knowledge to:

- Design, verify, and manufacture IC designs;
- Use known EDA design tools/techniques, including simulators and programming languages such as VHDL;
- Use known IC-verification tools/techniques, including assertion-based verification, in conjunction with known design techniques/tools;

- Use known tools/techniques for converting properties into assertion descriptions;
- Graphically edit specifications using known tools, e.g., Microsoft Visio or Excel.

Pet. 11–12 (citing Ex. 1003 ¶ 58).

Patent Owner does not propose a level of ordinary skill. *See* Prelim. Resp. Petitioner’s proposal is supported by the testimony of Dr. Ghiasi and is consistent with the ’636 patent. Accordingly, we apply Petitioner’s articulation of the level of ordinary skill in the art of the ’636 patent.

B. Claim Construction

We construe claim terms only as relevant to the parties’ contentions and only to the extent necessary to resolve the issues in dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner provides constructions for the following terms: “graphically editing” (Pet. 12–13); “property” (*id.* at 13); “a specification of the semiconductor” (*id.* at 13); “a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit” (*id.* at 13–14); and “assertion” (*id.* at 14). Patent Owner “disagrees with some of Petitioner’s claim-construction positions” but does not specify which ones. Prelim. Resp. 15. In addition to its unspecified disagreement, Patent Owner contends that its positions preclude institution even using Petitioner’s constructions. *Id.*

Based on the Preliminary Response, we have reviewed those terms which Patent Owner argues preclude institution and accordingly are in dispute. For Grounds 1, 2, 4, and 5, the first disputed term is the “property” limitation, which is present in all independent claims. *See* Prelim. Resp. 16 (Grounds 1 and 4), 31 (Grounds 2 and 5).

For Grounds 1 and 4, Patent Owner identifies the “property” limitation as disputed language in the independent claims. *Id.* at 16 (citing Ex. 1001, 13:40–44 (claim 1), 14:39–43 (claim 7), 15:4–8 (claim 8), 16:26–30 (claim 14)). The “property” limitation is in dispute for Grounds 2 and 5 for the “same reasons as Grounds 1 and 4.” *Id.* at 31–32.

For Grounds 3 and 6, the disputed term is the “graphically editing” limitation, which is present in in all independent claims. Prelim. Resp. 41. For Grounds 3 and 6, Patent Owner identifies the “graphically editing” limitation as disputed language in the independent claims. *Id.* (citing Ex. 1001, 13:34–35 (claim 1), 14:33–34 (claim 7), 14:67–15:1 (claim 8), 16:23–24 (claim 14)).

Patent Owner disputes Petitioner’s showing regarding limitation 1c. *See* Section II.D.2.a below. In doing so, Patent Owner argues the construction of “verify” based on the specification. Prelim. Resp. 17. The term “verification of a semiconductor integrated circuit” appears in the preamble, which we find is limiting based on Patent Owner’s argument. *Id.*

Based on the current record in this preceding, we preliminarily construe only the “property,” “graphically editing,” and “verify/verification” limitations. During trial, additional terms may require construction. The parties are cautioned to construe any additional term(s) prior to the final hearing in order to prevent waiver of any argument based on construction.

1. “*property*” limitation (claims 1, 7, 8, and 14)

The entire “property” limitation for claim 1 recites

a *property* generating unit that generates a *property* which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data.⁷

Ex. 1001, 13:40–44 (emphasis added).

Petitioner points to the ’636 patent as defining “‘property’ as ‘plain text that defines operations intended and expected in design data to be verified.’” Pet. 13 (citing Ex. 1001, 1:20–22; Ex. 1003 ¶ 70). We preliminarily adopt Petitioner’s construction, to which Patent Owner does not respond, for purposes of this decision.

2. “*graphically editing*” limitation (claims 1, 7, 8, and 14)

The entire “graphically editing” limitation for claim 1 recites

graphically editing the specification of the semiconductor integrated circuit based on user operations.⁸

Ex. 1001, 13:34–36 (emphasis added).

Petitioner proposes that “graphically editing” be construed as “editing with a graphical user interface (‘GUI’).” Pet. 13. Petitioner cites to intrinsic

⁷ The “property” limitation reproduced here for claim 1 is identically recited in independent claim 7 and similarly, but not identically, recited in independent claims 8 and 14. *See* Ex. 1001, 13:40–44 (claim 1), 14:39–43 (claim 7), 15:4–8 (claim 8), 16:26–30 (claim 14).

⁸ The “graphically editing” limitation reproduced here for claim 1 is identically recited in independent claims 7, 8, and 14. *See* Ex. 1001, 13:34–35 (claim 1), 14:33–34 (claim 7), 14:67–15:1 (claim 8), 16:23–24 (claim 14).

evidence of the '636 patent Specification indicating the term is a “visual expression.” Pet. 12–13 (citing Ex. 1001, Abs., 4:39–44, 3:64–65, 6:60–62, 7:51–60, 8:30–36, Figs. 2, 4–5). Petitioner also cites extrinsic evidence for support. *Id.* at 12 (citing Ex. 1039⁹; Ex. 1003 ¶¶ 65–66; Ex. 1031¹⁰; Ex. 1032¹¹).

We preliminarily adopt Petitioner’s construction, to which Patent Owner does not respond, for purposes of this decision.

3. “*verifies*” (*claims 1, 7, 8, and 14*)

Patent Owner contends “[i]n the context of the '636 patent, ‘verify^[12] means that the claimed property is used to troubleshoot an IC—i.e., to ensure that the IC functions in a manner described in its specification.” Prelim. Resp. 17 (citing Ex 1001, 1:8–19, 1:28–29, 4:35–38, 5:30–56, 7:61–64, 8:4–20). We do not conclude that “verifies” is as limited as Patent Owner proposes.

The '636 patent describes “a property extractor 204 generate[s] a property that *verifies the specification* of the semiconductor integrated circuit *based on the design data*.” Ex. 1001, Abs. (emphasis added). Thus, verification verifies the design to insure the “design description satisfies a

⁹ VisiCalc Page Vault December 21, 2023.

¹⁰ Petitioner’s “Preliminary Proposed Claim Constructions and Preliminary Identification of Evidence” in District Court.

¹¹ Patent Owner’s “Disclosure of Preliminary Claim Constructions and Extrinsic Evidence” in District Court.

¹² Claim 1 recites as part of the “property” limitation “verifies the specification of the semiconductor integrated circuit,” which is identically recited in independent claims 1, 7, 8, and 14. *See* Ex. 1001, 13:41–42 (claim 1), 14:40–41 (claim 7), 14:61–15:18 (claim 8), 16:28–29 (claim 14).

predetermined property.” *Id.* at 1:29–30. Patent Owner’s citations to the ’636 patent also establish verification is dependent on the design. Prelim. Resp. 17 (citing Ex. 1001, 1:8–19, 1:28–29, 4:35–38, 5:30–56, 7:61–64, 8:4–20).

Based on the preceding we preliminarily determine that “verifies” means “verification of the design of the integrated circuit.”

4. Remaining Terms

Unless otherwise indicated in this Decision, we do not expressly construe any remaining claim term and apply the plain and ordinary meaning to a person of ordinary skill in the art.

C. Obviousness

A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called “secondary considerations,” including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). At this stage, neither party has presented any evidence on the fourth *Graham* factor.

D. Claims 1, 2, 7–9, and 13 as Obvious Over Abarbanel and Kobayashi

Petitioner asserts that the combination of Abarbanel and Kobayashi discloses or teaches or suggests each limitation of claims 1, 2, 7–9, and 13 and provides a limitation-by-limitation analysis. Pet. 5, 14–41; Ex. 1003 ¶¶ 79–96. Patent Owner disputes that any claim is unpatentable based on Abarbanel and Kobayashi. Prelim. Resp. 16–31.

1. Reasons to Combine Abarbanel and Kobayashi

Petitioner’s rationale for combining Abarbanel and Kobayashi first summarizes Abarbanel as teaching

a Formal Checkers (“FoCs”) methodology/tool that takes properties of a specification and “translates them into VHDL programs (‘checkers’)” for simulation and verification. [] Abarbanel improved on “the inefficient process of manual checker writing” by “automatically generating checkers from formal specifications,” referring to a file that lists properties for verification. [] “For each property of the specification, represented as an RCTL formula, FoCs generates a checker for simulation.”

Pet. 14 (citing Ex. 1004, 538; Ex. 1003 ¶¶ 80–81); *see also* Ex. 2001 ¶¶ 18–19 (RCTL is used to “define properties in [IBM] circuit designs” and citing Exhibit 1023).

Petitioner further contends that because “an IC project and formulate properties of the intended design, it was common for engineers to use graphical representations of specifications, for example flowcharts that described IC requirements.” Pet. 14–15 (citing Ex. 1019,¹³ 1:13–16;

¹³ Saltou, US Pat. 7,046,246 B2, issued May 16, 2006.

Ex. 1016¹⁴ ¶¶ 7, 44; Ex. 1018,¹⁵ 29:8–11; Ex. 1021,¹⁶ 33:11–15; Ex. 1017¹⁷ ¶ 101; Ex. 1020,¹⁸ 1:14–26). Based on the preceding, Petitioner contends “[t]herefore, the prior art provides motivation to combine Abarbanel with teachings for graphically editing IC specifications, including flowcharts.” *Id.* at 15 (citing Ex. 1003 ¶ 82).

Petitioner cites to Kobayashi as teaching “a graphical flowchart editor for representing IC design requirements in a specification.” Pet. 15 (citing Ex. 1005, 2:24–57, 4:11–38). Kobayashi is further cited as “generating a statelist, and verifying the specification.” *Id.* (citing Ex. 1005, Abs., 1:51–54, 4:56–5:68, 6:57–7:58, Fig. 3). Petitioner concludes that a person of ordinary skill in the art

would have been motivated to combine these teachings from Abarbanel and Kobayashi, as a combination of prior art elements according to known techniques because Kobayashi teaches a graphically-edited specification and automatically-generated properties, while Abarbanel takes properties as input to generate checkers for verification. [] Graphically editing specifications was one of a finite number of identified predictable solutions, which Kobayashi teaches.

Pet. 15 (citing Ex. 1003 ¶¶ 82–84).

Petitioner cites additional motivation. Pet. 15–16. More specifically Petitioner alleges that a person of ordinary skill in the art “would naturally have looked to teachings of similar references in a combination that

¹⁴ Devine, US 2003/0217190 A1, published Nov. 20, 2003.

¹⁵ Rice, US Pat. 7,424,543 B2, issued Sept. 9, 2008.

¹⁶ Weise, US Pat. 7,631,255 B2, issued Dec. 8, 2009.

¹⁷ Hutten, US 2006/0047540 A1, published Mar. 2, 2006.

¹⁸ Schorr, US Pat. 7,944,445 B1, issued May 17, 2011.

facilitates their stated purposes—to simplify IC design by defining functional requirements ‘using an easily understood architecture’ without the need for manually writing checkers.” *Id.* (citing Ex. 1005, 2:6–20; Ex. 1003 ¶¶ 85–86).

Other reasons for the combination are also cited by Petitioner, including the need for improvement and that Kobayashi teaches “known techniques” and Abarbanel involves application of “known methodology” to achieve a predictable result. Pet. 16 (citing Ex. 1004, 538, 540—542; Ex. 1003 ¶ 86). Petitioner further notes that the combination is a substitution of a known element, Kobayashi’s statelist, i.e., a state machine, where Abarbanel discloses RCTL which describes state machines. *Id.* at 16 (citing Ex. 1003 ¶ 88). Finally, according to Petitioner, combining the references to Abarbanel and would have a reasonable expectation of success. *Id.* at 17–18 (citing Ex. 1003 ¶ 91).

Patent Owner contends that a person of ordinary skill in the art would not combine Kobayashi with Abarbanel. Prelim. Resp. 18–31. Patent Owner argues the reasons for combining Kobayashi with Abarbanel are “unclear and confusing.” *Id.* at 19–20. Specifically, Patent Owner argues Petitioner’s first theory alleges Kobayashi’s statelist would have been input to Abarbanel’s methodology. *Id.* at 20. According to Patent Owner, this combination is first alleged by Petitioner to substitute one known element for another to obtain a predictable result and would apply “Kobayashi’s known techniques to Abarbanel’s known methodology, which was ready for improvement.” *Id.* (citing Pet. 16, 17, 29).

Patent Owner argues the preceding is in conflict with Petitioner’s second combination argument based on modifying Kobayashi’s statelist into

RCTL code as taught by Abarbanel. *Id.* at 20–21 (citing Pet. 16, 26, 27). Patent Owner argues the “second theory of obviousness is predicated on Petitioner’s contention that a [person of ordinary skill in the art] would have improved *Kobayashi*’s system based on *Abarbanel*’s teachings—i.e., the exact opposite premise on which the first theory is based.” *Id.* at 21 (quoting Pet. 16 (“[A] POSITA would have been motivated to make this straightforward combination because *Kobayashi*’s teachings were ready for improvement.”)). Patent Owner concludes that “Petitioner does not clearly adopt one or the other, nor present them as alternative theories.” *Id.*

Patent Owner asserts there are technical differences between Abarbanel and Kobayashi which make the combination problematic to a person of ordinary skill in the art. Prelim. Resp. 22–28. Specifically, it is argued by Patent Owner that “Abarbanel is predicated on using RCTL, *not* statelists.” *Id.* at 22. Patent Owner highlights Abarbanel uses RCTL to express IC properties. *Id.* at 24–25; *see also* Ex. 2001 ¶¶ 20–24 (explaining Abarbanel’s use of RCTL). Patent Owner argues RCTL is not a substitute for state machines, such as described in Kobayashi. *Id.* at 26 n.2. In conclusion, Patent Owner contends “converting statelists into RCTL ‘is *not* trivial,’ at least in some cases.” *Id.* at 27 (citing Ex. 1004, 3 n.2; Ex. 2001 ¶¶ 23, 29).

On this record, we determine Petitioner has adequately shown reasons for combining Abarbanel and Kobayashi for purposes of institution. We do question whether after a trial the combination will meet the preponderance of the evidence burden applied to final written decisions.

We are not convinced that the lack of clarity is so compelling that we cannot decipher how the Petitioner asserts why a person of ordinary skill in

the art would have combined Abarbanel and Kobayashi. Any one of the arguments made by Petitioner is sufficient at this stage, even if Petitioner presents contradictory alternatives. At this stage of the proceeding, alternative inconsistent theories for combining the references are permissible.

We leave for trial the question whether or not Abarbanel's RCTL technology would have been combinable with the state machine/statelist technology of Kobayashi. However, on this record, and giving weight to the Ghiasi Declaration, Petitioner sufficiently supports its assertion that a person of ordinary skill in the art "would have been motivated to combine Abarbanel with teachings for graphically editing IC specifications, including flowcharts, because the prior art is replete with teaching, suggestion, and motivation to do so." Ex. 1003 ¶¶ 81–85. Furthermore, Abarbanel suggests related work involves "simulation efforts" with "automatically translating state machines." Ex. 1003 ¶ 122 (quoting Ex. 1004, 542).

In making this preliminary determination, we also note that Patent Owner's argument that Abarbanel is limited to RCTL and thus would not have been combined with Kobayashi, is essentially an argument that the two cannot be physically combined. The criterion is not whether the references could be physically combined but whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole. *Orthopedic Equipment Co. v. United States*, 702 F.2d 1005, 1013 (Fed. Cir. 1983).

On this record, we preliminarily determine Petitioner has sufficiently shown a rationale for combining Abarbanel and Kobayashi.

2. *Claim 1*

Patent Owner disputes only Petitioner's showing as to limitation 1c based on Kobayashi. Prelim. Resp. 16–18. We have reviewed Petitioner's showing for the remaining limitations and find the showing sufficient for those limitations. Our analysis of limitation 1c is below.

a. Limitation 1c

Limitation 1c recites in its entirety “a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data,” the “property” limitation.

Petitioner asserts that Kobayashi's “EDSIM” program is “a property generating unit that generates a property” by disclosing “generating a statelist, and verifying the specification.” Pet. 25 (citing Pet. 15 (citing Ex. 1005, Abs., 1:51–54, 4:56–5:68, 6:57–7:58, Fig. 3)). Petitioner states that the EDSIM program “will generate an intermediate file, called a statelist, for each flowchart.” *Id.* (citing Ex. 1005, 7:1–3, Fig. 10); Ex. 1003 ¶ 116.

Petitioner argues each entry in Kobayashi's statelist is a property that “defines operations intended and expected in design data to be verified, including when and under what conditions states will transition in the flowchart.” Pet. 26; *see also* Section I.H.2 above (comparing Kobayashi Figure 10 and example statelist). Similarly, Petitioner points to Abarbanel as suggesting “using RCTL to describe state machines.” *Id.* (citing Ex. 1004, 542).

Petitioner argues that the portion of the “property” limitation reciting that each “property **verifies the specification of the semiconductor integrated circuit**” is taught by Kobayashi’s flowchart, which is the specification. Pet. 28 (citing Pet. 19–24 (showing for limitation 1a)). Petitioner cites to Kobayashi’s teaching of “simulation and *verification of flowcharts*.” *Id.* (citing Ex. 1005, 4:56–60).

Petitioner’s showing for the “reading the design data generated by the specification inputting unit from the first storing unit and using the read design data” recitation of the “property” limitation is based on Kobayashi’s teachings that “‘flowchart’ ‘design data’ is stored in main memory.” Pet. 29–30 (citing Ex. 1005, 5:64–66). Petitioner then cites to Kobayashi’s teaching that a “CPU creates and uses the flowchart data to generate the statelist.” *Id.* at 30 (citing Ex. 1005, 7:1–3). According to Petitioner, this means the “CPU needs to read and write the flowchart design data from main memory so it can be used.” *Id.* (citing Ex-1005, 7:1–3, 5:49–68; Ex. 1003 ¶ 129).

Patent Owner disputes that the “property” limitation has been shown. Prelim. Resp. 16–18. Patent Owner specifically disputes Petitioner’s argument that “Kobayashi’s ‘flowchart’ (i.e., a graphical representation of transitions between IC states) corresponds to the claimed specification, and that Kobayashi’s ‘statelist’ (i.e., a textual description of the various states depicted in the flowchart) comprises a list of claimed properties.” *Id.* at 16 (citing Pet. 28–29). Relying on its proposed construction of “verify,” Patent Owner contends Petitioner is wrong because “Kobayashi’s statelist (the alleged list of properties) is not used to ‘verify’ Kobayashi’s flowchart (the

alleged specification), as the claims require.” *Id.* at 16–17; *see* Section II.B.3 above (rejecting Patent Owner’s proposed construction).

Petitioner cites to Kobayashi’s appendix (*see* Section I.H.2 above), and argues

each substantive line is an entry. Each entry is a **property**, as each is plain text that defines operations intended and expected in design data to be verified, including when and under what conditions states will transition in the flowchart.

Pet. 26 (citing Ex. 1005, 12:64–13:1). Petitioner then argues Kobayashi’s statelist contains “language to represent actions and conditions in a flowchart.” *Id.* (citing Ex. 1005, 9:8–13, Fig. 9; Ex. 1003 ¶ 117).

We are not persuaded that “verify” means that “the claimed property is used to troubleshoot an IC—i.e., to ensure that the IC functions in a manner described in its specification.” Prelim. Resp. 17.

For the reasons stated in Section II.B.3 above, we preliminarily determine that “verifies” means “verification of the design of the integrated circuit.” Kobayashi teaches “simulation and ***verification of flowcharts.***” Ex. 1005, 4:56–60. Kobayashi’s statelist uses simulation to check that the flowchart and implementation are consistent. Ex. 1004, 538–539. On this record, we agree with Petitioner that a “statelist is a language representation of the flowchart and provides the properties that the implementation must be designed to meet; *an error indicates that the design did not work as described by the flowchart.*” Pet. 28–29 (citing Ex. 1004, 538–539; Ex. 1003 ¶¶ 126–127) (emphasis added). “Abarbanel uses simulation to verify that the properties (written as assertion descriptions) are consistent with the design.” *Id.* at 29 (citing Ex. 1004, Fig. 1). The preceding meets our preliminary construction of “verifies.”

On this record, Petitioner has sufficiently shown the combination of Abarbanel and Kobayashi teaches limitation 1c.

3. Independent Claims 7 and 8

Petitioner's analysis of claims 7 and 8 incorporates much of its analysis of claim 1. Pet. 34–35 (claim 7), 36–39 (claim 8). Patent Owner does not provide any separate arguments relating to claims 7 or 8.

On this record, and for the reasons stated for claim 1, Petitioner has sufficiently shown the combination of Abarbanel and Kobayashi teaches the limitations of claims 7 and 8.

4. Dependent Claims 2, 9, and 13

Claim 2 depends from claim 1, and claims 9 and 13 depend from claim 8. Patent Owner does not separately argue for the patentability of claims 2, 9, or 13.

We have reviewed Petitioner's showing for claims 2, 9, and 13. On this record, we find Petitioner has sufficiently shown the additional limitations of the dependent claims. *See* Pet. 33–34 (claim 2), 39–40 (claim 9), 40–41 (claim 13).

5. Summary

Petitioner has shown a reasonable likelihood that claims 1–2, 7–9, and 13 would have been obvious over Abarbanel and Kobayashi.

E. Claims 1, 2, 7–9, and 13 as Obvious Over Narain and Kobayashi

A decision to institute under § 314 may not institute on fewer than all claims challenged in the petition. *SAS*, 138 S. Ct. at 1359–60. In addition, per Board practice, if the Board institutes trial, it will institute “on all of the

challenged claims and on all grounds of unpatentability asserted for each claim.” *See* 37 C.F.R. § 42.108(a) (2023). Accordingly, as to this and all remaining grounds we institute *inter partes* review. *See* Sections II.D.1, 2, 3, 4 above.

Specific to this ground, Petitioner asserts that Narain and Kobayashi teach each limitation of claims 1, 2, 7–9, and 13 and provides a limitation-by-limitation analysis for each. Pet. 41–59; Ex. 1003 ¶¶ 184–276.

*1. Claims 1, 7, and 8*¹⁹

Petitioner contends that a person of ordinary skill would have been motivated to combine Narain and Kobayashi because “Narain teaches an Intent-Driven Verification architecture that automatically generated assertions from a control file containing express design intent.” Pet. 41 (citing Ex. 1006, 9:55–59, 10:21:25, Fig. 1; Ex. 1003 ¶¶ 184–185). Petitioner then alleges “Kobayashi teaches an automatically-created control file, called a statelist, that lists the express intent of the design.” *Id.* (citing Ex. 1005, 7:1–3, 8:56–10:1, 13:32–35). Relying on the Ghiasi Declaration, Petitioner alleges “[t]his was a combination of prior art elements according to known techniques with predictable results” and that “[t]his was one of a finite number of known, predictable solutions for editing a specification.” *Id.* at 42 (citing Ex. 1003 ¶¶ 186–189).

¹⁹ As it did with the challenge based on Abarbanel and Koyabashi, Petitioner’s showing for claims 7 and 8 relies on the showing for claim 1. *See* Pet. 55–56 (claim 7), 57–59 (claim 8). For purposes of this Decision, we reference claim 1 unless otherwise indicated.

Patent Owner disputes that there is sufficient rationale to combine Kobayashi with Narain. Prelim. Resp. 39–41. Patent Owner repeats many of the arguments made against the combination of Abarbanel and Kobayashi above. *Id.*

On this record, and for some of the same reasons stated above in Section II.D.1, we are persuaded that Petitioner has sufficiently shown a rationale for the combination of Narain and Kobayashi.

Patent Owner also disputes that Narain shows the “property” limitation. Prelim. Resp. 32–38. Although Petitioner does contend Narain teaches the “property” limitation (Pet. 48), Petitioner first relies on Kobayashi as analyzed above in Section II.D.2.a. Pet. 48.

On this record, and, in part, based on the prior showing regarding limitation 1c based on Kobayashi and for reasons stated in the Ghiasi Declaration summarized above, Petitioner has sufficiently shown Kobayashi teaches limitation 1c.

2. Dependent Claims 2, 9, and 13

Claim 2 depends from claim 1, and claims 9 and 13 depend from claim 8. Patent Owner does not separately argue for the patentability of claims 2, 9, or 13.

We have reviewed Petitioner’s showing for claims 2, 9, and 13. On this record, we find Petitioner has sufficiently shown the additional limitations of the dependent claims. *See* Pet. 55 (claim 2), 59 (claims 9 and 13).

3. Summary

Petitioner has shown a reasonable likelihood that claims 1–2, 7–9, and 13 would have been obvious over Narain and Kobayashi.

F. Claims 1, 3, 7, 8, 10, and 13 as Obvious Over Abarbanel and Feyerabend

Specific to this ground, Petitioner alleges claims 1, 3, 7, 8, 10, and 13 would have been obvious over Abarbanel and Feyerabend. Pet. 59–80; Ex. 1003 ¶¶ 277–361.

1. Claims 1, 7, and 8

As to the rationale for the combination, Petitioner alleges “[i]t was common for engineers to use graphical representations of specifications.” Pet. 59 (citing Ex. 1027,²⁰ 212). Further, Petitioner alleges “[g]raphically-editing timing waveforms was one of a finite number of identified predictable solutions, which Feyerabend teaches.” *Id.* at 59–60. According to Petitioner a person of ordinary skill in the art, “would have been motivated to combine teachings from Abarbanel and Feyerabend because the prior art includes teaching, suggestion, and motivation to do so.” *Id.* at 60 (citing Ex. 1003 ¶ 280).

Patent Owner disputes that there is sufficient rationale to combine Abarbanel and Feyerabend. Prelim. Resp. 43–47. Patent Owner repeats many of the arguments made for the combination of Abarbanel and Kobayashi above. *Id.*

²⁰ Gupta, *Formal Hardware Verification Methods: A Survey*, School of Computer Science, Carnegie Mellon University, ©1992.

On this record, and for the same reasons stated above, specifically including that graphically-editing timing waveforms was one of a finite number of identified predictable solutions as discussed in Section II.D.1, we are persuaded that Petitioner has sufficiently shown a rationale for the combination of Abarbanel and Feyerabend.

Patent Owner also disputes that Feyerabend shows the “graphically editing” limitation, limitation 1a. Prelim. Resp. 41–43. Petitioner argues limitation 1a is shown because Feyerabend’s “TDEditor generates data by **graphically editing the specification . . . based on user operations.**” Pet. 64–65 (citing Ex. 1007, 158, Fig. 1). Petitioner cites to Feyerabend as teaching “the graphical appeal of conventional timing diagrams as widely used in hardware design.” *Id.* at 65 (citing Ex. 1007, 156).

Patent Owner argues, “Feyerabend provides a single screenshot of a waveform but does not describe the software that displays the waveform nor its capabilities.” Prelim. Resp. 42 (citing Ex. 1007, 3). As a result, Patent Owner argues Feyerabend “does not disclose or suggest that its waveforms (the alleged IC specifications) can be ‘graphically edited.’” *Id.*

Our preliminary construction of the “graphically editing” limitation is “editing a visual expression, as opposed to editing text.” *See* Section II.B.2 above. We question whether Petitioner has shown the “graphically editing” limitation for the reasons cited by Patent Owner.

2. Claims 3, 10, and 13

Claim 3 depends from claim 1, and claims 10 and 13 depend from claim 8. Patent Owner does not separately argue for the patentability of claims 3, 10, or 13.

We have reviewed Petitioner's showing for claims 3, 10, and 13. On this record, we find Petitioner has sufficiently shown the additional limitations of the dependent claims. *See* Pet. 73–75 (claim 3), 79–80 (claims 10 and 13).

3. Summary

We question whether Petitioner has shown a reasonable likelihood that claims 1, 3, 7, 8, 10, and 13 would have been obvious over Abarbanel and Feyerabend.

G. Claim 14 as Obvious Over (1) Abarbanel, Kobayashi, and McKeone; (2) Narain, Kobayashi, and McKeone; and (3) Abarbanel, Feyerabend, and McKeone

Specific to these grounds, Petitioner asserts that McKeone combined with the references above at Sections II.D, II.E, and II.F teach each limitation of claim 14 and provides a limitation-by-limitation analysis for each. Pet. 80–84; Ex. 1003 ¶¶ 362–392.

Patent Owner does not dispute Petitioner's showing. *See* Prelim. Resp. Petitioner argues claim 14 recites a manufacturing step and McKeone teaches this and renders claim 14 obvious in combination with the challenges analyzed in Sections II.D, II.E and II.F above. Pet. 80 (citing Ex. 1003 ¶ 362).

Petitioner has shown a reasonable likelihood that claim 14 would have been obvious over the combinations of Abarbanel, Kobayashi, and McKeone and Narain, Kobayashi, and McKeone. For reasons stated above, we question whether the combination of Abarbanel, Feyerabend, and McKeone would have rendered claim 14 obvious.

III. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition.

IV. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '636 patent is hereby instituted for all of the challenged claims on all of the asserted grounds; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.

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Patent 7,603,636 B2

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