

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CADENCE DESIGN SYSTEMS, INC.,

Petitioner,

v.

SEMICONDUCTOR DESIGN TECHNOLOGIES, LLC,

Patent Owner.

IPR2024-00356

U.S. Patent No. 7,603,636

PETITIONER'S UPDATED EXHIBIT LIST

PETITIONER'S EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 7,603,636 to Yamada (“the ’636 Patent”)
1002	Prosecution History of U.S. Patent No. 7,603,636
1003	Declaration of Soheil Ghiasi, Ph.D.
1004	FoCs – Automatic Generation of Simulation Checkers from Formal Specifications (“Abarbanel”)
1005	U.S. Patent No. 4,922,432 to Kobayashi (“Kobayashi”)
1006	U.S. Patent No. 6,651,228 to Narain (“Narain”)
1007	A Visual Formalism for Real Time Requirement Specifications (“Feyerabend”)
1008	U.S. Patent No. 6,957,413 to McKeone (“McKeone”)
1009	Plaintiff’s Infringement Contentions Cover Pleading
1010	Plaintiff’s Infringement Contentions Claim Chart – Exhibit A-1
1011	Plaintiff’s Infringement Contentions Claim Chart – Exhibit A-2
1012	Plaintiff’s Infringement Contentions Claim Chart – Exhibit B-1
1013	Certificate of English Translation of JPH01309185A
1014	Certified English Translation of JPH01309185A
1015	JPH 1-309185 to Kobayashi
1016	U.S. Patent Application Publication No. 2003/0217190A1 to Devine (“Devine”)
1017	U.S. Patent Application Publication No. 2006/0047540A1 to Hutten (“Hutten”)
1018	U.S. Patent No. 7,424,543 to Rice (“Rice”)
1019	U.S. Patent No. 7,046,246 to Saitou (“Saitou”)
1020	U.S. Patent No. 7,944,445 to Schorr (“Schorr”)
1021	U.S. Patent No. 7,631,255 to Weise (“Weise”)
1022	Synthesis of Programs in Computational Logic (“Basin”)
1023	On-the-Fly Model Checking of RCTL Formulas (“Beer – RCTL”)
1024	RuleBase: an Industry-Oriented Formal Verification Tool (“Beer – RuleBase”)
1025	The Temporal Logic Sugar (“Beer – Sugar”)
1026	Assertion-Based Design (“Foster”)
1027	Formal Hardware Verification Methods: A Survey (“Gupta”)
1028	Automatic Generation of Model Checking Properties and Constraints from Production Based Specification (“Jahanpour”)
1029	Formal Verification Made Easy (“Schlipf”)

Exhibit No.	Description
1030	IEEE Standard VHDL Language Reference Manual, IEEE Std 1076, 2000 Edition (“VHDL LRM”)
1031	Defendant Cadence Design Systems, Inc.’s Preliminary Proposed Claim Constructions and Preliminary Identification of Evidence
1032	Plaintiff’s Patent L.R. 4-2 Disclosure of Preliminary Claim Constructions and Extrinsic Evidence
1033	A Really Temporal Logic (“Alur”)
1034	A Visual Formalism for Real Time Requirement Specifications (Black & White) - (“Feyerabend BW”)
1035	VHDL Starter’s Guide (“Yalamanchili”)
1036	Declaration of Welmoed Spahr re Abarbanel and Feyerabend
1037	Declaration of Ms. Rachel J. Watters re Abarbanel
1038	Declaration of Ms. Rachel J. Watters re Feyerabend
1039	Website – VisiCalc of Dan Bricklin and Bob Frankston Guide: History, Origin, and More
1040	Confidential Settlement Agreement

Date: July 23, 2024

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that on July 23, 2024, complete copies of the foregoing document and Exhibit 1040 were served via email to all parties to this proceeding at the addresses indicated:

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