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(54) LOAD REDUCED MEMORY MODULE

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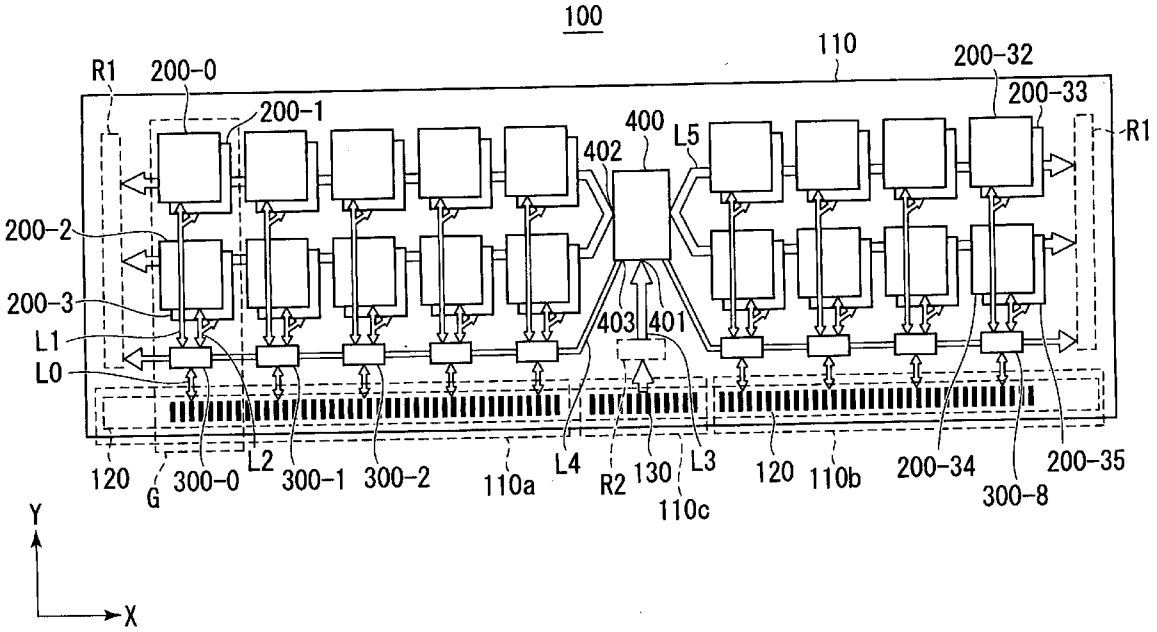
(52) **U.S. Cl.** **711/105**; 710/52; 711/154; 711/E12.001

(57) **ABSTRACT**

A memory module includes a plurality of memory chips and a plurality of data register buffers mounted on the module substrate. At least two memory chips are allocated to each of the data register buffers. Each of the data register buffers includes M input/output terminals (M is a positive integer equal to or larger than 1) that are connected to the data connectors via a first data line and N input/output terminals (N is a positive integer equal to or larger than 2M) that are connected to corresponding memory chips via second and third data lines, so that the number of the second and third data lines is N/M times the number of the first data lines. According to the present invention, because the load capacities of the second and third data lines are reduced by a considerable amount, it is possible to realize a considerably high data transfer rate.



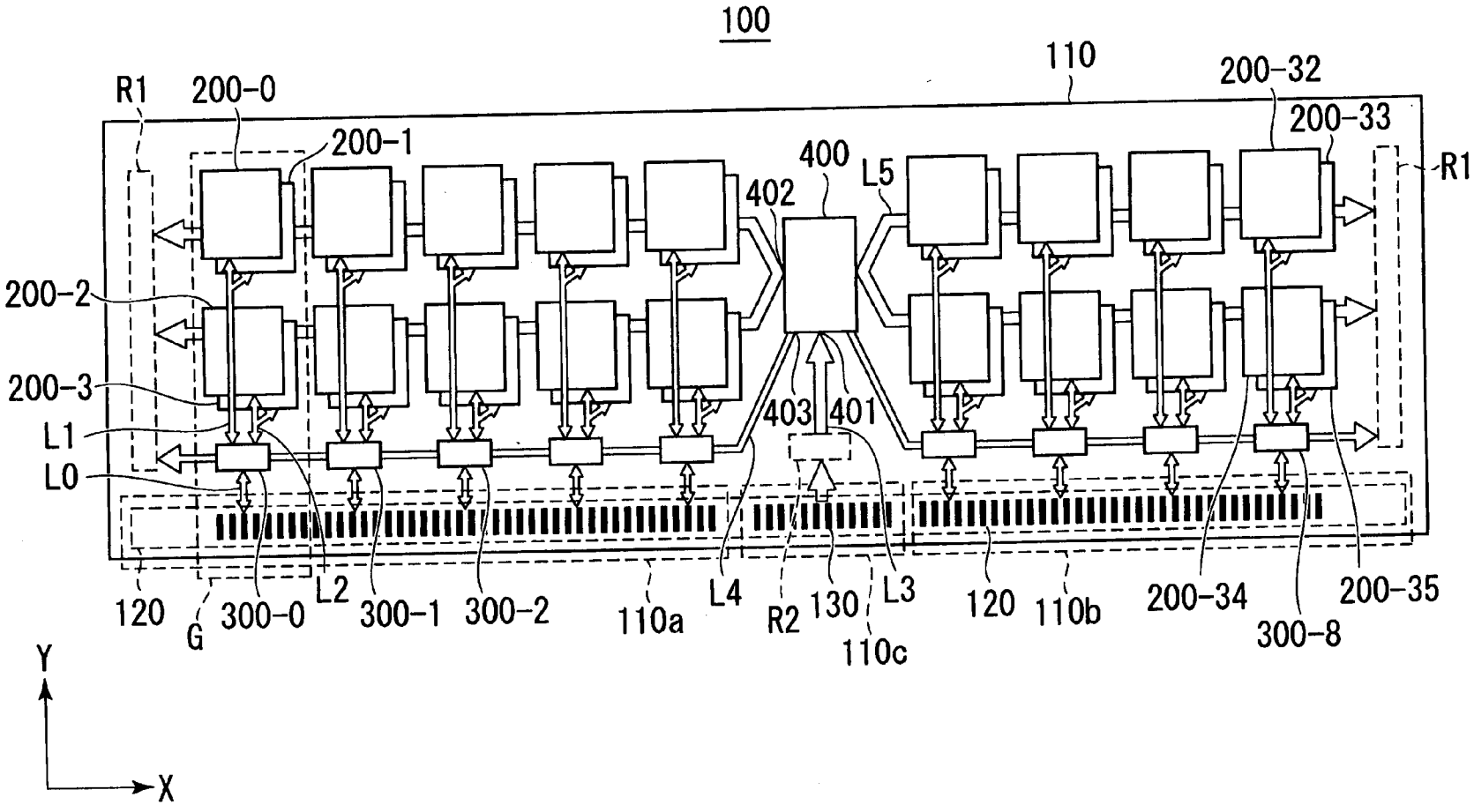

100
110
R1
200-0
200-1
200-2
200-3
L1
L0
400
402
L5
200-32
200-33
R1
403
401
120
G
300-0
L2
300-1
300-2
110a
L4
R2
130
L3
110c
120
110b
200-34
300-8
200-35
Y
X

FIG.1

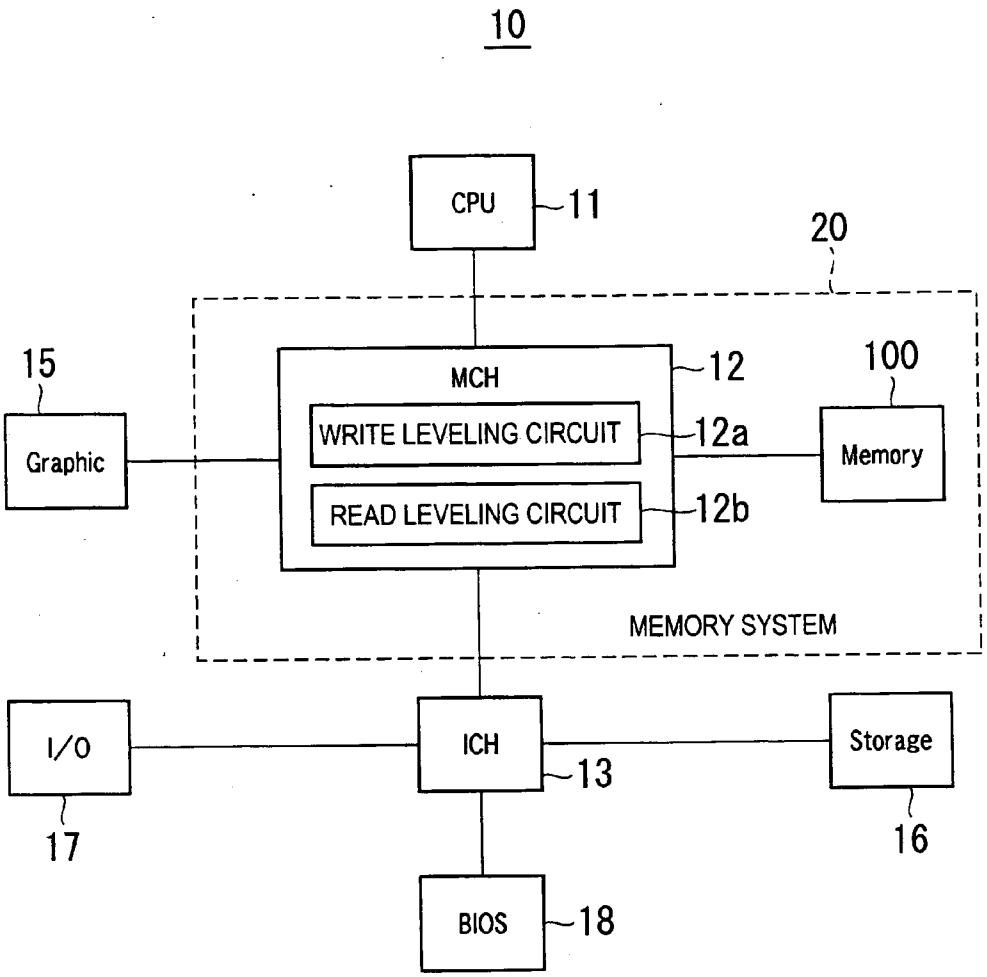

10
CPU
11
20
15
MCH
12
100
Graphic
WRITE LEVELING CIRCUIT
12a
Memory
READ LEVELING CIRCUIT
12b
MEMORY SYSTEM
I/O
ICH
Storage
13
17
16
BIOS
18

FIG.2

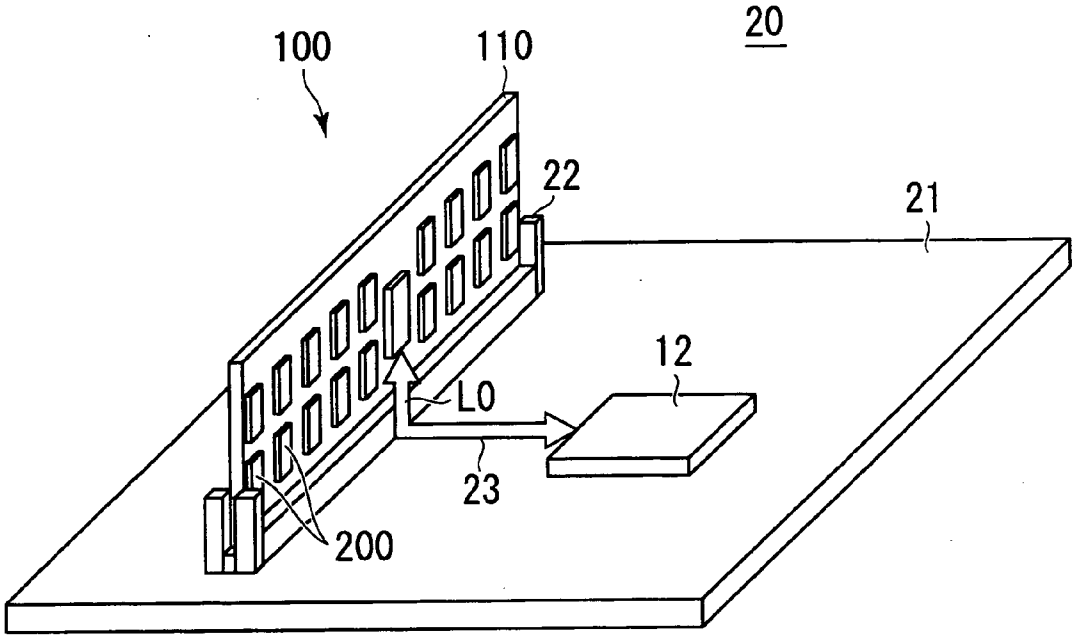


FIG.3

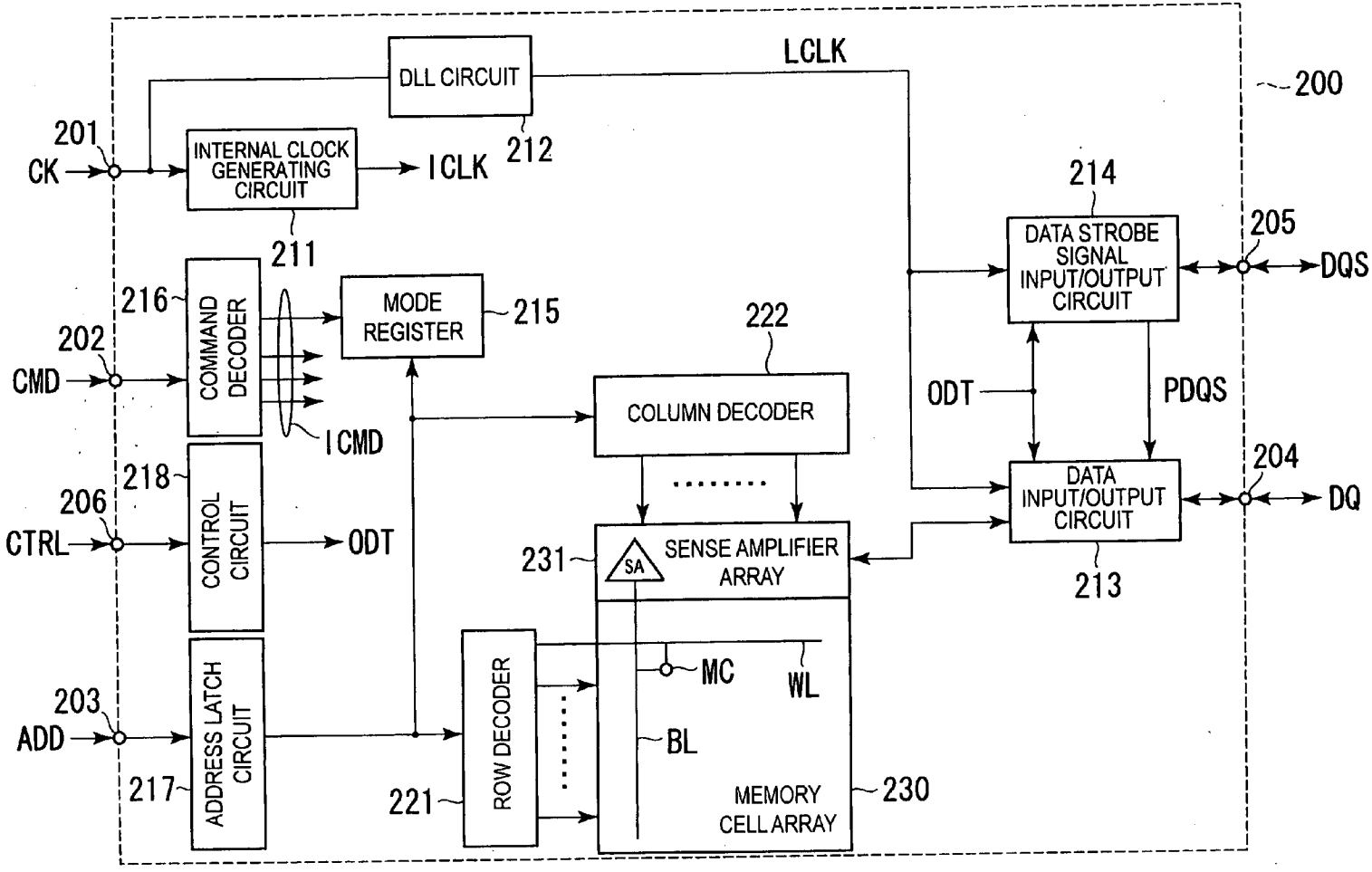

200
DLL CIRCUIT
LCLK
212
201
CK
INTERNAL CLOCK GENERATING CIRCUIT
ICLK
211
214
DATA STROBE SIGNAL INPUT/OUTPUT CIRCUIT
205
DQS
216
COMMAND DECODER
MODE REGISTER
215
222
202
CMD
COLUMN DECODER
ODT
PDQS
ICMD
218
CONTROL CIRCUIT
206
CTRL
ODT
DATA INPUT/OUTPUT CIRCUIT
204
DQ
231
SA
SENSE AMPLIFIER ARRAY
213
MC
WL
203
ADD
ADDRESS LATCH CIRCUIT
ROW DECODER
BL
217
221
MEMORY CELL ARRAY
230

FIG.4

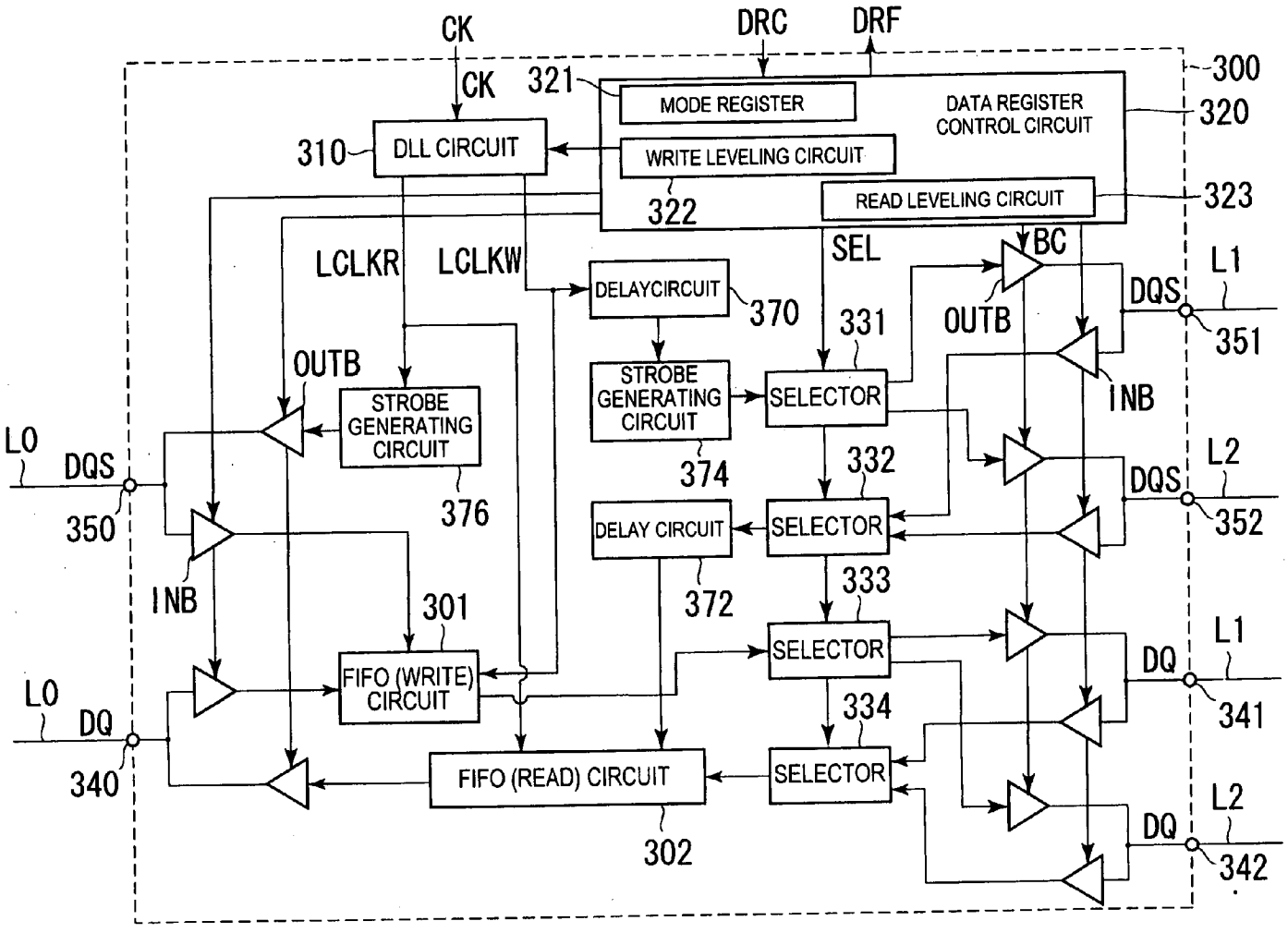

CK
DRC
DRF
300
CK
321
MODE REGISTER
DATA REGISTER CONTROL CIRCUIT
320
310
DLL CIRCUIT
WRITE LEVELING CIRCUIT
322
READ LEVELING CIRCUIT
323
LCLKR
LCLKW
SEL
BC
DELAYCIRCUIT
370
331
OUTB
L1
DQS
351
OUTB
STROBE GENERATING CIRCUIT
STROBE GENERATING CIRCUIT
SELECTOR
INB
L0
DQS
350
374
332
L2
DQS
352
376
DELAY CIRCUIT
SELECTOR
INB
301
372
333
L1
DQ
341
L0
DQ
340
FIFO (WRITE) CIRCUIT
SELECTOR
334
FIFO (READ) CIRCUIT
SELECTOR
L2
DQ
342
302

FIG.5

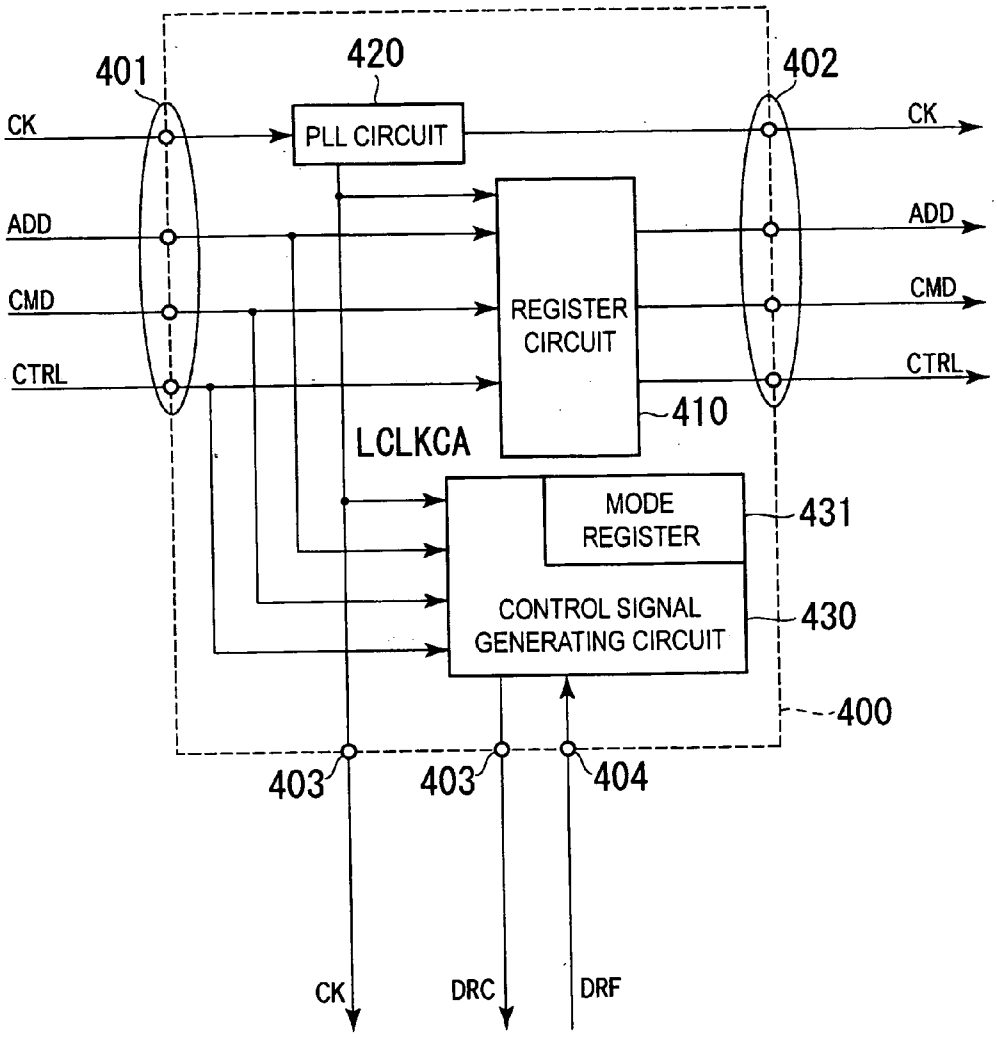

401
420
402
CK
PLL CIRCUIT
CK
ADD
ADD
CMD
REGISTER CIRCUIT
CMD
CTRL
CTRL
410
LCLKCA
MODE REGISTER
431
CONTROL SIGNAL GENERATING CIRCUIT
430
400
403
403
404
CK
DRC
DRF

FIG.6

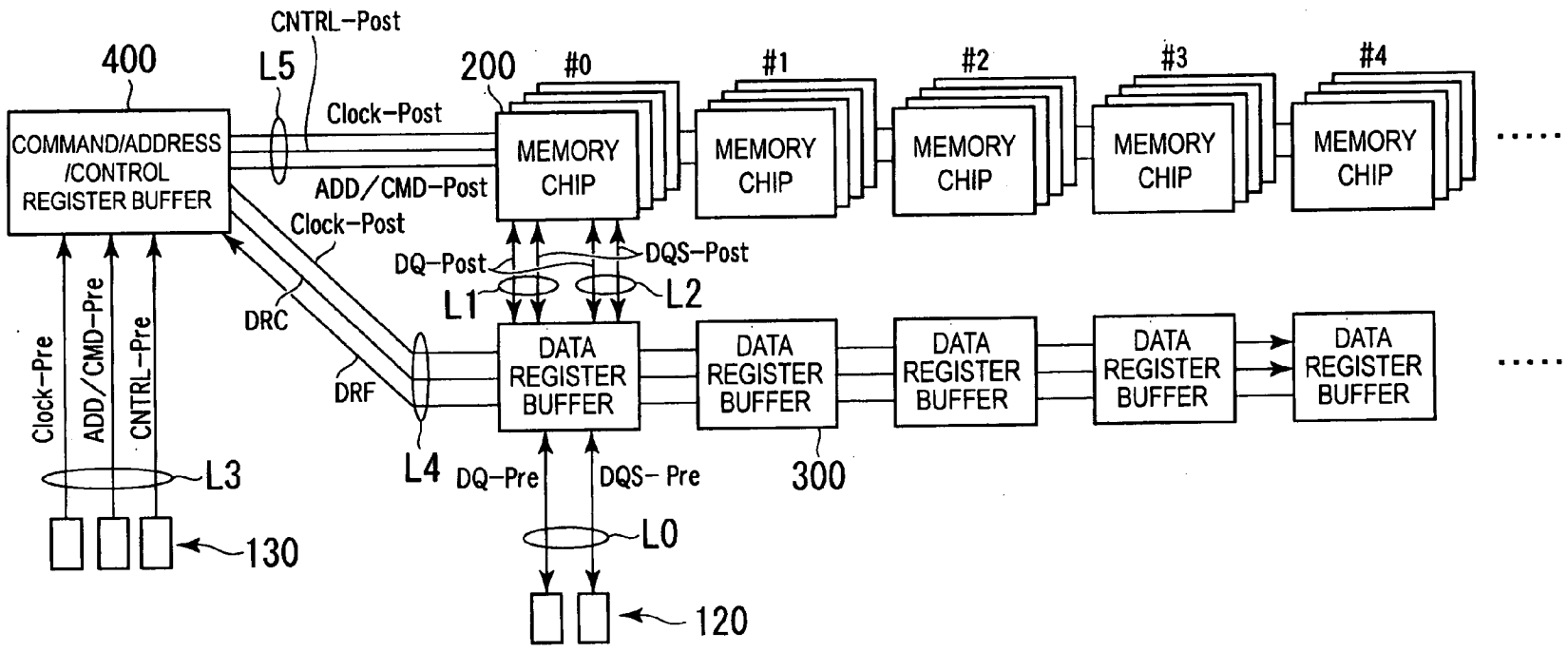

400
COMMAND/ADDRESS /CONTROL REGISTER BUFFER
L5
CNTRL-Post
Clock-Post
ADD/CMD-Post
Clock-Post
200
#0
#1
#2
#3
#4
MEMORY CHIP
MEMORY CHIP
MEMORY CHIP
MEMORY CHIP
MEMORY CHIP
DQ-Post
DQS-Post
L1
L2
DRC
DRF
DATA REGISTER BUFFER
DATA REGISTER BUFFER
DATA REGISTER BUFFER
DATA REGISTER BUFFER
DATA REGISTER BUFFER
Clock-Pre
ADD/CMD-Pre
CNTRL-Pre
L3
L4
DQ-Pre
DQS- Pre
300
L0
130
120

FIG.7

FIG.8A

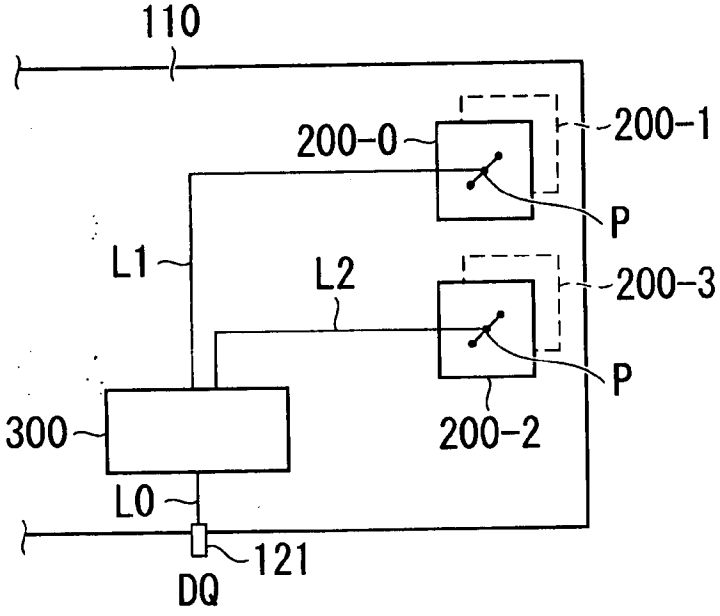

110
200-0
200-1
P
L1
L2
200-3
P
300
200-2
L0
121
DQ

FIG.8B

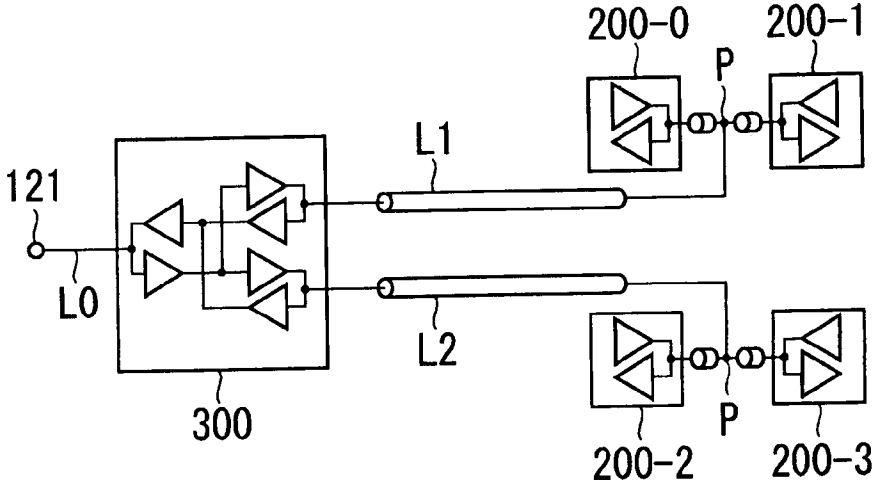

200-0
200-1
P
L1
121
L0
L2
300
P
200-2
200-3

FIG.9A

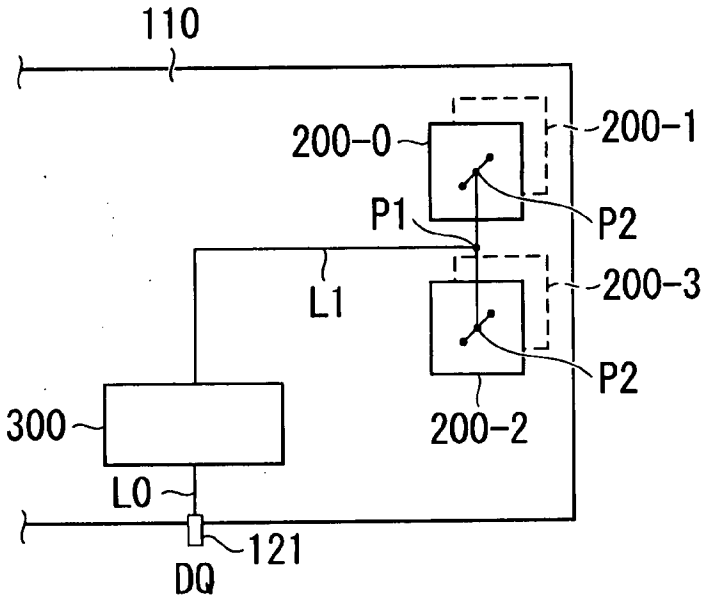
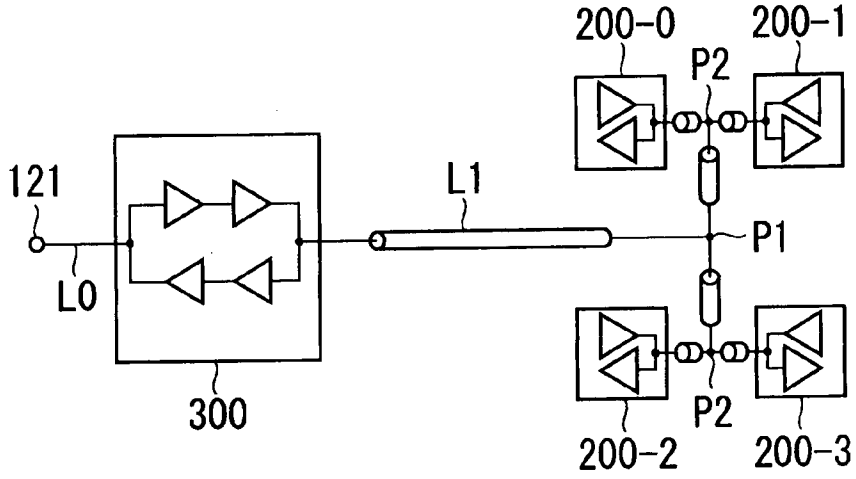

110
200-0
200-1
P1
P2
L1
200-3
P2
300
200-2
L0
121
DQ

FIG.9B


200-0
200-1
P2
121
L1
P1
L0
300
P2
200-2
200-3

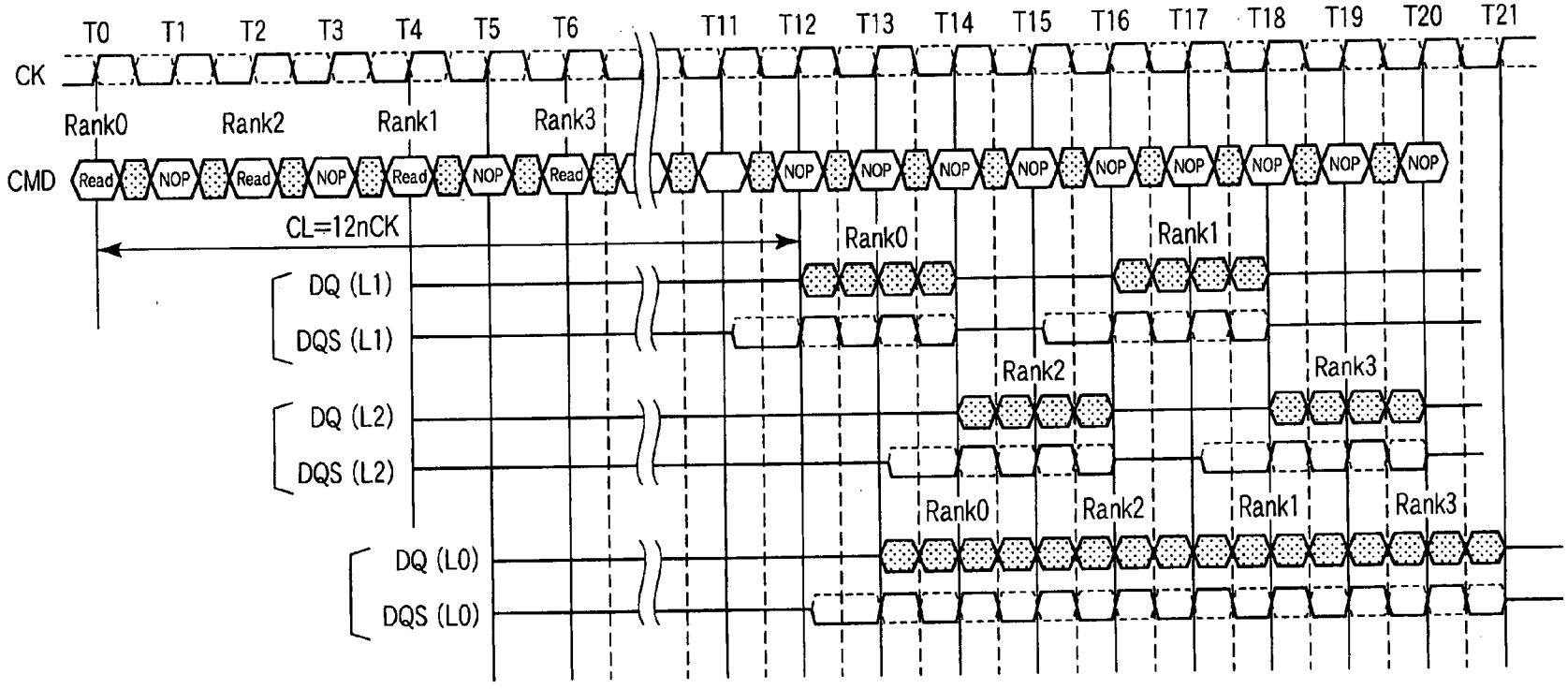

T0
T1
T2
T3
T4
T5
T6
T11
T12
T13
T14
T15
T16
T17
T18
T19
T20
T21
CK
Rank0
Rank2
Rank1
Rank3
CMD
Read
NOP
CL=12nCK
DQ (L1)
DQS (L1)
DQ (L2)
DQS (L2)
DQ (L0)
DQS (L0)

FIG.10

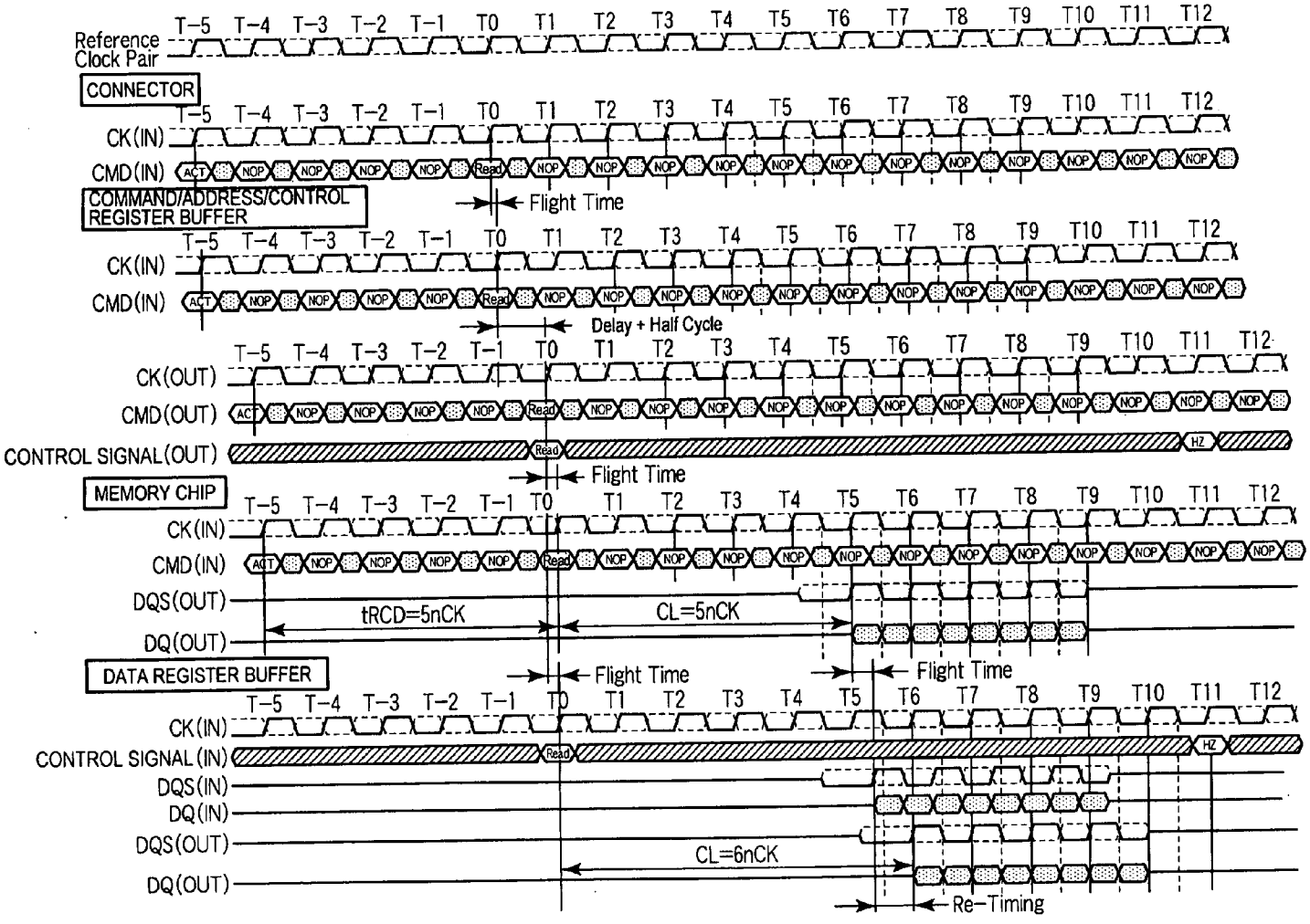

Reference Clock Pair
CONNECTOR
CK(IN)
CMD(IN)
COMMAND/ADDRESS/CONTROL REGISTER BUFFER
Flight Time
Delay + Half Cycle
CK(OUT)
CMD(OUT)
CONTROL SIGNAL(OUT)
MEMORY CHIP
DQS(OUT)
DQ(OUT)
tRCD=5nCK
CL=5nCK
DATA REGISTER BUFFER
CONTROL SIGNAL(IN)
DQS(IN)
DQ(IN)
CL=6nCK
Re-Timing
T-5 T-4 T-3 T-2 T-1 T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12
ACT NOP Read HZ

FIG.11

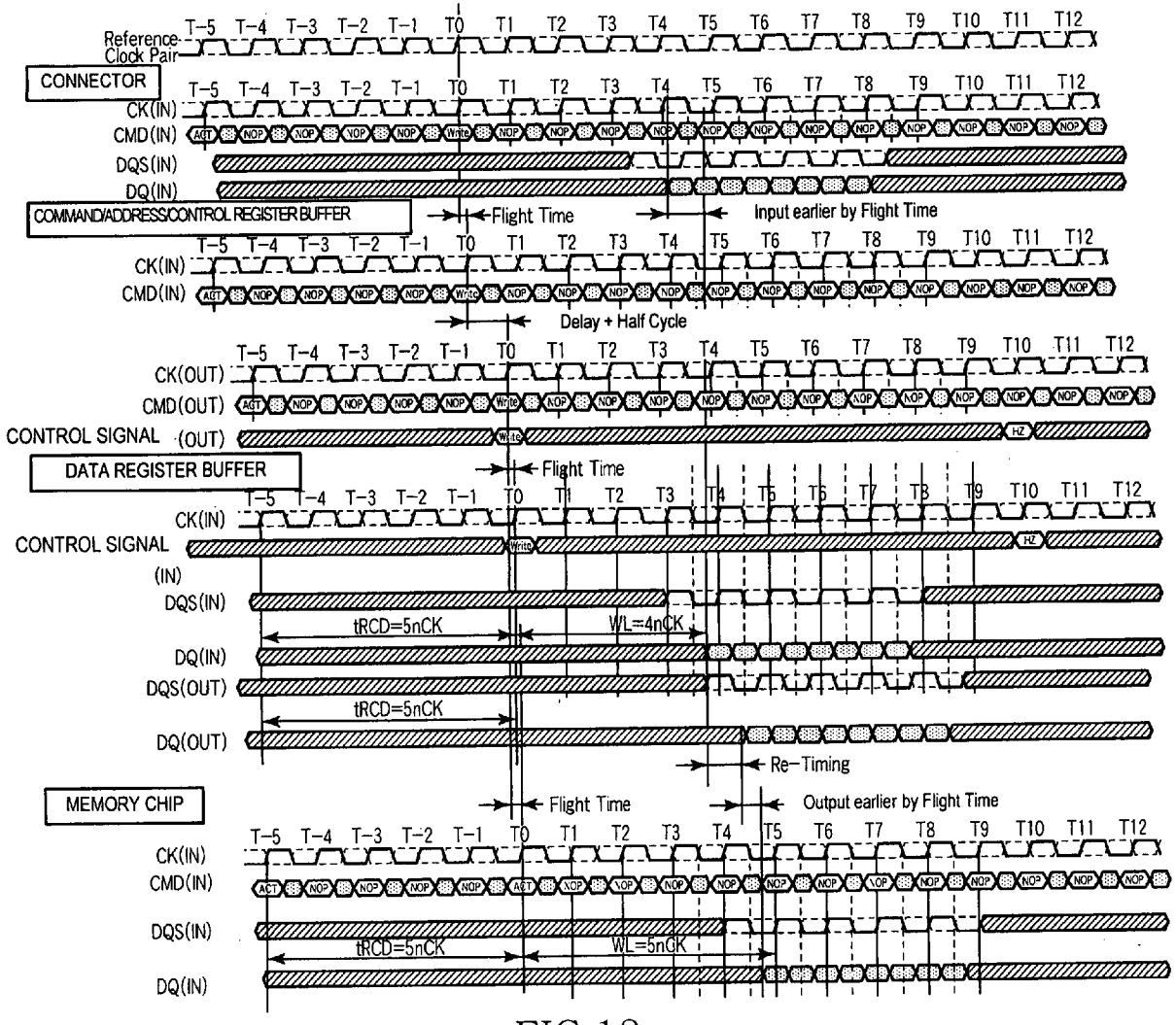

Reference Clock Pair
CONNECTOR
CK(IN)
CMD(IN)
DQS(IN)
DQ(IN)
COMMAND/ADDRESS/CONTROL REGISTER BUFFER
Flight Time
Input earlier by Flight Time
Delay + Half Cycle
CK(OUT)
CMD(OUT)
CONTROL SIGNAL (OUT)
DATA REGISTER BUFFER
CONTROL SIGNAL (IN)
tRCD=5nCK
WL=4nCK
DQS(OUT)
DQ(OUT)
Re-Timing
MEMORY CHIP
Output earlier by Flight Time
WL=5nCK
T-5 T-4 T-3 T-2 T-1 T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12

FIG.12

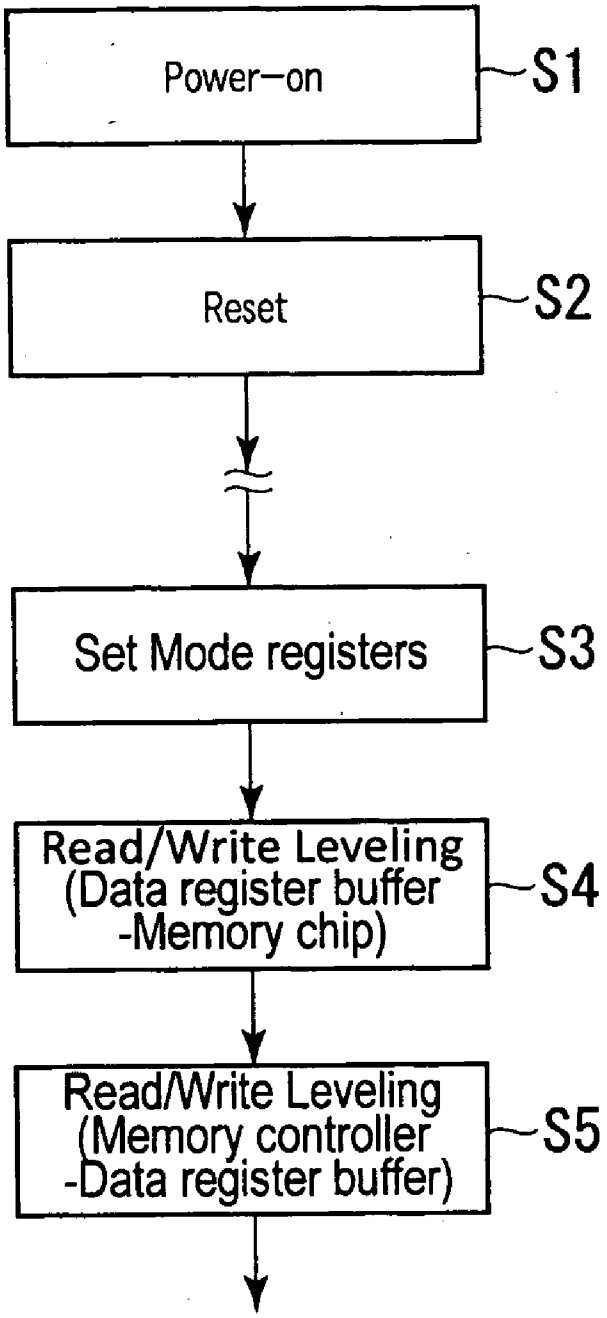

Power-on
S1
Reset
S2
Set Mode registers
S3
Read/Write Leveling
(Data register buffer
-Memory chip)
S4
Read/Write Leveling
(Memory controller
-Data register buffer)
S5

FIG.13

FIG.14A

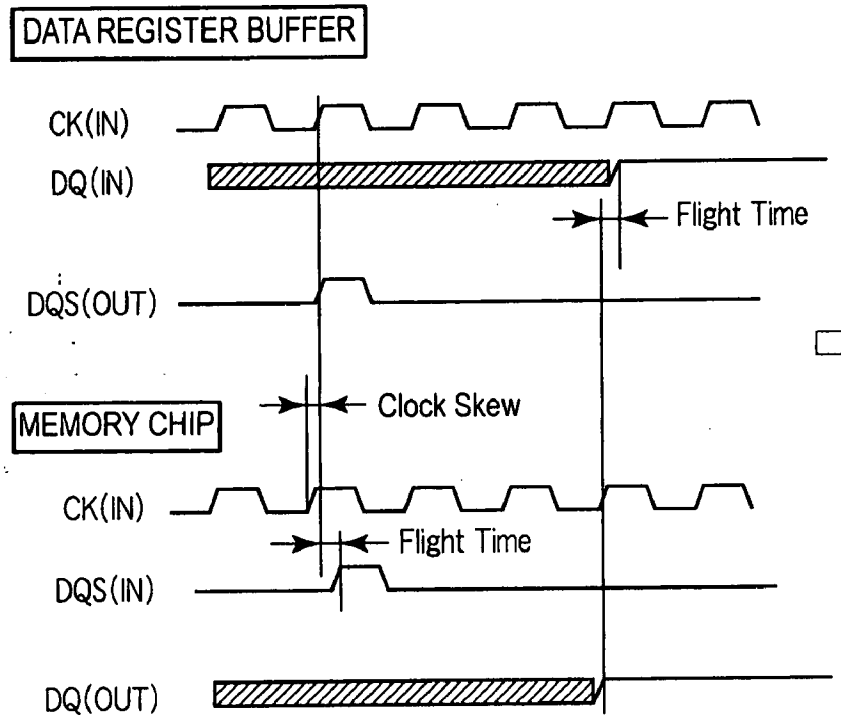
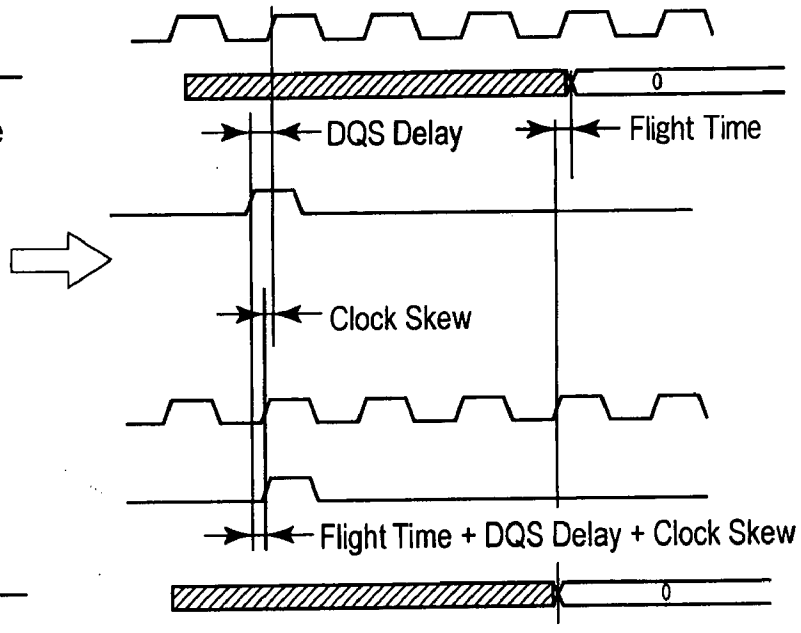


FIG.14B



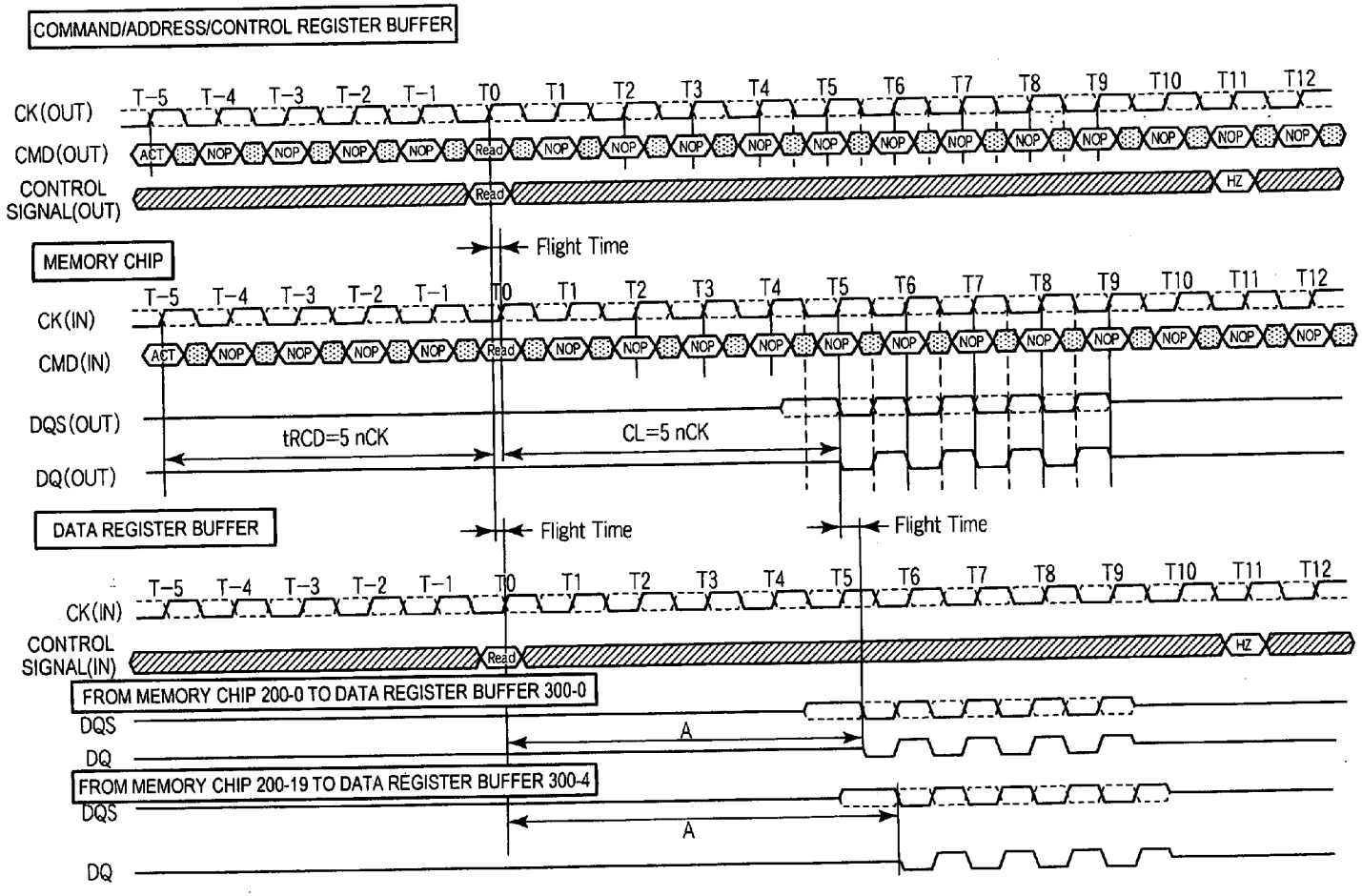

COMMAND/ADDRESS/CONTROL REGISTER BUFFER
CK(OUT)
CMD(OUT)
CONTROL SIGNAL(OUT)
T-5 T-4 T-3 T-2 T-1 T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12
ACT
NOP
Read
HZ
Flight Time
MEMORY CHIP
CK(IN)
CMD(IN)
DQS(OUT)
DQ(OUT)
tRCD=5 nCK
CL=5 nCK
DATA REGISTER BUFFER
CONTROL SIGNAL(IN)
FROM MEMORY CHIP 200-0 TO DATA REGISTER BUFFER 300-0
DQS
DQ
A
FROM MEMORY CHIP 200-19 TO DATA REGISTER BUFFER 300-4

FIG.15

FIG.16A

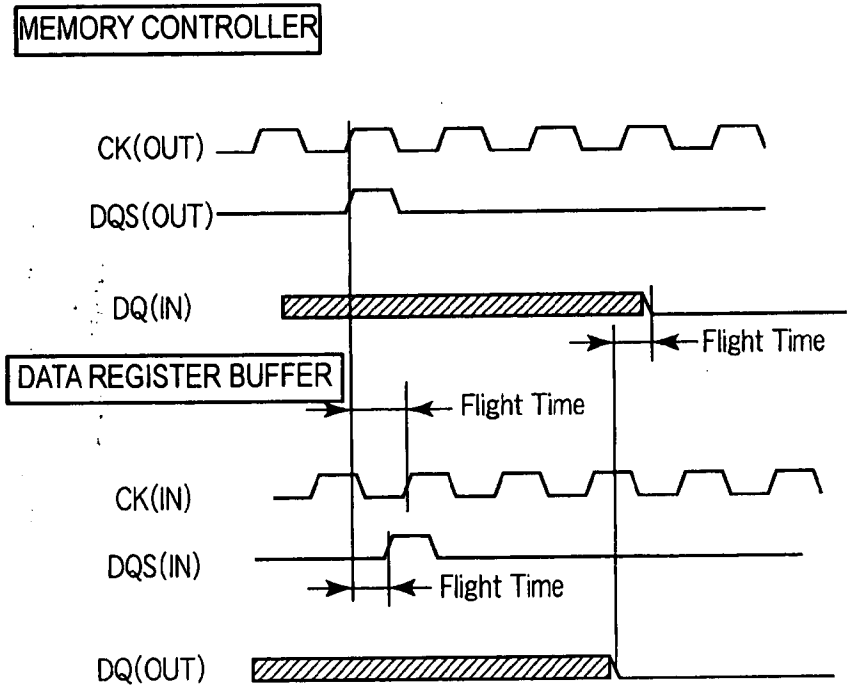
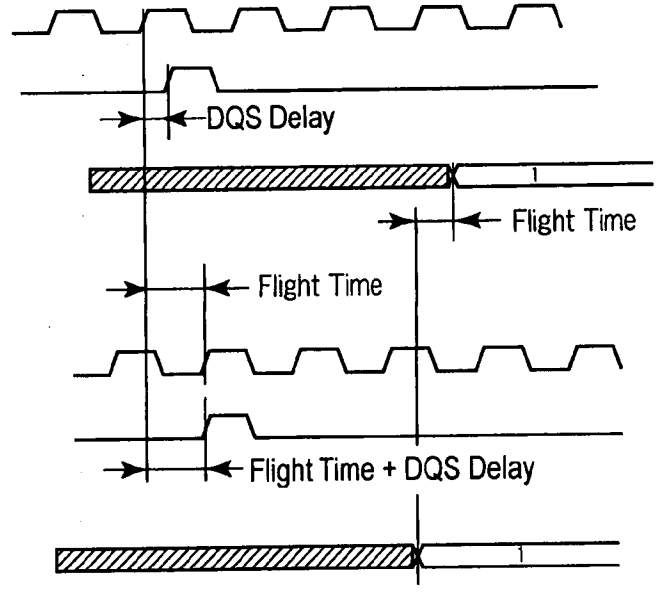


FIG.16B



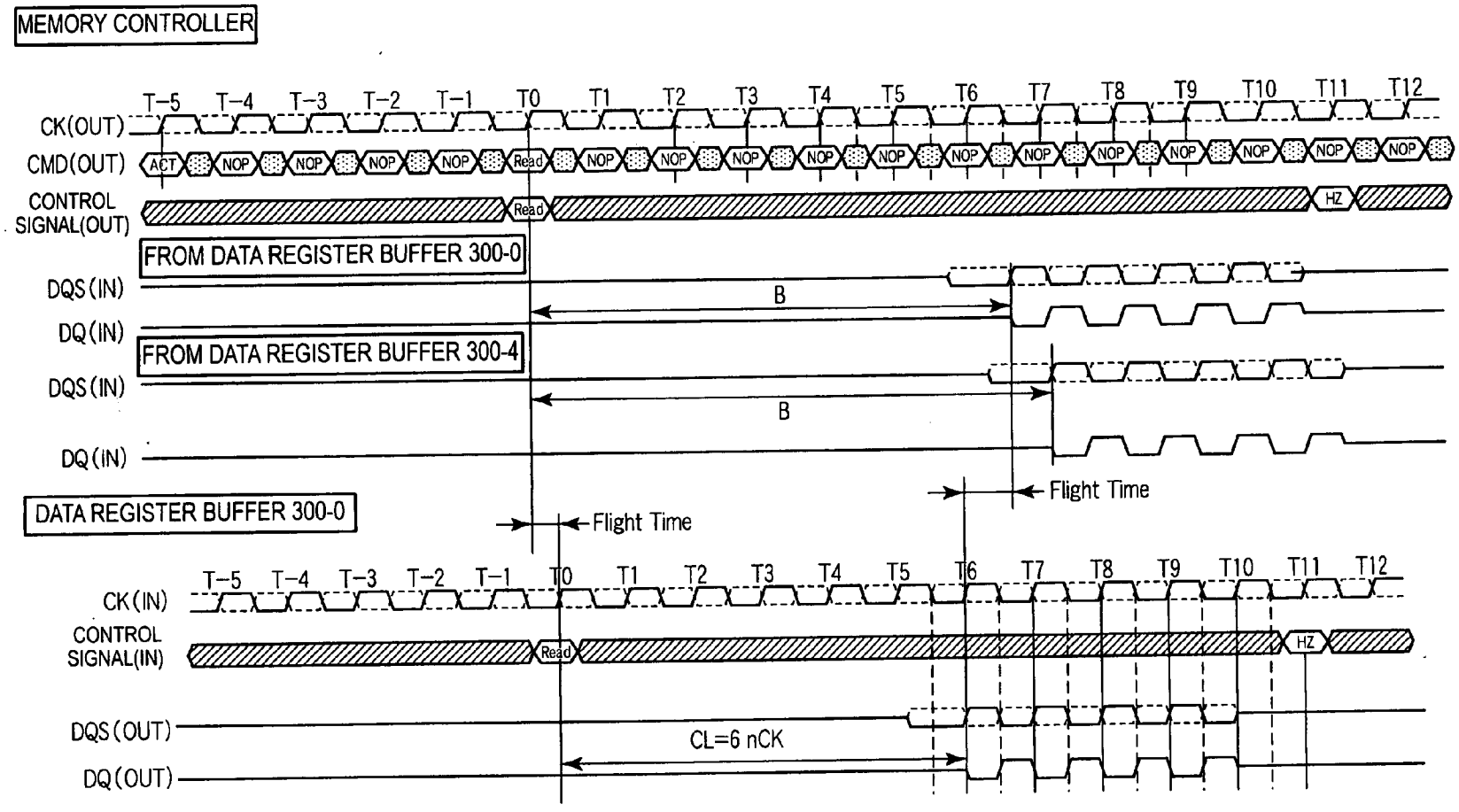

MEMORY CONTROLLER
T-5 T-4 T-3 T-2 T-1 T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12
CK(OUT)
CMD(OUT)
ACT NOP NOP NOP NOP Read NOP NOP NOP NOP NOP NOP NOP NOP NOP NOP NOP NOP NOP
CONTROL SIGNAL(OUT)
Read
HZ
FROM DATA REGISTER BUFFER 300-0
DQS(IN)
B
DQ(IN)
FROM DATA REGISTER BUFFER 300-4
DQS(IN)
B
DQ(IN)
Flight Time
Flight Time
DATA REGISTER BUFFER 300-0
T-5 T-4 T-3 T-2 T-1 T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12
CK(IN)
CONTROL SIGNAL(IN)
Read
HZ
DQS(OUT)
CL=6 nCK
DQ(OUT)

FIG.17

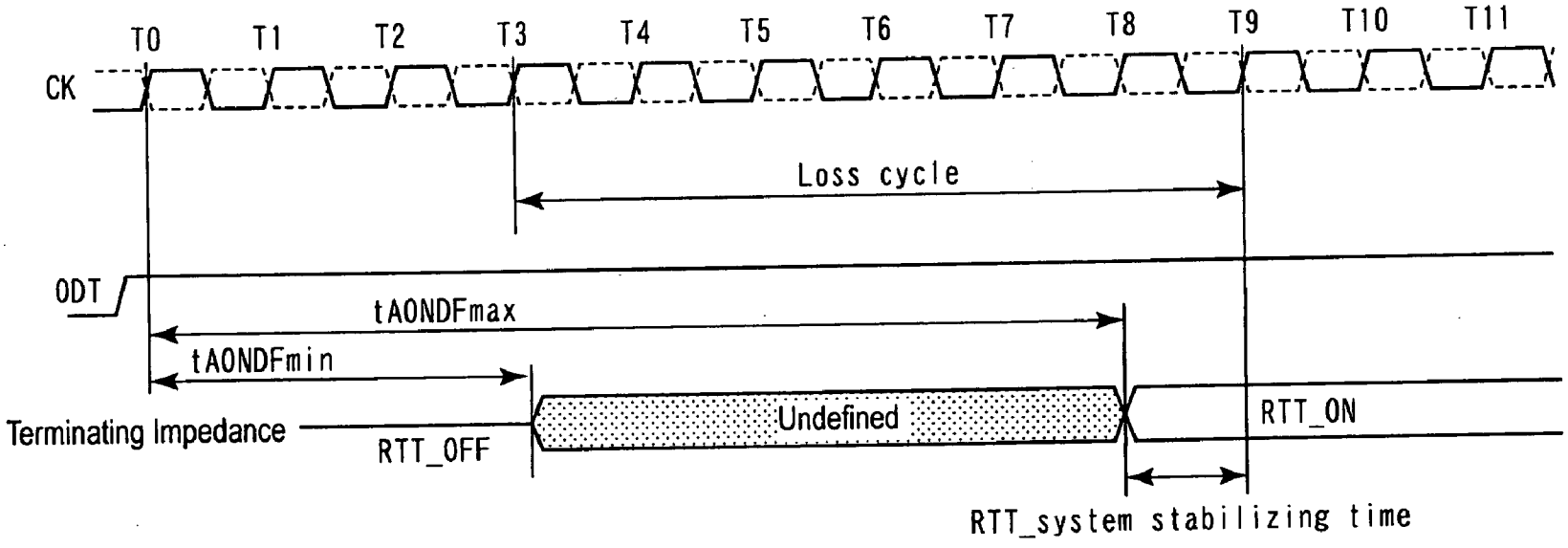

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
CK
Loss cycle
ODT
tAONDFmax
tAONDFmin
Terminating Impedance
RTT_OFF
Undefined
RTT_ON
RTT_system stabilizing time

FIG.18

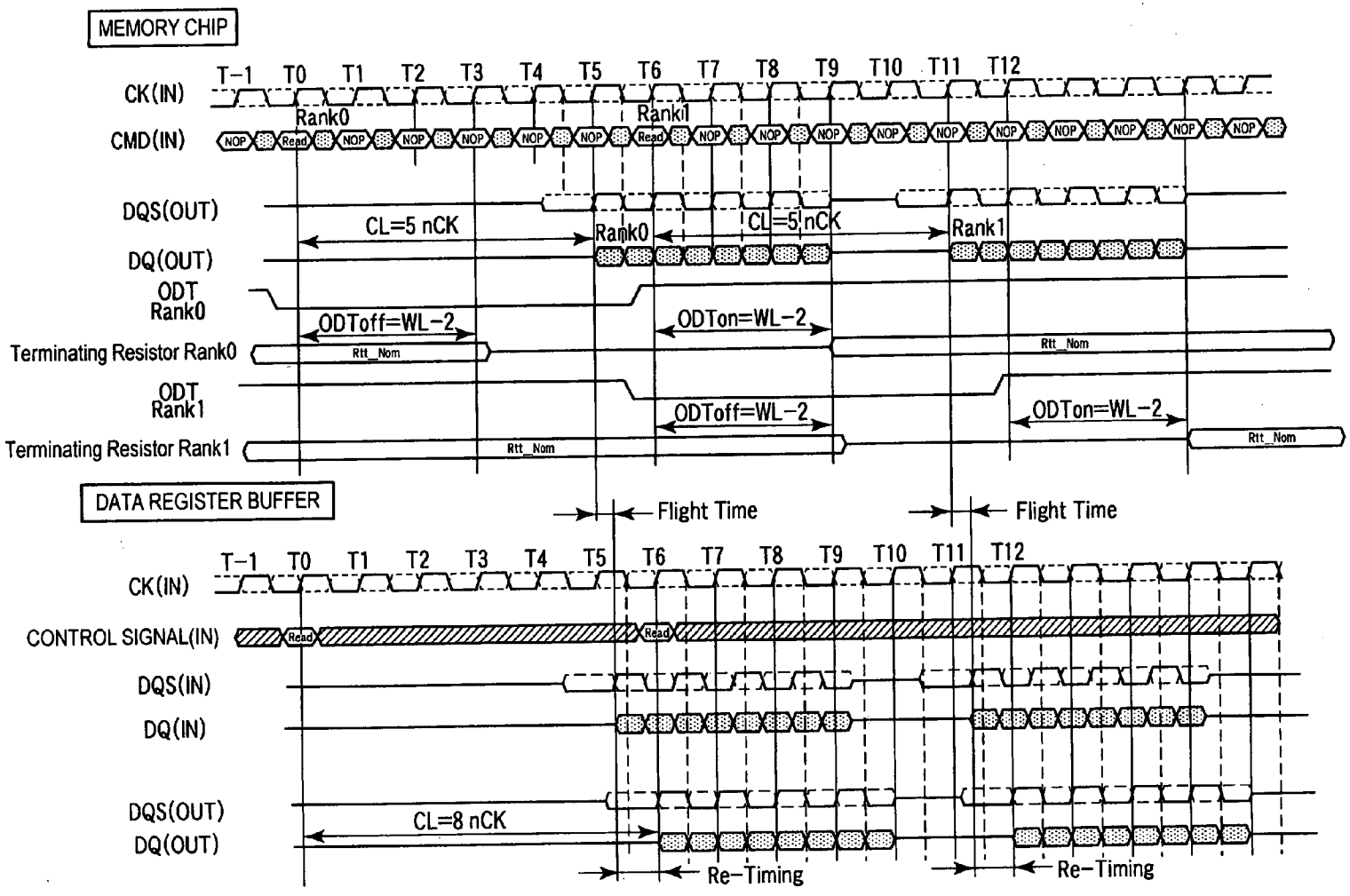

MEMORY CHIP
CK(IN)
T-1 T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12
Rank0
Rank1
CMD(IN)
NOP
Read
DQS(OUT)
DQ(OUT)
CL=5 nCK
Rank0
CL=5 nCK
Rank1
ODT Rank0
ODToff=WL-2
ODTon=WL-2
Terminating Resistor Rank0
Rtt_Nom
ODT Rank1
ODToff=WL-2
ODTon=WL-2
Terminating Resistor Rank1
Rtt_Nom
DATA REGISTER BUFFER
Flight Time
Flight Time
CK(IN)
CONTROL SIGNAL(IN)
DQS(IN)
DQ(IN)
DQS(OUT)
DQ(OUT)
CL=8 nCK
Re-Timing
Re-Timing

FIG.19

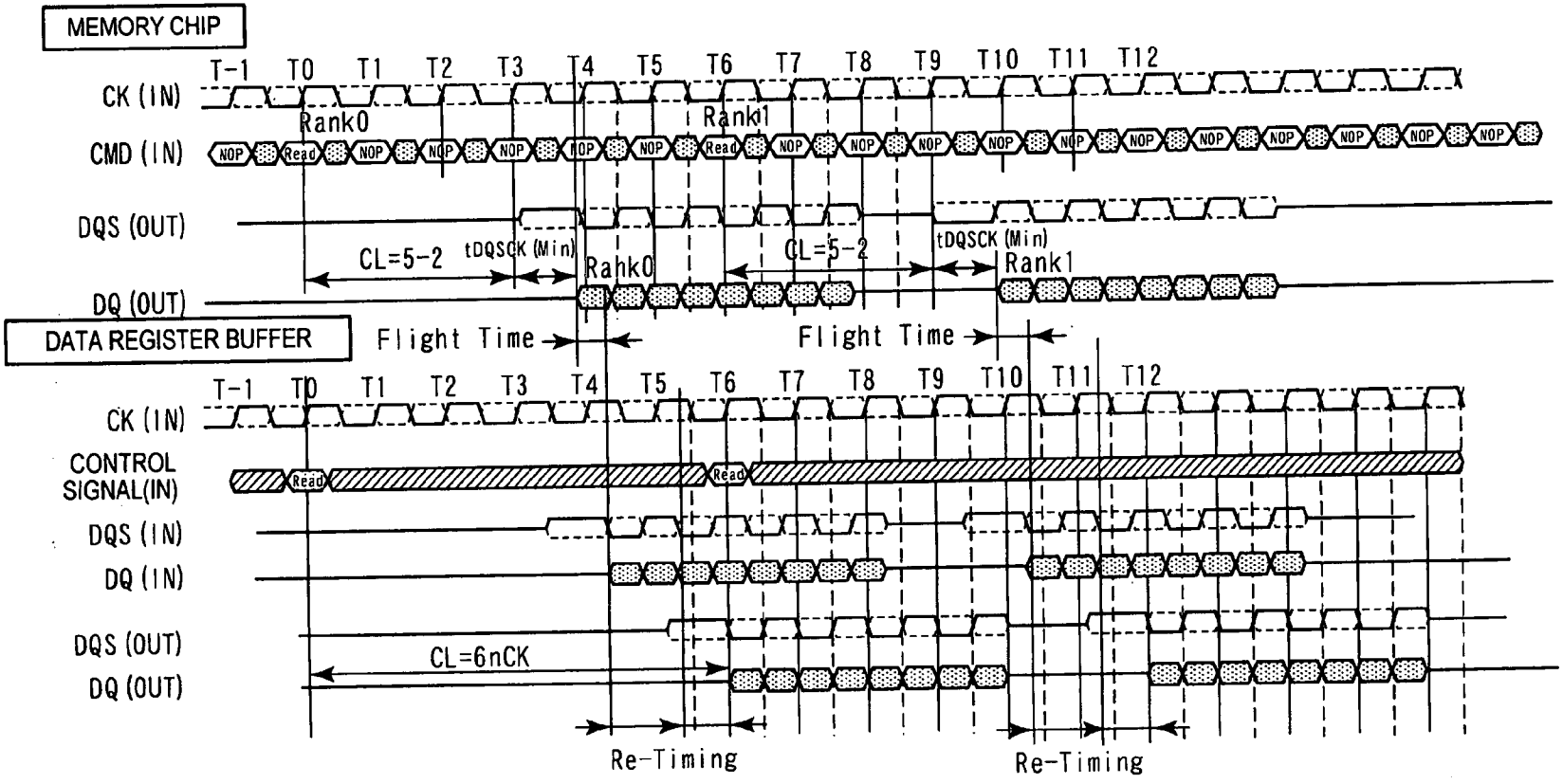

MEMORY CHIP
T-1 T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12
CK (IN)
Rank0
Rank1
CMD (IN)
NOP
Read
DQS (OUT)
CL=5-2
tDQSCK (Min)
Rank0
CL=5-2
tDQSCK (Min)
Rank1
DQ (OUT)
DATA REGISTER BUFFER
Flight Time
Flight Time
T-1 T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12
CK (IN)
CONTROL SIGNAL(IN)
Read
Read
DQS (IN)
DQ (IN)
DQS (OUT)
CL=6nCK
DQ (OUT)
Re-Timing
Re-Timing

FIG.20

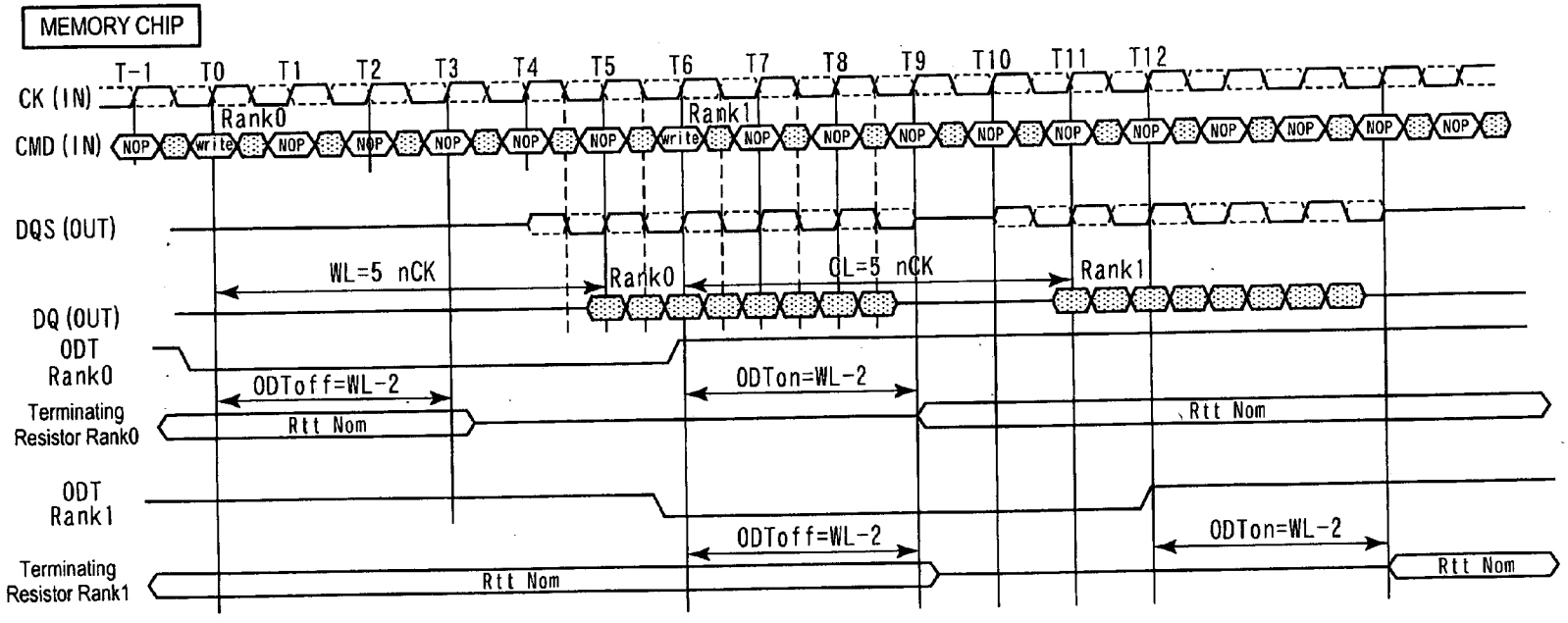

MEMORY CHIP
T-1
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
CK (IN)
CMD (IN)
Rank0
Rank1
NOP
write
DQS (OUT)
WL=5 nCK
CL=5 nCK
DQ (OUT)
ODT Rank0
ODToff=WL-2
ODTon=WL-2
Terminating Resistor Rank0
Rtt Nom
ODT Rank1
Terminating Resistor Rank1

FIG.21

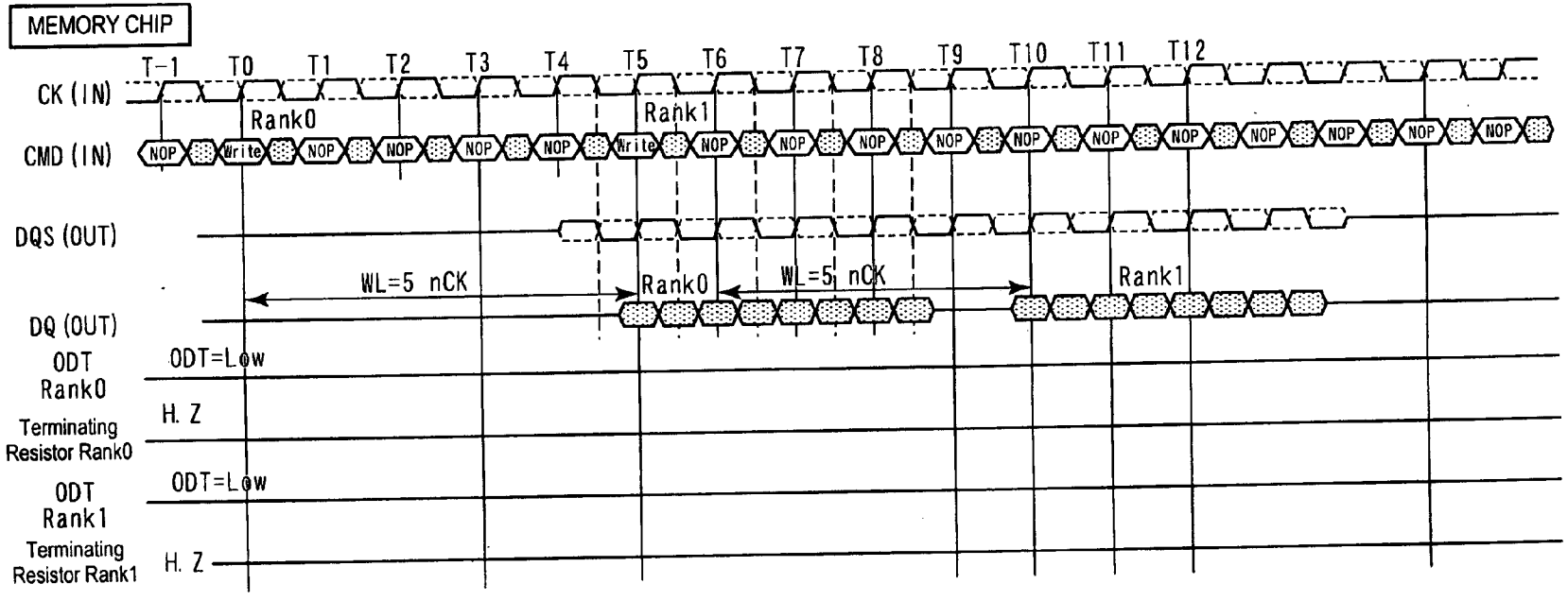

MEMORY CHIP
T-1
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
CK (IN)
CMD (IN)
Rank0
Rank1
NOP
Write
DQS (OUT)
WL=5 nCK
Rank0
WL=5 nCK
Rank1
DQ (OUT)
ODT Rank0
ODT=Low
Terminating Resistor Rank0
H. Z
ODT Rank1
ODT=Low
Terminating Resistor Rank1
H. Z

FIG.22

FIG.23A

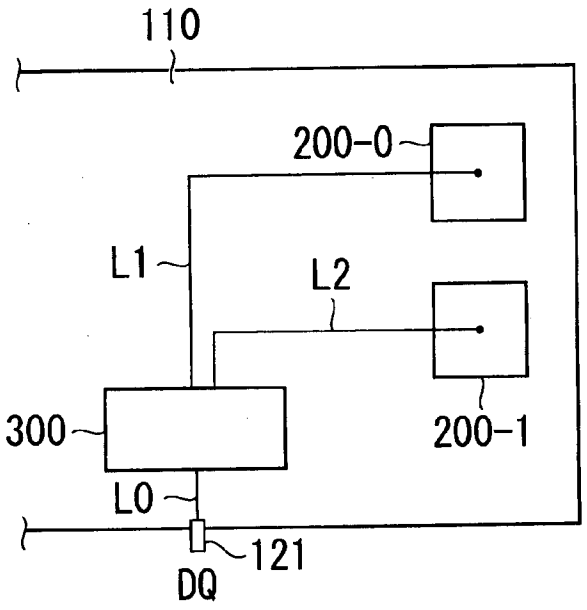


FIG.23B

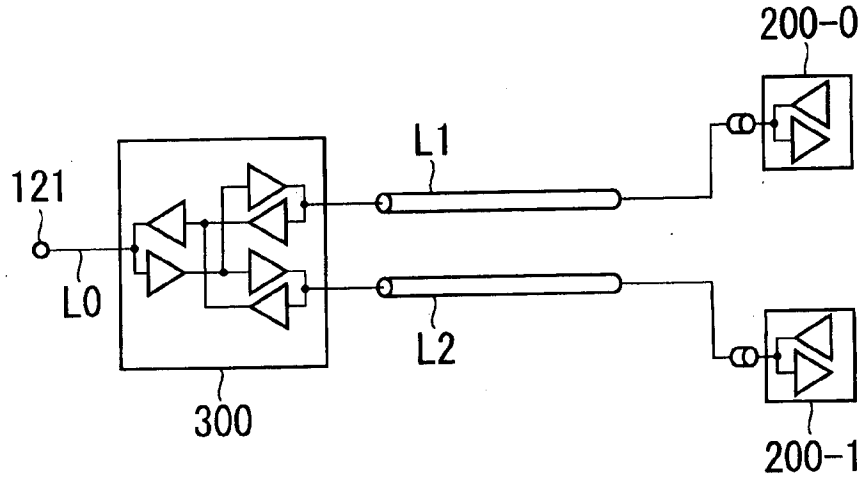


FIG.24A

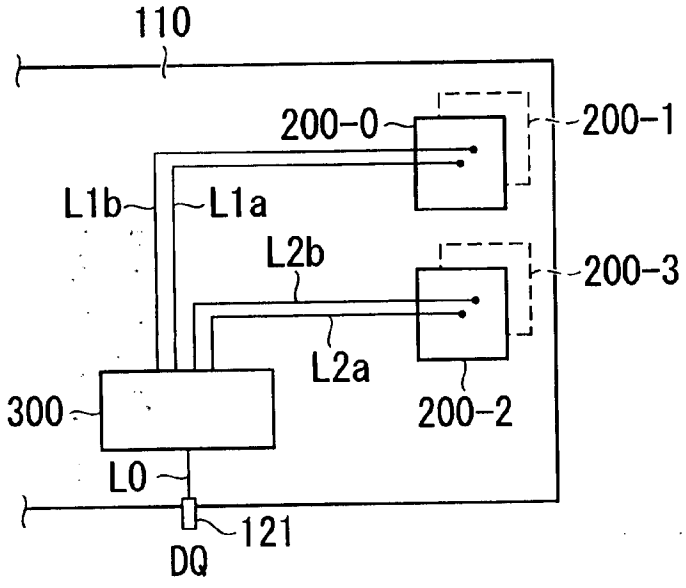
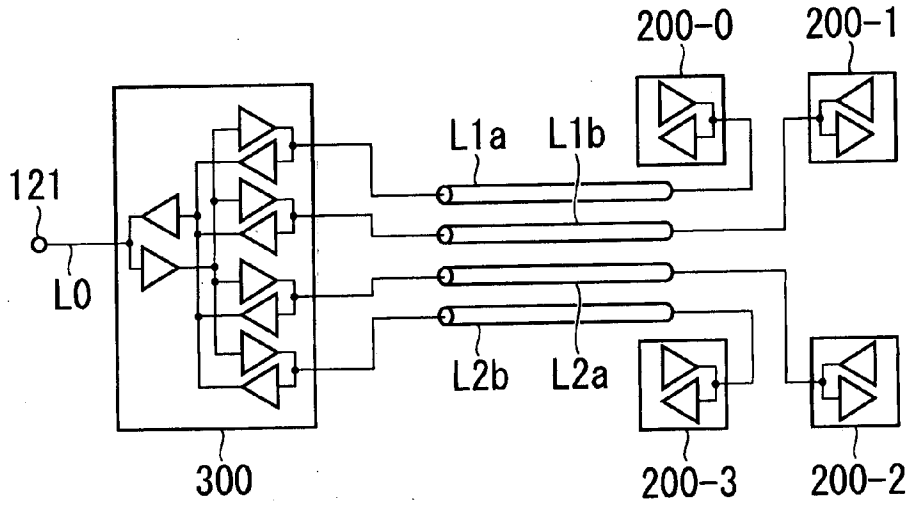


FIG.24B



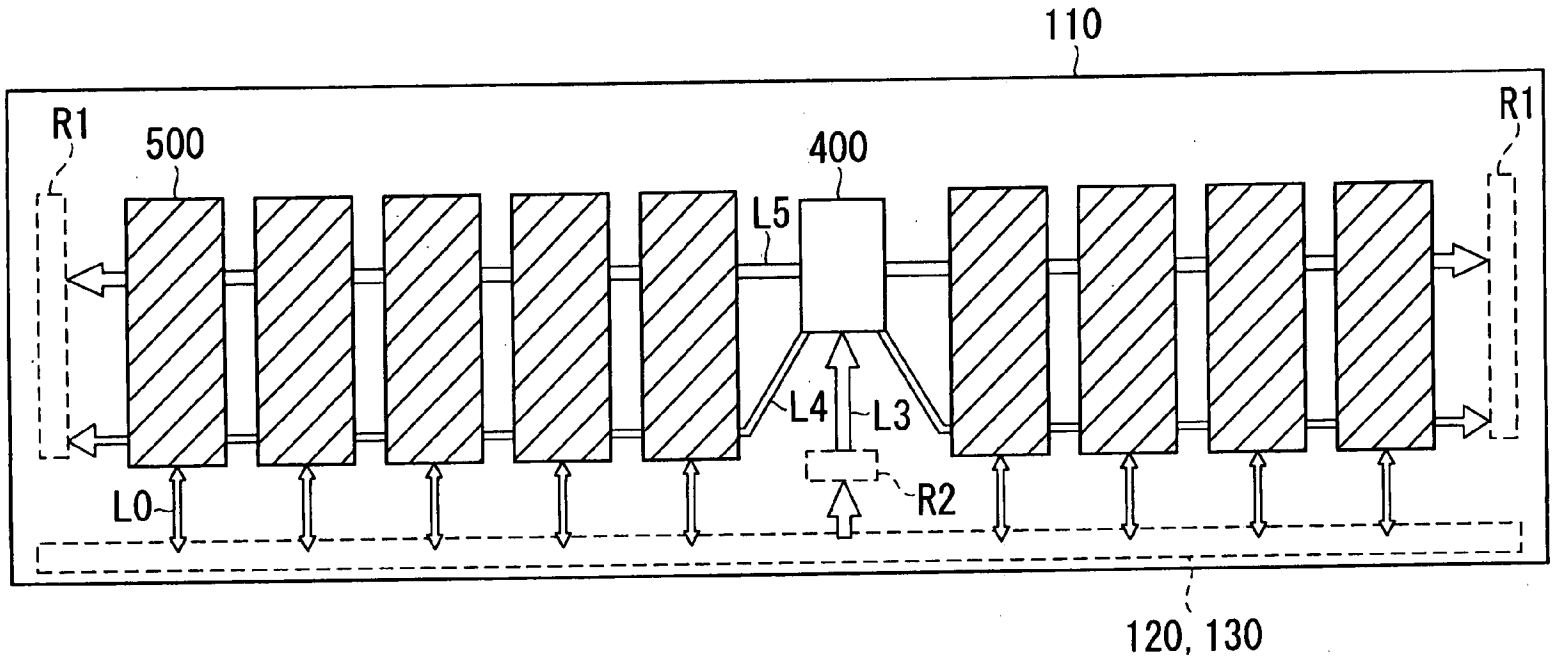


FIG.25

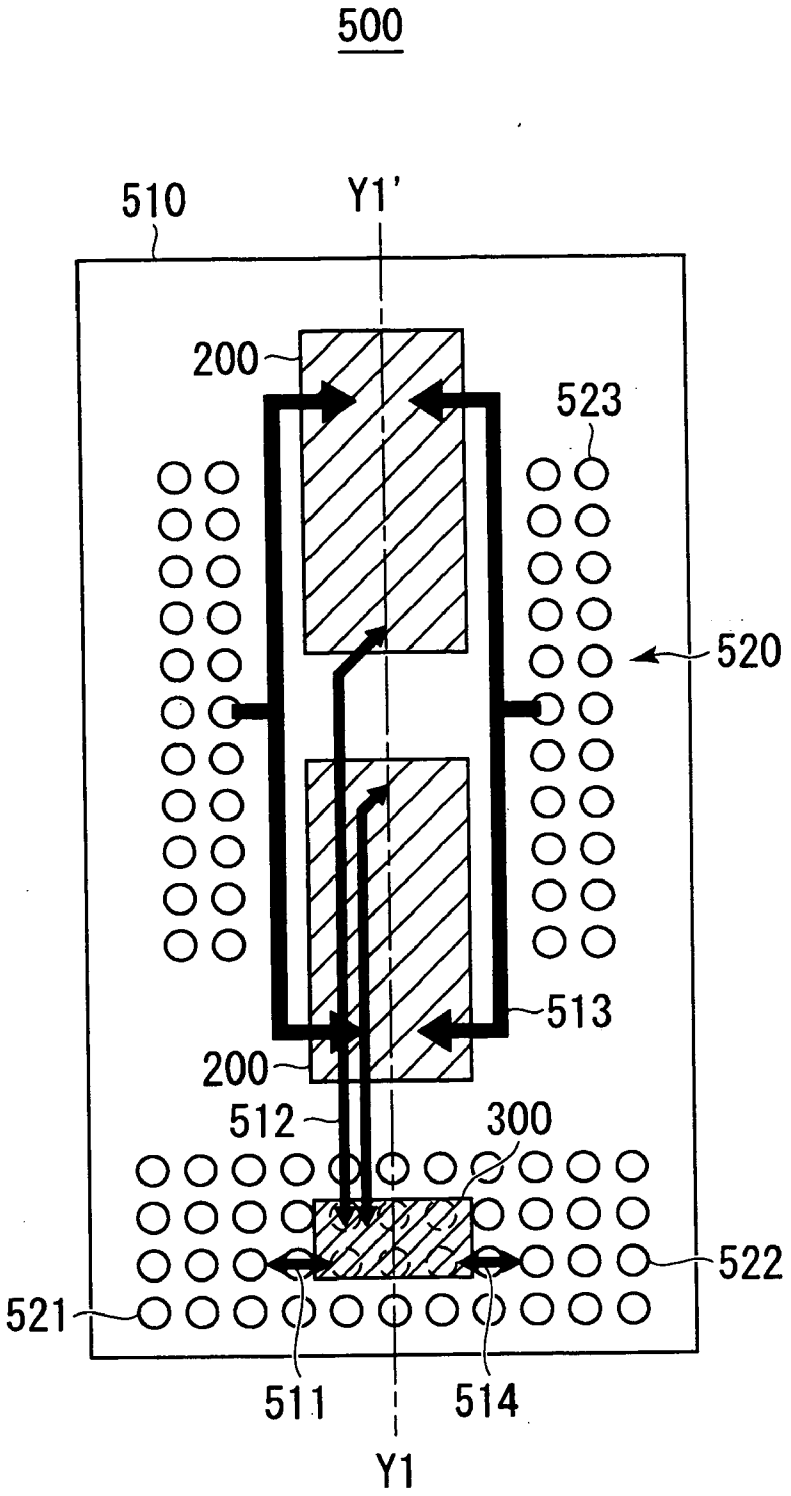


FIG.26

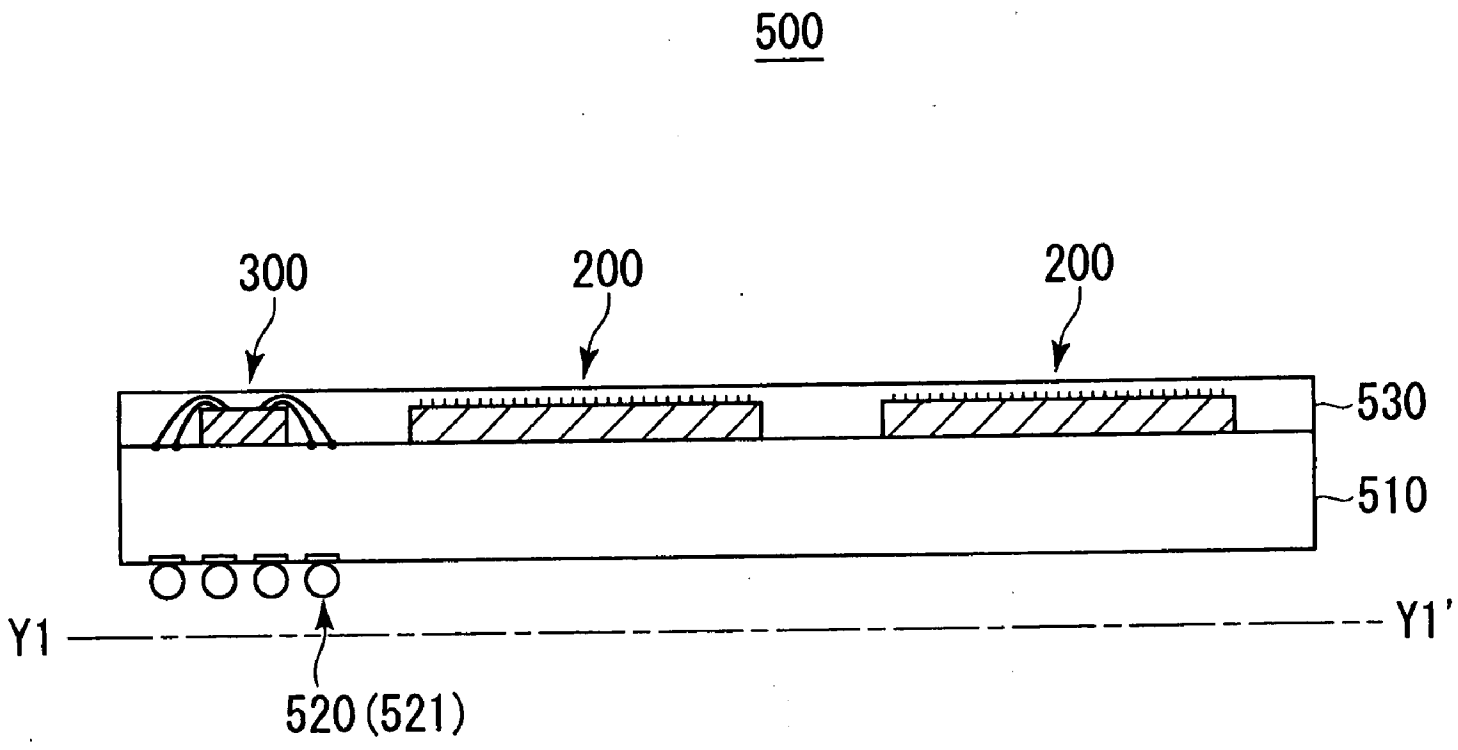


FIG.27

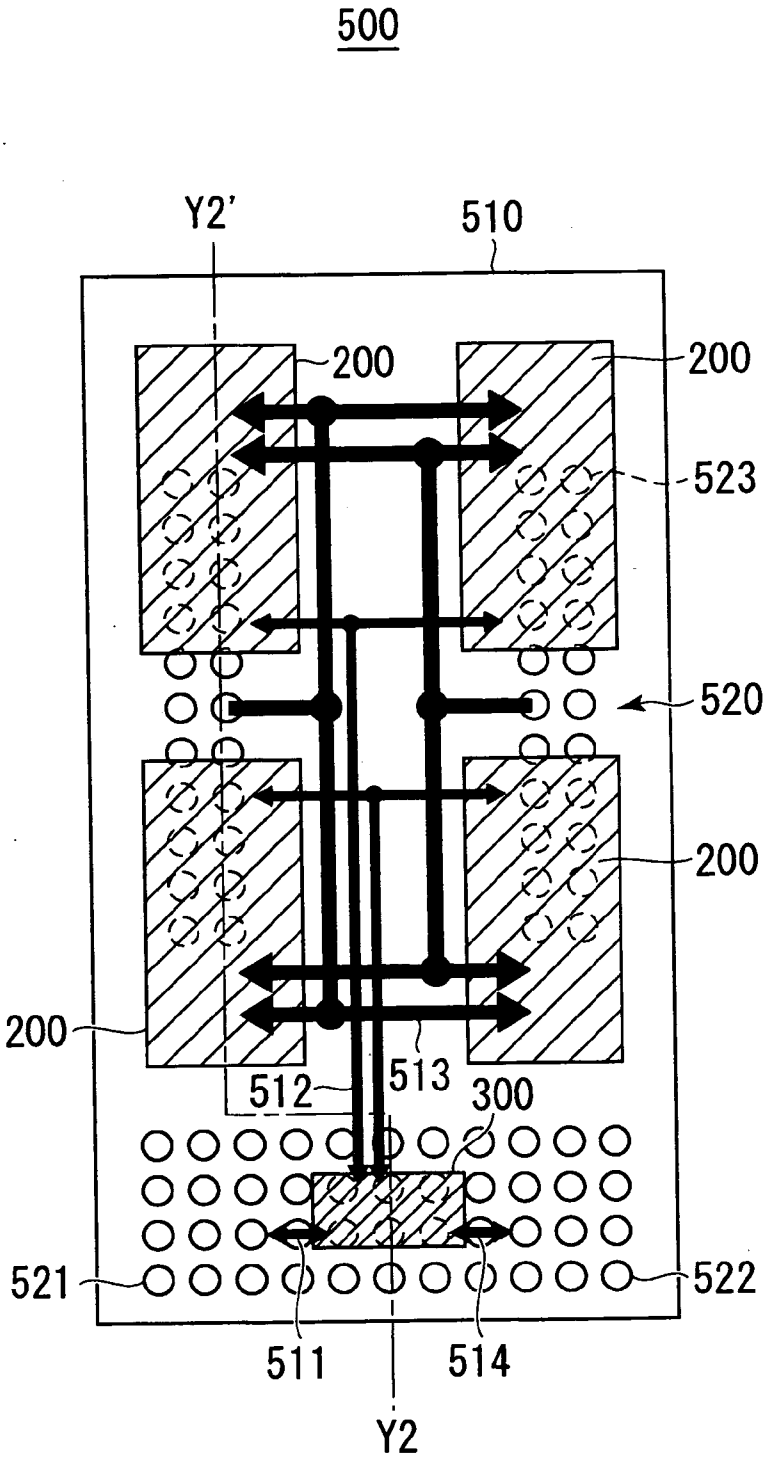


FIG.28

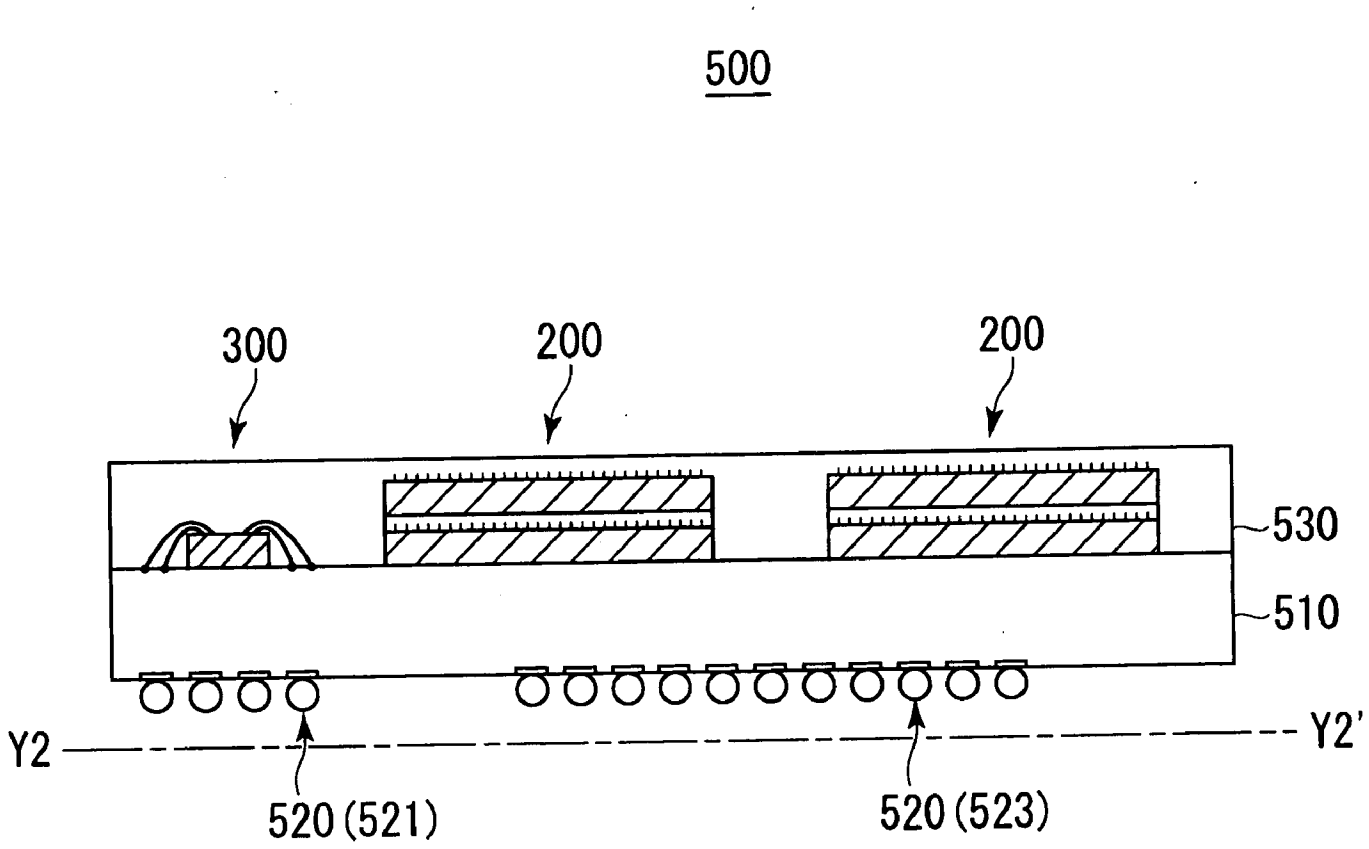


FIG.29

LOAD REDUCED MEMORY MODULE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a memory module, and particularly relates to a Load Reduced memory module.

[0003] 2. Description of Related Art

[0004] A memory module such as a DIMM (Dual Inline Memory Module) has a configuration in which a large number of memory chips such as DRAMs (Dynamic Random Access Memories) are mounted on a module substrate. Such a memory module is inserted in a memory slot provided on a motherboard, thereby a data transfer is performed between a memory controller and the memory module. In recent years, because a system requires a considerable amount of memory capacity, it is hard to provide the required memory capacity with a single memory module. Therefore, in most cases, the motherboard includes a plurality of memory slots, so that a plurality of memory modules can be mounted on the motherboard.

[0005] However, when a plurality of memory modules are mounted on a motherboard, a load capacity of a data line on the motherboard increases, resulting in a degradation of signal quality. Although it does not cause a serious problem when a data transfer rate between the memory controller and the memory module is relatively low, it may cause a serious problem that the data transfer cannot be performed in a proper manner due to the degradation of the signal quality when the data transfer rate increases to a certain level. In recent years, a data transfer rate as high as about 1.6 Gbps to 3.2 Gbps is required, and in order to realize such a high speed data transfer, it is necessary to reduce the load capacity of the data line on the motherboard to a sufficiently low level.

[0006] A so-called Fully Buffered memory module is known as a memory module in which the load capacity of the data line can be reduced (Japanese Patent Application Laid-open No. 2008-135597). In a write operation of the Fully Buffered memory module, a dedicated chip called an Advanced Memory Buffer (AMB) once receives all write data supplied from the memory controller, and then the AMB supplies the write data to a predetermined memory chip. A read operation is opposite to the write operation, in which all read data output from a memory chip is once supplied to the AMB, and then the read data is supplied from the AMB to the memory controller. As a result, because the memory controller does not experience the load capacity of each memory chip, the load capacity of the data line is considerably reduced.

[0007] However, because the AMB employed in the Fully Buffered memory module is a sophisticated chip, which is relatively expensive, it causes a problem that the cost of the memory module considerably increases. Further, because an interface between the memory controller and the AMB is different from a typical interface between the memory controller and the memory chip in the Fully Buffered memory module, it causes another problem that a conventional memory controller cannot be used as it is.

[0008] Because of such a background, a memory module called a Load Reduced memory module has been recently proposed. The Load Reduced memory module is a memory module in which a register buffer is used instead of the AMB. Because the register buffer is a chip that only buffers signals such as data and command/address, it can be provided at low cost. In addition, because an interface between the memory controller and the register buffer has no difference from the typical interface between the memory controller and the memory chip in the Load Reduced memory module, the conventional memory controller can be used as it is.

[0009] However, from a result of extensive researches on the Load Reduced memory module by the present inventors, it has been found that, when the data transfer rate is considerably high, simply using a single register buffer is not sufficient to maintain the signal quality on the module substrate. To deal with this problem, the present inventors performed further researches on a Load Reduced memory module in which a considerably high data transfer rate can be realized. The present invention has been achieved as a result of such researches.

SUMMARY

[0010] In one embodiment, there is provided a memory module comprising: a module substrate including a plurality of data connectors; a plurality of memory chips mounted on the module substrate, each of the memory chips including at least one data terminal; and a plurality of data register buffers mounted on the module substrate, each of the data register buffers being assigned to at least two memory chips, wherein each of the data register buffers includes M first input/output terminals each being connected to an associated one of the data connectors via a first data line formed on the module substrate, where M is a positive integer equal to or larger than 1, and N second input/output terminals each being connected to the data terminal of corresponding memory chips via a second data line formed on the module substrate, where N is a positive integer equal to or larger than 2M, so that number of the second data lines is N/M times number of the first data lines.

[0011] According to the present invention, because a plurality of data register buffers are mounted on a module substrate and numbers of data lines on a controller side and a memory chip side viewed from the data register buffers are asymmetrically provided, the load capacity of the data line on the module substrate is considerably reduced. This makes it possible to enhance the signal quality on the module substrate. As a result, it is possible to realize a considerably high data transfer rate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The above features and advantages of the present invention will be more apparent from the following description of certain preferred embodiments taken in conjunction with the accompanying drawings, in which:

[0013] FIG. **1** is a schematic diagram of a configuration of a memory module **100** according to an embodiment of the present invention;

[0014] FIG. **2** is a block diagram of a configuration of an information processing system **10** including the memory module **100** according to the present embodiment;

[0015] FIG. **3** is a perspective view of a part of a configuration of a motherboard **21** on which the memory system **20** is mounted;

[0016] FIG. **4** is a perspective view of a part of a configuration of a motherboard **21** on which the memory system **20** is mounted;

[0017] FIG. **5** is a block diagram of the configuration of the data register buffer **300**;

[0018] FIG. **6** is a block diagram of the configuration of the command/address/control register buffer **400**;

[0019] FIG. **7** is a connection diagram of the memory module **100**;

[0020] FIGS. **8**A and **8**B are schematic diagrams for explaining a data transfer path for transferring 1-bit data in the memory module **100** according to the present embodiment, where FIG. **8**A is a layout diagram and FIG. **8**B is a connection diagram

[0021] FIGS. **9**A and **9**B are schematic diagrams for explaining a data transfer path for transferring 1-bit data when the data lines L**1** and L**2** are put together in a single data line, where

[0022] FIG. **9**A is a layout diagram and FIG. **9**B is a connection diagram;

[0023] FIG. **10** is a timing chart for explaining an interleaving operation using the two data lines L**1** and L**2**;

[0024] FIG. **11** is a timing chart for explaining a read operation of the memory module **100** according to the present embodiment;

[0025] FIG. **12** is a timing chart for explaining the write operation of the memory module **100** according to the present embodiment;

[0026] FIG. **13** is a flowchart for explaining the initializing operation of the memory module **100** at the time of activation;

[0027] FIGS. **14**A and **14**B are timing charts for explaining the write leveling operation between the data register buffer **300** and the memory chip **200**, where FIG. **14**A is a timing chart at the time of starting the leveling and FIG. **14**B is a timing chart at the time of ending the leveling;

[0028] FIG. **15** is a timing chart for explaining the read leveling operation between the data register buffer **300** and the memory chip **200**;

[0029] FIGS. **16**A and **16**B are timing charts for explaining the write leveling operation between the memory controller **12** and the data register buffer **300**, where FIG. **16**A is a timing chart at the time of starting the leveling and FIG. **16**B is a timing chart at the time of ending the leveling;

[0030] FIG. **17** is a timing chart for explaining the read leveling operation between the memory controller **12** and the data register buffer **300**;

[0031] FIG. **18** is a timing chart for explaining a problem that occurs when performing the ODT operation without using the DLL circuit;

[0032] FIG. **19** is a timing chart for explaining a read-to-read operation when both the ODT function and the DLL circuit are in an ON state;

[0033] FIG. **20** is a timing chart for explaining the read-to-read operation when both the ODT function and the DLL circuit are in an OFF state;

[0034] FIG. **21** is a timing chart for explaining a write-to-write operation when both the ODT function and the DLL circuit are in an ON state;

[0035] FIG. **22** is a timing chart for explaining the write-to-write operation when both the ODT function and the DLL circuit are in an OFF state;

[0036] FIGS. **23**A and **23**B are schematic diagrams for explaining a data transfer path for transferring 1-bit data in a memory module according to a modification of the present embodiment, where FIG. **23**A is a layout diagram and FIG. **23**B is a connection diagram;

[0037] FIGS. **24**A and **24**B are schematic diagrams for explaining a data transfer path for transferring 1-bit data in a memory module according to another modification of the present embodiment, where FIG. **24**A is a layout diagram and FIG. **24**B is a connection diagram;

[0038] FIG. **25** is a schematic diagram of a configuration of a memory module according to still another modification of the present embodiment;

[0039] FIG. **26** is a plan view showing a configuration of the sub-module **500**;

[0040] FIG. **27** is a cross section of the sub-module **500** cut along a line Y**1**-Y**1**' shown in FIG. **26**;

[0041] FIG. **28** is a plan view showing another configuration of the sub-module **500**; and

[0042] FIG. **29** is a cross section of the sub-module **500** cut along a line Y**2**-Y**2**' shown in FIG. **28**.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0043] Preferred embodiments of the present invention will be explained below in detail with reference to the accompanying drawings.

[0044] FIG. **1** is a schematic diagram of a configuration of a memory module **100** according to an embodiment of the present invention.

[0045] As shown in FIG. **1**, the memory module **100** according to the present embodiment includes a module substrate **110**, a plurality of memory chips **200** mounted on the module substrate **110**, a plurality of data register buffers **300**, and a command/address/control register buffer **400**.

[0046] In the present embodiment, the memory module **100** includes thirty-six memory chips **200**. When it is necessary to specify each of the memory chips, the memory chips are respectively represented by memory chips **200-0** to **200-35**. Furthermore, in the present embodiment, the memory module **100** includes nine data register buffers **300**. When it is necessary to specify each of the data register buffers, the data register buffers are respectively represented by data register buffers **300-0** to **300-8**. On the other hand, the command/address/control register buffer **400** is provided as a single unit. However, it is not essential to set the number of units of the command/address/control register buffer **400** to one, but two or more units of the command/address/control register buffer **400** can be mounted without any limitation.

[0047] The module substrate **110** is a printed circuit board that includes a multilayer wiring. The planar shape of the module substrate **110** is substantially rectangle, as shown in FIG. **1**, with a long side in the X direction and a short side in the Y direction. On one side of the module substrate **110** along the X direction, which is the long side, a plurality of data connectors **120** and a plurality of command/address/control connectors **130** are provided. The data connectors **120** and the command/address/control connectors **130** are terminals for making an electrical connection with a memory controller via a memory slot, which will be described later.

[0048] The data connectors **120** are connectors for exchanging write data to be written in the memory chip **200** and read data read from the memory chip **200** between the memory module **100** and the memory controller. Although it is not particularly limited, the number of pins of the data connectors **120** is seventy two in the present embodiment. As shown in FIG. **1**, among the seventy-two data connectors **120**, data connectors corresponding to the memory chips **200-0** to **200-19** are arranged in an area **110**a that is located substantially right below the memory chips **200-0** to **200-19**, and data connectors corresponding to the memory chips **200-20** to

200-35 are arranged in an area **110***b* that is located substantially right below the memory chips **200-20** to **200-35**.

[0049] The command/address/control connectors **130** are connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer **400**. As shown in FIG. **1**, the command/address/control connectors **130** are arranged in an area **110***c* that is located between the area **110***a* and the area **110***b*.

[0050] The memory chips **200** are, for example, DRAMs. The memory chips **200-0**, **200-2**, . . . with even branch numbers are mounted on one surface of the module substrate **110** (a first surface), and the memory chips **200-1**, **200-3**, . . . with odd branch numbers are mounted on the other surface of the module substrate **110** (a second surface). Two corresponding memory chips, for example, the memory chips **200-0** and **200-1** are mounted at positions facing each other across the module substrate **110**, respectively.

[0051] The memory module **100** according to the present embodiment has a so-called 4-Rank configuration. The number of Ranks indicates the number of memory spaces that can be selected in an exclusive manner. Although the same address is assigned to each of the Ranks, one of the Ranks is selected by exclusively activating a chip select (CS) signal or a clock enable (CKE) signal.

[0052] In the present embodiment, four memory chips **200** constitute a single group (a single set), and the four memory chips **200** constituting the single group belong to different Ranks from each other. For example, the memory chips **200-0** to **200-3** constitute a single group, and the memory chips **200-0** to **200-3** belong to different Ranks from each other.

[0053] As shown in FIG. **1**, the four memory chips **200** constituting a single group are connected to one of the data register buffers **300**. For example, the group of the memory chips **200-0** to **200-3** is connected to the data register buffer **300-0**. Among the memory chips **200-0** to **200-3**, the memory chips **200-0** and **200-1** that are mounted on the upper side of the module substrate **110** are connected to the data register buffer **300-0** via a data line L**1**, and the memory chips **200-2** and **200-3** that are mounted on the lower side of the module substrate **110** are connected to the data register buffer **300-0** via a data line L**2**. An arrow of each of the data lines L**1** and L**2** shown in FIG. **1** indicates a line of 1 byte (8 bits). Both the data lines L**1** and L**2** are formed inside the module substrate **110**.

[0054] An operation of the memory chip **200** is controlled based on the command signal, the address signal, the control signal, and the clock signal supplied from the command/address/control register buffer **400**. Details on the memory chip **200** will be described later.

[0055] A single data register buffer **300** is allocated for every four memory chips **200**, as described above, so that nine data register buffers **300** are arranged along the X direction, which is the long side. The data register buffer **300** is a chip for buffering write data that is transferred via a data line L**0** and outputting the write data to either one of the data lines L**1** and L**2**, and at the same time, buffering read data that is transferred via either one of the data lines L**1** and L**2** and outputting the read data to the data line L**0**. The data line L**0** is also formed inside the module substrate **110**.

[0056] With the above configuration, the single data register buffer **300**, the data connectors **120** and the four memory chips **200** corresponding to the data register buffer **300** constitute a group G. The memory chips **200**, the data register buffer **300**, and the data connectors **120** included in the same group are arranged along the Y direction, which is the short side, and a plurality of groups G formed in the above manner are arranged along the X direction, which is the long side. Therefore, a relative positional relationship between each of the data register buffers **300** and corresponding four memory chips **200** becomes constant in all the groups G.

[0057] With this arrangement, a line length of the data line L**0** can be shortened, and at the same time, the line length of the data line L**0** can be made substantially equal among the groups. Similarly, line lengths of the data lines L**1** and L**2** can be shortened, and at the same time, the line lengths of the data lines L**1** and L**2** can be made substantially equal among the groups.

[0058] An operation of the data register buffer **300** is controlled based on the control signal supplied from the command/address/control register buffer **400**. Details on the data register buffer **300** will be described later.

[0059] Only a single command/address/control register buffer **400** is mounted on the module substrate **110**. As shown in FIG. **1**, the command/address/control register buffer **400** is arranged at an approximate center portion of the module substrate **110** in the X direction, which is the long side.

[0060] The command/address/control register buffer **400** receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a command/address/control signal and the like) that are supplied from the command/address/control connectors **130** through an input terminal **401**, buffers the signals, and supplies the signals to the memory chips **200**. At the same time, the command/address/control register buffer **400** generates a control signal. The command/address/control signal to be supplied to the memory chips **200** are output through an output terminal **402**, and the control signal to be supplied to the data register buffers **300** are output through an output terminal **403**.

[0061] The output terminal **402** is provided at each of the left side and the right side of the command/address/control register buffer **400**. For example, the output terminal **402** at the left side is commonly connected to the memory chips **200-0** to **200-19** except for a control signal that is used to select the Rank. That is, the command signal, the address signal, and the clock signal are commonly supplied to the memory chips **200-0** to **200-19**. Similarly, the output terminal **403** is provided at each of the left side and the right side of the command/address/control register buffer **400**. For example, the output terminal **403** at the left side is commonly connected to the data register buffers **300-0** to **300-4**, so that the generated control signal is commonly supplied to the data register buffers **300-0** to **300-4**.

[0062] In addition, on the module substrate **110**, a terminating resistor R**1** is provided at both edges in the X direction to prevent a reflection of the command/address signal and the control signal output from the command/address/control register buffer **400**. Furthermore, in order to prevent a reflection wave of the command/address/control signal that is input to the command/address/control register buffer **400**, a stub resistor R**2** is inserted on a command/address/control line L**3** that connects the command/address/control connectors **130** and the command/address/control register buffer **400**. Details on the command/address/control register buffer **400** will be described later.

[0063] FIG. **2** is a block diagram of a configuration of an information processing system **10** including the memory module **100** according to the present embodiment.

[0064] The information processing system **10** shown in FIG. **2** includes a CPU **11**, a memory control hub (MCH) **12**, and various devices that are connected to the CPU **11** via an interface controller hub (ICH) **13**.

[0065] The memory module **100** shown in FIG. **1** and a graphic controller **15** are connected to the MCH **12**. As shown in FIG. **2**, the memory module **100** and the MCH **12** constitute a memory system **20**, where the MCH **12** has a controller function for the memory module **100**. That is, the MCH **12** functions as a memory controller for the memory module **100**.

[0066] A storage device **16**, an I/O device **17**, and a BIOS (Basic Input/Output System) **18** are connected to the ICH **13**. The storage device **16** includes a magnetic drive such as a hard disk drive, an optical drive such as a CD-ROM drive, and the like. The I/O device **17** includes an input device such as a keyboard and a mouse, an output device such as a speaker, and a network device such as a modem and a LAN. The BIOS **18** is a kind of firmware that stores therein various pieces of basic information about the information processing system **10**, which is formed by a nonvolatile memory such as a flash memory.

[0067] FIG. **3** is a perspective view of a part of a configuration of a motherboard **21** on which the memory system **20** is mounted.

[0068] As shown in FIG. **3**, a memory slot **22** is provided on the motherboard **21**, so that the memory module **100** is inserted in the memory slot **22**. On the other hand, a memory controller **12** is directly mounted on the motherboard **21**. As described above, a plurality of memory chips **200** are mounted on the memory module **100**.

[0069] On a signal path between the memory controller **12** and the memory chips **200**, there exist a line **23** formed on the motherboard **21** and the data line L**0** and the command/address/control line L**3** formed on the module substrate **110**. However, as described above referring to FIG. **1**, in the memory module **100** according to the present embodiment, because the data register buffer **300** is connected to the data line L**0**, the memory controller **12** cannot experience the load capacity of the memory chips **200** that exist on the signal path beyond the data register buffer **300**. Similarly, because the command/address/control register buffer **400** is connected to the command/address/control line L**3**, the memory controller **12** cannot experience the load capacity of the memory chips **200** that exist on the signal path beyond the command/address/control register buffer **400**. Therefore, the load capacity of the signal path that connects the memory controller **12** and the memory module **100** is reduced, making it possible to ensure an excellent signal quality even with a high data transfer rate.

[0070] Although only a single memory slot **22** is provided on the motherboard **21** in the memory system **20** shown in FIG. **3**, in actual cases, a plurality of memory slots (for example, four) are provided on the memory system, so that the memory module **100** is mounted on each of the memory slots. As the number of units of the memory module **100** increases, the load capacity of the signal path increases by the number of memory modules. However, according to the present embodiment, because the load capacity per memory module is considerably smaller than that of a conventional memory module, it is possible to perform a high speed data transfer even when a plurality of memory modules are mounted.

[0071] A configuration of the memory chip **200** is explained next.

[0072] FIG. **4** is a block diagram of a configuration of the memory chip **200**.

[0073] The memory chip **200** is a DRAM, which includes, as shown in FIG. **4**, a clock'terminal **201**, a command terminal **202**, a control terminal **206**, an address terminal **203**, a data input/output terminal **204**, and a data strobe terminal **205** as external terminals. Among these terminals, the clock terminal **201**, the command terminal **202**, the control terminal **206**, and the address terminal **203** are connected to the command/address/control register buffer **400** via a command/address/control line L**5** shown in FIG. **1**. The data input/output terminal **204** and the data strobe terminal **205** are connected to the data register buffer **300** via the data line L**1** or the data line L**2** shown in FIG. **1**. Although not shown in FIG. **1**, the memory chip **200** further includes other terminals such as a power supply terminal.

[0074] The clock terminal **201** is a terminal to which a clock signal CK is supplied. The clock signal CK is then supplied to an internal clock generating circuit **211**. An internal clock ICLK, which is an output of the internal clock generating circuit **211**, is supplied to various internal circuits. The clock signal CK is also supplied to a DLL circuit **212**. The DLL circuit **212** takes a role of generating an internal clock LCLK and supplying the internal clock LCLK to a data input/output circuit **213** and a data strobe signal input/output circuit **214**. The internal clock LCLK is a signal that is phase-controlled with respect to the clock signal CK, of which a phase is slightly advanced with respect to the clock signal CK such that phases of read data DQ and a data strobe signal DQS match with a phase of the clock signal CK.

[0075] It is selected based on a set content in a mode register whether to use the DLL circuit **212**. That is, when "DLL on mode" is set in a mode register **215**, the DLL circuit **212** is enabled, so that the internal clock LCLK is phase-controlled with respect to the clock signal CK. On the other hand, when "DLL off mode" is set in the mode register **215**, the DLL circuit **212** is disabled (the clock signal CK is shortcut), so that the internal clock LCLK is not phase-controlled with respect to the clock signal CK.

[0076] The command terminal **202** is a terminal to which a command signal CMD that includes a row address strobe (RAS) signal, a column address strobe (CAS) signal, a write enable (WE) signal, and the like is supplied. The control terminal **206** is a terminal to which a control signal CTRL for each Rank, such as a chip select (CS) signal, a clock enable (CKE) signal, and an on die termination (ODT) signal, is supplied. By the chip select (CS) signal, a DRAM for which a command is to be issued is switched, and an activation of a clock system and a control of an on die termination in the DRAM are performed. The command signal CMD is supplied to a command decoder **216**. The command decoder **216** is a circuit that generates various internal commands ICMD by storing, decoding, and counting the command signal in synchronization with the internal clock ICLK. The generated internal commands are supplied to various control circuits (not shown) including the mode register **215**. The control signal CTRL is supplied to a control circuit **218**. The control circuit **218** is a circuit that generates an internal control signal such as the ODT signal based on the control signal CTRL.

[0077] The address terminal **203** is a terminal to which an address signal ADD is supplied. The address signal is then supplied to an address latch circuit **217**. The address latch circuit **217** is a circuit that latches the address signal ADD in synchronization with the internal clock ICLK. Among the address signals ADD that are latched in the address latch circuit **217**, a row address is supplied to a row decoder **221** and a column address is supplied to a column decoder **222**. In addition, upon entering a mode register set, the address signal ADD is supplied to the mode register **215**, by which a content of the mode register **215** is updated.

[0078] The row decoder **221** is a circuit that selects one of word lines WL included in a memory cell array **230**. In the memory cell array **230**, a plurality of word lines WL and a plurality of bit lines BL intersect with each other, and a memory cell MC is arranged at each intersection point (only a single word line WL, a single bit line BL, and a single memory cell MC are shown in FIG. **4**). The bit line BL is connected to one of sense amplifiers SA that are included in a sense amplifier array **231**. The column decoder **222** performs a selection of the sense amplifier SA.

[0079] The selected sense amplifier SA is connected to the data input/output circuit **213**. The internal clock LCLK and an internal data strobe signal PDQS are supplied to the data input/output circuit **213**. In a read operation, the data input/output circuit **213** outputs read data in synchronization with the internal clock LCLK, and in a write operation, the data input/output circuit **213** loads write data in synchronization with the internal data strobe signal PDQS. With this arrangement, in the read operation, the read data read out from the memory cell array **230** is output from the data input/output terminal **204**, and in the write operation, the write data received from the data input/output terminal **204** is supplied to the memory cell array **230**.

[0080] The data strobe terminal **205** is a terminal for performing input and output of the data strobe signal DQS, which is connected to the data strobe signal input/output circuit **214**. The data strobe signal input/output circuit **214** generates the internal data strobe signal PDQS described above, and supplies it to the data input/output circuit **213**.

[0081] The ODT signal, which is an output of the control circuit **218**, is also supplied to the data input/output circuit **213** and the data strobe signal input/output circuit **214**. When the ODT signal is activated, both the data input/output circuit **213** and the data strobe signal input/output circuit **214** function as terminating resistors.

[0082] The overall configuration of the memory chip **200** is as described above. A configuration of the data register buffer **300** is explained next.

[0083] FIG. **5** is a block diagram of the configuration of the data register buffer **300**.

[0084] As shown in FIG. **5**, the data register buffer **300** includes a FIFO (Write) circuit **301** and a FIFO (Read) circuit **302**. The FIFO (Write) circuit **301** buffers data DQ that is supplied via an input/output terminal **340** with a data strobe signal DQS that is supplied via an input/output terminal **350**. The FIFO (Read) circuit **302** buffers data DQ that is supplied via an input/output terminal **341** or **342** with a data strobe signal DQS that is supplied via an input/output terminal **351** or **352**. A strobe generating circuit **376** generates a data strobe signal DQS to be supplied to the data connectors **120**, in synchronization with an internal clock LCLKR that is generated by a DLL circuit **310**. A strobe generating circuit **374** generates a data strobe signal DQS to be supplied to the memory chip **200**, in synchronization with an internal clock LCLKW that is generated by the DLL circuit **310**.

[0085] The FIFO circuits **301** and **302** shown in FIG. **5** are circuits that perform input and output of 1-bit data, so that in an actual case, the number of sets of the FIFO circuits **301** and **302** as many as a width of input/output data are provided. In the present embodiment, because a single data register buffer **300** inputs and outputs 1-byte data, 8 sets of the FIFO circuits **301** and **302** are required.

[0086] The input/output terminals **340** and **350** are connected to the data connectors **120** via the data line L**0**. On the other hand, the input/output terminals **341** and **351** are connected to the memory chip **200** via the data line L**1**, and the input/output terminals **342** and **352** are connected to the memory chip **200** via the data line L**2**. In this manner, for the data register buffer **300**, the number of the input/output terminals (M) to be connected to the memory controller **12** and the number of the input/output terminals (N) to be connected to the memory chip **200** are different from each other, which is, in the present embodiment, N=2M. In other words, the number of the data lines L**1** and L**2** is N/M times the number of the data line L**0** (two times in the present embodiment).

[0087] An output operation timing of the FIFO (Write) circuit **301** is defined by the internal clock LCLKW that is generated by the DLL circuit **310**. An output operation timing of the FIFO (Read) circuit **302** is defined by the internal clock LCLKR that is generated by the DLL circuit **310**. The DLL circuit **310** is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer **400**, having the same circuit configuration and function as that of the DLL circuit **212** provided in the memory chip **200**. It is selected based on a set content in a data register control circuit **320** whether to use the DLL circuit **310**. The DLL circuit **310** can be replaced with a PLL circuit.

[0088] The data register control circuit **320** is a circuit that controls the operation of the data register buffer **300** based on a control signal DRC that is supplied from the command/address/control register buffer **400**. Specifically, the data register control circuit **320** controls operations of an input buffer INB and an output buffer OUTB by generating a buffer control signal BC, and at the same time, controls operations of selectors **331** to **334** by generating a select signal SEL. Contents of controlling the output buffer OUTB include, for example, an adjustment of output impedance and an on/off control of an ODT operation. It is selected based on a set content in a mode register **321** that is included in the data register control circuit **320** whether to use the ODT function.

[0089] In addition, the data register control circuit **320** generates a feedback signal DRF and supplies it to the command/address/control register buffer **400**. The feedback signal DRF is a signal indicating a current status of the data register buffer **300**.

[0090] Furthermore, the data register control circuit **320** includes a write leveling circuit **322** and a read leveling circuit **323**. The write leveling circuit **322** is a circuit for performing a write leveling operation, and the read leveling circuit **323** is a circuit for performing a read leveling operation. Details on the write leveling operation and the read leveling operation will be described later.

[0091] The selector **333** is a circuit that supplies data DQ that is an output of the FIFO (Write) circuit **301** to either one of the input/output terminals **341** and **342**. The selector **334** is a circuit that selects data DQ input from either one of the

input/output terminals **341** and **342** and supplies the selected data DQ to the FIFO (Read) circuit **302**. The selectors **331** and **332** perform the similar functions as those of the selectors **333** and **334**, respectively. Specifically, the selector **332** selects a data strobe signal DQS input from either one of the input/output terminals **351** and **352**. A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit **372**, and then the data strobe signal DQS is supplied to the FIFO (Read) circuit **302** as an input trigger signal. The selector **331** supplies the data strobe signal DQS that is supplied from the strobe generating circuit **374** to either one of the input/output terminals **351** and **352**. A phase of the data strobe signal DQS generated by the strobe generating circuit **374** is delayed by about **90** degrees with respect to the internal clock LCLKW by a delay circuit **370**. Each of the selections by the selectors **331** to **334** is specified by the select signal SEL that is an output of the data register control circuit **320**.

[0092] In this manner, the data register buffer **300** buffers the write data that is transferred via the data line L**0** and outputs the write data to either one of the data lines L**1** and L**2**, and buffers the read data that is transferred via either one of the data lines L**1** and L**2** and outputs the read data to the data line L**0**. Because the data register buffer **300** only performs the buffering of the data, transfer rates of the write data and the read data that are transferred via the data line L**0** and transfer rates of the write data and the read data that are transferred via the data lines L**1** and L**2** are equal to each other.

[0093] Therefore, the data register buffer **300** can be implemented with a chip that is provided at relatively low cost instead of an expensive chip such as an AMB used in a Fully Buffered memory module.

[0094] The overall configuration of the data register buffer **300** is as described above. A configuration of the command/address/control register buffer **400** is explained next.

[0095] FIG. **6** is a block diagram of the configuration of the command/address/control register buffer **400**.

[0096] As shown in FIG. **6**, the command/address/control register buffer **400** includes the input terminal **401** for connecting to the command/address/control connectors **130**, the output terminal **402** for connecting to the memory chip **200**, and the output terminal **403** and an input terminal **404** for connecting to the data register buffer **300**.

[0097] The command/address/control signal that is supplied from the memory controller **12** is input from the input terminal **401**. Among input command/address/control signals, the command signal CMD, the address signal ADD, and the control signal CTRL are supplied to a register circuit **410**, and the clock signal CK is supplied to a PLL circuit **420**. The register circuit **410** is a circuit that buffers the command signal CMD, the address signal ADD, and the control signal CTRL, and the buffered command signal CMD, address signal ADD, and control signal CTRL are supplied to the memory chip **200** via the output terminal **402**.

[0098] An operation timing of the register circuit **410** is defined by an internal clock LCLKCA that is generated by the PLL circuit **420**. The PLL circuit **420** is a circuit that generates the internal clock LCLKCA based on the clock signal CK supplied from the memory controller **12** having the same circuit configuration and function as that of the DLL circuit **212** provided in the memory chip **200**. It is selected based on a set content in a mode register **431** that is included in a control signal generating circuit **430** whether to use the PLL circuit **420**. The PLL circuit **420** can be replaced with a DLL circuit.

[0099] The control signal generating circuit **430** is a circuit that generates the control signal DRC to be supplied to the data register buffer **300** based on the command/address/control signal supplied via the input terminal **401**, of which an operation is performed in synchronization with the internal clock LCLKCA. The control signal DRC for the data register buffer **300** is supplied to the data register buffer **300** via the output terminal **403**. The feedback signal DRF is supplied to the control signal generating circuit **430** from the data register buffer **300** via the input terminal **404**.

[0100] The control signal DRC includes signals such as a signal indicating a direction of transmitting and receiving data, a signal for controlling an ODT timing at the data line L**0** side of the data register buffer **300**, a signal for controlling an ODT timing at the data lines L**1** and L**2** side, a signal for controlling on and off of the DLL circuit, a signal for controlling enable and disable of the data register buffer **300**, and a signal for performing a mode switching of the data register buffer **300** and a mode register set and the like. A separate line can be allocated to each of these signals, or a single common line can be allocated to a plurality of these signals. Alternatively, these signals can be transmitted to the data register buffer **300** as commands.

[0101] The overall configuration of the command/address/control register buffer **400** is as described above.

[0102] FIG. **7** is a connection diagram of the memory module **100** according to the present embodiment.

[0103] As shown in FIG. **7**, in the present embodiment, the data register buffer **300** intervenes between the data connectors. **120** and the memory chips **200**. The data connectors **120** and the data register buffer **300** are connected to each other with the data line L**0**, and the data register buffer **300** and the memory chips **200** are connected to each other with the data line L**1** or L**2**. In FIG. **7**, a plurality of data transferred through the data line L**0** is represented by data DQ-Pre, and a plurality of data transferred through the data lines L**1** and L**2** is represented by data DQ-Post. Similarly, a data strobe signal transferred through the data line L**0** is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L**1** or L**2** is represented by a data strobe signal DQS-Post.

[0104] Although the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer **300**, the timing is off between the data DQ-Pre and the data DQ-Post. The same is true for a relationship between the data strobe signal DQS-Pre and the data strobe signal DQS-Post. Therefore, in the present embodiment, it is required to perform a timing adjustment between the memory chips **200** and the data register buffer **300** and a timing adjustment between the data register buffer **300** and the memory controller in a separate manner. Details on the timing adjustments will be described later.

[0105] As described above, in the present embodiment, the four memory chips **200** are allocated to a single data register buffer **300**. The four memory chips **200** are memory chips that constitute different Ranks from each other, which are exclusively activated by the chip select (CS) signal or the clock enable (CKE) signal included in the control signal CTRL. The address signal ADD and the command signal CMD are commonly supplied to the four memory chips **200**.

[0106] The address signal ADD, the command signal CMD, the control signal CTRL, and the clock signal CK supplied to the memory chips **200** are supplied from the command/address/control register buffer **400**. The control signal DRC supplied to the data register buffer **300** is also supplied from the command/address/control register buffer **400**.

[0107] As shown in FIG. **7**, the command/address/control connectors **130** and the command/address/control register buffer **400** are connected to each other with the command/address/control line L**3**, the command/address/control register buffer **400** and the data register buffer **300** are connected to each other with a control line L**4**, and the command/address/control register buffer **400** and the memory chips **200** are connected to each other with a command/address/control line L**5**. In FIG. **7**, a command/address/control signal transferred through the command/address/control line L**3** is represented by a command/address signal ADD/CMD-Pre, and a command/address signal transferred through the command/address/control line L**5** is represented by a command/address signal ADD/CMD-Post. Similarly, a control signal transferred through the command/address/control line L**3** is represented by a control signal CNTRL-Pre, and a control signal transferred through the command/address/control line L**5** is represented by a control signal CNTRL-Post.

[0108] The clock signal CK to be supplied to the memory chip **200** and the data register buffer **300** is supplied from the command/address/control register buffer **400**. In FIG. **7**, a clock signal transferred through the command/address/control line L**3** is represented by a clock signal Clock-Pre, and a clock signal transferred through the command/address/control line L**5** is represented by a clock signal Clock-Post.

[0109] FIGS. **8**A and **8**B are schematic diagrams for explaining a data transfer path for transferring 1-bit data in the memory module **100** according to the present embodiment, where FIG. **8**A is a layout diagram and FIG. **8**B is a connection diagram.

[0110] As shown in FIGS. **8**A and **8**B, the 1-bit data is transferred via a predetermined connector **121** of the data connectors **120**. The connector **121** is connected to the data register buffer **300** via a single data line L**0**. As explained above referring to FIG. **5**, in the present embodiment, two data lines L**1** and L**2** are allocated to a single data line Lo. Specifically, the data line L**1** is commonly connected to the memory chips **200-0** and **200-1**, and the data line L**2** is commonly connected to the memory chips **200-2** and **200-3**.

[0111] With the above configuration, the load capacity of a single data line L**1** or L**2** is reduced, the number of branch points decreases, and a line length from a branch point is shortened. As a result, the signal quality of data transferred on the data lines L**1** and L**2** is enhanced. Specifically, terminals connected to the single data line L**1** are only three terminals total including data input/output terminals of the memory chips **200-0** and **200-1** and a data output terminal of the data register buffer **300**. Furthermore, because the memory chips **200-0** and **200-1** are arranged facing each other across the module substrate **110**, as shown in FIG. **8**A, if a branch point P is arranged in an area sandwiched by the memory chips **200-0** and **200-1**, the line length from the branch point to each of the memory chips **200-0** and **200-1** is considerably shortened. In addition, because the memory chips **200-0** to **200-3** are mounted at positions close to each other, a perspective difference in edges of the memory chips **200-0** to **200-3** is also suppressed to the minimum.

[0112] FIGS. **9**A and **9**B are schematic diagrams for explaining a data transfer path for transferring 1-bit data when the data lines L**1** and L**2** are put together in a single data line, where FIG. **9**A is a layout diagram and FIG. **9**B is a connection diagram.

[0113] As shown in FIGS. **9**A and **9**B, when the data lines L**1** and L**2** are put together in a single data line L**1**, the data register buffer **300** and the four memory chips **200-0** to **200-3** are commonly connected with the single data line L**1**. Therefore, as compared to the configuration shown in FIGS. **8**A and **8**B, the load capacity of the single data line L**1** increases, the number of branch points increases, and the line length from the branch point also increases. Specifically, terminals connected to the single data line L**1** become five terminals total including data input/output terminals of the memory chips **200-0** to **200-3** and the data output terminal of the data register buffer **300**. In addition, because the configuration becomes such that the line is branched into two at a branch point P**1** and further branched into two at a branch point P**2**, a line length from the branch point P**1** to each of the memory chips **200-0** to **200-3** increases.

[0114] On the other hand, in the present embodiment, because the two data lines L**1** and L**2** are employed, as shown in FIGS. **8**A and **8**B, the signal quality of data in the module substrate can be enhanced. Using the two data lines L**1** and L**2** doubles the number of lines for connecting the memory chips **200** and the data register buffer **300**. However, in the present embodiment, because the memory chips **200** and the data register buffer **300** constituting the same group G are arranged in the direction of the short side on the module substrate **110** as explained referring to FIG. **1**, there is an enough room for the line space. Therefore, even if the number of lines extending in the direction of the short side is doubled, it is possible to form the lines without difficulty.

[0115] Meanwhile, when a layout is taken in which data are concentrated in the center of the module substrate, as in the case of the Fully Buffered memory module, it is required to form a plurality of long data lines in the direction of the long side of the module substrate. In such a layout, because the total length of the data lines increases by a considerable amount as compared to the layout of the present embodiment, it is required to take a measure such as significantly increasing the number of insulating layers forming the module substrate in order to double the number of the data lines.. However, according to the present embodiment, because it does not cause such a problem, it is possible to double the number of lines for connecting the memory chips **200** and the data register buffer **300** without increasing the number of insulating layers forming the module substrate **110**.

[0116] FIG. **10** is a timing chart for explaining an interleaving operation using the two data lines L**1** and L**2**.

[0117] FIG. **10** shows a consecutive read operation from a Rank**0** to a Rank**3** with a case that a burst length is 4 bits (BL=4) (or a case that a burst operation is stopped at 4 bits by a burst chop). In the example shown in FIG. **10**, a read command is issued at times T**0**, T**2**, T**4**, and T**6** that are synchronized with the clock signal CK in the order of the Rank**0**, the Rank**2**, the Rank**1**, and the Rank**3**. In response to these read commands, after a lapse of a predetermined CAS latency (in this example, CL=12), 4-bit read data DQ is burst output.

[0118] As a result, in a period from a time T**12** to a time T**14**, a data transfer is performed from the memory chip **200** of the Rank**0** using the data line L**1**, in a period from the time T**14** to a time T**16**, a data transfer is performed from the

memory chip **200** of the Rank**2** using the data line L**2**, in a period from the time T**16** to a time T**18**, a data transfer is performed from the memory chip **200** of the Rank**1** using the data line L**1**, and in a period from the time T**18** to a time T**20**, a data transfer is performed from the memory chip **200** of the Rank**3** using the data line L**2**. That is, the data lines L**1** and L**2** are used in an alternate manner.

[0119] The read data sequentially transferred in the above manner are supplied to the data register buffer **300**, and after being buffered in a FIFO circuit included in the data register buffer **300**, output to the data line L**0**. In the example, shown in FIG. **10**, since the read data is input to the data register buffer **300**, the read data is output with one cycle delay.

[0120] In this manner, in the present embodiment, because the interleaving operation can be performed using the two data lines L**1** and L**2**, it is possible to perform a read operation for a plurality of memory chips without interruption. As a result, the read data output from the data register buffer **300** can also be supplied to the memory controller without interruption, so that the usage efficiency of a bus can be enhanced. Although the data lines L**1** and L**2** are not simultaneously used in the present embodiment, if the data lines L**1** and L**2** are put together in a single data line, it is required to spare a time equal to or longer than one cycle between read data output from different memory chips. On the other hand, in the present embodiment, because the two data lines L**1** and L**2** are alternately used, it is not necessary to put a time between read data output from different memory chips.

[0121] Although the read operation is explained as an example in FIG. **10**, a similar interleaving operation can be applied for a write operation.

[0122] The operation of the memory module **100** according to the present embodiment is explained below in more detail.

[0123] FIG. **11** is a timing chart for explaining a read operation of the memory module **100** according to the present embodiment.

[0124] In the read operation, an active command ACT and a read command Read are issued in order from the memory controller **12**. In the example shown in FIG. **11**, the active command ACT reaches the command/address/control connectors **130** at a time T-**5** that is synchronized with the clock signal CK, and the read command Read reaches the command/address/control connectors **130** at a time T**0**.

[0125] The commands ACT and Read reaching the command/address/control connectors **130** are input to the command/address/control register buffer **400**. At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the commands ACT and Read reaches the command/address/control connectors **130** and a timing at which the commands ACT and Read are input to the command/address/control register buffer **400**.

[0126] The command/address/control register buffer **400** registers the received commands ACT and Read with an input clock signal in the register circuit **410** shown in FIG. **6**, and then outputs them to the memory chip **200**. At this time, a synchronization with the output of the commands ACT and Read is taken by delaying the output of the clock signal CK by an amount equivalent to an additional ½ clock cycle. In addition, the command/address/control register buffer **400** supplies a read command Read to the data register buffer **300** as a part of the control signal DRC.

[0127] The memory chip **200** receives the commands ACT and Read, and starts an actual read operation. At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the commands ACT and Read are output from the command/address/control register buffer **400** and a timing at which the commands ACT and Read are input to the memory chip **200**.

[0128] Because CL=5 in the example shown in FIG. **11**, the memory chip **200** starts a burst output of read data DQ at a time T**5** in five clock cycles after receiving the read command Read. In the example shown in FIG. **11**, the burst length is **8** bits (BL=8). The read data DQ and a data strobe signal DQS burst output from the memory chip **200** are supplied to the data register buffer **300**.

[0129] The data register buffer **300** loads the read data DQ that is output from the memory chip **200** in the FIFO (Read) circuit **302** with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip **200** and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer **300**.

[0130] Thereafter, the data register buffer **300** performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit **302** to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.

[0131] The read operation of the memory module **100** according to the present embodiment is as described above. A write operation of the memory module **100** is explained next.

[0132] FIG. **12** is a timing chart for explaining the write operation of the memory module **100** according to the present embodiment.

[0133] In the write operation, the memory controller issues an active command ACT and a write command Write in order, and after a lapse of a write latency (WL) since the write command Write is issued, burst outputs write data. In the example shown in FIG. **12**, the active command ACT reaches the command/address/control connectors **130** at the time T-**5** that is synchronized with the clock signal CK, and the write command Write reaches the command/address/control connectors **130** at the time T**0**. In this example, WL=4, so that write data DQ is input to the data connectors **120** from a time T**4**.

[0134] Because a flow of the command is similar to that in the read operation shown in FIG. **11**, redundant explanations will be omitted. The write data DQ reaching the data connectors **120** is input to the data register buffer **300**. At this moment, there occurs a time difference (Flight Time) between a timing at which the write command reaches the command/address/control connectors **130** and a timing at which the write command (Direction Control) is input to the data register buffer **300**. In consideration of this point, the memory controller outputs the write data DQ by delaying it by an amount equivalent to the Flight Time.

[0135] The data register buffer **300** loads the received write data DQ in the FIFO (Write) circuit **301** with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer **300** then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit **301** to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS. As described above, the write data is transferred from the data register buffer **300**

to the memory chip **200** using either one of the two data lines L**1** and L**2**. The data line to be used is determined by a designated Rank.

[0136] The memory chip **200** receives the write data DQ that is burst output from the data register buffer **300**, and writes it in the memory cell array. At this time, there occurs a predetermined time difference (Flight Time) between a timing at which the write data DQ and the data strobe signal DQS are output from the data register buffer **300** and a timing at which the write data DQ and the data strobe signal DQS are input to the memory chip **200**. In consideration of this point, the data register buffer **300** outputs the write data DQ earlier by an amount equivalent to the Flight Time. With this configuration, it becomes possible for the memory chip **200** to receive the write data DQ in a correct manner.

[0137] An initializing operation of the memory module **100** according to the present embodiment at the time of activation is explained next.

[0138] FIG. **13** is a flowchart for explaining the initializing operation of the memory module **100** at the time of activation.

[0139] With a power-on of the system (Step S**1**), each of the memory chip **200**, the data register buffer **300**, and the command/address/control register buffer **400** internally activates a reset signal to reset the internal circuit (Step S**2**). By resetting the internal circuit, each of the memory chip **200**, the data register buffer **300**, and the command/address/control register buffer **400** performs the initializing operation. The initializing operation includes a mode register setting operation by which predetermined mode information is set in the mode registers **215**, **321**, and **431** that are included in the memory chip **200**, the data register buffer **300**, and the command/address/control register buffer **400**, respectively (Step S**3**).

[0140] Upon completing the mode register setting operation, a leveling operation between the data register buffer **300** and the memory chip **200** is performed (Step S**4**). The leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a signal. The adjustment of the write timing is performed by a write leveling operation, and the adjustment of the read timing is performed by a read leveling operation.

[0141] When the leveling operation between the data register buffer **300** and the memory chip **200** is completed, a leveling operation between the memory controller and the data register buffer **300** is performed (Step S**5**).

[0142] FIGS. **14**A and **14**B are timing charts for explaining the write leveling operation between the data register buffer **300** and the memory chip **200**, where FIG. **14**A is a timing chart at the time of starting the leveling and FIG. **14**B is a timing chart at the time of ending the leveling. This operation is performed by the write leveling circuit **322** shown in FIG. **5**.

[0143] In the write leveling operation between the data register buffer **300** and the memory chip **200**, as shown in FIG. **14**A, the data register buffer **300** outputs a data strobe signal DQS that is synchronized with the clock signal CK. The clock signal CK is a signal that is supplied from the command/address/control register buffer **400**, which is also supplied to the memory chip **200** as described above. Because it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip **200**, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip **200** side.

[0144] In the example in FIG. **14**A, there is shown a case that a logical level of the clock signal CK at a rising edge of the data strobe signal DQS is "High level". In response to the logical level of the clock signal CK, the memory chip **200** outputs a signal DQ of "High level" from the data input/output terminal **204**. The signal DQ is input to the data register buffer **300**, by which the data register buffer **300** can find a direction of phase shift of the clock signal CK and the data strobe signal DQS.

[0145] The write leveling circuit **322** of the data register buffer **300** changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW based on the direction of the phase shift. In the example shown in FIG. **14**A, because the data strobe signal DQS is retarded as compared to a rising edge of the clock signal CK reaching the memory chip **200**, the data register buffer **300** advances the output timing of the data strobe signal DQS.

[0146] By repeating the above operation, as shown in FIG. **14**B, the logical level of the clock signal CK is changed to "Low level" at the rising edge of the data strobe signal DQS on the memory chip **200** side. This leads to an end of the write leveling operation, and the data register buffer **300** can find a timing to output the data strobe signal DQS based on the input clock signal CK. A result of the write leveling operation is stored in the data register control circuit **320** in the data register buffer **300**. Upon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the memory chip **200** are substantially matched with each other.

[0147] FIG. **15** is a timing chart for explaining the read leveling operation between the data register buffer **300** and the memory chip **200**. This operation is performed by the read leveling circuit **323** shown in FIG. **5**.

[0148] In the read leveling operation between the data register buffer **300** and the memory chip **200**, as shown in FIG. **15**, the command/address/control register buffer **400** outputs the clock signal CK, and at the same time, issues the active command ACT and the read command Read. The clock signal CK is supplied to the memory chip **200** and the data register buffer **300**, and the commands ACT and Read are supplied to the memory chip **200**. The read command Read is also supplied to the data register buffer **300** as a part of the control signal DRC.

[0149] In the example shown in FIG. **15**, the active command ACT is issued at the time T-**5** that is synchronized with the clock signal CK, and the read command Read is issued at the time T**0**. Therefore, a RAS-CAS delay (tRCD) is five clock cycles.

[0150] The memory chip **200** receives the read command Read and performs an actual read operation. In the example shown in FIG. **15**, the CAS latency is set to five clock cycles (CL=5), so that an output of read data DQ begins at the time T**5**. The read data DQ at the time of the read leveling is, for example, a signal in which a High level and a Low level are repeated in an alternate manner.

[0151] The read data DQ output from the memory chip **200** reaches the data register buffer **300**, by which the data register buffer **300** can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips **200**, stored in the data register control circuit **320** in the data register buffer **300**, and used in an adjustment of an activation timing of the input buffer circuit INB and the like. In FIG. **15**, two cases are shown including a first case that the time A from the input of the read command Read until the input of the read data DQ is short

(between the memory chip **200-0** and the data register buffer **300-0**) and a second case that the time A is long (between the memory chip **200-19** and the data register buffer **300-4**).

[0152] FIGS. **16**A and **16**B are timing charts for explaining the write leveling operation between the memory controller **12** and the data register buffer **300**, where FIG. **16**A is a timing chart at the time of starting the leveling and FIG. **16**B is a timing chart at the time of ending the leveling. This operation is performed by a write leveling circuit **12**a shown in FIG. **2**.

[0153] In the write leveling operation between the memory controller **12** and the data register buffer **300**, as shown in FIG. **16**A, the memory controller **12** outputs the clock signal and the data strobe signal DQS. The clock signal CK is supplied to the data register buffer **300** via the command/address/control register buffer **400**, and the data strobe signal DQS is directly supplied to the data register buffer **300**. Therefore, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the data register buffer **300** side.

[0154] In the example shown in FIG. **16**A, on the data register buffer **300**, a case that in which the logical level of the clock signal CK at the rising edge of the data strobe signal DQS is "Low level". In response to the logical level of the clock signal CK, the data register buffer **300** outputs a signal DQ of "Low level" from the input/output terminal **340**. The signal DQ is supplied to the memory controller **12**, by which the memory controller **12** can find a direction of phase shift of the clock signal CK and the data strobe signal DQS.

[0155] The memory controller **12** changes an output timing of the data strobe signal DQS based on the direction of the phase shift. In the example shown in FIG. **16**A, because the data strobe signal DQS reaches the data register buffer **300** earlier than the rising edge of the clock signal CK reaching the data register buffer **300**, the memory controller **12** delays the output timing of the data strobe signal DQS.

[0156] By repeating the above operation, as shown in FIG. **16**B, the logical level of the clock signal CK is changed to "High level" at the rising edge of the data strobe signal DQS on the data register buffer **300** side. This leads to an end of the write leveling operation, and the memory controller **12** can find a timing to output the data strobe signal DQS based on the clock signal CK that is output from the memory controller **12** itself. A result of the write leveling operation is stored in an internal circuit of the memory controller **12**. Upon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the data register buffer **300** are substantially matched with each other.

[0157] FIG. **17** is a timing chart for explaining the read leveling operation between the memory controller **12** and the data register buffer **300**. This operation is performed by a read leveling circuit **12**b shown in FIG. **2**.

[0158] In the read leveling operation between the memory controller **12** and the data register buffer **300**, as shown in FIG. **17**, the memory controller **12** outputs the clock signal CK, and at the same time, issues an active command ACT and a read command Read. The clock signal CK is supplied to the data register buffer **300**, and the commands ACT and Read are supplied to the data register buffer **300** via the command/address/control register buffer **400** as a part of the control signal DRC.

[0159] In the example shown in FIG. **17**, the active command ACT is issued at the time T-**5** that is synchronized with the clock signal CK, and the read command Read is issued at the time T**0**. Therefore, a RAS-CAS delay (tRCD) is five clock cycles.

[0160] The data register buffer **300** receives the read command Read, and after a lapse of a predetermined CAS latency, outputs dummy data DQ. The dummy data DQ is not the read data read out from the memory chip **200** but data that is automatically generated by the data register control circuit **320** in the data register buffer **300**. In the example shown in FIG. **17**, the CAS latency is set to six clock cycles (CL=6), so that an output of the dummy data DQ begins at a time T**6**. The dummy data DQ is, for example, a signal in which a High level and a Low level are repeated in an alternate manner.

[0161] The dummy data DQ output from the data register buffer **300** reaches the memory controller **12**, by which the memory controller **12** can find a time B from an issuance timing of the read command Read until the read data DQ is input. The time is measured for each of the data register buffers **300**, stored in the internal circuit of the memory controller **12**, and used in an adjustment of an activation timing of an input buffer circuit (not shown) and the like. In FIG. **17**, two cases are shown including a first case that the time B from the issuance of the read command Read until the input of the read data DQ is short (between the memory controller **12** and the data register buffer **300-0**) and a second case that the time B is long (between the memory controller **12** and the data register buffer **300-4**).

[0162] The initializing operation of the memory module **100** according to the present embodiment is as described above. A relationship between the DLL circuit and the ODT function of the memory module **100** according to the present invention is explained next.

[0163] As described above, the DLL circuit is a circuit that generates an internal clock signal of which a phase is controlled with respect to an external clock signal, which is used for matching the phases of the read data DQ and the data strobe signal DQS with the phase of the clock signal CK. In a recent high speed memory such as a DDR**3** DRAM, a use of the DLL circuit is substantially essential. If the DLL circuit is not used, it is difficult to perform a data transfer in a proper manner. On the other hand, the DLL circuit has a problem of relatively large power consumption.

[0164] Meanwhile, the ODT function is a function of incorporating a terminating resistor inside a memory chip, which is used for preventing a degradation of signal quality due to a reflection of the signal. In a typical memory module, a large number of memory chips are commonly connected to a single data line. Therefore, in a recent high speed memory, a use of the ODT function is substantially essential. If the ODT function is set to off, a signal waveform is significantly degraded. On the other hand, if the ODT function is set to on, it causes a problem of increasing the power consumption. In addition, because the ODT operation necessitates a synchronization with a data input/output operation, the use of the DLL circuit is basically assumed.

[0165] FIG. **18** is a timing chart for explaining a problem that occurs when performing the ODT operation without using the DLL circuit.

[0166] In the example shown in FIG. **18**, the ODT signal is activated just before the time T**0**. In response to the activation of the ODT signal, the internal circuit of the memory chip **200** turns on the ODT function in synchronization with the clock signal at the time T**0**. However, the ODT impedance (impedances of the data input/output terminal **204** and the data strobe

terminal **205**) does not reach a desired value immediately, and it is not changed from a high impedance state (RTT_OFF) unless tAONDFmin passes. In the present example, the tAONDFmin is about three clock cycles.

[0167] After a lapse of the tAONDFmin, although the ODT impedance becomes no longer the high impedance state according to a condition such as the power supply voltage and the chip temperature, it still does not reach the desired impedance RTT_ON depending on the condition. Under the worst condition, the desired impedance RTT_ON is obtained after tAONDFmax passes from the time T**0**. In the present example, the tAONDFmax is about eight clock cycles.

[0168] Therefore, in a period from a time T**3** at which the ODT impedance becomes an undefined state to a time T**9** that is next to a cycle at which the ODT impedance becomes the desired value RTT, the impedance becomes undefined. Accordingly, this period becomes a loss cycle in which an access to another memory chip is not allowed. In this manner, when the ODT operation is performed without using the DLL circuit, a switching between on and off controls of the ODT function is not synchronized, resulting in an increase of the period in which the impedance is undefined during which the read/write operation is inhibited.

[0169] In consideration of the loss cycle problem described above, it is desirable not to use the ODT function when the DLL circuit is not used. However, the ODT function is substantially essential in the typical memory module, so that it is difficult to turn the function off.

[0170] However, in the memory module **100** according to the present embodiment, because the load capacities of the data lines L**1** and L**2** connected to the memory chip **200** are considerably small, even when a high speed memory such as a DDR**3** DRAM is used, the ODT operation can be set off in an actual operation. Besides, because a distance between the memory chip **200** and the data register buffer **300** is considerably short, even if a synchronization control is not performed using a DLL circuit, it is possible to perform a data transfer in a correct manner. That is, because both the ODT function and the DLL circuit can be set to off, it is possible to reduce the power consumption by a considerable amount. In addition, because the ODT function and the DLL circuit can be eliminated from the memory chip **200**, it is also possible to reduce the chip dimension.

[0171] A difference in operation timings depending on the use of the ODT function and the DLL circuit is explained next.

[0172] FIG. **19** is a timing chart for explaining a read-to-read operation when both the ODT function and the DLL circuit are in an ON state.

[0173] As shown in FIG. **19**, a read operation timing in a state where both the ODT function and the DLL circuit are set to on is basically the same as the operation timing shown in FIG. **11**. In the example shown in FIG. **19**, a read command Read is issued for the Rank**0** at the time T**0**, and another read command Read is issued for the Rank**1** at the time T**6**. Because the memory chip **200** of the Rank**0** and the memory chip **200** of the Rank**1** are commonly connected to the data line L**1**, they cause an influence on each other.

[0174] Accordingly, in a period from the time T**5** to the time T**9** during which read data DQ is burst output from the memory chip **200** of the Rank**0**, an impedance of the data input/output terminal **204** of the memory chip **200** of the Rank**1** is set to Rtt_Nom by the ODT function. Similarly, in a period from a time T**11** to a time T**15** during which read data DQ is burst output from the memory chip **200** of the Rank**1**, an impedance of the data input/output terminal **204** of the memory chip **200** of the Rank**0** is set to Rtt_Nom by the ODT function.

[0175] In this manner, during the read data DQ is output from the memory chip **200** on one side, the memory chip **200** on the other side performs the ODT operation, which prevents a reflection of a signal. However, as described above, current consumption is generated due to the usage of the ODT function and the DLL circuit.

[0176] FIG. **20** is a timing chart for explaining the read-to-read operation when both the ODT function and the DLL circuit are in an OFF state.

[0177] As shown in FIG. **20**, when the DLL circuit is set to off, an output timing of the read data DQ is asynchronous with the clock signal CK. However, in the present embodiment, because the distance between the memory chip **200** and the data register buffer **300** is considerably short, the data register buffer **300** can correctly receive the read data DQ that is output in an asynchronous manner. In addition, because the memory chip of the Rank**0** and the memory chip of the Rank**1** are arranged at substantially the end of the data line L**1**, an influence of a reflection of a signal from the memory chip **200** on the non-operating side is considerably small. The read data DQ output in an asynchronous manner is subjected to a re-timing by the data register buffer **300**, and then output to the memory controller **12**.

[0178] In this manner, in the present embodiment, even when both the ODT function and the DLL circuit of the memory chip **200** are set to off, it is possible to perform the same read operation as in a case that the ODT function and the DLL circuit are set to on. Rather, the output timing of the read data DQ is made earlier because the timing adjustment by the DLL circuit is not performed, which makes it possible to realize an even higher speed access.

[0179] FIG. **21** is a timing chart for explaining a write-to-write operation when both the ODT function and the DLL circuit are in an ON state.

[0180] As shown in FIG. **21**, a write operation timing in a state where both the ODT function and the DLL circuit are set to on is basically the same as the operation timing shown in FIG. **12**. In the example shown in FIG. **21**, a write command Write is issued for the Rank**0** at the time T**0**, and another write command Write is issued for the Rank**1** at the time T**6**. As described above, because the memory chip **200** of the Rank**0** and the memory chip **200** of the Rank**1** are commonly connected to the data line L**1**, they cause an influence on each other.

[0181] Accordingly, in a period from the time T**5** to the time T**9** during which write data DQ is burst input to the memory chip **200** of the Rank**0**, an impedance of the data input/output terminal **204** of the memory chip **200** of the Rank**1** is set to Rtt_Nom by the ODT function. Similarly, in a period from the time T**11** to the time T**15** during which write data DQ is burst input to the memory chip **200** of the Rank**1**, an impedance of the data input/output terminal **204** of the memory chip **200** of the Rank**0** is set to Rtt_Nom by the ODT function.

[0182] In this manner, during the memory chip **200** on one side receives the write data DQ, the memory chip **200** on the other side performs the ODT operation, which prevents a reflection of a signal. However, as described above, current consumption is generated due to the usage of the ODT function and the DLL circuit.

[0183] FIG. **22** is a timing chart for explaining the write-to-write operation when both the ODT function and the DLL circuit are in an OFF state.

[0184] As shown in FIG. **22**, when the ODT function is set to off, the data input/output terminal **204** of the memory chip **200** on the non-operating side becomes in a high impedance state, from which a reflection of a signal occurs. However, in the present embodiment, because the distance between the memory chip **200** and the data register buffer **300** is considerably short and the memory chip of the Rank**0** and the memory chip of the Rank**1** are arranged at substantially the end of the data line L**1**, the influence of the reflection of the signal from the memory chip **200** on the non-operating side is considerably small. Therefore, it is possible for each of the memory chips **200** to receive the write data DQ in a correct manner.

[0185] In this manner, in the present embodiment, even when both the ODT function and the DLL circuit of the memory chip **200** are set to off, that is, the current consumption due to the ODT function and the DLL circuit is made zero, it is possible to perform the same write operation as in a case that the ODT function and the DLL circuit are set to on. Rather, because an operation for switching the ODT impedance is not necessary, it is also possible to make an input timing of the write data DQ earlier. Actually, the speed of the write-to-write operation is increased by one clock cycle in the operation timing shown in FIG. **22** than in the operation timing shown in FIG. **21**.

[0186] Some modifications of the present invention are explained nest.

[0187] FIGS. **23**A and **23**B are schematic diagrams for explaining, a data transfer path for transferring 1-bit data in a memory module according to a modification of the present embodiment, where FIG. **23**A is a layout diagram and FIG. **23**B is a connection diagram.

[0188] In the example shown in FIGS. **23**A and **23**B, unlike the embodiment described above, only a single memory chip **200** is connected to each of the data lines L**1** and L**2**. Specifically, only the memory chip **200-0** is connected to the data line L**1**, and only the memory chip **200-1** is connected to the data line L**2**. The present invention also includes this type of mode. That is, the number of memory chips **200** allocated to a single data line (L**1** or L**2**) that connects the memory chip **200** and the data register buffer **300** is not limited to a particular number. However, in order to reduce the load capacities of the data lines L**1** and L**2**, the branch points, and the line lengths, it is preferable that the number of the memory chips **200** connected to a single data line should be equal to or less smaller than two.

[0189] FIGS. **24**A and **24**B are schematic diagrams for explaining a data transfer path for transferring 1-bit data in a memory module according to another modification of the present embodiment, where FIG. **24**A is a layout diagram and FIG. **24**B is a connection diagram.

[0190] In the example shown in FIGS. **24**A and **24**B, unlike the embodiment described above, four data lines L**1***a*, L**1***b*, L**2***a*, and L**2***b* are allocated to a single data line L**0**. Specifically, only the memory chip **200-0** is connected to the data line L**1***a*, only the memory chip **200-1** is connected to the data line L**1***b*, only the memory chip **200-2** is connected to the data line L**2***a*, and only the memory chip **200-3** is connected to the data line L**2***b*. The present invention also includes this type of mode. That is, the number of the memory chips **200** allocated to a single data register buffer **300** is not limited to a particular number as long as it is equal to or larger than two.

[0191] FIG. **25** is a schematic diagram of a configuration of a memory module according to still another modification of the present embodiment.

[0192] The memory module shown in FIG. **25** has such a configuration that a plurality of memory chips **200** forming the same group and a single data register buffer **300** are integrated in a sub-module **500**. By using the sub-module **500**, the data lines L**1** and L**2** can be formed on a substrate of the sub-module, so that a line density of the module substrate **110** can be relieved. In addition, because the number of parts to be mounted on the module substrate **110** is reduced by a considerable amount, the mounting process on the module substrate **110** can be simplified.

[0193] FIG. **26** is a plan view showing a configuration of the sub-module **500**; and FIG. **27** is a cross section of the sub-module **500** cut along a line Y**1**-Y**1'** shown in FIG. **26**. In FIG. **26**, external terminals formed on the other side are shown transparently.

[0194] The sub-module **500** shown in FIGS. **26** and **27** is configured with a sub-module substrate **510**, two memory chips **200** and a data register buffer **300** mounted on the sub-module substrate **510**, and external terminals (solder balls) **520** formed on the other side of the sub-module substrate **510**. The memory chips **200** and the data register buffer **300** are sealed with a sealant **530**.

[0195] The external terminals **520** include DQ balls **521** for performing an exchange of data, Control balls **522** for performing a reception of a control signal to be supplied to the data register buffer **300**, and CA balls **523** for performing a reception of a command/address/control signal. The DQ balls **521** and the Control balls **522** are arranged on the other side of the sub-module substrate **510** near an area in which the data register buffer **300** is mounted. On the other hand, the CA balls **523** are arranged on the other side of the sub-module substrate **510** near an area in which the memory chips **200** are mounted.

[0196] The DQ balls **521** and the Control balls **522** are connected to the data register buffer **300** via internal lines **511** and **514** that are formed on the sub-module substrate **510**. The CA balls **523** are connected to the memory chips **200** via internal lines **513** that are formed on the sub-module substrate **510**.

[0197] Using the sub-module **500** configured in the above manner eliminates a necessity of forming the data lines L**1** and L**2** for connecting the memory chips **200** and the data register buffer **300** on the module substrate **110**. As a result, a freedom in the layout of the module substrate **110** is enhanced.

[0198] FIG. **28** is a plan view showing another configuration of the sub-module **500**; and FIG. **29** is a cross section of the sub-module **500** cut along a line Y**2**-Y**2'** shown in FIG. **28**. In FIG. **28**, external terminals formed on the other side are shown transparently.

[0199] The sub-module **500** shown in FIGS. **28** and **29** has basically the same configuration as that of the sub-module **500** shown in FIGS. **26** and **27**, with a difference in that eight memory chips **200** are mounted on the sub-module substrate **510**. The eight memory chips **200** are formed with four layered bodies in each of which two memory chips **200** are layered. The four layered bodies are two-dimensionally mounted on the sub-module substrate **510**. Using the sub-

module **500** configured in the above manner makes it possible to increase a memory capacity of the memory module.

[0200] It is apparent that the present invention is not limited to the above embodiments, but may be modified and changed without departing from the scope and spirit of the invention. For example, while the above embodiment has described a memory chip that includes a DLL circuit therein as the memory chip **200**, a memory chip that does not include a DLL circuit therein can be alternatively used. In this case, the DLL circuit included in the data register buffer **300** is used to adjust the input/output timing.

What is claimed is:

1. A memory module comprising:

a module substrate including a plurality of data connectors;

a plurality of memory chips mounted on the module substrate, each of the memory chips including at least one data terminal; and

a plurality of data register buffers mounted on the module substrate, each of the data register buffers being assigned to at least two memory chips, wherein

each of the data register buffers includes M first input/output terminals each being connected to an associated one of the data connectors via a first data line formed on the module substrate, where M is a positive integer equal to or larger than 1, and N second input/output terminals each being connected to the data terminal of corresponding memory chips via a second data line formed on the module substrate, where N is a positive integer equal to or larger than 2M, so that number of the second data lines is N/M times number of the first data lines.

2. The memory module as claimed in claim **1**, wherein each of the data register buffers receives write data transferred via a corresponding first data line, outputs received write data to any one of the second data lines, receives read data transferred via any one of the second data lines, and outputs received read data to the corresponding first data line.

3. The memory module as claimed in claim **2**, wherein a transfer rate of the write data and the read data transferred via the first data lines and a transfer rate of the write data and the read data transferred via the second data lines are substantially equal to each other.

4. The memory module as claimed in claim **1**, wherein each of the second data lines is connected to at least two of the corresponding memory chips in common.

5. The memory module as claimed in claim **4**, wherein at least two of the memory chips connected to same one of the second data lines are arranged close to each other.

6. The memory module as claimed in claim **5**, wherein two of the memory chips connected to the same second data line are mounted at positions facing each other across the module substrate, respectively.

7. The memory module as claimed in claim **1**, wherein at least two of the memory chips connected to different one of the second data lines connected to same one of the data register buffers are arranged close to each other.

8. The memory module as claimed in claim **1**, wherein

the module substrate has a long side and a short side,

the data connectors are arranged along the long side, and

each of the data register buffers, the data connectors corresponding to the data register buffer, and the memory chips corresponding to the data register buffer are arranged in a direction of the short side.

9. The memory module as claimed in claim **1**, further comprising a command/address/control register buffer that is mounted on the module substrate and includes input terminals, a first output terminal, and a second output terminal, wherein

the module substrate further includes a plurality of command/address/control connectors, each of the input terminals is connected to an associated one of the command/address/control connectors, the first output terminal is connected to the memory chips, and the second output terminal is connected to the data register buffers.

10. The memory module as claimed in claim **9**, wherein

the command/address/control register buffer includes a register circuit that receives and holds a command/address/control signal supplied via the input terminals, and a control signal generating circuit that generates a control signal based on the command/address/control signal supplied via the input terminals, the command/address/control signal held in the register circuit is supplied to the first output terminal, and

the control signal generated by the control signal generating circuit is supplied to the second output terminal.

11. The memory module as claimed in claim **10**, wherein

the first output terminal of the command/address/control register buffer is commonly connected to the memory chips, and

the second output terminal of the command/address/control register buffer is commonly connected to the data register buffers.

* * * * *