Paper No. 1

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY SOLUTIONS INC.,

Petitioners,

v.

NETLIST, INC.

Patent Owner.

Patent No. 9,128,632

Issued: September 8, 2015

Filed: July 27, 2013

Inventors: Hyun Lee and Jayesh R. Bhakta

Title: Memory Module with Distributed Data Buffers and Method of Operation

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*Inter Partes* Review No. IPR2017-00730

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**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,128,632 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1-.80 & 42.100-.123**

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## TABLE OF CONTENTS

**I. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW ..... 1**

A. Certification the 632 Patent May Be Contested by Petitioners ..... 1

B. Fee for Inter Partes Review (§ 42.15(a)) ..... 1

C. Mandatory Notices (37 CFR § 42.8(b)) ..... 1

D. Proof of Service (§§ 42.6(e) and 42.105(a)) ..... 2

**II. Identification of Claims Being Challenged (§ 42.104(b)) ..... 2**

**III. Relevant Information Concerning the Contested Patent ..... 3**

A. Effective Filing Date of the 632 Patent ..... 3

B. Person of Ordinary Skill in the Art ..... 3

C. The 632 Patent ..... 4

1. Technical Overview of the 632 Patent ..... 4

2. The Prosecution History of The 632 Patent ..... 5

D. Construction of Terms Used in the 632 Patent Claims ..... 6

1. "*memory module*" ..... 6

2. "*memory system*" ..... 7

3. "*memory controller*" ..... 7

4. "*memory bus*" ..... 7

5. "*memory command signals*" ..... 8

6. "*module command signals*" ..... 9

7. "*module control signals*" ..... 9

8. "*metastability*" ..... 9

**IV. Overview Of The Prior Art ..... 10**

A. USPPA 2010/0309706 to Saito (Ex. 1005) ..... 10

B. USP 7,808,849 to Swain (Ex. 1006) ..... 13

C. USP 6,184,701 to Kim (Ex. 1007) ..... 14

**V. Precise Reasons for Relief Requested ..... 15**

A. Claims 1-5, 12-14, and 19-20 are Obvious Over Saito in view of Swain ..... 15

1. Claim 1 is Obvious ..... 15
2. Claim 2 is Obvious ..... 33
3. Claim 3 is Obvious ..... 35
4. Claim 4 is Obvious ..... 39
5. Claim 5 is Obvious ..... 42
6. Claim 12 is Unpatentable ..... 42
7. Claim 13 is Obvious ..... 45
8. Claim 14 is Obvious ..... 46
9. Claim 19 is Obvious ..... 46
10. Claim 20 is Obvious ..... 49

B. Claims 3 and 13-14 are Obvious Over Saito in view of Swain in further view of Kim ..... 49

1. Claim 3 is Obvious ..... 49

**VI. CONCLUSION ..... 53**

**Attachment A. Proof of Service of the Petition**

**Attachment B. List of Evidence and Exhibits Relied Upon in Petition**

# I. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

## A. Certification the 632 Patent May Be Contested by Petitioners

Petitioners certify they are not barred or estopped from requesting *inter partes* review of U.S. Patent No. 9,128,632 ("the 632 Patent") (Ex. 1001). No Petitioner, nor any party in privity with a Petitioner, has filed a civil action challenging the validity of any claim of the 632 Patent. The 632 Patent has not been the subject of a prior *inter partes* review by any Petitioner or a privy of a Petitioner. Petitioners also certify this petition for *inter partes* review is filed within one year of the date of service of a complaint alleging infringement of a patent – no complaint alleging infringement of the 632 Patent has been served on any Petitioner. Petitioners therefore certify this patent is available for *inter partes* review.

## B. Fee for Inter Partes Review (§ 42.15(a))

The Director is authorized to charge the fee specified by 37 CFR § 42.15(a) to Deposit Account No. 50-1597.

## C. Mandatory Notices (37 CFR § 42.8(b))

The real parties of interest of this petition are the Petitioners.

The 632 Patent is not involved in any other legal proceedings, to Petitioners' knowledge.

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Service on Petitioner may be made by mail or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

### D. Proof of Service (§§ 42.6(e) and 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

## II. Identification of Claims Being Challenged (§ 42.104(b))

Claims 1-5, 12-14 and 19-20 of the 632 Patent are unpatentable as follows:

(i) Claims 1-5, 12-14 and 19-20 of the 632 Patent are unpatentable as obvious under 35 U.S.C. § 103 over United States Published Patent Application No. 2010/0309706 to Saito ("Saito"), attached hereto as Ex. 1005, in view of United States Patent No. 7,808,849 to Swain ("Swain"), attached hereto as Ex. 1006; and

(ii) Claims 3 and 13-14 of the 632 Patent are unpatentable as obvious under 35 U.S.C. § 103 Saito in view of Swain in further view of United States Patent No. 6,184,701 to Kim ("Kim"), attached hereto as Ex. 1007.

Petitioner's proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided in §§ **III-V**, below. The evidence relied upon in this petition is listed in **Attachment B**.

## III. Relevant Information Concerning the Contested Patent

### A. Effective Filing Date of the 632 Patent

The application that resulted in the 632 Patent is U.S. Patent Application Serial No. 13/952,599, filed Jul. 27, 2013. Ex. 1001 at Face. The 632 Patent claims priority to U.S. Provisional Application No. 61/676,883, filed Jul. 27, 2012. Petitioner therefore assumes that the claims of the 632 Patent have an effective filing date of **July 27, 2012**.

### B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the 632 Patent would have been someone with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working the field. Such a person would have been knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs and less sophisticated circuits such as data buffers, flip flops and registers. Ex. 1003 at ¶39.

## C. The 632 Patent

### 1. Technical Overview of the 632 Patent

The 632 Patent discloses memory modules with multiple memory devices, data buffers and circuitry for controlling write and read operations between the memory module and a memory controller. Ex. 1001 at Abstract. In one exemplary embodiment, the memory module includes memory devices organized in groups, each group with an associated data buffer and one module control device for the entire module, *id.* at 3:8-10, wherein the memory devices and data buffers are distributed length-wise across the memory module and the module control device is centrally located, *id.* at 3:12-36, Fig. 2C. Ex. 1003 at ¶40.

A memory bus includes control/address (C/A) signal lines between the memory controller and the module control device and data/strobe signal lines between the memory controller and each memory device via each data buffer. Ex. 1001 at 4:1-13. The memory controller issues C/A signals to the memory module via the module control device, and sends and receives data/strobe signals to/from the memory devices via the data buffers. *Id.; see also id.* at 4:45-52, 5:34-6-3; Ex. 1003 at ¶¶41-43.

Because the data buffers and their associated memory devices are distributed across the memory module varying distances from the module control device, they receive module control signals at different times. Ex. 1001 at 9:23-42. Each data

buffer thus includes signal alignment circuits that determine appropriate time intervals to use to adjust for the signals arriving at different times. *Id.* at 9:43-56; *see also* Ex. 1003 at ¶44. The 632 patent discloses that a time interval can be determined by the data buffer based on the timing of a write operation and that such time interval can be used to adjust timing during a read operations. Ex. 1001 at 15:1-54; *see also* Ex. 1003 at ¶45.

### 2. The Prosecution History of The 632 Patent

The Examiner rejected the original claims of the application underlying the 632 Patent as anticipated by Manohararajah. Ex. 1002 at 100-108. In response, the applicant amended the claims, *inter alia*, by adding language requiring each data buffer to be configured to "determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation" and to "time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter . . . ." Ex. 1002 at 134-135. Among other things, the applicant argued that "[n]owhere in Manohararajah it is [sic] described the transmission of read data signal from each respective buffer is timed in accordance with a time interval determined based signals [sic] received by the each respective buffer. Thus, Manohararajah does not anticipate claim 1 as amended."

*Id.* at 8-9; *See also* Ex. 1003 at ¶47. In response, the Examiner issued a notice of allowance. Ex. 1002 at 1078.

### D. Construction of Terms Used in the 632 Patent Claims

In this proceeding, claims must be given their broadest reasonable construction in light of the specification. 37 CFR § 42.100(b). If Patent Owner contends terms in the claims should be read to have a special meaning, those contentions should be disregarded unless Patent Owner also amends the claims compliant with 35 U.S.C. § 112 to make them expressly correspond to those contentions. *See* 77 Fed. Reg. 48764 at II.B.6 (Aug. 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed. Cir. 2012).

#### 1. *"memory module"*

The broadest reasonable interpretation of "memory module" is "a removable circuit board, cartridge, or other carrier that contains one or more RAM memory chips." For instance, the Microsoft Computer Dictionary defines a "memory module" as "[a] removable circuit board, cartridge, or other carrier that contains one or more RAM memory chips." Microsoft Computer Dictionary 334 (5th ed. 2002) (attached as Ex. 1009). This is consistent with the 632 Patent: "A memory module usually includes multiple memory devices, such as dynamic random access memory devices (DRAM) or synchronous dynamic random access memory

devices (SDRAM), packaged individually or in groups, and/or mounted on a printed circuit board (PCB)." Ex. 1001 at 1:39-44; *see also* Ex. 1003 at ¶¶53-55.

**2. *"memory system"***

The broadest reasonable interpretation of "memory system" is "a collection of component elements that work together to perform a memory task, including a memory module and memory controller." For instance, the Microsoft Computer Dictionary defines a "system" as "[a] collection of component elements that work together to perform a task." Ex. 1009 at 508. And the 632 patent states that its memory system includes a memory module and a memory controller. Ex. 1001 at Abstract ("A memory module is operable in a memory system with a memory controller."); *see also id.* at Fig. 1. *See also* Ex. 1003 at ¶¶56-58.

**3. *"memory controller"***

The broadest reasonable interpretation of "memory controller" is "a device capable of sending instructions or commands or otherwise controlling memory devices." The 632 Patent explicitly states that, "[i]n the context of the present description, a memory controller refers to any device capable of sending instructions or commands, or otherwise controlling the memory devices 112." Ex. 1001 at 4:27-30. This is consistent with the understanding in the field. *See* Ex. 1003 at ¶¶59-61.

**4. *"memory bus"***

The broadest reasonable interpretation of "memory bus" is "any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller." The 632 Patent explicitly states that: "a memory bus refers to any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller." Ex. 1001 at 4:30-38. This is consistent with the understanding in the field. *See* Ex. 1003 at ¶¶62-64.

### 5. *"memory command signals"*

The broadest reasonable interpretation of "memory command signals" is "signals from the memory controller, including control and address signals, that direct memory operations." The 632 Patent states that "[t]he memory module is operable to perform memory operations in response to <u>memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module</u>. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals." Ex. 1001 at 3:12-21 (emphasis added); *see also* Ex. 1003 at ¶¶65-67.

### 6. *"module command signals"*

The broadest reasonable interpretation of "module command signals" is "signals derived from the memory command signals that are provided to memory devices to control operation of the memory devices." The 632 Patent states that "the module control device … generates a set of module command signals … in response to each memory command from the memory controller", Ex. 1001 at 3:24-27, and that the "module command signals are provided to memory devices . . . ." *Id.* at Abstract; *see also* Ex. 1003 at ¶¶68-70.

### 7. *"module control signals"*

The broadest reasonable interpretation of "module control signals" is "signals derived from the memory command signals that are provided to buffer circuits to control operations of the buffer circuits." The 632 Patent states that "the module control device … generates … a set of module control signals in response to each memory command from the memory controller," Ex. 1001 at 3:24-27, and that the "module control signals are provided to a plurality of buffer circuits to control data paths in the buffer circuits." *Id.* at Abstract; *see also* Ex. 1003 at ¶¶71-73.

### 8. *"metastability"*

The broadest reasonable interpretation of "metastability" is "misalignment of a signal from the relevant clock signal." The 632 Patent states that, "[a]s the module control signals travel over such a distance, they can <u>become misaligned</u>

with the module clock signal, resulting in metastability in the received module control signals." Ex. 1001 at 9:15-20 (emphasis added); *see also* Ex. 1003 at ¶¶74-76.

## IV. Overview Of The Prior Art

### A. USPPA 2010/0309706 to Saito (Ex. 1005)

United States Published Patent Application No. 2010/0309706 to Saito ("Saito") was filed on June 3, 2010 and published on December 9, 2010. Saito is thus prior art to the 632 Patent under 35 U.S.C. §§ 102(a), (b) & (e).

Saito discloses a memory module including "thirty-six memory chips." Ex. 1005 at [0044]. The memory chips and other components are mounted on "a printed circuit board that includes a multilayer wiring. The planar shape of the module PCB 110 is substantially rectangle." *Id.* at [0045]. Along one of the long sides, "a plurality of data connectors 120 and a plurality of command/address/control connectors 130 are provided … for making an electrical connection with a memory controller via a memory slot . . . ." *Id.*; Ex. 1003 at ¶78.

The 36 memory chips are in a "4-rank configuration." Ex. 1005 at [0049]. "[F]our memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other." *Id.* at [0050]. "[T]he memory module 100 includes nine data register buffers 300," one for each of the nine groups of four memory chips. *Id.* at [0044],

[0053]. "The data connectors 120 are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and the memory controller." *Id.* at [0046]. The data connectors are "substantially right below the memory chips," with the corresponding data register buffers in between the memory chips and the connectors. *Id.;* Ex. 1003 at ¶79.

The memory module also includes one centrally located "command/address/control register buffer 400." Ex. 1005 at [0057]. "The command/address/control connectors 130 are connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer 400." *Id.* at [0047]. They are also centrally located, below the "command/address/control register buffer." *Id.;* Ex. 1003 at ¶80.

"The command/address/control register buffer 400 receives the command signal, the address signal, the control signal, and the clock signal" from the memory controller, "buffers the signals, and supplies the signals to the memory chips 200." Ex. 1005 at [0058]. "At the same time, the command/address/control register buffer 400 generates a control signal" and supplies it "to the data register buffers . . . ." *Id.* at [0059]; Ex. 1003 at ¶81.

Figure 1 of Saito illustrates its memory module, reproduced below with the "command/address/control register buffer" colored red, the "memory chips" colored green, the "data register buffers" colored blue, the "data connectors" (data buses) colored yellow, the "command/address/control connectors" (command/address/control bus) colored purple, and the command and control signal buses on the module between the "command/address/control register buffer" and the "memory chips" and "data register buffers" colored orange:

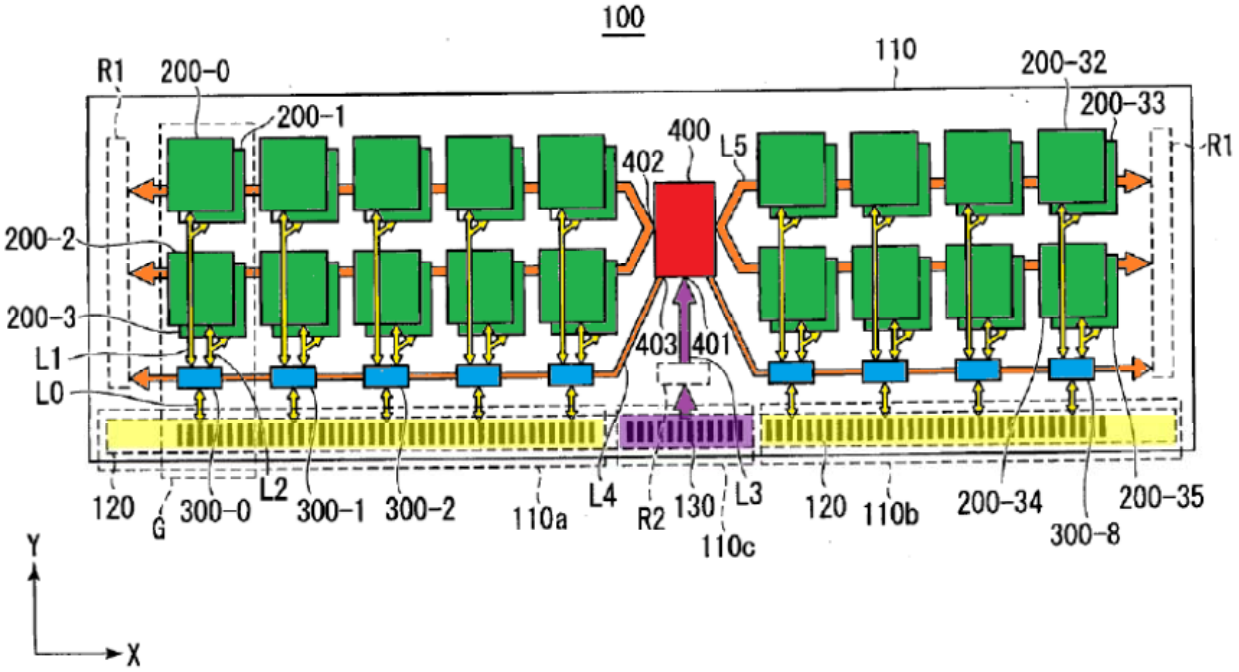


FIG.1

Saito recognizes that, with high speed operation and "memory chips" and "data register buffers" distributed different distances from the "command/address/control register buffer," there will be timing issues with the signals arriving at the respective chips and buffers requiring "timing adjustments."

Ex. 1005 at [0087], [0101]. The memory module sets these "timing adjustments" during initialization by performing write leveling and read leveling operations. Each group of memory chips/data register buffer performs two sets of write and read leveling operations, one "between the data register buffer 300 and the memory chip 200," *id.* at [0138], and one "between the memory controller and the data register buffer 300 . . . ." *Id.* at [0139]; Ex. 1003 at ¶83.

Saito's "data register buffers" also include "DLL circuits" that operate during normal operation as opposed to initialization. Ex. 1005 at [0082]. "The DLL circuit 310 is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400 . . . ." *Id.* at [0084]. It "generates an internal clock signal of which a phase is controlled with respect to an external clock signal, which is used for matching the phases of the read data DQ and the data strobe signal DQS with the phase of the clock signal CK." *Id.* at [0161]; Ex. 1003 at ¶84.

**B. USP 7,808,849 to Swain (Ex. 1006)**

United States Patent No. 7,808,849 to Swain ("Swain") was filed on July 8, 2008 and issued on October 5, 2010. Swain is thus prior art to the 632 Patent under 35 U.S.C. §§ 102(a), (b) & (e).

Swain is focused on systems and methods for performing read leveling in memory modules with memory devices spread across a PCB, what Swain refers to

as "a sequential chained topology." Ex. 1006 at Abstract. "Read leveling needs to be performed for each of the memory units since the accurate values for corresponding compensation delay are different for different memory units [based on different propagation delays.]" *Id.* at 1:39-50; *see also* Ex. 1003 at ¶86.

Swain teaches that its system first performs write leveling during initialization and that, during the read leveling operation during initialization, one option for setting the timing adjustment or delay for read operations is to use the "parameters determined while write leveling." Ex. 1006 at 5:59-64. Swain's exemplary memory module is one without data register buffers between the memory chips and the memory controller, consequently, Swain has only a single set of write and read leveling operations, between the memory controller and the memory chips. "However," as Swain explains, "various features can be implemented in other environments … without departing from the scope and spirit of various aspects of the present invention, as will be apparent to one skilled in the relevant arts by reading the disclosure provided herein." *Id.* at 5:31-36; *see also* Ex. 1003 at ¶87.

### C. USP 6,184,701 to Kim (Ex. 1007)

United States Patent No. 6,184,701 to Kim ("Kim") was filed on May 27, 1999 and issued on February 6, 2001. Kim is thus prior art to the 632 Patent under 35 U.S.C. §§ 102(a), (b) & (e).

Kim discloses "a metastability detection/prevention circuit 20" to be incorporated with any "main active circuit 10" in need thereof. Ex. 1007 at 2:21-22. Kim teaches that "the circuit 10 may comprise a data input buffer . . . ." *Id.* at 2:30-31. "[T]he metastability detection/prevention circuit 20 preferably performs the function of detecting whether the output POUT of the main active circuit 10 has been disposed in a metastable state for a duration in excess of a transition duration." *Id.* at 2:33-37; Ex. 1003 at ¶89.

## V. Precise Reasons for Relief Requested

### A. Claims 1-5, 12-14, and 19-20 are Obvious Over Saito in view of Swain

#### 1. Claim 1 is Obvious

##### *a)* *Preamble part 1*

The first part of the preamble of claim 1 requires "*[a] memory module to operate in a memory system with a memory controller*."

Saito discloses a memory module 100 that operates in a memory system 20 with a memory controller (or MCH) 12. Ex. 1005 at [0062-64], Fig 2. Saito thus discloses this claim element. Ex. 1003 at ¶¶90-92.

##### *b)* *Preamble part 2*

The second part of the preamble of claim 1 requires "*the memory system operating according to a system clock*."

Saito discloses that his "*memory system*" operates according to a "*system clock*" **CK**, provided by the memory controller. Ex. 1005 at [0045]. Saito thus discloses this claim element. Ex. 1003 at ¶¶93-95.

***c)*** *Preamble Part 3*

The third part of the preamble of claim 1 requires "*the memory system including a memory bus coupling the memory module to the memory controller, the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising*."

Saito discloses a group of components and connections that provide electrical communication between the memory module and the memory controller, *i.e.*, a "*memory bus*," including data signal lines and control/address signal lines. Specifically, Saito discloses data connectors 120 and command/address/control connectors 130 that connect the signal line 23 on the motherboard to data and control signal lines on the memory module. These data and control signal lines connect to the components of the memory module and the memory controller, respectively. Ex. 1005 at [0045]; [0046]; [0068]; Figs. 1 and 3 (annotated below).

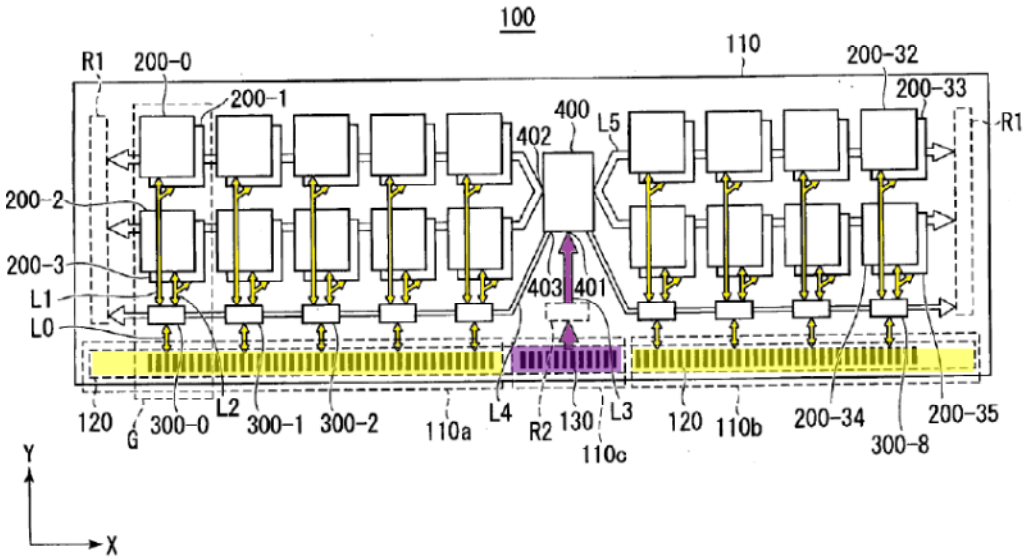


FIG.1

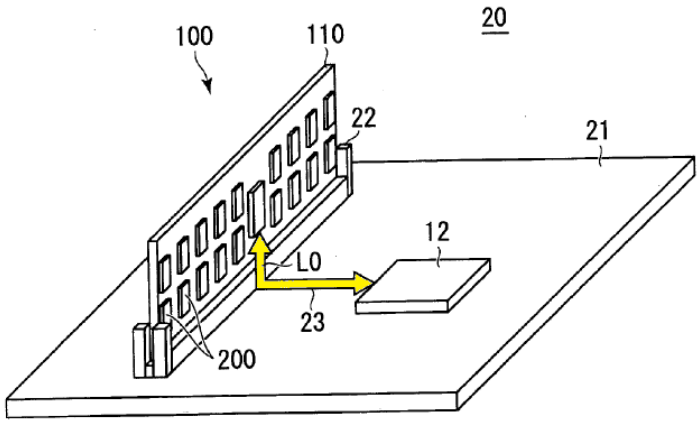


FIG.3

Saito discloses that the **L0, L1 and L2 signal lines** above in Figure 1, "*the plurality of data signal lines*," each provide **data signal lines DQ and data strobe signal lines DQS** to the plurality of memory chips 200 and data register buffers 300. Ex. 1005 at [0100].

Saito further discloses that the command/address/control register buffer 400 (*i.e., "module control device"*) "receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a **command/address/control signal** and the like) that are supplied from the **command/address/control connectors 130** through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200." *Id.* at [0058] (emphasis added). Figure 1, annotated above, illustrates that the command/address/control register buffer 400 receives this set of "*control/address signal lines"* via command/address/control connectors 130 and command/address/ control line L3.

Data connectors 120, command/address/control line connectors 130, data lines L0, L1 and L2 and command/address/control line L3 are all part of the memory bus, as they are used to provide electrical communication between a memory module and a memory controller. Ex. 1003 at ¶100.

Saito thus discloses this claim element. *Id.* at ¶¶96-101.

***d)*** *module control device*

Claim 1 requires "*a module control device to receive memory command signals from the memory controller and to output module command signals and module control signals in response to the memory command signals*."

Saito discloses a command/address/control register buffer 400 ("*module control device*") that receives memory command signals from the memory controller. Specifically, Saito discloses that "[t]he **command/address/control register buffer 400** receives the **command signal**, **the address signal, the control signal, and the clock signal** ["*memory command signals*"] . . . that are supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200." Ex. 1005 at [0058] (emphasis added); *see also id.* at [0052]. As explained above, command/address/control connectors 130 connect the command/address/control register buffer 400 to **the memory controller**. *Id.* at [0045], [0093].

The command/address/control register buffer 400 ("*module control device*") outputs module command signals in response to the memory command signals. For example, Saito discloses that "[t]he **command/address/control signal** ["*memory command signal*"] that is supplied from the memory controller 12 is input from the input terminal 401. Among input command/address/control signals, the command signal CMD, the address signal ADD, and the control signal CTRL are supplied to a register circuit 410, and the clock signal CK is supplied to a PLL circuit 420. The register circuit 410 is a circuit that buffers the command signal CMD, the address signal ADD, and the control signal CTRL, and **the buffered command signal CMD, address signal ADD, and control signal CTRL**

["*module command signals*"] are supplied to the memory chip 200 via the output terminal 402." Ex. 1005 at [0094] (emphasis added); *see also id*. at [0072-0077], Figs. 4 and 6.

The command/address/control register buffer 400 ("*module control device*") likewise outputs module control signals in response to the memory command signals, including the DRC signals and the CK signal. Ex. 1005 at [0096], [0059], Fig. 6. The **DRC signals** and **CK signal** are therefore "*module control signals*" because they are derived from the memory command signals and provided to the buffer circuits to control operations of the buffer circuits. *See also, id.* at [0084], [0097], Fig. 5; Ex. 1003 at ¶105.

Saito thus discloses this claim element. Ex. 1003 at ¶¶102-106.

***e)*** *memory devices organized in groups*

Claim 1 further requires "*memory devices organized in groups, each group including at least one memory device, the memory devices receiving the module command signals from the module control device and performing one or more memory operations in accordance with the module command signals*."

Saito discloses memory devices organized in groups with each group including at least one memory device. Ex. 1005 at [0051]; *see also id.* at [0054]. One group is included in the red box in annotated Figure 1 below:

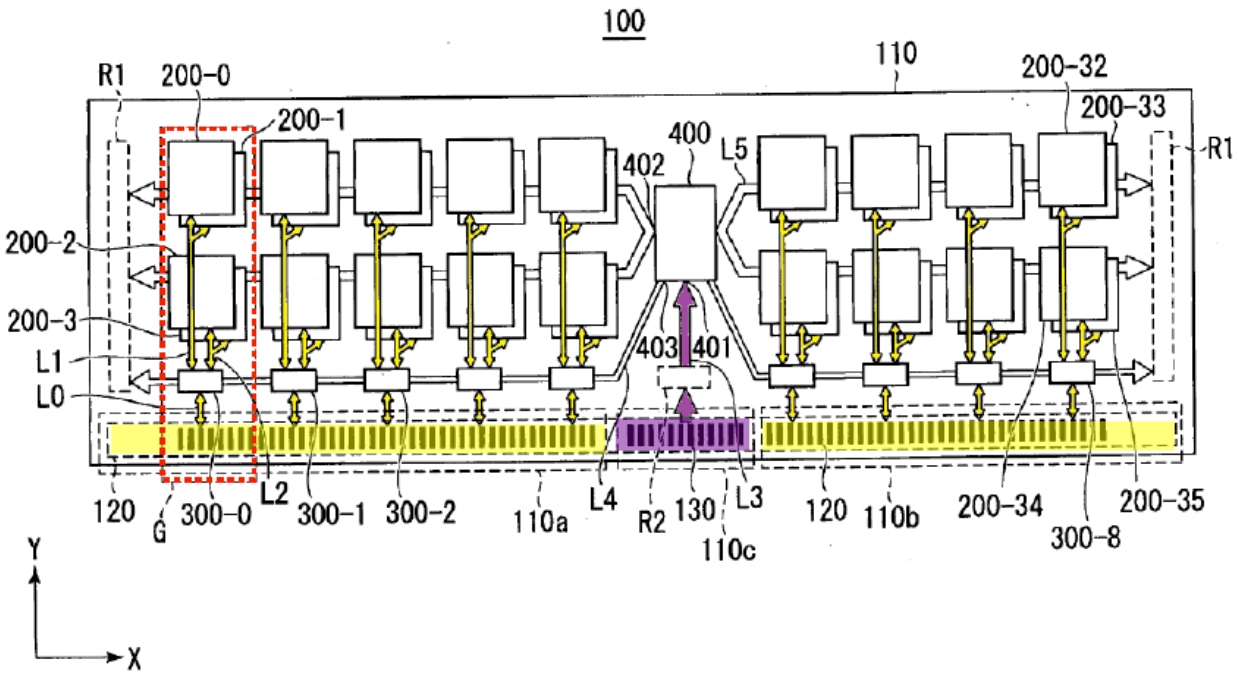


FIG.1

Saito further explains that each memory device in the group (*e.g.*, memory chips 200-0 to 200-3) receives the module command signals from the module control device and performs one or more memory operations in accordance with the module command signals. Ex. 1005 at [0052] ("**An operation of the memory chip 200 is controlled** based on **the command signal, the address signal, the control signal, and the clock signal** ["*module command signals*"] supplied from the command/address/control register buffer 400.") (emphasis added); *id.* at [0060].

Saito thus discloses this claim element. Ex. 1003 at ¶¶107-110.

### *f) a plurality of buffer circuits*

Claim 1 further requires "*a plurality of buffer circuits to receive the module control signals, each respective buffer circuit corresponding to a respective group of memory devices and coupled between the respective group of memory devices and a respective set of the plurality of sets of data/strobe signal lines, the respective buffer circuit including data paths for communicating data between the memory controller and the respective group of memory devices, the data paths being controlled by at least one of the module control signals*."

Saito discloses a plurality of data register buffer circuits 300 that each correspond to a group G of memory devices. Ex. 1005 at [0054] ("With the above configuration, the single **data register buffer 300**, the data connectors 120 and **the four memory chips 200 corresponding to the data register buffer 300** constitute a **group G**.") (emphasis added). The data register buffers are colored blue in annotated Figure below:

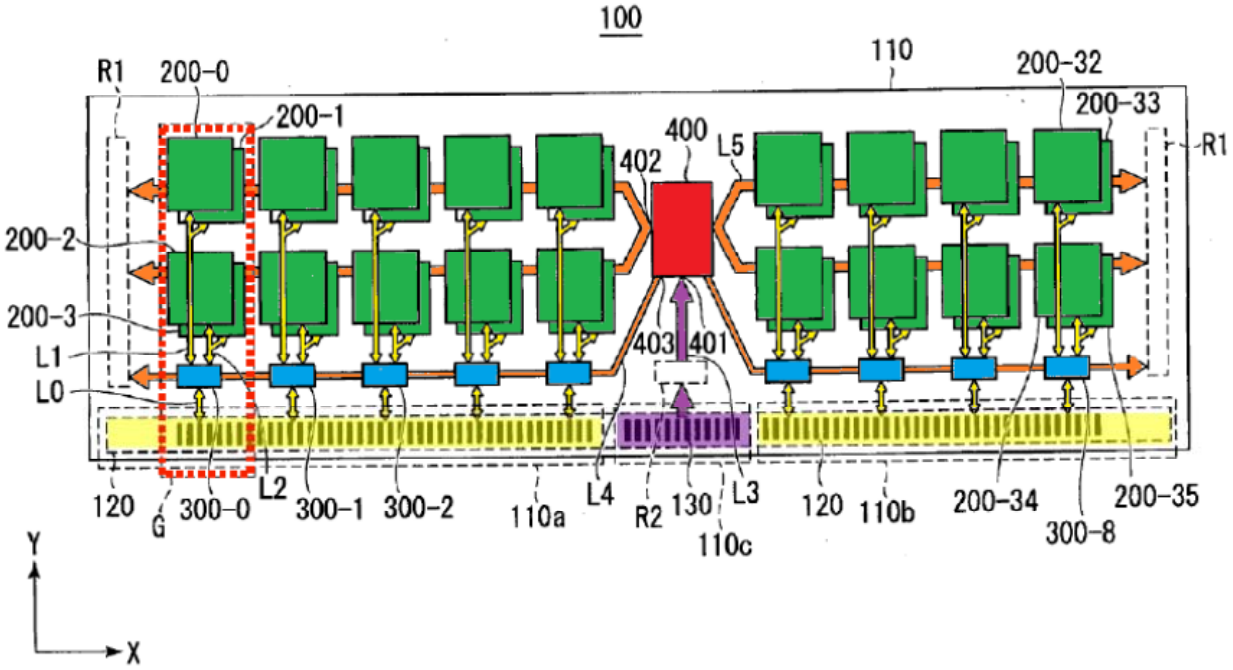


FIG.1

The data register buffers 300 receive module control signals and are coupled between the group G of memory devices and sets of data and strobe signal lines. *Id.* at [0100]; *see also id.* at [0082]. Annotated Figure 7 below illustrates the connections:

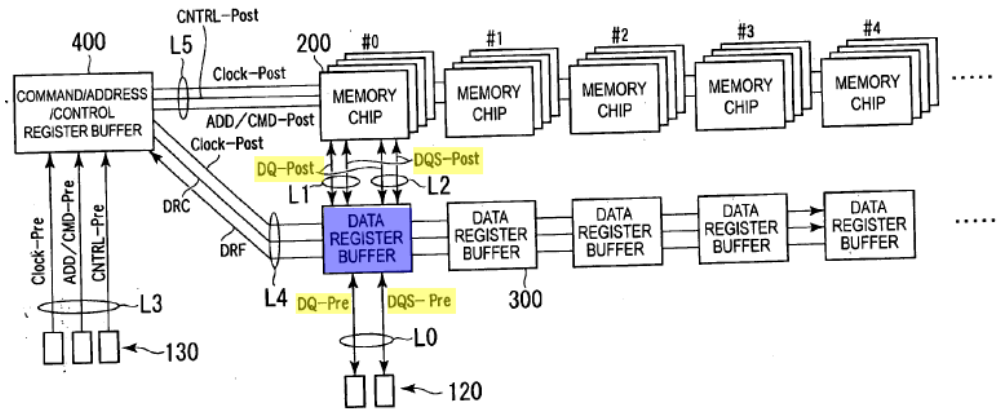


FIG.7

The **data register buffer 300** includes data paths for communicating data between the memory controller and the group of memory devices 200. Ex. 1005 at [0046], [0053]. Saito further discloses that the data paths are controlled by at least one of the module control signals. *Id.* at [0085], [0094]; *see also id.* at [0060], [0088]. And, as shown below in annotated Figure 5, Saito discloses that the data paths of data register buffer circuit 300 are also controlled by the CK signal provided by the command/address/control register buffer 400:

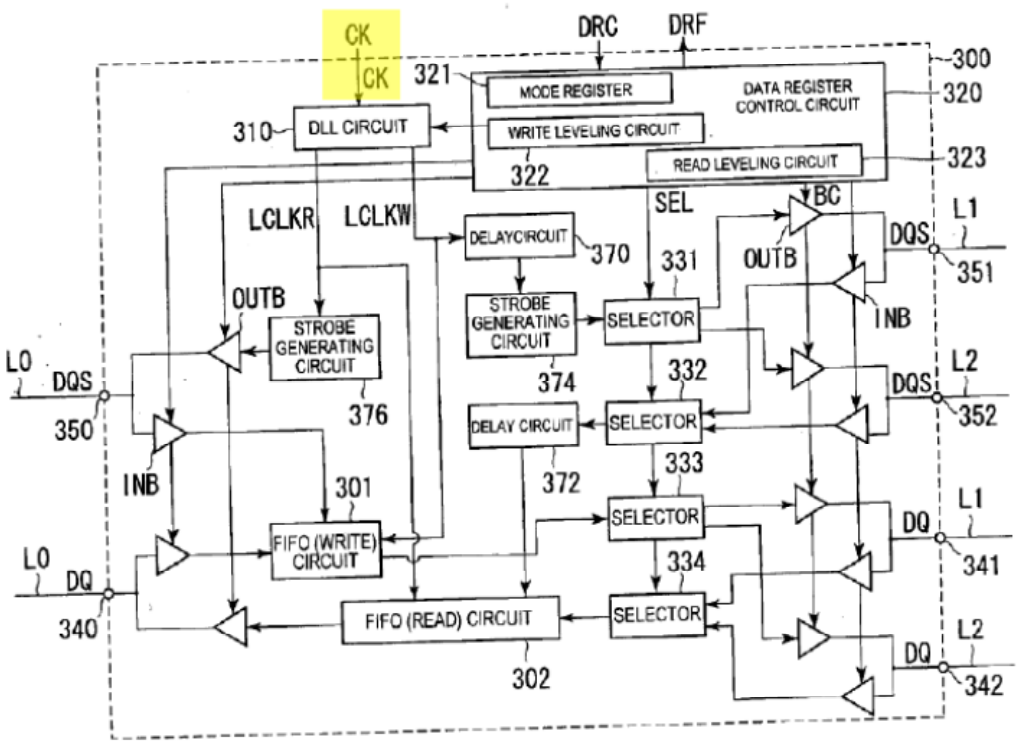


FIG.5

Specifically, at the top left, note clock signal CK being received by the DLL circuit 310, which "is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400, having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200." Ex. 1005 at [0084]. *Compare id.* at Fig. 5 *with* Fig.6. Ex. 1003 at ¶¶112-116.

Saito thus discloses this claim element.

***g)*** *wherein the plurality of buffer circuits are distributed*

Claim 1 further requires "*and wherein the plurality of buffer circuits are distributed across a surface of the memory module in positions corresponding to*

*respective sets of the plurality of sets of data/strobe signal lines such that each module control signal arrives at the plurality of buffer circuits at different points in time*."

Saito discloses that the plurality of data register buffer circuits are distributed across a surface of the memory module in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines. Ex. 1005 at [0054]; *see also id.* at [0082], [0100] (data register buffers 300 are coupled between the memory devices and sets of data and strobe signal lines). The distributed nature of the data register buffers and their correspondence with respective portions of data connectors 120 is illustrated in annotated Figure 1 below:

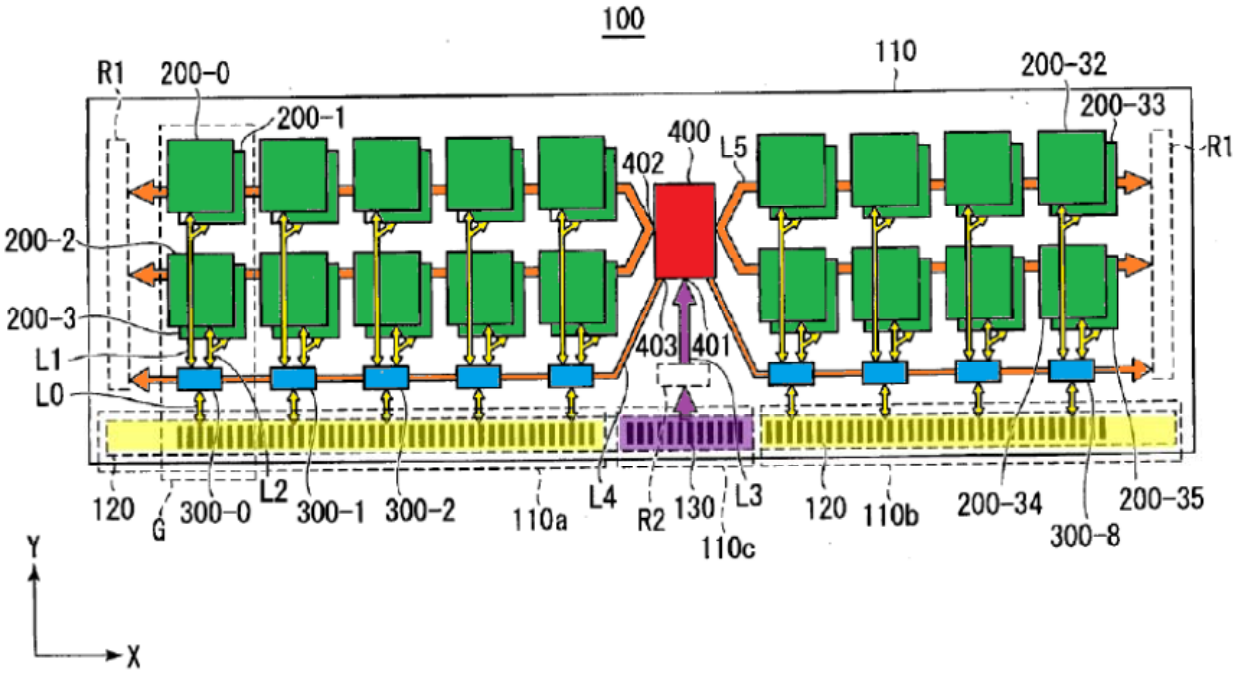


FIG.1

An ordinarily skilled artisan would understand that, in the memory module of Saito, the plurality of data register buffer circuits 300 are distributed such that each module control signal (DRC) arrives at the plurality of buffer circuits at different points in time. Ex. 1003 at ¶120; *see also, e.g.*, U.S. Patent No. 8,565,033 to Manohararajah et al. ("Manohararajah," attached hereto as Ex. 1008) at 6:41-48. Indeed, Saito recognizes that the DRC control signals will arrive at the data register buffers at different times, requiring different signal timing adjustments for each one. Ex. 1005 at [0159]; *see also* Ex. 1006 at 3:18-21.

Saito thus discloses this claim element. Ex. 1003 at ¶¶118-122.

***h)*** *each respective buffer circuit is configured to determine a respective time interval*

Claim 1 further requires "*wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation*."

Saito recognizes that, with high speed operation "memory chips" and "data register buffers" distributed different distances from the "command/address/control register buffer," there will be timing issues with the signals arriving at the

respective chips and buffers requiring "timing adjustments." Ex. 1005 at [0087], [0101]. The memory module of Saito sets these "timing adjustments" during initialization by performing write leveling and read leveling operations. *Id.; see also id.* at [0138-39]; Ex. 1003 at ¶124.

Regarding the write leveling operation "between the data register buffer 300 and the memory chip 200," Ex. 1005 at [0138], Saito explains that the data register buffer "outputs a data strobe signal DQS that is synchronized with the clock signal CK" that is "supplied from the command/address/control register buffer 400" to both the data register buffer and the memory chips, *id.* at [0141]. In response, the memory chip outputs a data signal DQ that "is input to the data register buffer 300, by which the data register buffer 300 can find a direction of phase shift of the clock signal CK and the data strobe signal DQS." *Id.* at [0142]. Thus, utilizing the data signal DQ and the clock signal CK that are input into it, "[t]he write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW based on the direction of the phase shift." *Id.* at [0143]. In this manner, "[u]pon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other." *Id.* at [0144]. While Figure 5 of Saito depicts the clock signal CK being supplied to the DLL circuit 310 of the data register buffer 300, one of

ordinary skill in the art would understand from the description of the operation of the write leveling circuit 322 within the data register control circuit 320 that the write leveling circuit 322 receives the clock signal CK as well – it "find[s] a timing to output the data strobe signal DQS **based on the input clock signal CK**." *Id.(emphasis added); see also* Ex. 1003 at ¶125.

The data register buffers of Saito's memory module separately conduct read leveling operations in a similar manner to write leveling, wherein the data register buffers utilize signals they receive (a read command Read, the clock signal CK and read data DQ) to determine timing adjustments to make. Ex. 1005 at [0145- 0149]; Ex. 1003 at ¶126.

Saito also discloses that its memory module has a known read latency, referred to as CAS latency, that "is set to five clock cycles (CL=5)" in the initialization examples in the specification. Saito discloses that its memory module's known CAS latency ("*read latency*") is used during read operations during normal operation as well. Ex. 1005 at [0126]. And the timing adjustment ("*respective time interval*") that is the result of the read leveling operation during initialization is used with that CAS latency ("*read latency*") to time transmission during read operations. *Id.* at [0128]; Ex. 1003 at ¶127.

The data register buffers of Saito are thus "*configured to determine a respective time interval based on signals received by the each respective buffer*

*circuit during a memory write operation*." And the data register buffers are also "*configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with*" a time interval (determined during the read leveling operation – but not the time interval determined during the writing leveling operation), "*and a read latency parameter of the memory system during a memory read operation*." Saito thus meets the limitations of this element, but for using its time interval determined during the writing leveling operation ("*a memory write operation*") with the read latency parameter during a memory read operation. Ex. 1003 at ¶¶123-128.

However, Swain discloses using the timing intervals determined during write leveling operations in the read leveling operations as well. *Id.* at ¶¶131-133.

Saito and Swain are analogous art to the 632 Patent because each is directed to the field of memory system design, *see* Ex. 1001 at 1:25-28; Ex. 1005 at [0002]; Ex. 1006 at 1:10-14, 3:6-9, and also because they are reasonably pertinent to the particular problem the named inventors of the 632 Patent were trying to solve (dealing with timing constraints involved in memory operations). *See* Ex. 1001 at 1:30-2:21; Ex. 1005 at [0004-0012]; Ex. 1006 at 1:15-2:3; *See also* Ex. 1003 at ¶130.

Swain is focused on systems and methods for performing read leveling in memory modules with memory devices spread across a PCB, Ex. 1006 at Abstract,

as are the memory chips of Saito. And, like Saito, Swain teaches that "[r]ead leveling needs to be performed for each of the memory units since the accurate values for corresponding compensation delay are different for different memory units." *Id.* at 1:39-50.

Of particular relevance, Swain teaches that its system first performs write leveling during initialization and that, during the read leveling operation during initialization, one option for setting the timing adjustment or delay is to use the "parameters determined while write leveling." *Id.* at 5:54-57. In that way, the time interval determined during write leveling is used in read leveling as well, and thus the memory read operations during normal operation. Ex. 1003 at ¶¶131-132.

Given that Saito discloses that the bus line lengthens and transfer rates in its system are the same for both reads and writes, an ordinarily skilled artisan would understand that any time intervals for writes and reads should be the same for a particular portion of the system (*e.g.*, memory chip-data register buffer or data register buffer-memory controller) and time intervals for one could be used for the other, such as Swain teaches for using time intervals determined during write leveling for read leveling as well. *Id.*at ¶133. For instance, Saito teaches:

> Because the data register buffer 300 only performs the buffering of the data, transfer rates of the write data and the read data that are transferred via the data line L0 and transfer rates of the write data and the read data that are

> transferred via the data lines L1 and L2 are equal to each other.

Ex. 1005 at [0089].

A person of ordinary skill in the art would have been motivated to look to the read leveling operation described in Swain as utilizing the time intervals determined during the writing leveling operation when considering Saito because Saito expressly teaches that the write and read intervals are the same, as explained above. Ex. 1003 at ¶134. This teaching is an express suggestion in Saito to use the read leveling operation of Swain (that are based on "parameters determined while write leveling," Ex. 1006 at 5:63-64) for purposes of determining the time interval for memory read operations. A skilled artisan would also have been motivated to use the write-leveling timing as a basis for read leveling in order to avoid having to measure the same period twice. Ex. 1003 at ¶134. Moreover, when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious, which is the case here. Ex. 1005 at [0089]; Ex. 1006 at 5:54-57; Ex. 1003 at ¶135.

If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or

her skill. By 2012 Swain's read leveling operation based on the results of its write leveling operation was well-known. Ex. 1003 at ¶136; Ex. 1006 at 5:54-57. It was thus known to improve memory modules on which it was used. Ex. 1003 at ¶136. Further, its actual application was well within the level of ordinary skill in the art, as it was described and taught by Swain. *Id.*

The combination of Saito and Swain would therefore have been obvious, and satisfies this claim element. *Id.* at ¶¶130-139. Accordingly, claim 1 is obvious over Saito in view of Swain. *Id.* at ¶¶90-140.

**2. Claim 2 is Obvious**

Claim 2 requires *"[t]he memory module of claim 1, wherein each module control signal arrives at the plurality of buffer circuits at different points in time across more than one clock cycle of the system clock."*

As explained above, an ordinarily skilled artisan would understand that, in the memory module of Saito, the plurality of data register buffers 300 are distributed such that each module control signal (DRC) arrives at the plurality of buffers at different points in time. *Id.* at ¶¶118-122. Given the frequencies disclosed in Saito and the distances between the nine different memory ranks on its standard size DIMM, one of ordinary skill in the art would also understand that each module control signal (DRC) arrives at different data register buffers across more than one clock cycle. Ex. 1005 at [0005]; Ex. 1003 at ¶142. Indeed, the 632

Patent itself teaches that it is at 1600 MHz in standard DIMMs when signals arrive at different data buffers across more than one clock cycle. Ex. 1001 at 9:36-42. Saito thus discloses "*wherein each module control signal arrives at the plurality of buffer circuits at different points in time across more than one clock cycle of the system clock.*" Ex. 1003 at ¶¶141-143.

Claim 2 also requires "*and wherein the each respective buffer circuit is configured to align the respective set of read data signals such that different sets of read data signals corresponding to the memory read operation are transmitted by the different buffer circuits onto different sets of data/strobe signal lines in the memory bus within one system clock cycle*."

As described above, Saito performs write and read leveling operations to adjust the timing of writes and reads. *Id.* at ¶¶123-139; Ex. 1005 at [0138]. These leveling operations are performed such that "the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other." Ex. 1005 at [0144]. For read leveling, "**[t]he time is measured** for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and **used in an adjustment of an activation timing of the input buffer circuit INB and the like**." *Id.* at [0149] (emphasis added). And, during normal operation, the data register buffers use the time intervals determined during leveling operations to properly time data transfers to the memory

controllers. *Id*. at [0128]. One of ordinary skill would therefore understand this to mean that the data register buffers each transmit the data requested by a read operation during one system clock cycle. Ex. 1003 at ¶145; *see also* Ex. 1003 at ¶146; Ex. 1006 at 3:31-44.

Saito thus discloses this claim element, and claim 2 is obvious over Saito in view of Swain. Ex. 1003 at ¶¶141-148.

### 3. Claim 3 is Obvious

Claim 3 requires *"[t]he memory module of claim 1, wherein each buffer circuit includes receiver circuits to receive corresponding ones of the module control signals.*"

Saito discloses that each data register buffer 300 ("*buffer circuit*") receives a control signal DRC and clock signal CK ("*module control signals*") via its data register control circuit 320 and DLL circuit 310 ("*receiver circuits*"). Ex. 1005 at [0085]. The **DRC and CK signals** depicted below in annotated Figure 5 are module control signals. *See, e.g., id.* at [0097].

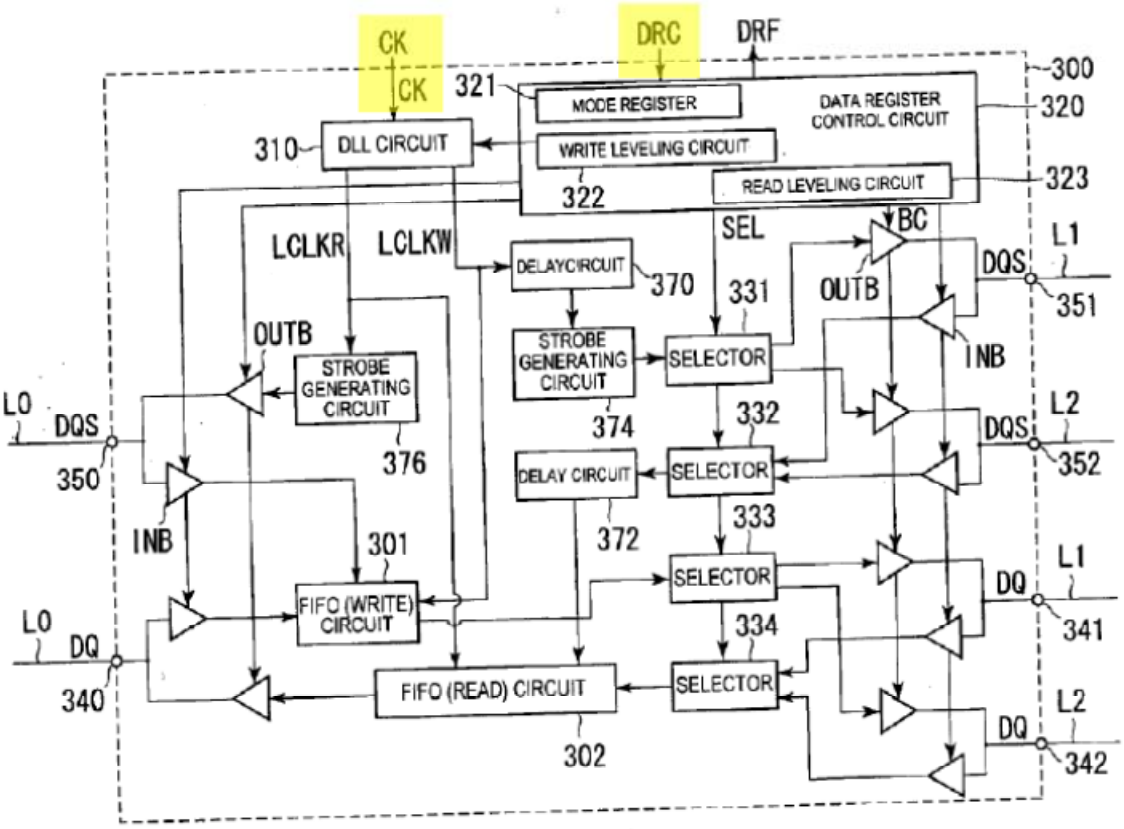


FIG.5

Saito thus discloses "*wherein each buffer circuit includes receiver circuits to receive corresponding ones of the module control signals*." Ex. 1003 at ¶¶149-151.

Claim 3 also requires "*each receiver circuit including a metastability detection circuit to detect metastability condition in the corresponding module control signal, and wherein each buffer circuit further includes at least one signal adjustment circuit to adjust one or more the module control signals to mitigate any metastability condition in the module control signals*." The broadest reasonable

interpretation of "metastability" is "misalignment of a signal from the relevant clock signal."

Saito discloses that its data register buffers 300 ("*buffer circuits*") each include a data register control circuit 320 and DLL circuit 310 ("*receiver circuits*") "that controls the operation of the data register buffer 300 based on a control signal DRC that is supplied from the command/address/control register buffer 400." Ex. 1005 at [0085]. Saito further discloses that the DLL circuits (that includes a "*metastability detection circuit*" and a "*signal adjustment circuit*") adjust the timing of data transfers to mitigate metastability conditions. To illustrate this, Figure 5 of Saito is reproduced below with annotations:

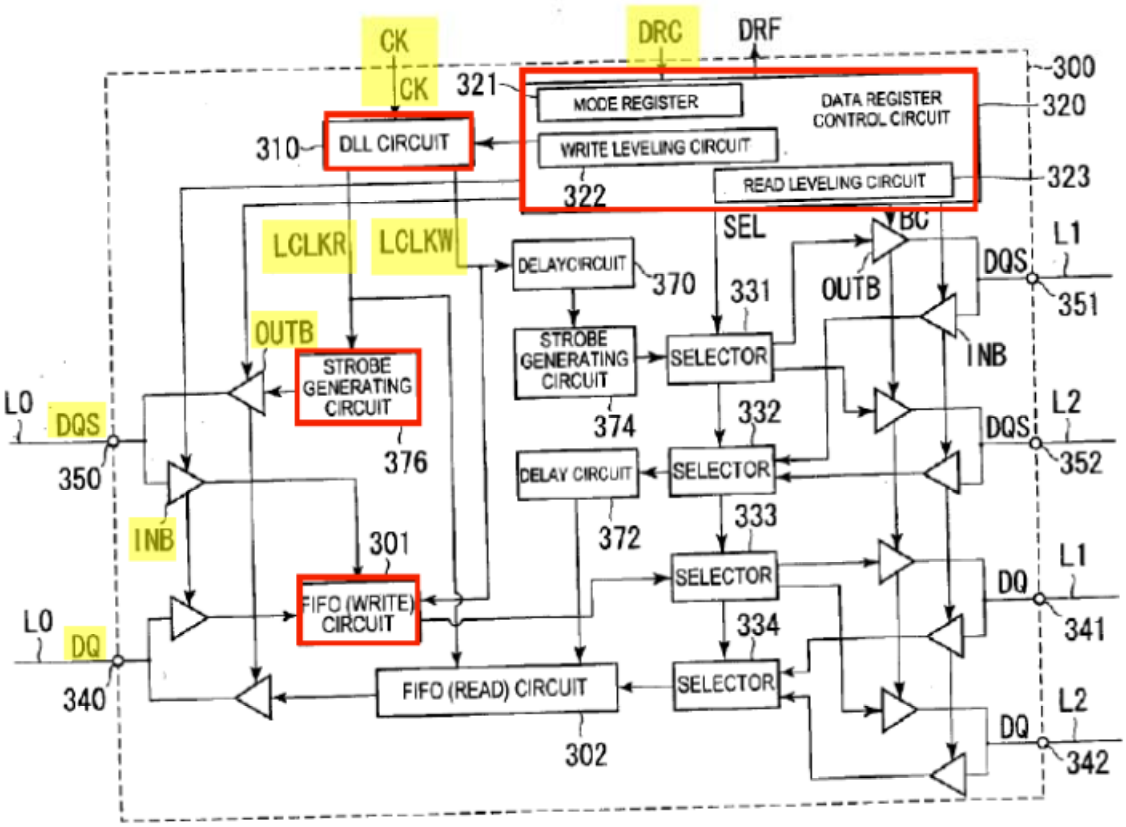


FIG.5

The DLL circuit 310 of the data register buffers "is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400, having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200." Ex. 1005 at [0084]. And Saito explains that the DLL circuit detects misalignments of the DQ and DQS signals compared to the clock signal CK and makes adjustments to correct the misalignments. *Id.* at [0073]; Ex. 1003 at ¶154. The DLL circuit thus includes a "*metastability detection circuit*."

The internal clocks LCLKW and LCLKR are fed to, among other circuits in the data register buffers, a "strobe generating circuit 376" that "generates a data strobe signal DQS to be supplied to the data connectors 120, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310," and a "FIFO (Read) circuit 302 [that] buffers data DQ" and whose timing "is defined by the internal clock LCLKW that is generated by the DLL circuit 310." *Id.* at [0082], [0084]. The DLL circuit, through its phase adjustment of internal clocks LCLKW and LCLKR, thus adjusts module control signals such as CK. The DLL circuit's internal circuitry that adjusts the CK signal is a "*signal adjustment circuit*." Ex. 1003 at ¶154.

Saito thus discloses this claim element, and claim 3 is obvious over Saito in view of Swain. *Id.* at ¶¶149-156.

#### 4. Claim 4 is Obvious

Claim 4 requires "*[t]he memory module of claim 1, wherein the module control device further receives the system clock from the system memory controller and transmits a registered clock signal to the plurality of buffer circuits*."

Saito discloses that the **command/address/control register buffer 400** ("*module control device*") receives the system clock **CK** from the **memory controller**. Ex. 1005 at [0045]. Saito further discloses that the command/address/control register buffer 400 ("*module control device*") transmits a

registered clock signal to the plurality of data register buffers 300 ("*plurality of buffer circuits*"). Ex. 1005 at [0105]; *see also Id.* at Fig. 7. Clock signal "Clock-Post" is a "*registered clock signal*."

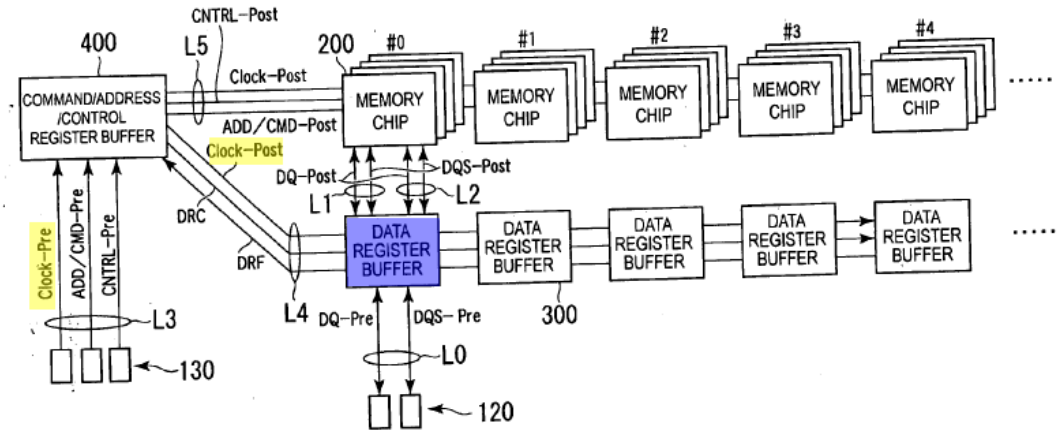


FIG.7

Saito thus discloses "*[t]he memory module of claim 1, wherein the module control device further receives the system clock from the system memory controller and transmits a registered clock signal to the plurality of buffer circuits*." Ex. 1003 at ¶¶162-165.

Claim 4 also requires "*and wherein the each respective buffer circuit regenerates one or more clock signals from the registered clock signal and provides a regenerated clock signal to the respective group of memory devices*."

As described above, the DLL circuit of each data register buffer creates adjusted ("*regenerated*") clock signals to account for misalignment of the clock

signal with control signals. Ex. 1003 at ¶¶149-161. While Saito does not disclose providing those adjusted clock signals to the data register buffer's respective memory chips (instead, each memory chip includes its own DLL circuit that adjusts the clock signal from the command/address/control register buffer), it would have been obvious to one or ordinary skill in the art to remove those DLL circuits from the memory chips and instead provide the adjusted ("*regenerated*") clock signals from the data register buffers (and their DLL circuits) instead. *Id.* at ¶167. Saito explains that the respective DLL circuits function in the same manner. Ex. 1005 at [0084]. And one of ordinary skill would understand that removing the DLL circuit from the memory chips would save space in those chips, reduce their complexity and lessen potential failure points. Ex. 1003 at ¶167. And Saito specifically teaches that, "while the above embodiment has described a memory chip that includes a DLL circuit therein as the memory chip 200, a memory chip that does not include a DLL circuit therein can be alternatively used. In this case, the DLL circuit included in the data register buffer 300 is used to adjust the input/output timing." Ex. 1005 at [0197]. A skilled artisan would therefore have been motivated to employ such modified circuitry in Saito. Ex. 1003 at ¶¶166-170. Accordingly, claim 4 is obvious over Saito in view of Swain. *Id.* at ¶¶162-171.

### 5. Claim 5 is Obvious

Claim 5 requires "*[t]he memory module of claim 1, wherein the respective buffer circuit comprises: a time interval determination circuit to receive, during a write operation, a first signal from the module controller and a second signal from the memory bus and to generate a delay signal indicating a time interval between the first signal and the second signal and a delay circuit to delay the respective set of read data signals received from the respective group of memory devices according to the delay signal*."

As explained above, Saito in view of Swain renders this limitation obvious. *See supra* Part V.A.1.h). Claim 5 merely labels some of the circuitry and signals discussed above. Specifically, Saito's "write leveling circuit 322" is the "*time interval determination circuit*" and it receives the clock signal CK from the module controller and the data signal DQ from the memory bus and uses them to generate delay signals that the data register buffers then use during normal read operations to delay read data signals. Ex. 1003 at ¶173. *See also supra* Part V.A.1.h). Saito in view of Swain thus render obvious this claim element, and claim 5 is obvious over Saito in view of Swain. *Id.* at ¶¶172-175.

### 6. Claim 12 is Unpatentable

#### ***a)*** *Preamble part 1*

The first part of the preamble of claim 12 requires "*[a] buffer circuit for use in a memory module coupled to a memory controller via a memory bus*." Saito

discloses a plurality of **data register buffer circuits 300** ("*buffer circuits*") that connect to **data connectors 120 via data line L0** ("*memory bus*"). Ex. 1005 at [0083]. The data connectors 120 are "terminals for making an electrical connection with a memory controller via a memory slot." *Id.* at [0045]. Saito thus discloses this claim element. Ex. 1003 at ¶¶176-178.

***b)*** *Preamble part 2*

The second part of the preamble of claim 12 requires "*the memory bus including a set of control/address signal lines and a plurality of sets of data/strobe signal lines*." Saito discloses this claim element for the same reasons stated above with respect to the third part of the preamble of claim 1. *See supra* Part V.A.1.c).

***c)*** *Preamble part 3*

The third part of the preamble of claim 12 requires "*the memory module including a plurality of memory devices organized in groups and a module controller coupled to the memory controller via the set of control/address signal lines, comprising*."

As explained with respect to the "*memory devices organized in groups*" element of claim 1 above, *see supra* Part V.A.1.e), Saito discloses a memory module "*including a plurality of memory devices organized in groups*". Ex. 1005 at [0051].

Saito further discloses a command/address/control register buffer 400 ("*module controller*") coupled to the memory controller via a set of control/address signal lines. Specifically, Saito discloses that the **command/address/control register buffer 400** "receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a **command/address/control signal** and the like) that are supplied from the **command/address/control connectors 130** through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200." Ex. 1005 at [0058] (emphasis added). As previously explained, the command/address/control connectors 130 are terminals for making an electrical connection with a memory controller via a memory slot. *See supra* Part V.A.1.c). Figure 1 illustrates that the command/address/control register buffer 400 receives this set of control/address signals via command/address/control line L3.

Saito thus discloses this claim element. Ex. 1003 at ¶¶181-184.

***d)*** *"time interval determination circuit" and "delay circuit"*

Claim 12 requires "*a time interval determination circuit to determine a time interval between receiving a first signal from the module controller and receiving a second signal from the memory bus; and a delay circuit to time transmission of data/strobe signals received from a respective group of the plurality of memory*

*devices to the memory controller via a respective set of the plurality of sets of data/strobe signal lines according to the time interval*."

As explained above, Saito in view of Swain renders this limitation obvious. *See supra* Part V.A.1.h). This element of claim 12 merely labels some of the circuitry and signals discussed above, and omits the requirement that the time interval necessarily be determined during a write operation. Specifically, Saito's "write leveling circuit 322" is the "*time interval determination circuit*" and it receives the clock signal CK from the module controller and the data signal DQ from the memory bus and uses them to generate delay signals that circuitry in the data register buffers ("*delay circuit*") then use during normal read operations to delay read data signals. Ex. 1003 at ¶186; *see also supra* Part V.A.1.h).

Accordingly, claim 12 is obvious over Saito in view of Swain. Ex. 1003 at ¶¶176-188.

**7. Claim 13 is Obvious**

Claim 13 requires "*[t]he buffer circuit of claim 12 wherein the buffer further comprises receiver circuits to receive corresponding ones of the module control signals, each receiver circuit including a metastability detection circuit to detect metastability condition in the corresponding module control signal.*" Saito discloses this claim element for the same reasons stated above with respect to claim 3. *See supra* Part V.A.3. This claim includes a subset of the limitations of

claim 3. Saito thus discloses this claim element. Accordingly, claim 13 is obvious over Saito in view of Swain. Ex. 1003 at ¶¶189-192.

**8. Claim 14 is Obvious**

Claim 14 requires "*[t]he buffer circuit of claim 12 wherein the buffer circuit further comprises at least one signal adjustment circuit to adjust one or more the module control signals to mitigate metastability condition in the module control signals.*" Saito discloses this claim element for the same reasons stated above with respect to claim 3. *See supra* Part V.A.3. This claim includes a subset of the limitations of claim 3. Saito thus discloses this claim element. Accordingly, claim 14 is obvious over Saito in view of Swain. *Id.* at ¶¶193-196.

**9. Claim 19 is Obvious**

Claim 19 requires "*[t]he buffer circuit of claim 12, further comprising: a clock regeneration circuit to receive a clock signal from the module controller and to regenerate a regenerated clock signal according to the time interval.*"

As described above, the DLL circuit of each data register buffer creates adjusted ("*regenerated*") clock signals to account for misalignment of the clock signal with control signals. *See supra* Part V.A.3. The DLL circuit is a "*clock regeneration circuit*" that receives a clock signal CK from the command/address/control register buffer ("*module controller*") and creates adjusted clock signals LCLKR and LCLWR ("*regenerated clock signals*"). Ex.

1005 at [0084] (stating that DLL circuit 310 of the data register buffers "is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400"). Saito teaches that the DLL circuit performs that adjustment of the clock signal CK based at least in part on the time interval determined during the write leveling operation, *i.e.*, the claimed "time interval." *See supra* Part V.A.1.h). Specifically, Saito explains that "[t]he write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS **by displacing the internal clock LCLKW based on the direction of the phase shift**." Ex. 1005 at [0143] (emphasis added). And Figure 5 shows the write leveling circuit 322 outputing a signal to the DLL circuit that adjusts the clock signal CK to create adjusted clock signals LCLKR and LCLWR:

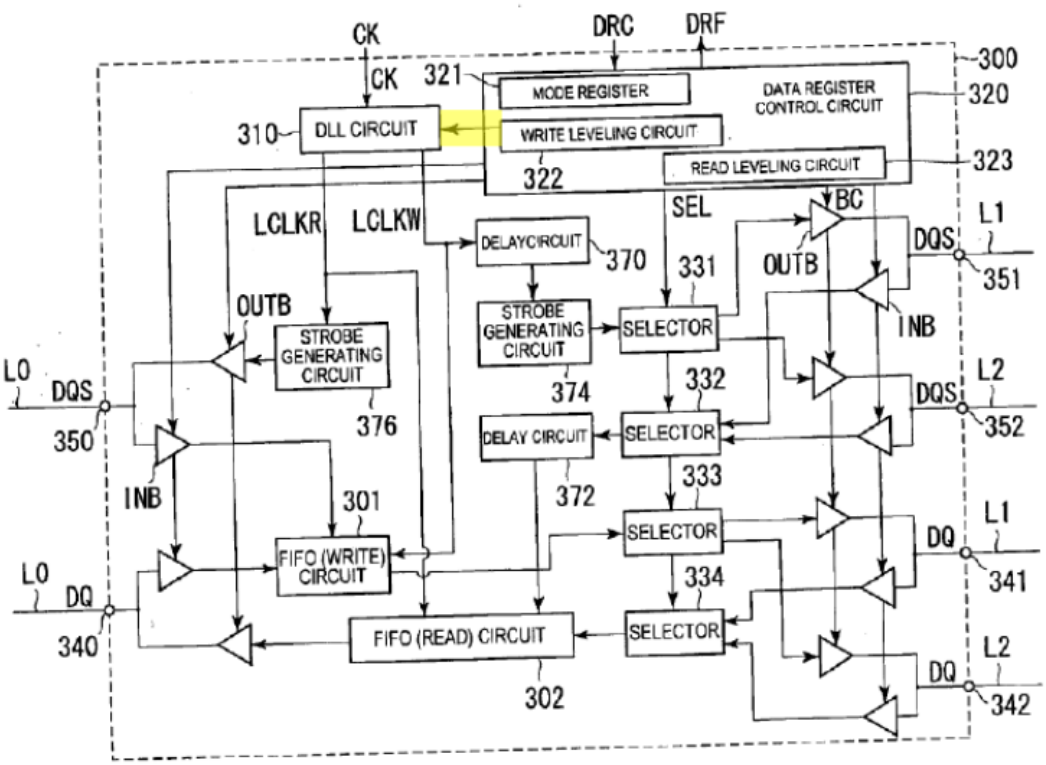


FIG.5

As Dr. Mudge opines, Ex. 1003 at ¶198, one of ordinary skill in the art would understand that the signal from the write leveing circuit 322 to the DLL circuit 310 that "displac[es] the internal clock LCLKW based on the direction of the phase shift" represents the claimed "time interval" that is determined by the write leveling circuit 322 during write leveling operations in the combined Saito/Swain circuit as described *supra* Part V.A.1.h).

Accordingly, claim 19 is obvious over Saito in view of Swain. Ex. 1003 at ¶¶197-200.

#### 10. Claim 20 is Obvious

Claim 20 requires "*[t]he buffer circuit of claim 12, wherein the buffer circuit is coupled to a respective group of the plurality of memory devices on the memory module*."

Saito discloses this claim element for the same reasons stated above with respect to the "*a plurality of buffer circuits*" element of claim 1. *See supra* Part V.A.1.f). This claim element includes a subset of the limitations of the "*a plurality of buffer circuits*" element of claim 1. Claim 20 also requires "*and wherein the buffer circuit further comprises a clock regeneration circuit to receive a clock signal from the module controller and to provide a regenerated clock signal to the respective group of the plurality of memory devices*." Saito renders obvious this claim element for the same reasons stated above with respect to the second element of claim 4. *See supra* Part V.A.4. Accordingly, claim 20 is obvious over Saito in view of Swain. Ex. 1003 at ¶¶201-205.

### B. Claims 3 and 13-14 are Obvious Over Saito in view of Swain in further view of Kim

#### 1. Claim 3 is Obvious

Claim 3 requires "*[t]he memory module of claim 1, wherein each buffer circuit includes receiver circuits to receive corresponding ones of the module control signals*." Saito discloses this element for the reasons as described above for this element when applying the combination of Saito and Swain to claim 3. *See*

*supra* Part V.A.3. Saito thus discloses "*wherein each buffer circuit includes receiver circuits to receive corresponding ones of the module control signals*."

Claim 3 also requires "*each receiver circuit including a metastability detection circuit to detect metastability condition in the corresponding module control signal, and wherein each buffer circuit further includes at least one signal adjustment circuit to adjust one or more the module control signals to mitigate any metastability condition in the module control signals*."

To the extent one might argue that Saito's DLL circuit does not include a metastability detection circuit and/or signal adjustment circuit as claimed, U.S. Patent No. 6,184,701 to Kim ("Kim") (Ex. 1007) discloses such circuitry and it would have been obvious to combine that circuitry with Saito's data register buffers. Ex. 1003 at ¶¶157-161.

Kim discloses "a metastability detection/prevention circuit 20" to be incorporated with any "main active circuit 10" in need thereof. Ex. 1007 at 2:23-24. Kim teaches that the "**the circuit 10 may comprise a data input buffer**." *Id.* at 2:33-37 (emphasis added). "[T]he metastability detection/prevention circuit 20 preferably performs the function of detecting whether the output POUT of the main active circuit 10 has been disposed in a metastable state for a duration in excess of a transition duration." *Id.* at 2:3-57.

A skilled artisan would have been motivated to employ such a combination. It was well-known that metastability of signals transmitted between clock domains (such as the register devices of Saito) can cause problems "because the designer cannot guarantee that the signal will meet setup and hold time requirements," thereby causing communication failures, Altera Corp., Quartus II Handbook Volume 3: Verification, Section II at 12 (Ver. 11.0 May 2011) (Ex. 1010); U.S. Patent No. 6,072,346 at 1:27-61 (Ex. 1011); U.S. Patent No. 8,552,779 at 5:62-6:12 (Ex. 1012), so a skilled artisan would have been motivated to avoid such problems. Kim discloses that its "metastability detection/prevention circuit" is useful for and can be used in Saito's data register buffers to avoid metastable conditions. Ex. 1007 at 2:30-31 ("**the circuit 10 may comprise a data input buffer**") (emphasis added). This would motivate one of ordinary skill in the art to incorporate Kim's circuit in the buffer of Saito. Ex. 1003 at ¶159.

Specifically, Kim's "metastability detection/prevention circuit" would be incorporated into Saito's data register buffer circuits with the buffers' data register control circuits and DLL circuits to detect metastability in input signals clock signal CK and control signal DRC by sampling the directly related output data signals DQ and/or data strobe signals DQS and adjusting the input signals by providing a PCON signal to the inputs to avoid metastable conditions. When incorporated in Saito's data register buffers, Kim's "metastability

detection/prevention circuit" would be "*a metastability detection circuit to detect metastability condition in the corresponding module control signal* [detecting the metastability of the input CK signal and control DRC signal by measuring the metastability of the directly related output DQ and DQS signals], *and wherein each buffer circuit further includes at least one signal adjustment circuit* [the circuit that generates PCON and adds it to the input signals] *to adjust one or more the module control signals to mitigate any metastability condition in the module control signals*." Ex. 1003 at ¶160.

Accordingly, claim 3 is obvious over Saito in view of Swain in further view of Kim. *Id.* at ¶¶157-161.

**2. Claim 13 is Obvious**

Claim 13 requires "*[t]he buffer circuit of claim 12 wherein the buffer further comprises receiver circuits to receive corresponding ones of the module control signals, each receiver circuit including a metastability detection circuit to detect metastability condition in the corresponding module control signal*."

Saito renders obvious in view of Kim this claim element for the same reasons stated above with respect to claim 3. *See supra* Part V.B.1. This claim includes a subset of the limitations of claim 3. Saito thus renders obvious in view of Kim "*[t]he buffer circuit of claim 12 wherein the buffer further comprises receiver circuits to receive corresponding ones of the module control signals, each*

*receiver circuit including a metastability detection circuit to detect metastability condition in the corresponding module control signal.*" Accordingly, claim 13 is obvious over Saito in view of Swain in further view of Kim. Ex. 1003 at ¶¶189-192.

#### 1. Claim 14 is Obvious

Claim 14 requires "*[t]he buffer circuit of claim 12 wherein the buffer circuit further comprises at least one signal adjustment circuit to adjust one or more the module control signals to mitigate metastability condition in the module control signals.*" Saito renders obvious in view of Kim this claim element for the same reasons stated above with respect to claim 3. *See supra* Part V.B.1. This claim includes a subset of the limitations of claim 3. Saito thus renders obvious in view of Kim "*[t]he buffer circuit of claim 12 wherein the buffer circuit further comprises at least one signal adjustment circuit to adjust one or more the module control signals to mitigate metastability condition in the module control signals.*" Accordingly, claim 14 is obvious over Saito in view of Swain in further view of Kim. Ex. 1003 at ¶¶193-196.

## VI. CONCLUSION

Because the information presented in this petition shows that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the petition, the Petitioner respectfully requests that a

Trial be instituted and that claims 1-5, 12-14 and 19-20 be canceled as unpatentable.

Dated: January 20, 2017

Respectfully Submitted,

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## CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 10,024 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

**PETITION FOR INTER PARTES REVIEW**

**OF U.S. PATENT NO. 9,128,632**

**Attachment A:**

**Proof of Service of the Petition**

## CERTIFICATE OF SERVICE

I hereby certify that on this 20th day of January, 2017, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by overnight mail on the following counsel of record for patent owner:

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# PETITION FOR INTER PARTES REVIEW

# OF U.S. PATENT NO. 9,128,632

## Attachment B:

## List of Evidence and Exhibits Relied Upon in Petition

| Exhibit # | Reference Name |
|---|---|
| 1001 | U.S. Patent No. 9,128,632 |
| 1002 | File History of U.S. Patent No. 9,128,632 |
| 1003 | Declaration of Dr. Trevor Mudge |
| 1004 | Curriculum Vitae of Dr. Trevor Mudge |
| 1005 | United States Published Patent Application No. 2010/0309706 to Saito ("Saito") |
| 1006 | United States Patent No. 7,808,849 to Swain ("Swain") |
| 1007 | United States Patent No. 6,184,701 to Kim ("Kim") |
| 1008 | United States Patent No. 8,565,033 to Manohararajah ("Manohararajah") |
| 1009 | MICROSOFT COMPUTER DICTIONARY (5th Ed. 2002) |
| 1010 | Altera Corp., Quartus II Handbook Volume 3: Verification (Version 11.0 May 2011) |
| 1011 | U.S. Patent No. 6,072,346 |
| 1012 | U.S. Patent No. 8,552,779 |