I, Julie Carlson, declare as follows:

1. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same.

2. I have been involved in semiconductor standardization and publication services for over twenty years. For nearly all of this time, I have worked at JEDEC, a standards-setting organization for the microelectronics industry, to edit, publish, and maintain JEDEC business records and standards developed by its numerous committees and subcommittees.

3. I have been involved with the standardization and publication activities of JEDEC continuously since 1997. I was the Manager of Standards and Publications at JEDEC from February 1997 through June 2005. Since June 2005, I have continued to work for JEDEC as a Consultant where my responsibilities include the maintenance and publication of JEDEC documents and standards. In addition, I am familiar with JEDEC's historical record-keeping and publication practices since at least 1992, based on my review of JEDEC's business records since that time and my regular discussions with JEDEC employees and members.

4. For over 50 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry. JEDEC's membership consists of more than 3,000 volunteers representing nearly 300



Micron Technology Inc. et al.
Ex. 1017, p. 1

member companies, and includes key technical individuals from most device, assembly, system and testing companies. JEDEC publications and standards are adopted worldwide. JEDEC is accredited by ANSI and maintains liaisons with numerous standards bodies throughout the world.

5. Since at least 2000, JEDEC standards have been publicly available for download from the JEDEC website (https://www.jedec.org), where they are cataloged and indexed by keyword and technological subject matter. By 2000, the JEDEC website was publicly available and commonly used by manufactures, companies in the microelectronics industry, and other interested parties to access and obtain standards information pertaining to that industry. Anyone interested can join JEDEC online, at JEDEC.org.

6. This declaration concerns JEDEC Standard No. 21-C, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification (January 2002), Page 4.20.4-1 to -82 (hereinafter, "JESD21-C"). The copy of JESD21-C attached to this declaration as Exhibit A is identical to the copy of JESD21-C in JEDEC's files.

7. The following statements on the public availability of JESD21-C as of January 2002 and October 2003 are based on personal knowledge. The development of all JEDEC documents follows the process set forth in JM21: JEDEC Manual of Organization and Procedure. According to that process, the

date on the cover of a JEDEC document is the month the document was finalized, approved by legal, and posted to the website. For JESD21-C, the date on the cover is January 2002. However, JESD21-C was part of JEDEC Standard No. 21-C, for which JEDEC provided an update service where specific pages could be updated as part of a periodic "Release." In the copy of JESD21-C attached as Exhibit A, most pages (like the cover page dated January 2002) were published in January 2002. A few pages were updated as part of Release 12, *see* Exhibit A at pages 4.20.4-6 to -9, -22, and one page was updated as part of Release 13 in October 2003, *see* Exhibit A at page 4.20.4-71.

8. I am familiar with the circulation and publication procedures used by JEDEC. Upon approval of the Board of Directors, the JEDEC publications department prepares documents for publication, and seeks final review and approval to publish from the JEDEC legal department. Once legal approval is received, the JEDEC publications department uploads the approved document to the JEDEC website with a brief description. An email announcement is then sent to the sponsoring committee and any approved resellers. By 2000, JEDEC made its published standards available for download from www.jedec.org, as mentioned above.

9. Based on my personal knowledge of JEDEC's policies, most of the pages of the copy of JESD21-C attached as Exhibit A were made publicly

available in January 2002 and all of the pages of the copy of JESD21-C attached as Exhibit A were made publicly available by October 2003. My knowledge of the procedures surrounding the creation of the date notation and publication is based on JEDEC's policies and practices as I understand them through my work at JEDEC. I rely on these policies and practices in the course of my work. I have no reason to believe that JEDEC's typical practice was not followed. I have no reason to believe that JESD21-C was not made publicly accessible in January 2002 in October 2003 as described above.

10. To further confirm my statements above regarding JESD21-C, I have visited the Internet Archive to look at the first capture of the online catalog at www.jedec.org after January 2002, which occurred on November 5, 2002: <http://web.archive.org/web/20021105112938/http://www.jedec.org/Catalog/display.cfm>. A printout of this capture is attached as Exhibit B and is consistent with my personal recollection of the JEDEC website. As can be seen from this capture on November 5, 2002, the JEDEC Standard No. 21-C was cataloged, indexed with the title "CONFIGURATIONS FOR SOLID STATE MEMORIES" and the keyword "21-C," and was available to the public by that date, consistent with my statements above. *See* Exhibit B at pages 6, 43, 66. The JEDEC website explained, "JESD21-C is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC Council

from September 1989. This latest issue has changed to a loose-leaf format and comes in a three-ring binder so that new drawings can be added without requiring a new publication." *See* Exhibit B at page 6. In addition, the JEDEC website offered an "ANNUAL UPDATING SERVICE" for the JEDEC Standard No. 21-C: "The JEDEC Office has generated a mailing list for those who wish to subscribe to updates of this publication." *See* Exhibit B at page 6. As explained above, JESD21-C attached as Exhibit A was part of JEDEC Standard No. 21-C, for which JEDEC provided an update service where specific pages could be updated as part of a periodic "Release." The capture on November 5, 2002, attached as Exhibit B included a link to the Table of Contents for the current Release of the JEDEC Standard No. 21-C. *See* Exhibit B at page 66. I have visited the Internet Archive to look at the first capture of that Table of Contents after January 2002, which occurred on April 21, 2003: <http://web.archive.org/web/20021105112938/http://www.jedec.org/download/search/21C_TOCR11b.pdf>. A printout of this capture is attached as Exhibit C and is consistent with my personal recollection of the JEDEC website and the JEDEC Standard No. 21-C. As can be seen from this Table of Contents attached as Exhibit C, "4.20.4 — 184 Pin PC1600/2100 DDR SDRAM Registered DIMM Design Specification" was included as part of "Release 11" to the JEDEC Standard No.

21-C and made available to the public, consistent with my statements above about JESD21-C attached as Exhibit A. *See* Exhibit C at page xxi.

11. Exhibit D is a printout of <https://web.archive.org/web/20031208154552/http://www.jedec.org:80/service_members/New_Members/memberco.cfm>, which is a capture on December 8, 2003. Exhibit D shows the list of member companies on JEDEC's website as of that date, which is consistent with my personal recollection of JEDEC's membership. All of those member companies would have had access to JESD21-C attached as Exhibit A no later than that date.

I, Julie Carlson, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on 2021/09/16 Julie D. Carlson

Julie D. Carlson

# Exhibit A

# PC2100 and PC1600 DDR SDRAM Registered DIMM

# **Design Specification**

Revision 1.3

January 2002



Micron Technology Inc. et al.
Ex. 1017, p. 8

Micron Technology Inc. et al.
Ex. 1017, p. 9

**Product Description** ..... **5**

**Environmental Requirements** ..... **6**

**Architecture** ..... **6**
Block Diagram: Raw Card Version A/L (x72 DIMM, One Physical Bank) ..... 10
Block Diagram: Raw Card Version A/L (x64 DIMM, One Physical Bank) ..... 11
Block Diagram: Raw Card Version A/L (x72 DIMM, Two Physical Banks) ..... 12
Block Diagram: Raw Card Version A/L (x64 DIMM, Two Physical Banks) ..... 13
Block Diagram: Raw Card Version B/M ..... 10
Block Diagram: Raw Card Version N ..... 15
Block Diagram: Raw Card Version C/E ..... 16
Differential Clock Net Wiring (CK0, $\overline{CK0}$) ..... 17

**Component Details** ..... **20**
Pin Assignments for 64Mb, 128Mb, 256Mb, 512Mb and 1Gb DDR SDRAM Planar Components ..... 20
Pin Assignments for 64Mb, 128Mb, 256Mb, 512Mb and 1Gb DDR SDRAM 2-High Stack Package . 21
DDR SDRAM Component Specifications ..... 21
Register Component Specifications ..... 22
Register Sourcing ..... 23
PLL Component Specifications ..... 23
PLL Sourcing ..... 24

**Registered DIMM Details** ..... **25**
DDR Registered Design File Releases ..... 28
Example Raw Card Versions A (1 Physical Bank) Component Placement ..... 29
Example Raw Card Versions A (2 Physical Banks) Component Placement ..... 30
Example Raw Card Version B Component Placement ..... 31
Example Raw Card Version C/E Component Placement ..... 32
Example Raw Card Versions L (2 Physical Banks) and M Component Placement ..... 33
Example Raw Card Versions L (1 Physical Banks) Component Placement ..... 34
Example Raw Card Versions N (2 Physical Banks) Component Placement ..... 35

**DIMM Wiring Details** ..... **36**
Signal Groups ..... 36
General Net Structure Routing Guidelines ..... 36
Explanation of Net Structure Diagrams ..... 37
Differential Clock Net Structures ..... 38
Data Net Structures ..... 44
Net Structure Routing for CS and CKE ..... 54
Cross Section Recommendations ..... 66



Micron Technology Inc. et al.
Ex. 1017, p. 10

**Timing Budget** ..... **67**

**Serial PD Definition** ..... **68**

**Product Label** ..... **71**

**DIMM Mechanical Specifications** ..... **72**

**Supporting Hardware** ..... **73**
Clock Reference Board ..... 73

**Application Notes** ..... **74**
Clocking Timing Methodology ..... 74

**Revision Log** ..... **75**



Micron Technology Inc. et al.
Ex. 1017, p. 11

# Product Description

This specification defines the electrical and mechanical requirements for 184-pin, 2.5 Volt, PC1600/PC2100, 64/72 bit-wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs).These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC1600/PC2100 refers to the JEDEC standard DIMM naming convention in which PC1600 indicates a 184-pin DIMM running at 100 MHz clock speed and offering 1600MB/s bandwidth.

Reference design examples are included which provide an initial basis for Registered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC1600/PC2100 support. All registered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 184-pin Registered DDR SDRAM DIMM product (refer to JEDEC Standards Manual 21-C, at http://www.jedec.org).

## Product Family Attributes

| | |
|---|---|
| DIMM organization | x72 ECC, x64 |
| DIMM dimensions (nominal) | 5.25" x 1.2”/1.7" |
| Pin count | 184 |
| SDRAMs supported | 64Mb, 128Mb, 256Mb, 512Mb, 1Gb |
| Capacity | 64MB, 128MB, 256MB, 512MB, 1GB, 2GB, 4GB |
| Serial PD | Consistent with JC 42.5 Rev 0 |
| Voltage options | 2.5 volt ($V_{DD}/V_{DDQ}$) |
| Interface | SSTL_2 |



Micron Technology Inc. et al.
Ex. 1017, p. 12

# Environmental Requirements

DDR SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

## Environmental Parameters

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| $T_{OPR}$ | Operating temperature (ambient) | 0 to +55 | °C | 1 |
| $H_{OPR}$ | Operating humidity (relative) | 10 to 90 | % | 1 |
| $T_{STG}$ | Storage temperature | -50 to +100 | °C | 1 |
| $H_{STG}$ | Storage humidity (without condensation) | 5 to 95 | % | 1 |
| $P_{BAR}$ | Barometric pressure (operating & storage) | 105 to 69 | K Pascal | 1, 2 |

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

# Architecture

## Pin Description

| Pin Name | Description | Pin Name | Description |
|---|---|---|---|
| A0 - A15 | SDRAM address bus | CK0 | SDRAM clock (positive line of differential pair) |
| BA0 - BA1 | SDRAM bank select | $\overline{CK0}$ | SDRAM clock (negative line of differential pair) |
| DQ0 - DQ63 | DIMM memory data bus | SCL | IIC serial bus clock for EEPROM |
| CB0 - CB7 | DIMM ECC check bits | SDA | IIC serial bus data line for EEPROM |
| $\overline{RAS}$ | SDRAM row address strobe | SA0 - SA2 | IIC slave address select for EEPROM |
| $\overline{CAS}$ | SDRAM column address strobe | $V_{DD}$ | SDRAM positive power supply |
| $\overline{WE}$ | SDRAM write strobe | $V_{DDQ}$ | SDRAM I/O Driver positive power supply |
| $\overline{S}0$ - $\overline{S}3$ | SDRAM chip select lines (Physical. banks 0, 1, 2, and 3) | $V_{REF}$ | SDRAM I/O reference supply |
| CKE0 - CKE1 | SDRAM clock enable lines | $V_{SS}$ | Power supply return (ground) |
| DQS0 - DQS8 | SDRAM low data strobes | $V_{DDSPD}$ | Serial EEPROM positive power supply (Supports both 2.5 Volt and 3.3 Volt operation) |
| DM(0-8)/DQS(9-17) | SDRAM low data masks/high data strobes (x4, x8-based x72 DIMMs) | NC | Spare Pins (no connect) |
| $V_{DDID}$ | $V_{DD}$ Identification Flag | $\overline{RESET}$ | Reset pin (forces register inputs low) |
| Test | Used by memory bus analysis tools (unused on memory DIMMs) | | |



Micron Technology Inc. et al.
Ex. 1017, p. 13

## Input/Output Functional Description

| Symbol | Type | Polarity | Function |
|---|---|---|---|
| CK0 | SSTL | Positive Edge | Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL. (All DDR SDRAM addr/cntl inputs are sampled on the rising edge of their associated clocks.) |
| $\overline{CK0}$ | SSTL | Negative Edge | Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL. |
| CKE0, CKE1 | SSTL | Active High | Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode. |
| $\overline{S}0$, $\overline{S}1$, $\overline{S}2$, $\overline{S}3$ | SSTL | Active Low | Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | SSTL | Active Low | When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM. |
| $V_{REF}$ | Supply | | Reference voltage for SSTL2 inputs |
| $V_{DDQ}$ | Supply | | Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity |
| BA0,BA1 | SSTL | — | Selects which SDRAM bank of four is activated. |
| A0 - A9, A11 A10/AP, A12- A15 | SSTL | — | During a Bank Activate command cycle, A0-A15 defines the row address (RA0-RA15) when sampled at the rising clock edge.<br>During a Read or Write command cycle, A0-A12 defines the column address (CA0-CA12) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled.<br>During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge. |
| DQ0 - DQ63, CB0 - CB7 | SSTL | — | Data and Check Bit Input/Output pins |
| DM0-DM8 | SSTL | Active High | Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM. |
| $V_{DD}$, $V_{SS}$ | Supply | | Power and ground for the DDR SDRAM input buffers and core logic |
| DQS0-DQS8 | SSTL | Negative and Positive Edge | Data strobe for input and output data. |
| SA0 - 2 | | — | These signals are tied at the system planar to either $V_{SS}$ or $V_{DD}$ to configure the serial SPD EEPROM address range. |
| SDA | | — | This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to $V_{DD}$ to act as a pullup. |
| SCL | | — | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to $V_{DD}$ to act as a pullup. |
| $V_{DDSPD}$ | Supply | | Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports both 2.3 Volt and 3.3 Volt operation). |
| $\overline{RESET}$ | LV-CMOS | Active Low | This signal is asynchronous and driven low to the register to guarantee that the register outputs are low. |



Micron Technology Inc. et al.
Ex. 1017, p. 14

## 184-Pin DDR SDRAM DIMM Pin Assignments

| Front Side (left side 1 - 52, right side 53 - 92) | | | Back Side (left side 93 -144, right side 145 -184) | | | Front Side (left side 1 - 52, right side 53 - 92) | | | Back Side (left side 93 -144, right side 145 -184) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin # | x64 Non-Parity | x72 ECC | Pin # | x64 Non-Parity | x72 ECC | Pin # | x64 Non-Parity | x72 ECC | Pin # | x64 Non-Parity | x72 ECC |
| 1 | $V_{REF}$ | $V_{REF}$ | 93 | $V_{SS}$ | $V_{SS}$ | 48 | A0 | A0 | 140 | NC | DM8,DQS17 |
| 2 | DQ0 | DQ0 | 94 | DQ4 | DQ4 | 49 | NC | CB2 | 141 | A10 | A10 |
| 3 | $V_{SS}$ | $V_{SS}$ | 95 | DQ5 | DQ5 | 50 | $V_{SS}$ | $V_{SS}$ | 142 | NC | CB6 |
| 4 | DQ1 | DQ1 | 96 | $V_{DDQ}$ | $V_{DDQ}$ | 51 | NC | CB3 | 143 | $V_{DDQ}$ | $V_{DDQ}$ |
| 5 | DQS0 | DQS0 | 97 | DM0,DQS9 | DM0,DQS9 | 52 | BA1 | BA1 | 144 | NC | CB7 |
| 6 | DQ2 | DQ2 | 98 | DQ6 | DQ6 | KEY | | | KEY | | |
| 7 | $V_{DD}$ | $V_{DD}$ | 99 | DQ7 | DQ7 | 53 | DQ32 | DQ32 | 145 | $V_{SS}$ | $V_{SS}$ |
| 8 | DQ3 | DQ3 | 100 | $V_{SS}$ | $V_{SS}$ | 54 | $V_{DDQ}$ | $V_{DDQ}$ | 146 | DQ36 | DQ36 |
| 9 | NC,A15 | NC,A15 | 101 | NC | NC | 55 | DQ33 | DQ33 | 147 | DQ37 | DQ37 |
| 10 | $\overline{RESET}$ | $\overline{RESET}$ | 102 | NC,TEST | NC,TEST | 56 | DQS4 | DQS4 | 148 | $V_{DD}$ | $V_{DD}$ |
| 11 | $V_{SS}$ | $V_{SS}$ | 103 | NC | NC | 57 | DQ34 | DQ34 | 149 | DM4,DQS13 | DM4,DQS13 |
| 12 | DQ8 | DQ8 | 104 | $V_{DDQ}$ | $V_{DDQ}$ | 58 | $V_{SS}$ | $V_{SS}$ | 150 | DQ38 | DQ38 |
| 13 | DQ9 | DQ9 | 105 | DQ12 | DQ12 | 59 | BA0 | BA0 | 151 | DQ39 | DQ39 |
| 14 | DQS1 | DQS1 | 106 | DQ13 | DQ13 | 60 | DQ35 | DQ35 | 152 | $V_{SS}$ | $V_{SS}$ |
| 15 | $V_{DDQ}$ | $V_{DDQ}$ | 107 | DM1,DQS10 | DM1,DQS10 | 61 | DQ40 | DQ40 | 153 | DQ44 | DQ44 |
| 16 | NC (CK1)[1] | NC (CK1)[1] | 108 | $V_{DD}$ | $V_{DD}$ | 62 | $V_{DDQ}$ | $V_{DDQ}$ | 154 | $\overline{RAS}$ | $\overline{RAS}$ |
| 17 | NC ($\overline{CK1}$)[1] | NC ($\overline{CK1}$)[1] | 109 | DQ14 | DQ14 | 63 | $\overline{WE}$ | $\overline{WE}$ | 155 | DQ45 | DQ45 |
| 18 | $V_{SS}$ | $V_{SS}$ | 110 | DQ15 | DQ15 | 64 | DQ41 | DQ41 | 156 | $V_{DDQ}$ | $V_{DDQ}$ |
| 19 | DQ10 | DQ10 | 111 | CKE1 | CKE1 | 65 | $\overline{CAS}$ | $\overline{CAS}$ | 157 | $\overline{S0}$ | $\overline{S0}$ |
| 20 | DQ11 | DQ11 | 112 | $V_{DDQ}$ | $V_{DDQ}$ | 66 | $V_{SS}$ | $V_{SS}$ | 158 | $\overline{S1}$ | $\overline{S1}$ |
| 21 | CKE0 | CKE0 | 113 | NC(BA2) | NC(BA2) | 67 | DQS5 | DQS5 | 159 | DM5,DQS14 | DM5,DQS14 |
| 22 | $V_{DDQ}$ | $V_{DDQ}$ | 114 | DQ20 | DQ20 | 68 | DQ42 | DQ42 | 160 | $V_{SS}$ | $V_{SS}$ |
| 23 | DQ16 | DQ16 | 115 | A12,NC | A12,NC | 69 | DQ43 | DQ43 | 161 | DQ46 | DQ46 |
| 24 | DQ17 | DQ17 | 116 | $V_{SS}$ | $V_{SS}$ | 70 | $V_{DD}$ | $V_{DD}$ | 162 | DQ47 | DQ47 |
| 25 | DQS2 | DQS2 | 117 | DQ21 | DQ21 | 71 | NC, $\overline{S2}$ | NC, $\overline{S2}$ | 163 | NC, $\overline{S3}$ | NC, $\overline{S3}$ |
| 26 | $V_{SS}$ | $V_{SS}$ | 118 | A11 | A11 | 72 | DQ48 | DQ48 | 164 | $V_{DDQ}$ | $V_{DDQ}$ |
| 27 | A9 | A9 | 119 | DM2,DQS11 | DM2,DQS11 | 73 | DQ49 | DQ49 | 165 | DQ52 | DQ52 |
| 28 | DQ18 | DQ18 | 120 | $V_{DD}$ | $V_{DD}$ | 74 | $V_{SS}$ | $V_{SS}$ | 166 | DQ53 | DQ53 |
| 29 | A7 | A7 | 121 | DQ22 | DQ22 | 75 | NC ($\overline{CK2}$)[1] | NC ($\overline{CK2}$)[1] | 167 | A13,NC | A13,NC |
| 30 | $V_{DDQ}$ | $V_{DDQ}$ | 122 | A8 | A8 | 76 | NC (CK2)[1] | NC (CK2)[1] | 168 | $V_{DD}$ | $V_{DD}$ |
| 31 | DQ19 | DQ19 | 123 | DQ23 | DQ23 | 77 | $V_{DDQ}$ | $V_{DDQ}$ | 169 | DM6,DQS15 | DM6,DQS15 |
| 32 | A5 | A5 | 124 | $V_{SS}$ | $V_{SS}$ | 78 | DQS6 | DQS6 | 170 | DQ54 | DQ54 |
| 33 | DQ24 | DQ24 | 125 | A6 | A6 | 79 | DQ50 | DQ50 | 171 | DQ55 | DQ55 |
| 34 | $V_{SS}$ | $V_{SS}$ | 126 | DQ28 | DQ28 | 80 | DQ51 | DQ51 | 172 | $V_{DDQ}$ | $V_{DDQ}$ |

NC = No Connect; NU = Not Useable; DU = Do Not Use

1. These pins reserved for unbuffered DDR DIMMs. Systems supporting both unbuffered and registered DIMMs may be connected to an active signal on the baseboard.
2. The TEST pin is reserved for bus analysis probes and is not connected on normal memory modules (DIMMs)



Micron Technology Inc. et al.
Ex. 1017, p. 15

## 184-Pin DDR SDRAM DIMM Pin Assignments

| Front Side (left side 1 - 52, right side 53 - 92) | | | Back Side (left side 93 -144, right side 145 -184) | | | Front Side (left side 1 - 52, right side 53 - 92) | | | Back Side (left side 93 -144, right side 145 -184) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin # | x64 Non-Parity | x72 ECC | Pin # | x64 Non-Parity | x72 ECC | Pin # | x64 Non-Parity | x72 ECC | Pin # | x64 Non-Parity | x72 ECC |
| 35 | DQ25 | DQ25 | 127 | DQ29 | DQ29 | 81 | $V_{SS}$ | $V_{SS}$ | 173 | NC,A14 | NC,A14 |
| 36 | DQS3 | DQS3 | 128 | $V_{DDQ}$ | $V_{DDQ}$ | 82 | $V_{DDID}$ | $V_{DDID}$ | 174 | DQ60 | DQ60 |
| 37 | A4 | A4 | 129 | DM3,DQS12 | DM3,DQS12 | 83 | DQ56 | DQ56 | 175 | DQ61 | DQ61 |
| 38 | $V_{DD}$ | $V_{DD}$ | 130 | A3 | A3 | 84 | DQ57 | DQ57 | 176 | $V_{SS}$ | $V_{SS}$ |
| 39 | DQ26 | DQ26 | 131 | DQ30 | DQ30 | 85 | $V_{DD}$ | $V_{DD}$ | 177 | DM7,DQS16 | DM7,DQS16 |
| 40 | DQ27 | DQ27 | 132 | $V_{SS}$ | $V_{SS}$ | 86 | DQS7 | DQS7 | 178 | DQ62 | DQ62 |
| 41 | A2 | A2 | 133 | DQ31 | DQ31 | 87 | DQ58 | DQ58 | 179 | DQ63 | DQ63 |
| 42 | $V_{SS}$ | $V_{SS}$ | 134 | NC | CB4 | 88 | DQ59 | DQ59 | 180 | $V_{DDQ}$ | $V_{DDQ}$ |
| 43 | A1 | A1 | 135 | NC | CB5 | 89 | $V_{SS}$ | $V_{SS}$ | 181 | SA0 | SA0 |
| 44 | NC | CB0 | 136 | $V_{DDQ}$ | $V_{DDQ}$ | 90 | NC | NC | 182 | SA1 | SA1 |
| 45 | NC | CB1 | 137 | CK0 | CK0 | 91 | SDA | SDA | 183 | SA2 | SA2 |
| 46 | $V_{DD}$ | $V_{DD}$ | 138 | $\overline{CK0}$ | $\overline{CK0}$ | 92 | SCL | SCL | 184 | $V_{DDSPD}$ | $V_{DDSPD}$ |
| 47 | NC | DQS8 | 139 | $V_{SS}$ | $V_{SS}$ | | | | | | |

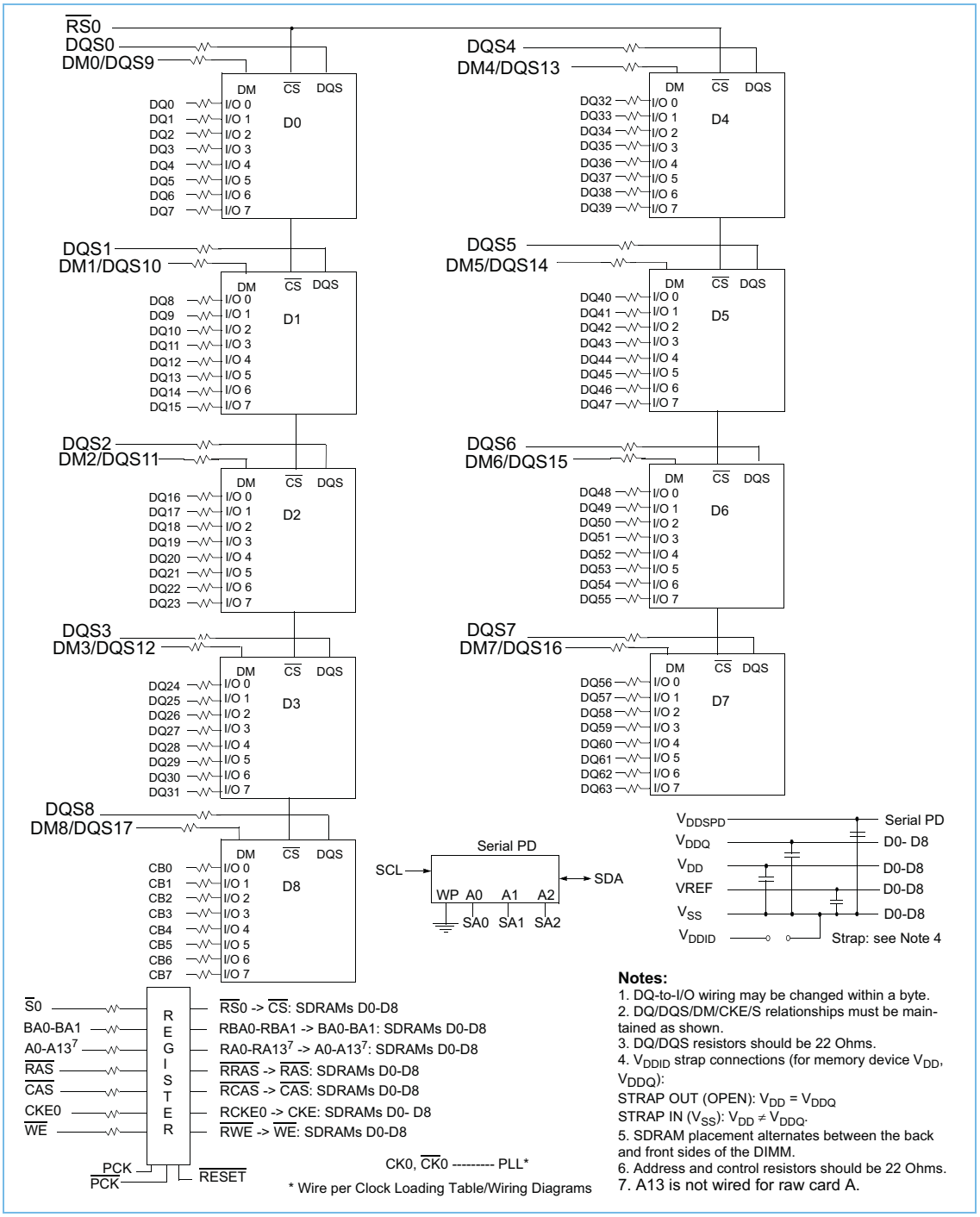
NC = No Connect; NU = Not Useable; DU = Do Not Use

1. These pins reserved for unbuffered DDR DIMMs. Systems supporting both unbuffered and registered DIMMs may be connected to an active signal on the baseboard.
2. The TEST pin is reserved for bus analysis probes and is not connected on normal memory modules (DIMMs)



Micron Technology Inc. et al.
Ex. 1017, p. 16

## Block Diagram: Raw Card Version A/L (x72 DIMM, populated as one physical bank of x8 DDR SDRAMs)

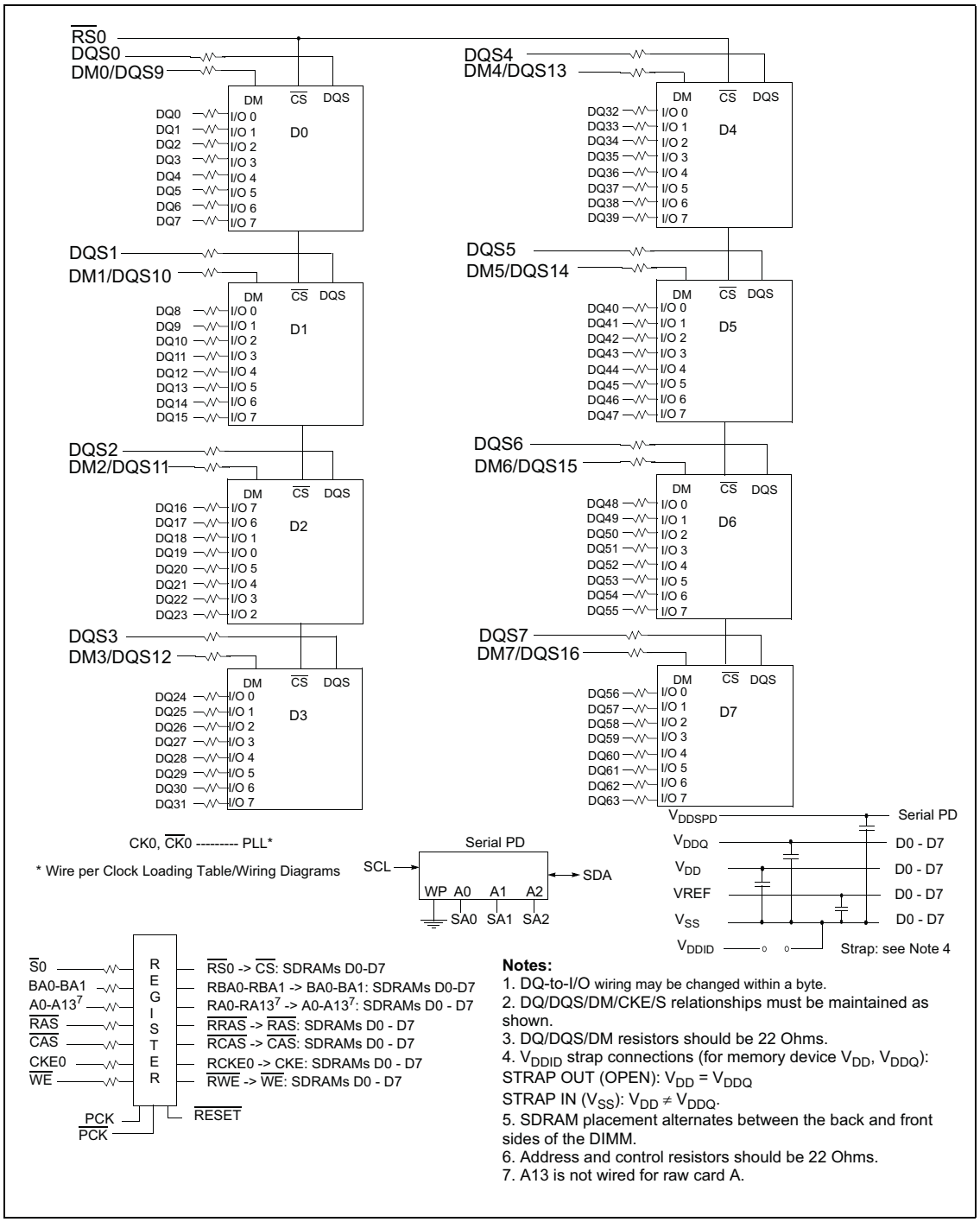



**Notes:**
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN ($V_{SS}$): $V_{DD} \neq V_{DDQ}$.
5. SDRAM placement alternates between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.
7. A13 is not wired for raw card A.



Micron Technology Inc. et al.
Ex. 1017, p. 17

## Block Diagram: Raw Card Version A/L (x64 DIMM, populated as one physical bank of x8 DDR SDRAMs)

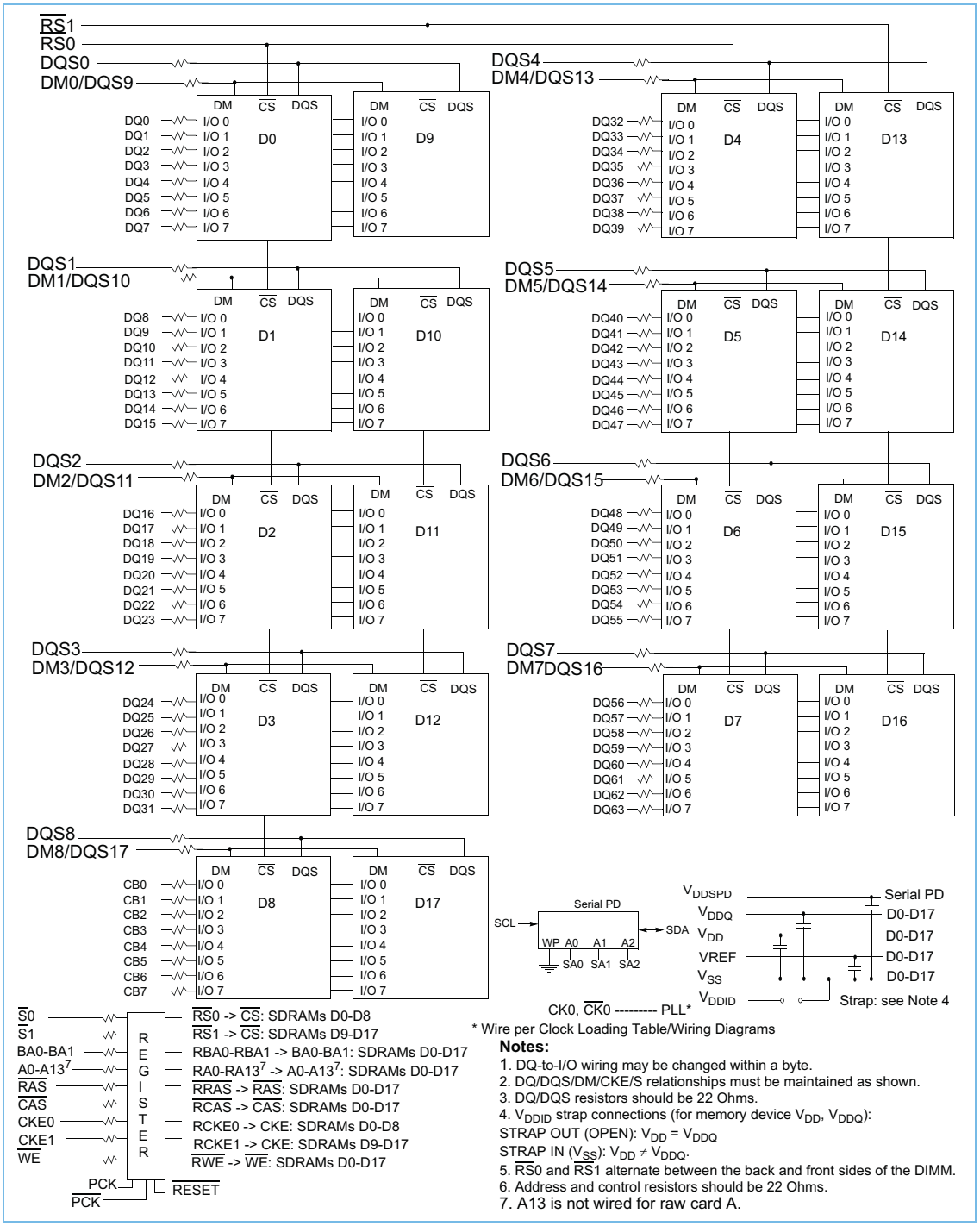



**Notes:**
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS/DM resistors should be 22 Ohms.
4. $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN ($V_{SS}$): $V_{DD} \neq V_{DDQ}$.
5. SDRAM placement alternates between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.
7. A13 is not wired for raw card A.



Micron Technology Inc. et al.
Ex. 1017, p. 18

## Block Diagram: Raw Card Version A/L (x72 DIMM, populated as two physical banks of x8 DDR SDRAMs)




* Wire per Clock Loading Table/Wiring Diagrams

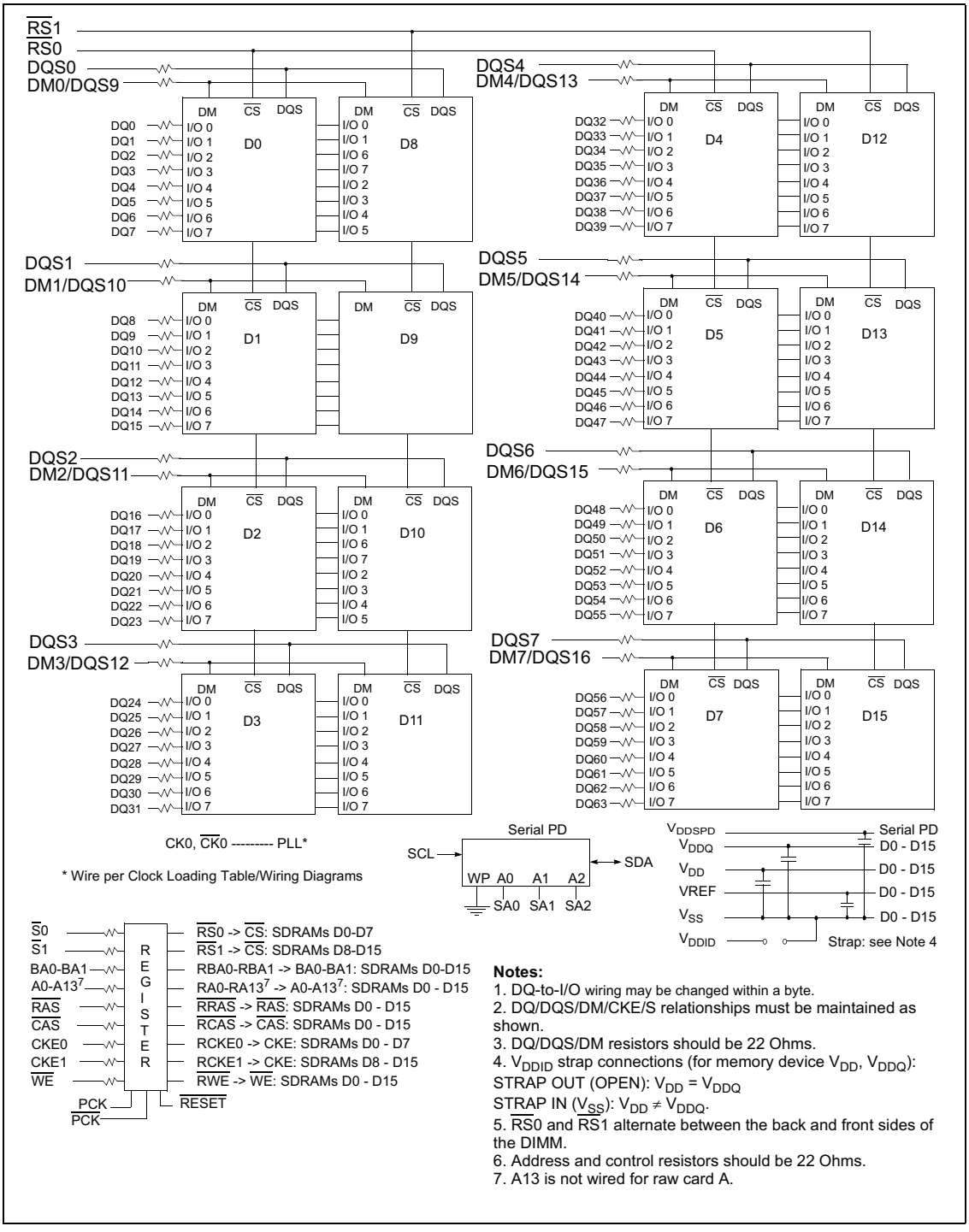
**Notes:**

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN ($V_{SS}$): $V_{DD} \neq V_{DDQ}$.
5. $\overline{RS}0$ and $\overline{RS}1$ alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.
7. A13 is not wired for raw card A.



Micron Technology Inc. et al.
Ex. 1017, p. 19

## Block Diagram: Raw Card Version A/L (x64 DIMM, populated as two physical banks of x8 DDR SDRAMs)

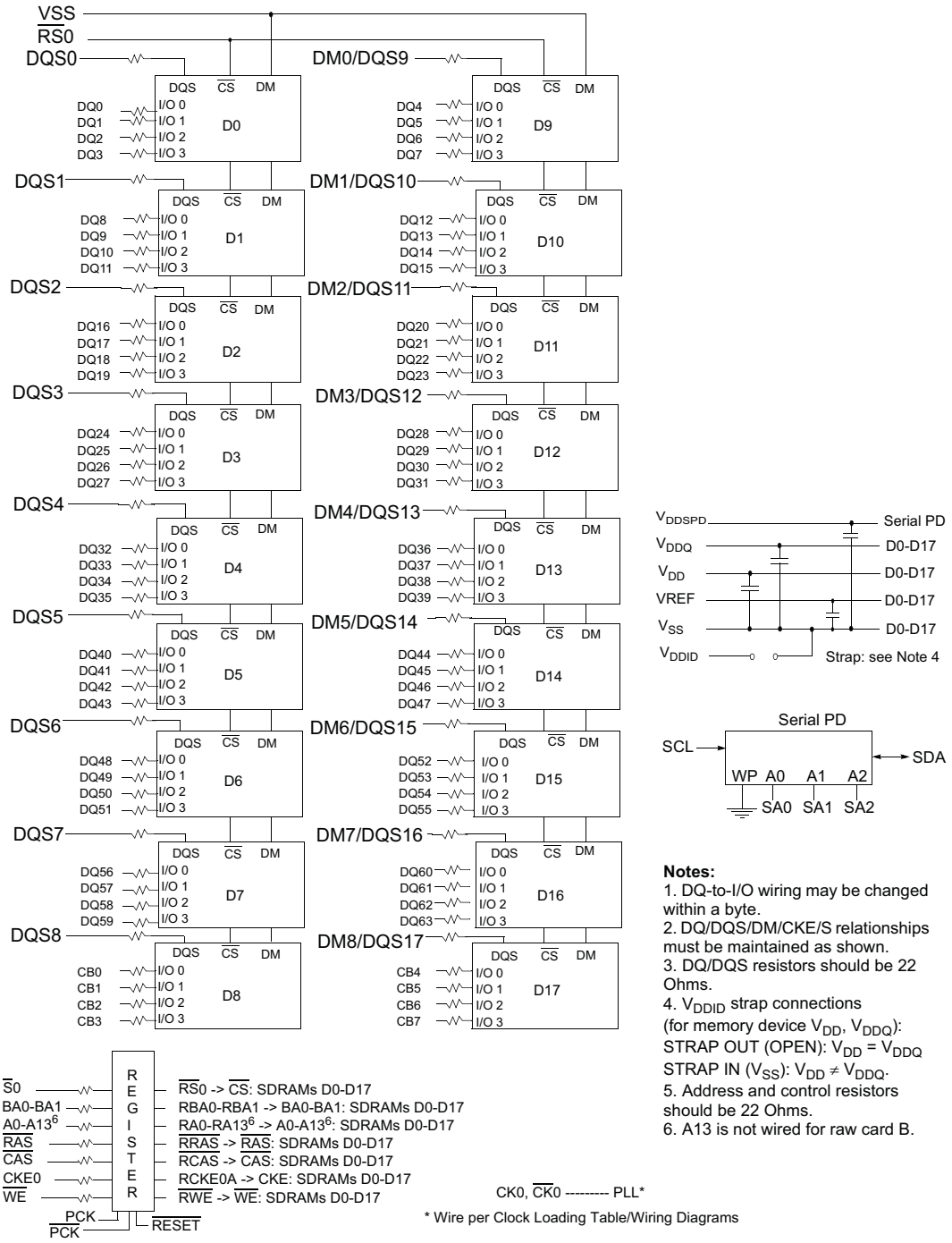



**Notes:**
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS/DM resistors should be 22 Ohms.
4. $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN ($V_{SS}$): $V_{DD} \neq V_{DDQ}$.
5. $\overline{RS0}$ and $\overline{RS1}$ alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.
7. A13 is not wired for raw card A.



Micron Technology Inc. et al.
Ex. 1017, p. 20

## Block Diagram: Raw Card Version B/M (Populated as one physical bank of x4 DDR SDRAMs)

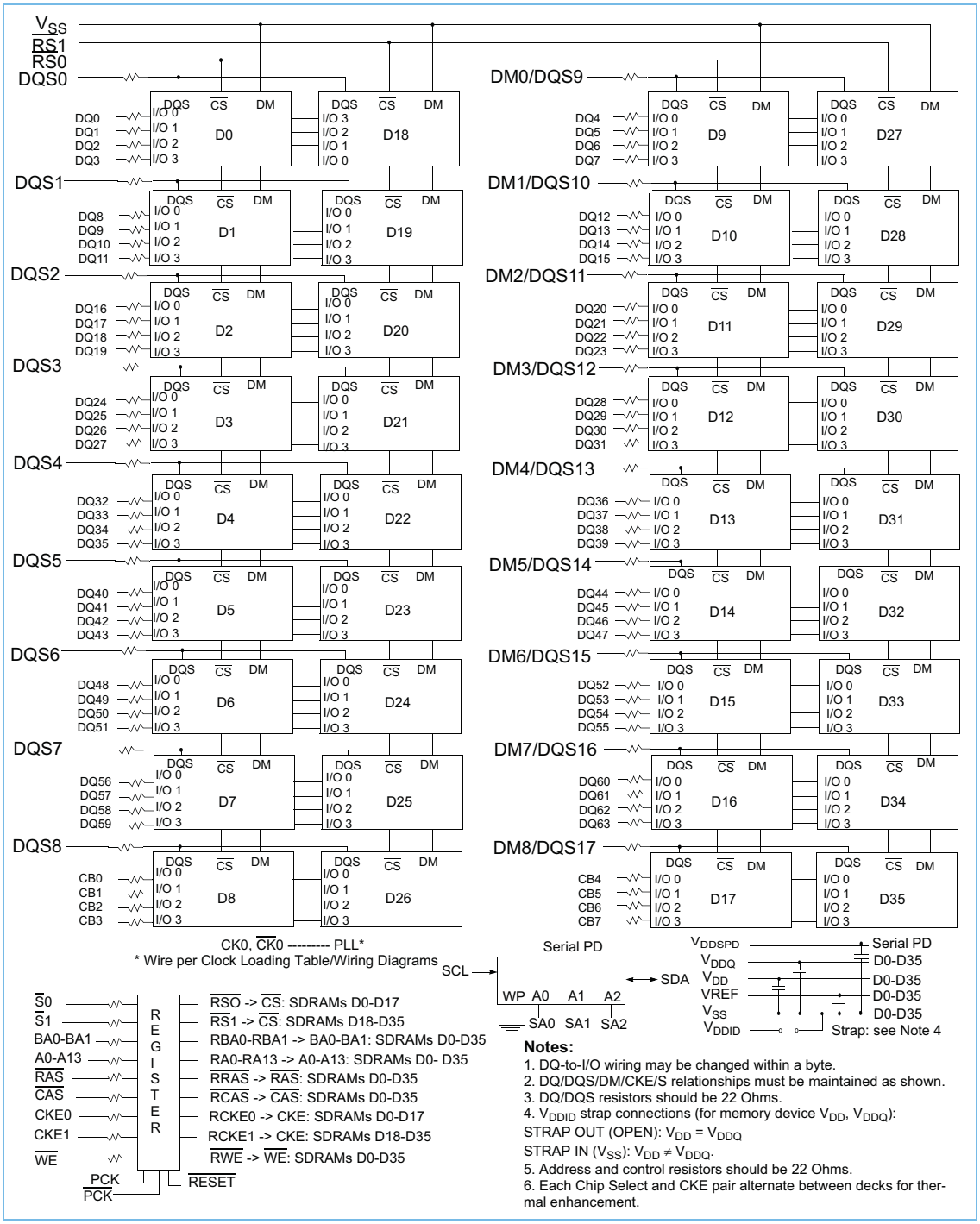



**Notes:**
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN ($V_{SS}$): $V_{DD} \neq V_{DDQ}$.
5. Address and control resistors should be 22 Ohms.
6. A13 is not wired for raw card B.



Micron Technology Inc. et al.
Ex. 1017, p. 21

## Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)

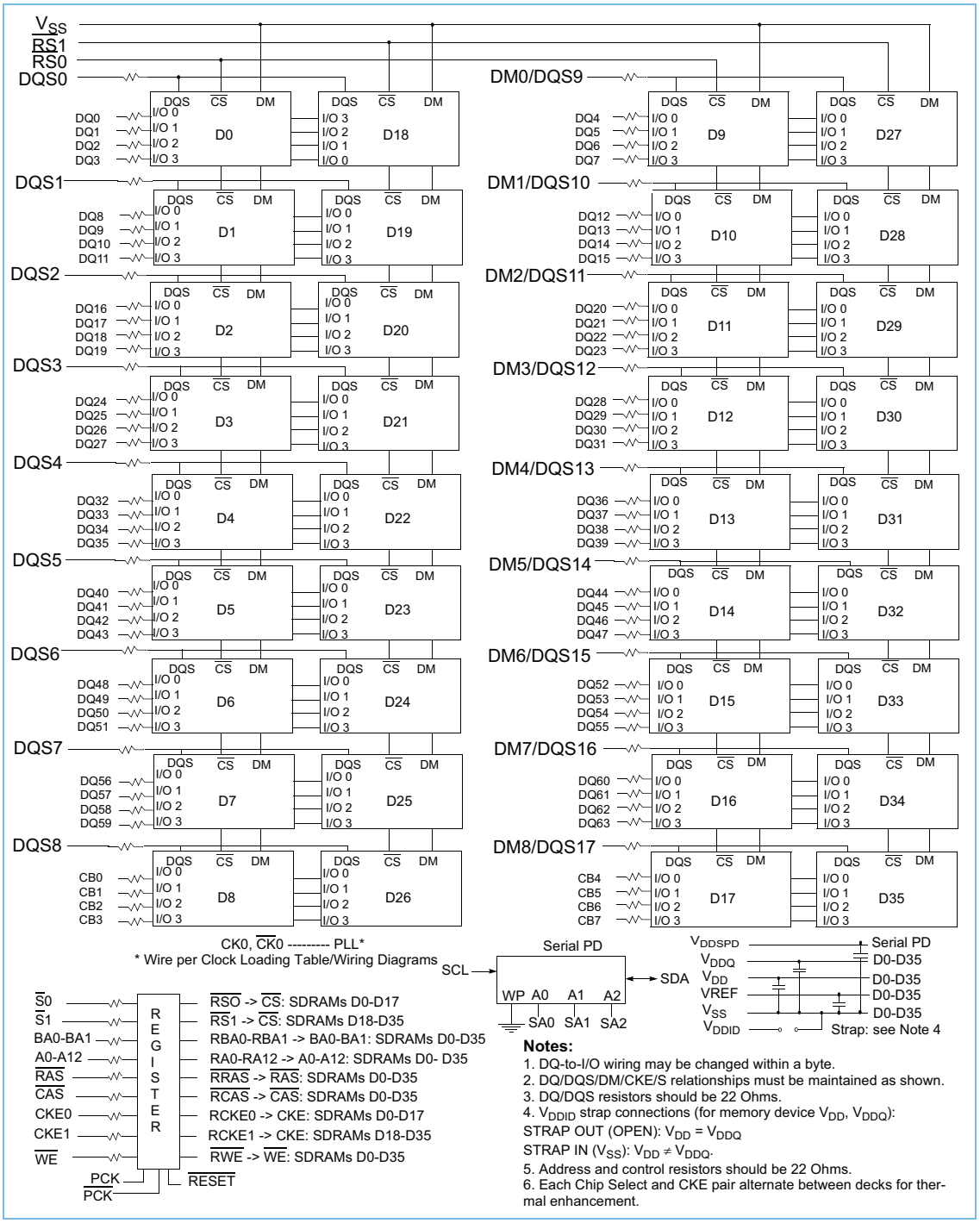



**Notes:**
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN ($V_{SS}$): $V_{DD} \neq V_{DDQ}$.
5. Address and control resistors should be 22 Ohms.
6. Each Chip Select and CKE pair alternate between decks for thermal enhancement.



Micron Technology Inc. et al.
Ex. 1017, p. 22

## Block Diagram: Raw Card Version C/E (Populated as two physical banks of x4 DDR SDRAMs)



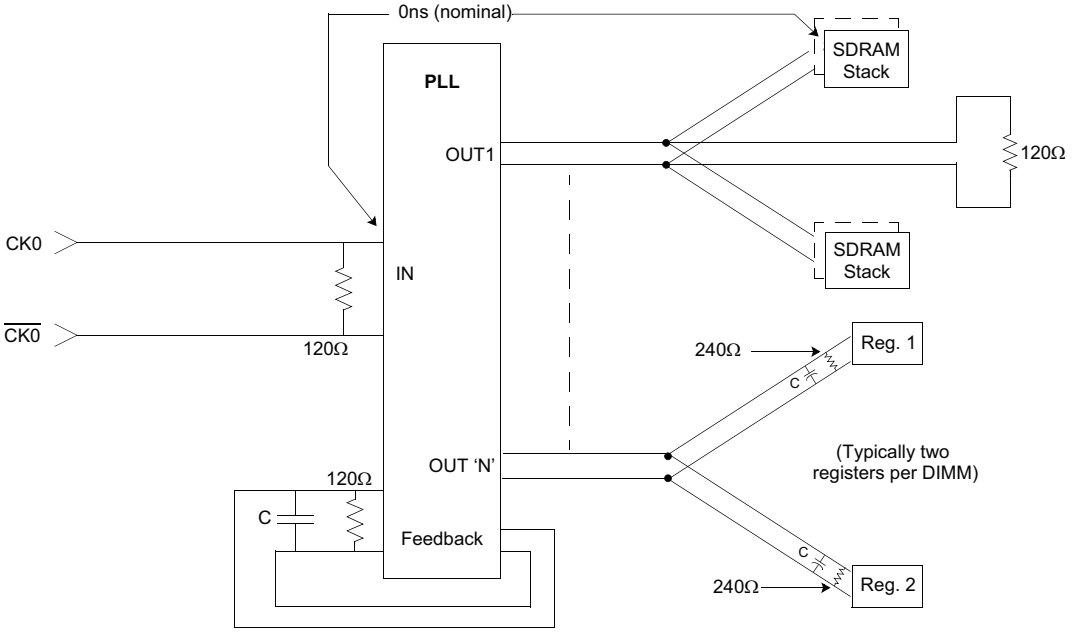

**Notes:**

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. $V_{DDID}$ strap connections (for memory device $V_{DD}$, $V_{DDQ}$):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN ($V_{SS}$): $V_{DD} \neq V_{DDQ}$.
5. Address and control resistors should be 22 Ohms.
6. Each Chip Select and CKE pair alternate between decks for thermal enhancement.



Micron Technology Inc. et al.
Ex. 1017, p. 23

## Differential Clock Net Wiring (CK0, $\overline{CK0}$)




1. The clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0ns (nominal). See “Clocking Timing Methodology” on page 74.
2. Input, output, and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for the PLL feedback path clocks are located as close to the input pin of the PLL as possible.



Micron Technology Inc. et al.
Ex. 1017, p. 24

## Register Functional Assignments

| Raw Card Versions A, B, and L (Two SSTV16857 1:1 Registers) | | | | Raw Card Versions C and E (Two SSTV16859 1:2 Registers) | | | |
|---|---|---|---|---|---|---|---|
| Register 1 | | Register 2 | | Register 1 | | Register 2 | |
| In | Out | In | Out | In | Out | In | Out |
| A1 | RA1 | A0 | RA0 | A1 | RA1A | A0 | RA0A |
| A2 | RA2 | A10 | RA10 | | RA1B | | RA0B |
| A3 | RA3 | $\overline{S}0$ | $\overline{RS}0$ | A2 | RA2A | A10 | RA10A |
| A4 | RA4 | $\overline{S}1$ | $\overline{RS}1$ | | RA2B | | RA10B |
| A5 | RA5 | $\overline{CAS}$ | $\overline{RCAS}$ | A3 | RA3A | $\overline{S}0$ | $\overline{RS}0$A |
| A6 | RA6 | $\overline{RAS}$ | $\overline{RRAS}$ | | RA3B | | $\overline{RS}0$B |
| A7 | RA7 | BA0 | RBA0 | A4 | RA4A | $\overline{S}1$ | $\overline{RS}1$A |
| A8 | RA8 | BA1 | RBA1 | | RA4B | | $\overline{RS}1$B |
| A9 | RA9 | $\overline{WE}$ | $\overline{RWE}$ | A5 | RA5A | $\overline{CAS}$ | $\overline{RCAS}$A |
| A11 | RA11 | | | | RA5B | | $\overline{RCAS}$B |
| A12[1] | RA12 | | | A6 | RA6A | $\overline{RAS}$ | $\overline{RRAS}$A |
| A13[2] | RA13 | | | | RA6B | | $\overline{RRAS}$B |
| CKE0 | RCKE0 | | | A7 | RA7A | BA0 | RBA0A |
| CKE1 | RCKE1 | | | | RA7B | | RBA0B |
| | | | | A8 | RA8A | BA1 | RBA1A |
| | | | | | RA8B | | RBA1B |
| | | | | A9 | RA9A | $\overline{WE}$ | $\overline{RWE}$A |
| | | | | | RA9B | | $\overline{RWE}$B |
| | | | | A11 | RA11A | | |
| | | | | | RA11B | | |
| | | | | A12[1] | RA12A | | |
| | | | | | RA12B | | |
| | | | | CKE0 | RCKE0A | | |
| | | | | | RCKE0B | | |
| | | | | CKE1 | RCKE1A | | |
| | | | | | RCKE1B | | |

1. Only used with 256Mbit, 512Mbit, 1Gbit DDR SDRAMs.
2. Only used with 1Gbit DDR SDRAMs.



Micron Technology Inc. et al.
Ex. 1017, p. 25

## Register Functional Assignments

| Raw Card Versions M (Two SSTV16857 1:1 Registers) | | | | Raw Card Versions N (One SSTV32852[3] 1:2 Registers) | | | |
|---|---|---|---|---|---|---|---|
| Register 1 | | Register 2 | | Register 1 | | | |
| In | Out | In | Out | In | Out | In | Out |
| A2 | RA2 | A0 | RA0 | A1 | RA1A | CKE0 | RCKE0A |
| A3 | RA3 | A1 | RA1 | | RA1B | | RCKE0B |
| A4 | RA4 | A10 | RA10 | A2 | RA2A | CKE1 | RCKE1A |
| A5 | RA5 | S0 | R$\overline{S}$0 | | RA2B | | RCKE1B |
| A6 | RA6 | $\overline{CAS}$ | R$\overline{CAS}$ | A3 | RA3A | A0 | RA0A |
| A7 | RA7 | $\overline{RAS}$ | R$\overline{RAS}$ | | RA3B | | RA0B |
| A8 | RA8 | BA0 | RBA0 | A4 | RA4A | A10 | RA10A |
| A9 | RA9 | BA1 | RBA1 | | RA4B | | RA10B |
| A11 | RA11 | $\overline{WE}$ | $\overline{RWE}$ | A5 | RA5A | $\overline{S}$0 | $\overline{RS0}$A |
| A12[1] | RA12 | | | | RA5B | | $\overline{RS0}$B |
| A13[2] | RA13 | | | A6 | RA6A | $\overline{S}$1 | $\overline{RS1}$A |
| CKE0 | RCKE0 | | | | RA6B | | $\overline{RS1}$B |
| | | | | A7 | RA7A | $\overline{CAS}$ | $\overline{RCAS}$A |
| | | | | | RA7B | | $\overline{RCAS}$B |
| | | | | A8 | RA8A | $\overline{RAS}$ | $\overline{RRAS}$A |
| | | | | | RA8B | | $\overline{RRAS}$B |
| | | | | A9 | RA9A | BA0 | RBA0A |
| | | | | | RA9B | | RBA0B |
| | | | | A11 | RA11A | BA1 | RBA1A |
| | | | | | RA11B | | RBA1B |
| | | | | A12[1] | RA12A | $\overline{WE}$ | $\overline{RWE}$A |
| | | | | | RA12B | | $\overline{RWE}$B |
| | | | | A13[2] | RA13A | | |
| | | | | | RA13B | | |
| | | | | | | | |
| | | | | | | | |

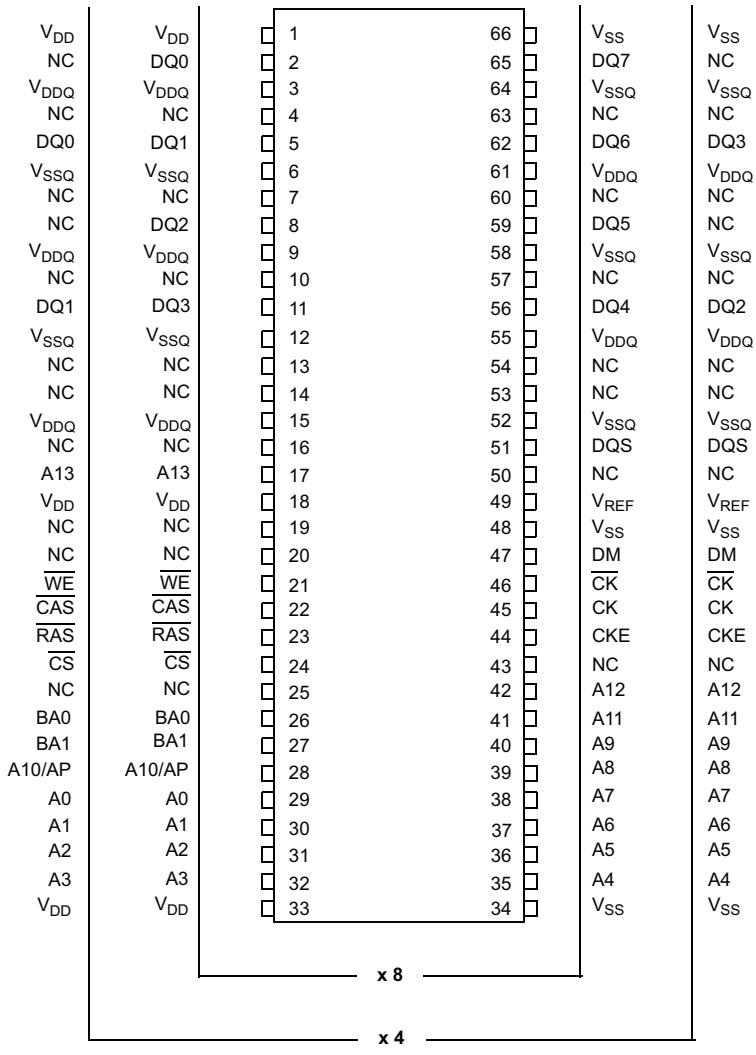
1. Only used with 256Mbit, 512Mbit, 1Gbit DDR SDRAMs.
2. Only used with 1Gbit DDR SDRAMs
3. Reference to the JC40 nomenclature and ballots for support chips (Registers and PLLs)



Micron Technology Inc. et al.
Ex. 1017, p. 26

# Component Details

## Pin Assignments for 64Mb, 128Mb, 256Mb, 512Mb and 1Gb DDR SDRAM Planar Components (Top View)



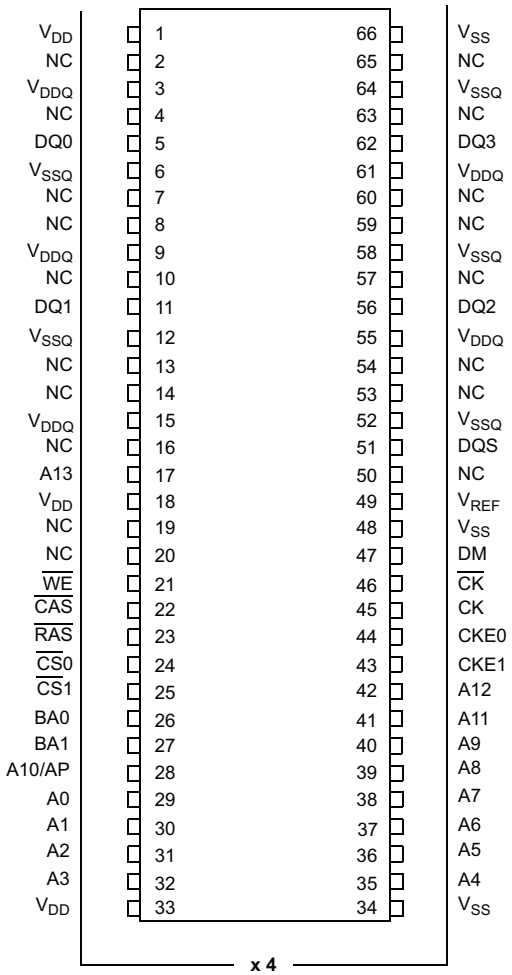

| | | | | | |
|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ | 1 | 66 | $V_{SS}$ | $V_{SS}$ |
| NC | DQ0 | 2 | 65 | DQ7 | NC |
| $V_{DDQ}$ | $V_{DDQ}$ | 3 | 64 | $V_{SSQ}$ | $V_{SSQ}$ |
| NC | NC | 4 | 63 | NC | NC |
| DQ0 | DQ1 | 5 | 62 | DQ6 | DQ3 |
| $V_{SSQ}$ | $V_{SSQ}$ | 6 | 61 | $V_{DDQ}$ | $V_{DDQ}$ |
| NC | NC | 7 | 60 | NC | NC |
| NC | DQ2 | 8 | 59 | DQ5 | NC |
| $V_{DDQ}$ | $V_{DDQ}$ | 9 | 58 | $V_{SSQ}$ | $V_{SSQ}$ |
| NC | NC | 10 | 57 | NC | NC |
| DQ1 | DQ3 | 11 | 56 | DQ4 | DQ2 |
| $V_{SSQ}$ | $V_{SSQ}$ | 12 | 55 | $V_{DDQ}$ | $V_{DDQ}$ |
| NC | NC | 13 | 54 | NC | NC |
| NC | NC | 14 | 53 | NC | NC |
| $V_{DDQ}$ | $V_{DDQ}$ | 15 | 52 | $V_{SSQ}$ | $V_{SSQ}$ |
| NC | NC | 16 | 51 | DQS | DQS |
| A13 | A13 | 17 | 50 | NC | NC |
| $V_{DD}$ | $V_{DD}$ | 18 | 49 | $V_{REF}$ | $V_{REF}$ |
| NC | NC | 19 | 48 | $V_{SS}$ | $V_{SS}$ |
| NC | NC | 20 | 47 | DM | DM |
| $\overline{WE}$ | $\overline{WE}$ | 21 | 46 | $\overline{CK}$ | $\overline{CK}$ |
| $\overline{CAS}$ | $\overline{CAS}$ | 22 | 45 | CK | CK |
| $\overline{RAS}$ | $\overline{RAS}$ | 23 | 44 | CKE | CKE |
| $\overline{CS}$ | $\overline{CS}$ | 24 | 43 | NC | NC |
| NC | NC | 25 | 42 | A12 | A12 |
| BA0 | BA0 | 26 | 41 | A11 | A11 |
| BA1 | BA1 | 27 | 40 | A9 | A9 |
| A10/AP | A10/AP | 28 | 39 | A8 | A8 |
| A0 | A0 | 29 | 38 | A7 | A7 |
| A1 | A1 | 30 | 37 | A6 | A6 |
| A2 | A2 | 31 | 36 | A5 | A5 |
| A3 | A3 | 32 | 35 | A4 | A4 |
| $V_{DD}$ | $V_{DD}$ | 33 | 34 | $V_{SS}$ | $V_{SS}$ |

Note: This pin assignment is for use with planar DIMMs.



Micron Technology Inc. et al.
Ex. 1017, p. 27

## Pin Assignments for 64Mb, 128Mb, 256Mb, 512Mb and 1Gb DDR SDRAM 2-High Stack Package (Top View)




Note: This pin assignment is for use with stacked DIMMs.

## DDR SDRAM Component Specifications

The DDR SDRAM components used with this DIMM design specification are intended to be consistent with JEDEC standard JESD79. DDR SDRAM component specification violations also violate the DDR SDRAM Registered DIMM specifications.



Micron Technology Inc. et al.
Ex. 1017, p. 28

## Register Component Specifications

Please refer to the vendor register data sheets for all technical specifications and requirements. Below is a chart explaining which registers should be used on each DIMM type.

## DIMM Register Use

| Raw Card Version | # of Banks | # of SDRAMs per output | Register Type | Package | Quantity |
|---|---|---|---|---|---|
| A/L | 1 | 9 | SSTV16857 (1:1 14-bit SSTL) | TSSOP | 2 |
| | 2 | 18 | SSTV16857 (1:1 14-bit SSTL) | TSSOP | 2 |
| B/M | 1 | 18 | SSTV16857 (1:1 14-bit SSTL) | TSSOP | 2 |
| N | 2 | 18 | SSTV32852 (1:2 24-bit SSTL) | BGA | 1 |
| C/E | 2 | 18 | SSTV16859 (1:2 13-bit SSTL) | TSSOP | 2 |

The following specifications for the register are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the device. Detailed information on both the 1:1 and 1:2 registers, including driver characteristics, has been standardized at the JEDEC JC-40 Committee, as SSTV16857 (1:1), SSTV16859 (1:2) and SSTV32852(1:2).

## Critical Register Specifications

| Register | Symbol | Parameter | Conditions | $T_A$ = 0-70° C, $V_{DD}$ = 2.5V ± 0.2V | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SSTV16857 (1:1 14-bit) and SSTV16859 (1:2 13-bit) and SSTV32852 (1:2 24-bit) | $t_{CK}$ | Clock Frequency | | 60 | 170 | MHz | |
| | $t_{PD}$ | Clock to Output Time | 30pF to GND and 50 Ohms to $V_{TT}$ | 1.1 | 2.8 | ns | 4 |
| | $t_{RST}$ | Reset to Output Time | | — | 5 | ns | |
| | $t_{SL}$ | Output Slew Rate | 30pF to GND and 50 Ohms to $V_{TT}/2$ | 0.5 | 4 | V/ns | |
| | $t_{su}$ | Setup time, fast slew rate (see Notes 1 and 3) | | 0.75 | — | ns | 1, 3 |
| | | Setup time, slow slew rate (see Notes 2 and 3) | | 0.9 | — | ns | 2, 3 |
| | $t_h$ | Hold time, fast slew rate (see Notes 1 and 3) | | 0.75 | — | | 1, 3 |
| | | Hold time, slow slew rate (see Notes 2 and 3) | | 0.9 | — | | 2, 3 |
| | $C_{IN(CK)}$ | Clock Input Capacitance | | 2.5 | 3.5 | pF | |
| | $C_{IN(data)}$ | Data Input Capacitance | | 2.5 | 3.5 | pF | |

1. For data signal, input slew rate ≥ 1 V/ns.
2. For data signal, input slew rate ≥ 0.5 V/ns and < 1V/ns.
3. For CLK and $\overline{CLK}$ signals, input slew rates are ≥ 1 V/ns.
4. For the SSTV32852, $t_{PD}$ is 3.1ns max



Micron Technology Inc. et al.
Ex. 1017, p. 29

## Register Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all DDR SDRAM RDIMM registers meet the specifications documented above, it is up to each DIMM producer to select the registers and register vendors which meet these requirements, and to guarantee robustly designed DIMMs. In order to facilitate industry consistency, the functionality and technical requirements of both the 1:1 and 1:2 registers have been standardized at JEDEC in JC-40, as SSTV16857 (1:1), SSTV16859 (1:2) and SSTV32852(1:2).

## PLL Component Specifications

Please refer to the vendor PLL data sheets for all technical specifications and requirements. Below is a chart explaining which PLLs are used on each DIMM type.

## DIMM PLL Use

| Raw Card Version | # of Banks | # of SDRAMs per output | PLL Type | Package | Quantity |
|---|---|---|---|---|---|
| A/L | 1 | 2[1] | CDCV857 (1:10, 2.5 Volt) | TSSOP | 1 |
| | 2 | 2 | CDCV857 (1:10, 2.5 Volt) | TSSOP | 1 |
| B/M | 1 | 2 | CDCV857 (1:10, 2.5 Volt) | TSSOP | 1 |
| N | 2 | 4 | CDCV857 (1:10, 2.5 Volt) | TSSOP | 1 |
| C/E | 2 | 4 | CDCV857 (1:10, 2.5 Volt) | TSSOP | 1 |

1. In the case of the One-Bank A/L Card, a padding capacitor is added across each SDRAM clock and $\overline{\text{clock}}$ pair to ensure that timing is the same for One and Two-Bank DIMMs. Also, on X64 A cards, a padding capacitor is used across the clock pair for the depopulated ninth SDRAM(s) position(s).

The following specifications for the PLL are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the device. Detailed information on this part, including driver characteristics, has been standardized at the JEDEC JC-40 Committee, as CDCV857 (Item #25).



Micron Technology Inc. et al.
Ex. 1017, p. 30

## Critical PLL Specifications

| Device | Symbol | Parameter | Conditions | $T_A$ = 0-70° C, $V_{DD}$ = 2.5V ± 0.2V | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| CDCV857 (1:10, 2.5 Volt) | $f_{CK}$ | Operating Clock Frequency | | 60 | 170 | MHz | 1 |
| | $f_{CK}$ | Application Clock Frequency | | 95 | 170 | MHz | 1 |
| | $t_{SPE}$ | Static Phase Error | Application Load | -50 | 50 | ps | 2 |
| | $t_{SK}$ | Output Clock Skew | Application Load | — | 100 | ps | 2 |
| | $t_{SL}$ | Output Slew Rate | | 1 | 3 | V/ns | 2 |
| | $t_{jit}$(per) | Period | | -75 | 75 | ps | 3, 4 |
| | $t_{jit}$(cc) | Cycle-to-Cycle | | | | | |
| | $t_{jit}$(hper) | Half-period | | -100 | 100 | | 4 |
| | $t_{STAB}$ | PLL Stabilization Time | | | 100 | µs | |
| | $C_{IN}$ | Input Capacitance | | 2.5 | 3.5 | pF | |

1. The PLL used on the registered DIMM needs to support SSC synthesizers with a Modulation Frequency of 30 to 50KHz and a Clock Frequency Deviation of -0.5%. PLL designs should target the following values:
   - Greater than 2MHz PLL loop bandwidth
   - Less than -0.031 degrees of phase angle
2. The application load is defined in *Differential Clock Net Structures* on page 38.
3. Period jitter defines the largest variation in clock period, around a nominal clock period.
4. Period jitter and half-period jitter are independent from each other.

## PLL Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all DDR SDRAM Registered DIMM PLLs meet the specifications documented above, it is up to each DIMM producer to select the PLL and PLL vendors which meet these requirements, and to guarantee robustly operating DIMMs. In order to facilitate industry consistency, the functionality and technical requirements of this part have been standardized at JEDEC in JC-40, as CDCV857 (Item #25).



Micron Technology Inc. et al.
Ex. 1017, p. 31

## Registered DIMM Details

### DDR SDRAM Module Configurations (Reference Designs) (Part 1 of 3)

| Raw Card Version | DIMM | | SDRAM | | # of SDRAMs | SDRAM Package Type | # of Physical Banks | # of Banks in SDRAM | # of Address bits row/col | FET Switch |
|---|---|---|---|---|---|---|---|---|---|---|
| | Capacity | Organization | Density | Organization | | | | | | |
| A | 64MB | 8Mx72 | 64Mbit | 8Mx8 | 9 | 66 lead TSOP | 1 | 4 | 12/9 | No |
| | 128MB | 16Mx72 | 128Mbit | 16Mx8 | 9 | 66 lead TSOP | 1 | 4 | 12/10 | No |
| | 256MB | 32Mx72 | 256Mbit | 32Mx8 | 9 | 66 lead TSOP | 1 | 4 | 13/10 | No |
| | 512MB | 64Mx72 | 512Mbit | 64Mx8 | 9 | 66 lead TSOP | 1 | 4 | 13/11 | No |
| | 128MB | 16Mx72 | 64Mbit | 8Mx8 | 18 | 66 lead TSOP | 2 | 4 | 12/9 | No |
| | 256MB | 32Mx72 | 128Mbit | 16Mx8 | 18 | 66 lead TSOP | 2 | 4 | 12/10 | No |
| | 512MB | 64Mx72 | 256Mbit | 32Mx8 | 18 | 66 lead TSOP | 2 | 4 | 13/10 | No |
| | 1GB | 128Mx72 | 512Mbit | 64Mx8 | 18 | 66 lead TSOP | 2 | 4 | 13/11 | No |
| | 64MB | 8Mx64 | 64Mbit | 8Mx8 | 8 | 66 lead TSOP | 1 | 4 | 12/9 | No |
| | 128MB | 16Mx64 | 128Mbit | 16Mx8 | 8 | 66 lead TSOP | 1 | 4 | 12/10 | No |
| | 256MB | 32Mx64 | 256Mbit | 32Mx8 | 8 | 66 lead TSOP | 1 | 4 | 13/10 | No |
| | 512MB | 64Mx64 | 512Mbit | 64Mx8 | 8 | 66 lead TSOP | 1 | 4 | 13/11 | No |
| | 128MB | 16Mx64 | 64Mbit | 8Mx8 | 16 | 66 lead TSOP | 2 | 4 | 12/9 | No |
| | 256MB | 32Mx64 | 128Mbit | 16Mx8 | 16 | 66 lead TSOP | 2 | 4 | 12/10 | No |
| | 512MB | 64Mx64 | 256Mbit | 32Mx8 | 16 | 66 lead TSOP | 2 | 4 | 13/10 | No |
| | 1GB | 128Mx64 | 512Mbit | 64Mx8 | 16 | 66 lead TSOP | 2 | 4 | 13/11 | No |



Micron Technology Inc. et al.
Ex. 1017, p. 32

## DDR SDRAM Module Configurations (Reference Designs) (Part 2 of 3)

| Raw Card Version | DIMM | | SDRAM | | # of SDRAMs | SDRAM Package Type | # of Physical Banks | # of Banks in SDRAM | # of Address bits row/col | FET Switch |
|---|---|---|---|---|---|---|---|---|---|---|
| | Capacity | Organization | Density | Organization | | | | | | |
| L | 64MB | 8Mx72 | 64Mbit | 8Mx8 | 9 | 66 lead TSOP | 1 | 4 | 12/9 | No |
| | 128MB | 16Mx72 | 128Mbit | 16Mx8 | 9 | 66 lead TSOP | 1 | 4 | 12/10 | No |
| | 256MB | 32Mx72 | 256Mbit | 32Mx8 | 9 | 66 lead TSOP | 1 | 4 | 13/10 | No |
| | 512MB | 64Mx72 | 512Mbit | 64Mx8 | 9 | 66 lead TSOP | 1 | 4 | 13/11 | No |
| | 1GB | 128Mx72 | 1Gb | 128Mx8 | 9 | 66 lead TSOP | 1 | 4 | 14/11 | No |
| | 128MB | 16Mx72 | 64Mbit | 8Mx8 | 18 | 66 lead TSOP | 2 | 4 | 12/9 | No |
| | 256MB | 32Mx72 | 128Mbit | 16Mx8 | 18 | 66 lead TSOP | 2 | 4 | 12/10 | No |
| | 512MB | 64Mx72 | 256Mbit | 32Mx8 | 18 | 66 lead TSOP | 2 | 4 | 13/10 | No |
| | 1GB | 128Mx72 | 512Mbit | 64Mx8 | 18 | 66 lead TSOP | 2 | 4 | 13/11 | No |
| | 2GB | 256Mx72 | 1Gb | 128Mx8 | 18 | 66 lead TSOP | 2 | 4 | 14/11 | No |
| | 64MB | 8Mx64 | 64Mbit | 8Mx8 | 8 | 66 lead TSOP | 1 | 4 | 12/9 | No |
| | 128MB | 16Mx64 | 128Mbit | 16Mx8 | 8 | 66 lead TSOP | 1 | 4 | 12/10 | No |
| | 256MB | 32Mx64 | 256Mbit | 32Mx8 | 8 | 66 lead TSOP | 1 | 4 | 13/10 | No |
| | 512MB | 64Mx64 | 512Mbit | 64Mx8 | 8 | 66 lead TSOP | 1 | 4 | 13/11 | No |
| | 1GB | 128Mx64 | 1Gb | 128Mx8 | 8 | 66 lead TSOP | 1 | 4 | 14/11 | No |
| | 128MB | 16Mx64 | 64Mbit | 8Mx8 | 16 | 66 lead TSOP | 2 | 4 | 12/9 | No |
| | 256MB | 32Mx64 | 128Mbit | 16Mx8 | 16 | 66 lead TSOP | 2 | 4 | 12/10 | No |
| | 512MB | 64Mx64 | 256Mbit | 32Mx8 | 16 | 66 lead TSOP | 2 | 4 | 13/10 | No |
| | 1GB | 128Mx64 | 512Mbit | 64Mx8 | 16 | 66 lead TSOP | 2 | 4 | 13/11 | No |
| | 2GB | 256Mx64 | 1Gb | 128Mx8 | 16 | 66 lead TSOP | 2 | 4 | 14/11 | No |
| B | 128MB | 16Mx72 | 64Mbit | 16Mx4 | 18 | 66 lead TSOP | 1 | 4 | 12/10 | No |
| | 256MB | 32Mx72 | 128Mbit | 32Mx4 | 18 | 66 lead TSOP | 1 | 4 | 12/11 | No |
| | 512MB | 64Mx72 | 256Mbit | 64Mx4 | 18 | 66 lead TSOP | 1 | 4 | 13/11 | No |
| | 1GB | 128Mx72 | 512Mbit | 128Mx4 | 18 | 66 lead TSOP | 1 | 4 | 13/12 | No |
| M | 128MB | 16Mx72 | 64Mbit | 16Mx4 | 18 | 66 lead TSOP | 1 | 4 | 12/10 | No |
| | 256MB | 32Mx72 | 128Mbit | 32Mx4 | 18 | 66 lead TSOP | 1 | 4 | 12/11 | No |
| | 512MB | 64Mx72 | 256Mbit | 64Mx4 | 18 | 66 lead TSOP | 1 | 4 | 13/11 | No |
| | 1GB | 128Mx72 | 512Mbit | 128Mx4 | 18 | 66 lead TSOP | 1 | 4 | 13/12 | No |
| | 2GB | 256Mx72 | 1Gb | 256Mx4 | 18 | 66 lead TSOP | 1 | 4 | 14/12 | No |
| C | 256MB | 32Mx72 | 64Mbit | 16Mx4 | 36 | 66 lead stacked TSOP | 2 | 4 | 12/10 | No |
| | 512MB | 64Mx72 | 128Mbit | 32Mx4 | 36 | 66 lead stacked TSOP | 2 | 4 | 12/11 | No |
| | 1GB | 128Mx72 | 256Mbit | 64Mx4 | 36 | 66 lead stacked TSOP | 2 | 4 | 13/11 | No |
| | 2GB | 256Mx72 | 512Mbit | 128Mx4 | 36 | 66 lead stacked TSOP | 2 | 4 | 13/12 | No |



Micron Technology Inc. et al.
Ex. 1017, p. 33

## DDR SDRAM Module Configurations (Reference Designs) (Part 3 of 3)

| Raw Card Version | DIMM | | SDRAM | | # of SDRAMs | SDRAM Package Type | # of Physical Banks | # of Banks in SDRAM | # of Address bits row/col | FET Switch |
|---|---|---|---|---|---|---|---|---|---|---|
| | Capacity | Organization | Density | Organization | | | | | | |
| N | 256MB | 32Mx72 | 64Mbit | 16Mx4 | 36 | 66 lead stacked TSOP | 2 | 4 | 12/10 | No |
| | 512MB | 64Mx72 | 128Mbit | 32Mx4 | 36 | 66 lead stacked TSOP | 2 | 4 | 12/11 | No |
| | 1GB | 128Mx72 | 256Mbit | 64Mx4 | 36 | 66 lead stacked TSOP | 2 | 4 | 13/11 | No |
| | 2GB | 256Mx72 | 512Mbit | 128Mx4 | 36 | 66 lead stacked TSOP | 2 | 4 | 13/12 | No |
| | 4GB | 512Mx72 | 1Gb | 256Mx4 | 36 | 66 lead stacked TSOP | 2 | 4 | 14/12 | No |
| E | 256MB | 32Mx72 | 64Mbit | 16Mx4 | 36 | 66 lead stacked TSOJ | 2 | 4 | 12/10 | No |
| | 512MB | 64Mx72 | 128Mbit | 32Mx4 | 36 | 66 lead stacked TSOJ | 2 | 4 | 12/11 | No |
| | 1GB | 128Mx72 | 256Mbit | 64Mx4 | 36 | 66 lead stacked TSOJ | 2 | 4 | 13/11 | No |
| | 2GB | 256Mx72 | 512Mbit | 128Mx4 | 36 | 66 lead stacked TSOJ | 2 | 4 | 13/12 | No |



Micron Technology Inc. et al.
Ex. 1017, p. 34

## Input Loading Matrix

| Signal Names | Input Device | Raw Card Version | | |
|---|---|---|---|---|
| | | A/L | B/M | C/E/N |
| Clock (CK0) | PLL | 1 | 1 | 1 |
| CKE0 | Register | 1 | 1 | 1 |
| CKE1 | Register | 1 or 0 | N/A | 1 |
| Addr/RAS/CAS/BA/WE | Register | 1 | 1 | 1 |
| Chip Selects | Register | 1 | 1 | 1 |
| DQ/DQS | DDR SDRAM | 1 or 2 | 1 | 2 |
| DM | DDR SDRAM | 1 or 2 | N/A | N/A |
| SCL/SDA/SA | EEPROM | 1 | 1 | 1 |

## DDR Registered Design File Releases

'Reference' Design file updates will be released as needed. This Registered DIMM specification will reflect the most recent Design files, but may also be updated to reflect clarifications to the specification only; in these cases the Design files will not be updated. The following table outlines the most recent Design file releases.

**Note:** Future Design file releases will include both a date and a revision label. All changes to the Design file are also documented in detail within the 'read-me' file.

| Raw Card Version | Specification Revision | Applicable Design File | Notes |
|---|---|---|---|
| A | 0.6 | A0 | Release on 12/15/99 |
| | 1.0 | A1 | Release on 03/31/00 |
| B | 0.6 | B1 | Release on 11/26/99 |
| | 1.0 | B2 | Release on 03/31/00 |
| C | 0.9[1] | C1 | Release on 02/25/00 |
| | 0.95 (JEDEC ballot) | C2[2] | Release on 06/23/00 |
| | 1.0 | C3[2] | Release on 08/01/00 |
| E | 1.0 | TBD | Original Release |
| L | 1.2 | 1.0 | Release on 10/05/01 |
| M | 1.2 | 1.0 | Release on 10/05/01 |
| N | 1.3 | N0 | Release on 11/30/01 |

1. With exception of the cross section which utilized Revision 0.6.
2. The C2 release is missing the gnd via connection for impedance coupons. The C3 release corrects this error. This omission has no bearing on the use of this design level in system applications.



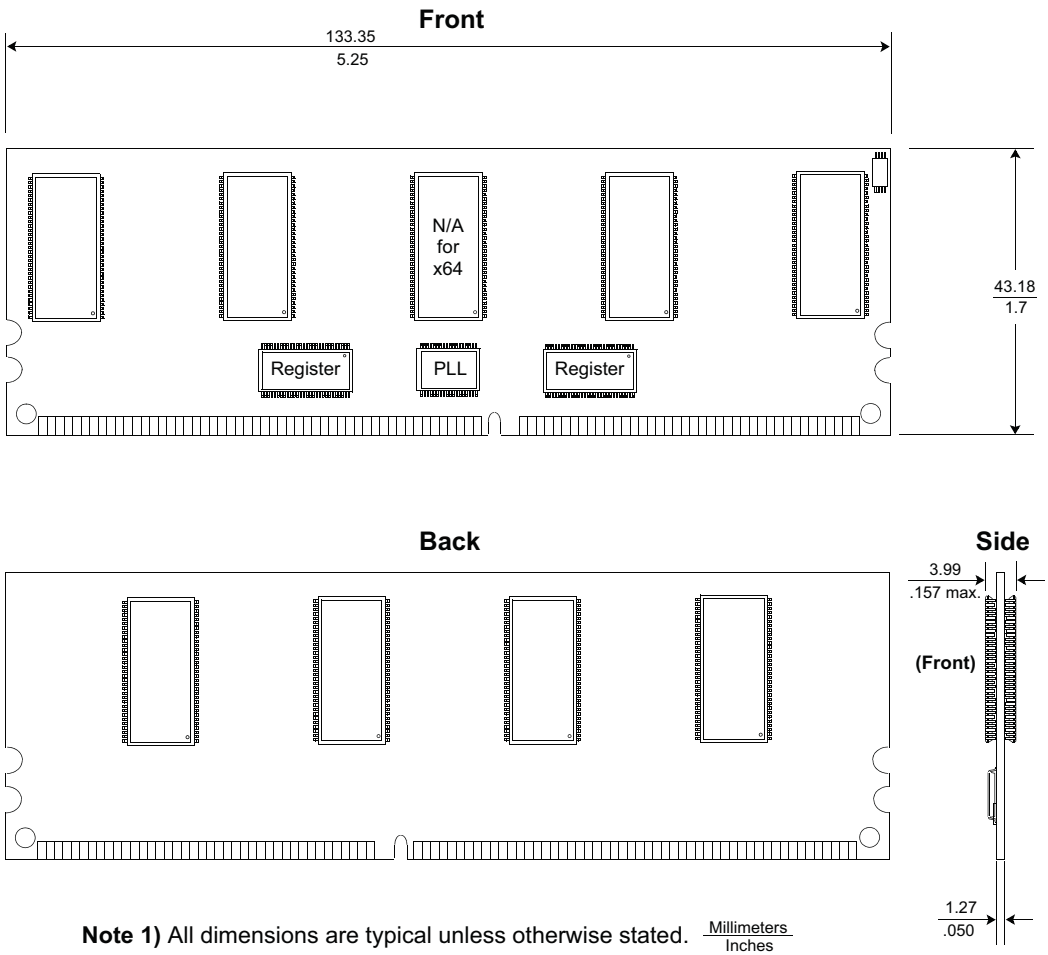
Micron Technology Inc. et al.
Ex. 1017, p. 35

### Component Types and Placement

Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors for DDR SDRAM devices must be located near the device power pins. In two-bank, x4 based DDR SDRAM designs, the second DDR SDRAM bank devices will be stacked on the first DDR SDRAM bank devices.

The following layouts suggest placement for the Raw Card Versions A, B, C, E, L,M and N. Exact spacing is not provided, but should be based on manufacturing constraints and signal routing constraints imposed by this design guide.

## Example Raw Card Versions A (1 Physical Bank) Component Placement



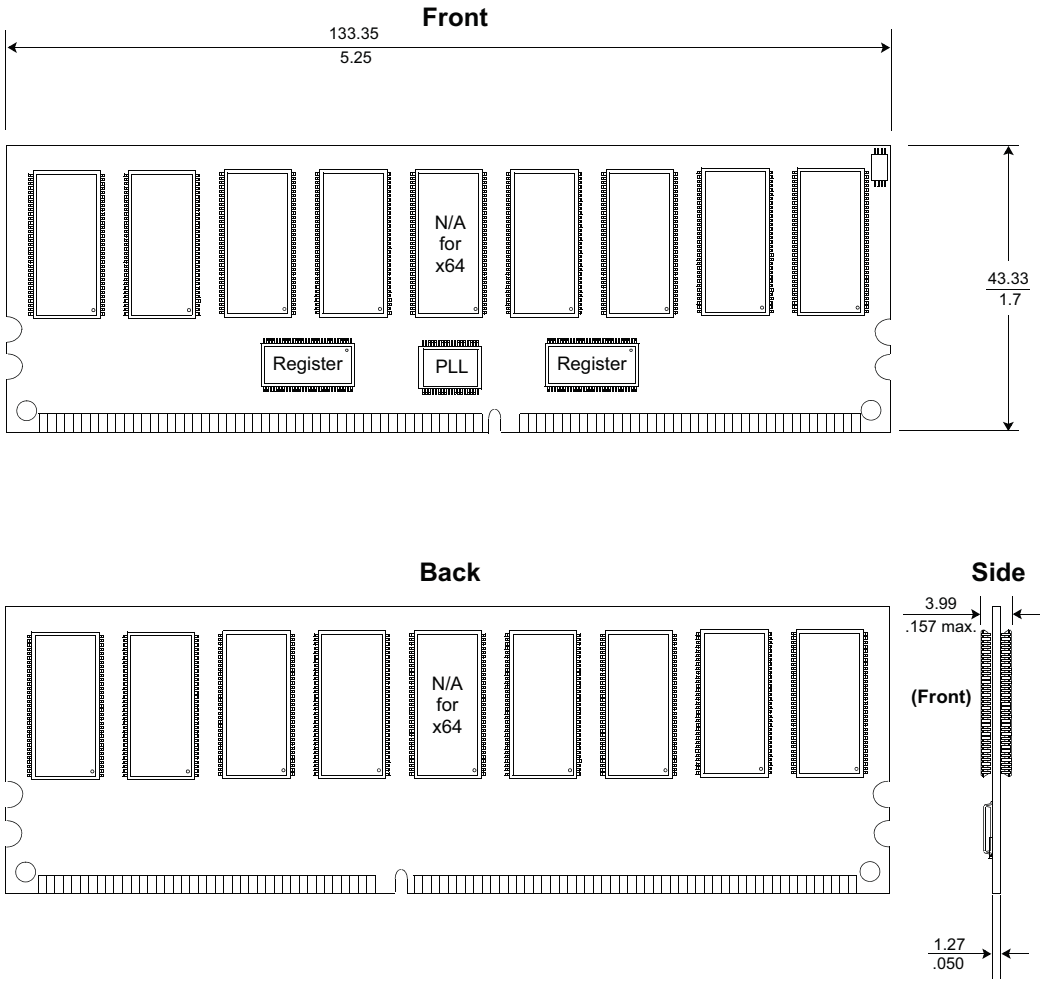

**Note 1)** All dimensions are typical unless otherwise stated. Millimeters / Inches

**Note 2)** All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.



Micron Technology Inc. et al.
Ex. 1017, p. 36

## Example Raw Card Versions A (2 Physical Banks) Component Placement



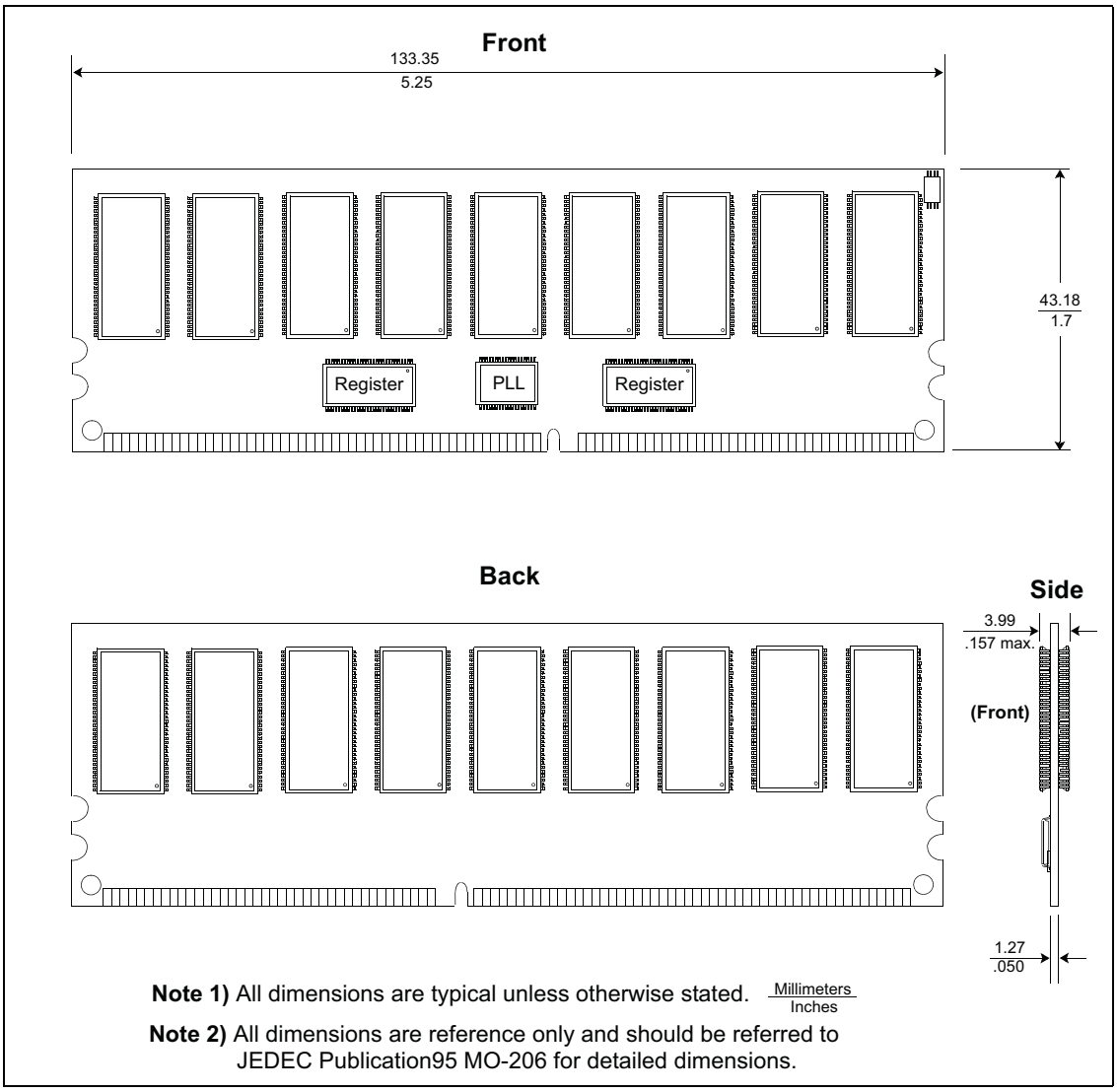

**Note 1)** All dimensions are typical unless otherwise stated. Millimeters / Inches

**Note 2)** All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.



Micron Technology Inc. et al.
Ex. 1017, p. 37

## Example Raw Card Version B Component Placement



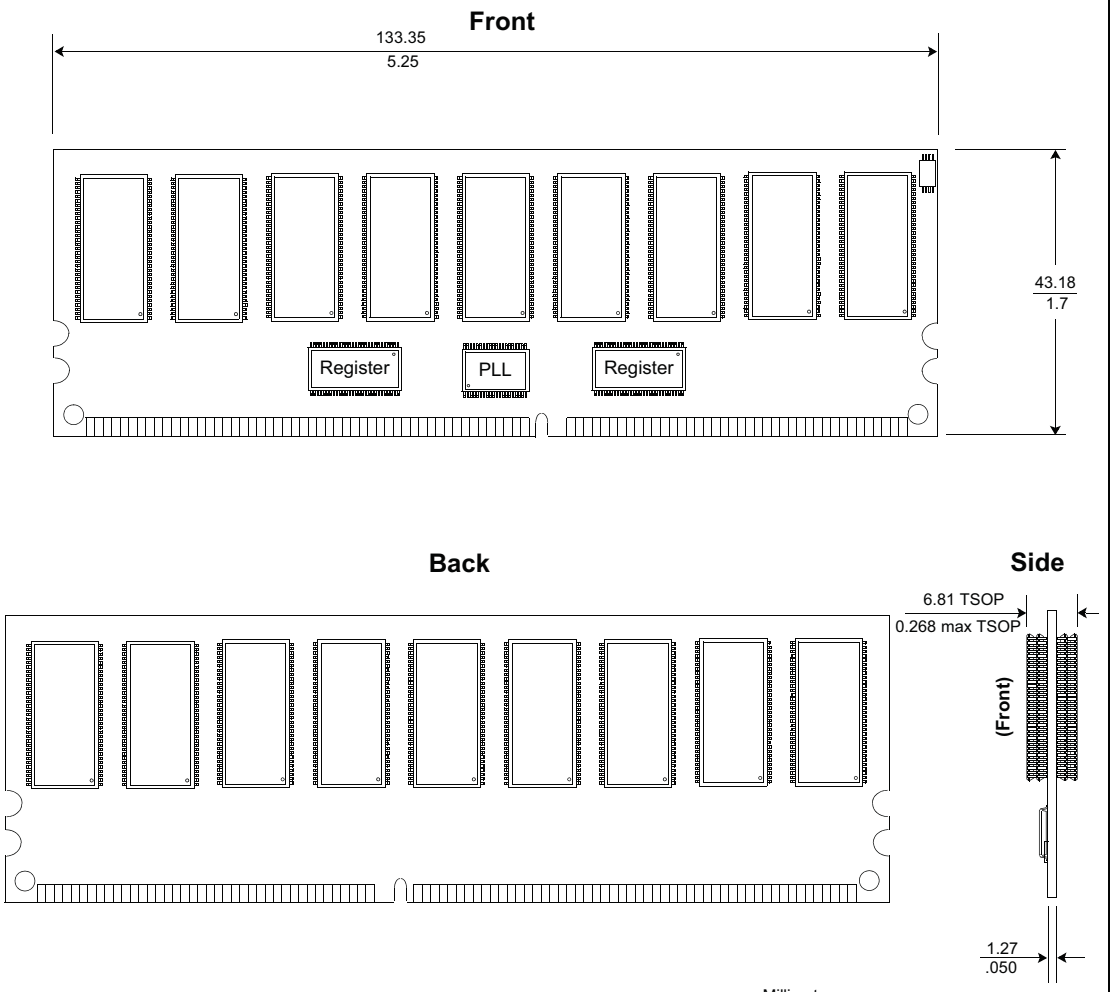

**Note 1)** All dimensions are typical unless otherwise stated. Millimeters / Inches

**Note 2)** All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.



Micron Technology Inc. et al.
Ex. 1017, p. 38

## Example Raw Card Version C/E Component Placement



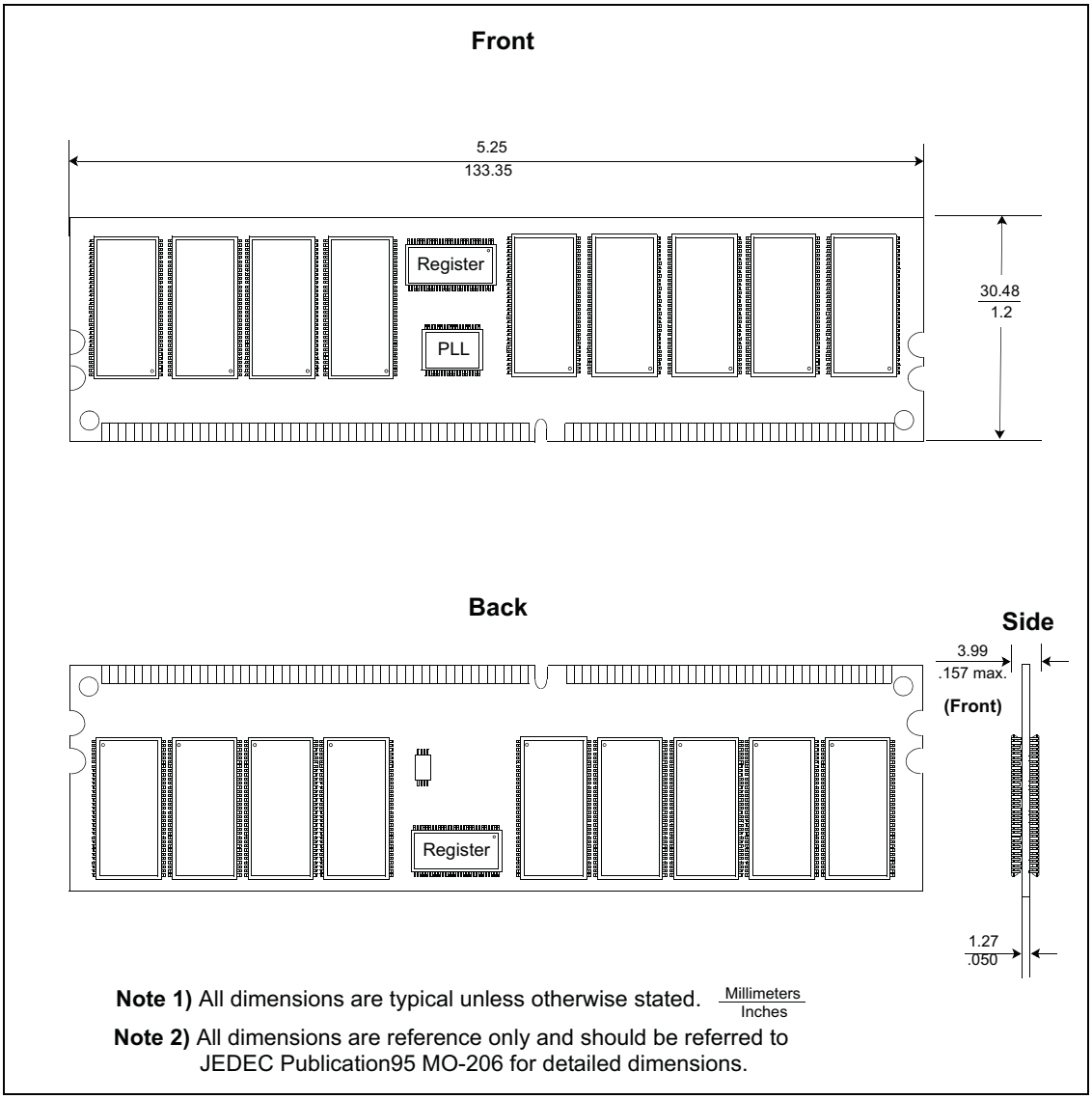

**Note 1)** All dimensions are typical unless otherwise stated. Millimeters / Inches

**Note 2)** All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.



Micron Technology Inc. et al.
Ex. 1017, p. 39

## Example Raw Card Versions L (2 Physical Banks) and M Component Placement



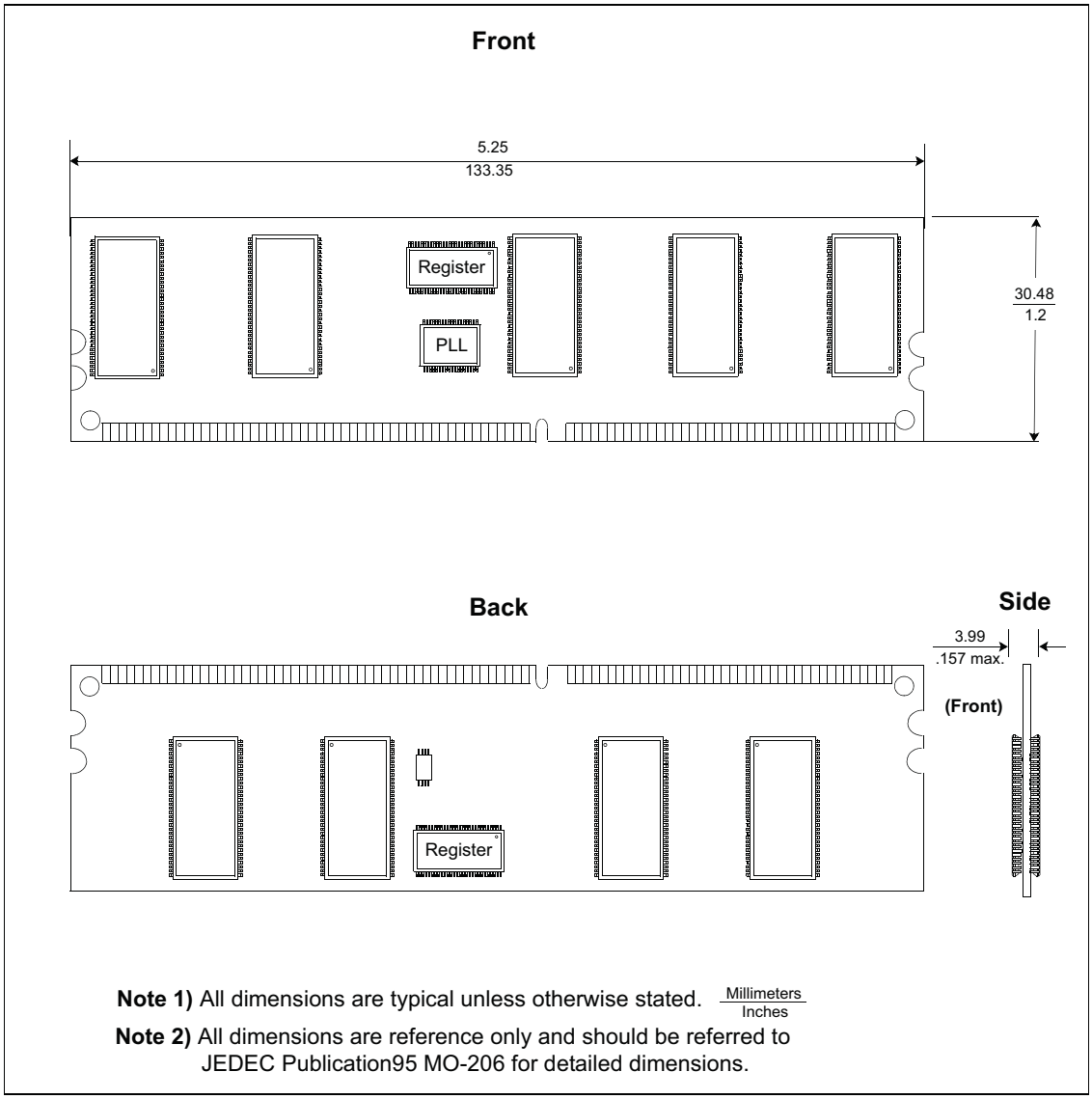

**Note 1)** All dimensions are typical unless otherwise stated. Millimeters / Inches

**Note 2)** All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.



Micron Technology Inc. et al.
Ex. 1017, p. 40

## Example Raw Card Versions L (1 Physical Banks) Component Placement




**Note 1)** All dimensions are typical unless otherwise stated. Millimeters / Inches

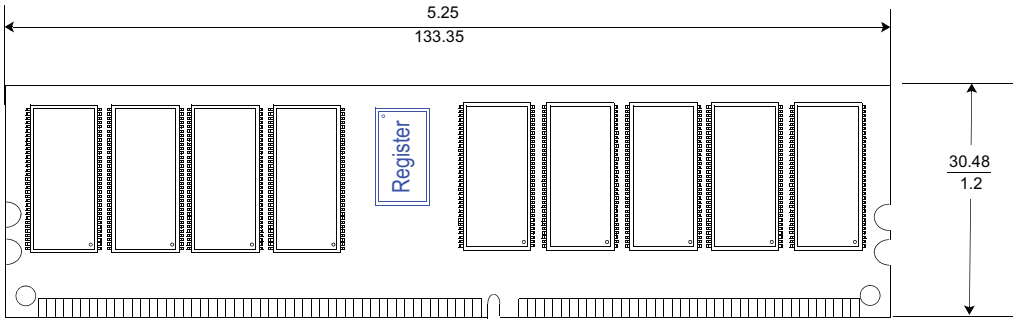
**Note 2)** All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.



Micron Technology Inc. et al.
Ex. 1017, p. 41

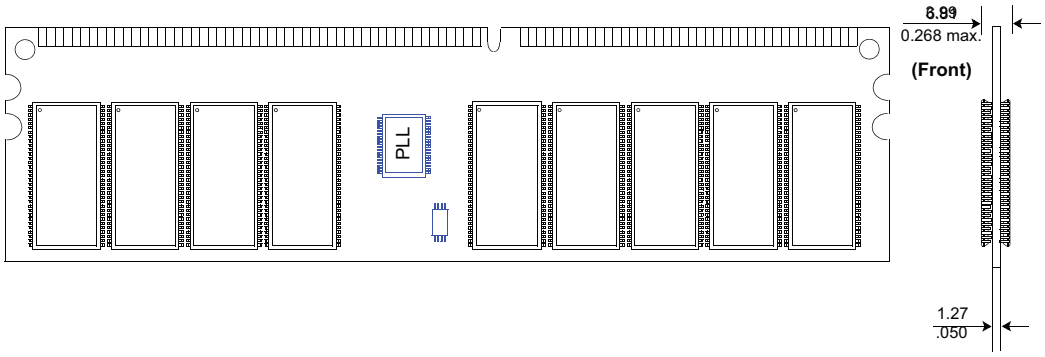
## Example Raw Card Versions N (2 Physical Banks) Component Placement

**Front**




**Back**

**Side**




**Note 1)** All dimensions are typical unless otherwise stated. Millimeters / Inches

**Note 2)** All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.



Micron Technology Inc. et al.
Ex. 1017, p. 42

# DIMM Wiring Details

## Signal Groups

This specification categorizes DDR SDRAM timing-critical signals into seven groups. The following table summarizes the signals contained in each group.

| Signal Group | Signals In Group | Raw Card Version | Page |
|---|---|---|---|
| PLL Input / Unused Clocks | CK, $\overline{CK}$ | A, B, C, E, L, M, N | 39 |
| PLL Output | PCK[9:0] | A, B, C, E, L, M | 40, 42. 43, 44 |
| | | N | 41, 45 |
| Data | DQ[63:0], CB[7:0] | B, C, E, M, N | 44 |
| | | A, L | 44-45 |
| DQS | DQS[17:0] | B, C, E, M, N | 44 |
| | | A, L | 44-45 |
| DM | DM[8:0] | A, L | 45 |
| Address and Control | A[12:0], BA[1:0], RAS, CAS, WE | A, B | 46, 47 |
| | A[13:0], BA[1:0], RAS, CAS, WE | L, M | 48, 49 |
| | A[13:0], BA[1:0], RAS, CAS, WE | N | 54, 55 |
| | A[12:0], BA[1:0], RAS, CAS, WE | C, E | 62, 63 |
| Chip Select, Clock Enable | $\overline{CS}$[0-1], CKE[0-1] | A | 58, 59 |
| | | L | 52, 57 |
| | | B | 60, 61 |
| | | M | 54, 55 |
| | | N | 60, 61 |
| | | C, E | 64, 65 |

## General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing requirements are as follows

- Route all signal traces except clocks using 4/6 rules, i.e., 4 mil traces and 6 mil minimum spacing between adjacent traces.
- Route clocks using 4 mil lines and 6 mil spaces between differential clock pairs.
- Route clocks using at least 90% of the total trace length in the inner layers.



Micron Technology Inc. et al.
Ex. 1017, p. 43

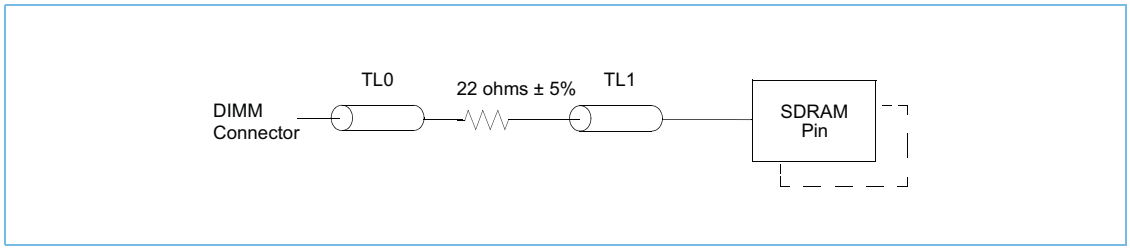
## Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for registered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. **The given net structures and trace lengths are not inclusive for all solutions.**

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. **It is highly recommended that the net structure routing data in this document be simulated by the user.**

## Net Structure Example

A 512MB double-sided x72 DIMM using 128Mbit, 32Mx4 SDRAM devices would have a data net structure as shown in the following diagram.






Micron Technology Inc. et al.
Ex. 1017, p. 44

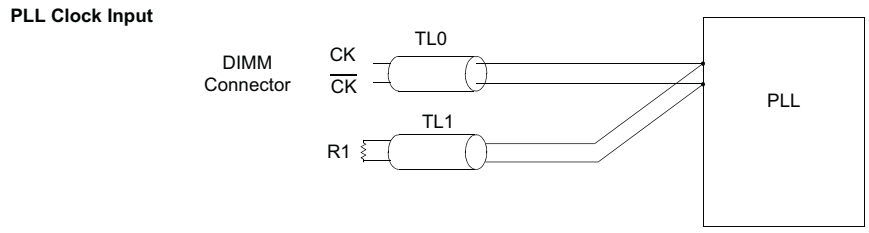
## Differential Clock Net Structures

### CK, $\overline{CK}$

DDR SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/Fall time
- Cross point of the differential pair into the SDRAM and register
- JEDEC-compatible reference delays
- Minimal segment length differences (less than 100 mils total) between clocks of the same function
- PLL input net segment length is newly defined and optimized for high speed DDR Registered DIMMs.

## Net Structure Routing for PLL Input




## Clock Net Lengths for PLL Input Net Structures

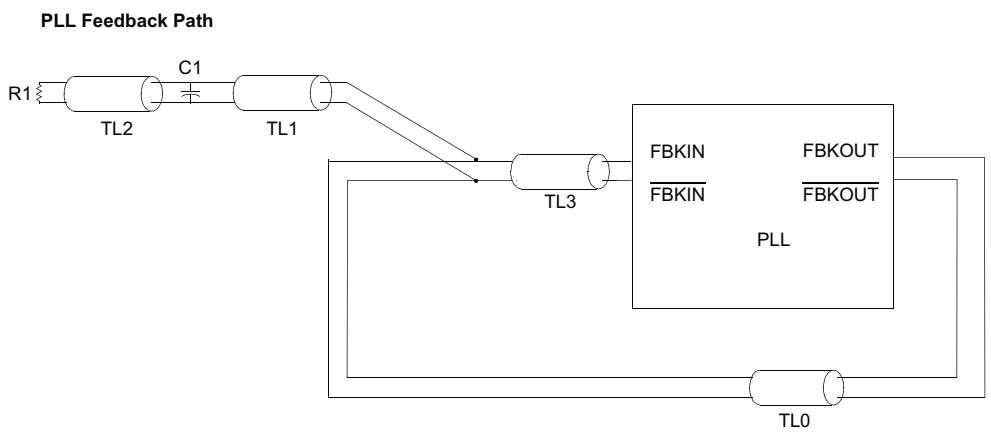
| Raw Card | TL0 | TL1 | R1 (Ohms) | Notes |
|---|---|---|---|---|
| A, B, C, E, L, M, N | 1.00 | 0.20 | 120 | 1, 2, 3 |

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%.
3. The termination resistor and loading capacitor are both placed after the pin of the PLL.



Micron Technology Inc. et al.
Ex. 1017, p. 45

## Net Structure Routing for PLL Feedback Path




## Trace Lengths for PLL Feedback Path Net Structure

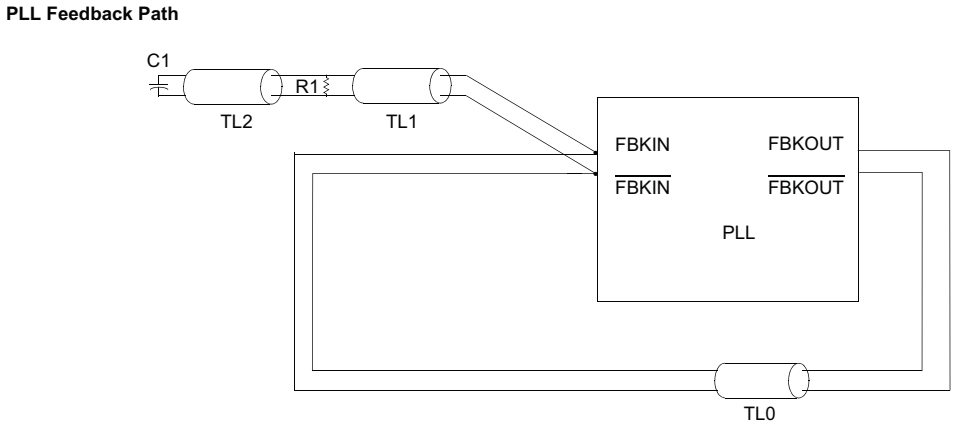
| Raw Card | TL0 | | TL1 | TL2 | TL3 | | R1 (Ohms) | C1 [pF] | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | | | Min | Max | | | |
| A, B | 2.92 | 3.02 | 0.04 | 0.29 | 0.05 | 0.09 | 120 | Not populated | 1, 2, 3 |
| C, E | 2.93 | 3.02 | 0.04 | 0.29 | 0.05 | 0.09 | 120 | 5.6 | 1, 2, 3 |
| L | 3.00 | 3.00 | 0.04 | 0.06 | 0.09 | 0.09 | 120 | Not populated | 1, 2, 3 |
| M | 3.00 | 3.00 | 0.05 | 0.13 | 0.05 | 0.06 | 120 | Not populated | 1, 2, 3 |

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%.
3. The termination resistor and loading capacitor are both placed as close to the pin of the PLL as possible.



Micron Technology Inc. et al.
Ex. 1017, p. 46

## Net Structure Routing for PLL Feedback Path (Raw Card N)




## Trace Lengths for PLL Feedback Path Net Structure

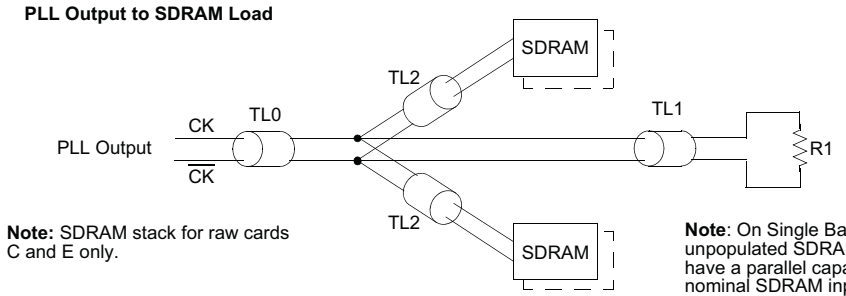
| Raw Card | TL0 | | TL1 | TL2 | R1 (Ohms) | C1 [pF] | Notes |
|---|---|---|---|---|---|---|---|
| | Min | Max | | | | | |
| N | 3.00 | 3.00 | 0.15 | 0.05 | 120 | Not populated | 1, 2, 3 |

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%.
3. The termination resistor and loading capacitor are both placed as close to the pin of the PLL as possible.



Micron Technology Inc. et al.
Ex. 1017, p. 47

## Net Structure Routing for PLL Output to SDRAM Load




**Note:** SDRAM stack for raw cards C and E only.

**Note**: On Single Bank A-Card, unpopulated SDRAM clock pair inputs have a parallel capacitor equal to one-half nominal SDRAM input clock load.

## Trace Lengths for PLL Clock Output to SDRAM Load Net Structure

| Raw Card | TL0 | | TL1 | | TL2 | | R1 Ohms | Notes |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | | |
| A | 2.46 | 2.50 | 0.49 | 0.58 | 0.29 | 0.30 | 120 | 1, 2 |
| B | 2.46 | 2.49 | 0.49 | 0.57 | 0.29 | 0.31 | 120 | 1, 2 |
| C/E | 2.51 | 2.52 | 0.57 | 0.57 | 0.29 | 0.31 | 120 | 1, 2 |
| L | 2.50 | 2.51 | 0.58 | 0.58 | 0.30 | 0.30 | 120 | 1, 2 |
| M | 2.46 | 2.50 | 0.54 | 0.57 | 0.30 | 0.31 | 120 | 1, 2 |
| N | 2.46 | 2.50 | 0.54 | 0.57 | 0.30 | 0.31 | 120 | 1, 2 |

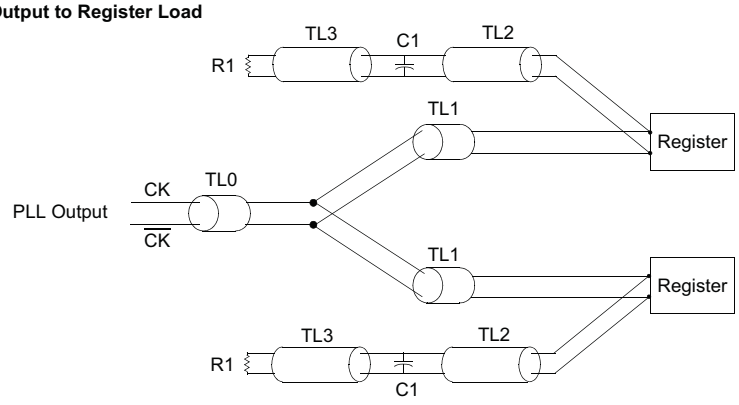
1. All distances are in inches and should be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and should be kept within a tolerance of ± 5%.



Micron Technology Inc. et al.
Ex. 1017, p. 48

## Net Structure Routing for PLL Output to Register Load

**PLL Output to Register Load**




**Unloaded PLL Output**

All PLL outputs are used in each design.

## Trace Lengths for PLL Clock Output to Register Load Net Structure

| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | R1 [Ohms[ | C1 [pF] | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| A | 0.05 | 0.05 | 2.71 | 2.72 | 0.13 | 0.15 | 0.07 | 0.07 | 240 | Not populated | 1, 2 |
| B | 0.05 | 0.05 | 2.71 | 2.72 | 0.13 | 0.15 | 0.07 | 0.07 | 240 | Not populated | 1, 2 |
| C/E | 0.05 | 0.05 | 3.51 | 3.51 | 0.13 | 0.14 | 0.07 | 0.07 | 240 | Not populated | 1, 2 |
| L | 0.05 | 0.05 | 2.71 | 2.71 | 0.10 | 0.11 | 0.06 | 0.06 | 240 | TBD | 1, 2 |
| M | 0.10 | 0.11 | 2.68 | 2.70 | 0.14 | 0.14 | 0.06 | 0.06 | 240 | TBD | 1, 2 |

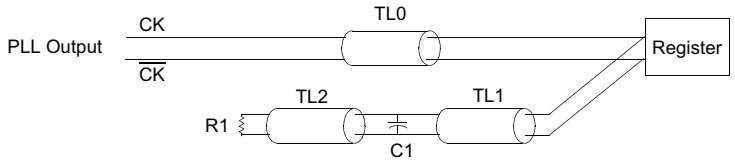
1. All distances are in inches and should be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and should be kept within a tolerance of ± 5%.



Micron Technology Inc. et al.
Ex. 1017, p. 49

## Net Structure Routing for PLL Output to Register Load (Raw Card N)

**PLL Output to Register Load**




**Unloaded PLL Output**

All PLL outputs are used in each design.

## Trace Lengths for PLL Clock Output to Register Load Net Structure

| Raw Card | TL0 | | TL1 | | TL2 | | R1 [Ohms[ | C1 [pF] | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | | | |
| N | 2.80 | 2.80 | 0.14 | 0.14 | 0.06 | 0.06 | 240 | TBD | 1, 2 |

1. All distances are in inches and should be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and should be kept within a tolerance of ± 5%.



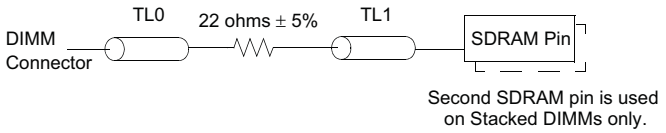
Micron Technology Inc. et al.
Ex. 1017, p. 50

## Data Net Structures

**DQ[63:0], CB[7:0]**
**DQS[17:0]**

Special attention has been paid to balancing data nets within a DDR SDRAM, within a particular DIMM, and across the DIMM family. Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing. Although it is not necessary to ensure consistent delays between SDRAMs and/or card types, doing so facilitates system design, system simulation, and DIMM specifications. We recommend consistent delays for all nets, as described in the following tables.

### Net Structure Routing for Data and DQS (Raw Cards B, C, E, M and N)



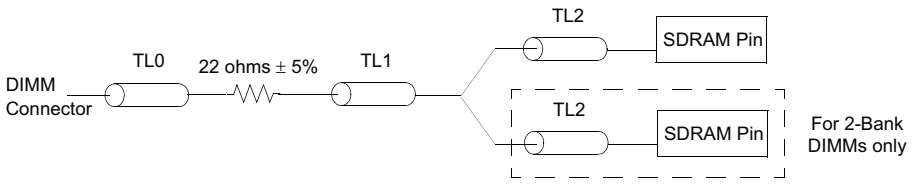

### Trace Lengths for Data and DQS Net Structure (Raw Cards B, C, E and M)

| Raw Card | TL0 | | TL1 | | Total | | Notes |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| B | 0.13 | 0.19 | 0.95 | 1.02 | 1.13 | 1.14 | 1, 2 |
| C/E | 0.13 | 0.19 | 0.95 | 1.02 | 1.13 | 1.15 | 1, 2 |
| M | 0.13 | 0.17 | 0.70 | 0.77 | 0.86 | 0.92 | 1, 2 |
| N | 0.13 | 0.17 | 0.70 | 0.77 | 0.86 | 0.92 | 1, 2 |

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1.

**DQ[63:0], CB[7:0]**
**DQS[8:0]**

### Net Structure Routing for Data and DQS (Raw Cards A and L)






Micron Technology Inc. et al.
Ex. 1017, p. 51

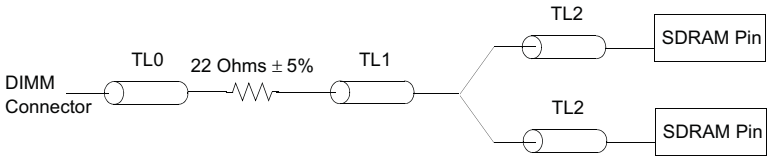
## Trace Lengths for Data and DQS Net Structure (Raw Cards A and L)

| Raw Card | TL0 | | TL1 | | TL2 | | Total | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| A | 0.13 | 0.19 | 0.59 | 0.65 | 0.37 | 0.37 | 1.15 | 1.15 | 1, 2 |
| L | 0.20 | 0.20 | 0.50 | 0.50 | 0.25 | 0.25 | 0.93 | 0.94 | 1, 2 |

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2

**DM[8:0]**

## Net Structure Routing for DM (Raw Cards A and L)




## Trace Lengths for DM Net Structure (Raw Cards A and L)

| Raw Card | TL0 | | TL1 | | TL2 | Total | | Notes |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | Min | Max | |
| A | 0.13 | 0.19 | 0.67 | 0.69 | 0.44 | 1.25 | 1.30 | 1, 2 |
| L | 0.19 | 0.20 | 0.51 | 0.51 | 0.31 | 1.01 | 1.02 | 1, 2 |

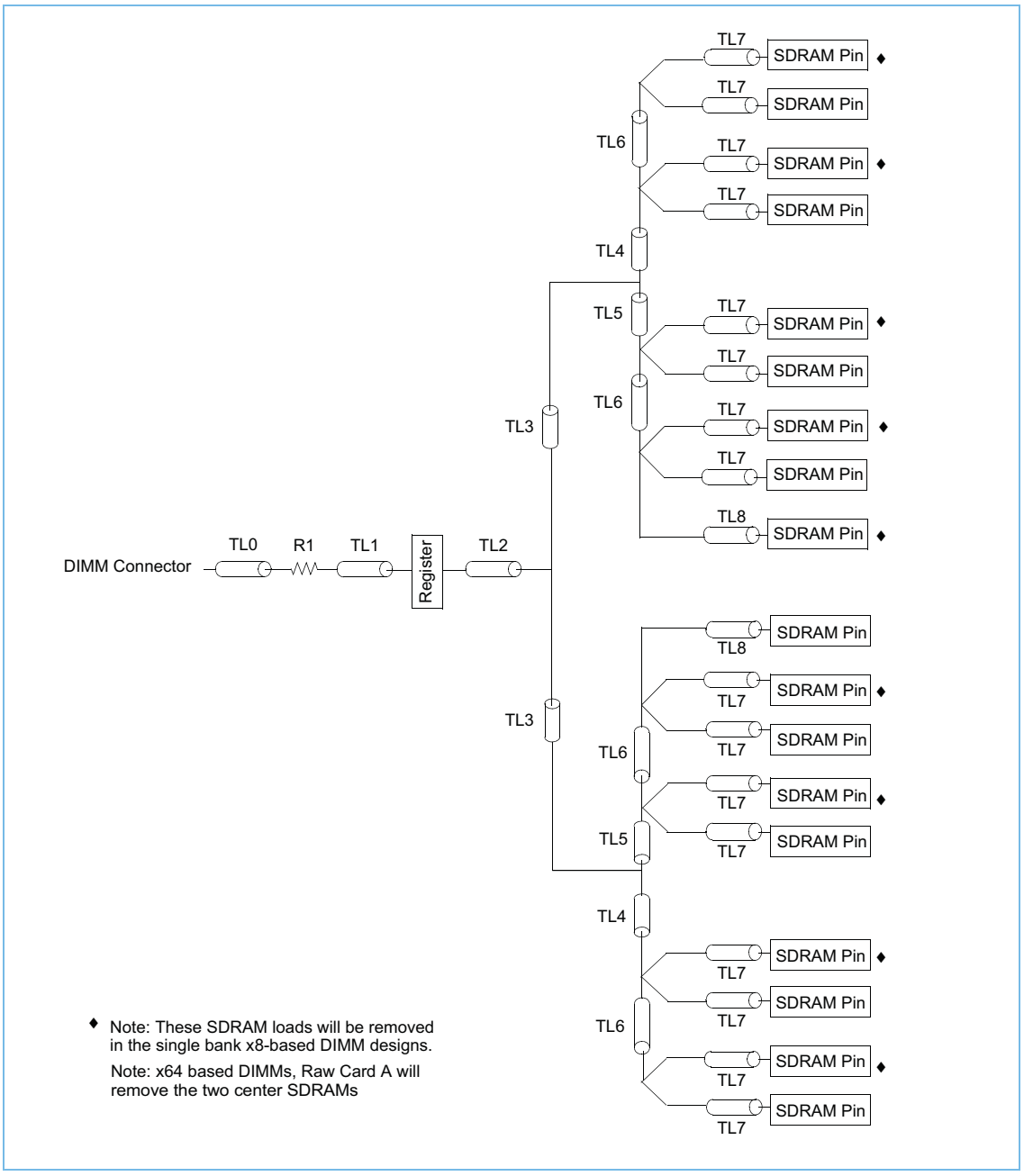
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1.



Micron Technology Inc. et al.
Ex. 1017, p. 52

## Net Structure Routing for Address and Control (Raw Cards A and B)

A[12:0], BA[1:0], RAS, CAS, WE






Micron Technology Inc. et al.
Ex. 1017, p. 53

## Trace Lengths for Address and Control Net Structure (Raw Cards A and B)

A[12:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | TL4 | | TL5 | | TL6 | | TL7 | | TL8 | | R1 [Ohms] | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| A | 0.13 | 0.26 | 0.56 | 0.66 | 0.62 | 1.37 | 1.39 | 2.57 | 0.40 | 0.56 | 0.14 | 0.15 | 0.48 | 0.63 | 0.20 | 0.32 | 0.49 | 0.72 | 22 | 1 |
| B | 0.13 | 0.28 | 0.54 | 0.67 | 0.66 | 1.38 | 1.31 | 2.55 | 0.40 | 0.53 | 0.12 | 0.15 | 0.50 | 0.64 | 0.20 | 0.29 | 0.49 | 0.72 | 22 | |

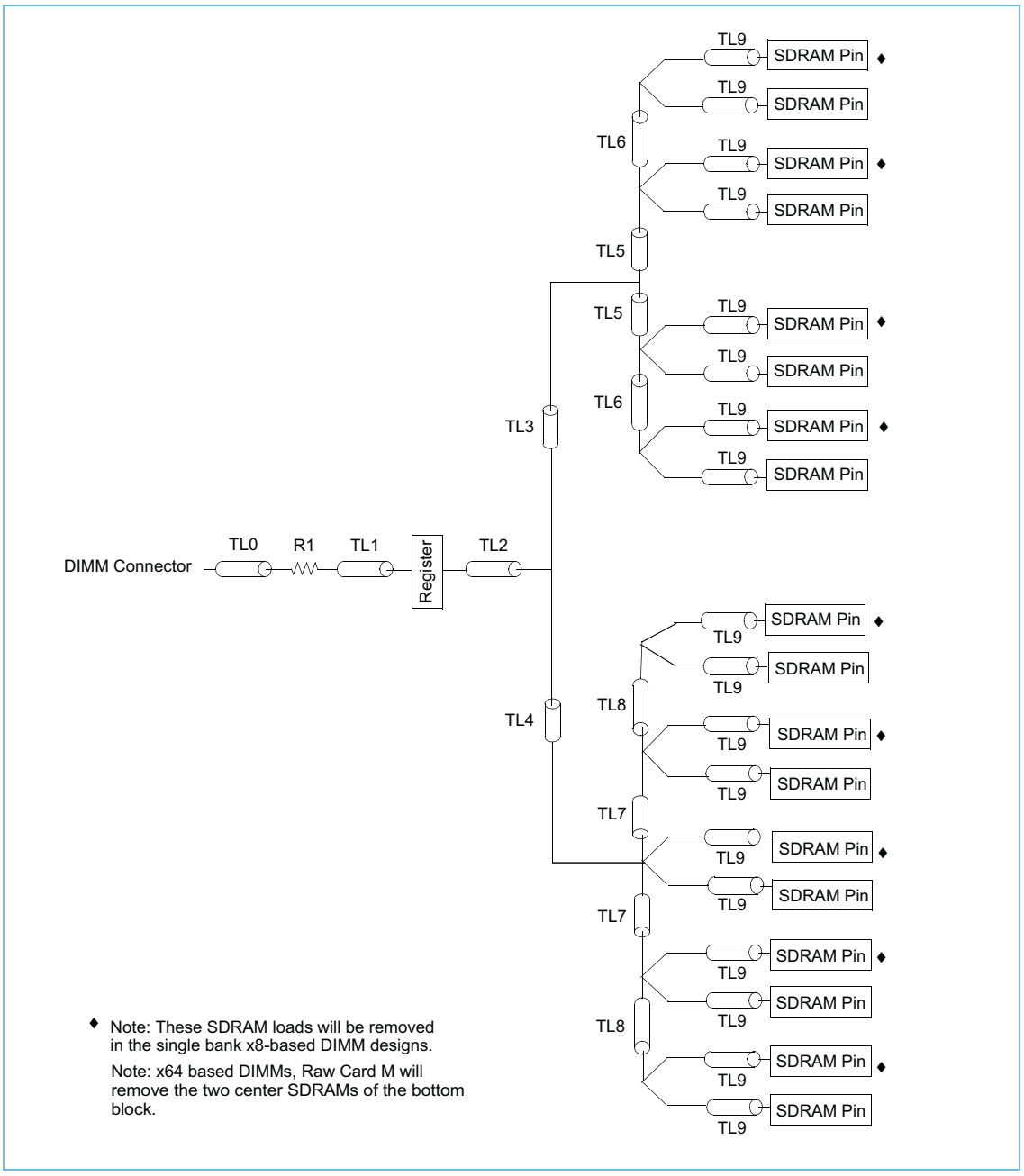
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch



Micron Technology Inc. et al.
Ex. 1017, p. 54

## Net Structure Routing for Address and Control (Raw Cards L, and M)

A[13:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$






Micron Technology Inc. et al.
Ex. 1017, p. 55

## Trace Lengths for Address and Control Net Structure (Raw Cards L and M)

A[13:0], BA [1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | TL4 | | TL5 | | TL6 | | TL7 | | TL8 | | TL9 | | R1 (Ohms) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| L | 0.14 | 0.21 | 1.16 | 1.96 | 0.05 | 0.27 | 1.55 | 2.25 | 1.54 | 1.80 | 0.19 | 0.42 | 0.48 | 0.59 | 0.51 | 0.53 | 0.50 | 0.54 | 0.17 | 0.37 | 22 |
| M | 0.13 | 0.20 | 1.34 | 1.91 | 0.12 | 0.23 | 2.13 | 2.17 | 1.69 | 1.86 | 0.21 | 0.38 | 0.52 | 0.54 | 0.52 | 0.53 | 0.52 | 0.53 | 0.20 | 0.30 | 22 |

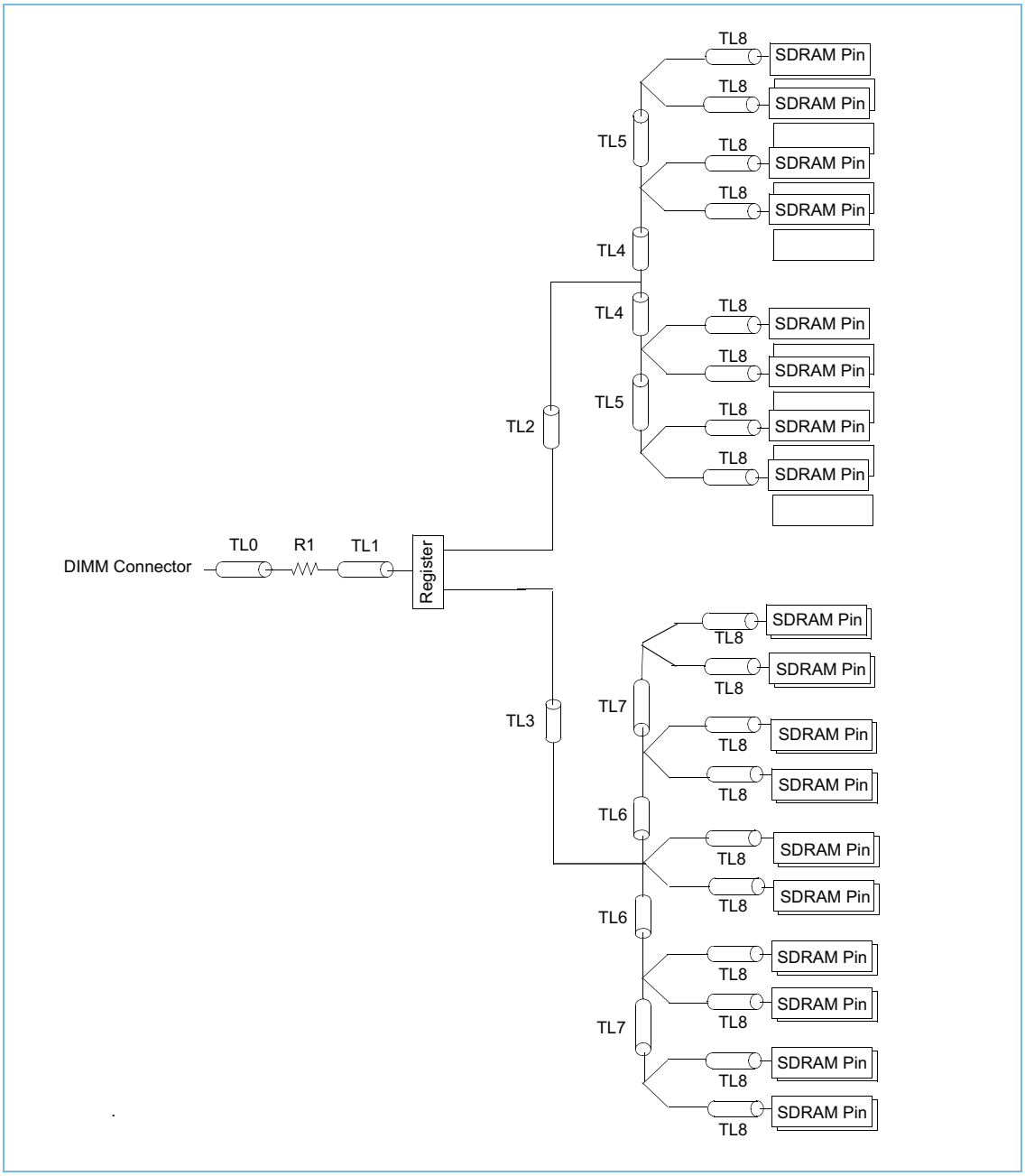
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.
2. For Raw Card L, min(TL3 - TL4) = -0.02", max(TL3 - TL4) = 0.55",
   and for Raw Card M, min(TL3 - TL4) = 0.27", max(TL3 - TL4) = 0.46"



Micron Technology Inc. et al.
Ex. 1017, p. 56

## Net Structure Routing for Address and Control (Raw Card N)

A[13:0], BA[1:0],RAS, CAS, WE






Micron Technology Inc. et al.
Ex. 1017, p. 57

## Trace Lengths for Address and Control Net Structure (Raw Card N)

A[13:0], BA [1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

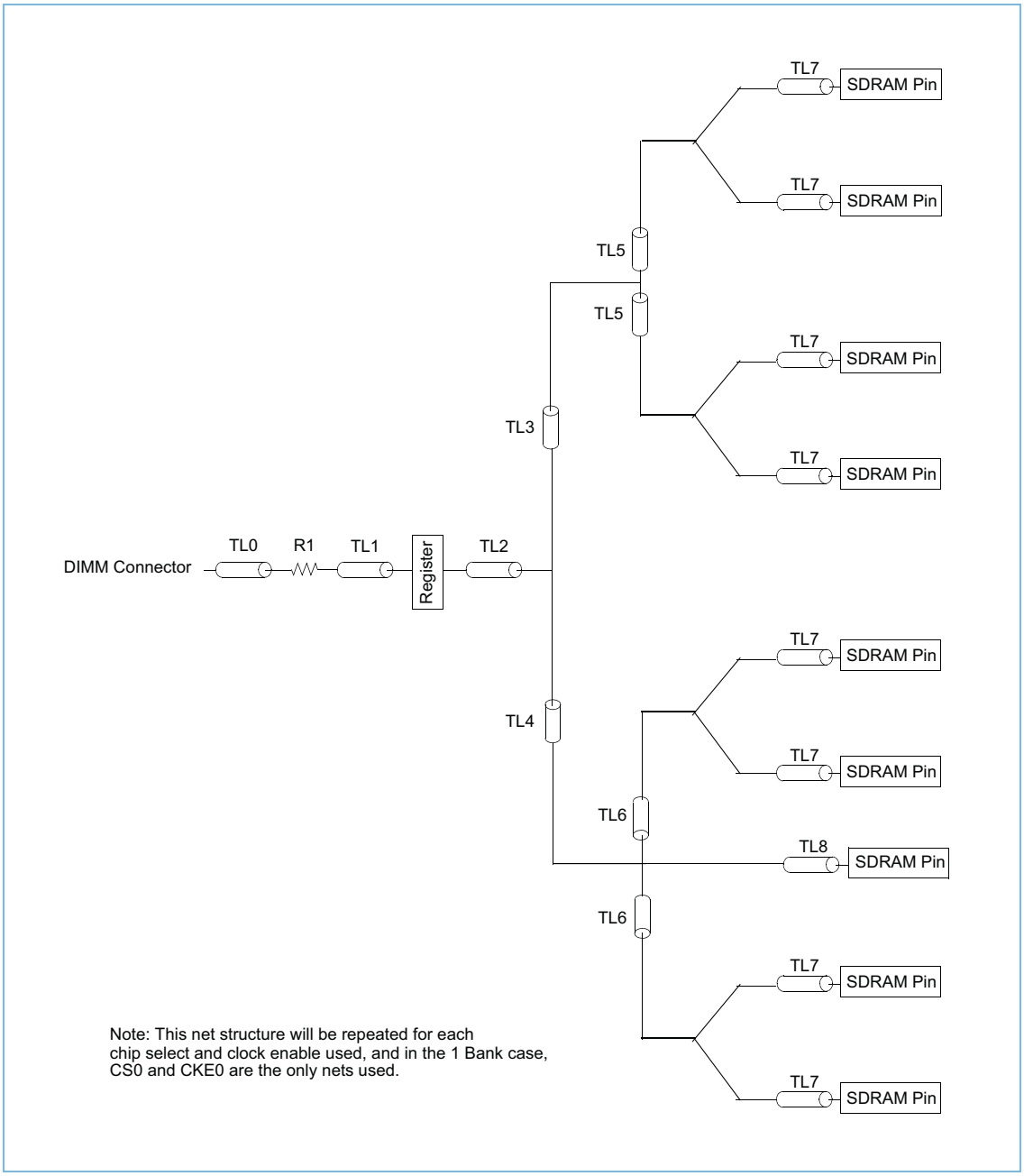
| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | TL4 | | TL5 | | TL6 | | TL7 | | TL8 | | R1 (Ohms) | note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| N | 0.13 | 0.21 | 1.79 | 1.80 | 2.06 | 2.07 | 1.66 | 1.67 | 0.20 | 0.39 | 0.53 | 0.54 | 0.53 | 0.54 | 0.53 | 0.54 | 0.20 | 0.30 | 22 | |
| | 0.13 | 0.21 | 1.79 | 2.07 | 2.06 | 2.07 | 1.66 | 1.67 | 0.20 | 0.39 | 0.53 | 0.54 | 0.53 | 0.54 | 0.53 | 0.54 | 0.20 | 0.30 | 22 | A13 only |
| 1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches. | | | | | | | | | | | | | | | | | | | | |



Micron Technology Inc. et al.
Ex. 1017, p. 58

## Net Structure Routing for $\overline{CS}$ and CKE (Raw Card L)

$\overline{CS}$[1:0], CKE[1:0]






Micron Technology Inc. et al.
Ex. 1017, p. 59

## Trace Lengths for $\overline{CS}$ and CKE Net Structure (Raw Card L)

A[13:0], BA [1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | TL4 | | TL5 | | TL6 | | TL7 | | TL8 | | TL9 | | R1 (Ohms) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| L | 0.14 | 0.21 | 1.16 | 1.96 | 0.05 | 0.27 | 1.55 | 2.25 | 1.54 | 1.80 | 0.19 | 0.42 | 0.48 | 0.59 | 0.51 | 0.53 | 0.50 | 0.54 | 0.17 | 0.37 | 22 |

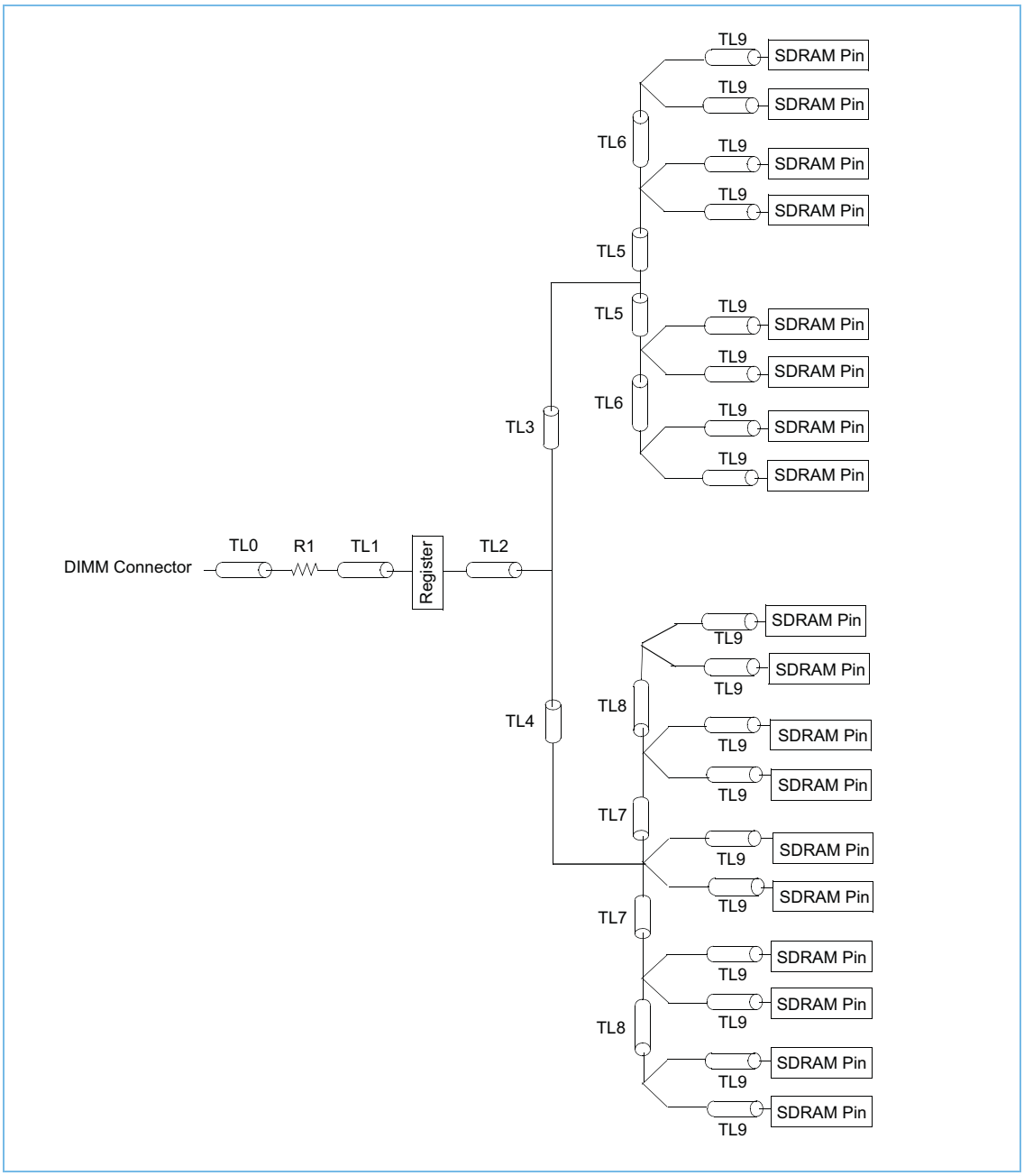
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.
2. For Raw Card L, min(TL3 - TL4) = -0.02", max(TL3 - TL4) = 0.55"



Micron Technology Inc. et al.
Ex. 1017, p. 60

## Net Structure Routing for $\overline{CS}$ and CKE (Raw Card M)

$\overline{CS}$[0], CKE[0]






Micron Technology Inc. et al.
Ex. 1017, p. 61

## Trace Lengths for $\overline{CS}$ and CKE Net Structure (Raw Card M)

CS[0], CKE [0]

| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | TL4 | | TL5 | | TL6 | | TL7 | | TL8 | | TL9 | | R1 (Ohms) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| M | 0.13 | 0.20 | 1.34 | 1.46 | 0.12 | 0.23 | 2.13 | 2.17 | 1.69 | 1.86 | 0.21 | 0.38 | 0.52 | 0.53 | 0.52 | 0.53 | 0.52 | 0.53 | 0.20 | 0.30 | 22 |

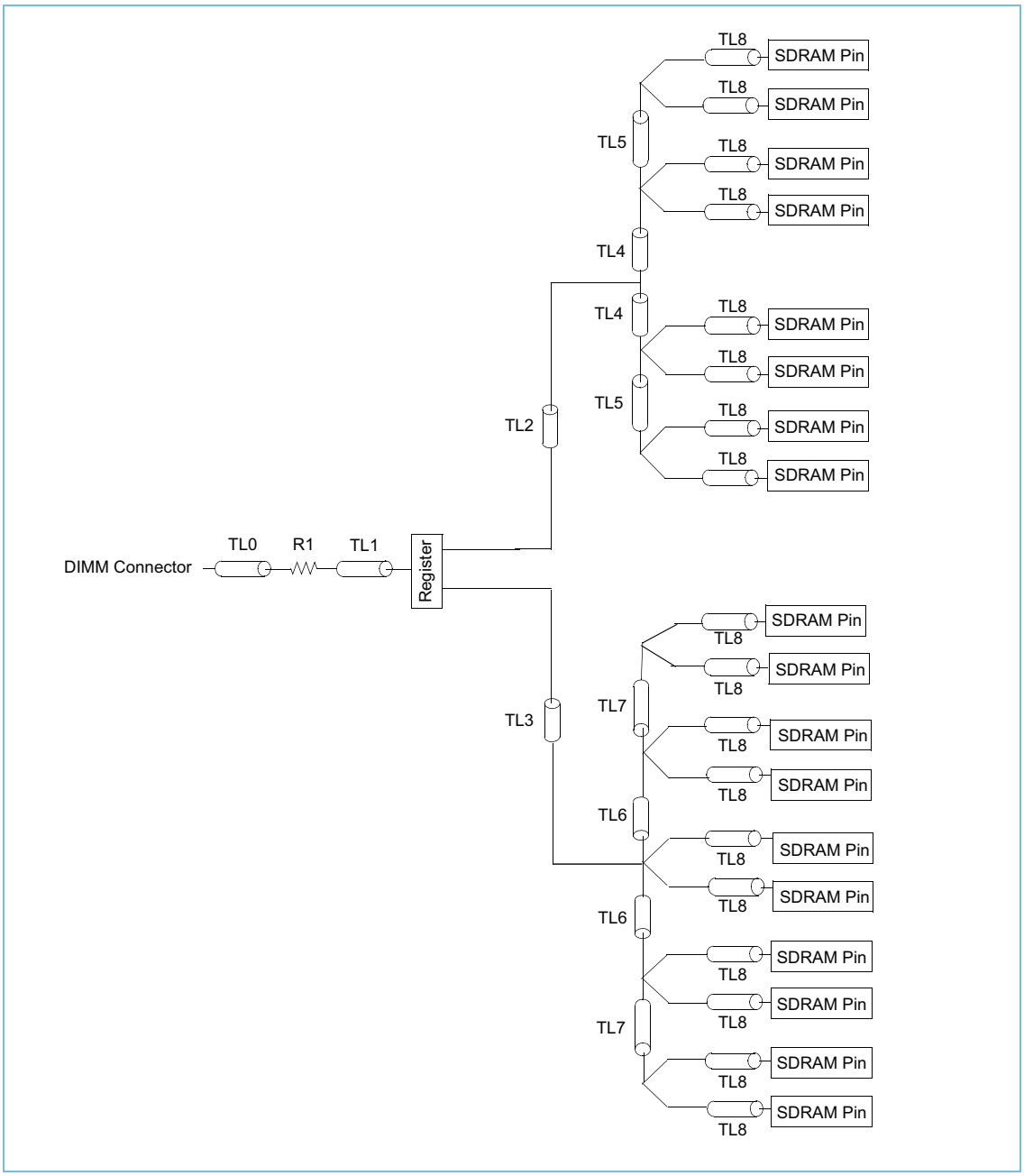
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.
2. For Raw Card M, min(TL3 - TL4) = 0.29", max(TL3 - TL4) = 0.41"



Micron Technology Inc. et al.
Ex. 1017, p. 62

## Net Structure Routing for $\overline{CS}$ and CKE (Raw Card N)

$\overline{CS}$[1:0], CKE[1:0]






Micron Technology Inc. et al.
Ex. 1017, p. 63

## Trace Lengths for $\overline{CS}$ and CKE Net Structure (Raw Card N)

CS[1:0], CKE [1:0]

| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | TL4 | | TL5 | | TL6 | | TL7 | | TL8 | | R1 (Ohms) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| N | 0.13 | 0.21 | 1.79 | 1.80 | 2.06 | 2.07 | 1.66 | 1.67 | 0.20 | 0.39 | 0.53 | 0.54 | 0.53 | 0.54 | 0.53 | 0.54 | 0.22 | 0.35 | 22 |

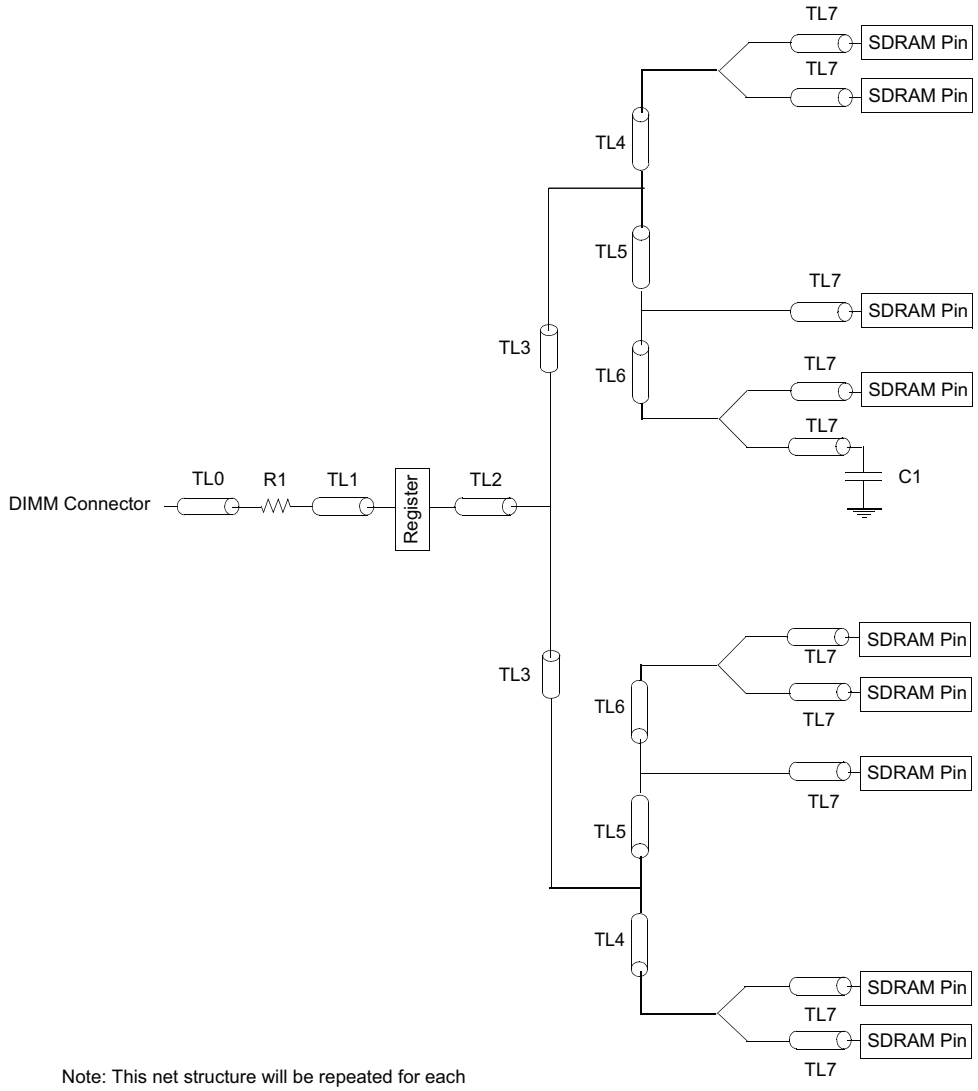
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.



Micron Technology Inc. et al.
Ex. 1017, p. 64

## Net Structure Routing for $\overline{CS}$ and CKE (Raw Card A)

$\overline{CS}$ [1:0], CKE [1:0]




Note: This net structure will be repeated for each chip select and clock enable used, and in the 1 Bank case, CS0 and CKE0 are the only nets used.



Micron Technology Inc. et al.
Ex. 1017, p. 65

## Trace Lengths for $\overline{CS}$ and CKE (Raw Card A)

**CS [1:0], CKE [1:0]**

| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | TL4 | | TL5 | | TL6 | | TL7 | | C1 [pF] | R1 [Ohms] | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | | |
| A | 0.12 | 0.21 | 0.60 | 0.65 | 1.16 | 1.43 | 1.67 | 2.10 | 0.15 | 0.28 | 0.53 | 0.69 | 0.23 | 0.77 | 0.08 | 0.78 | 3.0 | 22 | 1 |

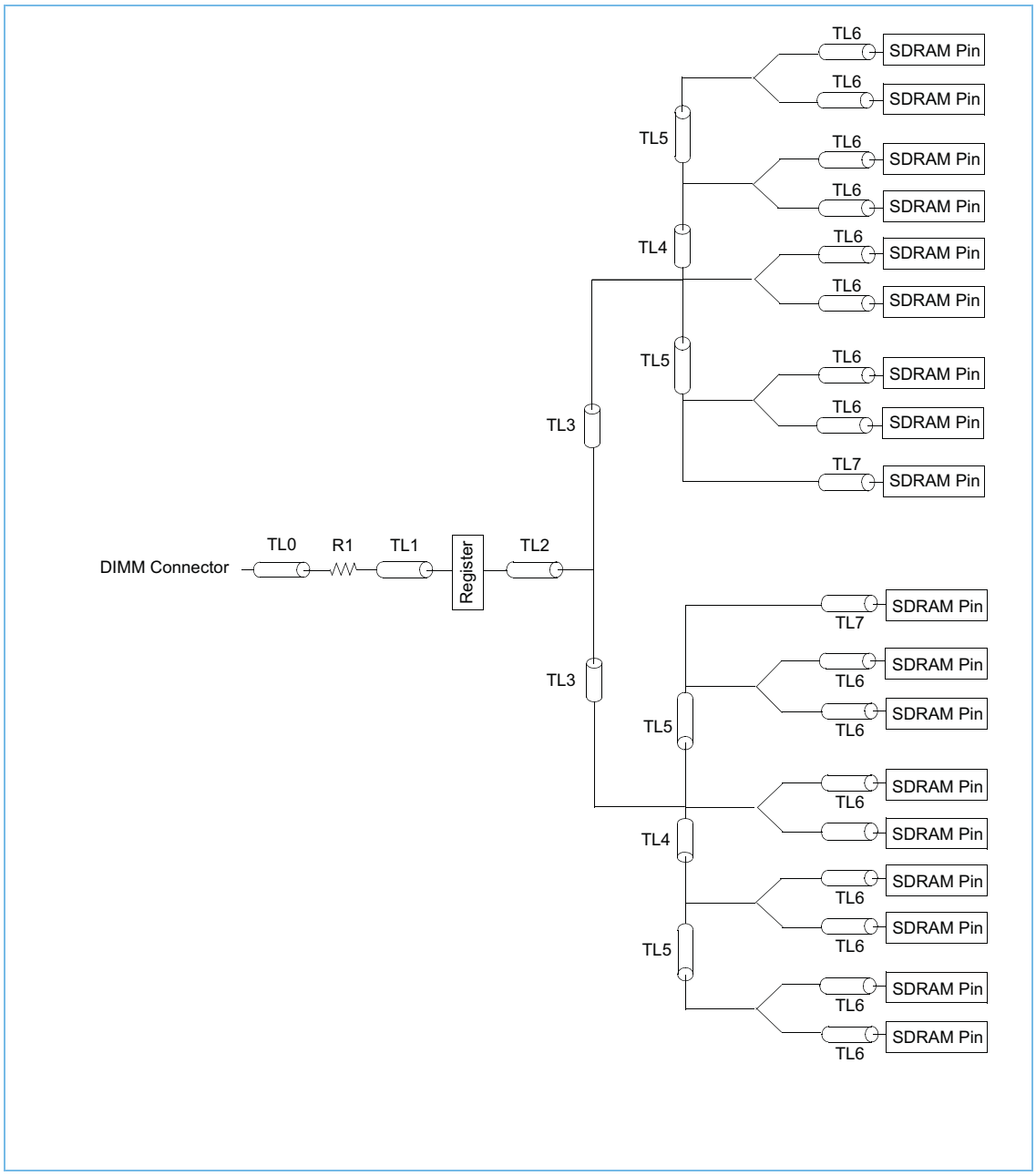
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch



Micron Technology Inc. et al.
Ex. 1017, p. 66

## Net Structure Routing for $\overline{CS}$ and CKE (Raw Card B)

$\overline{CS}$ [0], CKE [0]






Micron Technology Inc. et al.
Ex. 1017, p. 67

## Trace Lengths for $\overline{CS}$ and CKE (Raw Card B)

**CS [0], CKE [0]**

| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | TL4 | | TL5 | | TL6 | | TL7 | | R1 [Ohms] | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| B | 0.13 | 0.16 | 0.612 | 0.65 | 1.17 | 1.23 | 1.43 | 1.68 | 0.58 | 0.72 | 0.40 | 0.58 | 0.15 | 0.35 | 0.56 | 0.76 | 22 | 1 |

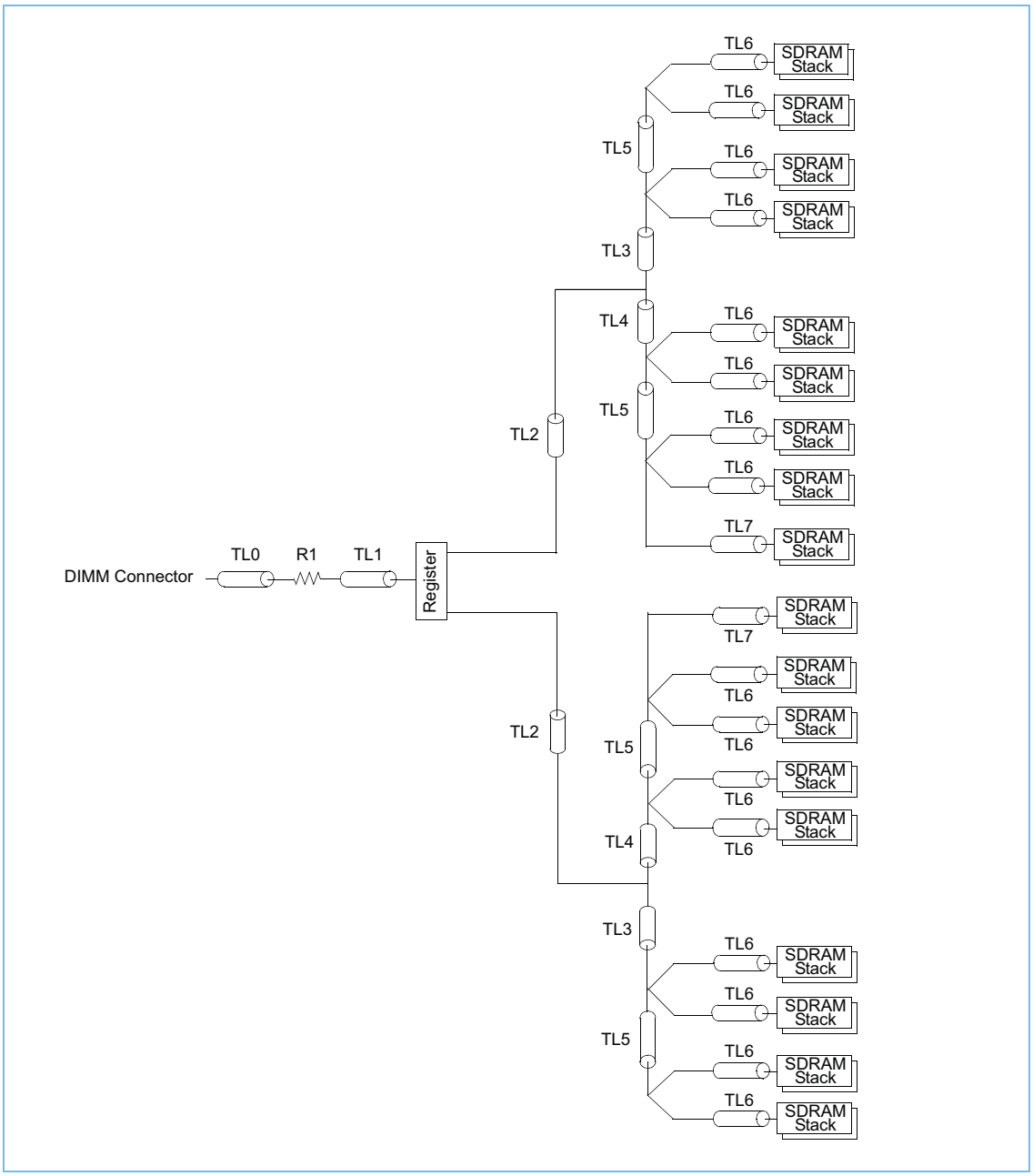
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch



Micron Technology Inc. et al.
Ex. 1017, p. 68

## Net Structure Routing for Address and Control (Raw Cards C and E)

A[12:0], BA[1:0], RAS, CAS, WE






Micron Technology Inc. et al.
Ex. 1017, p. 69

## Trace Lengths for Address and Control Net Structure (Raw Cards C and E)

A[12:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | TL4 | | TL5 | | TL6 | | TL7 | | R1 (Ohms) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| C | 0.13 | 0.25 | 0.56 | 0.66 | 0.70 | 2.81 | 0.40 | 0.58 | 0.07 | 0.23 | 0.48 | 0.61 | 0.20 | 0.35 | 0.49 | 0.74 | 22 | 1 |
| E | 0.13 | 0.23 | 0.56 | 0.66 | 0.70 | 2.81 | 0.40 | 0.58 | 0.07 | 0.15 | 0.48 | 0.61 | 0.20 | 0.35 | 0.49 | 0.74 | 22 | 1 |

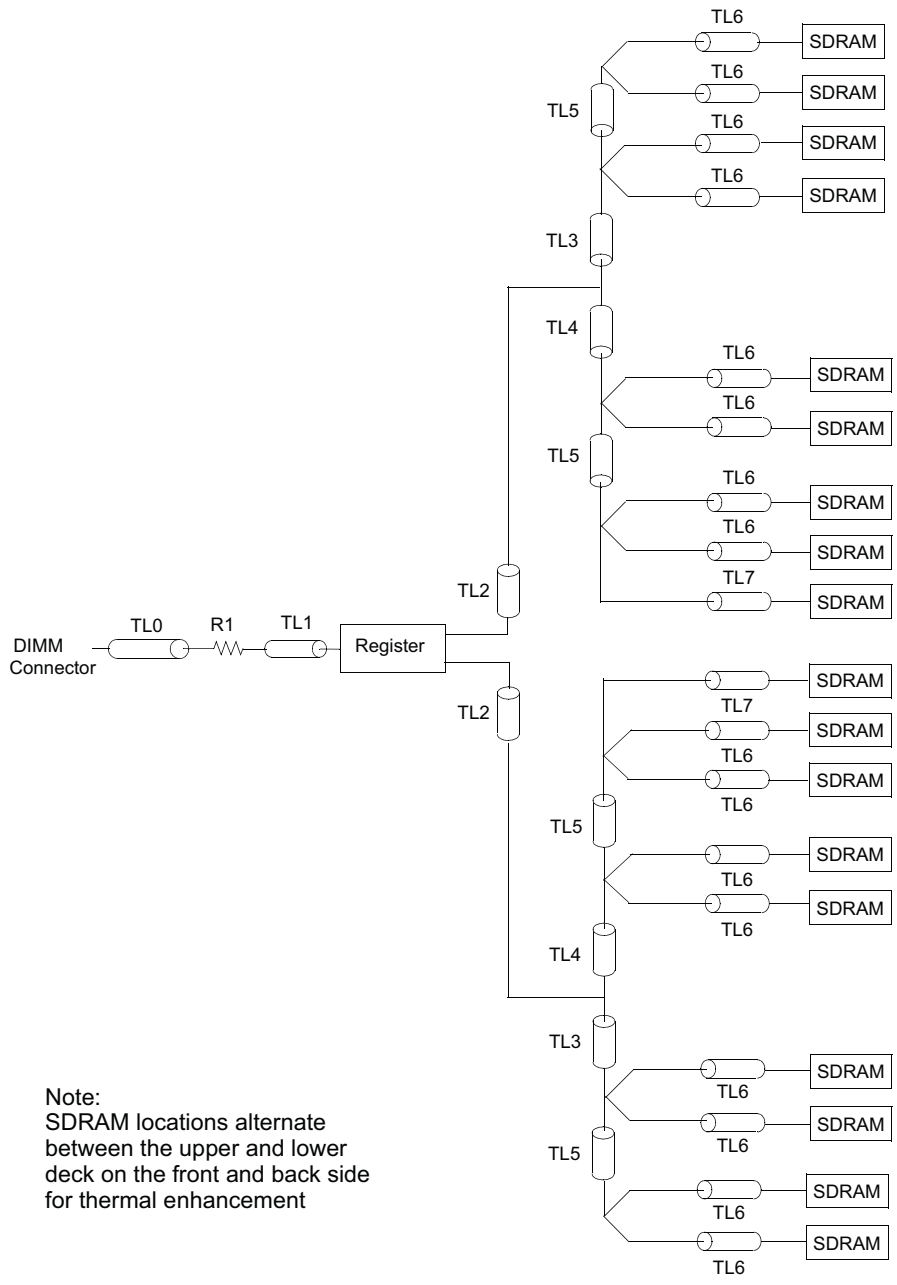
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch.



Micron Technology Inc. et al.
Ex. 1017, p. 70

## Net Structure Routing for $\overline{CS}$ and CKE (Raw Cards C and E)

$\overline{CS}$[1:0], CKE [1:0]






Micron Technology Inc. et al.
Ex. 1017, p. 71

## Trace Lengths for $\overline{CS}$ and CKE Net Structure (Raw Cards C and E)

$\overline{CS}$[1:0], CKE [1:0]

| Raw Card | TL0 | | TL1 | | TL2 | | TL3 | | TL4 | | TL5 | | TL6 | | TL7 | | R1 (Ohms) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| C | 0.14 | 0.19 | 0.50 | 0.51 | 2.14 | 3.14 | 0.45 | 0.61 | 0.08 | 0.23 | 0.42 | 0.57 | 0.11 | 0.45 | 0.68 | 0.83 | 22 |
| E | 0.14 | 0.19 | 0.50 | 0.51 | 2.14 | 3.14 | 0.45 | 0.61 | 0.08 | 0.23 | 0.42 | 0.57 | 0.11 | 0.45 | 0.68 | 0.83 | 22 |
| 1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches. | | | | | | | | | | | | | | | | | |



Micron Technology Inc. et al.
Ex. 1017, p. 72

## Cross Section Recommendations

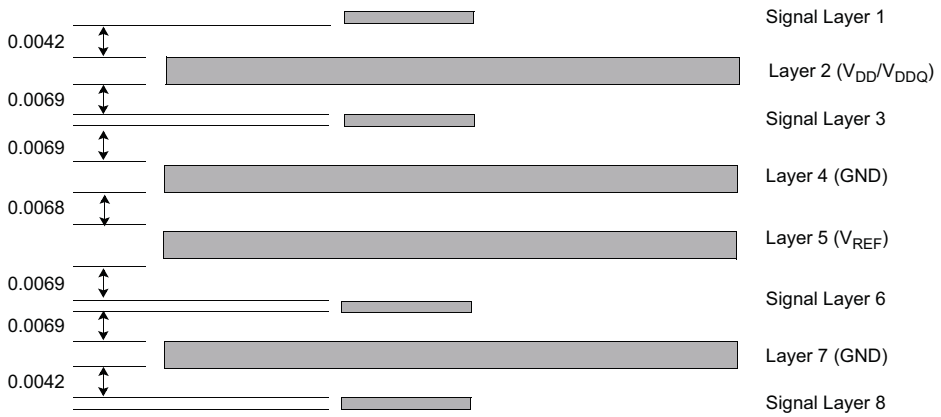
The DIMM printed circuit board design uses eight layers of glass epoxy material. PCBs must contain full ground plane and full power plane layers. The PCB stackup must be designed with 4 mil wide traces.

**Note:** The PCB edge connector contacts shall be gold-plated and not chamfered.

## PCB Electrical Specifications

| Parameter | Min | Max | Units |
|---|---|---|---|
| Trace velocity: S0 (outer layers) | 1.6 | 2.2 | ns/ft |
| Trace velocity: S0 (inner layers) | 2.0 | 2.2 | ns/ft |
| Trace impedance: $Z_0$ (all layers) | 54 | 66 | Ohms |

## Example Eight Layer Stackup




**Note:** This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

### Impedance Measurement Coupons

In order to allow DIMM manufacturers to verify and monitor the trace impedance ($Z_0$) listed above, measurement coupons have been added to each of the Registered DIMM designs. There are four single-ended coupons located on each of the four signal layers, as well as a pair of nets wired on the clock signal layer as a differential pair. These nets are all located on the right side of the DIMM.The single ended nets use the EEPROM wires, while the differential pair has been designed in for this purpose. Each net is two inches in length and has a via near a large ground via placed at the bottom of the DIMM. Each net is clearly labeled 1,2,3,4, or DIFF. A Time Domain Reflectometer (T.D.R.) can be used to perform these measurements (for the differential net, odd mode must be used) before DIMM assembly.



Micron Technology Inc. et al.
Ex. 1017, p. 73

# Timing Budget

The post-register timings on the Registered DIMMs are critical. The following table describes a preliminary post-register timing budget for a typical DDR PC1600 Registered DIMM. This method is 'Time to Vm' that uses the register timing into its specified test load (instead of $t_{CO}$, open circuit) and adds or subtracts the timing into the SDRAM net and loads.

## DIMM Post-Register Timing

| Symbol | Parameter | Time (ns) Set-up | Time (ns) Hold | Notes |
|---|---|---|---|---|
| $t_{CLK}$ | Clock cycle time | 10.0 | N/A | 1 |
| $t_{PD}$ | Maximum time for the signal to exit the register. This is measured from the rising edge of the register clock input (the falling edge of $\overline{CK}$) to the register output into a standard register test load (30 pF to GND, 50 Ohms to $V_{TT}$. | - 2.8 | 1.1 | 1, 2 |
| $t_{NETDELAY}$ | Maximum time for the signal to propagate from the register to any SDRAM. The switching point for a rising edge is VREF ± 100mV. | - 2.0 | 0.5 | 1, 2, 3 |
| $t_{REG}$ | Shift in the register clock in relationship to the SDRAM. The input clocks to the registers and the SDRAM are intended to track, but some error is likely. | - 0.10 | - 0.10 | 1 |
| $t_{IS}$ | Setup time required for the SDRAM inputs | - 1.1 | NA | 1 |
| $t_{IH}$ | Hold time required for the SDRAM inputs | NA | - 1.1 | 1 |
| $t_{Skew*}$ | Clock jitter and skew on the DIMM | - 0.275 | - 0.2 | 1, 4 |
| $t_{SS}$ | Simultaneous Switch effect | - 0.35 | NA | 1, 2 |
| $t_{XTALK}$ | Crosstalk Adder | - 0.10 | NA | |
| **Margin** | | **3.275** | **0.2** | 1 |

1. The timing values shown are consistent with registers available at the time this specification was written. All registers must meet the combined delay values and ensure positive margin, although the specific delay value for each term may vary.
2. The timing values for $t_{NETDELAY}$, $t_{PD}$, and $t_{SS}$, when added together, define the overall delay from clock at the register to the time when the last re-driven signal arrives at the SDRAM (setup time), or earliest re-driven signal changes state after clock (hold time).
3. The $T_{NETDELAY}$ is determined via simulation analysis. The register driver is simulated into both the standard test load and the actual DIMM net and SDRAM loads and the difference is the actual net delay of the DIMM.
4. See the tables below.

### *DIMM Clock Contributions ($t_{Skew}$)

| $t_{Skew}$ for Setup | | Units |
|---|---|---|
| DIMM PLL Jitter | 0.075 | ns |
| DIMM PLL Skew | 0.100 | ns |
| DIMM Clock Net Skew | 0.100 | ns |
| Total | 0.275 | ns |

| $t_{Skew}$ for Hold | | Units |
|---|---|---|
| DIMM PLL Skew | 0.100 | ns |
| DIMM Clock Net Skew | 0.100 | ns |
| Total | 0.200 | ns |



Micron Technology Inc. et al.
Ex. 1017, p. 74

# Serial PD Definition

The Serial Presence Detect function MUST be implemented on the PC DDR SDRAM Registered DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR SDRAM Serial Presence Detect Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices.

The following table is intended to be an **example** of the SPD data for a PC1600 512MB (64M x 72), 184 Pin Registered SDRAM DDR DIMM using two physical banks of 32M x 8 DDR200 devices with 13/10/2 addressing and $\overline{\text{CAS}}$ latencies of 2 and 2.5.

## Serial Presence Detect Example Raw Card Version ‘A’ (Part 1 of 3)

64M x 72 DDR

| Byte # | Description | SPD Entry Value | Serial PD Data Entry (Hexadecimal) | Notes |
|---|---|---|---|---|
| 0 | Number of Serial PD Bytes Written during Production | 128 | 80 | |
| 1 | Total number of bytes in Serial PD Device | 256 | 08 | |
| 2 | Fundamental Memory Type | SDRAM DDR | 07 | |
| 3 | Number of Row Addresses on Assembly | 13 | 0D | |
| 4 | Number of Column Addresses on Assembly | 10 | 0A | |
| 5 | Number of Physical Banks on DIMM | 2 | 02 | |
| 6 - 7 | Data Width of Assembly | x72 | 4800 | |
| 8 | Voltage Interface Level of this Assembly | SSTL 2.5V | 04 | |
| 9 | SDRAM Device Cycle Time at Maximum CL (CLX = 2.5) | 8.0ns | 80 | 1 |
| 10 | SDRAM Device Access Time from Clock at CL=2.5 | ± 0.8ns | 80 | |
| 11 | DIMM Configuration Type | ECC | 02 | |
| 12 | Refresh Rate/Type | 7.8µs/SR | 82 | |
| 13 | Primary SDRAM Device Width | x8 | 08 | |
| 14 | Error Checking SDRAM Device Width | x8 | 08 | |
| 15 | SDRAM Device Attributes: Minimum Clock Delay, Random Column Access | 1 Clock | 01 | |
| 16 | SDRAM Device Attributes: Burst Lengths Supported | 2, 4, 8 | 0E | |
| 17 | SDRAM Device Attributes: Number of Device Banks | 4 | 04 | |
| 18 | SDRAM Device Attributes: $\overline{\text{CAS}}$ Latency | 2, 2.5 | 0C | |
| 19 | SDRAM Device Attributes: $\overline{\text{CS}}$ Latency | 0 | 01 | |
| 20 | SDRAM Device Attributes: $\overline{\text{WE}}$ Latency | 1 | 02 | |
| 21 | SDRAM Module Attributes | Registered with PLL, Differential clock | 26 | |

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{\text{CAS}}$ latency).
2. cc = Checksum Data byte, 00-FF (Hex).
3. “R” = Alphanumeric revision code, A-Z, 0-9.
4. rr = ASCII coded revision code byte “R”.
5. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex).
6. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex).
7. ss = Serial number data byte, 00-FF (Hex).



Micron Technology Inc. et al.
Ex. 1017, p. 75

## Serial Presence Detect Example Raw Card Version 'A' (Part 2 of 3)

64M x 72 DDR

| Byte # | Description | SPD Entry Value | Serial PD Data Entry (Hexadecimal) | Notes |
|---|---|---|---|---|
| 22 | SDRAM Device Attributes: General | $V_{DD} \pm 0.2V$ | 00 | |
| 23 | Minimum Clock Cycle at CLX-0.5 (CL = 2) | 10.0ns | A0 | 1 |
| 24 | Maximum Data Access Time ($t_{AC}$) from Clock at CLX-0.5 (CL = 2) | ± 0.8ns | 80 | |
| 25 | Minimum Clock Cycle Time at CLX-1 (CL = 1.5) | N/A | 00 | |
| 26 | Maximum Data Access Time ($t_{AC}$) from Clock at CLX-1 (CL = 1.5) | N/A | 00 | |
| 27 | Minimum Row Precharge Time ($t_{RP}$) | 20.0ns | 50 | |
| 28 | Minimum Row Active to Row Active Delay ($t_{RRD}$) | 15.0ns | 3C | |
| 29 | Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay ($t_{RCD}$) | 20.0ns | 50 | |
| 30 | Minimum Active to Precharge Time ($t_{RAS}$) | 50.0ns | 32 | |
| 31 | Module Bank Density | 256MB | 40 | |
| 32 | Address and Command Setup Time before Clock | 1.1ns | B0 | |
| 33 | Address and Command Hold Time after Clock | 1.1ns | B0 | |
| 34 | Data/Data Mask Input Setup Time before Data Strobe | 0.6ns | 60 | |
| 35 | Data/Data Mask Input Hold Time after Data Strobe | 0.6ns | 60 | |
| 36 - 40 | Reserved for VCSDRAM | Undefined | 00 | |
| 41 | Minimum Active/Auto-Refresh Time ($t_{RC}$) | 70ns | 86 | |
| 42 | SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh Command Period ($t_{RFC}$) | 80ns | 50 | |
| 43 | SDRAM Device Maximum Cycle Time ($t_{ck}$max) | 12ns | 30 | |
| 44 | SDRAM Device Maximum DQS-DQ Skew time ($t_{DQSQ}$) | 0.6ns | 3C | |
| 45 | SDRAM Device Maximum Read Data Hold Skew Factor ($t_{QHS}$) | 1.0ns | A0 | |
| 46 - 61 | Superset Information (may be used in future) | Undefined | 00 | |
| 62 | SPD Revision | 0 | 00 | |
| 63 | Checksum for Bytes 0 - 62 | Checksum Data | cc | 2 |
| 64 - 71 | Manufacturers' JEDEC ID Code | | | |
| 72 | Module Manufacturing Location | | | |
| | | | | |
| 73 - 90 | Module Part Number | | | 3, 4 |

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{CAS}$ latency).
2. cc = Checksum Data byte, 00-FF (Hex).
3. "R" = Alphanumeric revision code, A-Z, 0-9.
4. rr = ASCII coded revision code byte "R".
5. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex).
6. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex).
7. ss = Serial number data byte, 00-FF (Hex).



Micron Technology Inc. et al.
Ex. 1017, p. 76

## Serial Presence Detect Example Raw Card Version ‘A’ (Part 3 of 3)

64M x 72 DDR

| Byte # | Description | SPD Entry Value | Serial PD Data Entry (Hexadecimal) | Notes |
|---|---|---|---|---|
| 91 - 92 | Module Revision Code | “R” plus ASCII blank | rr20 | 4 |
| 93 - 94 | Module Manufacturing Date | Year/Week Code | yyww | 5, 6 |
| 95 - 98 | Module Serial Number | Serial Number | ssssssss | 7 |
| 99 - 127 | Reserved | Undefined | 00 | |
| 128 - 255 | Open for Customer Use | Undefined | 00 | |

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{\text{CAS}}$ latency).
2. cc = Checksum Data byte, 00-FF (Hex).
3. “R” = Alphanumeric revision code, A-Z, 0-9.
4. rr = ASCII coded revision code byte “R”.
5. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex).
6. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex).
7. ss = Serial number data byte, 00-FF (Hex).



Micron Technology Inc. et al.
Ex. 1017, p. 77

# Product Label

The following label should be applied to all DDR-compatible DIMMs, to describe the performance and reference design attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of eight points should be used, and the number can be printed in one, or more, rows on the label. Note that in addition to this label, the manufacturer's name and DIMM assembly part number shall also appear on the DIMM.

## Format:

PCwwwwm-aabcd-ef

## Where:

wwww: Module Bandwidth
- 1600: 1.6 GB/sec
- 2100: 2.1 GB/sec

m: Module Type
- R = Registered DIMM
- U = Unbuffered DIMM (no registers on DIMM)

aa: SDRAM CAS Latency, with no decimal point (25 = 2.5ns $\overline{CAS}$ Latency)

b: SDRAM minimum $t_{RCD}$ specification (in clocks)

c: SDRAM minimum $t_{RP}$ specification (in clocks)

d: JEDEC SPD Encoding Level used on this DIMM

e: Gerber file used for this design (if applicable)
- A: Reference design for R/C 'A' is used for this assembly
- B: Reference design for R/C 'B' is used for this assembly
- C: Reference design for R/C 'C' is used for this assembly
- E: Reference design for R/C 'E' is used for this assembly
- L: Reference design for R/C 'L' is used for this assembly
- M: Reference design for R/C 'M' is used for this assembly
- N: Reference design for R/C 'N' is used for this assembly
- Z: None of the 'Reference' designs were used on this assembly

f: Revision number of the reference design used:
- 1: 1st revision (1st release)
- 2: 2nd revision (2nd release)
- 3: 3rd revision (3rd release)
- Blank: Not Applicable (used with 'Z' above)

## Example:

PC1600R-25330-A1
is a PC1600 DDR Registered DIMM
with CL = 2.5, $t_{RCD}$ = 3, $t_{RP}$ = 3
using the latest JEDEC SPD Encoding Level 0.0
and produced based on the 'A' raw card Gerber, 1st release



Micron Technology Inc. et al.
Ex. 1017, p. 78

## DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 184 Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to http://www.jedec.org.
2. Click on ‘Free Standards’
3. Type ‘MO-206’ in the box under ‘By Document Number:’
4. Click on ‘Find’
5. Click on ‘Open File’ to open the PDF for this product family.



Micron Technology Inc. et al.
Ex. 1017, p. 79

# Supporting Hardware

## Clock Reference Board

To facilitate the measurement of clock arrival time to the DDR SDRAM for both DDR Unbuffered and Registered SDRAM DIMMs, a ‘Clock Reference Board’ will be released. This board includes the following:

- A frequency synthesizer *to provide 100MHz and 133MHz clocks*
- A clock buffer *to re-drive clocks to the module socket and reference nets*
- A 184P DIMM socket, with three clock inputs wired and *CS and CKE pins tied inactive*
- A ‘Registered’ DIMM reference net *consistent with the JEDEC-approved Registered DIMM Clock Input net structure*
- An ‘Unbuffered’ DIMM reference net *consistent with the JEDEC-approved Unbuffered DIMM clock input structure*
- A clock buffer ‘standard test load’ *to permit characterization of the clock buffer into its test load*

This clock reference board will be made generally available in the industry, and should be used by module producers, as well as system designers, to ensure modules meet the intended clock timings defined in this specification. Every effort will be taken to minimize clock variations and clock skew on these boards.



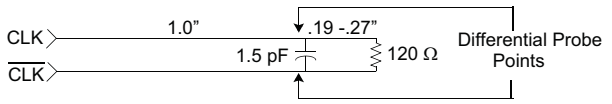
Micron Technology Inc. et al.
Ex. 1017, p. 80

# Application Notes

## Clocking Timing Methodology

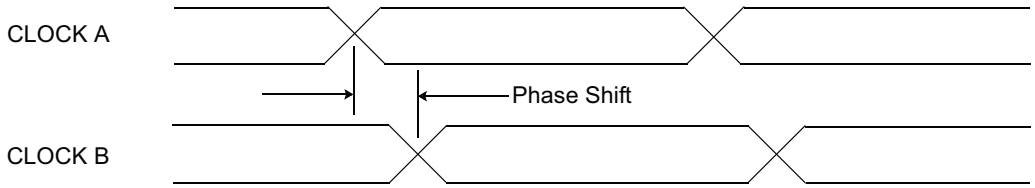
The clock to SDRAM delay is intended to be optimized for high speed operation, while permitting a variety of component layout options. As with Registered DIMMs, the entire clock delay is present between the clock tab pin and the PLL input, and is accomplished via a trace length and a series resistor. This delay should be modeled by the module supplier, to ensure accuracy, if a raw card other than one of the 'reference designs' is utilized. The clock proposed 'Reference Net' below is provided for use during module simulation to ensure an accurate clock delay, since measurement of the delay is impractical (due to the reflections at the clock tab pin).

## Registered DIMM Differential Clock Reference Net




**Note:** Lengths in inches
$Z_0$ = 60.0 Ohms
$t_0$ = 2.2 ns/ft

Timing phase shift in two different DDR clock-pair signals is always measured between the two crossing points of the two-clock pairs as follows:




The clock delay from the input of the PLL to the input of any SDRAM is designed to be 0ns (nominal). The clock arrival time at the PLL input should not be adjusted, although sources of timing variation include PLL input capacitance, padding capacitor and termination resistor tolerances, and DIMM impedance variations (the latter items have a minor affect). Due to these variations, it is possible that there will be a difference between the input of the PLL and the input of the SDRAM. A reasonable target for this variation is +/–100ps (mean value).

The most important factor in clock measurements is to ensure consistent clock arrival times at the SDRAM. The clock reference board Registered DIMM reference net provides the standard net delay for this measurment. The DIMM suppliers must adjust the value of the PLL feedback capacitor to place the clock arrival at the SDRAM on the DIMM within ±100ps of the clock arrival at the Registered DIMM clock reference net (measured as a 'mean', since the PLL and source jitter makes this measurement difficult). This value is a target for DIMM suppliers and does not include worst case contributions of PLL skew, PLL phase error, feedback capacitor variations, and DIMM variations.

On DDR DIMMs, the clock to the register should be in phase with the SDRAM clock. The target range for variation is ±100ps. The actual delay may vary as a result of the input capacitance of the SDRAMs, the register clock input capacitance, PLL output skew variations of the PCB parasitics, and measurement skew (the later two having secondary effects). In the case when the register clocks arrive prior to the SDRAM input clock, this



Micron Technology Inc. et al.
Ex. 1017, p. 81

relationship may be adjusted by increasing the value of the register clock padding capacitor.

All changes defined above require simulation to verify the targeted results. Simulation of the clock nets will allow each DIMM manufacturer to determine the most effective method for achieving a 0ps nominal relationship between the register input clock and the SDRAM input clock. It is critical that this analysis be done in order to maintain the required rise-time characteristics as well as signal integrity at the input of both the SDRAM and the registers. In cases where the register clock cannot be placed in the ideal timing window, post-register timings will need to be adjusted, by the DIMM producer, to ensure robust module operation. (See Post Register Timing Example in this document for summarized clock contributions to the RDIMM budget.)

## Revision Log (Part 1 of 8)

| Revision Info | Page of Revision | Description of Change |
|---|---|---|
| Revision 0.2 | | Initial Release. |
| Revision 0.6 | All | Combined Raw Card A and E into Raw Card A |
| | | Added Raw Card E and K for TSOJ support |
| | 1 | Added x64 to organizations |
| | | Removed support for 1Gbit SDRAMs |
| | 6-14 | Added DM support for all Raw Cards (except x4 based) |
| | | Added CKE1 support to all 2 Bank Raw Cards |
| | | Updated DQS/DM/DQ series resistor to 18 Ohms |
| | | Updated Address and control series resistor to 22 Ohms |
| | | Added 47kOhm pull down resistor to the WP on the EEPROM |
| | | Added several notes for clarification |
| | 15 | Indicated 0ns between PLL input and SDRAM input is ‘nominal’ |
| | | Reversed order of the capacitor and resistor on the register input clock |
| | | Added note indicating location of terminating resistor and padding capacitor |
| | | Updated register clock net resistor termination value |
| | 16 | Fixed typo on location of A10 on the 1:2 register |
| | | Removed note indicating use of CKE1 |
| | 20 | Updated DIMM register use chart |
| | | Changed ‘clock to output’ time specification into a standard test load versus no load. Also updated this value accordingly |
| | | Updated setup and hold times to reflect changes with input slew rate |
| | | Updated 1:2 register to indicate that it is only 13 bits |
| | 21 | Updated DIMM PLL use chart |
| | 22 | Updated max slew rate specification for the PLL |
| | | Added cycle to cycle, half period, and half period cycle to cycle jitter parameters to the PLL specification |
| | | Removed average pulse width symmetry and duty cycle parameters |
| | | Indicated clock frequency deviation for spread spectrum is a negative percentage of the clock |
| | 23-24 | Updated Raw Card Versions<br>--Merged A and D into A<br>--Merged F and J into F<br>--Added E and K |



Micron Technology Inc. et al.
Ex. 1017, p. 82

## Revision Log (Part 2 of 8)

| Revision Info | Page of Revision | Description of Change |
|---|---|---|
| Revision 0.6 Continued | 25 | Updated Input loading matrix (CKE1, DM changes) |
| | | Added target release dates for Design files |
| | | Changed naming convention for gerbers to design files |
| | 33-49 | Add preliminary Raw Card A and B net segment lengths |
| | | Updated DQ/DQS/DM series resistor to 18 Ohms |
| | | Updated address and control series resistor to 22 Ohms |
| | | Move terminating resistor and padding capacitor for all clock inputs to after the pin of the devices |
| | 38-41 | Updated data net structures to accurately reflect current designs |
| | 44 | Added a new net structure for CKE and CS on Raw Cards A, B and F |
| | 49 | Changed $V_{DD}$ and $V_{DDQ}$ power plane locations in stack-up |
| | 50 | Updated post register timing example with up to date data |
| | | Changed example to 'Time to Vm' instead of using tco into no load |
| | | Added clarification notes |
| | 51-52 | Added DIMM SPD example |
| | 56 | Added differential clock reference net |
| | | Updated wording in register to SDRAM clock relationship paragraph |
| Revision 0.9 | 2-3, 5 | Removed WP feature for upper 128 bytes in the EEPROM |
| | 4 | Corrected typo on pins 75 and 76 |
| | 6-16 | Removed 47K resistor on WP<br>Changed DQ/DQS/DM series resistor from 18 ohms to 22 ohms<br>Removed $V_{DDQ}$ to $V_{REF}$ decoupling |
| | 15 | Changed terminating resistor on the register clock net from 120 ohms to 240 ohms |
| | 20 | Updated register $t_{PD}$ Maximum to 2.8 (fixed 2.7 typo) |
| | 22 | Updated PLL specification parameters |
| | 24 | Corrected addressing on Raw Card F |
| | 25 | Updated current design file release schedule |
| | 21-22 | Updated support chip vendor list |
| | 35-48 | Added Design File C and E net structure length information |
| | 36 | Changed register clock net terminating resistor to 240 ohms |
| | 41-44 | Added post register net structure length information for Design Files A and B |
| | 47 | Updated CKE/CS net structure for Design Files C and E in order to reflect nine SDRAM loads per register output |
| | 49 | Changed stack-up: combined $V_{DD}$ and $V_{DDQ}$ planes and added an additional ground plane |
| | 50 | Updated post register timing budget with JEDEC changes to SDRAM input setup and hold specs.<br>Fixed typo on DIMM PLL jitter |
| | 53 | Updated label so that Raw Card type and Revision would follow the last dash |
| | 56 | Updated Registered DIMM differential clock net to one inch from the DIMM connector to loading capacitor representing the PLL input pins |



Micron Technology Inc. et al.
Ex. 1017, p. 83

## Revision Log (Part 3 of 8)

| Revision Info | Page of Revision | Description of Change |
|---|---|---|
| 0.95 | All | Changed all references of PC200 and PC266 at the DIMM level to PC1600 and PC2100 |
| | 2 | Updated $V_{DDSPD}$ description to include operation at 3.3 Volts |
| | 3 | Added $V_{DDSPD}$ functional description |
| | 6-14 | Corrected WP on EEPROM block diagram (placed WP inside the EEPROM) |
| | | Updated $\overline{S}$ to $\overline{CS}$ on all block diagrams |
| | 11-14 | Corrected CB labeling on the D8/26 and D17/35 SDRAM block diagram |
| | 17-18 | Changed CLK and $\overline{CLK}$ to CK and $\overline{CK}$ for consistency |
| | 20 | Added wording about IV driver characteristics and added the JEDEC item # for the registers |
| | 21 | Removed vendor names from the register sourcing |
| | | Added PLL JEDEC item # |
| | 22 | Removed vendor names from the PLL sourcing |
| | 23-24 | Removed # of bank bits from the SDRAM Module Configuration Table |
| | 25 | Updated Design file release schedule according to the latest specification and applicable releases |
| | 29-31 | Updated TSOP stacked thickness |
| | 34-50 | Rounded all net lengths to two decimal places |
| | 35-50 | Indicated that all data for Raw Cards H&K is TBD |
| | 51 | Changed wording to indicate an “Example Eight Layer Stack” |
| | | Added note indicating thicknesses are an example only |
| | | Updated cross section to match production level raw card releases |
| | | Added new section on impedance measurement coupons |
| | 55 | Updated product label to indicate Module Bandwidth instead of SDRAM frequency characteristics |
| 1.0 | 1 | Added full JEDEC website reference |
| | 1-57 | Updated subscripts for consistency |
| | 2 | Added FETEN, and changed address support to A12 only |
| | 3 | Added FETEN<br>Removed A13<br>Removed SSTL parentheses |
| | 4-5 | CK1 and CK2 clocks flagged with note that systems may drive these pins<br>Indicated A13 at the DIMM connector was NC for these raw cards<br>Added WP in parentheses on pin 90<br>BA2 changed to NC(BA2) |
| | 6-14 | Changed EEPROM to Serial PD in the block diagram schematics |
| | 7 | Added overbar to the RESET on the register |
| | 12-14 | Added $\overline{FETEN}$ to block diagrams |
| | 15 | Updated wording in Note 4 to better describe the location of the terminating resistors |
| | 16 | Fixed typos in register pin description |
| | 17-18 | Added $\overline{QFC}$ to SDRAM pin assignments, pin 19 |
| | 19 | Added conditions for output slew rate |



Micron Technology Inc. et al.
Ex. 1017, p. 84

## Revision Log (Part 4 of 8)

| Revision Info | Page of Revision | Description of Change |
|---|---|---|
| 1.0 Continued | 20 | Fixed typo indicating raw card C/E has two banks<br>Added a note to the DIMM PLL Use Table describing clock padding capacitors |
| | 21 | Fixed typo - Raw Card C changed to Raw Card F |
| | 24 | Fixed typo - Raw Card F has one register on CKE1<br>Added note describing FET switch loading<br>Updated DDR RDIMM design file release table to indicate raw card compliance with Revision 1.0 of the specification<br>Added description of C3 raw card version<br>Standardized date format in all “Released on ...” dates in the Notes column |
| | 25-30 | Flipped the PLL so that Pin 1 is on the left bottom side, the same as the design files<br>Moved serial EEPROM to the top right corner to be consistent with design files<br>Moved components to more accurately reflect the design file component placement |
| | 28, 30 | Updated TSOP stack thickness values to encompass industry standard values |
| | 32, 36, 37 | Updated DQ resistor tolerance to ± 5% |
| | 33 | Updated CK[2:0] to CK[0]<br>Updated TL1 value to match design file<br>Revised TL1 value |
| | 34 | Corrected typo on length designators<br>Added min and max values for TL0<br>Corrected TL2 length<br>Added TL3 lengths<br>Corrected TL2 max value for A card and TL1 max and min for B card (PLL to SDRAM)<br>Corrected A and B cards’ min TL2 length (PLL to Register) |
| | 36 | Corrected Total lengths |
| | 41 | Corrected numerous net lengths |
| | 43 | Changed shown lengths to two decimal places |
| | 45 | Changed TL4 min value |
| | 47 | Changed TL0 max value on C card and TL4 max value on E card |
| | 50 | Corrected mistake in cross section to match design file releases<br>Removed extra “example” label |
| | 51 | Updated PC200 DIMM to PC1600 naming convention |
| | 52 | Corrected JEDEC reference for DDR SPDs |
| | 54 | Updated 1 GB/sec typo to 1.6 GB/sec<br>Added comment on DIMM manufacturer’s label |
| | 55 | Updated side width callouts to go to edges of DRAMs<br>Moved components to more accurately reflect the design file component placement |
| 1.1 | i | Deleted “Prepared By IBM, Micron Technology, and Server Works” |
| | ii | Removed disclaimer |
| | iii | Added overbar to CS |
| | 1 | Change description on JEDEC SPD spec to JC 42.5, rev 0<br>Added 64 bit version |



Micron Technology Inc. et al.
Ex. 1017, p. 85

## Revision Log (Part 5 of 8)

| Revision Info | Page of Revision | Description of Change |
|---|---|---|
| 1.1 Continued | 2 | Added A13<br>Changed $\overline{S0}$ - $\overline{S3}$ to $\overline{S}0$ - $\overline{S}3$ |
| | 3 | Changed $\overline{S0}$ - $\overline{S3}$ to $\overline{S}0$ - $\overline{S}3$<br>Added A13; increased row addresses to R13 and column addresses to C12 |
| | 4 | Pin 103 now $\overline{FETEN}$ or NC, pin 167 now A13/NC and pin 115 definition clarified as A12/NC<br>Changed note 1 to permit NC pins 103 and 157 “be connected to inactive signals on the base-board.”<br>Changed $\overline{S0}$ - $\overline{S3}$ to $\overline{S}0$ - $\overline{S}3$ |
| | 6, 7, 10 | $\overline{CS}0$ changed to $\overline{S}0$ and $\overline{S}0$ changed to $\overline{CS}$<br>Clarified $V_{SS}$ TO $V_{DDSPD}$ connection |
| | 8, 9, 11, 14 | Corrected subscript notation on voltages<br>$\overline{CS}0$, $\overline{CS}1$, changed to S0, S1 changed to CS, CS1<br>Clarified $V_{SS}$ to $V_{DDSPD}$ connection<br>Corrected subscript notation on voltages<br>Changed $\overline{FETEN}$ pin from TBD to 103 |
| | 12 | Corrected subscript notation on voltages<br>$\overline{CS}0$, $\overline{CS}1$, changed to $\overline{S}0$, $\overline{S}1$ and $\overline{S}0$, $\overline{S}1$ changed to $\overline{CS}$<br>Clarified $V_{SS}$ to $V_{DDSPD}$ connection<br>Corrected subscript notation on voltages<br>Corrected block diagram error on DM0 AND DQS0<br>Changed $\overline{FETEN}$ pin from TBD to 103 |
| | 13 | Corrected subscript notation on voltages<br>$\overline{CS}0$ - $\overline{CS}1$ changed to $\overline{S}0$ - $\overline{S}1$ and $\overline{S}0$ - $\overline{S}1$ changed to $\overline{CS}$. Also $\overline{S}0$, $\overline{S}1$ and address register outputs incorrectly identified<br>Clarified $V_{SS}$ to $V_{DDSPD}$ connection<br>Corrected subscript notation on voltages<br>Corrected block diagram error on DMO and DQS0<br>Changed $\overline{FETEN}$ pin from TBD to 103 |
| | 16 | Corrected typo showing A1/RA1 assigned to Register 2 rather than Register 1<br>Removed reference to card D<br>Added Card E to 1:2 register group<br>Changed $\overline{CS}0$, $\overline{CS}1$ to $\overline{S}0$, $\overline{S}1$ |
| | 17, 18 | 256MB now 256Mb |
| | 19 | Changed CLK and CLK to CLK and $\overline{CLK}$ |
| | 20 | Clarified use of padding capacitors in note 1 on Card A |
| | 21 | Changed Max $t_{jit}$(hper) to 100ps; was -100ps<br>Added “or by external control $\overline{FETEN}$ at DIMM connector pin 103” |
| | 25-30 | Changed hole spacing to correct JEDEC standard of 128.95/5.077<br>Changed hole size to correct JEDEC standard of 2.50/0.098<br>Changed overall DIMM height to 43.18<br>Showed more realistic PLL physical size |



Micron Technology Inc. et al.
Ex. 1017, p. 86

## Revision Log (Part 6 of 8)

| Revision Info | Page of Revision | Description of Change |
|---|---|---|
| 1.1 Continued | 31, 33 | Changed CK[0] to CK, $\overline{CK}$ |
| | 31, 41, 43, 44, 45, 48 | Added overbar to CS[0:1] |
| | 34 | Corrected errors on clock feedback notation<br>TL0 Min. for cards C, E, H, K changed to 2.93<br>Added note clarifying use of padding capacitor on A-card |
| | 43 | Changed TL7 to reflect max and min values for card A |
| | 51 | Corrected $t_{REG}$ setup time to -0.10 and changed Margin to 3.275 |
| | 52 | Removed reference to JEDEC Ballot JC 42.5-5-99-129 item 894A<br>Added that example was for PC1600 and DDR 200 |
| | 53 | Changed bytes 32 and 33 to reflect correct times -1.2 ns<br>Corrected definition of bytes 34 and 35<br>Changed byte 40 to 61 (in 36-61 row) and added reserved “for VCSDRAM”<br>Added new definitions for bytes 41 through 45<br>Added bytes 46-61 as Superset Information |
| | 56 | Changed card overall height dimension to “nom” - was max<br>Showed more realistic PLL physical size |
| | 58 | Clarified differential probe points and cross-point timing measurements and measurement methodology |



Micron Technology Inc. et al.
Ex. 1017, p. 87

## Revision Log (Part 7 of 8)

| Revision Info | Page of Revision | Description of Change |
|---|---|---|
| 1.2 | 5 | Added 1.2” height to DIMM dimension.<br>Added 1Gb SDRAM to SDRAM supported. |
| | 10, 11, 12, 13 | Added Raw Card L.<br>Changed A12 to A13.<br>Added Note 7. |
| | 14 | Added Raw Card M.<br>Changed A12 to A13.<br>Added Note 6. |
| | 18 | Added Raw Card L to the left table.<br>Added In: A13 - Out: RA13.<br>Changed Note 1 to include 1Gb.<br>Added Note 2 for 1Gb.<br>Added the reference to JC-40 naming conventions and package type. |
| | 19 | Added Table for Raw Card M.<br>Added the reference to JC-40 naming conventions and package type. |
| | 20 | Added 1Gb<br>Changed Pin17 to A13. |
| | 21 | Added 1Gb<br>Changed Pin17 to A13.<br>Changed the reference from the ballot JC-42.3-98-227A to the standard JESD 79. |
| | 22, 23, 24 | Added Raw Card L and M.<br>Added the reference to JC-40 naming conventions and package type. |
| | 26 | Added Raw Card L and M module configurations.<br>Added 1GB and 2GB DIMM configurations for Raw Card L and M. |
| | 28 | Added Raw Card L and M. |
| | 33 | Added Raw Card L and M Component Placement. |
| | 34 | Added Raw Card L Component Placement. |
| | 36, 38, 39, 42, 42, 44, 45 | Added Raw Card L and M and its trace length in the tables. |
| | 48, 49 | Added Raw Card L and M Net Structure Routing for Address and Control. |
| | 52, 54, 55 | Added Raw Card L and M Net Structure Routing for $\overline{CS}$ and CKE |
| | 71 | Added Raw Card L and M to Product label. |
| | | Added 1.2” height drawing. |
| 1.3 | | Removed all Raw Card F/H/K relative comments, Block Diagram and Tables |
| | | Corrected the errata |
| | 11 | Added Raw Card N Block Diagram |
| | 15 | Corrected to One SSTV32852 from two SSTV32852 and added the note |
| | 18, 19 | Added SSTV32852 Register specification and DIMM PLL use |
| | 24 | Changed the Design File name |
| | 36 | Added Net structure routing for PLL feedback Path (Raw Card N) |
| | 40 | Added Net structure routing for PLL Output to Register load (Raw Card N) |



Micron Technology Inc. et al.
Ex. 1017, p. 88

## Revision Log (Part 8 of 8)

| Revision Info | Page of Revision | Description of Change |
|---|---|---|
| 1.3 | 41 | Added Trace Length for Data and DQS Net structure (Raw Card N) |
| | 47 | Added Net Structure Routing for Address and Control (Raw Card N) |
| | 48 | Added Trace Length for Address and Control Net structure (Raw Card N) |
| | 53 | Added Net Structure Routing for $\overline{CS}$ and CKE (Raw Card N) |
| | 54 | Added Trace Length for $\overline{CS}$ and CKE (Raw Card N) |
| | 68 | Added Product label for Raw Card N |



Micron Technology Inc. et al.
Ex. 1017, p. 89

# Exhibit B

# Displayed by Document Type

| NUMBER | JEDEC Engineering Bulletins (JEB ) | PRICE |
|---|---|---|
| JEB 5-A | METHODS OF MEASUREMENT FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS: The purpose of this bulletin is to recommend for use in the rating of semiconductor logic gating microcircuits which use the binary states to represent and process logic information. Both static and dynamic measurements are covered.<br>January 1970; Reaffirmed February 1984 /JEDEC Committee | $56.00 |
| JEB 6 | STANDARD MEASURMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS<br>December 1966; Rescinded October 1984 | |
| JEB 15 | TERMINOLOGY AND METHODS OF MEASUREMENT FOR BISTABLE SEMICONDUCTOR MICROCIRCUITS: This bulletin explains the terminology and methods of measurement for bistable semiconductor microcircuits. It is also intended to be used with the EIA Registration Data Format for semiconductor integrated bistable logic circuits.<br>November 1969 | $100.00 |
| JEB 16 | USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS: This guide defines generalized procedures for the failure analysis of monolithic integrated microelectronic circuits. Although the generalized procedural steps may apply to all microelectronic circuits, additional analysis steps unique to thin/thick film hybrid devices are not covered.<br>July 1970 /JC-14 Committee | $34.00 |
| JEB 17 | USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS<br>November 1970; Rescinded April 1987 | |
| JEB 19 | RECOMMENDED CHARACTERIZATION OF MOS SHIFT REGISTERS: This recommendation applies to MOS Shift Registers. Definitions are given for P-channel registers but are applicable to all CMOS and N-channel with changes in power supply notation.<br>November 1972 /JC-40 Committee | $33.00 |
| JEB 20 | ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS<br>January 1975; Rescinded November 1988 /JC-11 Committee | |
| **NUMBER** | **Tentative Standards (TENTSTD )** | **PRICE** |
| TENTSTD 11 | HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC TYPE PACKAGES: Included in JESD282 and EIA397.<br>July 1973; Rescinded June 1992 | |
| TENTSTD 12 | STANDARD FOR SELENIUM SURGE SUPPRESSORS: The suppresser furnished under this standard shall be a product that has been tested and meets the definitions and minimum requirements specified herein.<br>November 1973 /JC-22.5 Subcommittee | $42.00 |
| **NUMBER** | **JEDEC Specifications (JES )** | **PRICE** |
| JES 2 | TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION: Establishes guideline requirements and quality assurance provisions for gallium arsenide power field-effect transistors (FETs, also know as MESFETs) designed for use in high-reliability space application such as spacecraft communications transmitters. Identifies the electrical parameters, wafer acceptance tests, screening tests, qualification tests, and lot acceptance tests pertinent to power GaAs FETs. Applicable to packaged and chip-carrier parts; portions may not be applicable to unpackaged and unmounted chips.<br>July 1992 /JC-14.7 Subcommittee | $63.00 |



Micron Technology Inc. et al.
Ex. 1017, p. 91

| NUMBER | JEDEC Standards (JESD ) | PRICE |
|---|---|---|
| JESD 1 | **LEADLESS CHIP CARRIER PINOUTS STANDARDIZED FOR LINEARS:** This standard shows how to convert existing DIP pinouts for op-amps, comparators, and D/A convertors, to chip carrier packages.<br>April 1982 / Committee!33JC41 | $34.00 |
| JESD 2 | **DIGITAL BIPOLAR LOGIC PINOUTS FOR CHIP CARRIERS:** This standard provides a chip carrier format for digital devices by defining pin functions and locations for 20, 38, 44, 52, and 68-terminal devices.<br>December 1982 JC-40.1 | $34.00 |
| JESD 3-C | **STANDARD DATA TRANSFER FORMAT BETWEEN DATA PREPARATION SYSTEM AND PROGRAMMABLE LOGIC DEVICE PROGRAMMER:** This standard was developed to prevent the proliferation of data transfer formats that occurred with microprocessor development systems. The focus of the standard is on field programmable devices and their support tools. It is not intended for other types of semicustom logic devices or other types of fabrication or testing equipment.<br>June 1994 / Committee!33JC421 | $54.00 |
| JESD 4 | **DEFINITION OF EXTERNAL CLEARANCE AND CREEPAGE DISTANCES OF DISCRETE SEMICONDUCTOR PACKAGES FOR THYRISTORS AND RECTIFIER DIODES:** This standard defines reference distances between terminals of the device and the external package at specific voltages.<br>November 1983; Reaffirmed January 1991, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee | $31.00 |
| JESD 5 | **MEASUREMENT OF TEMPERATURE COEFFICIENT OF VOLTAGE REGULATOR DIODES:** This standard is designed to define voltage-temperature characteristic measurement techniques and a method of calculation. Although many methods could be defined, this method provides a desired uniformity and lends itself to production testing. Formerly JEDEC Suggested Standard No. 5A<br>February 1982; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee | $31.00 |
| JESD 6 | **MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:** This standard gives a test method for measuring transistor capacitance using a three-terminal bridge which employs a guard-circuit that eliminates the effect of extraneous capacitance.<br>February 1967; Reaffirmed September 1981, April 1999 /JC-25 Committee | $40.00 |
| JESD 7-A | **STANDARD FOR DESCRIPTION OF 54/74HCXXXX AND 54/74HCTXXXX HIGH SPEED CMOS DEVICES:** This standard provides uniformity, multiplicity of sources, eliminate confusion, and ease of device specification and design by users for HC, and HCT CMOS devices. This standard specifies electrical parameters. It also includes appendices listing part numbers.<br>August 1986 JC-40.2 | $100.00 |
| JESD 8- 1 | **ADDENDUM No. 1 to JESD8: INTERFACE STANDARD FOR LOW VOLTAGE TTL-COMPATIBLE (LVTTL) VLSI DIGITAL CIRCUITS**<br>June 1994; Incorporated into JESD8-A, June 1994 /JC-16 Committee | |
| JESD 8- 1-A | **INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS**<br>June 1994; Incorporated into JESD8-A, June 1994 /JC-16 Committee | |
| JESD 8- 2 | **ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS:** This Addendum No. 2 to JEDEC Standard No. 8 provides standard operating voltage and interface levels that can be used by designers and application engineers as they develop and introduce new products. Covers the ECL logic family designated 300K ECL. The 300K ECL family is Voltage and Temperature Compensated, with I/O interface levels compatible with the existing 100K ECL and 101K ECl families.<br>March 1993 /JC-16 Committee | $33.00 |
| JESD 8- 3 | **ADDENDUM No. 3 to JESD8 - GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL, HIGH-** | |



Micron Technology Inc. et al.
Ex. 1017, p. 92

| | | |
|---|---|---|
| | **SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This Addendum No. 3 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices.<br>November 1993 /JC-16 Committee | $31.00 |
| **JESD 8- 4** | **ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This Addendum No. 4 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices that can be a super-set of LVCMOS and LVTTL.<br>November 1993 /JC-16 Committee | $31.00 |
| **JESD 8- 5** | **ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:** This standard defines power supply voltage ranges, dc interface parameters for a high speed, low voltage family of non-terminated digital circuits driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for CMOS-compatible circuits.<br>October 1995 /JC-16 Committee | $33.00 |
| **JESD 8- 6** | **ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL)- A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This standard is a 1.5 volt high performance CMOS-based interface document suitable for high I/O count CMOS and BiCMOS devices operating at frequencies in excess of 200 Mhz.<br>August 1995 /JC-16 Committee | $41.00 |
| **JESD 8- 7** | **ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE), AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:** This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established. Since this migration is driven by both process changes and performance/power, more entries can be expected in supporting required voltage levels. The rapidity of this evolution is expecting to increase because of the same feature sizes expected.<br>February 1997 /JC-16 Committee | $33.00 |
| **JESD 8- 8** | **ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This standard is a result of a major effort by the JC-16 Committee to develop a high performance CMOS-based interface suitable for high speed main memory applications in excess of 125 MHz.<br>August 1996 /JC-16 Committee | $40.00 |
| **JESD 8- 9B** | **ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002.** This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_2 logic switching range, nominally 0 V to 2.5 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. This standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs.<br>May 2002 /JC-16 Committee | $53.00 |
| **JESD 8-11** | **ADDENDUM No. 11 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:** This new standard provides specifications that will be used by several companies in new 1.5 V products designed in 0.12-0.15 um CMOS technologies, and in components that interface with them. The specifications allow limited interoperability with products using the existing JEDEC HSTL specification (JESD8-6).<br>October 2000 /JC-16 Committee | $31.00 |
| **JESD 8-12** | **1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY** | |



Micron Technology Inc. et al.
Ex. 1017, p. 93

| | | |
|---|---|---|
| | **VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:** This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits.<br>May 2001 /JC-16 Committee | |
| **JESD 8-13** | **SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400):** This standard defines the input, output, and termination specifications for differential signaling in the SLVS-400 environment, nominally between 0 and 400 mV. Power supplies other than the nominal 800 mV power for the SLVS interface are not specified.<br>October 2001 /JC-16 Committee | $34.00 |
| **JESD 8-14** | **1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:** This new standard provides specifications that will be used by several companies in new 1.0 V products designed in 0.10-0.12 um CMOS technologies, and in components that interface with them. This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits.<br>December 2001 /JC-16 Committee | $31.00 |
| **JESD 8-15** | **STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18):** This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_18 logic switching range. SSTL_18 is used as the basis for communications between DDR-II SDRAMs and the various support components used with them.<br>October 2002 /JC-16 Committee | $45.00 |
| **JESD 8-B** | **INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS:** This standard (a replacement of JEDEC Standards No. 8, 8-1, 8-1-A, and 8-A) defines dc interface parameters for a family of digital circuits operating from a power supply of nominal 3.0 V/3.3. V and driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for LVTTL-compatible and LVCMOS-compatible circuits.<br>September 1999 /JC-16 Committee | $33.00 |
| **JESD 9-A** | **METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS:** This standard establishes the general requirements and quality assurance provisions that can be specified and met in procuring microelectronics packages and covers, manufactured from matched seal with and without high thermal conductivity base materials, intended for use in fabricating hybrid microelectronics circuits. This document details those minimum requirements necessary for metal packages' use exclusively.<br>April 1987 /JC-13.5 Subcommittee | $63.00 |
| **JESD 10** | **LOW FREQUENCY POWER TRANSISTORS:** This standard consists of a listing of letter symbols, terms, and definitions that are used in power transistors. It also includes information on JEDEC registration procedures, verification tests, and thermal characteristics.<br>September 1981; Reaffirmed April 1999 /JC-25 Committee | $137.00 |
| **JESD 11** | **CHIP CARRIER PINOUTS STANDARDIZED FOR CMOS 4000, HC AND HCT SERIES OF LOGIC CIRCUITS:** This standard indicates the procedures used to convert existing DIP and flat packages for digital parts (SSI & MSI) to chip carrier packages.<br>December 1984 JC-40.2 | $34.00 |
| **JESD 12** | **SEMICUSTOM INTEGRATED CIRCUITS (FORMERLY PUBLISHED AS STANDARD FOR GATE ARRAY BENCHMARK SET):** The purpose of these benchmarks is to provide a common set of high level functions which serve as vehicles for comparing the performance of gate arrays implemented in any technology using any internal structure. These benchmarks effectively provide an unbiased measure of gate array vendors' ability to implement a desired complex function on a particular gate array at a known level of performance. | |



Micron Technology Inc. et al.
Ex. 1017, p. 94

| | | |
|---|---|---|
| | June 1985 / Committee!33JC44 | $36.00 |
| JESD 12-1-B | **ADDENDUM No. 1 to JESD12 - TERMS AND DEFINITIONS FOR GATE ARRAYS AND CELL-BASED INTEGRATED CIRCUITS:** The purpose of this standard is to promote the uniform use of abbreviations, terms, and definitions throughout the semiconductor industry. It is a useful guide for users, manufactures, educators, technical writers, and others interested in the characterization, nomenclature, and classification of semicustom integrated circuits. August 1993 / Committee!33JC44 | $41.00 |
| JESD 12-2 | **ADDENDUM No. 2 to JESD12 - STANDARD FOR CELL-BASED INTEGRATED CIRCUIT BENCHMARK SET:** The purpose of these benchmarks is to provide a common set of high level functions that serve as vehicles for comparing the performance of cell-based ICs implemented in any technology using any internal structure. JESD12-2 extends the gate array benchmark set (JESD12) to cell-based ICs. February 1986 / Committee!33JC44 | $54.00 |
| JESD 12-3 | **ADDENDUM No. 3 to JESD12 - CMOS GATE ARRAY MACROCELL STANDARD:** This standard defines a minimum set of macro cell standards for CMOS gate arrays. A total of 41 macro cell types are addressed, all of which are commonly used by gate array designers to implement Application Specific Integrated Circuits. June 1986 / Committee!33JC44 | $40.00 |
| JESD 12-4 | **ADDENDUM No. 4 to JESD12 - METHOD OF SPECIFICATION OF PERFORMANCE PARAMETERS FOR CMOS SEMICUSTOM INTEGRATED CIRCUITS:** This standard defines how to specify various performance parameters of semicustom ICs, including cell and interconnect propagation delays, input/output levels and capacitance, and power dissipation. April 1987 / Committee!33JC44 | $41.00 |
| JESD 12-5 | **ADDENDUM No. 5 to JESD12 - DESIGN FOR TESTABILITY GUIDELINES:** This standard is intended to provide circuit designers with the information needed to develop complex integrated circuits that can be reliably and economically tested without compromising flexibility. August 1988 / Committee!33JC44 | $100.00 |
| JESD 12-6 | **ADDENDUM No. 6 to JESD12 - INTERFACE STANDARD FOR SEMICUSTOM INTEGRATED CIRCUITS:** This standard defines logic interface levels for CMOS, TTL, ECL, and BiCC inputs and outputs. This standard is intended to provide an industry-wide set of specifications, for Application Specific Integrated Circuit (ASIC) signal inputs and outputs, both necessary and sufficient to define a circuits electrical interfacing with the external environment. JESD12-6 is intended to provide the ASIC manufacturer and user with a common set of signal interface levels. The standard defines interface levels for 5 volt operation. March 1991 / Committee!33JC44 | $36.00 |
| JESD 13-B | **STANDARD SPECIFICATION FOR DESCRIPTION OF B SERIES CMOS DEVICES:** This standard provides for uniformity, multiplicity of sources, elimination of confusion, and ease of device specifications and system design by users. It gives electrical levels and timing diagrams for B Series CMOS devices. May 1980 JC-40.2 | $56.00 |
| JESD 14 | **SEMICONDUCTOR POWER CONTROL MODULES:** Semiconductor Power Control Modules (SPCM) are modules consisting of thyristors or transistors, or both, as the primary controlling elements. Methods of manufacture of semiconductor power control modules include the assembling of individual components and the use of semiconductor hybrids or monolithic processing technologies, or both. November 1986; Reaffirmed June 1992, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee | $43.00 |
| JESD 16-A | **ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM):** This standard was revised to clarify assumptions necessary to estimate AOQ, revise the minimum sample size algorithm, address small sample size concerns, and provide methods for combining groups for AOQ estimation. Derivation of any new methods for combing groups for AOQ estimation. Derivation of any new methods introduced into this document have been provided in annexes. A statistical method is based on confidence interval | |



Micron Technology Inc. et al.
Ex. 1017, p. 95

| | | |
|---|---|---|
| | statistics. A procedure was established for reporting AOQ when the minimum sample size criterion is not met.<br>April 1995 /JC-13 Committee | $54.00 |
| **JESD 17** | **LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999**<br>August 1988; Rescinded February 1999 JC-40.2 | |
| **JESD 18-A** | **STANDARD FOR DESCRIPTION OF FAST CMOS TTL COMPATIBLE LOGIC:** The purpose of this standard is to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. The standard covers specifications for description of '54/74FCTXXXX' series fast CMOS TTL compatible devices.<br>January 1993 JC-40.2 | $56.00 |
| **JESD 19** | **GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A**<br>July 1988; Rescinded July 1995 /JC-13 Committee | |
| **JESD 20** | **STANDARD FOR DESCRIPTION OF 54/74ACXXXXX AND 54/74ACTXXXXX ADVANCED HIGH-SPEED CMOS DEVICES:** This standard describes electrical parameters for this class of CMOS devices.<br>September 1990 JC-40.2 | $137.00 |
| **JESD 21-C** | **CONFIGURATIONS FOR SOLID STATE MEMORIES:** This revision of JESD21 is substantially different from previous issues because it reflects advancement in semiconductor technology and computer design needs. A new class of memory devices, the multiport DRAM (MPDRAM) C also know as 'Video Ram' because of the most common application for the devices C is represented. A new family of SRAMs which addresses the increasing need for high speed is introduced. Additional families of devices in the SOJ and Zip packages are included. The material in this revision is organized primarily by function (ROM, EPROM, SRAM, DRAM, etc.) rather than by technology and word length. Pinouts for SIMM and DIMM are included along with presence detect schemes. A current set of terms has also been included. JESD21-C is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC Council from September 1989. This latest issue has changed to a loose-leaf format and comes in a three-ring binder so that new drawings can be added without requiring a new publication.<br>September 1989 /JC-42 Committee | $150.00 |
| **JESD 21-C AUS** | **ANNUAL UPDATING SERVICE:** The JEDEC Office has generated a mailing list for those who wish to subscribe to updates of this publication. A payment is required for subscription to this updating service.<br>September 2000 | $50.00 |
| **JESD 22-A100-B** | **CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST:** The Cycled Temperature-humidity-bias Life Test is performed for the purpose of evaluating the reliability of nonhermetic packaged solid state devices in humid environments. It employs conditions of temperature cycling, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. The Cycled Temperature-Humidity-Bias Life Test is typically performed on cavity packages (e.g. MQUADs, lidded ceramic pin grid arrays, etc.) as an alternative to JESD22-A101 or JESD22-A110.<br>April 2000 /JC-14.1 Subcommittee | $33.00 |
| **JESD 22-A101-B** | **STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST:** This standard establishes a defined method and conditions for performing a temperature humidity life test with bias applied. The test is used to evaluate the reliability of non-hermetic packaged solid state devices in humid environments. It employs high temperature and humidity conditions to accelerate the penetration of moisture through external protective material or along interfaces between the external protective coating and conductors or other features which pass through it. This revision enhances the ability to perform this test on a device which cannot be biased to achieve very low power dissipation.<br>April 1997 /JC-14.1 Subcommittee | $33.00 |



Micron Technology Inc. et al.
Ex. 1017, p. 96

**JESD 22-A102-C** **ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE:** This test allows the user to evaluate the moisture resistance of nonhermetic packaged solid state devices. The Unbiased Autoclave Test is performed to evaluate the moisture resistance integrity of non-hermetic packaged solid state devices using moisture condensing or moisture saturated steam environments. It is a highly accelerated test which employs conditions of pressure, humidity and temperature under condensing conditions to accelerate moisture penetration through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors passing through it. This test is used to identify failure mechanisms internal to the package and is destructive.

December 2000 /JC-14.1 Subcommittee $31.00

---

**JESD 22-A103-B** **HIGH TEMPERATURE STORAGE LIFE:** The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices. High Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). During the test elevated temperatures (accelerated test conditions) are used without electrical stress applied. This test may be destructive, depending on Time, Temperature and Packaging (if any).

August 2001 /JC-14.1 Subcommittee $31.00

---

**JESD 22-A104-B** **TEMPERATURE CYCLING:** This standard provides a method for determining solid state devices capability to withstand extreme temperature cycling. Changes in this revision include requirements that the worst-case load temperature must reach the specific extremes rather than just requiring that the chamber ambient temperature reach the extremes. This ensures that the test specimens will reach the specified temperature extremes regardless of chamber loading. Definitions are provided for Load, Monitoring Sensor, Worst-Case Load Temperature, and Working Zone. The transfer time has been tightened from 5 minutes to 1 minute. Five new test conditions have been added as well as a caution on test conditions which exceed the glass transition temperature of plastic package solid devices.

July 2000 /JC-14.1 Subcommittee $36.00

---

**JESD 22-A105-B** **POWER AND TEMPERATURE CYCLING:** This Power and Temperature Cycling Test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed. It is intended to simulate worst-case conditions encountered in typical applications. This test method is considered destructive, and is intended primarily for device qualification.

February 1996 /JC-14.1 Subcommittee $31.00

---

**JESD 22-A106-A** **THERMAL SHOCK:** This test is conducted to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes.

April 1995 /JC-14.1 Subcommittee $34.00

---

**JESD 22-A107-A** **SALT ATMOSPHERE:** This standard provides a method for determining solid state devices resistance to corrosion as a result of salt atmosphere exposure. Changes in this revision include making preconditioning optional, making the temperature tolerance in the chamber +3 degrees C and the deposition tolerance +10 grams. This will allow better correlation among test chambers. Added was a requirement for the pH of the salt solution to be maintained between 6.0 and 7.5 at 35 degrees C minimum.

December 1989; Reaffirmed January 1998 /JC-14.1 Subcommittee $31.00

---

**JESD 22-A108-B** **TEMPERATURE, BIAS, AND OPERATING LIFE:** A revised method for determining the effects of bias conditions and temperature, over time, on solid state devices is now available. Revision B of A108 includes low temperature operating life (LTOL) and high temperature gate bias (HTGB) stress conditions, revised cool down requirements for high temperature stress, and a procedure to follow if parts are not tested within the allowed time window.

December 2000 /JC-14.1 Subcommittee $33.00

---

**JESD 22-A109-A** **HERMETICITY:** This revised test method establishes a standard procedure for determining the effectiveness of the seal of hermetically sealed solid state devices. The objective of this revision was to modify the test parameters to reflect current practice and to eliminate the specification of fluorocarbons, banned from use due to environmental concerns.



Micron Technology Inc. et al.
Ex. 1017, p. 97

July 2001 /JC-14.1 Subcommittee $36.00

**JESD 22-A110-B** **HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)** The purpose of this new test method is to evaluate the reliability of nonhermetic packaged solid state devices in humid environments. It employs severe conditions of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

February 1999 /JC-14.1 Subcommittee $33.00

**JESD 22-A112-A** **MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.** See J-STD-020B, published July 2002.

November 1995; Rescinded May 2000

**JESD 22-A113-B** **PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING:** This test method establishes an industry standard preconditioning flow for plastic SMDs (surface mount devices) that is representative of a typical industry multiple solder reflow operation. Plastic SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in-house reliability testing (qualification and reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow.

March 1999 /JC-14.1 Subcommittee $34.00

**JESD 22-A114-B** **ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM):** This test method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined electrostatic Human Body Model (HBM) discharge (ESD). The objective is to provide reliable, repeatable HBM ESD test results so that accurate classifications can be performed.

June 2000 /JC-14.1 Subcommittee $38.00

**JESD 22-A115-A** **ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM):** This method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined Machine Model (MM) electrostatic discharge (ESD). The objective is to provide reliable, repeatable MM ESD test results so that accurate classifications can be performed.

October 1997 /JC-14.1 Subcommittee $38.00

**JESD 22-A117** **ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST:** This method establishes a standard procedure for determining the data cycling endurance and data retention capability of non-volatile memory cells. It is intended as a qualification and monitor test procedure. This test is also applicable to FLASH EEPROM integrated circuits and Erasable Programmable Logic Devices (EPLD) with embedded EEPROM or FLASH memory.

January 2000 /JC-14.1 Subcommittee $33.00

**JESD 22-A118** **ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST:** The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive.

December 2000 /JC-14.1 Subcommittee $34.00

**JESD 22-A120** **TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN INTEGRATED CIRCUITS:** This specification details the procedures for the measurement of characteristic bulk material properties of moisture diffusivity and water solubility in organic materials used in the packaging of IC components. These two material properties are important parameters for the effective reliability performance of plastic packaged ICs after exposure to moisture and subjected to high temperature solder reflow.



Micron Technology Inc. et al.
Ex. 1017, p. 98

June 2001 /JC-14.1 Subcommittee $34.00

**JESD 22-B100-A** **PHYSICAL DIMENSION:** The standard provides a method for determining whether the external physical dimensions of the device are in accordance with the applicable procurement document. This revision includes a change in details to be specified by the procurement document.

April 1990 /JC-14.1 Subcommittee $30.00

**JESD 22-B101** **EXTERNAL VISUAL:** The purpose of this inspection is to verify that the materials, design, construction, markings, and workmanship of the device are in accordance with the applicable procurement document. External visual is a nondestructive test and applicable for all package types. The test is useful for qualification, process monitor, or lot acceptance.

September 1987 /JC-14.1 Subcommittee $30.00

**JESD 22-B102-C** **SOLDERABILITY:** The purpose of this test method is to provide a means of determining the solderability of device package terminations that are intended to be joined to another surface using solder for the attachment. It also provides optional conditions for aging and soldering for the purpose of allowing simulation of the soldering process to be used in the device applications. It provides procedures for dip and look solderability testing of through hole, axial and surface mount devices and reflow simulated use testing for surface mount packages.

September 1998 /JC-14.1 Subcommittee $42.00

**JESD 22-B103-B** **VIBRATION, VARIABLE FREQUENCY:** The Vibration, Variable Frequency Test Method is intended to determine the ability of component(s) to withstand moderate to severe vibration as a result of motion produced by transportation or filed operation of electrical equipment. This is a destructive test that is intended for component qualification.

June 2002 /JC-14.1 Subcommittee $41.00

**JESD 22-B104-B** **MECHANICAL SHOCK:** This test is intended to determine the suitability of component parts for use in electronic equipment that may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shock of this type may disturb operating characteristics, particularly if the shock pulses are repetitive. This is a destructive test intended for device qualification. It is normally applicable to cavity-type packages.

May 2001 /JC-14.1 Subcommittee $31.00

**JESD 22-B105-B** **LEAD INTEGRITY:** This test method provides various tests for determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly. For hermetic packages it is rececommend that this test be followed by hermeticity tests in accordance with Test Method A109 to determine if there are any adverse effects from the stresses applied to the seals as well as to the leads. These tests, including each of its test conditions, is considered destructive and is only recommended for qualification testing. This test is applicable to all through-hole devices and surface-mount devices requiring lead forming by the user.

January 1999 /JC-14.1 Subcommittee $41.00

**JESD 22-B106-B** **RESISTANCE TO SOLDERING TEMPERATURE FOR THROUGH-HOLE MOUNTED DEVICES:** This method established a standard procedure for determining whether through-hole solid state devices can withstand the effects of the temperature to which they will be subject during soldering of their leads. This revision updates the references to currently military standards.

February 1999 /JC-14.1 Subcommittee $31.00

**JESD 22-B107-A** **MARKING PERMANENCY:** The purpose of this test method is to verify that the markings on solid state semiconductor devices will not become illegible when subjected to solvents or cleaning solutions commonly used during the removal of solder flux residue from printed circuit board assembly process. The primary reasons for revising this test method are: 1) eliminate chemicals containing carcinogens; 2) reduce CFCs and 3) to align with MIL-STD-883 basic document.

September 1995 /JC-14.1 Subcommittee $33.00

**JESD 22-B108**



Micron Technology Inc. et al.
Ex. 1017, p. 99

| | | |
|---|---|---|
| | **COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES:** The purpose of this test is to measure the deviation of the leads from the coplanarity for surface-mount semiconductor devices.<br>November 1991 /JC-14.1 Subcommittee | $30.00 |
| **JESD 22-B110** | **SUBASSEMBLY MECHANICAL SHOCK:** The new test method JESD22-B110 provides guidance for in-situ testing of mechanical shock resistance of components as mounted in a subassembly. Using terms, procedures, and test levels in common with JESD22-B104B, this test method provides a range of test level options to improve test applicability and compatibility with fragility test procedures. Test procedures are detailed, including test card and fixture needs, test tolerances, test documentation, component preparation, and definition of terms.<br>May 2001 /JC-14.1 Subcommittee | $34.00 |
| **JESD 22-B116** | **WIRE BOND SHEAR TEST:** This test method establishes a standard procedure for determining the strength of an integrated circuit wire bond by shearing the wire from the surface it is bonded to and measuring the force required. This method serves as an alternative to pulling the wire vertically until the wire separates from one of it's two bonded surfaces. It also provides guidelines for determining an appropriate minimum shear force for gold balls on aluminum alloy bonding surfaces.<br>July 1998 /JC-14.1 Subcommittee | $38.00 |
| **JESD 22-B117** | **BALL GRID ARRAY (BGA) BALL SHEAR:** Test method for BGA Ball Shear. This test method has ball shear terms and definitions; apparatus description; the BGA ball shear procedure; and BGA ball shear failure modes and their criteria. Where applicable, figures are included to show the apparatus and six typical failure modes.<br>July 2000 /JC-14.1 Subcommittee | $34.00 |
| **JESD 22-C100-A** | **HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999**<br>April 1990; Rescinded November 1999 /JC-14.1 Subcommittee | |
| **JESD 22-C101-A** | **FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS:** This new test method describes a uniform method for establishing charged-device model electrostatic discharge withstand thresholds. The charged-device-model simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing. One of many examples is a device sliding down a shipping tube hitting a metal surface. Discharges to devices on unterminated circuit assemblies are also well-modeled by the CDM test. DM ESD events not only reduce assembly yields but can also produce device damage that goes undetected by factory test and later is the cause of a latent failure.<br>June 2000 /JC-14.1 Subcommittee | $34.00 |
| **JESD 23** | **TEST METHODS AND CHARACTER DESIGNATION FOR LIQUID CRYSTAL DEVICES:** This standard specifies a collection of procedures for testing and character designation of liquid crystal devices.<br>May 1982 | $50.00 |
| **JESD 24** | **POWER MOSFETS:** This standard contains a listing of terms and definitions and letter symbols; a description of established procedures that are followed in the assignment of semiconductor-industry-type designations to power transistors; electrical verification test; thermal characteristics; and a user's guide.<br>July 1985 /JC-25 Committee | $63.00 |
| **JESD 24- 1** | **ADDENDUM No. 1 to JESD24 - METHOD FOR MEASUREMENT OF POWER DEVICE TURN-OFF SWITCHING LOSS:** Describes the method of a typical oscilloscope waveform and the basic test circuit employed in the measurement of turn off loss for bipolar, IGBT and MOSFET power semiconductors. This method can be used as a standard for evaluating power semiconductor turn-off switching loss capability and defines standard terminology that should be referenced within the electronic industry.<br>October 1989; Reaffirmed April 1999 /JC-25 Committee | $34.00 |



Micron Technology Inc. et al.
Ex. 1017, p. 100

| | | |
|---|---|---|
| JESD 24- 2 | **ADDENDUM No. 2 to JESD24 - GATE CHARGE TEST METHOD:** This addendum establishes a method for measuring power device gate charge. A gate charge test is performed by driving the device gate with a constant current and measuring the resulting gate voltage response. Constant gate current scales the gate voltage, a function of time, to a function of coulombs. The slope of the generated response reflects the active device capacitance as it varies during the switching transition . Gate charge measurements are useful for characterizing the large signal switching performance of power MOS and IGBT devices. Developed over a four year span by the JEDEC JC-25 Committee, the method defines a repeatable means of measuring the widely published Qgd charge values.<br>January 1991; Reaffirmed April 1999 /JC-25 Committee | $34.00 |
| JESD 24- 3 | **ADDENDUM No. 3 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD):** The purpose of this test method is to measure the thermal impedance of the MOSFET under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity if the forward voltage drop of the source-drain is used as the junction temperature indicator. This method is particularly suitable to enhancement mode, power MOSFETs having relatively long thermal response times. This test method may be used to measure the thermal response of junction to a heating pulse, to ensure proper die mountdown to its case, or the dc thermal resistance, by the proper choice of the pulse duration and magnitude if the heating pulse.<br>November 1990; Reaffirmed April 1999 /JC-25 Committee | $40.00 |
| JESD 24- 4 | **ADDENDUM No. 4 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR BIPOLAR TRANSISTORS (DELTA BASE-EMITTER VOLTAGE METHOD):** The purpose of this test method is to measure the thermal impedance of the Bipolar Transistor under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the base-emitter voltage is used as the junction temperature indicator. This test method is used to measure the thermal response of the junction to a heating pulse. Specifically, the test may be used to measure dc thermal resistance, and to ensure proper die mountdown to its case. This is accomplished through the appropriate choice of pulse duration and heating power magnitude.<br>November 1990; Reaffirmed April 1999 /JC-25 Committee | $40.00 |
| JESD 24- 5 | **ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD:** This method describes a means for testing the ability of a power switching device to withstand avalanche breakdown.<br>August 1990; Reaffirmed April 1999 /JC-25 Committee | $31.00 |
| JESD 24- 6 | **ADDENDUM No. 6 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS:** This standard describes in detail the method for thermal measurements of Insulated Gate Bipolar Transistors (IGBTs) and is suitable for use both in manufacturing and application of the devices. The method covers both thermal transient and thermal equilibrium measurements for manufacturing process control and device characterization purposes. Properly implemented, JESD24-6 provides a basis for obtaining realistic thermal parametric values that will benefit supplier's internal effectiveness and will be useful to the design and manufacturer of reliable IGBT circuits.<br>October 1991; Reaffirmed April 1999 /JC-25 Committee | $40.00 |
| JESD 24- 7 | **ADDENDUM No. 7 to JESD24 - COMMUTATING DIODE SAFE OPERATING AREA TEST PROCEDURE FOR MEASURING dv/dt DURING REVERSE RECOVERY OF POWER TRANSISTORS:** Defines methods for verifying the diode recovery stress capability of power transistors.<br>August 1982; Reaffirmed April 1999 /JC-25 Committee | $33.00 |
| JESD 24- 8 | **ADDENDUM No. 8 to JESD24 - METHOD FOR REPETITIVE INDUCTIVE LOAD AVALANCHE SWITCHING:** Determines the repetitive inductive avalanche switching capability of power switching transistors.<br>August 1992; Reaffirmed April 1999 /JC-25 Committee | $33.00 |
| JESD 24- 9 | **ADDENDUM No. 9 to JESD24 - SHORT CIRCUIT WITHSTAND TIME TEST METHOD:** Test method to determine how long a device can survive a short circuit condition with a given drive level.<br>August 1992; Reaffirmed April 1999 /JC-25 Committee | $33.00 |



Micron Technology Inc. et al.
Ex. 1017, p. 101

| | | |
|---|---|---|
| JESD 24-10 | **ADDENDUM No. 10 to JESD24 - TEST METHOD FOR MEASUREMENT OF REVERSE RECOVERY TIME trr FOR POWER MOSFET DRAIN-SOURCE DIODES:** Test method to measure the reverse recovery characteristics of the drain source diode of a power MOSFET.<br>August 1994; Reaffirmed April 1999 /JC-25 Committee | $34.00 |
| JESD 24-11 | **ADDENDUM No. 11 to JESD24 - POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD:** Test method to measure the equivalent resistance of the gate to source of a power MOSFET.<br>August 1996; Reaffirmed March 2001 /JC-25 Committee | $31.00 |
| JESD 25 | **MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:** This standard provides a test method and definition for small-signal conditions at microwave frequencies.<br>November 1972; Reaffirmed September 1981, April 2000 /JC-25 Committee | $50.00 |
| JESD 26-A | **GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001**<br>April 1990; Rescinded July 2001 /JC-13.2 Subcommittee | |
| JESD 27 | **CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES:** The intent of this standard is to be a guide in the manufacture and procurement of ceramic packages, especially for the hybrid industry. Manufacturers or ceramic packages and procuring activities for these packages will now be able to use this document as the means for agreement in the imposition of minimum requirements in qualification, screening, and quality conformance.<br>August 1993 /JC-13 Committee | $60.00 |
| JESD 28-1 | **N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS:** This addendum provides data analysis examples useful in analyzing MOSFET n-channel hot-carrier- induced degradation data. This addendum to JESD28 (Hot carrier n-channel testing standard) suggests hot-carrier data analysis techniques.<br>September 2001 /JC-14.2 Subcommittee | $36.00 |
| JESD 28-A | **A PROCEDURE FOR MEASURING N-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS:** This document describes an accelerated test for measuring the hot-carrier-induced degradation of a single n-channel MOSFET using dc bias. The purpose of this document is to specify a minimum set of measurements so that valid comparisons can be made between different technologies, IC processes, and process variations in a simple, consistent and controlled way. The measurements specified should be viewed as a starting point in the characterization and benchmarking of the transistor manufacturing process.<br>December 2001 /JC-14.2 Subcommittee | $40.00 |
| JESD 29-A | **FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996.**<br>July 1996 /JC-14.3 Subcommittee | |
| JESD 30-B | **DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES:** The package designators in this standard have been updated and are in general agreement with the latest publications and proposals of EIAJ, IEC, and MIL-STD-1835. Important additions to the standard include a package-specific features data field to describe package thickness and lead pitch, quick-connect and screw terminals, and TAB devices. Included are standard industry acronyms and abbreviations such as DIP, FP, PLCC, PGA, SO-G, and SO-J and new descriptors describing fine or shrink pitch, thin shrink, thin or low profile and others.<br>April 1995 /JC-10 Committee | $48.00 |
| JESD 31-B | **GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES:** This publication identifies the general requirements for Distributors that supply Commercial and Military products. This document identifies the general requirements for Distributors that supply Commercial and Military products. Now updated to provide clarification, these requirements apply to all discrete semiconductors, integrated circuits and hybrids, whether packaged or in wafer/die form, manufactured by all component Manufacturers. JESD31-B assures damage-free components without degradation to component reliability throughout the entire supply channel. | |



Micron Technology Inc. et al.
Ex. 1017, p. 102

| | | |
|---|---|---|
| | October 2002 /JC-14.4 Subcommittee | $47.00 |
| **JESD 32** | **STANDARD FOR CHAIN DESCRIPTION FILE:** This document provides a standard for describing an ISP device chain, opening up the possibility for third-party companies to provide value-added ISP software. The purpose of the Chain Description File is to describe the configuration of a programming chain made up of devices that can be connected in some serial fashion. No assumptions are made about how data is used by the device, nor about the nature or configuration of the control signals that affect programming. It will support devices configured using electrically-erasable(EE), Flash, SRAM, or any other reconfigurable cell. For devices programmed via an IEEE programmable devices in the same chain. | |
| | June 1996 / Committee!33JC421 | $40.00 |
| **JESD 33-A** | **STANDARD METHOD FOR MEASURING AND USING THE TEMPERATURE COEFFICIENT OF RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE:** This revised standard provides the results of an interlaboratory experiment to determine the reproducibility and repeatability of the methods for measuring the temperature coefficient of resistance (TCR) of a metallization and for using the TCR to determine the temperature rise in a metal line due to joule heating and to use the metal line to monitor its temperature. It provides a list of potential measurement interference's to be considered in determining the TCR of a metallization and provides a number of precautions in the use of the TCR to measure joule heating and to monitor ambient temperature. This standard is designed for both wafer and package-level measurements. | |
| | October 1995 /JC-14.2 Subcommittee | $48.00 |
| **JESD 34** | **FAILURE-MECHANISM-DRIVEN RELIABILITY QUALIFICATION OF SILICON DEVICES:** This document applies to the reliability qualification of new or changed silicon devices, and their materials or manufacturing processes. Does not address qualification of product quality or functionality. Provides an alternative to traditional stress-driven qualification. | |
| | March 1993 /JC-14.2 Subcommittee | $36.00 |
| **JESD 35-1** | **ADDENDUM No. 1 to JESD35 - GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:** This addendum expands the usefulness of the Standard 35 (JESD35) by detailing the various sources of measurement error that could effect the test results obtained by the ramped tests described in JESD35. Each source of error is described and its implications on test structure design is noted. This addendum can be used as a guide when designing test structures for the qualification and characterization of thin oxide reliability, specifically, by implementing accelerated voltage or current ramp tests. | |
| | September 1995 /JC-14.2 Subcommittee | $45.00 |
| **JESD 35-2** | **ADDENDUM No. 2 to JESD35 - TEST CRITERIA FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:** This addendum includes test criteria to supplement JESD35. JESD35 describes procedures developed for estimating the overall integrity of thin oxides in the MOS Integrated Circuit manufacturing industry. Two test procedures are included in JESD35: a Voltage-Ramp (V-Ramp) and a Current-Ramp (J-Ramp). As JESD35 became implemented into production facilities on a variety of test structures and oxide attributes, a need arose to clarify end point determination and point out some of the obstacles that could be overcome by careful characterization of the equipment and test structures. | |
| | February 1996 /JC-14.2 Subcommittee | $36.00 |
| **JESD 35-A** | **PROCEDURE FOR WAFER-LEVEL-TESTING OF THIN DIELECTRICS:** The revised JESD35 is intended for use in the MOS Integrated Circuit manufacturing industry. It describes procedures developed for estimating the overall integrity and reliability of thin gate oxides. Three basic test procedures are described, the Voltage-Ramp (V-Ramp), the Current-Ramp (J-Ramp) and the new Constant Current (Bounded J-Ramp) test. Each test is designed for simplicity, speed and ease of use. The standard has been updated to include breakdown criteria that are more robust in detecting breakdown in thinner gate oxides that may not experience hard thermal breakdown. | |
| | April 2001 /JC-14.2 Subcommittee | $60.00 |
| **JESD 36** | **STANDARD DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE, 5 V TOLERANT CMOS LOGIC DEVICES:** This standard outlines the standard dc specifications, test conditions, and test loading for logic products that are designed to tolerate input and output voltages which | |



Micron Technology Inc. et al.
Ex. 1017, p. 103

exceed the device's power supply. More specifically this standardizes 5 V - tolerant logic prducts that run from 'low voltage' (2.7 V to 3.6 V) power supplies. Products that meet this standard can be used to effectively interface between LVCMOS/LVTTL and 5 V TTL buses, bridging the gap between low-voltage and 5 V TTL busses.

June 1996 /JC-40 Committee $38.00

---

**JESD 37** **STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD:** This standard details techniques for estimating the values of a two parameter lognormal distribution from complete lifetime data (all samples in an experiment have failed) or singly right-censored lifetime data (the experiment have failed) or singly right-censored lifetime data gathered from rapid stress test; however, not all types of failure data can be analyzed with these techniques.

October 1992 /JC-14.2 Subcommittee $52.00

---

**JESD 38** **STANDARD FOR FAILURE ANALYSIS REPORT FORMAT:** This standard is to promote unification of content and format of semiconductor device failure-analysis reports so that reports from diverse laboratories may be easily read, compared, and understood by customers. Additional objectives are to ensure that reports can be easily ready by users, satisfactorily reproduced on copying machines, adequately transmitted by telefax, and conveniently stored in standard filing cabinets.

December 1995 /JC-14.6 Subcommittee $36.00

---

**JESD 39-A** **QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.**

June 1997 /JC-14.4 Subcommittee

---

**JESD 40** **PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994**

July 1994 /JC-13 Committee

---

**JESD 41** **REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.**

May 1995; Rescinded June 2002 /JC-22.1 Subcommittee

---

**JESD 42** **REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.**

March 1994 /JC-13 Committee

---

**JESD 43** **COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996.**

November 1996 /JC-14.4 Subcommittee $36.00

---

**JESD 45** **MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: Rescinded June 2002. Replaced by JESD282-B.**

December 1994; Rescinded June 2002 /JC-22.2 Subcommittee

---

**JESD 46-B** **CUSTOMER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS:** This standard establishes procedures to notify customers of semiconductor product and process changes. Requirements include: documentation; procedures for classification, notification and customer response; content; and records. Documentation of a suppliers change notification system should set clear and understandable expectations for both the originators of the change and their end customers.

August 2001 /JC-14.4 Subcommittee $31.00

---

**JESD 47-A** **STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS:** This standard establishes a standardized suite of tests, their recommended test conditions and sample sizes for the qualification of new and changed integrated circuits. The table of tests have been updated to reflect the latest JEDEC test methods, such as EEPROM Program/Erase and data Retention JESD22-A117 and Electrostatic Discharge - Charged Device Model JESD22-C101.

November 2001 /JC-14.3 Subcommittee $45.00

---

**JESD 48-A** **PRODUCT DISCONTINUANCE:** This standard establishes the requirements for timely customer notification of planned product discontinuance, which will assist customers in managing



Micron Technology Inc. et al.
Ex. 1017, p. 104

| | | |
|---|---|---|
| | end-of-life supply, or to transition on-going requirements to alternate products.<br>August 2001 /JC-14.4 Subcommittee | $30.00 |
| **JESD 49** | **PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD):** This standard was created to facilitate the procurement and use of high reliability semiconductor microcircuits or discrete devices provided in bare die form, commonly known as Known Good Die (KGD).<br>February 1996 /JC-13 Committee | $38.00 |
| **JESD 50** | **SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION:** This standard applies to the identification and control of Maverick Product that can occur during fabrication, assembly, packaging, or test of any electronic component. It can be implemented for an entire product line or to segregate product that has a higher probability of adversely impacting quality or reliability.<br>December 1995 /JC-14.3 Subcommittee | $33.00 |
| **JESD 51** | **METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE)** This standard and its subsequent addendum's, provides a standard for thermal measurement that, if followed fully, will provide correct and meaningful data that will allow for determination of junction temperature for specific conditions. The data can be used for package design evaluation, device characterization and reliability predictions.<br>December 1995 /JC-15 Committee | $33.00 |
| **JESD 51- 1** | **INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE):** The purpose of this test method is to define a standard Electrical Test Method (ETM) that can be used to determine the thermal characteristics of single integrated circuit devices housed in some form of electrical package. This method will provide a basis for comparison of different devices housed in the same electronic package or similar devices housed in different electronic packages.<br>December 1995 /JC-15 Committee | $54.00 |
| **JESD 51- 2** | **INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR):** This document outlines the environmental conditions necessary to ensure accuracy and repeatability for a standard junction-to-ambient thermal resistance measurement in natural convection.<br>December 1995 /JC-15 Committee | $40.00 |
| **JESD 51- 3** | **LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:** This standard describes design requirements for a single layer, leaded surface mount integrated circuit package thermal test board. The standard describes board material and geometry requirements, minimum trace lenghts, trace thickness, and routing considerations. Application includes still air and moving air thermal tests.<br>August 1996 /JC-15.1 Subcommittee | $34.00 |
| **JESD 51- 4** | **THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP):** This guideline describes design requirements for wire bond type semiconductor chips to be used for thermal resistance listing of IC packages. This document provides specific guidelines for chip design but allows flexibility in the materials and layout requirements.<br>February 1997 /JC-15.1 Subcommittee | $38.00 |
| **JESD 51- 5** | **EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES WITH DIRECT THERMAL ATTACHMENT MECHANISMS:** This extension of the thermal standards provides a standard fixture for direct attach type packages such as deep-downset of thermally tabbed packages. This specification provides additional design detail for use in developing thermal test boards with application to these package types. This document is in addition to and not replacement for the design specifications in other standards.<br>February 1999 /JC-15.1 Subcommittee | $31.00 |
| **JESD 51- 6** | **INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR):** This standard specifies the environmental conditions for determining thermal performance of an integrated circuit device in a forced convection environment when mounted on a standard thermal test board. | |



Micron Technology Inc. et al.
Ex. 1017, p. 105

| | | |
|---|---|---|
| | March 1999 /JC-15.1 Subcommittee | $31.00 |
| **JESD 51- 7** | **HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:** This fixturing further defines the environment for thermal test of packaged microelectronic devices. Its function is to provide an alternate mounting surface for the analysis of heat flow in electronic components. The objective of the standard is to provide a high effective thermal conductivity mounting surface that can be compared equally against standard tests done in different laboratories with typical variations of less than or equal to 10%. | |
| | February 1999 /JC-15.1 Subcommittee | $34.00 |
| **JESD 51- 8** | **INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - JUNCTION-TO-BOARD:** This specification should be used in conjunction with the overview document JESD51, Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device) [1] and the electrical test procedures described in JESD51-1, 'Integrated Circuit Thermal Measurement Method (Single Semiconductor Device' [2. The environmental conditions described in this document are specifically designed for testing of integrated circuit devices that are mounted on standard test boards with two internal copper planes [3]. This standard is not applicable to packages that have asymmetric heat flow paths to the printed board caused by such thermal enhancements as fused leads (leads connected to the die pad) or power style packages with the exposed heat slug on one side of the package. | |
| | October 1999 /JC-15.1 Subcommittee | $38.00 |
| **JESD 51- 9** | **TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of ball grid array (BGA) and land grid array (LGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-9 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families. | |
| | July 2000 /JC-15.1 Subcommittee | $41.00 |
| **JESD 51-10** | **TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Dual-Inline Packages (DIP) and Single-Inline Packages (SIP). It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-10 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families. | |
| | July 2000 /JC-15.1 Subcommittee | $38.00 |
| **JESD 51-11** | **TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENT:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Pin Grid Array (PGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-11 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families. | |
| | June 2001 /JC-15.1 Subcommittee | $40.00 |
| **JESD 52** | **STANDARD FOR DESCRIPTION OF LOW VOLTAGE TTL-COMPATIBLE CMOS LOGIC DEVICES:** This standard describes dc interface specifications and test environment for these devices that operate with 2.7 V to 3.6 V power supplies. The goal is to provide a consistent set of dc specifications for reference by logic suppliers and users alike. | |
| | November 1995 /JC-40 Committee | $38.00 |
| **JESD 53** | **MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: Rescinded, October 2002** | |



Micron Technology Inc. et al.
Ex. 1017, p. 106

January 1996; Rescinded October 2002 /JC-13.2 Subcommittee

| | | |
|---|---|---|
| JESD 54 | **STANDARD FOR DESCRIPTION OF 54/74ABTXXX AND 74BCXXX TTL-COMPATIBLE BiCMOS LOGIC DEVICES:** The purpose is to provide a standard of BiCMOS Logic series specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.<br>February 1996 /JC-40 Committee | $54.00 |
| JESD 55 | **STANDARD FOR DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE BiCMOS LOGIC DEVICES:** The purpose is to provide a standard of BiCMOS Logic series specifications for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.<br>May 1996 /JC-40 Committee | $42.00 |
| JESD 57 | **TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION:** This test method defines requirements and procedures for ground simulation and single event effects (SEE) and implementation of the method in testing integrated circuits. This standard is valid when using a cyclotron or Van de Graaff accelerator. Microcircuits under test must be delidded. The ions used at the facilities have an atomic number Z > 2. It does not apply to SEE testing that uses protons, neutrons, or other lighter particles. This standard is designed to eliminate any misunderstanding between users of the method and test facilities, to minimize delays, and to promote standardization of testing and test data.<br>December 1996 /JC-13.4 Subcommittee | $60.00 |
| JESD 59 | **BOND WIRE MODELING STANDARD:** This standard describes the modeling of a bond wire from an integrated circuit (IC) die to a package lead in a ball or wedge type wire bond configuration.<br>June 1997 /JC-15 Committee | $38.00 |
| JESD 60 | **A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION AT MAXIMUM GATE CURRENT UNDER DC STRESS:** This method establishes a standard procedure for accelerated testing of the hot-carrier-induced change of a p-channel MOSFET. The objective is to provide a minimum set of measurements so that accurate comparisons can be made.<br>April 1997 /JC-14.2 Subcommittee | $38.00 |
| JESD 61 | **ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE:** This standard describes an algorithm for the execution of the isothermal test, using computer-controlled instrumentation. The primary use of this test is for the monitoring of microelectronic metallization lines at water level (1) in process development, to evaluate process options, (2) in manufacturing, to monitor metallization reliability and (3) to monitor/evaluate process equipment. While it is developed as a fast WLR test, it can also be an effective tool for controlling the uniformity of stress applied during the standard package level electromigration test.<br>April 1997 /JC-14.2 Subcommittee | $42.00 |
| JESD 62-A | **OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS:** This revision incorporates recommended tests and an example of a statistics-based method for identifying and removing outliers, i.e., parts that meet supplier specifications and end-user requirements but lie outside typical distribution limits. Outlier product can occur during fabrication, assembly, packaging, or test of any electronic components.<br>May 2002 /JC-14.3 Subcommittee | $43.00 |
| JESD 63 | **STANDARD METHOD FOR CALCULATING THE ELECTROMIGRATION MODEL PARAMETERS FOR CURRENT DENSITY AND TEMPERATURE:** This method provides procedures to calculate sample estimates and their confidence intervals for the electromigration model parameters of current density and temperature. The model parameter for current density is the exponent (n) to which the current density is raised in Black's equation. The parameter for temperature is the activation energy for the electromigration failure process.<br>February 1998 /JC-14.2 Subcommittee | $54.00 |
| JESD 64-A | **STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES WITH 3.6 V CMOS TOLERANT INPUTS AND OUTPUTS:** The purpose is to provide a standard for 2.5 V nominal supply | |



Micron Technology Inc. et al.
Ex. 1017, p. 107

| | | |
|---|---|---|
| | voltage logic devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This specification provides for compatibility between devices operating between either the Standard Range of 1.8 V to 2.7 V or the optional Extended Range of 1.65 V to 2.7 V supply voltages, as well as over-voltage tolerance with devices operating at 3.6 V.<br>October 2000 /JC-40 Committee | $33.00 |
| **JESD 65-A** | **DEFINITION OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES:** JESD65A is an update to JESD65 that includes new definitions for static phase offset, half-period jitter, duty-cycle jitter, phase locked, frequency locked and others. These definitions are used and needed by PLL device vendors to define component characteristics and provide uniform data sheet specifications. These definitions are specifically targeted toward PLL devices used in DDR (Double Data Rate) applications.<br>August 2001 JC-40.3 | $40.00 |
| **JESD 66** | **TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE:** This standard is applicable to Thyristor Surge Protective Devices. It describes terms and definitions and explains methods for verifying device ratings and measuring device characteristics. The intended users of this standard are those interested in Thyristor Surge Protective Device characterization and rating verification. These devices are used primarily by the telecommunications industry to protect circuits from harmful overvoltages. The Thyristor Surge Protective Device (TSPD) is a semiconductor device that is finding widespread application in the telecommunication industry. The intent of this stand is to provide information on test methods that will reduce the possibility of disagreement and misunderstanding between TSPD vendors and users, and facilitate the determination of device interchangeability.<br>November 1999 /JC-22.5 Subcommittee | $83.00 |
| **JESD 67** | **I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD:** This standard attempts to aid in the design of electronic systems comprised of components that operate at several different supply voltages. This document covers respectively configurable I/O voltage, receiver type and switchpoint, and driver impedance.<br>February 1999 /JC-16 Committee | $38.00 |
| **JESD 68** | **COMMON FLASH INTERFACE (CFI):** The Common Flash Interface (CFI) specification outlines a device and host system software interrogation handshake that allows specific software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specific flash families. It allows flash vendors to standardize their existing interfaces for long-term compatibility.<br>September 1999 /JC-42.4 Subcommittee | $40.00 |
| **JESD 69** | **INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES:** This standard establishes the information required by semiconductor users from IC manufacturers and distributors in order to judge whether a semiconductor component is fit for use in their particular application. It establishes a set of data elements that describes the component and defines what each element means. It does not define the quality and reliability requirements that the component must satisfy. This standard can be used in conjunction with other reliability qualification standards, such as JESD34 'Failure Mechanism-Driven Reliability Qualification of Silicon Devices' and JESD47 'Stress Test Driven Qualification of Integrated Circuits'.<br>April 2000 /JC-14.3 Subcommittee | $33.00 |
| **JESD 70** | **2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS:** The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use, thus providing compatibility between devices operating between 2.3 V and 2.7 V supply voltages, as well as overvoltage tolerance with devices operating at 3.3 V, or 5 V.<br>June 1999 /JC-40 Committee | $34.00 |
| **JESD 71** | **STANDARD TEST AND PROGRAMMING LANGUAGE (STAPL):** STAPL is a vendor- and platform-independent language for programming and testing devices via the IEEE standard 1149.1 | |



Micron Technology Inc. et al.
Ex. 1017, p. 108

interface, commonly known as JTAG. STAPL enables programming of designs into programmable logic devices (PLDs) offered by a variety of PLD vendors. STAPL is also suitable for testing 1149.1-compliant devices.

August 1999 / Committee!33JC421 $60.00

---

**JESD 72** **TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS:** This Test Method covers the minimum requirements that should be in effect for the evaluation and acceptance of polymeric materials for use in industrial, military, space, and other special-condition products which may require capabilities beyond standard commercial microelectronics applications. It is not the intent of this Publication to specify a material, but to evaluate the material to assure that the quality and reliability of the microelectronic devices are not compromised. This document replaces JEP105, JEP107 and JEP112.

June 2001 January 2001 /JC-13.5 Subcommittee $45.00

---

**JESD 73** **DESCRIPTION OF 5 V BUS SWITCH WITH TTL-COMPATIBLE CONTROL INPUTS:** This standard covers specifications for a family of 5 V NMOS FET bus switch devices with 5 V TTL compatible control inputs. Not included in this document are device-specific parameters and performance levels that the vendor must also apply for full device description.

June 1999 /JC-40 Committee $33.00

---

**JESD 73-1** **STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES:** This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this document is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

August 2001 /JC-40 Committee $33.00

---

**JESD 73-2** **STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS:** This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices with integrated charge pumps. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this standard is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

August 2001 /JC-40 Committee $33.00

---

**JESD 73-3** **STANDARD FOR DESCRIPTION OF 3867 - 2.5 V, SINGLE 10-BIT, 2-PORT, DDR FET SWITCH:** This standard provides a set of uniform data sheet parameters for the description of a single 10-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay.

November 2001 JC-40.2 $33.00

---

**JESD 73-4** **STANDARD FOR DESCRIPTION OF 3877 - 2.5 V, DUAL 5-BIT, 2-PORT, DDR FET SWITCH:** This standard provides a set of uniform data sheet parameters for the description of a dual 5-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay.

November 2001 JC-40.2 $33.00

---

**JESD 74** **EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR ELECTRONIC COMPONENTS:** This new standard defines a procedure for calculating the point estimate of the time-dependent failure rate of electronic components from early life failure rate (ELFR) reliability test data. Calculation techniques are developed for constant failure rate and decreasing failure rate distributions. Projections can be used to compare reliability performance with objectives, provide line feedback, support service cost estimates, and set product test and reliability screen strategies.

April 2000 /JC-14.3 Subcommittee $36.00

---



Micron Technology Inc. et al.
Ex. 1017, p. 109

| | | |
|---|---|---|
| JESD 75 | **BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS:** The purpose of this standard is to provide a pinout standard for dual-die 32-bit logic devices offered in a 96- and 144-ball grid array package for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This standard defines device output for 32-bit wide buffer, driver and transceiver functions. This pinout specifically applies to the conversion of DIP-packaged 16-bit logic devices to LFBGA-packaged dual-die 32-bit logic devices.<br>November 1999 /JC-40 Committee | $31.00 |
| JESD 75-1 | **BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16, 18, AND 20-BIT LOGIC FUNCTIONS USING A 54 BALL PACKAGE:** This standard establishes a 54 Ball Grid Array pinout for 16, 18 and 20-bit standard logic devices that are currently being produced in 48 and 56 Pin SSOP and TSSOP packages. The 54 Ball Grid Array Package is organized as a 6 x 9 array with balls on a .8mm x .8mm grid pitch.<br>October 2001 /JC-40 Committee | $31.00 |
| JESD 75-2 | **BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS:** This standard provides a pinout standard for 16-bit wide logic devices offered in a 56-ball area grid array package to provide for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.<br>July 2001 /JC-40 Committee | $31.00 |
| JESD 75-3 | **BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS:** This standard provides a pinout standard for 8-bit logic devices offered in a 20-ball area grid array package to provide for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.<br>July 2001 /JC-40 Committee | $30.00 |
| JESD 76 | **DESCRIPTION OF 1.8 V CMOS LOGIC DEVICES:** This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established in JESD80. In this standard, the input and output conditions are described for CMOS Logic products in a 1.8 V (Normal Range) application.<br>April 2000 JC-40.1 | $31.00 |
| JESD 76-1 | **STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (WIDE RANGE OPERATION):** This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (nominal) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.<br>June 2001 /JC-40 Committee | $31.00 |
| JESD 76-2 | **STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (NORMAL RANGE OPERATION):** This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (normal range) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.<br>June 2001 /JC-40 Committee | $31.00 |
| JESD 76-3 | **STANDARD DESCRIPTION OF 1.5 V CMOS LOGIC DEVICES:** This standard continues the voltage specification migration to the next level beyond the 1.8 V specification already established. The purpose is to provide a standard for 1.5 V nominal supply voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.<br>August 2001 JC-40.1 | $31.00 |
| JESD 77-B | **TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES:** A revised and significantly expanded reference for technical writers and educators, manufacturers, buyers and users of discrete semiconductor and optoelectronic devices, is now available. Revision B of JEDEC Standard No. 77 includes extensive information on: letter symbol conventions; diodes and rectifiers (including signal, rectifier, microwave, tunnel and backward, voltage-regulator, voltage-reference, current regulator, and varactor diodes); transistors (including FETs, JFETs, and IGBTs); photosensitive devices, photoemitters, and optocouplers; thyristors and PUTs; and | |



Micron Technology Inc. et al.
Ex. 1017, p. 110

transient voltage suppressors. Terms and symbols, with their definitions, are arranged alphabetically by product type. Where applicable, graphical symbols are also included.

February 2000 /JC-10 Committee $152.00

---

**JESD 78**

**IC LATCH-UP TEST:** This standard has been adopted by the Defense Logistics Agency (DLA) as project 5962-1880. This standard establishes a defined method for latch-up testing of ICs. It defines Classes and Levels for a device's latch-up capability so that both the user and supplier understand a device's latch-up capabilities. It is applicable to NMOS, CMOS, Bipolar, and all variations and combinations of these technologies. Latch-up is an extremely important factor in determining product reliability.

March 1997 /JC-14.1 Subcommittee $41.00

---

**JESD 79-2**

**DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION:** This comprehensive standard defines all required aspects of 64Mb through 1Gb DDR SDRAMs with X4/X8/X16 data interfaces, including features, functionality, ac and dc parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 64Mb through 1Gb, X4/X8/X16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

May 2002 JC-42.3C $105.00

---

**JESD 80**

**STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES:** The purpose of this standard is to provide a standard for 2.5 V nominal supply-voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This standard defines dc interface parameters and test loading for CMOS digital logic family based on 2.5 V (nominal) power supply levels at 2.5 V input tolerance.

November 1999 /JC-40 Committee $31.00

---

**JESD 82**

**DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS:** This specification is a reference for Registered DDR DIMM designers. JESD82 defines the physical, electrical, interface and timing requirements of a 1:10 PLL clock driver for DDR Registered DIMMs from DDR200 to DDR266 as refined in revision C of JEDEC Standard 21-C (JESD21-C). JESD82 was also written to meet the future performance requirements of Registered DIMMs for DDR300 and DDR333.

July 2000 /JC-40 Committee $40.00

---

**JESD 82-1**

**DEFINITION OF CV857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, AND PC2700 DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CV857 PLL clock device for registered PC1600, PC2100 and PC2700 DIMM applications. The purpose is to provide a standard for a CV857 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

October 2002 /JC-40 Committee $46.00

---

**JESD 82-2**

**STANDARD FOR DESCRIPTION OF A 3.3 V, 18-BIT, LVTTL I/O REGISTER FOR PC133 REGISTERED DIMM APPLICATIONS:** This standard defines the register support devices needed for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics required for this type of SDRAM module.

July 2001 /JC-40 Committee $38.00

---

**JESD 82-3A**

**DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16857 14-bit SSTL_2 registered buffer for DDR DIMM applications. The purpose is to provide a standard for the SSTV16857 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

October 2002 /JC-40 Committee $41.00

---

**JESD 82-4A**

**STANDARD FOR DEFINITION OF THE SSTV16859 2.5 V, 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR STACKED DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading



Micron Technology Inc. et al.
Ex. 1017, p. 111

for definition of the SSTV16859 13-bit to 26-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV16859 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

October 2002 /JC-40 Committee $41.00

---

**JESD 82-5** **STANDARD FOR DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH THE JESD21-C PC133 REGISTERED DIMM SPECIFICATION** This standard defines the PLL support devices required for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics of the PLL used on JEDEC standard modules. JESD82-5 is the latest specification to be added to the JESD82 family of specifications for memory module support devices. Additional specifications are currently under development for DDRII support devices.

July 2002 /JC-40 Committee $41.00

---

**JESD 85** **METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS:** This standard establishes methods for calculating failure rates in units of FITs by using data in varying degrees of detail such that results can be obtained from almost any data set. The objective is to provide a reference to the way failure rates are calculated.

July 2001 /JC-14.3 Subcommittee $48.00

---

**JESD 86** **ELECTRICAL PARAMETERS ASSESSMENT:** This standard is intended to describe various methods for obtaining electrical variate data on devices currently produced on the manufacturing and testing process to be qualified. The intent is to assess the device's capability to function within the specification parameters over time and the application environment (operating range of temperature, voltage, humidity, input/output levels, noise, power supply stability etc.).

August 2001 /JC-14.3 Subcommittee $31.00

---

**JESD 87** **STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS** This document describes design of test structures needed to assess the reliability of aluminum-copper, refractory metal barrier interconnect systems. This includes any metal interconnect system where a refractory metal barrier or other barrier material prevents the flow of aluminum and/or copper metal ions from moving between interconnect layers. This document is not intended to show design of test structures to assess aluminum or aluminum-copper alloy systems, without barriers to Al and Cu ion movement, nor for Cu only metal systems. Some total interconnect systems might not include barrier materials on all metal layers. The structures in this standard are designed for cases where a barrier material separates two Al or Al alloy metal layers. The purpose of this document is to describe the design of test structures needed to assess electromigration (EM) and stress-induced-void (SIV) reliability of AlCu barrier metal systems.

July 2001 /JC-14.2 Subcommittee $36.00

---

**JESD 88** **DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, First Edition:** This reference for technical writers and educators, manufacturers, and buyers and users of discrete solid state devices is now available. It should aid the technical committees of JEDEC in the avoidance of multiple definitions and reduce the proliferation of redundant definitions. The long-term goal is to include definitions from all JEDEC publications and standards. Even in this first edition, that goal has been largely met. Each of the approximately two thousand entries is referenced to its source publication, and an annex listing the names of the source publications and their releases dates is included. All entries were reviewed for punctuation, grammar, and clarity, as well as accuracy, and reworded if such was considered warranted. The purpose of this dictionary is to promote the uniform use of terms, definitions, abbreviations, and symbols throughout the solid state industry.

September 2001 /JC-10 Committee $50.00

---

**JESD 89** **MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES:** This specification defines the standard requirements and procedures for terrestrial soft-error-rate (SER) testing of integrated circuits and reporting of results. Both real-time (unaccelerated) and accelerated testing procedures are described. At terrestrial, Earth-based altitudes, the predominant sources of radiation include both cosmic-ray radiation and alpha-particle radiation from



Micron Technology Inc. et al.
Ex. 1017, p. 112

radioisotopic impurities in the package and chip materials. An overall assessment of a device's SER is complete, only when an unaccelerated test is done, or accelerated SER data for the alpha-particle component and the cosmic-radiation component has been obtained.

August 2001 /JC-13.4 Subcommittee $75.00

---

**JESD 91** **METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC COMPONENT FAILURE MECHANISMS:** This standard provides a reference for developing acceleration models for defect-related and wear-out mechanisms in electronic components. The document provides several informative examples of how this method can be applied.

December 2001 /JC-14.3 Subcommittee $40.00

---

**JESD 99-1** **ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS:** This addendum has now been incorporated into JESD99-A.

July 1989 /JC-10 Committee

---

**JESD 99-A** **TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES:** This standard will be useful to users, manufacturers, educators, technical writers, and others interested in the characterization, nomenclature, and classification of microelectronics devices. There are general guidelines for both letter symbols and abbreviations applicable to all integrated circuits, and detailed sections for digital ICs, linear (analog) ICs, interface ICs (including D/A and A/D converters), voltage regulators, charge-transfer devices. The standard lists and defines more than 400 of the most common physical and electrical terms applicable to these devices and shows the industry-standard symbol and abbreviations that have been established for such terms.

May 2000 /JC-10 Committee $118.00

---

**JESD 100-B** **TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND, MEMORY INTEGRATED CIRCUITS:** A revised reference for technical writers and educators, manufacturers, buyers and users of microprocessors, microcomputers, mircocontrollers, memory ICs, and other complex devices. The terms and their definitions in this standard have been updated and are in general agreement with the latest publications of the IEEE and the IEC. The companion standard for other integrated circuits is JESD99A. Also included is a system for generating symbols for time intervals found in complex sequential circuits, including memories.

December 1999 /JC-10 Committee $63.00

---

**JESD 22-B109** **FLIP CHIP TENSILE PULL:** The Flip Chip Tensile Pull Test Method is performed to determine the fracture mode and strength of the solder bump interconnection between the flip chip die and the substrate. It should be used to assess the consistency of the chip join process. This test method is a destructive test.

June 2002 /JC-14.1 Subcommittee $39.00

---

**JESD 282-B** **SILICON RECTIFIER DIODES:** This standard provided definitions, electrical characteristics circuit technology, letter symbols and registration format for diodes and stacks. It also covers rating and characteristics, manufacturing and performance as well as test practices to demonstrate the performance of semiconductor rectifier diodes and rectifier stacks used for the conversion and/or control of electric power.

April 2000 /JC-22.2 Subcommittee $166.00

---

**JESD 286-B** **STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES:** This method updates the standard procedure for characterizing the switching of signal or switching diodes when a step function of forward current is applied. The objective is to provide a standard so that accurate comparisons can be made.

February 2000 /JC-22.4 Subcommittee $33.00

---

**JESD 307** **VOLTAGE REGULATOR DIODE NOISE VOLTAGE MEASUREMENT:** This standard is intended to cover the measurement of noise voltage in voltage regulator diodes in the reverse breakdown region. It describes noise voltage measurements at specified conditions, but may be used as a guide for making such measurements at other than specified conditions. (Formerly EIA-307)

May 1965; Reaffirmed January 1992, April 1999, April 2002 April 2002 /JC-22.4 $36.00



Micron Technology Inc. et al.
Ex. 1017, p. 113

| | | |
|---|---|---|
| | Subcommittee | |
| JESD 313-B | **THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS:** This standard provides a test method for measuring thermal resistance for conduction cooled power transistors.<br>October 1975; Reaffirmed April 1981, March 2001 /JC-25 Committee | $38.00 |
| JESD 320-A | **CONDITIONS FOR MEASUREMENT OF DIODE STATIC PARAMETERS:** This standard provides guidance for achieving equilibrium when measuring temperature sensitive static parameters of signal diodes. (Formerly EIA-302-A)<br>December 1992; Reaffirmed April 1999, April 2002 (Original publication July 1965) April 2002 /JC-22.4 Subcommittee | $35.00 |
| JESD 381-A | **METHOD OF DIODE Q MEASUREMENT:** This standard was updated and revised for the purpose of clarifying the method used to measure Q of a Voltage-Variable-Capacitance Diode in the low VHF range using an RF admittance bridge. ANSI/EIA-381-A-1992.<br>August 1992; Reaffirmed April 1999 April 1999 /JC-22.4 Subcommittee | $41.00 |
| JESD 482-A | **LIST OF PREFERRED VALUES FOR USE ON VARIOUS TYPES OF SMALL SIGNAL AND REGULATOR DIODES:** This standard specifies preferred values to be used on signal and regulator diodes. It will facilitate the standardization for nominal values used on small signal regulator diodes previously established in JEDEC Suggested Standard No. 2. (Formerly EIA-482-A)<br>August 1984; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee | $36.00 |
| JESD 531 | **THERMAL RESISTANCE TEST METHOD FOR SIGNAL AND REGULATOR DIODES (FORWARD VOLTAGE, SWITCHING METHOD):** This standard describes a test method for measuring the thermal resistance of signal and regulator diodes. The need for modification of this test method arose out of the limited description that existed earlier for both signal and regulator diode applications in testing for thermal resistance. ANSI/EIA-531-1986<br>July 1986; Reaffirmed April 1999 April 1999 /JC-22.4 Subcommittee | $40.00 |
| JESD 625-A | **REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES:** This standard establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD). The passage of a static charge through an electrostatic-discharge-sensitive (ESDS) device can result in catastrophic failure or performance degradation of the part. Device sensitivity to ESD is determined by test methods such as EIA/JESD22-A114. ESDS devices with human body model sensitivities of less than +200 volts may need additional protective measures beyond those specified in this standard.<br>December 1999 /JC-14.1 Subcommittee | $48.00 |
| JESD 659-A | **FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING:** This method establishes requirements for application of Statistical Reliability Monitoring 'SRM' technology to monitor and improve the reliability of electronic components and subassemblies. The standard also describes the condition under with a monitor may be replaced or eliminated.<br>September 1999 /JC-14.3 Subcommittee | $41.00 |
| JESD 671-A | **COMPONENT QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS (INCLUDING ADMINISTRATIVE QUALITY PROBLEMS):** This revision now encompasses administrative quality problems, in addition to the electrical and visual/mechanical quality problems that were addressed in the original release. A standard set of problem categories for each of these three types of component problems is presented for tracking and reporting purposes. A common set of customer and supplier expectations and requirements are set forth to help facilitate the successful problem analysis and corrective action of any type of component quality problem.<br>December 1999 /JC-14.4 Subcommittee | $36.00 |
| **NUMBER** | **Joint IPC/JEDEC Standards (J-STD- )** | **PRICE** |
| J-STD- 020-B | **JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES:** This document identifies the | |



Micron Technology Inc. et al.
Ex. 1017, p. 114

| | | |
|---|---|---|
| | classification level of nonhermetic solid-state surface mount devices (SMDs) that are sensitive to moisture-induced stress. It is used to determine what classification level should be used for initial reliability qualification. Once identified, the SMDs can be properly packaged, stored and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation. This revision now covers components to be processed at higher temperatures for lead-free assembly. A hard cop version is available for $20 each for IPC/JEDEC members and $40 for nonmembers.<br>July 2002 /JC-14.1 Subcommittee | |
| J-STD- 033A | **JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES:** This document provides SMD manufacturers and users with standardized methods for handling, packing, shipping and use of moisture/reflow sensitive SMDs. Now updated to support components that may need to be processed at higher temperatures, such as lead-free processes, these methods help avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. IPC/JEDEC J-STD-033A helps achieve safe and damage-free reflow with the dry packing process and provides a minimum shelf life of 12 months from the seal date when using sealed dry bags. Hard copies of this document are available for $20 each for IPC/JEDEC members and $40 for nonmembers.<br>July 2002 /JC-14.1 Subcommittee | |
| J-STD- 035 | **JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS:** This test method defines the procedures for performing acoustic microscopy on non-hermetic encapsulated electronic components. This method provides users with an acoustic microscopy process reflow for detecting defects non-destructively in plastic packages while achieving reproducibility.<br>May 1999 /JC-14.1 Subcommittee | $35.00 |

| NUMBER | Joint Publication (JP ) | PRICE |
|---|---|---|
| JP 001 | **FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)** This document provides a guideline for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g. analog CMOS, bipolar, BICMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g. Cu/Low K interconnects or ultra thin gate oxide. This publication, is co-sponsored by JEDEC JC-14.2 and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification requirements.<br>September 2002 /JC-14.2 Subcommittee | $65.00 |

| NUMBER | JEDEC Publications (JEP ) | PRICE |
|---|---|---|
| JEP 64 | **SOLID STATE PRODUCTS REGISTRATION LIST(ORDER FROM TYPE ADMINISTRATION OFFICE):** This publication includes addenda from 1976 to August 1986. The purpose of this list is to determine release numbers (file numbers) for JEDEC Type Designations. (See page 6 for more information.)<br>September 1986 | $152.00 |
| JEP 65 | **TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS:** This publication describes tests which are intended to represent the verification of maximum ratings for data sheets; they are not tests for performance or quality level. This material is to be used in conjunction with formats developed for device registration and defining data.<br>December 1967; Reaffirmed September 1981, April 1999 /JC-25 Committee | $45.00 |
| JEP 69-B | **PREFERRED LEAD CONFIGURATION FOR FIELD-EFFECT TRANSISTORS:** This publication indicates preferred pinouts for FETs in various package designs.<br>November 1973; Reaffirmed September 1981, April 1999 /JC-25 Committee | $31.00 |
| JEP 70-B | **QUALITY AND RELIABILITY STANDARDS AND PUBLICATIONS:** Contains a listing and description of commonly used quality and reliability related standards and publications that are applicable to the semiconductor industry. It is intended to be a reference aid in finding available standards and obtaining a copy from the source of the standard. It is not intended | |



Micron Technology Inc. et al.
Ex. 1017, p. 115

| | | |
|---|---|---|
| | to recommend or imply the applicability of any standard for a specific purpose. This revision has been updated to include recent releases as well as revisions, in addition, URLs have been added to the "Addresses of Standards Sources" section, to help facilitate procurement of standards through the internet.<br>October 1999 /JC-14.4 Subcommittee | $50.00 |
| **JEP 74** | **STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996.**<br>July 1969; Rescinded February 1996 /JC-25 Committee | $31.00 |
| **JEP 75** | **LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.**<br>August 1984; Rescinded August 1984 /JC-10 Committee | $30.00 |
| **JEP 78** | **RELATIVE SPECTRAL RESPONSE CURVES FOR SEMICONDUCTOR INFRARED DETECTORS:** The intent of this publication is to facilitate the specification of infrared detector diodes, particularly in conjunction with the preparation of data for JEDEC type registration.<br>October 1969 /JEDEC Committee | $45.00 |
| **JEP 79** | **LIFE TEST METHODS FOR PHOTOCONDUCTIVE CELLS:** This publication is for photoconductive cells sensitive primarily in the visible and near infrared region.<br>September 1969 | $45.00 |
| **JEP 84** | **RECOMMENDED PRACTICE FOR MEASUREMENT OF TRANSISTOR LEAD TEMPERATURE:** This publication covers recommended methods for measurement of transistor lead temperatures under various load conditions. The techniques described are sufficiently accurate for most applications.<br>February 1973; Reaffirmed February 1982 /JC-25 Committee | $31.00 |
| **JEP 86-A** | **RECOMMENDED PRACTICE FOR DUAL DIMENSIONING**<br>May 1976; Rescinded November 1999 /JC-11 Committee | |
| **JEP 87** | **FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A.**<br>June 1992; Rescinded June 1985 /JC-22.2 Subcommittee | |
| **JEP 88** | **THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS**<br>January 1974; Rescinded June 1992 /JC-22.1 Subcommittee | |
| **JEP 90** | **THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986.**<br>September 1983; Rescinded September 1986 /JC-22.4 Subcommittee | |
| **JEP 93** | **MICROELECTRONIC DEVICE TYPE ASSIGNMENTS**<br>August 1975; Rescinded June 1992 / Committee!33JCJEDC | |
| **JEP 95** | **JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS:** This publication is a compilation of some 1800 pages of outline drawings for microelectronic packages including transistors, diodes, DIPS, chip carriers and package interface BGA outlines in both inch and metric versions.<br>January 2000 /JC-11 Committee | $350.00 |
| **JEP 95 AUS** | **ANNUAL UPDATING SERVICE:** Subscription to this updating service is available from the JEDEC Office. New outlines are shipped to subscribers for insertion into the appropriate sections of Publication No. 95. JEP95 and Updating Service must be ordered through JEDEC at (703) 907-7540.<br>January 2000 /JC-11 Committee | $110.00 |
| **JEP 95-1** | **DESIGN REQUIREMENTS (Book 1, Section 4)** Type 'section' in the 'by document number' to see the contents of this document. This is currently under construction. Once it has been | |



Micron Technology Inc. et al.
Ex. 1017, p. 116

completed you will be able to click on the 'entire document' icon below and see all the sections contained in this document.

January 2000 /JC-11 Committee

---

**JEP 96** **GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES**

March 1977; Rescinded April 2000 /JC-13.5 Subcommittee

---

**JEP 99** **GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.**

July 1977; Rescinded June 1985 /JC-10 Committee

---

**JEP 100** **TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.**

September 1979; Rescinded October 1983 /JC-10 Committee

---

**JEP 101-C** **JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS:** This revision reflects the following changes in MIL-Specs: 1) The conversion form MIL-M-38510 to MIL-I-38535 (renamed MIL-PRF-38535) as the General Specification for Microelectronics Devices. 2)The transfer of "Compliancy Requirements" from General Provisions paragraph 1.2.1 of MIL-STD-883 to Appendix A of MIL-PRF-38535.

November 1995 /JC-13.2 Subcommittee $31.00

---

**JEP 102** **STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C.**

September 1978; Rescinded April 1985 /JC-42 Committee

---

**JEP 103-A** **SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS** In order to improve understanding between manufacturers and users, a consistent set of product-documentation classifications associated with the stages of product development.

July 1996; Reaffirmed November 1999 /JC-10 Committee $30.00

---

**JEP 104-C** **REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES:** This publication provides a quick reference to the letter symbols and corresponding terms that are defined in JESD77-B, Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices; JESD99-A, Terms, Definitions, and Letter Symbols for Microelectronic Devices, and JESD100-B, Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits. It is intended to simplify interpretation of data sheets and specifications and to promote the uniform use of these symbols. The symbols relate to ratings and characteristics found in data sheets and other specifications. Some abbreviations used in lieu of symbols are also included. The newly added Annex B is provided as an aid to determining what symbol should be used and is organized by term, whereas the main body of the publication is organized by symbol or abbreviation as in previous versions.

June 2002 /JC-10 Committee $88.00

---

**JEP 105** **JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001**

April 1983; Rescinded June 2001 /JC-13.5 Subcommittee $42.00

---

**JEP 106-K** **STANDARD MANUFACTURERS IDENTIFICATION CODE:** The manufacturers identification code is defined by one or more 8 bit fields, each consisting of 7 data bits plus 1 odd parity bit. The manufacturers identification code is assigned, maintained and updated by the JEDEC Office. The intent of this identification code is that it may be used whenever a digital field is required, e.g., hardware, software, documentation, etc.

September 2001 /JC-42.3 Subcommittee $38.00

---

**JEP 107** **TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001**

April 1985; Rescinded June 2001 /JC-13.5 Subcommittee $40.00

---

**JEP 108-B** **DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC -DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.**

April 1991



Micron Technology Inc. et al.
Ex. 1017, p. 117

| | | |
|---|---|---|
| JEP 109-C | **GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:** Superseded by JESD31-A, June 2001.<br>March 1995; Rescinded November 2001 /JC-13 Committee | $41.00 |
| JEP 110 | **GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS:** This publication is intended for power GaAs FET applications requiring high reliability. An accurate measurement of thermal resistance is extremely important to provide the user with knowledge of the FETs operating temperature so that more accurate life estimates can be made. FET failure mechanisms and failure rates have, in general, an exponential dependence on temperature (which is why temperature-accelerated testing is successful). Because of the exponential relationship of failure rate with temperature, the thermal resistance should be referenced to the hottest part of the FET.<br>July 1988 /JC-14.7 Subcommittee | $36.00 |
| JEP 111 | **TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.**<br>July 1986; Rescinded June 1996 | |
| JEP 112 | **TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001**<br>June 1987; Rescinded June 2001 /JC-13 Committee | $45.00 |
| JEP 113-B | **SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES:** Certain PSMC (Plastic Surface-mount Components) are subject to permanent damage due to moisture-induced failures encountered during high-temperature surface-mount processing unless appropriate precautions are observed. The purpose of this publication is to provide a distinctive symbol and labels to be used to identify those devices that require special packing and handling precautions.<br>May 1999 /JC-14.1 Subcommittee | $38.00 |
| JEP 114 | **GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION:** This publication was developed to help the user of this test methodology avoid common interference's to successful application. The guide contains sections on typical specification requirements, sources of particles, PIND test systems, calibration, maintenance, test interference's, operator training, particle recovery and failure analysis. Application of the information contained in the guide will improve the quality and affectivity for any PIND testing operation.<br>December 1989 /JC-13 Committee | $54.00 |
| JEP 115 | **POWER MOSFET ELECTRICAL DOSE RATE TEST METHOD:** The purpose of this Test Method is to establish electrical criteria for comparing and specifying power MOSFET performance under high dose rate radiation.<br>August 1989; Reaffirmed April 1999 /JC-25 Committee | $34.00 |
| JEP 116 | **CMOS SEMICUSTOM DESIGN GUIDELINES:** The design of ASIC circuits is becoming a significant part of system or product design, yet many problems continue to exist in current design practice. The guidelines in this document provide an explanation of common ASIC design problems and concerns and where possible offer solutions.<br>November 1991 / Committee!33JC44 | $100.00 |
| JEP 117 | **GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.**<br>April 1994; Rescinded July 1994 /JC-14.4 Subcommittee | |
| JEP 118 | **GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING:** These guidelines apply to monolithic microwave GaAs integrated circuits (MMICs) and their individual component building blocks, such as GaAs field effect transistors (FETs), resistors, and capacitors. The purpose of this document is to define a standard approach for evaluating the expected live of GaAs MMICs so that results from different life tests can be compared and so that wording of this document that the MMIC contains at least one FET, but the use of this document has no such limitation.<br>January 1993 /JC-14.7 Subcommittee | $41.00 |



Micron Technology Inc. et al.
Ex. 1017, p. 118

| | | |
|---|---|---|
| JEP 119 | **A PROCEDURE FOR EXECUTING SWEAT:** The intent of the publication is to provide a complete description of a basic, functional SWEAT algorithm that will allow a programmer to begin accelerated electromigration testing with ease.<br>September 1994 /JC-14.2 Subcommittee | $42.00 |
| JEP 120-A | **INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS:** This publication provides an index to terms that are defined in certain JEDEC publications. It is intended to promote the uniform use of these terms and their definitions while reducing the proliferation of new definitions for old terms.<br>May 2000 /JC-10 Committee | $100.00 |
| JEP 121 | **GUIDELINES FOR MIL-STD-883 SCREENING AND QCI OPTIMIZATION:** The intent of this publication was developed to establish uniform guidelines, which would allow the use of In-Line Process Controls and Statistical Process Control as viable alternatives to the 100% screens and "after the fact" quality conformance inspections (QCI). The benefits of this system for both user and manufacturer would include improved manufacturing effectiveness (e.g., use of "Best Commercial Practices"), productivity and quality/reliability.<br>April 1995 /JC-13 Committee | $100.00 |
| JEP 122-A | **FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES:** This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum-of-the-Failure-Rates method.<br>December 2001 /JC-14.1 Subcommittee | $56.00 |
| JEP 123 | **GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS:** The need for this guideline arose from widespread lack of consistency in characterizing electrical parameters of electronic packages, which existed in the industry until the early 1990s. Then, the JEDEC Committee JC-15 provided the forum where various methods were discussed and commonality in approach emerged. The result is that today we have relatively consistent results in measuring and reporting electrical package parameters, as well as specialized tools (e.g., the IPA-510, the interconnect parameter analyzer) which were developed to support the methodology.<br>October 1995 /JC-15 Committee | $42.00 |
| JEP 124 | **GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.**<br>December 1995; Rescinded November 1999 November 1999 /JC-14.4 Subcommittee | |
| JEP 126 | **GUIDELINE FOR DEVELOPING AND DOCUMENTING PACKAGE ELECTRICAL MODELS DERIVED FROM COMPUTATIONAL ANALYSIS:** This publication provides a guideline to suppliers of IC components with a template for documenting the numerical simulation assumptions. In addition this guideline also suggests a model environment to reference when comparing various packages or component suppliers. This publication should improve the communication between the package model suppliers. This publication should improve the communication between the package model supplier and the end user.<br>May 1996 /JC-15.2 Subcommittee | $31.00 |
| JEP 128 | **GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER LEVEL ELECTRICAL TESTING:** This guide was developed to expedite inter-laboratory experiments used to evaluate or develop standard test methods that involve test-structure measurements or tests. It also facilitates, generally, any electrical tests that require wafer-probe card to make electrical contact to test structures. Widespread use of this guide will afford the efficient and cost-effective use of water-probe test stations because of the need for fewer probe cards and probe-card changes to accommodate the various test structures that may need to be tested.<br>November 1996 /JC-14.2 Subcommittee | $33.00 |
| JEP 129 | **THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP)- SUPERSEDED BY JESD51-4, September 1997.**<br>February 1997; Elevated September 1997 /JC-15.1 Subcommittee | |



Micron Technology Inc. et al.
Ex. 1017, p. 119

**JEP 130** — **GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING:** This document establishes guidelines for integrated circuit unit container and the next level (intermediate) container packing and labeling. The guidelines include tube/rail standardization, intermediate packing, date codes, tube labeling, intermediate container and shipping labels, and standardize tube quantities. Future revisions of this document will also include tray and reel guidelines. The objective of this publication is to promote the standardization of practices between manufacturers and distributors resulting in improved efficiency, profitability, and product quality.

August 1997 /JC-14.4 Subcommittee — $33.00

---

**JEP 131** — **PROCESS FAILURE MODE AND EFFECTS ANALYSIS (FMEA):** This publication was created in response to the need for a straight forward FMEA procedure. The objective is to provide a guideline for the application of FMEA techniques to improve quality, reliability and/or consistency of electronic components and subassemblies by continually evaluating processes/products against potential failure modes.

February 1998 /JC-14.3 Subcommittee — $41.00

---

**JEP 132** — **PROCESS CHARACTERIZATION GUIDELINE:** This guideline provides a methodology to characterize a new or existing process and is applicable to any manufacturing or service process. It describes when to use specific tools such as failure mode effects analysis (FEMA), design or experiments (DOE), measurement system evaluation (MSE), capability analysis (CpK), statistical process control (SPC), and problem solving tools. It also provides a brief description of each tool.

July 1998 /JC-13 Committee — $52.00

---

**JEP 133-A** — **GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS:** A revised and expanded publication for suppliers and users of radiation hardness assured (RHA) multichip modules (MCMs) and hybrid microcircuits, is now available. Revision A of JEP133 includes modifications to the introduction, clarification of a definition and clarification of several technical issues within the document. In addition, the Bibliography section was updated to include added references. The document provides guidance as to how to achieve, maintain and ensure required levels of radiation-hardness given the fact that the constituent dice can have different levels of hardness assurance. It also describes how to deal with the various radiation hardness situations that an MCM/Hybrid developer, procuring activity or user will encounter. The guide is intended to supplement three relevant performance specifications: MIL-PRF-38534, MIL-PRF-38535 and MIL-PRF-19500.

July 2001 /JC-13.5 Subcommittee — $52.00

---

**JEP 134** — **GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE ANALYSIS:** The purpose of this Guideline is to provide a vehicle for acquiring and transmitting the necessary information in a concise, organized, and consistent format. Included in the Guideline is a sample form that facilitates transferring the maximum amount of background data to the failure analyst in a readily interpretable format. Immediate availability of this key information assists that analyst in completing a timely and accurate failure analysis.

September 1998 /JC-14.6 Subcommittee — $38.00

---

**JEP 136** — **SIGNATURE ANALYSIS:** Signature Analysis is a method to reduce the number of comprehensive physical failure analyses by the application of statistical inference techniques. The purpose of this document is to promote a common definition of Signature Analysis by inference, using the same statistical techniques, and to recognize that it is formal means of doing failure analysis.

July 1999 /JC-14.6 Subcommittee — $40.00

---

**JEP 137-A** — **COMMON FLASH INTERFACE (CFI) IDENTIFICATION CODES:** This publication is a companion document to the Common Flash Interface (CFI) standard, JESD68, which outlines the device and host system software interrogation handshake. JEP137 documents ID Code assignments for: 1)) the Algorithm-specific Command Set and Control Interfaces and 2) the Device Interfaces. It is published as needed when additions are made to either of these lists of codes. To make a request for an ID Code please contact the JEDEC Office at (703)907-7558.

September 2001 /JC-42.4 Subcommittee — $34.00

---



Micron Technology Inc. et al.
Ex. 1017, p. 120

| | | |
|---|---|---|
| JEP 138 | **USER GUIDELINES FOR IR THERMAL IMAGING DETERMINATION OF DIE TEMPERATURE:** The purpose of these user guidelines is to provide background and an example for the use of an infrared (IR) microscope to determine die temperature of electronic devices for calculations such as thermal resistance.<br>September 1999 /JC-25 Committee | $34.00 |
| JEP 139 | **GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING:** This document describes a constant temperature (isothermal) aging method for testing aluminum (Al) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding. This method is valid for metallization/dielectric systems in which the dielectric is deposited onto the metallization at a temperature considerably above the intended use temperature, and above or equal to the deposition temperature of the metal. Although this is a wafer test, it is not a fast (less than 5 minutes per probe) test. It is intended to be used for lifetime prediction and failure analysis, not for production Go-NoGo lot checking.<br>December 2000 /JC-14.2 Subcommittee | $40.00 |
| JEP 140 | **BEADED THERMOCOUPLE TEMPERATURE MEASUREMENT OF SEMICONDUCTOR PACKAGES:** The beaded thermocouple temperature measurement guideline provides a procedure to accurately and consistently measure the temperature of semiconductor packages during exposure to thermal excursions. The guideline applications can include, but not limited to, temperature profile measurement in reliability test chambers and solder reflow operations that are associated with component assembly to printed wiring boards.<br>June 2002 /JC-14.1 Subcommittee | $41.00 |
| JEP 142 | **GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS:** This document provides guidance regarding design considerations, material assessment techniques, and recommendations for material acceptance prior to use in Hybrid / MCM Products. As part of the risk assessment process, both technical requirements and cost should be carefully considered with regard to testing / evaluating the elements of a hybrid microcircuit or Multi-chip Module (MCM) prior to material release for assembly. The intent of this document is to highlight various options that are available to the Hybrid / MCM manufacturer and provide associated guidance, not to impose a specific set of tests.<br>May 2002 /JC-13.5 Subcommittee | $53.00 |
| JEP 143 | **SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES:** This publication is a reference for the suite of reliability, modeling and qualification documents and publications that available through JEDEC. It provides background on reliability assessment and qualification methodologies and includes a brief overview on each of the pertinent documents and publications.<br>November 2001 /JC-14.3 Subcommittee | $38.00 |
| JEP 144 | **GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES** The intent of this document is to give guidance on the Residual Gas Analysis (RGA) process and surrounding issues. The guideline describes how to select a suitable test lab and includes RGA history, measurement methodology, and issues that arise with the test. Interpreting the lab results along with common failure mechanisms are discussed at length along with process controls and alternative test techniques for measuring the moisture content within packages.<br>July 2002 /JC-13 Committee | $55.00 |

| NUMBER | EIA Standards (EIA ) | PRICE |
|---|---|---|
| EIA 236-C | **COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES:** This standard details the methods to be followed if color coding is used to identify JEDEC-assigned type numbers or for cathode identification of discrete semiconductor devices. ANSI/EIA-236-C-1986.<br>March 1986; Reaffirmed November 1999 /JC-10 Committee | $31.00 |
| EIA 282-A | **STANDARD FOR SILICON RECTIFIER DIODES: SEE JESD282-B** ANSI/EIA-282-A-1989<br>February 1990 Became JESD282-B after revision April 2000 /JC-22.2 Subcommittee | |
| EIA 283 | **TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A.** | |



Micron Technology Inc. et al.
Ex. 1017, p. 121

November 1963; Rescinded Reaffirmed November 1981 November 1981 /JC-25 Committee

| | | |
|---|---|---|
| **EIA 284-A** | **TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE:** The test methods described in this Standard are generally applicable to alloy-like devices for which the usual simplified equivalent circuits can be employed.<br>November 1963; Reaffirmed November 1963, June 1972, April 1981, April 1999 /JC-25 Committee | $63.00 |
| **EIA 286-A** | **STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: SEE JESD286-B.** ANSI/EIA-286-A-1991.<br>February 1991 Became JESD286-B after revision February 2000 /JC-22.4 Subcommittee | |
| **EIA 302** | **RANGES AND CONDITIONS FOR SPECIFYING BETA FOR LOW POWER, AUDIO FREQUENCY TRANSISTORS FOR ENTERTAINMENT SERVICE:** This standard establishes the preferred rating ranges and conditions for specifying beta for low power, audio frequency transistors intended for entertainment service.<br>January 1965; Reaffirmed April 1981, April 1999 /JC-25 Committee | $30.00 |
| **EIA 306** | **MEASUREMENT OF SMALL SIGNAL HF, VHF, AND UHF POWER GAIN OF TRANSISTORS:** This standard provides a method of measurement for small-signal HF, VHF, and UHF power gain of low power transistors.<br>May 1965; Reaffirmed April 1981, April 1999 /JC-25 Committee | $31.00 |
| **EIA 308-A** | **PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION:** This standard is intended to serve as a guide to manufacturers of solid state products for the preparation of outline drawings of solid state product packages for JEDEC type registration.<br>August 1981 /JC-11 Committee | $31.00 |
| **EIA 311-A** | **MEASUREMENT OF TRANSISTOR NOISE FIGURE AT MF, HF, AND VHF:** This standard describes a test method for measurement of transistor noise figure and effective input noise temperature at MF, HF, and VHF. This standard also adds the necessary information to make 'effective input noise temperature measurements'. This method is a revision of EIA-311 and incorporates material previously found in EIA-283.<br>November 1981; Reaffirmed April 1999 /JC-25 Committee | $41.00 |
| **EIA 318-B** | **MEASUREMENT OF REVERSE RECOVERY TIME FOR SEMICONDUCTOR SIGNAL DIODES:** This standard describes the measurement of signal diodes ($I_F$ <=500mA dc) reverse recovery times of less than 300 ns duration. It may, however, also be used for the measurement of longer recovery times. This standard is also intended to establish a method which to characterize the test fixture used for this measurement.<br>July 1996; Reaffirmed April 1999 /JC-22.4 Subcommittee | $40.00 |
| **EIA 321-C** | **NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES:** This standard gives the system for numbering like-named electrodes or terminal functions in semiconductor devices and for assigning numerical designations to units of multiple-unit semiconductor devices. It applies to both integrated circuits and discrete devices. ANSI/EIA-321-C-1987<br>February 1987; Reaffirmed November 1995 /JC-10 Committee | $34.00 |
| **EIA 323** | **AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES:** This standard is applicable to life testing of lead-mounted semiconductor devices intended for applications in a natural air-cooled environment where most of the power dissipation is obtained by convection and radiation losses from the body to the device.<br>March 1966; Reaffirmed February 1972 /JC-22.1 Subcommittee | $33.00 |
| **EIA 340** | **STANDARD FOR THE MEASUREMENT OF CRE:** This standard offers an easily measured parameter which is one of the significant characteristics in determining the stability of a transistor intended for small-signal operation. The measurement technique allows rapid testing. Its correlation to AC stability will help to establish the interchangeability of a device. | |



Micron Technology Inc. et al.
Ex. 1017, p. 122

| | | |
|---|---|---|
| | November 1967; Reaffirmed April 1981, April 1999 /JC-25 Committee | $36.00 |
| **EIA 353** | **THE MEASUREMENT OF TRANSISTOR NOISE FIGURE AT FREQUENCIES UP TO 20 kHz BY SINUSOIDAL SIGNAL-GENERATOR METHOD:** This noise measurement method applies to transistors whose noise has a Gaussian power distribution, to transistors whose noise has a flat (white) power distribution, and to transistors whose noise has a l/f (power inversely proportional to frequency) power distribution.<br>April 1968; Reaffirmed April 1981, April 1999 /JC-25 Committee | $33.00 |
| **EIA 354** | **THE MEASUREMENT OF TRANSISTOR EQUIVALENT NOISE VOLTAGE AND EQUIVALENT NOISE CURRENT AT FREQUENCIES OF UP TO 20 kHz:** This standard provides a method for determining values, for device registration purposes, for transistor equivalent noise voltage and equivalent noise current at frequencies up to 20 kHz. This method is applicable to transistors whose noise has a Gaussian, flat (white) or I/f power distribution.<br>April 1968; Reaffirmed April 1981, April 1999 /JC-25 Committee | $33.00 |
| **EIA 365** | **PERFORMANCE TEST PROCEDURE FOR SOLAR CELLS AND CALIBRATION PROCEDURE FOR SOLAR CELL STANDARDS FOR SPACE VEHICLE SERVICE:** The purpose of this standard is to classify the output of solar cells for space vehicle service in accordance with requirements of EIA Format JS4-RDF4.<br>November 1969; Reaffirmed February 1984 / Committee!33JC231 | $40.00 |
| **EIA 370-B** | **DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:** This standard includes several new items and has been completely rewritten from the original EIA-370. The first is a new letter symbol C so that a JEDEC type designation may now be 2C1234, to indicate that a chip is being designated that if it were properly mounted on the package registered for the 2N1234, it would display characteristics similar to those of the 2N1234. The second major addition is the method for assigning the first numeric symbol for type designations of optoelectronic devices. ANSI/EIA-370-B-1992.<br>February 1982; Reaffirmed November 1995, November 1999 /JC-10 Committee | $63.00 |
| **EIA 371** | **THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO:** This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor short-circuit forward current transfer ratio, in preparing data sheets for JEDEC registration of low power transistors.<br>February 1970; Reaffirmed April 1981, April 1999 /JC-25 Committee | $34.00 |
| **EIA 372** | **THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS:** This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor admittance parameters, in preparing data sheets for JEDEC registration of low power transistors.<br>May 1970; Reaffirmed April 1981, April 1999 /JC-25 Committee | $36.00 |
| **EIA 390-A** | **STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS:** The purpose of this standard is to define the dc (Steady-State) noise margin and the ac (Transient) Noise Margin in Semiconductor Logic Gating Microcircuits, and to describe the procedures used to measure these parameters. The standardization of the definitions and test procedures is intended to improve the ability to ensure interchangeability of elements by test specification, and to eliminate misunderstandings between manufacturers and users.<br>February 1981 /JC-13 Committee | $36.00 |
| **EIA 397** | **RECOMMENDED STANDARD FOR THYRISTORS:** One section of this standard presents a thorough explanation of thyristor principals, defining the different classes of these devices, their Physical structure and detailing the numerous test methods and ratings required in their application to electronic and power circuitry. Another section presents a universally accepted listing of letter symbols. Considerable effort is devoted to the use of JEDEC Type Registration System as related to thyristors. This will permit the device manufacturer to employ a uniform procedure in the development of maximum rating and presentation of performance data.<br>June 1972 /JC-22.1 Subcommittee | $166.00 |
| **EIA 397-1** | **ADDENDUM No. 1 TO EIA-397:** A compilation of 12 new or revised thyristor test methods | |



Micron Technology Inc. et al.
Ex. 1017, p. 123

| | | |
|---|---|---|
| | which have been adopted since the original standard was issued in 1972.<br>July 1980 /JC-22.1 Subcommittee | $75.00 |
| **EIA 398** | **MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:** This standard contains a three-terminal procedure for capacitance measurement with due precautions for shielding of extraneous effects due to terminal leads and metal enclosures.<br>July 1972; Reaffirmed April 1981, April 1999 /JC-25 Committee | $36.00 |
| **EIA 428-A** | **TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES**<br>October 1988; Rescinded September 1993 | |
| **EIA 435** | **STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:** This standard specifies the standard for the measurement of small-signal transistor scattering parameters.<br>June 1976; Reaffirmed April 1999 /JC-25 Committee | $42.00 |
| **EIA 471** | **SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES:** This standard will be useful to anyone engaged in handling semiconductor devices and integrated circuits that are subject to permanent damage due to electrostatic potentials. The standard establishes a symbol and label that will gain the attention of those persons who might inflict electrostatic damage to the device. The label which is placed on the lowest practical level of packaging contains the words 'ATTENTION - OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES'. The symbol contained in this label, which may be used on the device itself, shows a hand in a triangle with a bar through it.<br>February 1980; Reaffirmed October 1988, September 1996, November 1996 /JC-10 Committee | $31.00 |
| **EIA 557-A** | **STATISTICAL PROCESS CONTROL SYSTEMS:** SPC embraces a management philosophy of continuous process improvement that has a primary focus on prevention of defects. After a process has been characterized using statistical techniques (i.e., design experiments (DOE), capability studies, etc.), SPC is a tool that can be applied to control and optimize the process and reduce variability. An acceptable approach toward an SPC system involves the use of 'end-of-process' data to control the process through the application of SPC techniques. However, the intent of this standard is to emphasize the use of in-process data in order to better control and forecast system quality. This proactive use of SPC in conjunction with other techniques and the appropriate responsiveness to out-of-control situations serves to make SPC techniques critical in continuous process improvement and achieving excellence.<br>July 1995 /JC-13.5 Subcommittee | $54.00 |
| **EIA 599-A** | **NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS:** This standard is applicable to suppliers of electronic components, assemblies, equipment, and related materials. This standard establishes the general requirements to achieve a certified process. The use of this standard is intended for any manufacturing or servicing company whose goal is to achieve customer satisfaction through continuous improvement.<br>June 1998 /JC-14.4 Subcommittee | $36.00 |
| **EIA 623** | **PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS:** This standard defines the practices to be used by government contractors related to the procurement of solid state components. These practices include parts selection, supplier management, and receiving inspection and test.<br>July 1994 /JC-13 Committee | $33.00 |
| **EIA 625** | **REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A.**<br>November 1994 Became JESD625A after Revision December 1999 /JC-13 Committee | |
| **EIA 659** | **FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING (SUPERSEDES JESD29-A): SEE JESD659-A.**<br>July 1996 Became JESD659A after Revision September 1999 /JC-14.3 Subcommittee | |
| **EIA 670** | **QUALITY SYSTEM ASSESSMENT (SUPERSEDES JESD39-A):** This standard is used by the | |



Micron Technology Inc. et al.
Ex. 1017, p. 124

| | | |
|---|---|---|
| | electronic industry for preparation of audit checklists for assessing compliance of quality systems to the requirements of ANSI/ASQC Q9001 (ISO9001), ANSI/ASQC Q9002 (ISO9002), ANSI/ASQC Q9003 (ISO9003), and ANSI/EIA599, National Electronic Process Certification Standard. It also provides a tool for quality system evaluation in accordance with the guidelines of ANSI/ASQC Q9004 (ISO9004) and the Malcolm Baldrige National Quality Award Criteria.<br>June 1997 /JC-14.4 Subcommittee | $56.00 |
| **EIA 671** | **COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A.**<br>November 1996 Became JESD671A after revision December 1999 /JC-14.4 Subcommittee | |
| **JESD 419-A** | **STANDARD LIST OF VALUES TO BE USED IN SEMICONDUCTOR DEVICE SPECIFICATIONS AND REGISTRATION FORMAT:** This document contains standard lists of values which are recommended for use in semiconductor device specification and JEDEC Registration Formats. Good reasons should exist in those cases where values are used that are not included in these lists.<br>October 1980; Reaffirmed March 2001 /JC-25 Committee | $30.00 |

# Displayed by Committee

## JC-10 Terms/Defin/Symbols

| | |
|---|---|
| **EIA 236-C** | COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES: |
| **EIA 321-C** | NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES: |
| **EIA 370-B** | DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES: |
| **EIA 471** | SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES: |
| **JEP 100** | TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993. |
| **JEP 103-A** | SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS |
| **JEP 120-A** | INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS: |
| **JEP 75** | LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A. |
| **JEP 99** | GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985. |
| **JESD 100-B** | TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND, MEMORY INTEGRATED CIRCUITS: |
| **JESD 30-B** | DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES: |
| **JESD 99-A** | TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES: |
| **JESD 99-1** | ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS: |
| **JEP 104-C** | REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES: |
| **JESD 77-B** | TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES: |
| **JESD 88** | DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, First Edition: |

## JC-11 Mechanical Pkg Outlines

| | |
|---|---|
| **EIA 308-A** | PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION: |
| **JEB 20** | ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS |
| **JEP 86-A** | RECOMMENDED PRACTICE FOR DUAL DIMENSIONING |
| **JEP 95 AUS** | ANNUAL UPDATING SERVICE: |
| **JEP 95** | JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS: |



Micron Technology Inc. et al.
Ex. 1017, p. 125

| | |
|---|---|
| JEP 95-1 | DESIGN REQUIREMENTS (Book 1, Section 4) |

## JC-13 Government Liaison

| | |
|---|---|
| EIA 390-A | STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS: |
| EIA 623 | PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS: |
| EIA 625 | REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A. |
| JEP 109-C | GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES: |
| JEP 112 | TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001 |
| JEP 114 | GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION: |
| JEP 121 | GUIDELINES FOR MIL-STD-883 SCREENING AND QCI OPTIMIZATION: |
| JEP 132 | PROCESS CHARACTERIZATION GUIDELINE: |
| JESD 16-A | ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM): |
| JESD 19 | GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A |
| JESD 27 | CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES: |
| JESD 40 | PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994 |
| JESD 42 | REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994. |
| JESD 49 | PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD): |
| JEP 144 | GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES |

## JC-13.2 Microelec. Devices

| | |
|---|---|
| JEP 101-C | JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: |
| JESD 26-A | GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001 |
| JESD 53 | MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: Rescinded, October 2002 |

## JC-13.4 Radiation Hardness

| | |
|---|---|
| JESD 57 | TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION: |
| JESD 89 | MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES: |

## JC-13.5 Committee on Hybrid

| | |
|---|---|
| EIA 557-A | STATISTICAL PROCESS CONTROL SYSTEMS: |
| JEP 105 | JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001 |
| JEP 107 | TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001 |
| JEP 133-A | GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS: |
| JEP 96 | GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES |
| JESD 9-A | METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS: |
| JESD 72 | TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS: |



Micron Technology Inc. et al.
Ex. 1017, p. 126

| | |
|---|---|
| JEP 142 | GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS: |

## JC-14 Quality/Reliability

| | |
|---|---|
| JEB 16 | USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS: |

## JC-14.1 Rel.Test Meth.Pkg.Dev.

| | |
|---|---|
| J-STD- 020-B | JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES: |
| J-STD- 033A | JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES: |
| JEP 113-B | SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES: |
| JEP 122-A | FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES: |
| JESD 22-A100-B | CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST: |
| JESD 22-A101-B | STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST: |
| JESD 22-A102-C | ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE: |
| JESD 22-A103-B | HIGH TEMPERATURE STORAGE LIFE: |
| JESD 22-A104-B | TEMPERATURE CYCLING: |
| JESD 22-A105-B | POWER AND TEMPERATURE CYCLING: |
| JESD 22-A106-A | THERMAL SHOCK: |
| JESD 22-A107-A | SALT ATMOSPHERE: |
| JESD 22-A109-A | HERMETICITY: |
| JESD 22-A110-B | HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST) |
| JESD 22-A113-B | PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING: |
| JESD 22-A114-B | ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM): |
| JESD 22-A115-A | ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM): |
| JESD 22-A117 | ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST: |
| JESD 22-B100-A | PHYSICAL DIMENSION: |
| JESD 22-B101 | EXTERNAL VISUAL: |
| JESD 22-B102-C | SOLDERABILITY: |
| JESD 22-B103-B | VIBRATION, VARIABLE FREQUENCY: |
| JESD 22-B104-B | MECHANICAL SHOCK: |
| JESD 22-B105-B | LEAD INTEGRITY: |
| JESD 22-B106-B | RESISTANCE TO SOLDERING TEMPERATURE FOR THROUGH-HOLE MOUNTED DEVICES: |
| JESD 22-B107-A | MARKING PERMANENCY: |
| JESD 22-B108 | COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES: |



Micron Technology Inc. et al.
Ex. 1017, p. 127

| | |
|---|---|
| JESD 22-B116 | WIRE BOND SHEAR TEST: |
| JESD 22-C100-A | HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999 |
| JESD 22-C101-A | FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS: |
| JESD 625-A | REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES: |
| JESD 22-B117 | BALL GRID ARRAY (BGA) BALL SHEAR: |
| JESD 78 | IC LATCH-UP TEST: |
| JESD 22-A108-B | TEMPERATURE, BIAS, AND OPERATING LIFE: |
| JESD 22-A118 | ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST: |
| JESD 22-B110 | SUBASSEMBLY MECHANICAL SHOCK: |
| JESD 22-A120 | TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN INTEGRATED CIRCUITS: |
| JESD 22-B109 | FLIP CHIP TENSILE PULL: |
| JEP 140 | BEADED THERMOCOUPLE TEMPERATURE MEASUREMENT OF SEMICONDUCTOR PACKAGES: |

## JC-14.1B JEDEC/IPC Joint Task

| | |
|---|---|
| J-STD- 035 | JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS: |

## JC-14.2 Wafer Level Reliab

| | |
|---|---|
| JEP 119 | A PROCEDURE FOR EXECUTING SWEAT: |
| JEP 128 | GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER LEVEL ELECTRICAL TESTING: |
| JESD 28-A | A PROCEDURE FOR MEASURING N-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS: |
| JESD 33-A | STANDARD METHOD FOR MEASURING AND USING THE TEMPERATURE COEFFICIENT OF RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE: |
| JESD 34 | FAILURE-MECHANISM-DRIVEN RELIABILITY QUALIFICATION OF SILICON DEVICES: |
| JESD 35-A | PROCEDURE FOR WAFER-LEVEL-TESTING OF THIN DIELECTRICS: |
| JESD 35-1 | ADDENDUM No. 1 to JESD35 - GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS: |
| JESD 35-2 | ADDENDUM No. 2 to JESD35 - TEST CRITERIA FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS: |
| JESD 37 | STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD: |
| JESD 60 | A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION AT MAXIMUM GATE CURRENT UNDER DC STRESS: |
| JESD 61 | ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE: |
| JESD 63 | STANDARD METHOD FOR CALCULATING THE ELECTROMIGRATION MODEL PARAMETERS FOR CURRENT DENSITY AND TEMPERATURE: |
| JEP 139 | GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING: |
| JESD 87 | STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS |
| JESD 28-1 | N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS: |
| JP 001 | FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites) |

## JC-14.3 Silicon Devices RQM

| | |
|---|---|
| EIA 659 | FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING (SUPERSEDES JESD29-A): SEE JESD659-A. |



Micron Technology Inc. et al.
Ex. 1017, p. 128

| | |
|---|---|
| JEP 131 | PROCESS FAILURE MODE AND EFFECTS ANALYSIS (FMEA): |
| JESD 29-A | FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996. |
| JESD 47-A | STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS: |
| JESD 50 | SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION: |
| JESD 62-A | OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS: |
| JESD 659-A | FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING: |
| JESD 69 | INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES: |
| JESD 74 | EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR ELECTRONIC COMPONENTS: |
| JESD 85 | METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS: |
| JESD 86 | ELECTRICAL PARAMETERS ASSESSMENT: |
| JEP 143 | SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES: |
| JESD 91 | METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC COMPONENT FAILURE MECHANISMS: |

## JC-14.4 Quality System Stand

| | |
|---|---|
| EIA 599-A | NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS: |
| EIA 670 | QUALITY SYSTEM ASSESSMENT (SUPERSEDES JESD39-A): |
| EIA 671 | COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A. |
| JEP 117 | GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997. |
| JEP 124 | GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999. |
| JEP 130 | GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING: |
| JEP 70-B | QUALITY AND RELIABILITY STANDARDS AND PUBLICATIONS: |
| JESD 31-B | GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES: |
| JESD 39-A | QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997. |
| JESD 43 | COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996. |
| JESD 46-B | CUSTOMER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS: |
| JESD 48-A | PRODUCT DISCONTINUANCE: |
| JESD 671-A | COMPONENT QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS (INCLUDING ADMINISTRATIVE QUALITY PROBLEMS): |

## JC-14.6 Failure Analysis

| | |
|---|---|
| JEP 134 | GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE ANALYSIS: |
| JEP 136 | SIGNATURE ANALYSIS: |
| JESD 38 | STANDARD FOR FAILURE ANALYSIS REPORT FORMAT: |

## JC-14.7 GaAs Rel. & Quality

| | |
|---|---|
| JEP 110 | GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS: |
| JEP 118 | GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING: |
| JES 2 | TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION: |

## JC-15 Elect./Thermal



Micron Technology Inc. et al.
Ex. 1017, p. 129

| | |
|---|---|
| **JEP 123** | GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS: |
| **JESD 51** | METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE) |
| **JESD 51- 1** | INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE): |
| **JESD 51- 2** | INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR): |
| **JESD 59** | BOND WIRE MODELING STANDARD: |

## JC-15.1 Thermal Character.

| | |
|---|---|
| **JEP 129** | THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP)- SUPERSEDED BY JESD51-4, September 1997. |
| **JESD 51- 3** | LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES: |
| **JESD 51- 4** | THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP): |
| **JESD 51- 5** | EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES WITH DIRECT THERMAL ATTACHMENT MECHANISMS: |
| **JESD 51- 6** | INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR): |
| **JESD 51- 7** | HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES: |
| **JESD 51- 8** | INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - JUNCTION-TO-BOARD: |
| **JESD 51- 9** | TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS: |
| **JESD 51-10** | TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS: |
| **JESD 51-11** | TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENT: |

## JC-15.2 Elec. Char. Tech.

| | |
|---|---|
| **JEP 126** | GUIDELINE FOR DEVELOPING AND DOCUMENTING PACKAGE ELECTRICAL MODELS DERIVED FROM COMPUTATIONAL ANALYSIS: |

## JC-16 Elec. Intrfcs/Pwr Supply

| | |
|---|---|
| **JESD 8- 1** | ADDENDUM No. 1 to JESD8: INTERFACE STANDARD FOR LOW VOLTAGE TTL-COMPATIBLE (LVTTL) VLSI DIGITAL CIRCUITS |
| **JESD 8- 2** | ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS: |
| **JESD 8- 3** | ADDENDUM No. 3 to JESD8 - GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: |
| **JESD 8- 4** | ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: |
| **JESD 8- 5** | ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT: |
| **JESD 8- 6** | ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL)- A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: |
| **JESD 8- 7** | ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE), AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT: |
| **JESD 8- 8** | ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: |
| **JESD 8- 9B** | ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002. |
| **JESD 67** | I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND |



Micron Technology Inc. et al.
Ex. 1017, p. 130

RECEIVER THRESHOLD:

| | |
|---|---|
| JESD 8- 1-A | INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS |
| JESD 8-B | INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS: |
| JESD 8-11 | ADDENDUM No. 11 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: |
| JESD 8-12 | 1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: |
| JESD 8-13 | SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400): |
| JESD 8-14 | 1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: |
| JESD 8-15 | STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18): |

## JC-22.1 Thyristors

| | |
|---|---|
| EIA 323 | AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES: |
| EIA 397-1 | ADDENDUM No. 1 TO EIA-397: |
| JEP 88 | THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS |
| JESD 41 | REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002. |
| EIA 397 | RECOMMENDED STANDARD FOR THYRISTORS: |

## JC-22.2 Rectifier Diodes

| | |
|---|---|
| EIA 282-A | STANDARD FOR SILICON RECTIFIER DIODES: SEE JESD282-B |
| JEP 87 | FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A. |
| JESD 14 | SEMICONDUCTOR POWER CONTROL MODULES: |
| JESD 4 | DEFINITION OF EXTERNAL CLEARANCE AND CREEPAGE DISTANCES OF DISCRETE SEMICONDUCTOR PACKAGES FOR THYRISTORS AND RECTIFIER DIODES: |
| JESD 45 | MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: Rescinded June 2002. Replaced by JESD282-B. |
| JESD 282-B | SILICON RECTIFIER DIODES: |

## JC-22.4 Signal Regltr Diodes

| | |
|---|---|
| EIA 286-A | STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: SEE JESD286-B. |
| JESD 307 | VOLTAGE REGULATOR DIODE NOISE VOLTAGE MEASUREMENT: |
| EIA 318-B | MEASUREMENT OF REVERSE RECOVERY TIME FOR SEMICONDUCTOR SIGNAL DIODES: |
| JESD 320-A | CONDITIONS FOR MEASUREMENT OF DIODE STATIC PARAMETERS: |
| JESD 381-A | METHOD OF DIODE Q MEASUREMENT: |
| JESD 482-A | LIST OF PREFERRED VALUES FOR USE ON VARIOUS TYPES OF SMALL SIGNAL AND REGULATOR DIODES: |
| JESD 531 | THERMAL RESISTANCE TEST METHOD FOR SIGNAL AND REGULATOR DIODES (FORWARD VOLTAGE, SWITCHING METHOD): |
| JEP 90 | THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. |
| JESD 5 | MEASUREMENT OF TEMPERATURE COEFFICIENT OF VOLTAGE REGULATOR DIODES: |
| JESD 286-B | STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: |

## JC-22.5 Transient Voltage Supp



Micron Technology Inc. et al.
Ex. 1017, p. 131

| | |
|---|---|
| **JESD 66** | TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE: |
| **TENTSTD 12** | STANDARD FOR SELENIUM SURGE SUPPRESSORS: |

## JC-25 Transistors

| | |
|---|---|
| **EIA 283** | TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A. |
| **EIA 284-A** | TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE: |
| **EIA 302** | RANGES AND CONDITIONS FOR SPECIFYING BETA FOR LOW POWER, AUDIO FREQUENCY TRANSISTORS FOR ENTERTAINMENT SERVICE: |
| **EIA 306** | MEASUREMENT OF SMALL SIGNAL HF, VHF, AND UHF POWER GAIN OF TRANSISTORS: |
| **EIA 311-A** | MEASUREMENT OF TRANSISTOR NOISE FIGURE AT MF, HF, AND VHF: |
| **JESD 313-B** | THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS: |
| **EIA 340** | STANDARD FOR THE MEASUREMENT OF CRE: |
| **EIA 353** | THE MEASUREMENT OF TRANSISTOR NOISE FIGURE AT FREQUENCIES UP TO 20 kHz BY SINUSOIDAL SIGNAL-GENERATOR METHOD: |
| **EIA 354** | THE MEASUREMENT OF TRANSISTOR EQUIVALENT NOISE VOLTAGE AND EQUIVALENT NOISE CURRENT AT FREQUENCIES OF UP TO 20 kHz: |
| **EIA 371** | THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO: |
| **EIA 372** | THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS: |
| **EIA 398** | MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE: |
| **JESD 419-A** | STANDARD LIST OF VALUES TO BE USED IN SEMICONDUCTOR DEVICE SPECIFICATIONS AND REGISTRATION FORMAT: |
| **EIA 435** | STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS: |
| **JEP 115** | POWER MOSFET ELECTRICAL DOSE RATE TEST METHOD: |
| **JEP 138** | USER GUIDELINES FOR IR THERMAL IMAGING DETERMINATION OF DIE TEMPERATURE: |
| **JEP 65** | TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS: |
| **JEP 69-B** | PREFERRED LEAD CONFIGURATION FOR FIELD-EFFECT TRANSISTORS: |
| **JEP 74** | STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996. |
| **JEP 84** | RECOMMENDED PRACTICE FOR MEASUREMENT OF TRANSISTOR LEAD TEMPERATURE: |
| **JESD 24** | POWER MOSFETS: |
| **JESD 24- 1** | ADDENDUM No. 1 to JESD24 - METHOD FOR MEASUREMENT OF POWER DEVICE TURN-OFF SWITCHING LOSS: |
| **JESD 24-10** | ADDENDUM No. 10 to JESD24 - TEST METHOD FOR MEASUREMENT OF REVERSE RECOVERY TIME trr FOR POWER MOSFET DRAIN-SOURCE DIODES: |
| **JESD 24-11** | ADDENDUM No. 11 to JESD24 - POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD: |
| **JESD 24- 2** | ADDENDUM No. 2 to JESD24 - GATE CHARGE TEST METHOD: |
| **JESD 24- 3** | ADDENDUM No. 3 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD): |
| **JESD 24- 4** | ADDENDUM No. 4 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR BIPOLAR TRANSISTORS (DELTA BASE-EMITTER VOLTAGE METHOD): |
| **JESD 24- 5** | ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD: |
| **JESD 24- 6** | ADDENDUM No. 6 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS: |
| **JESD 24- 7** | ADDENDUM No. 7 to JESD24 - COMMUTATING DIODE SAFE OPERATING AREA TEST PROCEDURE FOR MEASURING dv/dt DURING REVERSE RECOVERY OF POWER TRANSISTORS: |
| **JESD 24- 8** | ADDENDUM No. 8 to JESD24 - METHOD FOR REPETITIVE INDUCTIVE LOAD AVALANCHE |



Micron Technology Inc. et al.
Ex. 1017, p. 132

| | |
|---|---|
| | SWITCHING: |
| JESD 24- 9 | ADDENDUM No. 9 to JESD24 - SHORT CIRCUIT WITHSTAND TIME TEST METHOD: |
| JESD 25 | MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS: |
| JESD 6 | MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE: |
| JESD 10 | LOW FREQUENCY POWER TRANSISTORS: |

## JC-40 CMOS Digital Logic

| | |
|---|---|
| JEB 19 | RECOMMENDED CHARACTERIZATION OF MOS SHIFT REGISTERS: |
| JESD 36 | STANDARD DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE, 5 V TOLERANT CMOS LOGIC DEVICES: |
| JESD 52 | STANDARD FOR DESCRIPTION OF LOW VOLTAGE TTL-COMPATIBLE CMOS LOGIC DEVICES: |
| JESD 54 | STANDARD FOR DESCRIPTION OF 54/74ABTXXX AND 74BCXXX TTL-COMPATIBLE BiCMOS LOGIC DEVICES: |
| JESD 55 | STANDARD FOR DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE BiCMOS LOGIC DEVICES: |
| JESD 70 | 2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS: |
| JESD 73 | DESCRIPTION OF 5 V BUS SWITCH WITH TTL-COMPATIBLE CONTROL INPUTS: |
| JESD 80 | STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES: |
| JESD 64-A | STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES WITH 3.6 V CMOS TOLERANT INPUTS AND OUTPUTS: |
| JESD 75 | BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS: |
| JESD 82 | DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS: |
| JESD 76-1 | STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (WIDE RANGE OPERATION): |
| JESD 76-2 | STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (NORMAL RANGE OPERATION): |
| JESD 82-2 | STANDARD FOR DESCRIPTION OF A 3.3 V, 18-BIT, LVTTL I/O REGISTER FOR PC133 REGISTERED DIMM APPLICATIONS: |
| JESD 75-2 | BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS: |
| JESD 75-3 | BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS: |
| JESD 82-3A | DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS: |
| JESD 73-1 | STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES: |
| JESD 73-2 | STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS: |
| JESD 82-4A | STANDARD FOR DEFINITION OF THE SSTV16859 2.5 V, 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR STACKED DDR DIMM APPLICATIONS: |
| JESD 75-1 | BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16, 18, AND 20-BIT LOGIC FUNCTIONS USING A 54 BALL PACKAGE: |
| JESD 82-5 | STANDARD FOR DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH THE JESD21-C PC133 REGISTERED DIMM SPECIFICATION |
| JESD 82-1 | DEFINITION OF CV857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, AND PC2700 DIMM APPLICATIONS: |

## JC-42 for all 42.xx members

| | |
|---|---|
| JEP 102 | STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C. |
| JESD 21-C | CONFIGURATIONS FOR SOLID STATE MEMORIES: |

## JC-42.3 RAM Memories

| | |
|---|---|
| JEP 106-K | STANDARD MANUFACTURERS IDENTIFICATION CODE: |

## JC-42.4 Non-Volatile Memories



Micron Technology Inc. et al.
Ex. 1017, p. 133

| | |
|---|---|
| JEP 137-A | COMMON FLASH INTERFACE (CFI) IDENTIFICATION CODES: |
| JESD 68 | COMMON FLASH INTERFACE (CFI): |

## JEDEC BOD

| | |
|---|---|
| JEB 5-A | METHODS OF MEASUREMENT FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS: |

## JEDEC Council

| | |
|---|---|
| JEP 78 | RELATIVE SPECTRAL RESPONSE CURVES FOR SEMICONDUCTOR INFRARED DETECTORS: |

# Displayed by key words

TEMPORARILY REMOVED

**A**

| | |
|---|---|
| Abbreviations - Packages | JESD 30-B |
| Accelerated Moisture Resistance | JESD 22-A102-C<br>JESD 22-A118 |
| Acceleration Factor | JEP 122-A<br>JESD 85 |
| Acceleration Models | JESD 91 |
| Acoustic Microscopy | J-STD- 035 |
| Acronyms - packages - Packages - Semiconductor Devices | JESD 30-B |
| Activation Energy | JEP 122-A<br>JESD 85 |
| Administrative Quality Problems | JESD 671-A |
| Air Convection Cooled Life Test | EIA 323 |
| AlCu | JESD 87 |
| Alpha Particles | JESD 89 |
| Analysis - Heat Flow | JESD 51- 7 |
| Annex | SDRAM 3_20<br>MODULE 4_20_0 |
| Applications - Rugged | JESD 26-A |
| Archive | JEP 95 Index |
| Area Array | JESD 51- 9 |
| ASIC | JEP 116 |
| Assembling - Individual Components | JESD 14 |
| Assessing Compliance | EIA 670 |
| Assessment | JEP 143 |
| Assessment - Average Outgoing Quality | JESD 16-A |
| Assessment - Electrical Parameter | JESD 86 |
| assessment techniques | JEP 142 |
| Audit Checklist - Preparation | EIA 670 |
| Avalance | JESD 24- 5 |
| Avalanhce Switching | JESD 24- 8 |
| Average Outgoing Quality | JESD 16-A |

**B**

| | |
|---|---|
| B Series - CMOS Devices | JESD 13-B |
| Ball Grid | CO 029-H |
| Ball Grid Array | JESD 75-2<br>JESD 75-3<br>JESD 75-1<br>Design 4.17-A |



Micron Technology Inc. et al.
Ex. 1017, p. 134

| | |
|---|---|
| | MO 210G<br>MO 216-D |
| Ball Grid Array Pinouts | JESD 75 |
| Bare Die | JESD 49 |
| Barrier Materials | JESD 87 |
| Beaded | JEP 140 |
| Benchmark Set - Cell Based Integrated Circuits | JESD 12-2 |
| Beta | EIA 302 |
| BGA | MO 211-B<br>MO 221-C<br>Design 4.5-C<br>Design 4.7-C<br>JESD 75-2<br>JESD 75-3<br>MO 233-A<br>JESD 75-1<br>Design 4.17-A<br>MO 210G<br>MO 234-A<br>MO 233-B<br>PR N02-SR2 |
| BGA Ball Shear | JESD 22-B117 |
| Bias | JESD 22-A108-B |
| Bias Life | JESD 22-A100-B |
| Bias Life State-State Temperature Humidity | JESD 22-A101-B |
| BiCC | JESD 12-6 |
| BiCMOS | JESD 8- 6 |
| BiCMOS Logic Devices | JESD 54<br>JESD 55<br>JESD 70 |
| Bipolar | JESD 78 |
| Bipolar Logic Pinouts | JESD 2 |
| Bipolar Transistors | JESD 24- 4 |
| Bipolar Transistors - Insulated Gate | JESD 24- 6 |
| Bit Wide | SRAM 3_7_1<br>DRAM 3_9_1 |
| Bit Write | DRAM 3_9_5 |
| Bond Wire - Modeling | JESD 59 |
| Bridge Rectifier Assemblies | JESD 45 |
| Buffered SDRAM | MODULE 4_6_1 |
| Bump | PR N02-SR2 |
| Bus Switch | JESD 73<br>JESD 73-1<br>JESD 73-2<br>JESD 73-3<br>JESD 73-4 |
| Byte Wide | DRAM 3_9_3<br>SDRAM 3_11_3<br>EEPROM 3_5_1 |
| Byte Wide PROM | PROM 3_3_2 |
| Byte Wide ROM | ROM 3_2_1 |
| **C** | |
| Calculation - ELFR | JESD 74 |
| Calibration Procedure - Solar Cells | EIA 365 |
| Capacitance - Transistor | JESD 6 |
| Capacitance Model | JEP 123 |



Micron Technology Inc. et al.
Ex. 1017, p. 135

| | |
|---|---|
| Card | **MODULE 4_4_3** |
| Cards | **MODULE 4_3** |
| Catastrophic Failure | **JEP 134** |
| CDCV857 | **JESD 82** |
| Cell Based - Integrated Circuits | **JESD 12** |
| Cells - Photoconductive | **JEP 79** |
| Center Tap Terminated - CTT | **JESD 8- 4** |
| Ceramic Package | **JESD 27** |
| Certification | **EIA 599-A** |
| Certification - PIND Testing | **JEP 114** |
| CFI - Common Flash Interface | **JEP 137-A**<br>**JESD 68** |
| Chain Description File | **JESD 32** |
| Character Designation - LCD | **JESD 23** |
| Characterization | **JESD 86** |
| Characterization - Hybrid Polymeric Materials | **JEP 105** |
| Charge Pump | **JESD 73-2** |
| Charged Device Model (CDM) | **JESD 22-C101-A** |
| Chip - Thermal Test | **JESD 51- 4** |
| Chip Carrier | **MO 217-B** |
| Chip Carrier - Leadless Pinouts | **JESD 1** |
| Chip Carrier Pinouts | **JESD 11** |
| Chip Carriers | **JESD 2** |
| Circuit Support Films | **JEP 112** |
| Class B Microcircuits | **JEP 101-C** |
| Classifications | **JEP 103-A** |
| Clearance Distance | **JESD 4** |
| Clock Driver | **JESD 82-1** |
| Clock Drivers | **JESD 65-A** |
| CMOS | **JEP 116**<br>**JESD 8- 6**<br>**JESD 78**<br>**JESD 76-1**<br>**JESD 76-3**<br>**JESD 8-14** |
| CMOS Devices | **JESD 20**<br>**JESD 20** |
| CMOS Devices - 4000 | **JESD 11** |
| CMOS Devices - B Series | **JESD 13-B** |
| CMOS Devices - Fast | **JESD 18-A** |
| CMOS Devices - Gate Array | **JESD 12-3** |
| CMOS Devices - High Speed | **JESD 7-A** |
| CMOS Devices - Semicustom ICs | **JESD 12-4** |
| CMOS Interface | **JESD 8-14** |
| CMOS Logic Device - TTL Compatible - CMOS Logic Devices | **JESD 36** |
| CMOS Logic Devices | **JESD 52**<br>**JESD 80**<br>**JESD 64-A**<br>**JESD 76-2** |
| CMOS Logic Devices - 1.8 V | **JESD 76** |
| Collector-Base Time Constant | **EIA 284-A** |
| Color Coding | **EIA 236-C** |
| Column | **MO 158-D** |
| Commercial Practices | **JESD 31-B** |



Micron Technology Inc. et al.
Ex. 1017, p. 136

| | |
|---|---|
| Commercial Semiconductor Devices - Distributor Requirements | **JESD 31-B** |
| Common Flash Interface - CFI | **JESD 68** |
| Common-Emitter Input | **EIA 284-A** |
| Component Assembly | **JEP 140** |
| Component Obsolescence | **JESD 53** |
| Component Quality Problem | **JESD 671-A** |
| Conduction Cooled Power Transistors | **JESD 313-B** |
| Configurable Communication Voltage | **JESD 67** |
| Control Inputs | **JESD 73** |
| Coplanarity Test - Surface Mount Devices | **JESD 22-B108** |
| Corrective Action Requirements | **JESD 671-A** |
| Corrosion | **JEP 122-A** |
| Cosmic Rays | **JESD 89** |
| Covers - Metal Package Specification | **JESD 9-A** |
| Cre Measurement | **EIA 340** |
| Creepage Distance | **JESD 4** |
| CSP | **MO 211-B** |
| Current Density | **JESD 63** |
| Customer Notification | **JESD 48-A** |
| Customer-Supplied Background Information | **JEP 134** |
| CV857 | **JESD 82-1** |
| Cycling - Power and Temperature | **JESD 22-A105-B** |
| **D** | |
| Data Sheet Disclaimers | **JEP 103-A** |
| Data Transfer Format | **JESD 3-C** |
| dc interface | **JESD 82-1** |
| DC Interface Parameters | **JESD 80** |
| DC Stress | **JESD 28-A**<br>**JESD 60** |
| DDR | **MODULE 4_5_09**<br>**MODULE 4_5_10**<br>**JESD 82-3A**<br>**JESD 73-3**<br>**JESD 73-4**<br>**MODULE 4_20_6**<br>**MO 206-C**<br>**PR N02-NM4A**<br>**PR N02-NM2**<br>**PR N02-NM6** |
| DDR - Double Data Rate | **JESD 79-2** |
| DDR DIMM | **MODULE 4_20_4** |
| DDR200 | **JESD 82**<br>**JESD 82-1** |
| DDR266 | **JESD 82**<br>**JESD 82-1** |
| DDR333 | **JESD 82-1** |
| DDRII | **PR N02-DR3**<br>**PR N02-DR4** |
| DDRII Interface | |
| Delta Base-Emitter Voltage Method | **JESD 24- 4** |
| Delta Source-Drain Voltage Method | **JESD 24- 3** |
| Description - Fast CMOS TTL Compatible Logic | **JESD 18-A** |
| Description - Problem Solving Tools | **JEP 132** |
| Design | **Design 4-A** |



Micron Technology Inc. et al.
Ex. 1017, p. 137

| | |
|---|---|
| | **Design 4.7-C**<br>**MODULE 4_20_6** |
| Design - Testability | **JESD 12-5** |
| design considerations | **JEP 142** |
| Design Requirements - Leaded Surface Mount | **JESD 51- 3** |
| Design Specification | **MODULE 4_20_2** |
| Designation of Units - Multiple Unit Devices | **EIA 321-C** |
| Designation System | **EIA 370-B** |
| Detectors - Infrared | **JEP 78** |
| Device | **SDRAM 3_20** |
| Device Interchageability | **EIA 340** |
| Device Specification - BiCMOS Logic Devices | **JESD 55** |
| Device Type | **JEP 95 Index** |
| Dictionary | **JESD 88** |
| Die Size | **MO 211-B**<br>**MO 207-E** |

**E**

| | |
|---|---|
| Early Life - Failure Rate Calculation | **JESD 74** |
| ECL | **JESD 12-6** |
| ECL - Emitter-Coupled Logic | **JESD 8- 2** |
| EDO-DRAM | **MODULES 4_5_13** |
| EEPROM | **EEPROM 3_5_2**<br>**MODULE 4_4_7**<br>**EEPROM 3_5_1**<br>**PR N02-NV2**<br>**PR N02-NV1** |
| Effects | **JEP 131** |
| Eight Byte | **MODULE 4_5** |
| Electrical Levels - B Series CMOS Devices | **JESD 13-B** |
| Electromigration | **JESD 63**<br>**JESD 87**<br>**JP 001** |
| Electromigration Test | **JESD 61** |
| Electronic Components | **JESD 74** |
| Electronic Components - Management System | **JESD 62-A** |
| ELFR - Early Life Failure Rate | **JESD 74** |
| EM | **JESD 87** |
| Emitter-Coupled Logic - ECL | **JESD 8- 2** |
| Encapsulated Electronic Components | **J-STD- 035** |
| Encapsulated Microcircuits | **JESD 26-A** |
| Endurance and Data Retention Test | **JESD 22-A117** |
| Environment of Life Test for Lead-Mounted Devices | **EIA 323** |
| Environmental | **PR N02-NM1A** |
| Environmental Conditions | **JESD 51- 2** |
| Environmental Conditions - Forced Convection | **JESD 51- 6** |
| EP-7 | JM 7 |
| EP18 | **JM 18-F** |
| Equivalent Noise Voltage | **EIA 354** |
| ESD - Charged Device Model | **JESD 22-C101-A** |
| ESD - Electrostatic Sensitive Device | **EIA 471** |
| ESD - Electrostatic Sensitive Devices | **JESD 625-A** |
| ESD - Symbol and Label | **EIA 471** |
| ESDS Devices | **JESD 625-A** |



Micron Technology Inc. et al.
Ex. 1017, p. 138

| | |
|---|---|
| Evaluation | **JESD 22-A103-B** |
| Evaluation - Polymeric Materials | **JESD 72** |
| External Visual | **JESD 22-B101** |
| Extremely Thin | **MO 221-C** |

**F**

| | |
|---|---|
| F-XBGA | **MO 207-E** |
| Failure | **JESD 91** |
| Failure Analysis | **JEB 16**<br>**JEP 136** |
| Failure Analysis - Report Format | **JESD 38** |
| Failure Analysis Laboratory | **JEP 134** |
| Failure Mechanism | **JEP 122-A** |
| Failure Mechanisms | **JESD 91** |
| Failure Mode | **JEP 131** |
| Failure Models | **JEP 122-A** |
| Failure Modes - BGA Ball Shear | **JESD 22-B117** |
| Failure-Mechanism-Driven | **JESD 659-A** |
| Failures in Time | **JESD 85** |
| FBGA | **MO 228-A** |
| FET | **JESD 73-3** |
| FET Life Testing | **JEP 118** |
| FET Switch | **JESD 73-4** |
| FETs - Field Effect Transistors | **JES 2** |
| FETs - Lead Configuration | **JEP 69-B** |
| Field Programmable Devices | **JESD 3-C** |
| File Naming | **JM 19** |
| Fine | **MO 233-A**<br>**MO 233-B** |
| Fine Pich | **Design 4.5-C**<br>**MO 220-D** |
| Fine Pitch | **MO 208-C**<br>**MO 207-E**<br>**MO 210G**<br>**MO 207-F** |
| Finite Population Analysis | **JEP 136** |
| FITs | **JESD 85** |
| Flange | **TO 251-D**<br>**TO 252-D** |
| Flange mounted | **TO 220-K**<br>**MO 235-A** |
| Flash | **PR N02-NV1** |
| Flash Families | **JESD 68** |
| Flat | **MO 229-B**<br>**MO 232-A**<br>**MO 220-D** |
| Flat Lead | **DO 219-B** |
| Flatpack | **Design 4-A** |
| Flip Chip | **JESD 22-B109** |
| FMEA - Failure Mode Effects Analysis | **JEP 131** |
| Forced Convection (Moving Air) | **JESD 51- 6** |
| Forward Current Transfer Ratio | **EIA 371** |
| Forward Switching Characteristics | **JESD 286-B** |
| Forward Voltage | **JESD 531** |
| foundry | **JP 001** |



Micron Technology Inc. et al.
Ex. 1017, p. 139

| | |
|---|---|
| Four Byte | MODULE 4_4_TOC |
| Frequency Variable | JESD 22-B103-B |
| Functional Failure | JEP 134 |
| **G** | |
| GaAs FETs | JEP 110<br>JEP 118 |
| GaAs Power FETs | JES 2 |
| Gas Analysis | JEP 144 |
| Gate Array | JESD 12-3 |
| Gate Arrays | JESD 12-1-B |
| Gate Arrays - Performance | JESD 12 |
| Gate Charge | JESD 24- 2 |
| Gate Current | JESD 60 |
| gate oxide integrity | JP 001 |
| Gate Resistance - Power MOSFET | JESD 24-11 |
| Gating Microcircuits | EIA 390-A |
| Gaussian | EIA 354 |
| Government Contractors | EIA 599-A<br>JESD 53 |
| Grid Array | MO 158-D |
| Gunning Transceiver Logic - GTL | JESD 8- 3 |
| **H** | |
| Half-period Jitter | JESD 65-A |
| Handling | J-STD- 033A<br>Design 4.10D<br>CO 034-C<br>CO 029-H |
| HAST | JESD 22-A118 |
| HBM | JESD 22-A114-B |
| HCI | JESD 28-1 |
| header | TO 220-K |
| Heat Sink | MO 230-A |
| Heavy Ion Irradiation | JESD 57 |
| Hermeticity | JESD 22-A109-A |
| High Reliability | JESD 49 |
| High Speed - CMOS Devices | JESD 7-A |
| High Speed Interface - Digital Integrated Circuits | JESD 8- 3 |
| High Speed Transceiver Logic - HSTL | JESD 8- 6 |
| High Temperature Storage | JESD 22-A103-B |
| High-Speed - CMOS Devices | JESD 20<br>JESD 20 |
| Highly Accelerated Temperature and Humidity | JESD 22-A110-B |
| Hot Carrier | JESD 60<br>JESD 28-1 |
| Hot Carrier Induced Degradation | JESD 28-A |
| hot carrier integrity | JP 001 |
| Hot Electrons | JESD 28-1 |
| HSTL | JESD 8-11 |
| Hybrid | JEP 142 |
| Hybrid Microcircuits | JEP 133-A |
| Hybrid Microelectronic Applications | JEP 107 |
| Hybrid Polymeric Materials | JEP 105 |
| **I** | |



Micron Technology Inc. et al.
Ex. 1017, p. 140

| | |
|---|---|
| I/O Burst | **PR N02-SR2** |
| I/O Drivers | **JESD 67** |
| I/O Interface | **JESD 8-15** |
| Identification Code | **JEP 106-K** |
| Identification Codes - CFI | **JEP 137-A** |
| Impedance | **JESD 67** |
| In-line | **MO 231-A** |
| In-Process Data | **EIA 557-A** |
| Index | **JEP 95 Index** |
| Index of Terms | **JEP 120-A** |
| Inductance Model | **JEP 123** |
| Information Requirements - Qualification of Silicon Devices | **JESD 69** |
| Infrared - Detectors | **JEP 78** |
| Inline | **MO 206-C** |
| Input and Output - 5 V Tolerant | **JESD 70** |
| Inputs and Outputs - CMOS Tolerant | **JESD 64-A** |
| insertion | **TO 251-D** |
| Insulated Gate Bipolar Transistors (IGBT) | **JESD 24- 6** |
| Integrated Circuit Thermal Measurement | **JESD 51- 1** |
| Integrated Circuits | **JESD 8- 2**<br>**JESD 47-A** |
| Integrated Circuits - Cell Based | **JESD 12-2** |
| Integrated Circuits - Interface Levels | **JESD 8-B** |
| inter/intra-metal dielectric integrity | **JP 001** |
| Interface | **JESD 8-11** |
| Interface Levels - 5 V Operation | **JESD 12-6** |
| Interface Levels - ECL | **JESD 8- 2** |
| Interface Levels - Integrated Circuits | **JESD 8-B** |
| Interface Standard - Semicustom ICs | **JESD 12-6** |
| Introduction | **SPD 4_1_TOC**<br>**MODULE 4_0** |
| IR - Infrared | **JEP 138** |
| IR Thermal Imaging | **JEP 138** |
| Isothermal Test | **JESD 61** |
| ISP Chain Device | **JESD 32** |
| **J** | |
| J-Lead | **Design 13** |
| JEDEC Committees | **JM 18-F** |
| JEDEC Manual | **JM 19** |
| JEDEC Type Registration - Outline Drawings | **EIA 308-A** |
| JEP95 | **JEP 95 Index** |
| Jitter | **JESD 65-A** |
| JTAG | **JESD 71** |
| Junction-to-Board | **JESD 51- 8** |
| **K** | |
| Known Good Die - KGD | **JESD 49** |
| **L** | |
| Label - Electrostatic Sensitive Devices | **EIA 471** |
| Labels - Moisture Sensitive | **JEP 113-B** |
| Latch-up | **JESD 78** |
| Lead Configuration - FETs | **JEP 69-B** |



Micron Technology Inc. et al.
Ex. 1017, p. 141

| | |
|---|---|
| Lead Integrity | **JESD 22-B105-B** |
| Lead Temperature - Transistor | **JEP 84** |
| Leadless Pinouts - Chip Carriers | **JESD 1** |
| Letter Symbols | JEB 15<br>**JEP 104-C** |
| LFBGA | **JESD 75** |
| Life Testing - Lead Mounted Semiconductor Devices | **EIA 323** |
| Linears | **JESD 1** |
| Liquid Crystal Devices - LCD | **JESD 23** |
| Lock | **JESD 65-A** |
| Logic Circuits - HC and HCT | **JESD 11** |
| Logic Device Programmer | **JESD 3-C** |
| Logic Functions | **JESD 75-1** |
| Logic Gating Microcircuits | **EIA 390-A**<br>**JEB 5-A** |
| Logic Interface Levels - CMOS | **JESD 12-6** |
| Logic Switching | **JESD 8- 9B** |
| Lognormal Analysis | **JESD 37** |
| Low Frequency - Power Transistors | **JESD 10** |
| Low Power CMOS | **JESD 8-13** |
| Low Power Transistors | **EIA 372** |
| Low Profile | **MO 204-B**<br>**JESD 75**<br>**CO 034-C**<br>**MO 234-A** |
| Low Voltage | **JESD 76** |
| Low Voltage - CMOS Devices | **JESD 52** |
| Low Voltage - CMOS Logic Devices | **JESD 36** |
| LVCMOS | **JESD 8- 4**<br>**JESD 8-11** |
| LVCMOS-Compatible Circuits | **JESD 8-B** |
| LVTTL | **JESD 8- 4**<br>**JESD 82-2** |
| LVTTL-Compatible Circuits | **JESD 8-B** |

**M**

| | |
|---|---|
| Macrocell Types | **JESD 12-3** |
| Management - Component Obsolescence | **JESD 53** |
| Manufacturers Identification Code | **JEP 106-K** |
| Marking Permanency | **JESD 22-B107-A** |
| Master | **JEP 95 Index** |
| Matrix | **Design 4.10D** |
| Maverick Product Elimination | **JESD 50** |
| Maximum Ratings - Power Transistors | **JEP 65** |
| MCM | **JEP 142** |
| Measurement | **Design 4.17-A** |
| Measurement - Diode Static Parameters | **JESD 320-A** |
| Measurement - dv/dt During Reverse Recovery | **JESD 24- 7** |
| Measurement - Package Inductance/Capacitance Model Parameters | **JEP 123** |
| Measurement - Power Device Turn-Off Switching Loss | **JESD 24- 1** |
| Measurement - Reverse Recovery Time | **EIA 318-B** |
| Measurement - Reverse Recovery Time (trr) | **JESD 24-10** |
| Measurement - Scattering Parameters | **JESD 25** |
| Measurement - Small Signal HF | **EIA 306** |



Micron Technology Inc. et al.
Ex. 1017, p. 142

| | |
|---|---|
| Measurement - Small Value Transistor Capaitance | **JESD 6** |
| Measurement - Static and Dynamic | **JEB 5-A** |
| Measurement - Temperature Coefficient | **JESD 33-A**<br>**JESD 5** |
| Measurement - Thermal Resistance | **JESD 45** |
| Measurement - Thermal Resistance of GaAs FETs | **JEP 110** |
| Measurement - Transistor Capacitance | **EIA 398** |
| Measurement - Transistor Lead Temperature | **JEP 84** |
| Measurement - Transistor Noise | **EIA 353** |
| Measurement of Cre | **EIA 340** |
| Mechanical Shock | **JESD 22-B104-B** |
| Mechanical Shock - Subassembly | **JESD 22-B110** |
| Memory | **MO 206-C** |
| Memory Integrated Circuits | **JEP 104-C** |
| Memory Integrated Circuits - Symbols | **JESD 100-B** |
| Memory Modules | **JESD 82-5** |
| Metal - Package Specification | **JESD 9-A** |
| Metal Enclosures | **EIA 398** |
| Metal Voiding | **JEP 139** |
| Metallization Line | **JESD 33-A** |
| Metallization Lines | **JESD 61** |
| Methodology | **Design 4.17-A** |
| Metric | **Design 13** |
| Micro | **MO 214-B** |
| Microcircuits - Class B | **JEP 101-C** |
| Microcomputers | **JEP 104-C** |
| Microcomputers - Symbols | **JESD 100-B** |
| Microelectronic Applications | **JEP 112** |
| Microelectronic Packages - Ceramic | **JESD 27** |
| Microelectronics Packages | **JESD 9-A** |
| Microprocessors | **JEP 104-C** |
| Microprocessors - Symbols | **JESD 100-B** |
| Military Practices | **JESD 31-B** |
| Military Semiconductor Devices - Distributor Requirements | **JEP 109-C** |
| MM | **JESD 22-A115-A** |
| MMIC Life Testing | **JEP 118** |
| Model Development | **JESD 91** |
| Modeling - Bond Wire | **JESD 59** |
| Module | **MODULE 4_2**<br>**MODULE 4_3**<br>**MODULE 4_4_TOC**<br>**MODULE 4_4_1**<br>**MODULE 4_4_2**<br>**MODULE 4_4_3**<br>**MODULE 4_4_4**<br>**MODULE 4_4_6**<br>**MODULE 4_4_7**<br>**MODULE 4_4_8**<br>**MODULE 4_5**<br>**MODULE 4_5_1**<br>**MODULE 4_5_2**<br>**MODULE 4_5_3**<br>**MODULE 4_5_5**<br>**MODULE 4_5_6**<br>**MODULE 4_5_09**<br>**MODULE 4_5_10** |



Micron Technology Inc. et al.
Ex. 1017, p. 143

| | |
|---|---|
| | **MODULE 4_6**<br>**MODULE 4_6_1**<br>**MODULE 4_5_11**<br>**MODULE 4_20_0**<br>**MODULE 4_20_1**<br>**MODULE 4_0** |
| Modules | **MODULE 4_20_4**<br>**MODULE 4_20_3**<br>**MODULE 4_20_2**<br>**JESD 82-2** |
| Moisture | **J-STD- 033A** |
| Moisture Resistance | **JESD 22-A118** |
| Moisture Sensitive - Symbol and Labels | **JEP 113-B** |
| Moisture Sensitivity | **J-STD- 020-B** |
| Monolithic Processing Technologies | **JESD 14** |
| MOS | **SRAM 3_07_07**<br>**SRAM 3_07_08** |
| MOSFET | **JESD 28-1** |
| MOSFETs | **JESD 24- 3**<br>**JESD 60** |
| MPDRAM | **MODULE 4_4_6** |
| Multi Chip Module | **JEP 142** |
| Multichip Modules | **JEP 133-A** |
| **N** | |
| N-Channel | **JESD 28-1** |
| N-Channel MOSFET | **JESD 28-A** |
| National Electronic Process Certification | **EIA 599-A** |
| Natural Convection (Still Air) | **JESD 51- 2** |
| NFET Switch | **JESD 73-1**<br>**JESD 73-2** |
| Nibble Wide | **SRAM 3_7_4**<br>**DRAM 3_9_2**<br>**SDRAM 3_11_2** |
| Nibble Wide PROM | **PROM 3_3_1** |
| Nibble Wide SRAM | **SRAM 3_7_3** |
| NMOS | **JESD 78** |
| NMOS FET | **JESD 73** |
| No Lead | **MO 208-C**<br>**MO 229-B**<br>**MO 232-A**<br>**MO 220-D**<br>**MO 220-E** |
| Noise Detection - Particle Impact | **JEP 114** |
| Noise Figure Measurement | **EIA 311-A** |
| Noise Margin Measurements | **EIA 390-A** |
| Noise Voltage | **EIA 354** |
| Noise Voltage Measurement | **JESD 307** |
| Nominal Supply Voltage - 2.5 V | **JESD 80** |
| Nonhermetic | **J-STD- 020-B**<br>**J-STD- 035** |
| Nonterminated | **JESD 8-14** |
| Nonterminated - Digital Integrated Circuits | **JESD 8- 5**<br>**JESD 8- 7** |
| Nonvolatile Memories | **JESD 22-A103-B** |
| Nonvolatile RAM | **NVRAM 3_6** |
| Normal Range | **JESD 76-2** |



Micron Technology Inc. et al.
Ex. 1017, p. 144

| | |
|---|---|
| Normal Range - Power Supply Voltage | **JESD 8- 5**<br>**JESD 8- 7** |
| Numbering - Liked Named Terminal Functions | **EIA 321-C** |
| NVRAM | **NVRAM 3_6** |
| **O** | |
| One Byte | **MODULE 4_2** |
| Ongoing Process Analysis | **JEP 136** |
| Operating Life | **JESD 22-A108-B** |
| Operating Voltages | **JESD 80** |
| Operating Voltages - ECL | **JESD 8- 2** |
| Operator Training - PIND Testing | **JEP 114** |
| Optional Features | **DRAM 3_9_5** |
| Optoelectronic | **JEP 104-C** |
| Organic Materials | **JESD 22-A120** |
| Outlier Identification | **JESD 62-A** |
| Outline Drawings - Solid State Products | **EIA 308-A** |
| Output Buffer Supply Voltage | **JESD 8- 6** |
| Output Drivers | **JESD 8- 9B** |
| **P** | |
| P-Channel - MOSFET | **JESD 60** |
| Package | **MO 230-A** |
| Package - Metal | **JESD 9-A** |
| Package Designators | **JESD 30-B** |
| Packing | **J-STD- 033A** |
| Parametric Failure | **JEP 134** |
| Parametric Shift | **JESD 86** |
| Particle Getters | **JEP 107** |
| Parts Per Million (PPM) - Quality Assessment | **JESD 16-A** |
| Parts Selection | **EIA 623** |
| PC-133 | **MODULE 4_20_3**<br>**MODULE 4_20_2** |
| PC-2700 | **PR N02-NM4A** |
| PC133 | **JESD 82-2**<br>**PR N02-NM3**<br>**JESD 82-5** |
| PC1600 | **MODULE 4_20_5**<br>**MODULE 4_20_4**<br>**JESD 82-1** |
| PC200 | **JESD 79-2** |
| PC2100 | **MODULE 4_20_5**<br>**MODULE 4_20_4**<br>**JESD 82-1** |
| PC266 | **JESD 79-2** |
| PC2700 | **MODULE 4_20_6**<br>**PR N02-NM6**<br>**JESD 82-1** |
| PCN - Product Chance Notification | **JESD 46-B** |
| PEMM Families | **MODULES 4_5_13** |
| Performance Parameters - CMOS Devices | **JESD 12-4** |
| peripheral | **TO 252-D** |
| Peripheral Leaded | |
| peripheral terminals | **TO 220-K** |
| perripheral | **TO 251-D** |
| Persson and Rootzen Method | **JESD 37** |



Micron Technology Inc. et al.
Ex. 1017, p. 145

| | |
|---|---|
| PGA | **JESD 51-11** |
| Photoconductive Cells | **JEP 79** |
| Physical Dimensions | **JESD 22-B100-A** |
| Pin 1 | **MO 220-E** |
| PIND - Particle Impact Noise Detection | **JEP 114** |
| Pinout Logic | **JESD 75-3** |
| Pinout. | **PR N02-SR1** |
| Pinouts | **JESD 1**<br>**JESD 75-2**<br>**JESD 75-1** |
| plasma-process | **JP 001** |
| Plastic | **MO 153-F**<br>**MO 204-B**<br>**MO 208-C**<br>**MO 230-A**<br>**MO 232-A**<br>**DO 219-B**<br>**MO 187-D**<br>**MO 235-A**<br>**TO 261-C**<br>**MO 137-B** |
| Plastic - Encapsulated Microcircuits | **JESD 26-A** |
| PLL | **JESD 65-A**<br>**JESD 82-5**<br>**JESD 82-1** |
| PLL Clock Driver | **JESD 82** |
| Polymeric Material | **JESD 72** |
| Potential Contributors | **JEP 144** |
| Power Control Modules | **JESD 14** |
| Power MOSFET | **JESD 24-11** |
| Power MOSFET Drain-Source Diodes | **JESD 24-10** |
| Power MOSFETs | JESD 24 |
| Power MOSFETs - Dose Rate | **JEP 115** |
| Power Supply Interface | **JESD 8-12** |
| Power Supply Voltage - Wide Range | **JESD 8- 5** |
| Power Transistors | **JESD 24- 7** |
| Power Transistors - Low Frequency | **JESD 10** |
| Power Transistors - Maximum Rating Verifications | **JEP 65** |
| PQFP | **MO 204-B**<br>**PR N02-NV2** |
| Preconditioning of Plastic Surface Mount Devices | **JESD 22-A113-B** |
| Preferred Values - Small Signal Diodes | **JESD 482-A** |
| Preliminary | **PR N02-SR1** |
| Preliminary Release | **PR N02-DR2** |
| Preparation of Outline Drawings | **EIA 308-A** |
| Probe - Pad Sizes and Layouts | **JEP 128** |
| Problem Analysis | **JESD 671-A** |
| Process Characterization. Problem Solving Tools | **JEP 132** |
| Procurement Quality | **EIA 623** |
| Product Discontinuance | **JESD 48-A** |
| Product Elimination - Maverick | **JESD 50** |
| Product Life Cycle - PLC | **JESD 48-A** |
| Product Reliability - Latch-up | **JESD 78** |
| Product-Documentation Classifications | **JEP 103-A** |



Micron Technology Inc. et al.
Ex. 1017, p. 146

| | |
|---|---|
| Product/Process Changes | **JESD 46-B** |
| Programmable Devices | **JESD 71** |
| Programmable Language | **JESD 71** |
| Programmable Logic Device | **JESD 3-C** |
| Programming Failure | **JEP 134** |
| Pseudo-Static RAM | **PSRAM 3_08** |
| PSRAM | **PSRAM 3_08** |

**Q**

| | |
|---|---|
| Q Measurement | **JESD 381-A** |
| QCI Optimization | **JEP 121** |
| QFN | **MO 220-C**<br>**MO 220-E** |
| Quad | **MO 208-C**<br>**MO 217-B**<br>**Design 4-A**<br>**MO 220-D** |
| Qualification | **JEP 143** |
| Qualification of Silicon Devices | **JESD 69** |
| Qualifications | **JESD 47-A** |
| Quality and Reliability - Standards and Publications | **JEP 70-B** |
| Quality Levels - Outgoing | **JESD 16-A** |
| Quality System Assessment | **EIA 670** |
| Quick Reference Guide | JEB 15 |

**R**

| | |
|---|---|
| R-PDSO-G | **TO 261-C**<br>**MO 137-B** |
| R-PSFM-G | **MO 235-A** |
| R-PSIP-Fxx | **MO 231-A** |
| Radiation-Hardness | **JEP 133-A** |
| RAM - Random Access Memory | **JESD 79-2** |
| Raw Card | **PR N02-NM3** |
| Receiver Type | **JESD 67** |
| Receiving Inspection | **EIA 623** |
| Rectangular | **MO 233-A**<br>**MO 207-F**<br>**MO 234-A**<br>**MO 216-D** |
| Rectifier Diodes | **JESD 4**<br>**JESD 282-B** |
| Rectifier Stacks | **JESD 282-B** |
| Reflow | **J-STD- 020-B**<br>**J-STD- 033A** |
| Refresh Control | **DRAM 3_9_5** |
| Register | **JESD 82-2** |
| Registered | **MODULE 4_5_07** |
| Registered Buffer | **JESD 82-4A** |
| Registered DDR DIMM Applications | **JESD 82** |
| Registration Format | **JESD 419-A** |
| Registration List - Solid State Products | JEP 64 |
| Registration Procedures | **JESD 10** |
| Regtangular | **MO 233-B** |
| Release 10 | **TOC21C R11** |
| Reliability | **JEP 139**<br>**JEP 143** |



Micron Technology Inc. et al.
Ex. 1017, p. 147

| | |
|---|---|
| Reliability Monitoring | **JESD 31-B**<br>**JESD 659-A** |
| Reliability Monitoring - Electrostatic-Discharge Sensitive Devices | **JESD 625-A** |
| Reliability Monitoring - Requirements | **JEP 101-C** |
| Report Format - Failure Analysis | **JESD 38** |
| Residual | **JEP 144** |
| Resistance - Thermal for Signal /Regulator Diodes | **EIA 435** |
| Reverse Recovery Characteristics - Silicon Diodes | **JESD 41** |
| Reverse Recovery Time - Measurement of | **JESD 24-10** |
| Reverse Recovery Time - Signal Diodes | **EIA 318-B** |
| RF Admittance Bridge | **JESD 381-A** |
| ROM DIMM | **MODULE 4_4_8** |
| Rugged Applications | **JESD 26-A** |

**S**

| | |
|---|---|
| Salt Atmosphere | **JESD 22-A107-A** |
| Scalable Signaling | **JESD 8-13** |
| Scattering Parameters | **JESD 25** |
| Scope | **JM 18-F** |
| Screening | **JESD 22-A103-B** |
| Screening - MIL-STD-883 | **JEP 121** |
| SDR | **MODULE 4_5_11**<br>**PR N02-NM3** |
| SDRAM | **SDRAM 3_11_2**<br>**SDRAM 3_11_3**<br>**SDRAM 3_11_4**<br>**MODULE 4_4_8**<br>**MODULE 4_5_2**<br>**MODULE 4_5_6**<br>**MODULE 4_5_11**<br>**MODULES 4_5_13**<br>**MODULE 4_5_07**<br>**JESD 79-2**<br>**MODULE 4_20_6**<br>**PR N02-NM3**<br>**PR N02-NM4A**<br>**PR N02-NM1A**<br>**PR N02-DR1** |
| SDRAM. DDRII | **MO 237-A** |
| SDRAM. SPD | **SPD 4_1_2_5** |
| Semiconductor | **JEP 104-C** |
| Semiconductor Device Failure | **JEP 134** |
| Semiconductor Devices - Designation System | **EIA 370-B** |
| Semiconductor Power Control Modules - SPCM | **JESD 14** |
| Semiconductor Suppliers - User Notification | **JESD 46-B** |
| Semicustom Design - ASIC | **JEP 116** |
| Semicustom Integrated Circuits | **JESD 12-1-B**<br>**JESD 12-6** |
| Sensitivity Testing | **JESD 22-A114-B**<br>**JESD 22-A115-A** |
| Serial Data | **DRAM 3_9_5** |
| SGRAM | **MODULE 4_5_09**<br>**MODULE 4_5_10** |
| SGRAM/SDRAM | **MODULES 4_5_8** |
| Shipping | **J-STD- 033A**<br>**Design 4.10D** |



Micron Technology Inc. et al.
Ex. 1017, p. 148

| | |
|---|---|
| | **CO 034-C**<br>**CO 029-H** |
| Short Circuit Withstand Time | **JESD 24- 9** |
| Shrink | **MO 137-B** |
| Signal Diodes | **EIA 318-B**<br>**EIA 435**<br>**JESD 531** |
| Signature Analysis | **JEP 136** |
| Silicon Diodes - Reverse Recovery Characteristics | **JESD 41** |
| SIMM | **MODULE 4_4_1**<br>**MODULE 4_4_2**<br>**MODULE 4_4_7** |
| Single | **MO 231-A** |
| Single Semiconductor Device | **JESD 51**<br>**JESD 51- 1** |
| Single-Event Effects - SEE | **JESD 57** |
| Single-Supply | **PR N02-NV2** |
| Singly Right - Censored Data | **JESD 37** |
| Sinusoidal Signal-Generator Method | **EIA 353** |
| SIV | **JEP 139**<br>**JESD 87** |
| Sixteen Byte | **MODULE 4_6** |
| Skew Specification | **JESD 65-A** |
| SLVS | **JESD 8-13** |
| Small | **DO 219-B**<br>**MO 137-B** |
| Small Outline | **MO 230-A** |
| Small Signal - Preferred Values | **JESD 482-A** |
| Small Signal Transistors | **JESD 25** |
| Small Signal VHF-UHF | **EIA 371**<br>**EIA 372** |
| Small Values - Transistor Capacitance | **JESD 6** |
| SO-DIMM | **MODULE 4_4_4**<br>**MODULE 4_5_5**<br>**MODULE 4_5_6**<br>**MODULE 4_5_09**<br>**MODULE 4_20_3**<br>**MODULES 4_5_8**<br>**PR N02-NM4A** |
| SODIMM | **MODULE 4_20_6** |
| Soft Error Rate | **JESD 89** |
| SOIC | **MO 137-B** |
| SOJ | **Design 13** |
| Solar Cells | **EIA 365** |
| Solder Reflow Operations | **JEP 140** |
| Solderability Testing - Dip and Look | **JESD 22-B102-C** |
| Solid State Components - Procurement Quality | **EIA 623** |
| Solid State Products - Registration List | JEP 64 |
| SOP | **MO 187-D**<br>**TO 261-C** |
| SOT | **TO 261-C** |
| Space Vehicle Service | **EIA 365** |
| SPC System | **EIA 557-A** |
| SPD | **SPD 4_1_TOC**<br>**SPD 4_1_2** |



Micron Technology Inc. et al.
Ex. 1017, p. 149

| | |
|---|---|
| | **SPD 4_1_2_2**<br>**SPD 4_1_2_4** |
| Specification | **SDRAM 3_20** |
| Spectral Response Curves | **JEP 78** |
| Square | **MO 228-A**<br>**MO 207-F**<br>**MO 216-D** |
| Square Outlines | **Design 4.5-C** |
| SRAM | **SRAM 3_7**<br>**SRAM 3_7_1**<br>**SRAM 3_7_4**<br>**SRAM 3_07_07**<br>**SRAM 3_07_08**<br>**MODULE 4_4_1**<br>**SRAM 3_07_09**<br>**PR N02-SR1**<br>**PR N02-SR2** |
| SSOP | **MO 153-F**<br>**MO 137-B** |
| SSTL - SSTL_2 | **JESD 8- 9B** |
| SSTL_18 | **JESD 8-15** |
| SSTL_2 | **JESD 82-2**<br>**JESD 82-3A** |
| SSTL_3 | **JESD 8- 8** |
| SSTV | **JESD 82-2** |
| SSTV16857 | **JESD 82-3A** |
| SSTV16859 | **JESD 82-4A** |
| Stacked DDR | **JESD 82-4A** |
| STAPL | **JESD 71** |
| Static Phase Offset | **JESD 65-A** |
| Statistical Process Control - SPC | **EIA 557-A** |
| Statistical Reliability Monitoring - SRM | **JESD 659-A** |
| Storage Life | **JESD 22-A103-B** |
| Stress | **JEP 139** |
| Stress Migration | **JEP 122-A** |
| stress migration/voiding | **JP 001** |
| Stress Test | **JESD 22-A110-B** |
| Stress Test Driven | **JESD 47-A** |
| Stress Test Driven Qualification of ICs | **JESD 39-A** |
| Stress Voiding | **JEP 139** |
| Stress-Induced-Voids | **JESD 87** |
| Stub Series | **JESD 8-15** |
| Stub Series - Terminated Logic | **JESD 8- 8** |
| Stub Series Terminated Logic | **JESD 8- 9B** |
| Style Manual | JM 7 |
| Subassembly | **JESD 22-B110** |
| Superset Memory Types | **SPD 4_1_2_2** |
| Supplementary Design | **MODULES 4_5_12** |
| Supplier management | **EIA 623** |
| Supply Voltage | **JESD 8- 9B**<br>**JESD 8-14** |
| Suppressor - Transient Voltage | **JESD 66** |
| Surface mount | **TO 252-D** |
| Surge Protective Device | **JESD 66** |
| Switching - Inductive | **JESD 24- 5** |



Micron Technology Inc. et al.
Ex. 1017, p. 150

| | |
|---|---|
| Switching Loss | **JESD 24- 1** |
| Switching Method | **EIA 435**<br>**JESD 531** |
| switching parameters | **JESD 82-1** |
| Symbol - Electrostatic Sensitive Devices | **EIA 471** |
| Symbol - Moisture Sensitive | **JEP 113-B** |
| Symbols - Analog-to-Digital | **JESD 99-A** |
| Symbols - Discrete Devices | **JESD 77-B** |
| Symbols - Optoelectronic Devices | **JESD 77-B** |
| Symbols - Quick Reference Guide | **JEP 104-C** |
| Symbols - Quick Reference Guide Data Sheet Disclaimers | JEB 15 |
| Symbols - Voltage Suppressors | **JESD 77-B** |
| Synchronous | **PR N02-NV1** |
| Synchronous RAM | **JESD 79-2** |

**T**

| | |
|---|---|
| T-XBGA | **MO 216-D** |
| Table of Contents | **TOC21C R11** |
| Technology qualification | **JP 001** |
| Temperature | **JESD 22-A108-B** |
| Temperature Coefficient - Resistance | **JESD 33-A** |
| Temperature Coefficient - Voltage Regulator Diodes | **JESD 5** |
| Temperature Cycling | **JEP 122-A**<br>**JESD 22-A104-B** |
| Temperature Measurement | **JEP 140** |
| Template | **MODULE 4_20_1** |
| Tensile Pull | **JESD 22-B109** |
| Terminated Logic | **JESD 8-15** |
| Terminology | **TERM. 2** |
| Terms | **JESD 88** |
| Terms & Definitions - 240 Pin DIMM | **PR N02-NM5** |
| Terms and Definitions - Analog-to-Digital | **JESD 99-A** |
| Terms and Definitions - Binary Integrated Circuit | **JESD 99-A** |
| Terms and Definitions - Cell-Based | **JESD 12-1-B** |
| Terms and Definitions - Digital-to-Analog | **JESD 99-A** |
| Terms and Definitions - Discrete Devices | **JESD 77-B** |
| Terms and Definitions - Gate Arrays | **JESD 12-1-B** |
| Terms and Definitions - Index | **JEP 120-A** |
| Terms and Definitions - Low Frequency Power Transistors | **JESD 10** |
| Terms and Definitions - Memory Integrated Circuits | **JESD 100-B** |
| Terms and Definitions - Microcomputers | **JESD 100-B** |
| Terms and Definitions - Microelectronics | **JESD 99-A** |
| Terms and Definitions - Microprocessors | **JESD 100-B** |
| Terms and Definitions - Optoelectronic Devices | **JESD 77-B** |
| Terms and Definitions - Power MOSFETs | JESD 24 |
| Terms and Definitions - Voltage Suppressors | **JESD 77-B** |
| Terrestrial | **JESD 89** |
| Test Method - Unbiased Autoclave | **JESD 22-A102-C** |
| Test Board | **JESD 51-11** |
| Test Board - Leaded Surface Mount | **JESD 51- 7** |
| Test Boards | **JESD 51- 9** |
| Test Criteria - Thin Dielectrics | **JESD 35-2** |
| Test Method - BGA Ball Shear | **JESD 22-B117** |



Micron Technology Inc. et al.
Ex. 1017, p. 151

| | |
|---|---|
| Test Method - Circuit Support Films | **JEP 112** |
| Test Method - Collector-Base Time Constant | **EIA 284-A** |
| Test Method - Coplanarity | **JESD 22-B108** |
| Test Method - Cycled Temperature Humidity | **JESD 22-A100-B** |
| Test Method - Dose Rate | **JEP 115** |
| Test Method - EEPROM | **JESD 22-A117** |
| Test Method - Electrical | **JESD 51- 1** |
| Test Method - Environmental Conditions | **JESD 51- 2**<br>**JESD 51- 6**<br>**JESD 51- 8** |
| Test Method - ESD Human Body Model | **JESD 22-A114-B** |
| Test Method - ESD Machine Model | **JESD 22-A115-A** |
| Test Method - External Visual | **JESD 22-B101** |
| Test Method - Field-Induced Charged-Device Model | **JESD 22-C101-A** |
| Test Method - Gate Charge | **JESD 24- 2** |
| Test Method - Gate Resistance | **JESD 24-11** |
| Test Method - HAST | **JESD 22-A110-B** |
| Test Method - High Temperature Storage | **JESD 22-A103-B** |
| Test Method - Hot Carrier | **JESD 28-A** |
| Test Method - Humidity Bias Life | **JESD 22-A101-B** |
| Test Method - LCD | **JESD 23** |
| Test Method - Lead Integrity | **JESD 22-B105-B** |
| Test Method - Marking Permanency | **JESD 22-B107-A** |
| Test Method - Mechanical Shock | **JESD 22-B104-B** |
| Test Method - Moisture Diffusivity | **JESD 22-A120** |
| Test method - Particle Getters | **JEP 107** |
| Test Method - Physical Dimension | **JESD 22-B100-A** |
| Test Method - Plastic Surface Mount Preconditioning | **JESD 22-A113-B** |
| Test Method - Polymeric Materials | **JESD 72** |
| Test Method - Power and Temperature Cycling | **JESD 22-A105-B** |
| Test Method - Power Device Turn-Off Switching Loss | **JESD 24- 1** |
| Test Method - Power MOSFET Drain-Source Diodes | **JESD 24-10** |
| Test Method - Repetitive Inductive Load Avalanche Switching | **JESD 24- 8** |
| Test Method - Resistance to Soldering Temperature | **JESD 22-B106-B** |
| Test Method - Salt Atmosphere | **JESD 22-A107-A** |
| Test Method - Short Circuit Withstand Time | **JESD 24- 9** |
| Test Method - Single Pulse UIS Avalanche Test | **JESD 24- 5** |
| Test Method - Subassembly Mechanical Shock | **JESD 22-B110** |
| Test Method - Temperature Cycling | **JESD 22-A104-B** |
| Test Method - Thermal Shock | **JESD 22-A106-A** |
| Test Method - Vibration | **JESD 22-B103-B** |
| Test Method - Water Solubility | **JESD 22-A120** |
| Test Method - Wire Bond Shear | |
| Test Methods - Hermeticity | **JESD 22-A109-A** |
| Test Methods - Photoconductive Cells | **JEP 79** |
| Test Methods - Solderability | **JESD 22-B102-C** |
| Test Methods - Thyristors | **EIA 397** |
| Test Practices | **JESD 282-B** |
| Test Structure - Thin Dielectrics | **JESD 35-1** |
| Testability Guidelines | **JESD 12-5** |
| TF-XBGA | **MO 216-D** |
| TFBGA | **MO 210-F** |



Micron Technology Inc. et al.
Ex. 1017, p. 152

| | |
|---|---|
| Thermal Characteristics - Power MOSFETs | JESD 24 |
| Thermal Conductivity | **JESD 51- 7** |
| Thermal Impedance Measurements - Bipolar Transistors | **JESD 24- 4** |
| Thermal Impedance Measurements - IGBT | **JESD 24- 6** |
| Thermal Impedance Measurements - Vertical Power MOSFETs | **JESD 24- 3** |
| Thermal Measurement - Component Packages | **JESD 51** |
| Thermal Measurement - Integrated Circuit | **JESD 51- 1** |
| Thermal Measurements | **JESD 51- 9**<br>**JESD 51-10** |
| Thermal Resistance | **JESD 531** |
| Thermal Resistance - Bridge Rectifier Assemblies | **JESD 45** |
| Thermal Resistance - GaAs FETs | **JEP 110** |
| Thermal Resistance - Signal and Regulator Diodes | **EIA 435** |
| Thermal Resistance Measurement - Conduction-Cooled Power | **JESD 313-B** |
| Thermal Shock | **JEP 122-A**<br>**JESD 22-A106-A** |
| Thermal Test | **JESD 51- 5**<br>**JESD 51-11** |
| Thermal Test Board | **JESD 51- 3** |
| Thermal Test Chip | **JESD 51- 4** |
| Thermally | **MO 229-B** |
| Thermally enhanced | **MO 220-C**<br>**MO 232-A**<br>**MO 220-E** |
| Thermally Enhanceed | **MO 220-D** |
| Thermally Tabbed Packages | **JESD 51- 5** |
| Thermocouple | **JEP 140** |
| Thin | **MO 208-C**<br>**MO 210G**<br>**CO 029-H** |
| Thin Dielectrics | **JESD 35-A**<br>**JESD 35-1**<br>**JESD 35-2** |
| Thin Gate Oxides | **JESD 35-A** |
| Thin Profile | **MO 216-D** |
| Through-Hole Mounted Devices | **JESD 22-B106-B** |
| Through-Hole Packages | **JESD 51-10**<br>**JESD 51-11** |
| Thyristor Surge Protective Device - TSPD | **JESD 66** |
| Thyristor Test Methods | **EIA 397-1** |
| Thyristors | **EIA 390-A**<br>**JESD 4**<br>**EIA 397** |
| time-dependent dielectric breakdown | **JP 001** |
| Timing Diagrams - B Series CMOS Devices | **JESD 13-B** |
| Timing Failure | **JEP 134** |
| TOC | **MODULE 4_4_TOC** |
| TR-XBGA | **MO 216-D** |
| Transient Voltage Suppressor | **JESD 66** |
| transistor | **TO 220-K** |
| Transistor - AC Stability | **EIA 340** |
| Transistor - Capacitance | **JESD 6** |
| Transistor Admittance Parameters | **EIA 372** |
| Transistor Capacitance | **EIA 398** |



Micron Technology Inc. et al.
Ex. 1017, p. 153

| | |
|---|---|
| Transistor Lead Temperature | **JEP 84** |
| Transistor Short-Circuit | **EIA 371** |
| Transistors | **EIA 354**<br>**JEP 115** |
| Transistors - Conduction Cooled | **JESD 313-B** |
| Transistors - Noise Figure Measurement | **EIA 311-A** |
| Transistors - Field-Effect | **JEP 69-B** |
| Transistors - Insulated Bipolar Gate | **JESD 24- 6** |
| Transistors - Low Power Audio Frequency | **EIA 302** |
| Transistors - Power Gain | **EIA 306** |
| Transistors - Power MOSFETs | JESD 24 |
| Transistors - Small Signal | **EIA 306** |
| Transistors - Thermal Characteristics | **JESD 10** |
| Tray | **Design 4.10D**<br>**CO 034-C** |
| TSOP-Based DRAMs | **PR N02-NM6** |
| TTL | **JESD 12-6**<br>**SRAM 3_7_1**<br>**SRAM 3_07_07** |
| TTL Compatible - BiCMOS Logic Devices | **JESD 54**<br>**JESD 55** |
| TTL Compatible - CMOS Devices | **JESD 52** |
| TTL Compatible - Control Inputs | **JESD 73** |
| TTL Compatible Logic | **JESD 18-A** |
| Turn-Off Switching Loss | **JESD 24- 1** |
| Two Byte | **MODULE 4_3** |
| Type Designation | **EIA 370-B** |
| Type Designations | JEP 64 |
| **U** | |
| UHF | **EIA 306** |
| Unbiased HAST | **JESD 22-A118** |
| Unbuffered | **MODULE 4_5_3**<br>**MODULE 4_5_10**<br>**MODULE 4_20_3**<br>**MODULE 4_5_11**<br>**MODULE 4_20_6** |
| Unbuffered DIMM | **MODULE 4_20_5**<br>**PR N02-NM6** |
| Uncensored Data | **JESD 37** |
| Unclamped Inductive Switching (UIS) | **JESD 24- 5** |
| User Notification | **JESD 46-B** |
| **V** | |
| Values - Device Specifications | **JESD 419-A** |
| Values - Small Signal and Regulator Diodes | **JESD 482-A** |
| Vertical Power MOSFETs | **JESD 24- 3** |
| Very Thin | **MO 220-D**<br>**MO 187-D** |
| Very Very Thin | **MO 217-B**<br>**MO 229-B**<br>**MO 220-E** |
| VFBGA | |
| VHF | **EIA 306** |
| Vibration | **JESD 22-B103-B** |
| Voltage | **EIA 435** |



Micron Technology Inc. et al.
Ex. 1017, p. 154

| | |
|---|---|
| Voltage Regulator Diodes | JESD 5 |
| Voltage-Variable-Capacitance | JESD 381-A |
| **W** | |
| Wafer Level Electrical Testing | JEP 128 |
| wafer level reliability | JP 001 |
| Wafer-Level Testing | JESD 35-A<br>JESD 35-1<br>JESD 35-2 |
| wearout | JP 001 |
| Wide Range | JESD 76-1 |
| Wide Range - Power Supply Voltage | JESD 8- 5<br>JESD 8- 7 |
| Wire Bond Shear | JESD 22-B116 |
| Wire Bond Type Chip | JESD 51- 4 |
| Withstand Time - Short Circuit | JESD 24- 9 |
| Word Wide | EEPROM 3_5_2<br>SRAM 3_07_07<br>SRAM 3_07_08<br>DRAM 3_9_4<br>SDRAM 3_11_4 |
| Word Wide Graphics | MPDRAM 3_10_3 |
| Word Wide PROM | PROM 3_3_3-4 |
| Word Wide ROM | ROM 3_2_2 |
| **X** | |
| XFBGA | MO 221-C |
| **Z** | |
| ZIP | MODULE 4_4_1 |
| **MISCELLANY** | |
| 0.3 V | JESD 8-B |
| 1.2 V | JESD 76-1 |
| 1.5 V | JESD 76-3 |
| 1.5 V Interface | JESD 8-11 |
| 100 Pin | MODULE 4_4_8 |
| 112 pin | MODULE 4_4_6 |
| 144 Pin | MODULE 4_5_5<br>MODULE 4_5_6<br>MODULE 4_5_09<br>MODULE 4_20_3<br>MODULES 4_5_13<br>MODULES 4_5_8<br>MO 214-B |
| 16-Bit Logic | JESD 75-2 |
| 168 Pin | MODULE 4_5_1<br>MODULE 4_5_3<br>MODULES 4_5_13<br>MODULE 4_5_07<br>MODULE 4_20_2 |
| 172 pin | MO 214-B |
| 184 Pin | MODULE 4_5_10<br>MODULE 4_20_5<br>MODULE 4_20_4<br>MODULE 4_5_11<br>MODULES 4_5_12<br>MO 206-C |
| 2.5 V | JESD 8- 9B |
| 200 Pin | MODULE 4_5_2 |



Micron Technology Inc. et al.
Ex. 1017, p. 155

| | |
|---|---|
| 21-C | **TOC21C R11** |
| 278 Pin | **MODULE 4_6_1** |
| 3.3 V | **JESD 8-B** |
| 32-Bit Logic Functions | **JESD 75** |
| 5 V Tolerant - CMOS Devices | **JESD 36** |
| 54 Ball Package | **JESD 75-1** |
| 64 pin | **MODULE 4_4_1** |
| 72 pin | **MODULE 4_4_1**<br>**MODULE 4_4_2**<br>**MODULE 4_4_4** |
| 8-Bit | **JESD 75-3** |
| 80 Pin | **MODULE 4_4_7** |

# Displayed by revision status

**EIA 283** TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A.
November 1963; Rescinded November 1981

**EIA 318-1** ADDENDUM No. 1 to EIA-318 - CHARACTERIZATION OF A REVERSE TEST FIXTURE: SUPERSEDED BY EIA-318-B, July 1996.
February 1981; Rescinded

**EIA 428-A** TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES
October 1988; Rescinded September 1993

**JEB 17** USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS
November 1970; Rescinded April 1987

**JEB 20** ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS
January 1975; Rescinded November 1988

**JEB 6** STANDARD MEASURMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS
December 1966; Rescinded October 1984

**JEB 8** ALPHA NUMERIC GRID SYSTEM FOR DESIGNATING TERMINAL LEAD POSITIONS
June 1968; Rescinded November 1982

**JEP 100** TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.
September 1979; Rescinded October 1983

**JEP 102** STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C.
September 1978; Rescinded April 1985

**JEP 105** JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001
April 1983; Rescinded June 2001

**JEP 107** TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
April 1985; Rescinded June 2001

**JEP 109-C** GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:
March 1995; Rescinded November 2001

**JEP 111** TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.



Micron Technology Inc. et al.
Ex. 1017, p. 156

July 1986; Rescinded June 1996

**JEP 112** TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
June 1987; Rescinded June 2001

**JEP 117** GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.
April 1994; Rescinded July 1994

**JEP 124** GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.
December 1995; Rescinded November 1999

**JEP 74** STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996.
July 1969; Rescinded February 1996

**JEP 75** LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.
August 1984; Rescinded August 1984

**JEP 86-A** RECOMMENDED PRACTICE FOR DUAL DIMENSIONING
May 1976; Rescinded November 1999

**JEP 87** FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A.
June 1992; Rescinded June 1985

**JEP 88** THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS
January 1974; Rescinded June 1992

**JEP 90** THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986.
September 1983; Rescinded September 1986

**JEP 93** MICROELECTRONIC DEVICE TYPE ASSIGNMENTS
August 1975; Rescinded June 1992

**JEP 96** GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES
March 1977; Rescinded April 2000

**JEP 99** GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.
July 1977; Rescinded June 1985

**JESD 17** LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999
August 1988; Rescinded February 1999

**JESD 19** GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A
July 1988; Rescinded July 1995

**JESD 22-A112-A** MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.
November 1995; Rescinded May 2000

**JESD 22-C100-A** HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999
April 1990; Rescinded November 1999

**JESD 26-A** GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001
April 1990; Rescinded July 2001

**JESD 41** REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.



Micron Technology Inc. et al.
Ex. 1017, p. 157

May 1995; Rescinded June 2002

**JESD 45** MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: Rescinded June 2002. Replaced by JESD282-B.
December 1994; Rescinded June 2002

**JESD 53** MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: Rescinded, October 2002
January 1996; Rescinded October 2002

**TENTSTD 11** HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC TYPE PACKAGES: Included in JESD282 and EIA397.
July 1973; Rescinded June 1992

**MO 177-A** REGISTRATION - Rescission of 200 Pin Small Outline Dual-In-Line Memory Module (DIMM) Family, 0.65 mm Pitch. Item 11.14-044.
June 1999; Rescinded June 2001



Micron Technology Inc. et al.
Ex. 1017, p. 158

# Exhibit C

# Contents


| Section | Release # | Page # |
|---|---|---|
| 1 BACKGROUND | Release 1 | Page 1 – 1 |
| 2 TERMS AND DEFINITIONS | Release 1 | Page 2 – 1 |
| 2.1 Conventional Device Pin Names | Release 9r10 | Page 2 – 2 |
| 2.2 Multiport DRAM Pin Names | Release 3 | Page 2 – 5 |
| 2.3 Power Pin Names | Release 9 | Page 2 – 6 |
| 2.4 Device Type Names | Release 9r11 | Page 2 – 7 |
| 2.5 Miscellaneous Device Related Terms | Release 1 | Page 2 – 9 |
| 2.6 Special Operational Cycles for MPDRAM | Release 1 | Page 2 – 10 |
| 2.7 Package–Related Terms | Release 5 | Page 2 – 12 |
| 2.8 Memory Card Pin Names | Release 3 | Page 2 – 13 |
| 2.9 SRAM and SSRAM special Pin Names | Release 6r11 | Page 2–14 |
| 2.10 SLDRAM SPECIAL PIN NAMES | Release 9 | Page 2–15 |
| 3 MEMORY DEVICE STANDARDS | Release 1 | Page 3 – 1 |
| 3.1 General Standards | Release 1 | Page 3 .1 –1 |
| 3.1.1 Bytewide | Release 1 | Page 3 .1 –1 |
| 3.1.1.1 – 32K TO 256K BY 8 A/A MX FAMILY IN DIP | Release 1 | Page 3 .1 –1 |
| FIGURE 3.1-1, 32K TO 256K A/A MULTIPLEXED MEMORY IN DIP | Release 1 | Page 3 .1 -2 |
| 3.2 Read Only Memory (ROM) | Release 1 | Page 3.2–1 |
| 3.2.0 ROM General Standards | Release 5 | Page 3.2–2 |
| 3.2.0.1 – Mask ROM Fast Address Mode Definition | Release 5 | Page 3.2–2 |
| 3.2.1 ROM, Byte Wide | Release 1 | Page 3.2.1–1 |
| 3.2.1.1 – 2K TO 8K BY 8 ROM FAMILY IN DIP, TYPE A | Release 1 | Page 3.2.1–1 |
| 3.2.1.2 – 4K BY 8 ROM IN DIP, Type B | Release 1 | Page 3.2.1–1 |
| 3.2.1.3 – 8K TO 128K BY 8 ROM FAMILY IN DIP, | Release 1 | Page 3.2.1–1 |
| 3.2.1.4 – 2K TO 32K BY 8 ROM FAMILY IN RCC | Release 1 | Page 3.2.1–1 |
| 3.2.1.5 – 32K TO 512K BY 8 ROM FAMILY IN SOJ, | Release 1 | Page 3.2.1–1 |
| 3.2.1.6 – 128K TO 1M BY 8 ROM IN DIP, | Release 1 | Page 3.2.1–1 |
| 3.2.1.7 – 64K TO 512K BY 9 ROM IN DIP, | Release 1 | Page 3.2.1–1 |
| 3.2.1.8 – 2 TO 64 X 16K BY 8 PAGE SELECT ROM IN DIP, | Release 1 | Page 3.2.1–1 |
| 3.2.1.9 – 512K and 1M BY 8 ROM IN QFP, | Release 2 | Page 3.2.1–1 |
| FIGURE 3.2.1-1, 2K TO 8K BY 8 ROM IN DIP, TYPES A & B | Release 1 | Page 3.2.1-2 |
| FIGURE 3.2.1-2, 8K TO 128K BY 8 ROM IN DIP | Release 1 | Page 3.2.1-3 |
| FIGURE 3.2.1-3, 2K TO 32K BY 8 ROM IN CC | Release 1 | Page 3.2.1-4 |
| FIGURE 3.2.1-4, 32K TO 512K BY 8 ROM IN SOJ | Release 1 | Page 3.2.1-5 |
| FIGURE 3.2.1-5, 128K TO 1M BY 8 ROM IN DIP | Release 1 | Page 3.2.1-6 |
| FIGURE 3.2.1-6, 64K TO 512K BY 9 ROM IN DIP | Release 1 | Page 3.2.1-7 |
| FIGURE 3.2.1-7, 2 TO 64 X 16K BY 8 PAGE SELECT | Release 1 | Page 3.2.1-8 |
| FIGURE 3.2.1-8, 512K AND 1M BY 8 ROM IN QFP | Release 2 | Page 3.2.1-9 |
| 3.2.2 ROM, Word Wide | Release 1 | Page 3.2.2–1 |
| 3.2.2.1 – 32K TO 256K BY 16 ROM IN DIP | Release 1 | Page 3.2.2–3 |
| 3.2.2.2 – 32K TO 256K BY 16 ROM IN SCC | Release 1 | Page 3.2.2–3 |
| 3.2.2.3 – 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN DIP | Release 1 | Page 3.2.2–3 |
| 3.2.2.4 – 16K TO 256K BY 16 ADDRESS/DATA MX ROM IN RCC | Release 1 | Page 3.2.2–3 |
| 3.2.2.5 – 256K and 512K BY 16 ROM IN QFP | Release 2 | Page 3.2.2–3 |
| 3.2.2.6 – 512K TO 128M BY 16 ROM IN DIP AND SOP | Release 6 | Page 3.2.2–3 |
| 3.2.2.7 – 512K and 1M BY 16 ROM IN SCC | Release 3 | Page 3.2.2–3 |

| Section | Release # | Page # |
|---|---|---|
| FIGURE 3.2.2-1, 32K TO 256K BY 16 ROM IN DIP | Release 1 | Page 3.2.2-5 |
| FIGURE 3.2.2-2, 32K TO 256K BY 16 ROM IN CC | Release 1 | Page 3.2.2-6 |
| FIGURE 3.2.2-3, 16K TO 256K BY 16 AQ MX ROM IN DIP | Release 1 | Page 3.2.2-7 |
| FIGURE 3.2.2-4, 16K TO 256K BY 16 AQ MX ROM IN CC | Release 1 | Page 3.2.2-8 |
| FIGURE 3.2.2-5, 256K AND 512K BY 16 ROM IN QFP | Release 2 | Page 3.2.2-9 |
| FIGURE 3.2.2-6, 4M TO 128M BY 16 ROM IN DIP AND SOP | Release 2 | Page 3.2.2-10 |
| FIGURE 3.2.2-7, 512K & 1M BY 16 ROM IN SCC | Release 3 | Page 3.2.2-11 |
| FIGURE 3.2.2-8, 512K TO 2M BY 16 ROM IN DIP AND SOG | Release 6 | Page 3.2.2-12 |
| **3.3 Programmable Read Only Memory (PROM)** | **Release 1** | **Page 3.3–1** |
| **3.3.1 PROM, Nibble Wide** | **Release 1** | **Page 3.3.1–1** |
| 3.3.1.1 – .25K & .5K BY 4 TTL PROM IN DIP | Release 1 | Page 3.3.1–3 |
| 3.3.1.2 – .25K BY 4 ECL PROM IN DIP | Release 1 | Page 3.3.1–3 |
| 3.3.1.3 – 1K & 2K BY 4 TTL PROM IN DIP | Release 1 | Page 3.3.1–3 |
| 3.3.1.4 – 1K & 2K BY 4 TTL PROM IN SOP | Release 1 | Page 3.3.1–3 |
| 3.3.1.5 – 4K TO 8K BY 4 TTL PROM IN DIP | Release 2 | Page 3.3.1–3 |
| 3.3.1.6 – .25K TO 2K BY 4 TTL PROM FAMILY IN RCC | Release 1 | Page 3.3.1–3 |
| 3.3.1.7 – 4K BY 4 TTL PROM, 4K BY 4 TTL RPROM IN SCC | Release 1 | Page 3.3.1–3 |
| 3.3.1.8 – 1K TO 8K TTL BY 4 PROM FAMILY IN RCC | Release 1 | Page 3.3.1–3 |
| 3.3.1.9 – 1K TO 8K TTL BY 4 PROM FAMILY IN SCC | Release 1 | Page 3.3.1–3 |
| 3.3.1.10 – 1K TO 4K BY 4 DPROM FAMILIES IN DIP & SCC | Release 1 | Page 3.3.1–4 |
| 3.3.1.11 – 1K TO 16K BY 4 ECL PROM FAMILY IN DIP | Release 1 | Page 3.3.1–4 |
| FIGURE 3.3.1-1, .25K TO 2K BY 4 TTL PROM IN DIP | Release 1 | Page 3.3.1-5 |
| FIGURE 3.3.1-2, 256 BY 4 ECL PROM IN DIP | Release 1 | Page 3.3.1-6 |
| FIGURE 3.3.1-3, 1K & 2K BY 4 TTL PROM IN SOG | Release 1 | Page 3.3.1-7 |
| FIGURE 3.3.1-4, 4K AND 8K BY 4 TTL PROM IN DIP | Release 2 | Page 3.3.1-8 |
| FIGURE 3.3.1-5, .25K TO 4K BY 4 TTL PROM FAMILY IN CC | Release 1 | Page 3.3.1-9 |
| FIGURE 3.3.1-6, 1K TO 8K BY 4 TTL PROM IN RCC | Release 1 | Page 3.3.1-10 |
| FIGURE 3.3.1-7, 1K TO 8K BY 4 TTL PROM IN SCC | Release 1 | Page 3.3.1-11 |
| FIGURE 3.3.1-8, 1K TO 4K BY 4 TTL DPROM IN DIP | Release 1 | Page 3.3.1-12 |
| FIGURE 3.3.1-9, 1K TO 4K BY 4 DPROM IN CC | Release 1 | Page 3.3.1-13 |
| FIGURE 3.3.1-10, 1K TO 16K BY 4 ECL PROM IN DIP | Release 1 | Page 3.3.1-14 |
| **3.3.2 PROM, Bytewide** | **Release 1** | **Page 3.3.2–1** |
| 3.3.2.1 – 32 BY 8 TTL PROM IN DIP & SCC | Release 1 | Page 3.3.2–3 |
| 3.3.2.2 – 32 BY 8 ECL PROM IN DIP & SCC | Release 1 | Page 3.3.2–3 |
| 3.3.2.3 – .25K & .5K BY 8 TTL PROM IN DIP & SCC | Release 1 | Page 3.3.2–3 |
| 3.3.2.4 – .25K TO 8K BY 8 TTL PROM FAMILY IN DIP | Release 1 | Page 3.3.2–3 |
| 3.3.2.5 – .5K TO 4K BY 8 TTL LPROM FAMILY IN DIP | Release 1 | Page 3.3.2–3 |
| 3.3.2.6 – .5K TO 4K BY 8 TTL RPROM FAMILY IN DIP | Release 1 | Page 3.3.2–3 |
| 3.3.2.7 – .5K TO 8K BY 8 TTL PROM FAMILIES IN RCC & SCC | Release 1 | Page 3.3.2–3 |
| 3.3.2.8 – .5K TO 2K BY 8 TTL RPROM FAMILY IN SCC | Release 1 | Page 3.3.2–4 |
| 3.3.2.9 – 16K TO 64K BY 8 TTL PROM FAMILY IN DIP | Release 1 | Page 3.3.2–4 |
| 3.3.2.10 – 512 BY 8 ECL RPROM IN DIP & SCC | Release 2 | Page 3.3.2–4 |
| FIGURE 3.3.2-1, 32 BY 8 TTL & ECL PROM IN DIP | Release 1 | Page 3.3.2-5 |
| FIGURE 3.3.2-2, 32, 256, & 512 BY 8 TTL PROM IN CC, 32 BY 8 ECL PROM IN CC | Release 1 | Page 3.3.2-6 |
| FIGURE 3.3.2-3, 256 & 512 BY 8 TTL PROM IN DIP | Release 1 | Page 3.3.2-7 |
| FIGURE 3.3.2-4, .25K TO 8K BY 8 TTL PROM IN DIP | Release 1 | Page 3.3.2-8 |
| FIGURE 3.3.2-5, .5K TO 4K BY 8 TTL LPROM IN DIP | Release 1 | Page 3.3.2-9 |
| FIGURE 3.3.2-6, .5K TO 4K BY 8 TTL RPROM IN DIP | Release 1 | Page 3.3.2-10 |
| FIGURE 3.3.2-7, .5K TO 8K BY 8 TTL PROM IN SCC | Release 1 | Page 3.3.2-11 |
| FIGURE 3.3.2-8, .5K TO 8K BY 8 TTL PROM IN RCC | Release 1 | Page 3.3.2-12 |
| FIGURE 3.3.2-9, .5K TO 2K BY 8 RPROM IN CC | Release 1 | Page 3.3.2-13 |




Micron Technology Inc. et al.
Ex. 1017, p. 161

| Section | Release # | Page # |
|---|---|---|
| FIGURE 3.3.2-10, 16K TO 64K BY 8 TTL PROM IN DIP | Release 1 | Page 3.3.2-14 |
| FIGURE 3.3.2-11, 512 BY 8 10K & 100K ECL RPROM IN DIP AND SCC | Release 2 | Page 3.3.2-15 |
| **3.3.3 PROM, Word Wide** | **Release 1** | **Page 3.3.3–1** |
| 3.3.3.1 – 32 AND 64 BY 16 PROM IN DIP AND SCC | Release 1 | Page 3.3.3–3 |
| FIGURE 3.3.3-1, 32 AND 64 BY 16 TTL PROM IN DIP | Release 1 | Page 3.3.3-5 |
| FIGURE 3.3.3-2, 32 AND 64 BY 16 TTL PROM IN CC | Release 1 | Page 3.3.3-6 |
| **3.3.4 PROM Package Conversion** | **Release 1** | **Page 3.3.4–1** |
| 3.3.4.1 – PROM DIP TO SO CONVERSION, 16, 18, 20, 24 DIP | Release 1 | Page 3.3.4–1 |
| FIGURE 3.3.4-1, 1K AND 2K TTL PROM 18 DIP TO 20 SO CONVERSION | Release 1 | Page 3.3.4-3 |
| **3.4 Erasable Programmable Read Only Memory (EPROM)** | **Release 1** | **Page 3.4–1** |
| **3.4.1 EPROM, Byte Wide** | **Release 1** | **Page 3.4.1–1** |
| 3.4.1.1 – 4K BY 8 EPROM IN DIP, TYPE A | Release 1 | Page 3.4.1–3 |
| 3.4.1.2 – 4K AND 8K BY 8 EPROM IN DIP, | Release 1 | Page 3.4.1–3 |
| 3.4.1.3 – 8K TO 64K BY 8 EPROM FAMILY IN DIP, | Release 1 | Page 3.4.1–3 |
| 3.4.1.4 – 2K TO 512K BY 8 EPROM FAMILY IN RCC | Release 1 | Page 3.4.1–3 |
| 3.4.1.5 – 32K TO 512K BY 8 EPROM FAMILY IN SOJ, | Release 1 | Page 3.4.1–3 |
| 3.4.1.6 – 128K TO 1M BY 8 EPROM FAMILY IN DIP, | Release 1 | Page 3.4.1–3 |
| 3.4.1.7 – 64K TO 512K BY 9 EPROM FAMILY IN DIP, | Release 1 | Page 3.4.1–3 |
| 3.4.1.8 – 2 TO 64 X 16K BY 8 PAGE SELECT EPROM FAMILY IN DIP, | Release 1 | Page 3.4.1–3 |
| 3.4.1.9 – 128K TO 512K BY 8 EPROM FAMILY IN TSOP–1, | Release 4 | Page 3.4.1–3 |
| FIGURE 3.4.1-1, 4K AND 8K BY 8 EPROM IN DIP, TYPES A & B | Release 1 | Page 3.4.1-5 |
| FIGURE 3.4.1-2, 8K TO 64K BY 8 EPROM IN DIP | Release 1 | Page 3.4.1-6 |
| FIGURE 3.4.1-3, 2K TO 512K BY 8 EPROM IN CC | Release 1 | Page 3.4.1-7 |
| FIGURE 3.4.1-4, 32K TO 512K BY 8 EPROM IN SOJ | Release 1 | Page 3.4.1-8 |
| FIGURE 3.4.1-5, 128K TO 1M BY 8 EPROM IN DIP | Release 1 | Page 3.4.1-9 |
| FIGURE 3.4.1-6, 64K TO 512K BY 9 EPROM IN DIP | Release 1 | Page 3.4.1-10 |
| FIGURE 3.4.1-7, 2 TO 64 X 16K BY 8 PAGE SELECT EPROM IN DIP | Release 1 | Page 3.4.1-11 |
| FIGURE 3.4.1-8, 128K TO 512K BY 8 EPROM IN TSOP-1 | Release 4 | Page 3.4.1-12 |
| **3.4.2 EPROM, Word Wide** | **Release 1** | **Page 3.4.2–1** |
| 3.4.2.1 – 32K TO 256K BY 16 EPROM IN DIP | Release 1 | Page 3.4.2–3 |
| 3.4.2.2 – 32K TO 256K BY 16 EPROM IN SCC | Release 1 | Page 3.4.2–3 |
| 3.4.2.3 – 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP | Release 1 | Page 3.4.2–3 |
| 3.4.2.4 – 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC | Release 1 | Page 3.4.2–3 |
| 3.4.2.5 – 512K TO 128M BY 16 EPROM or OTP IN DIP AND SOP | Release 6 | Page 3.4.2–3 |
| 3.4.2.6 – 512K and 1M BY 16 EPROM IN SCC | Release 3 | Page 3.4.2–3 |
| 3.4.2.7 – 64K TO 256K BY 16 EPROM IN TSOP–1 | Release 4 | Page 3.4.2–3 |
| FIGURE 3.4.2-1, 32K TO 256K BY 16 EPROM IN DIP | Release 1 | Page 3.4.2-5 |
| FIGURE 3.4.2-2, 32K TO 256K BY 16 EPROM IN SCC | Release 1 | Page 3.4.2-6 |
| FIGURE 3.4.2-3, 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN DIP | Release 1 | Page 3.4.2-7 |
| FIGURE 3.4.2-4, 16K TO 256K BY 16 ADDRESS/DATA MX EPROM IN RCC | Release 1 | Page 3.4.2-8 |
| FIGURE 3.4.2-5, 4M TO 128M BY 16 EPROM OR OTP IN DIP AND SOP | Release 1 | Page 3.4.2-9 |
| FIGURE 3.4.2-6, 512K & 1M BY 16 EPROM IN CC | Release 3 | Page 3.4.2-10 |
| FIGURE 3.4.2-7, 64K BY 256K BY 16 EPROM IN TSOP-1 | Release 4 | Page 3.4.2-11 |
| FIGURE 3.4.2-8, 512K TO 2M BY 16 EPROM IN DIP AND SOG | Release 6 | Page 3.4.2-12 |
| **3.5 Electrically Erasable Programmable Read Only Memory (EEPROM)** | **Release 1** | **Page 3.5–1** |
| **3.5.1 EEPROM, Byte Wide** | **Release 1** | **Page 3.5.1–1** |
| 3.5.1.1 – .5K TO 2K BY 8 EEPROM FAMILY IN DIP | Release 1 | Page 3.5.1–2 |
| 3.5.1.2 – 2K & 4K BY 8 EEPROM IN RCC | Release 1 | Page 3.5.1–2 |
| 3.5.1.3 – 1K TO 32K BY 8 EEPROM FAMILY IN DIP | Release 1 | Page 3.5.1–2 |
| 3.5.1.4 – .5K TO 32K BY 8 EEPROM FAMILY IN RCC | Release 1 | Page 3.5.1–2 |




Micron Technology Inc. et al.
Ex. 1017, p. 162

| Section | Release # | Page # |
|---|---|---|
| 3.5.1.5 – 32K TO 256K BY 8 EEPROM FAMILY IN SOJ, | Release 1 | Page 3.5.1–2 |
| 3.5.1.6 – 32K TO 512K BY 8 EEPROM FAMILY IN DIP, | Release 1 | Page 3.5.1–2 |
| 3.5.1.7 – 32K TO 256K BY 8 EEPROM FAMILY IN RCC, | Release 1 | Page 3.5.1–2 |
| 3.5.1.8 – 32K TO 256K BY 9 EEPROM FAMILY IN DIP, | Release 1 | Page 3.5.1–2 |
| 3.5.1.9 – 128K TO 1M BY 8 EEPROM FAMILY IN SCC, | Release 1 | Page 3.5.1–2 |
| 3.5.1.10 – 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1 | Release 2 | Page 3.5.1–3 |
| 3.5.1.11 – EXTENDED FEATURE SET FOR 256K BIT EEPROM | Release 2 | Page 3.5.1–3 |
| 3.5.1.12 – OPTIONAL COMMAND SET FOR DUAL–SUPPLY EEPROM | Release 3 | Page 3.5.1–3 |
| 3.5.1.13 – 512K BY 8 DUAL–SUPPLY EEPROM IN RCC | Release 5 | Page 3.5.1–3 |
| 3.5.1.14 – 128K to 512K BY 8 SINGLE–SUPPLY EEPROM FAMILY IN DIP, RCC, & TSOP1 | Release 5 | Page 3.5.1–3 |
| 3.5.1.15 – 256K, 512K, &1M BY 8 DUAL–SUPPLY EEPROM IN TSOP1 | Release 6 | Page 3.5.1–4 |
| 3.5.1.16 – 1M TO 8M BY 8 SINGLE-SUPPLY EEPROM FAMILY IN TSOP1 | Release 5 | Page 3.5.1–4 |
| 3.5.1.17 – 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP2 | Release 6 | Page 3.5.1–4 |
| 3.5.1.18 – 1M, 2M BU 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP2 | Release 7 | Page 3.5.1–4 |
| 3.5.1.19 – 4Mb TO 32Mb DENSITY BY 8 Dual Supply Flash EEPROM in 8 X 5 GRID Micro BGA Package | Release 9 | Page 3.5.1–4 |
| 3.5.1.20 – 2K BIT SERIAL, SINGLE SUPPLY EEPROM IN 8 PIN SOG | Release 9 | Page 3.5.1–4 |
| FIGURE 3.5.1-1, .5K TO 2K BY 8 EEPROM IN DIP | Release 1 | Page 3.5.1-5 |
| FIGURE 3.5.1-2, 2K & 4K BY 8 EEPROM IN RCC | Release 1 | Page 3.5.1-6 |
| FIGURE 3.5.1-3, 1K TO 32K BY 8 EEPROM FAMILY IN DIP | Release 1 | Page 3.5.1-7 |
| FIGURE 3.5.1-4, .5K TO 32K BY 8 EEPROM FAMILY IN RCC | Release 1 | Page 3.5.1-8 |
| FIGURE 3.5.1-5, 32K TO 256K BY 8 EEPROM FAMILY IN SOJ | Release 1 | Page 3.5.1-9 |
| FIGURE 3.5.1-6, 32K TO 512K BY 8 EEPROM FAMILY IN DIP | Release 1 | Page 3.5.1-10 |
| FIGURE 3.5.1-7, 32K TO 256K BY 8 EEPROM FAMILY IN RCC | Release 1 | Page 3.5.1-11 |
| FIGURE 3.5.1-8, 32K TO 256K BY 9 EEPROM FAMILY IN DIP | Release 1 | Page 3.5.1-12 |
| FIGURE 3.5.1-9, 128K TO 1M BY 8 EEPROM FAMILY IN SCC | Release 1 | Page 3.5.1-13 |
| FIGURE 3.5.1-10, 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1 | Release 2 | Page 3.5.1-14 |
| ADDENDUM 1, 32K X 8 BIT EEPROM EXTENDED FEATURE STANDARD | Release 2 | Page 3.5.1-15 |
| FIGURE 3.5.1-11, DUAL SUPPLY EEPROM COMMAND SET | Release 3 | Page 3.5.1-23 |
| FIGURE 3.5.1-12, 512K BY 8 DUAL-SUPPLY EEPROM IN RCC | Release 5 | Page 3.5.1-24 |
| FIGURE 3.5.1-13, 128K to 512K SINGLE-SUPPLY EEPROM FAMILY IN DIP | Release 5 | Page 3.5.1-25 |
| FIGURE 3.5.1-14, 128K to 512K SINGLE-SUPPLY EEPROM FAMILY IN RCC | Release 5 | Page 3.5.1-26 |
| FIGURE 3.5.1-15, 128K to 512K SINGLE-SUPPLY EEPROM FAMILY IN TSOP1 | Release 5 | Page 3.5.1-27 |
| FIGURE 3.5.1-16, 1M BY 8 DUAL-SUPPLY EEPROM IN TSOP1 | Release 5 | Page 3.5.1-28 |
| FIGURE 3.5.1-17. 1M TO 8M SINGLE-SUPPLY EEPROM FAMILY IN TSOP1 | Release 5 | Page 3.5.1-29 |
| FIGURE 3.5.1-18, 256K & 512K BY 8 DUAL-SUPPLY EEPROM IN TSOP1 | Release 6 | Page 3.5.1-30 |
| FIGURE 3.5.1-19 A⇒C 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP2 | Release 6 | Page 3.5.1-31⇒33 |
| FIGURE 3.5.1-20. 1M, 2M BU 8 SINGLE OR DUAL SUPPLY EEPROM IN PSOP1 | Release 7 | Page 3.5.1-34 |
| FIGURE 3.5.1-512K TO 4096K X 8 Dual Supply Flash EEPROM IN 8 X 5 GRID Micro BGA Package | Release 9 | Page 3.5.1-35 |
| FIGURE 3.5.1-22 2K BIT SERIAL, SINGLE SUPPLY EEPROM IN 8 PIN SOG | Release 9 | Page 3.5.1-36 |
| **3.5.2 EEPROM, Word Wide** | **Release 1** | **Page 3.5.2–1** |
| 3.5.2.1 – 4K TO 32K BY 16 EEPROM IN DIP | Release 1 | Page 3.5.2–2 |
| 3.5.2.2 – 4K TO 256K BY 16 EEPROM IN SCC | Release 1 | Page 3.5.2–2 |
| 3.5.2.3 – 256K TO 128M BY 16 EEPROM IN DIP AND SOG | Release 6 | Page 3.5.2–2 |
| 3.5.2.4 – 1M TO 4M BY 16 DS EEPROM IN SSOP | Release 6 | Page 3.5.2–2 |
| 3.5.2.5 – 1M TO 4M DENSITY, BY 8 OR 16 FEEPROM IN PSOP | Release 7 | Page 3.5.2–2 |
| 3.5.2.6 – 1M TO 32M DENSITY, BY 8 OR 16 FEEPROM IN TSOP1 | Release 7 | Page 3.5.2–2 |
| 3.5.2.7 – 4Mb TO 32Mb DENSITY BY 8 & 16 Dual Supply Flash EEPROM in 8 X 6 GRID Micro BGA Package | Release 9 | Page 3.5.2–2 |
| 3.5.2.8 – 16Mb TO 64Mb DENSITY BY 8 & 16, Dual supply Flash EEPROM in 8 X 9 GRID Micro BGA Package | Release 9 | Page 3.5.2–3 |


**Release 11a**



Micron Technology Inc. et al.
Ex. 1017, p. 163

| Section | Release # | Page # |
|---|---|---|
| 3.5.2.9 – 8Mb TO 128Mb Density FEEPROM/SRAM in BGA | Release 10 | Page 3.5.2–3 |
| 3.5.2.10 – 4M TO 64M BY 16 FEEPROM IN TSOP1 | Release 11 | Page 3.5.2–3 |
| 3.5.2.11 – 2M TO 64M BY 16 FEEPROM IN FBGA | Release 11 | Page 3.5.2–3 |
| 3.5.2.12 – 4M, 8M, & 16M BY 16 FEEPROM with SDRAM Interface | Release 11 | Page 3.5.2–3 |
| 3.5.2.13 – 128Mb TO 4Gb Density FEEPROM, User Selectable as X8 OR X16 in SSOP | Release 11 | Page 3.5.2–4 |
| FIGURE 3.5.2-1, 4K TO 32K BY 16 EEPROM FAMILY IN DIP | Release 1 | Page 3.5.2-5 |
| FIGURE 3.5.2-2, 4K TO 256K BY 16 EEPROM FAMILY IN SCC | Release 1 | Page 3.5.2-6 |
| FIGURE 3.5.2-3, 4M TO 128M BY 16 EEPROM FAMILY IN DIP AND SOG | Release 2 | Page 3.5.2-7 |
| FIGURE 3.5.2-4, 256K TO 2M BY 16 EEPROM FAMILY IN DIP AND SOG | Release 6 | Page 3.5.2-8 |
| FIGURE 3.5.2-5, 1M TO 4M BY 16 DS EEPROM IN SSOP | Release 6 | Page 3.5.2-9 |
| FIGURE 3.5.2-6, 1M TO 4M DENSITY BY 8 OR16 FEEPROM IN PSOP | Release 7 | Page 3.5.2-10 |
| FIGURE 3.5.2-7, 1M TO 32M DEBSITY BY 8 OR16 FEEPROM IN PSOP | Release 7 | Page 3.5.2-11 |
| FIGURE 3.5.2-8, 512K TO 2048K X 8, 256K TO 2048K X 16, Dual Supply Flash EEPROM IN 8 X 6 GRID Micro BGA Package | Release 9 | Page 3.5.2-12 |
| FIGURE 3.5.2-9, 2048K & 8192K X 8, 1024K & 4096K X 16, Dual supply Flash EEPROM IN 8 X 9 GRID Micro BGA Package | Release 9 | Page 3.5.2-13 |
| FIGURE 3.5.2-10, FEEPROM/SRAM Mixed Technology, Multi Chip Device | Release 10r11 | Page 3.5.2-14⇒20 |
| FIGURE 3.5.2-11, 4M TO 64M BY 16 FEEPROM IN TSOP1 | Release 11 | Page 3.5.2-21 |
| FIGURE 3.5.2-12, 32Mb TO 1Gb Density BY 16 FEEPROM IN BGA | Release 11 | Page 3.5.2-22 |
| FIGURE 3.5.2-13, 4MTO 16M BY 16 FEEPROM With SDRAM Interface In TSOP2 | Release 11 | Page 3.5.2-23 |
| FIGURE 3.5.2-14, 4M TO 16M BY 16 FEEPROM With SDRAM Interface in FGBA | Release 11 | Page 3.5.2-24 |
| FIGURE 3.5.2-15, 128Mb TO 4Gb FEEPROM, user selectable as X8 or X16 in SSOP | Release 11 | Page 3.5.2-25 |
| **3.5.3 EEPROM EXTENDED FEATURES** | **Release 1** | **Page 3.5.3–1** |
| 3.5.3.1 – EXTENDED FEATURE SET FOR 256Kb EEPROM | Release 1 | Page 3.5.3–3 |
| 3.5.3.2 – DUAL SUPPLY EEPROM COMMAND SET | Release 7 | Page 3.5.3–13 |
| 3.5.3.3 – SINGLE SUPPLY EEPROM COMMAND CODES | Release 7 | Page 3.5.3–14 |
| 3.5.3.4 – EEPROM TOGGLE BIT FEATURE | Release 7 | Page 3.5.3–15 |
| **3.6 Non volatile Random Access Memory (NVRAM)** | **Release 1** | **Page 3.6–1** |
| **3.6.1 NVRAM, Nibble Wide** | **Release 1** | **Page 3.6–3** |
| 3.6.1.1 – .25K & 1K BY 4 NVRAM IN DIP | Release 1 | Page 3.6–3 |
| **3.6.2 NVRAM, BYTE WIDE** | **Release 1** | **Page 3.6–3** |
| 3.6.2.1 – .5K, 1K BY 8 NVRAM IN DIP | Release 1 | Page 3.6–3 |
| 3.6.2.2 – .5K & 1K BY 8 NVRAM IN RCC | Release 1 | Page 3.6–3 |
| 3.6.2.3 – .5K TO 16K BY 8 NVRAM FAMILY IN DIP | Release 1 | Page 3.6–3 |
| 3.6.2.4 – .5K TO 16K BY 8 NVRAM FAMILY IN RCC | Release 1 | Page 3.6–3 |
| 3.6.2.5 – 32K TO 256K BY 8 NVRAM FAMILY IN SOJ, | Release 1 | Page 3.6–3 |
| 3.6.2.6 – 32K TO 256K BY 8 NVRAM FAMILY IN DIP, | Release 1 | Page 3.6–3 |
| 3.6.2.7 – 16K TO 128K BY 9 NVRAM FAMILY IN DIP, | Release 1 | Page 3.6–3 |
| FIGURE 3.6-1, .25K & 1K BY 4 NVRAM IN DIP | Release 1 | Page 3.6-5 |
| FIGURE 3.6-2, .5K & 1K BY 8 NVRAM IN DIP | Release 1 | Page 3.6-6 |
| FIGURE 3.6-3, .5K & 1K BY 8 NVRAM IN RCC | Release 1 | Page 3.6-7 |
| FIGURE 3.6-4, .5K TO 16K BY 8 NVRAM FAMILY IN DIP | Release 1 | Page 3.6-8 |
| FIGURE 3.6-5, .5K TO 16K BY 8 NVRAM FAMILY IN RCC | Release 1 | Page 3.6-9 |
| FIGURE 3.6-6, 32K TO 256K BY 8 NVRAM FAMILY IN SOJ | Release 1 | Page 3.6-10 |
| FIGURE 3.6-7, 32K TO 256K NY 8 NVRAM FAMILY IN DIP | Release 1 | Page 3.6-11 |
| FIGURE 3.6-8, 16K TO 128K BY 9 NVRAM FAMILY IN DIP | Release 1 | Page 3.6-12 |
| **3.7 Static Random Access Memory (SRAM)** | **Release 1** | **Page 3.7–1** |
| **3.7.1 – JTAG Extension to Revolutionary Pinout SRAM Devices** | **Release 4** | **Page 3.7–1** |
| FIGURE 3.7-1, JTAG ADDITION TO REVOLUTIONARY PINOUT SRAM | Release 4 | Page 3.7-3 |
| FIGURE 3.7-2, State Diagram for Pipelined-Burst SRAM | Release 7 | Page 3.7-4 |
| **3.7.1 Bit Wide TTL SRAM** | **Release 1** | **Page 3.7.1–1** |


**Release 11a**



Micron Technology Inc. et al.
Ex. 1017, p. 164

| Section | Release # | Page # |
|---|---|---|
| 3.7.1.1 – .25K & 1K BY 1 TTL SRAM IN DIP | Release 1 | Page 3.7.1–3 |
| 3.7.1.2 – .25K & 1K BY 1 TTL SRAM IN SCC | Release 1 | Page 3.7.1–3 |
| 3.7.1.3 – 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP | Release 1 | Page 3.7.1–3 |
| 3.7.1.4 – 16K BY 1 TTL SRAM IN RCC | Release 1 | Page 3.7.1–3 |
| 3.7.1.5 – 64K BY 1 TTL SRAM IN RCC | Release 1 | Page 3.7.1–3 |
| 3.7.1.6 – 16K TO 2M BY 1 TTL SRAM IN SOJ | Release 5 | Page 3.7.1–3 |
| 3.7.1.7 – 256K TO 16M BY 1 TTL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.1–3 |
| 3.7.1.8 – 256K BY 1 TTL SRAM IN RCC | Release 1 | Page 3.7.1–3 |
| 3.7.1.9 – 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.1–3 |
| FIGURE 3.7.1-1, 0.25K & 1K BY 1 TTL SRAM IN DIP | Release 1 | Page 3.7.1-5 |
| FIGURE 3.7.1-2, 0.25K & 1K BY 1 TTL SRAM IN SCC | Release 1 | Page 3.7.1-6 |
| FIGURE 3.7.1-3, 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP | Release 1 | Page 3.7.1-7 |
| FIGURE 3.7.1-4, 16K BY 1 TTL SRAM IN RCC | Release 1 | Page 3.7.1-8 |
| FIGURE 3.7.1-5, 64K BY 1 TTL SRAM IN RCC | Release 1 | Page 3.7.1-9 |
| FIGURE 3.7.1-6, 16K TO 2M BY 1 TTL SRAM IN SOJ AND TSOP-2 | Release 5 | Page 3.7.1-10 |
| FIGURE 3.7.1-7, 256K TO 16M BY 1 TTL SRAM AND SSRAM FAMILY IN DIP, TSOP2, AND SOJ | Release 4 | Page 3.7.1-11 |
| FIGURE 3.7.1-8, 256K BY 1 TTL SRAM IN RCC | Release 1 | Page 3.7.1-12 |
| FIGURE 3.7.1-9, 4M AND 16M CONFIGURABLE SRAM IN DIP, TSOP2, AND SOJ | Release 4 | Page 3.7.1-13 |
| **3.7.2 Bit Wide ECL SRAM** | **Release 1** | **Page 3.7.2–1** |
| 3.7.2.1 – 1K TO 256K BY 1 ECL SRAM FAMILY IN DIP | Release 1 | Page 3.7.2–3 |
| 3.7.2.2 – 256K TO 16M BY 1 ECL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.2–3 |
| 3.7.2.3 – 64K AND 256K BY 1 ECL SRAM IN FLATPACK | Release 2 | Page 3.7.2–3 |
| 3.7.2.4 – 256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.2–3 |
| FIGURE 3.7.2-1, 1K TO 256K BY 1 ECL SRAM FAMILY IN DIP | Release 1 | Page 3.7.2-5 |
| FIGURE 3.7.2-2, 256K TO 16M BY 1 ECL SRAM AND SSRAM FAMILY IN DIP, TSOP2, & SOJ | Release 4 | Page 3.7.2-6 |
| FIGURE 3.7.2-3, 64K AND 256K BY 1 ECL SRAM IN FP | Release 2 | Page 3.7.2-7 |
| FIGURE 3.7.2-4, 256K TO 16M BY 1 ECL SSRAM FAMILY IN DIP, TSOP2, & SOJ | Release 4 | Page 3.7.2-8 |
| **3.7.3 Nibble Wide TTL SRAM** | **Release 1** | **Page 3.7.3–1** |
| 3.7.3.1 – 16 BY 4, INVERTING AND NON INVERTING TTL SRAM IN DIP & SCC | Release 1 | Page 3.7.3–3 |
| 3.7.3.2 – .25K BY 4 TTL SRAM IN DIP & RCC | Release 1 | Page 3.7.3–3 |
| 3.7.3.3 – 256 BY 4 TTL SRAM WITH G IN SCC | Release 1 | Page 3.7.3–3 |
| 3.7.3.4 – 4K TO 64K BY 4 TTL SRAM WITHOUT G FAMILY IN DIP | Release 1 | Page 3.7.3–3 |
| 3.7.3.5 – 4K BY 4 TTL SRAM IN RCC | Release 1 | Page 3.7.3–3 |
| 3.7.3.6 – 4K TO 1M BY 4 TTL SRAM WITH G FAMILY IN DIP | Release 1 | Page 3.7.3–3 |
| 3.7.3.7 – 16K TO 256K BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN RCC | Release 1 | Page 3.7.3–3 |
| 3.7.3.8 – 16K & 64K BY 4 TTL SRAM IN RCC | Release 1 | Page 3.7.3–3 |
| 3.7.3.9 – 4K TO 1M BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN SOJ AND TSOP–2 | Release 5 | Page 3.7.3–4 |
| 3.7.3.10 – 64K TO 4M BY 4 TTL SRAM IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.3–4 |
| 3.7.3.11 – 64K TO 4M BY 4 TTL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.3–4 |
| 3.7.3.12 – 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.3–4 |
| 3.7.3.13 – 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ | Release 1 | Page 3.7.3–4 |
| 3.7.3.14 – 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP AND SOJ | Release 1 | Page 3.7.3–4 |




Micron Technology Inc. et al.
Ex. 1017, p. 165

| Section | Release # | Page # |
|---|---|---|
| FIGURE 3.7.3–1, 16 BY 4 INVERTING AND NON–INVERTING TTL SRAM IN DIP | Release 1 | Page 3.7.3–5 |
| FIGURE 3.7.3–2, 16 BY 4 INVERTING AND NON–INVERTING TTL SRAM IN SCC | Release 1 | Page 3.7.3–6 |
| FIGURE 3.7.3–3, 256 BY 4 TTL SRAM IN DIP | Release 1 | Page 3.7.3–7 |
| FIGURE 3.7.3–4, 256 BY 4 TTL SRAM IN RCC | Release 1 | Page 3.7.3–8 |
| FIGURE 3.7.3–5, 256 BY 4 TTL SRAM IN SCC | Release 1 | Page 3.7.3–9 |
| FIGURE 3.7.3–6, 4K TO 64K BY 4 TTL SRAM FAMILY WITHOUT G IN DIP | Release 1 | Page 3.7.3–10 |
| FIGURE 3.7.3–7, 4K BY 4 TTL SRAM IN RCC | Release 1 | Page 3.7.3–11 |
| FIGURE 3.7.3–8, 4K TO 256K BY 4 TTL SRAM FAMILY WITH G IN DIP | Release 1 | Page 3.7.3–12 |
| FIGURE 3.7.3–9, 16K TO 256K BY 4 TTL SRAM FAMILY IN RCC | Release 1 | Page 3.7.3–13 |
| FIGURE 3.7.3–10, 16K & 64K BY 4 TTL SRAM IN RCC | Release 1 | Page 3.7.3–14 |
| FIGURE 3.7.3–11, 4K TO 1M BY 4 TTL SRAM WITH AND W/O G IN SOJ AND TSOP–2 | Release 1 | Page 3.7.3–15 |
| FIGURE 3.7.3–12, 64K TO 4M BY 4 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ | Release 4 | Page 3.7.3–16 |
| FIGURE 3.7.3–13, 64K TO 4M BY 4 TTL SRAM FAMILY WITH SEPARATE DATA I/O IN DIP, TSOP2, AND SOJ | Release 4 | Page 3.7.3–17 |
| FIGURE 3.7.3–14, 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) FAMILY IN DIP,SOJ,AND TSOP–2 | Release 4 | Page 3.7.3–18 |
| FIGURE 3.7.3–15, 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ | Release 1 | Page 3.7.3–19 |
| **3.7.4 Nibble Wide ECL SRAM** | **Release 1** | **Page 3.7.4–1** |
| 3.7.4.1 – .25K AND 1K BY 4, 100K ECL SRAM IN DIP AND SFP | Release 1 | Page 3.7.4–3 |
| 3.7.4.2 – 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP | Release 1 | Page 3.7.4–3 |
| 3.7.4.3 – .25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP | Release 1 | Page 3.7.4–3 |
| 3.7.4.4 – 16K BY 4,10K & 100K ECL SSRAM IN DIP | Release 1 | Page 3.7.4–3 |
| 3.7.4.5 – 64K TO 4M BY 4 ECL SRAM IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–3 |
| 3.7.4.6 – 64K TO 4M BY 4 ECL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–3 |
| , 3.7.4.7 – 64K TO 4M BY 4 ECL SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–4 |
| 3.7.4.8 – 64K BY 4 ECL SRAM IN FP | Release 2 | Page 3.7.4–4 |
| 3.7.4.9 – 256K BY 4/512K BY 2 RECONFIGURABLE SRAM IN DIP & SOJ | Release 2 | Page 3.7.4–4 |
| 3.7.4.10 – 64K TO 4M BY 4 SRAM FAMILY IN DIP AND SOJ IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–4 |
| 3.7.4.11 – 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–4 |
| 3.7.4.12 – 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–4 |
| FIGURE 3.7.4–1, 256 BY 4, 100K ECL SRAM IN DIP, 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP | Release 1 | Page 3.7.4–5 |
| FIGURE 3.7.4–2, 256 & 1K BY 4, 100K ECL SRAM IN SFP | Release 1 | Page 3.7.4–6 |
| FIGURE 3.7.4–4, 0.25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP | Release 1 | Page 3.7.4–7 |
| FIGURE 3.7.4–5, 16K BY 4, 10K & 100K ECL SSRAM IN DIP | Release 1 | Page 3.7.4–8 |
| FIGURE 3.7.4–6, 64K TO 4M BY 4 ECL SRAM FAMILY IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–9 |
| FIGURE 3.7.4–7, 64K TO 4M BY 4 ECL SRAM WITH SEPARATE I/O FAMILY IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–10 |
| FIGURE 3.7.4–8, 64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–11 |
| FIGURE 3.7.4–9, 64K BY 4 ECL SRAM IN FP | Release 2 | Page 3.7.4–12 |
| FIGURE 3.7.4–10, 256K BY 4 or 512K BY 2 CONFIGURABLE ECL SRAM IN DIP AND SOJ | Release 2 | Page 3.7.4–13 |
| FIGURE 3.7.4–11, 64K TO 4M BY 4 BIT SELECTABLE ECL SRAM FAMILY IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–14 |
| FIGURE 3.7.4–12, 64K TO 4M BY 4 ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–15 |
| FIGURE 3.7.4–13, 64K TO 4M BY 4 BIT SELECTABLE ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.4–16 |
| **3.7.5 Byte Wide TTL SRAM** | **Release 1** | **Page 3.7.5–1** |
| 3.7.5.1 – 64 BY 9 TTL SRAM IN SCC | Release 1 | Page 3.7.5–3 |


**Release 11a**



Micron Technology Inc. et al.
Ex. 1017, p. 166

| Section | Release # | Page # |
|---|---|---|
| 3.7.5.2 – 1K & 2K BY 8 TTL SRAM IN DIP | Release 1 | Page 3.7.5–3 |
| 3.7.5.3 – 2K & 4K BY 8 TTL SRAM IN RCC | Release 1 | Page 3.7.5–3 |
| 3.7.5.4 – 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ, | Release 1 | Page 3.7.5–3 |
| 3.7.5.5 – .5K TO 32K BY 8 TTL SRAM FAMILY IN RCC | Release 1 | Page 3.7.5–3 |
| 3.7.5.6 – 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ or TSOP–2, | Release 4 | Page 3.7.5–3 |
| 3.7.5.7 – 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP, | Release 1 | Page 3.7.5–3 |
| 3.7.5.8 – 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP, | Release 1 | Page 3.7.5–3 |
| 3.7.5.9 – 32K TO 2M BY 8 AND 512K TO 2M BY 9 TTL SRAM IN DIP, SOJ, AND TSOP–2 | Release 4 | Page 3.7.5–3 |
| 3.7.5.10 – 32K and 128K BY 8 TTL SSRAM IN DIP AND SOJ | Release 1 | Page 3.7.5–3 |
| 3.7.5.11 – 2K TO 32K BY 9 DPSRAM FAMILY IN 68 SCC | Release 1 | Page 3.7.5–4 |
| 3.7.5.12 – 32K BY 9 CACHE SRAM IN 44 SCC | Release 2 | Page 3.7.5–4 |
| 3.7.5.13 – 128K BY 8 SRAM IN TSOP1 | Release 2 | Page 3.7.5–4 |
| 3.7.5.14 – 128K BY 8 & 9 SSRAM IN SOJ | Release 2 | Page 3.7.5–4 |
| 3.7.5.15 – 1K AND 2K BY 8 DPSRAM FAMILY IN 48 DIP | Release 2 | Page 3.7.5–4 |
| 3.7.5.16 – 128K TO 512K BY 8 SRAM FAMILY IN 32 CDSO–N | Release 3 | Page 3.7.5–4 |
| 3.7.5.17 – 128K TO 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN 33 DIP AND SOJ | Release 3 | Page 3.7.5–4 |
| 3.7.5.18 – 128K TO 2M BY 8/9 BURST SRAM IN BGA | Release 5 | Page 3.7.5–4 |
| 3.7.5.19 – 128K TO 2M BY 8/9 SSRAM IN BGA | Release 5 | Page 3.7.5–4 |
| 3.7.5.20 – 32K BY 8 SRAM IN TSOP1 | Release 7 | Page 3.7.5–4 |
| FIGURE 3.7.5-1, 64 BY 9 SRAM IN SCC | Release 1 | Page 3.7.5-5 |
| FIGURE 3.7.5-2, 1K & 2K BY 8 TTL SRAM IN DIP | Release 1 | Page 3.7.5-6 |
| FIGURE 3.7.5-3, 2K & 4K BY 8 TTL SRAM IN RCC | Release 1 | Page 3.7.5-7 |
| FIGURE 3.7.5-4, 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ | Release 1 | Page 3.7.5-8 |
| FIGURE 3.7.5-5, 0.5K TO 32K BY 8 TTL SRAM FAMILY IN RCC | Release 1 | Page 3.7.5-9 |
| FIGURE 3.7.5-6, 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ | Release 4 | Page 3.7.5-10 |
| FIGURE 3.7.5-7, 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP | Release 1 | Page 3.7.5-11 |
| FIGURE 3.7.5-8, 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP | Release 1 | Page 3.7.5-12 |
| FIGURE 3.7.5-9, 32K TO 2M BY 8 AND 9 TTL SRAM FAMILY IN DIP, TSOP2, AND SOJ | Release 4 | Page 3.7.5-13 |
| FIGURE 3.7.5-10, 32K AND 128K BY 8 TTL SSRAM IN DIP, TSOP2, AND SOJ | Release 4 | Page 3.7.5-14 |
| FIGURE 3.7.5-11, 2K TO 32K BY 9 DPSRAM FAMILY IN SCC | Release 1 | Page 3.7.5-15 |
| FIGURE 3.7.5-12, 32K BY 9 TTL CACHE SRAM IN SCC | Release 2 | Page 3.7.5-16 |
| FIGURE 3.7.5-13, 128K BY 8 TTL SRAM IN TSOP1 | Release 2c9 | Page 3.7.5-17 |
| FIGURE 3.7.5-14, 128K BY 8 & 9 TTL SSRAM IN SOJ | Release 2 | Page 3.7.5-18 |
| FIGURE 3.7.5-15A, 1K AND 2K BY 9 DPSRAM IN DIP | Release 2 | Page 3.7.5-19 |
| FIGURE 3.7.5-15B, 1K AND 2K BY 9 DPSRAM TRUTH TABLE | Release 2 | Page 3.7.5-20 |
| FIGURE 3.7.5-16, 128K TO 512K BY 8 SRAM IN CDSO-N | Release 3 | Page 3.7.5-21 |
| FIGURE 3.7.5-17, 128K AND 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN DIP, TSOP2, & SOJ | Release 4 | Page 3.7.5-22 |
| FIGURE 3.7.5-18 - 128K TO 2M BY 8/9 BURST SRAM IN BGA | Release 5 | Page 3.7.5-23 |
| FIGURE 3.7.5-19 - 128K TO 2M BY 8/9 SSRAM BGA IN BGA | Release 5 | Page 3.7.5-24 |
| FIGURE 3.7.5-20 - 128K TO 2M BY 8/9 SSRAM BGA BOUNDRY SCAN ORDER | Release 5 | Page 3.7.5-25 |
| FIGURE 3.7.5-21, 32K BY 8 SRAM IN TSOP2 | Release 7 | Page 3.7.5-26 |
| **3.7.6 Byte Wide ECL SRAM** | **Release 1** | **Page 3.7.6–1** |
| 3.7.6.1 – 32K and 128K BY 8 ECL SSRAM IN SOJ, SSOP, AND FP | Release 2 | Page 3.7.6–1 |
| FIGURE 3.7.6-1, 32K AND 256K BY 9 ECL SSRAM IN SOJ, SOP, AND FP | Release 2 | Page 3.7.6-3 |
| **3.7.7 Word Wide TTL SRAM** | **Release 11** | **Page 3.7.7–1** |
| 3.7.7.1 – 4K TO 64K BY 16 TTL SRAM IN DIP | Release 1 | Page 3.7.7–2 |
| 3.7.7.2 – 4K TO 256K BY 16 TTL SRAM IN SCC | Release 1 | Page 3.7.7–2 |
| 3.7.7.3 – 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN DIP | Release 1 | Page 3.7.7–2 |


**Release 11a**



Micron Technology Inc. et al.
Ex. 1017, p. 167

| Section | Release # | Page # |
|---|---|---|
| 3.7.7.4 – 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN RCC | Release 1 | Page 3.7.7–2 |
| 3.7.7.5 – 16K AND 64K BY 18 SRAM IN SCC | Release 1 | Page 3.7.7–2 |
| 3.7.7.6 – 64K BY 16 & 18 SRAM IN 44 SOJ | Release 3 | Page 3.7.7–2 |
| 3.7.7.7 – 32K AND 64K BY 16 & 18 SRAM AND SSRAM IN 52 SCC WITH LOGIC FEATURES | Release 4 | Page 3.7.7–2 |
| 3.7.7.8 – 64K TO 256K BY 18 SRAM & SSRAM IN TQFP | Release 5 | Page 3.7.7–3 |
| 3.7.7.9 – 64K TO 1M BY 16/18 BURST SRAM IN BGA | Release 5 | Page 3.7.7–3 |
| 3.7.7.10 – 64K TO 1M BY 16/18 SSRAM IN BGA | Release 5 | Page 3.7.7–3 |
| 3.7.7.11 – 64K TO 256K BY 16/18 BURST SRAM IN QFP/TQFP | Release 6 | Page 3.7.7–3 |
| 3.7.7.12 – 256K AND 1M BY 16/18 SRAM IN TSOP2 | Release 6 | Page 3.7.7–3 |
| 3.7.7.13 – 1Mb TO 128Mb Density, BY 16 OR 18 BURST SRAM IN 221 BGA | Release 11 | Page 3.7.7–3 |
| 3.7.7.14 – 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 209 BGA | Release 11 | Page 3.7.7–3 |
| 3.7.7.15 – 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 221 BGA | Release 11 | Page 3.7.7–3 |
| FIGURE 3.7.7–1, 4K TO 64K BY 16 TTL SRAM FAMILY IN DIP | Release 1 | Page 3.7.7–5 |
| FIGURE 3.7.7–2, 4K TO 256K BY 16 TTL SRAM FAMILY IN RCC | Release 1 | Page 3.7.7–6 |
| FIGURE 3.7.7–3, 16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN DIP | Release 1 | Page 3.7.7–7 |
| FIGURE 3.7.7–4, 16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN RCC | Release 1 | Page 3.7.7–8 |
| FIGURE 3.7.7–5, 16K AND 64K BY 18 SRAM IN SCC | Release 1 | Page 3.7.7–9 |
| FIGURE 3.7.7–6, 64K BY 16 & 18 SRAM IN SOJ | Release 3 | Page 3.7.7–10 |
| FIGURE 3.7.7–7 A, 32K & 64K BY 16 & 18 SRAM AND SSRAM WITH LOGIC FEATURES IN SCC | Release 4 | Page 3.7.7–11 |
| FIGURE 3.7.7–7 B, WRITE CLOCK TIMING FOR SSRAM WITH BURST MODE | Release 4 | Page 3.7.7–12 |
| FIGURE 3.7.7–8, 64K TO 256K BY 18 SRAM AND SSRAM IN TQFP | Release 5 | Page 3.7.7–13 |
| FIGURE 3.7.7–9, 64K TO 1M BY 16/18 BURST SRAM BGA PADOUT | Release 5 | Page 3.7.7–14 |
| FIGURE 3.7.7–10, 64K TO 1M BY 16/18 SSRAM BGA PADOUT | Release 5 | Page 3.7.7–15 |
| FIGURE 3.7.7–11, 64K TO 1M BY 16/18 SSRAM BGA BOUNDRY SCAN ORDER | Release 5c8 | Page 3.7.7–16 |
| FIGURE 3.7.7–12, 64K TO 256K BY 16/18 BURST SRAM IN TQFP | Release 6 | Page 3.7.7–17 |
| FIGURE 3.7.7–13, 256K AND 1M BY 16/18 SRAM IN TSOP2 | Release 6 | Page 3.7.7–18 |
| FIGURE 3.7.7–14, 1Mb TO 128Mb Density, BY 16 OR 18 BURST SRAM IN 221 BGA | Release 11a | Page 3.7.7–19 |
| FIGURE 3.7.7–15, 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 209 BGA | Release 11a | Page 3.7.7–20 |
| FIGURE 3.7.7–16, 1Mb TO 128Mb Density, BY 16 OR 18 SIGMA SRAM IN 221 BGA | Release 11a | Page 3.7.7–21 |
| **3.7.8 Double Word Wide SRAM** | **Release 5** | **Page 3.7.8–1** |
| 3.7.8.1 – 32K TO 128K BY 36 SSRAM WITH BURST IN TQFP | Release 6 | Page 3.7.8–2 |
| 3.7.8.2 – 32K TO 128K BY 36 SRAM & SSRAM IN TQFP | Release 5 | Page 3.7.8–2 |
| 3.7.8.3 – 32K TO 512K BY 32/36 BURST SRAM BGA PADOUT | Release 5 | Page 3.7.8–2 |
| 3.7.8.4 – 32K TO 512K BY 32/36 SSRAM BGA PADOUT | Release 5c11 | Page 3.7.8–2 |
| 3.7.8.5 – 16K TO 36K BY 32 & 64 SSRAM With BURST Counter IN QFP | Release 7 | Page 3.7.8–2 |
| 3.7.8.6 – 16K TO 256K BY 36 & 72 BURST SRAM IN BGA | Release 7 | Page 3.7.8–2 |
| 3.7.8.7 – 1Mb TO 128Mb Density, BY 32 OR 36 BURST SRAM IN 221 BGA | Release 11 | Page 3.7.8–2 |
| 3.7.8.8 – 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 209 BGA | Release 11 | Page 3.7.8–3 |
| 3.7.8.9 – 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 221 BGA | Release 11 | Page 3.7.8–3 |
| FIGURE 3.7.8-1, 32K TO 128K BY 36 SSRAM WITH BURST IN TQFP | Release 6c9 | Page 3.7.8-5 |
| FIGURE 3.7.8-2, 32K TO 128K BY 36 SRAM AND SSRAM IN TQFP | Release 5 | Page 3.7.8-6 |
| FIGURE 3.7.7-3 - 32K TO 512K BY 32/36 BURST SRAM BGA PADOUT | Release 5 | Page 3.7.8-7 |
| FIGURE 3.7.7-4 - 32K TO 512K BY 32/36 SSRAM BGA PADOUT | Release 5 | Page 3.7.8-8 |
| FIGURE 3.7.7-5 - 32K TO 512K BY 32/36 SSRAM BGA BOUNDRY SCAN ORDER | Release 5 | Page 3.7.8-9 |
| FIGURE 3.7.8-6, 16K TO 36K BY 32 & 64 SSRAM With BURST Counter IN QFP | Release 7 | Page 3.7.8-10 |
| FIGURE 3.7.8-7, 16K TO 256K BY 36 & 72 BURST SSRAM IN BGA | Release 7 | Page 3.7.8-11 |
| FIGURE 3.7.8-8, 1Mb TO 128Mb Density, BY 32 OR 36 BURST SRAM IN 221 BGA | Release 11a | Page 3.7.8-12 |
| FIGURE 3.7.8-9, 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 209 BGA | Release 11a | Page 3.7.8-13 |


**Release 11a**



Micron Technology Inc. et al.
Ex. 1017, p. 168

| Section | Release # | Page # |
|---|---|---|
| FIGURE 3.7.8-10, 1Mb TO 128Mb Density, BY 32 OR 36 SIGMA SRAM IN 221 BGA | Release 11a | Page 3.7.8-14 |
| **3.7.9 Eight Byte Wide SRAM** | **Release 11a** | **Page 3.7.9–1** |
| 3.7.9.1 – 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 209 BGA | Release 11a | Page 3.7.9–2 |
| 3.7.9.2 – 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 221 BGA | Release 11a | Page 3.7.9–2 |
| 3.7.9.3 – 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 209 BGA | Release 11a | Page 3.7.9–2 |
| 3.7.9.4 – 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 221 BGA | Release 11a | Page 3.7.9–2 |
| FIGURE 3.7.9-1, 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 209 BGA | Release 11a | Page 3.7.9-3 |
| FIGURE 3.7.9-2, 1Mb TO 128Mb Density, BY 64 OR 72 BURST SRAM IN 221 BGA | Release 11a | Page 3.7.9-4 |
| FIGURE 3.7.9-3, 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 209 BGA | Release 11a | Page 3.7.9-5 |
| FIGURE 3.7.9-4, 1Mb TO 128Mb Density, BY 64 OR 72 SIGMA SRAM IN 221 BGA | Release 11a | Page 3.7.9-6 |
| **3.8 Pseudostatic Random Access Memory (PSRAM)** | **Release 1** | **Page 3.8–1** |
| **3.8.1 PSRAM, Byte Wide** | **Release 1** | **Page 3.8–3** |
| 3.8.1.1 – 2K TO 8K BY 8 PSRAM FAMILY IN DIP | Release 1 | Page 3.8–3 |
| 3.8.1.2 – 2K TO 16K BY 8 PSRAM FAMILY IN RCC | Release 1 | Page 3.8–3 |
| 3.8.1.3 – 32K TO 512K BY 8 PSRAM FAMILY IN SOJ | Release 1 | Page 3.8–3 |
| **3.8.2 PSRAM, Word Wide** | **Release 1** | **Page 3.8–3** |
| 3.8.2.1 – 4K TO 32K BY 16 PSRAM IN DIP | Release 1 | Page 3.8–3 |
| 3.8.2.2 – 4K TO 256K BY 16 PSRAM IN SCC | Release 1 | Page 3.8–3 |
| FIGURE 3.8-1, 2K TO 8K BY 8 PSRAM FAMILY IN DIP | Release 1 | Page 3.8-4 |
| FIGURE 3.8-2, 2K TO 16K BY 8 PSRAM FAMILY IN RCC | Release 1 | Page 3.8-5 |
| FIGURE 3.8-3, 32K TO 512K BY 8 PSRAM FAMILY IN SOJ | Release 1 | Page 3.8-6 |
| FIGURE 3.8-4, 4K TO 32K BY 16 PSRAM FAMILY IN DIP | Release 1 | Page 3.8-7 |
| FIGURE 3.8-5, 4K TO 256K BY 16 PSRAM FAMILY IN SCC | Release 1 | Page 3.8-8 |
| **3.9 Dynamic Random Access Memory (DRAM)** | **Release 1** | **Page 3.9–1** |
| **3.9.1 Bit Wide DRAM** | **Release 1** | **Page 3.9.1–1** |
| 3.9.1.1 – 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES | Release 1 | Page 3.9.1–3 |
| 3.9.1.2 – 16K TO 256K BY 1 DRAM FAMILY IN DIP | Release 1 | Page 3.9.1–3 |
| 3.9.1.3 – 16K TO 256K BY 1 DRAM IN RCC | Release 1 | Page 3.9.1–3 |
| 3.9.1.4 – 64K & 256K BY 1 DRAM IN ZIP | Release 1 | Page 3.9.1–3 |
| 3.9.1.5 – 1M AND 4M BY 1 DRAM FAMILY IN DIP | Release 1 | Page 3.9.1–3 |
| 3.9.1.6 – 1M TO 16M BY 1 DRAM FAMILY IN SOJ OR TSOP2 | Release 4 | Page 3.9.1–3 |
| 3.9.1.7 – 1M TO 16M BY 1 DRAM FAMILY IN ZIP | Release 4 | Page 3.9.1–3 |
| 3.9.1.8 – 1M TO 16M BY 1 NON–MUX DRAM FAMILY IN SOJ | Release 1 | Page 3.9.1–3 |
| 3.9.1.9 – 1M BY 1 DRAM IN TSOP1 | Release 1 | Page 3.9.1–4 |
| 3.9.1.10 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ | Release 1 | Page 3.9.1–4 |
| 3.9.1.11 – 64M BY 1 DRAM IN SOJ OR TSOP2 | Release 5 | Page 3.9.1–4 |
| 3.9.1.12 – 2 X 16M BY 1 DRAM IN TSOP2 | Release 4 | Page 3.9.1–4 |
| 3.9.1.13 – 16M BY 1 DRAM IN USON | Release 9 | Page 3.9.1–4 |
| FIGURE 3.9.1-1, 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES 16K TO 256K BY 1 DRAM FAMILY IN DIP | Release 1 | Page 3.9.1-5 |
| FIGURE 3.9.1-2, 16K TO 256K BY 1 DRAM IN RCC | Release 1 | Page 3.9.1-6 |
| FIGURE 3.9.1-3, 64K & 256K BY 1 DRAM IN ZIP | Release 1 | Page 3.9.1-7 |
| FIGURE 3.9.1-4, 1M TO 64M BY 1 DRAM FAMILY IN DIP | Release 1 | Page 3.9.1-8 |
| FIGURE 3.9.1-5, 1M TO 16M BY 1 DRAM FAMILY IN SOJ and TSOP-2 | Release 4 | Page 3.9.1-9 |
| FIGURE 3.9.1-6, 1M TO 16M BY 1 DRAM FAMILY IN ZIP | Release 4 | Page 3.9.1-10 |
| FIGURE 3.9.1-7, 1M TO 16M BY 1 NON-MUX DRAM FAMILY IN SOJ | Release 2 | Page 3.9.1-11 |
| FIGURE 3.9.1-8, 1M BY 1 DRAM IN TSOP1 | Release 2 | Page 3.9.1-12 |
| FIGURE 3.9.1-9, 16M X 1/4M X 4 CONFIGURABLE DRAM IN SOJ | Release 2 | Page 3.9.1-13 |
| FIGURE 3.9.1-10, 64M BY 1 DRAM IN SOJ & TSOP2 | Release 4 a | Page 3.9.1-14 |
| FIGURE 3.9.1-11, 2 X 16M BY 1 DRAM IN TSOP2 | Release 4 | Page 3.9.1-15 |




Micron Technology Inc. et al.
Ex. 1017, p. 169

| Section | Release # | Page # |
|---|---|---|
| FIGURE 3.9.1-12, 64M BY 1 DRAM IN SOJ & TSOP2 | Release 5r7 | Page 3.9.1-16 |
| FIGURE 3.9.1-13 16M BY 1 DRAM IN USON | Release 9 | Page 3.9.1-17 |
| **3.9.2 Nibble Wide DRAM** | **Release 1** | **Page 3.9.2–1** |
| 3.9.2.1 – 16K & 64K BY 4 DRAM IN DIP | Release 1 | Page 3.9.2–2 |
| 3.9.2.2 – 16K BY 4 DRAM IN DIP | Release 1 | Page 3.9.2–2 |
| 3.9.2.3 – 64K BY 4 DRAM IN RCC | Release 1 | Page 3.9.2–2 |
| 3.9.2.4 – 256K & 1M BY 4 DRAM FAMILY IN DIP | Release 2 | Page 3.9.2–2 |
| 3.9.2.5 – 256K TO 4M BY 4 DRAM FAMILY IN SOJ & TSOP2 | Release 4 | Page 3.9.2–2 |
| 3.9.2.6 – 64K TO 4M BY 4 DRAM IN ZIP | Release 2 | Page 3.9.2–2 |
| 3.9.2.7 – 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2 | Release 3 | Page 3.9.2–2 |
| 3.9.2.8 – 256K BY 4 DRAM IN TSOP1 | Release 2 | Page 3.9.2–2 |
| 3.9.2.9 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ | Release 2 | Page 3.9.2–3 |
| 3.9.2.10 – 256K TO 4M BY 4 NON–MUX DRAM FAMILY IN SOJ | Release 2 | Page 3.9.2–3 |
| 3.9.2.11 – 4M BY 4 DRAM WITH 1 CE AND 4 CE IN TSOP2 | Release 2 | Page 3.9.2–3 |
| 3.9.2.12 – 16M BY 4 DRAM IN SOJ & TSOP2 | Release 5r7 | Page 3.9.2–3 |
| 3.9.2.13 – 1M, 2M, 4M BY 2 DRAM IN SOJ & TSOP2 | Release 3r7 | Page 3.9.2–3 |
| 3.9.2.14 – 16M BY 4 DRAM WITH 4 $\overline{\text{CAS}}$ IN SOJ & TSOP2 | Release 6 | Page 3.9.2–3 |
| 3.9.2.15 – 64M BY 4 DRAM IN TSOP2 PIN ROTATION | Release 6 | Page 3.9.2–3 |
| 3.9.2.16 – 4M BY 4 DRAM IN USON | Release 9 | Page 3.9.2–4 |
| 3.9.2.17 – 16M BY 4 DRAM IN USON | Release 9 | Page 3.9.2–4 |
| FIGURE 3.9.2-1, 16K & 64K BY 4 DRAM IN DIP | Release 1 | Page 3.9.2-5 |
| FIGURE 3.9.2-2, 16K & 64K BY 4 DRAM IN RCC | Release 1 | Page 3.9.2-6 |
| FIGURE 3.9.2-3, 256K & 1M BY 4 DRAM FAMILY IN DIP | Release 1 | Page 3.9.2-7 |
| FIGURE 3.9.2-4, 256K TO 4M BY 4 DRAM IN SOJ AND TSOP-2 | Release 4 | Page 3.9.2-8 |
| FIGURE 3.9.2-5, 64K TO 4M BY 4 DRAM IN ZIP | Release 1 | Page 3.9.2-9 |
| FIGURE 3.9.2-6, 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2 | Release 6 | Page 3.9.2-10 |
| FIGURE 3.9.2-7, 256K BY 4 DRAM IN TSOP1 | Release 2 | Page 3.9.2-11 |
| FIGURE 3.9.2-8, 4M BY 4/16M BY 1 CONFIGURABLE DRAM IN SOJ | Release 2 | Page 3.9.2-12 |
| FIGURE 3.9.2-9, 256K TO 4M BY 4 NON-MUX DRAM IN SOJ | Release 2 | Page 3.9.2-13 |
| FIGURE 3.9.2-10, 4M BY 4 DRAM WITH 4 CE IN SOJ AND TSOP2 | Release 6 | Page 3.9.2-14 |
| FIGURE 3.9.2-11, 16M BY 4 DRAM IN SOJ & TSOP2 | Release 4 a | Page 3.9.2-15 |
| FIGURE 3.9.2-12, 1M, 2M, 4M BY 2 DRAM WITH 2 CE IN SOJ AND TSOP2 | Release 4r7 | Page 3.9.2-16 |
| FIGURE 3.9.2-13, 16M BY 4 DRAM IN SOJ & TSOP2 | Release 5r7 | Page 3.9.2-17 |
| FIGURE 3.9.2-14, 16M BY 4 DRAM WITH 4 $\overline{\text{CAS}}$ IN SOJ & TSOP2 | Release 6r7 | Page 3.9.2-18 |
| FIGURE 3.9.2-15, 64M BY 4 DRAM IN TSOP2 PIN ROTATION | Release 6 | Page 3.9.2-19 |
| FIGURE 3.9.2-16 4M BY 4 DRAM IN USON | Release 9 | Page 3.9.2-20 |
| FIGURE 3.9.2-17 16M BY 4 DRAM IN USON | Release 9 | Page 3.9.2-21 |
| **3.9.3 Byte Wide DRAM** | **Release 1** | **Page 3.9.3–1** |
| 3.9.3.1 – 32K BY 8 DRAM IN DIP | Release 1 | Page 3.9.3–3 |
| 3.9.3.2 – 32K BY 8 DRAM IN RCC | Release 1 | Page 3.9.3–3 |
| 3.9.3.3 – 512K BY 8 & BY 9 DRAM IN SOJ, TSOP2, & ZIP | Release 2 | Page 3.9.3–3 |
| 3.9.3.4 – 512K BY 8 & BY 9 NON–MUX DRAM IN SOJ | Release 2 | Page 3.9.3–3 |
| 3.9.3.5 – 2M BY 8 & 9 DRAM IN SOJ & TSOP2 | Release 5 | Page 3.9.3–3 |
| 3.9.3.6 – 8M BY 8 & 9 DRAM IN SOJ & TSOP2 | Release 5 | Page 3.9.3–3 |
| 3.9.3.7 – 32M BY 8 DRAM IN TSOP2 PIN ROTATION | Release 6 | Page 3.9.3–3 |
| 3.9.3.8 – 4M & 8M BY 8 DRAM IN SOP | Release 8 | Page 3.9.3–4 |
| 3.9.3.9 – 2M BY 8 DRAM IN USON | Release 9 | Page 3.9.3–4 |
| 3.9.3.10 – 8M BY 8 DRAM IN USON | Release 9 | Page 3.9.3–4 |
| FIGURE 3.9.3-1, 32K BY 8 DRAM IN DIP | Release 1 | Page 3.9.3-5 |
| FIGURE 3.9.3-2, 32K BY 8 DRAM IN RCC | Release 1 | Page 3.9.3-6 |
| FIGURE 3.9.3-3, 512K BY 8 & 9 DRAM IN SOJ | Release 2 | Page 3.9.3-7 |




Micron Technology Inc. et al.
Ex. 1017, p. 170

| Section | Release # | Page # |
|---|---|---|
| FIGURE 3.9.3-4, 512K BY 8 & 9 DRAM IN ZIP | Release 2 | Page 3.9.3-8 |
| FIGURE 3.9.3-5, 512K BY 8 & 9 NON-MUX DRAM IN SOJ | Release 2 | Page 3.9.3-9 |
| FIGURE 3.9.3-6, 2M BY 8 & 9 DRAM IN SOJ & TSOP2 | Release 5 | Page 3.9.3-10 |
| FIGURE 3.9.3-7, 8M BY 8 & 9 DRAM IN SOJ & TSOP2 | Release 4 a | Page 3.9.3-11 |
| FIGURE 3.9.3-8, 8M BY 8 DRAM IN SOJ & TSOP2 | Release 5r7 | Page 3.9.3-12 |
| FIGURE 3.9.3-9, 32M BY 8 DRAM IN TSOP2 PIN ROTATION | Release 6 | Page 3.9.3-13 |
| FIGURE 3.9.3-10, 4M & 8M BY 8 DRAM IN SOP | Release 8 | Page 3.9.3-14 |
| FIGURE 3.9.3-11 2M BY 8 DRAM IN USON | Release 9 | Page 3.9.3-15 |
| FIGURE 3.9.3-12 8M BY 8 DRAM IN USON | Release 9 | Page 3.9.3-16 |
| **3.9.4 Word Wide DRAM** | **Release 1** | **Page 3.9.4–1** |
| 3.9.4.1 – 64K BY 16 DRAM WITH 2 W IN SOJ & TSOP2 | Release 1 | Page 3.9.4–3 |
| 3.9.4.2 – 256K & 1M BY 16 & 18 DRAM WITH 2 CE IN SOJ & TSOP2 | Release 5 | Page 3.9.4–3 |
| 3.9.4.3 – 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ | Release 4 | Page 3.9.4–3 |
| 3.9.4.4 – 2M BY 16, 4M BY 16 & 18 DRAM IN TSOP2 | Release 6r7 | Page 3.9.4–3 |
| 3.9.4.5 – 128K AND 256K BY 16 BURST DRAM WITH 2 CAS IN SOJ, TSOP2, AND ZIP | Release 6 | Page 3.9.4–3 |
| 3.9.4.6 – 16M BY 16 DRAM IN TSOP2 PIN ROTATION | Release 6 | Page 3.9.4–4 |
| 3.9.4.7 – 128K ANS 256K BY 32 DRAM WITH 4 $\overline{\text{CAS}}$ IN TSOP2 | Release 6 | Page 3.9.4–4 |
| 3.9.4.8 – 512K AND 2M BY 32 & 36 DRAM WITH 4 $\overline{\text{CAS}}$ IN TSOP2 | Release 6r10 | Page 3.9.4–4 |
| 3.9.4.9 – 8M BY 32 DRAM IN TSOP2 PIN ROTATION | Release 6r9 | Page 3.9.4–4 |
| 3.9.4.10 – 2M BY 32 DRAM IN TSOP2 | Release 7 | Page 3.9.4–4 |
| 3.9.4.11 – 2M BY 32 DRAM WITH EDO IN QFP | Release 6r8 | Page 3.9.4–4 |
| 3.9.4.12 – 1M BY 16 DRAM IN USON | Release 9 | Page 3.9.4–4 |
| 3.9.4.13 – 4M BY 16 DRAM IN USON | Release 9 | Page 3.9.4–4 |
| FIGURE 3.9.4-1, 64K BY 16 DRAM IN SOJ | Release 1 | Page 3.9.4-5 |
| FIGURE 3.9.4-2, 256K BY 16 & 18 DRAM WITH 2 W OR 2 CE IN SOJ | Release 2 | Page 3.9.4-6 |
| FIGURE 3.9.4-3, 256K BY 16 & 18 DRAM WITH 2 W OR 2 CE IN TSOP2 | Release 4 | Page 3.9.4-7 |
| FIGURE 3.9.4-4, 1M BY 16 & 18 DRAM WITH 2 CE IN SOJ | Release 5 | Page 3.9.4-8 |
| FIGURE 3.9.4-5, 1M BY 16 & 18 DRAM WITH 2 CE IN TSOP2 | Release 5 | Page 3.9.4-9 |
| FIGURE 3.9.4-6, 64K BY 16 DRAM WITH 2 W IN TSOP-2 | Release 3 | Page 3.9.4-10 |
| FIGURE 3.9.4-7A, 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ | Release 4 | Page 3.9.4-11 |
| FIGURE 3.9.4-7B, 256K BY 16 DRAM MANDATORY EXTENDED FUNCTION TRUTH TABLE | Release 4 | Page 3.9.4-12 |
| FIGURE 3.9.4-8, 2M BY 16, 4M BY 16 & 18 DRAM IN TSOP-2 | Release 6r7 | Page 3.9.4-13 |
| FIGURE 3.9.4-9, 128K AND 256K BY 16 BURST DRAM IN SOJ | Release 6 | Page 3.9.4-14 |
| FIGURE 3.9.4-10, 128K AND 256K BY 16 BURST DRAM IN TSOP2 | Release 6 | Page 3.9.4-15 |
| FIGURE 3.9.4-11, 128K AND 256K BY 16 BURST DRAM IN ZIP | Release 6 | Page 3.9.4-16 |
| FIGURE 3.9.4-12, 16M BY 16 DRAM IN TSOP2 PIN ROTATION | Release 6 | Page 3.9.4-17 |
| FIGURE 3.9.4-13, 128K AND 256K BY 32 DRAM WITH 4 $\overline{\text{CAS}}$ IN SSOP | Release 8 | Page 3.9.4-18 |
| FIGURE 3.9.4-14, 512K AND 2M BY 32 & 36 DRAM IN SOJ AND TSOP2 | Release 6r10 | Page 3.9.4-19 |
| FIGURE 3.9.4-15, 8M BY 32 DRAM IN TSOP2 PIN ROTATION | Release 9 | Page 3.9.4-20 |
| FIGURE 3.9.4-16, 2M BY 32 DRAM IN TSOP2 | Release 7 | Page 3.9.4-21 |
| FIGURE 3.9.4-17, 256K BY 32 DRAM IN QFP | Release 8 | Page 3.9.4-22 |
| FIGURE 3.9.4-18 1M BY 16 DRAM IN USON | Release 9 | Page 3.9.4-23 |
| FIGURE 3.9.4-19 4M BY 16 DRAM IN USON | Release 9 | Page 3.9.4-24 |
| **3.9.5 DRAM Optional Features** | **Release 1** | **Page 3.9.5–1** |
| 3.9.5.1 – OPTIONAL OPERATIONAL MODES AND CYCLES FOR DRAM | Release 1 | Page 3.9.5–3 |
| 3.9.5.2 – 1M DRAM BUILT IN TEST FUNCTION | Release 1 | Page 3.9.5–3 |
| 3.9.5.3 – ON–CHIP REFRESH CONTROL FOR X8 DRAM | Release 1 | Page 3.9.5–3 |
| 3.9.5.4 – G BEFORE E REFRESH | Release 1 | Page 3.9.5–3 |
| 3.9.5.5 – DRAM SPECIAL TEST AND OPERATIONAL MODES | Release 1 | Page 3.9.5–3 |


**Release 11a**



Micron Technology Inc. et al.
Ex. 1017, p. 171

| Section | Release # | Page # |
|---|---|---|
| 3.9.5.6 – NON–MULTIPLEXED DRAM OPERATION | Release 1 | Page 3.9.5–3 |
| 3.9.5.7 – DRAM EXTENDED DATA OUT DEFINITION | Release 6 | Page 3.9.5–3 |
| 3.9.5.8 – 256m DRAM TEST MODE DATA AND ADDRESS COMPRESSION | Release 7 | Page 3.9.5–3 |
| 3.9.5.9 – PIPELINED NIBBLE MODE DEFINITION | Release 7 | Page 3.9.5–3 |
| FIGURE 3.9.5-1A, DRAM ON CHIP REFRESH TIMING | Release 1 | Page 3.9.5-5 |
| FIGURE 3.9.5-1B, DRAM SELF REFRESH MODE TIMING | Release 4 | Page 3.9.5-5 |
| FIGURE 3.9.5-2, DRAM BIT WRITE TIMING | Release 1 | Page 3.9.5-6 |
| DRAM SPECIAL TEST AND OPERATIONAL MODES | Release 4 | Page 3.9.5-7 |
| OPTIONAL DRAM OPERATIONAL MODES AND CYCLES | Release 3 | Page 3.9.5-11 |
| NON–ADDRESS MULTIPLEXED DRAM OPERATIONAL REQUIREMENTS | Release 3 | Page 3.9.5-13 |
| DRAM EXTENDED DATA OUT DEFINITION | Release 6 | Page 3.9.5-14 |
| 256M DRAM ADDRESS AND DATA COMPRESSION DEFINITION | Release 7 | Page 3.9.5-15 |
| PIPELINED NIBBLE MODE DEFINITION | Release 7 | Page 3.9.5-16 |
| **3.10 Multiport Dynamic RAM (MPDRAM)** | **Release 1** | **Page 3.10–1** |
| **3.10.1 Nibble Wide MPDRAM** | **Release 1** | **Page 3.10.1–1** |
| 3.10.1.1 – 64K BY 4 MPDRAM IN DIP, SOJ, & ZIP | Release 1 | Page 3.10.1–1 |
| 3.10.1.2 – 256K BY 4 MPDRAM IN DIP, SOJ, TSOP2, & ZIP | Release 3 | Page 3.10.1–1 |
| 3.10.1.3 – 256K BY 4 TPDRAM IN SOJ | Release 2 | Page 3.10.1–1 |
| FIGURE 3.10.1-1, 64K BY 4 MPDRAM IN DIP & SOJ | Release 1 | Page 3.10.1-2 |
| FIGURE 3.10.1-2, 64K BY 4 MPDRAM IN ZIP | Release 1 | Page 3.10.1-3 |
| FIGURE 3.10.1-3, 256K BY 4 MPDRAM IN DIP, SOJ, & TSOP2 | Release 3 | Page 3.10.1-4 |
| FIGURE 3.10.1-4, 256K BY 4 MPDRAM IN ZIP | Release 1 | Page 3.10.1-5 |
| FIGURE 3.10.1-5, 256K BY 4 TPDRAM IN SOJ | Release 2 | Page 3.10.1-6 |
| **3.10.2 Byte Wide MPDRAM** | **Release 1** | **Page 3.10.2–1** |
| 3.10.2.1 – 128K AND 256K BY 8 MPDRAM IN DIP, SOJ, & TSOP2 | Release 3 | Page 3.10.2–1 |
| FIGURE 3.10.2-1, 128K AND 256K BY 8 MPDRAM IN DIP & SOJ | Release 2 | Page 3.10.2-2 |
| FIGURE 3.10.2-2, 128K BY 8 MPDRAM IN TSOP2 | Release 3 | Page 3.10.2-3 |
| **3.10.3 Word Wide MPDRAM** | **Release 1** | **Page 3.10.3–1** |
| 3.10.3.1 – 128K & 256K BY 16 MPDRAM IN SOG WITH MULTIPLE CLOCKS | Release 2 | Page 3.10.3–1 |
| 3.10.3.2 – 128K & 256K BY 16 MPDRAM IN TSOP-2 WITH MULTIPLE CLOCKS | Release 5 | Page 3.10.3–1 |
| 3.10.3.3 – 256K BY 16 SGRAM IN TSOP2 | Release 6 | Page 3.10.3–1 |
| 3.10.3.4 – 128K, 256K, & 512K BY 32, 2 & 4 Bank SGRAM IN QFP/TQFP | Release 6r9r10 | Page 3.10.3–1 |
| 3.10.3.5 – 256K BY 32 GRAM IN TSOP-2 | Release 6 | Page 3.10.3–1 |
| 3.10.3.6 – 256K BY 32 SMPDRAM IN TSOP-2 | Release 6 | Page 3.10.3–2 |
| 3.10.3.7 – 256K BY 32 SMPDRAM IN TSOP-2 | Release 7 | Page 3.10.3–2 |
| 3.10.3.8 – 256K BY 32 MPDRAM IN TSOP-2 | Release 7 | Page 3.10.3–2 |
| 3.10.3.9 – 128K, 256K, & 512K BY 32 X 4 BANK SYNCHRONOUS DDR SGRAM IN LQFP | Release 9 | Page 3.10.3–2 |
| FIGURE 3.10.3-1, 128K & 256K BY 16 MPDRAM IN SOG with 2 W & 2 CE | Release 3 | Page 3.10.3-3 |
| FIGURE 3.10.3-2, 128K & 256K BY 16 MPDRAM IN TSOP-2 with 2 W & 2 CE | Release 5 | Page 3.10.3-4 |
| FIGURE 3.10.3-3, 256K BY 16 SGRAM IN TSOP-2 | Release 6 | Page 3.10.3-5 |
| FIGURE 3.10.3-4, 128K, 256K, & 512K BY 32 SGRAM, 2 & 4 BANK IN QFP/TQFP | Release 6c7r9r10 | Page 3.10.3-6 |
| FIGURE 3.10.3-5, 256K BY 32 SGRAM IN TSOP-2 | Release 6 | Page 3.10.3-7 |
| FIGURE 3.10.3-6, 256K BY 32 SYNCH. MPDRAM IN QFP/TQFP | Release 6 | Page 3.10.3-8 |
| FIGURE 3.10.3-7, 256K BY 32 MPDRAM IN QFP/TQFP | Release 7 | Page 3.10.3-9 |
| FIGURE 3.10.3-8 128K, 256K, & 512K BY 32 X 4 BANK DDR SGRAM IN LQFP | Release 9r10 | Page 3.10.3-10 |
| **3.10.4 MPDRAM Optional Features** | **Release 1** | **Page 3.10.4–1** |
| 3.10.4.1 – 256K X 4 MPDRAM MINIMUM FEATURE SET TRUTH TABLE | Release 1 | Page 3.10.4–3 |
| 3.10.4.2 – 256K X 4 MPDRAM EXTENDED FEATURE SET TRUTH TABLE | Release 1 | Page 3.10.4–3 |
| 3.10.4.3 – MPDRAM BIT WRITE OPTIONAL FEATURE | Release 1 | Page 3.10.4–3 |
| 3.10.4.4 – 128K X 8 MPDRAM MINIMUM FEATURE SET TRUTH TABLE | Release 1 | Page 3.10.4–3 |

| Section | Release # | Page # |
|---|---|---|
| 3.10.4.5 – 128K X 8 MPDRAM EXTENDED FEATURE SET TRUTH TABLE | Release 1 | Page 3.10.4–3 |
| 3.10.4.6 – 128K X 16, 256K X 8, & 256K X 16 MPDRAM MINIMUM FEATURE SET TRUTH TABLE | Release 5 | Page 3.10.4–3 |
| 3.10.4.7 – 128K X 16, 256K X 8, & 256K X 16 MPDRAM EXTENDED FEATURE SET TRUTH TABLE | Release 5 | Page 3.10.4–3 |
| 3.10.4.8 – SPLIT REGISTER WITH PROGRAMMABLE STOPS FOR MPDRAM | Release 3 | Page 3.10.4–3 |
| 3.10.4.9 – PIPELINED FAST PAGE MODE FOR MPDRAM | Release 2 | Page 3.10.4–4 |
| 3.10.4.10 – EXTENDED DATA OUT FAST PAGE MODE FOR MPDRAM | Release 2 | Page 3.10.4–4 |
| 3.10.4.11 – SAM LENGTH DEFINITION FOR 2/4M MPDRAM | Release 5 | Page 3.10.4–4 |
| 3.10.4.12 – SYNCH GRAM SPECIAL MODE SET PROCEDURE | Release 6 | Page 3.10.4–4 |
| 3.10.4.13 – SYNCH. MPDRAM SPECIAL MODE SET PROCEDURE | Release 6 | Page 3.10.4–4 |
| 3.10.4.14 – SYNCH. GRAM OPERATIONAL FUNCTION TRUTH TABLES | Release 6 | Page 3.10.4–4 |
| 3.10.4.15 – 8Mb MPDRAM FEATURE SET FUNCTION TABLE | Release 7 | Page 3.10.4–4 |
| 3.10.4.16 – EXTENDED FUNCTIONSFOR SGRAM & MPDRAM | Release 6r7 | Page 3.10.4–4 |
| TABLE 3.10.4-1, 256K X 4 MPDRAM FEATURE SET TRUTH TABLE | Release 1 | Page 3.10.4-5 |
| TABLE 3.10.4-2, 128K X 8 MPDRAM FEATURE SET TRUTH TABLE | Release 1 | Page 3.10.4-6 |
| FIGURE 3.10.4-1, BIT WRITE TIMING | Release 1 | Page 3.10.4-7 |
| TABLE 3.10.4-3, 2Mb & 4Mb MPDRAM FEATURE SET TRUTH TABLE | Release 5 | Page 3.10.4-8 |
| FIGURE 3.10.4-2, SPLIT REGISTER WITH PROGRAMMABLE STOPS | Release 2 | Page 3.10.4-9 |
| FIGURE 3.10.4-3A, PIPELINED FAST PAGE MODE | Release 2 | Page 3.10.4-10 |
| FIGURE 3.10.4-3B, PIPELINED FAST PAGE MODE | Release 2 | Page 3.10.4-11 |
| FIGURE 3.10.4-4, MPDRAM EXTENDED DATA OUT FAST PAGE MODE | Release 4 | Page 3.10.4-12 |
| FIGURE 3.10.4-5A & 5B, SAM LENGTH DEFINITION FOR 4M MPDRAM | Release 5 | Page 3.10.4-13, 14 |
| FIGURE 3.10.4-6, SYNCH GRAM SPECIAL MODE SET PROCEDURE | Release 6 | Page 3.10.4-15 |
| FIGURE 3.10.4-7, SYNCH. MPDRAM SPECIAL MODE SET PROCEDURE | Release 6 | Page 3.10.4-16 |
| TABLE 3.10.4–4 A,B, & C , SGRAM FUNCTION TRUTH TABLE | Release 6r7 | Page 3.10.4-17⇒19 |
| TABLE 3.10.4–5, 8Mb BURST MPDRAM FUNCTION TABLE | Release 7 | Page 3.10.4-20 |
| EXTENDED FUNCTIONS FOR SGRAM & MPDRAM | Release 7 | Page 3.10.4-21 |
| **3.11 Synchronous Dynamic Random Access Memory (SDRAM)** | **Release 4** | **Page 3.11–1** |
| **3.11.1 Bit Wide SDRAM** | **Release 4** | **Page 3.11.1–1** |
| FIGURE 3.11.1-1, | Release 4 | Page 3.11.1-5 |
| **3.11.2 Nibble Wide SDRAM** | **Release 4** | **Page 3.11.2–1** |
| 3.11.2.1 – 4M BY 4 SDRAM IN TSOP2 | Release 6r7r8 | Page 3.11.2–1 |
| 3.11.2.2 – 16M BY 4 SDRAM IN TSOP2 | Release 6 | Page 3.11.2–1 |
| 3.11.2.3 – 64M BY 4 SDRAM IN TSOP2 PIN ROTATION | Release 7r9 | Page 3.11.2–1 |
| 3.11.2.4 – 16M, 32M, 64M, & 128M BY 4 DDR SDRAM IN TSOP2 | Release 8r9r10r11 | Page 3.11.2–1 |
| 3.11.2.5 – 32M, 64M, & 64M BY 4 SDRAM IN TSOP2 | Release 8r9r10 | Page 3.11.2–1 |
| 3.11.2.6 – 16M BY 4 VIRTUAL CHANNEL SDRAM IN TSOP2 | Release 9 | Page 3.11.2–1 |
| 3.11.2.7 – 16M, 32M, & 64M BY 4 STACKABLE SDR SDRAM IN LSOJ | Release 9 | Page 3.11.2–2 |
| 3.11.2.8 – 16M, 32M, & 64M BY 4 VIRTUAL CHANNEL DDR SDRAM IN TSOP2 | Release 9r11 | Page 3.11.2–2 |
| 3.11.2.9 – 16M, 32M, 64M, & 128M BY 4 STACKABLE DDR SDRAM IN LSOJ | Release 9r10r11 | Page 3.11.2–2 |
| 3.11.2.10 – 16M BY 4 SDR SDRAM IN USON | Release 9 | Page 3.11.2–2 |
| 3.11.2.11 – 16M, 32M, & 64M BY 4 SDR SDRAM IN TSOP2 | Release 9 | Page 3.11.2–2 |
| 3.11.2.12 – 16M, & 32M BY 4 SDR SDRAM IN LFBGA | Release 9 | Page 3.11.2–2 |
| 3.11.2.13 – 16M, & 32M BY 4 DDR SDRAM IN LFBGA | Release 9 | Page 3.11.2–3 |
| 3.11.2.14 – 16M, & 32M BY 4 SDR SDRAM IN LFBGA | Release 9 | Page 3.11.2–3 |
| 3.11.2.15 – 16M, & 32M BY 4 DDR SDRAM IN LFBGA | Release 9r11 | Page 3.11.2–3 |
| 3.11.2.16 – 64M, & 128M BY 4 SDR SDRAM IN LFBGA | Release 11a | Page 3.11.2–3 |
| 3.11.2.17 – 16M, 32M, 64M, & 128M BY 4 DDR SDRAM IN LFBGA | Release 11a | Page 3.11.2–3 |
| FIGURE 3.11.2-1, 4M X 4 SDRAM IN TSOP2 | Release 6r7 | Page 3.11.2-5 |




Micron Technology Inc. et al.
Ex. 1017, p. 173

| Section | Release # | Page # |
|---|---|---|
| FIGURE 3.11.2-2, 16M X 4 SDRAM IN TSOP2 | Release 6 | Page 3.11.2-6 |
| FIGURE 3.11.2-3, 64M X 4 SDRAM IN TSOP2 PIN ROTATION | Release 7r9 | Page 3.11.2-7 |
| FIGURE 3.11.2-4, 16M, 32M, 64M, & 128M X 4 DDR SDRAM IN TSOP2 | Release 8r9r10r11 | Page 3.11.2-8 |
| FIGURE 3.11.2-5 32M, 64M, & 128M X 4 SDRAM IN TSOP2 | Release 8r9r10r11 | Page 3.11.2-9 |
| FIGURE 3.11.2-6 16M X 4 VC SDRAM IN TSOP2 | Release 9 | Page 3.11.2-10 |
| FIGURE 3.11.2-7 16M, 32M, & 64M BY 4 STACKABLE SDR SDRAM IN LSOJ | Release 9 | Page 3.11.2-11 |
| FIGURE 3.11.2-8 16M, 32M, & 64M BY 4 VC DDR SDRAM IN TSOP2 | Release 9c10r11 | Page 3.11.2-12 |
| FIGURE 3.11.2-9 16M, 32M, 64M & 128M BY 4 STACKABLE DDR SDRAM IN LSOJ | Release 9r10r11 | Page 3.11.2-13 |
| FIGURE 3.11.2-10 16M BY 4 SDRAM IN USON | Release 9 | Page 3.11.2-14 |
| FIGURE 3.11.2-11 16M, 32M, & 64M BY 4 SDR SDRAM IN TSOP2 | Release 9 | Page 3.11.2-15 |
| FIGURE 3.11.2-12 16M & 32M BY 4 SDR SDRAM IN LFBGA | Release 9 | Page 3.11.2-16 |
| FIGURE 3.11.2-13 16M & 32M BY 4 DDR SDRAM IN LFBGA | Release 9 | Page 3.11.2-17 |
| FIGURE 3.11.2-14 16M, 32M, & 64M BY 4 SDR SDRAM IN LFBGA | Release 9c10 | Page 3.11.2-18 |
| FIGURE 3.11.2-15 16M, 32M, & 64M BY 4 DDR SDRAM IN LFBGA | Release 9c10r11 | Page 3.11.2-19 |
| FIGURE 3.11.2-16 64M, & 128M BY 4 SDR SDRAM IN FBGA | Release 11a | Page 3.11.2-20 |
| FIGURE 3.11.2-17 32M, 64M, 128M, & 256M BY 4 DDR SDRAM IN FBGA | Release 11a | Page 3.11.2-21 |
| **3.11.3 BYTE WIDE SDRAM** | **Release 4** | **Page 3.11.3–1** |
| 3.11.3.1 – 2M BY 8 or 9 SDRAM IN TSOP2 | Release 6r7 | Page 3.11.3–1 |
| 3.11.3.2 – 8M BY 8 SDRAM IN TSOP2 | Release 6 | Page 3.11.3–1 |
| 3.11.3.3 – 32M BY 8 SDRAM PIN ROTATION | Release 7r9 | Page 3.11.3–1 |
| 3.11.3.4 – 8M, 16M, 32M, & 64M BY 8 DDR SDRAM IN TSOP2 | Release 8r9r10r11 | Page 3.11.3–1 |
| 3.11.3.5 – 16M, 32M, & 64M BY 8 SDRAM IN TSOP2 | Release 8r9r10 | Page 3.11.3–1 |
| 3.11.3.6 – 8M, 16M, & 32M BY 8 SDR SDRAM IN TSOP2 | Release 9 | Page 3.11.3–1 |
| 3.11.3.7 – 8M, 16M, & 32M BY 8 STACKABLE SDR SDRAM IN LSOJ | Release 9 | Page 3.11.3–2 |
| 3.11.3.8 – 8M, 16M, 32M, & 64M BY 8 STACKABLE DDR SDRAM IN LSOJ | Release 9r10r11 | Page 3.11.3–2 |
| 3.11.3.9 – 2M BY 8 SDR SDRAM IN USON | Release 9 | Page 3.11.3–2 |
| 3.11.3.10 – 8M BY 8 SDR SDRAM IN USON | Release 9 | Page 3.11.3–2 |
| 3.11.3.11 – 8M BY 8 VIRTUAL CHANNEL SDRAM IN TSOP2 | Release 9 | Page 3.11.3–2 |
| 3.11.3.12 – 8M, 16M, & 32M BY 8 VIRTUAL CHANNEL DDR SDRAM IN TSOP2 | Release 9r11 | Page 3.11.3–2 |
| 3.11.3.13 – 8M, & 16M BY 8 SDR SDRAM IN LFBGA | Release 9 | Page 3.11.3–3 |
| 3.11.3.14 – 8M, & 16M BY 8 DDR SDRAM IN LFBGA | Release 9 | Page 3.11.3–3 |
| 3.11.3.15 – 8M, & 16M BY 8 SDR SDRAM IN LFBGA | Release 9 | Page 3.11.3–3 |
| 3.11.3.16 – 8M, 16M, 32M, & 64M BY 8 DDR SDRAM IN LFBGA | Release 9r11 | Page 3.11.3–3 |
| 3.11.3.17 – 16M, 32M, & 64M BY 8 Low Power SDR SDRAM IN FBGA | Release 11a | Page 3.11.3–3 |
| 3.11.3.18 – 32M, & 64M BY 8 SDR SDRAM IN LFBGA | Release 11a | Page 3.11.3–3 |
| 3.11.3.19 – 16M, 32M, 64M, & 128M BY 8 DDR SDRAM IN FBGA | Release 11a | Page 3.11.3–4 |
| FIGURE 3.11.3-1, 2M BY 8 OR 9 SDRAM IN TSOP2 | Release 6r7 | Page 3.11.3-5 |
| FIGURE 3.11.3-2, 8M BY 8 SDRAM IN TSOP2 | Release 6 | Page 3.11.3-6 |
| FIGURE 3.11.3-3, 32M BY 8 SDRAM IN TSOP2 PIN ROTATION | Release 7r9 | Page 3.11.3-7 |
| FIGURE 3.11.3-4, 8M, 16M, & 32M BY 8 DDR SDRAM IN TSOP2 | Release 8r9r10r11 | Page 3.11.3-8 |
| FIGURE 3.11.3-5, 16M, 32M, & 64M BY 8 SDRAM IN TSOP2 PIN ROTATION | Release 8r9r10 | Page 3.11.3-9 |
| FIGURE 3.11.3-6 8M, 16M, & 32M BY 8 SDR SDRAM IN TSOP2 | Release 9 | Page 3.11.3-10 |
| FIGURE 3.11.3-7 8M, 16M, & 32M BY 8 STACKABLE SDR SDRAM IN LSOJ | Release 9 | Page 3.11.3-11 |
| FIGURE 3.11.3-8 8M, 16M, 32M, 64M & 128M BY 8 STACKABLE DDR SDRAM IN LSOJ | Release 9r10r11 | Page 3.11.3-12 |
| FIGURE 3.9.3-9 2M BY 8 SDRAM IN USON | Release 9 | Page 3.11.3-13 |
| FIGURE 3.11.3-10 8M BY 8 SDRAM IN USON | Release 9 | Page 3.11.3-14 |
| FIGURE 3.11.3-11 8M X 8 VC SDRAM IN TSOP2 | Release 9 | Page 3.11.3-15 |
| FIGURE 3.11.3-12 8M, 16M, & 32M BY 8 VC DDR SDRAM IN TSOP2 | Release 9c10r11 | Page 3.11.3-16 |
| FIGURE 3.11.3-13 8M & 16M BY 8 SDR SDRAM IN LFBGA | Release 9 | Page 3.11.3-17 |
| FIGURE 3.11.3-14 8M & 16M BY 8 DDR SDRAM IN LFBGA | Release 9 | Page 3.11.3-18 |
| FIGURE 3.11.3-15 8M, 16M, & 32M BY 8 SDR SDRAM IN LFBGA | Release 9c10 | Page 3.11.3-19 |


**Release 11a**



Micron Technology Inc. et al.
Ex. 1017, p. 174

| Section | Release # | Page # |
|---|---|---|
| FIGURE 3.11.3-16 8M, 16M, 32M & 64M BY 8 DDR SDRAM IN LFBGA | Release 9c10r11 | Page 3.11.3-20 |
| FIGURE 3.11.3-17 16M, 32M & 64M BY 8 SDR SDRAM IN FBGA | Release 11a | Page 3.11.3-21 |
| FIGURE 3.11.3-18 32M & 64M BY 8 SDR SDRAM IN FBGA | Release 11a | Page 3.11.3-22 |
| FIGURE 3.11.3-19 16M, 32M, 64M & 128M BY 8 DDR SDRAM IN FBGA | Release 11a | Page 3.11.3-23 |
| **3.11.4 WORD WIDE SDRAM** | **Release 5** | **Page 3.11.4–1** |
| 3.11.4.1 – 256K BY 16 AND 1M BY 16/18 SDRAM IN TSOP-2 | Release 6r7 | Page 3.11.4–2 |
| 3.11.4.2 – 2M & 4M BY 16 SDRAM IN TSOP-2 | Release 6r7 | Page 3.11.4–2 |
| 3.11.4.3 – 16M BY 16 SDRAM IN TSOP-2 PIN ROTATION | Release 6r9 | Page 3.11.4–2 |
| 3.11.4.4 – 128K, 256K, & 512K, 2 & 4 Bank BY 32 SDRAM IN QFP/TQFP/LQFP | Release 6r7r9r10 | Page 3.11.4–2 |
| 3.11.4.5 – 2M BY 32 SDRAM IN TSOP-2 | Release 6r7r10 | Page 3.11.4–2 |
| 3.11.4.6 – 8M BY 32 SDRAM IN TSOP-2 PIN ROTATION | Release 6r9 | Page 3.11.4–3 |
| 3.11.4.7 – 2M BY 32 & 36, 4M & 8M BY 32 SDRAM IN TSOP-2 | Release 7r8r10r11a | Page 3.11.4–3 |
| 3.11.4.8 – 4M, 8M, 16M, & 32M BY 16, DDR SDRAM IN TSOP-2 | Release 8r9r10r11 | Page 3.11.4–3 |
| 3.11.4.9 – 8M & 16M BY 16, SDRAM IN TSOP-2 | Release 8r9r10 | Page 3.11.4–3 |
| 3.11.4.10 – 4M, 8M, & 16M BY 16 SDR SDRAM IN TSOP2 | Release 9 | Page 3.11.4–3 |
| 3.11.4.11 – 4M, 8M, & 16M BY 16 STACKABLE SDR SDRAM IN LSOJ | Release 9 | Page 3.11.4–3 |
| 3.11.4.12 – 4M, 8M, 16M, 32M, & 64M BY 16 STACKABLE DDR SDRAM IN LSOJ | Release 9r11 | Page 3.11.4–4 |
| 3.11.4.13 – 4M BY 16 SDR SDRAM IN USON | Release 9 | Page 3.11.4–4 |
| 3.11.4.14 – 4M BY 16 VIRTUAL CHANNEL SDRAM IN TSOP2 | Release 9 | Page 3.11.4–4 |
| 3.11.4.15 – 4M, 8M, & 16M BY 16 VIRTUAL CHANNEL DDR SDRAM IN TSOP2 | Release 9r11 | Page 3.11.4–4 |
| 3.11.4.16 – 4M, & 8M BY 16 SDR SDRAM IN LFBGA | Release 9 | Page 3.11.4–4 |
| 3.11.4.17 – 4M, & 8M BY 16 DDR SDRAM IN LFBGA | Release 9 | Page 3.11.4–4 |
| 3.11.4.18 – 4M, & 8M BY 16 SDR SDRAM IN LFBGA | Release 9 | Page 3.11.4–5 |
| 3.11.4.19 – 4M, & 8M BY 16 DDR SDRAM IN LFBGA | Release 9r11 | Page 3.11.4–5 |
| 3.11.4.20 – 4M BY 16/18 SLDRAM IN TSOP2 | Release 9 | Page 3.11.4–5 |
| 3.11.4.21 – 4M TO 64M BY 16/18 SLDRAM IN R–PZIP | Release 9 | Page 3.11.4–5 |
| 3.11.4.22 – 128K, 256K, & 512K BY 32, 4 BANK DDR SDRAM IN LQFP | Release 9r10r11 | Page 3.11.4–5 |
| 3.11.4.23 – 2M & 4M BY 32, 4 BANK, DDR SDRAM IN FBGA | Release 11a | Page 3.11.4–5 |
| 3.11.4.24 – 8M, 16M, & 32M BY 16, Low Power SDR SDRAM IN FBGA | Release 11a | Page 3.11.4–6 |
| 3.11.4.25 – 16M, & 32M BY 16 SDR SDRAM IN FBGA | Release 11a | Page 3.11.4–6 |
| 3.11.4.26 – 8M, 16M, 32M, & 64M BY 16 DDR SDRAM IN FBGA | Release 11a | Page 3.11.4–6 |
| 3.11.4.27 – 2M & 4M BY 32 SDR SDRAM IN LFBGA | Release 11a | Page 3.11.4–6 |
| 3.11.4.28 – 2M, 4M, & 8M BY 32, Low Power SDR SDRAM IN FBGA | Release 11a | Page 3.11.4–6 |
| FIGURE 3.11.4-1, 256 BY 16 AND 1M BY 16/18 SDRAM IN TSOP-2 | Release 6r7 | Page 3.11.4-7 |
| FIGURE 3.11.4-2, 4M BY 16 SDRAM IN TSOP-2 | Release 6r7 | Page 3.11.4-8 |
| FIGURE 3.11.4-3, 16M BY 16 SDRAM IN TSOP-2 | Release 6c7r9 | Page 3.11.4-9 |
| FIGURE 3.11.4-4, 128K, 256K, & 512K BY 32 SDRAM IN QFP/TQFP | Release 6c7r9r10 | Page 3.11.4-10 |
| FIGURE 3.11.4-5, 2M BY 32 SDRAM IN TSOP-2 | Release 6r7r10 | Page 3.11.4-11 |
| FIGURE 3.11.4-6, 8M BY 32 SDRAM IN TSOP-2 PIN ROTATION | Release 6c7r9 | Page 3.11.4-12 |
| FIGURE 3.11.4-7, 2M BY 32 & 36, 4M & 8M BY 32 SDRAM IN TSOP-2 | Release 7r8r10 | Page 3.11.4-13 |
| FIGURE 3.11.4-8, 4M, 8M, 16M, & 32M BY 16 DDR SDRAM IN TSOP-2 | Release 8r9r10r11 | Page 3.11.4-14 |
| FIGURE 3.11.4-9, 8M, 16M, & 32M BY 16 SDRAM IN TSOP-2 | Release 8r9r10 | Page 3.11.4-15 |
| FIGURE 3.11.4-10 4M, 8M, & 16M BY 16 SDR SDRAM IN TSOP2 | Release 9 | Page 3.11.4-16 |
| FIGURE 3.11.4-11 4M, 8M, & 16M BY 16 SDR STACKABLE SDRAM IN LSOJ | Release 9 | Page 3.11.4-17 |
| FIGURE 3.11.4-12 4M, 8M, 16M, & 32M BY 16 STACKABLE DDR SDRAM IN LSOJ | Release 9r10r11 | Page 3.11.4-18 |
| FIGURE 3.11.4-13 4M BY 16 SDRAM IN USON | Release 9 | Page 3.11.4-19 |
| FIGURE 3.11.4-14 4M X 16 VC SDRAM IN TSOP2 | Release 9 | Page 3.11.4-20 |
| FIGURE 3.11.4-15 4M, 8M, & 16M BY 16 VC DDR SDRAM IN TSOP2 | Release 9c10r11 | Page 3.11.4-21 |
| FIGURE 3.11.4-16 4M & 16M BY 16 SDR SDRAM IN LFBGA | Release 9 | Page 3.11.4-22 |
| FIGURE 3.11.4-17 4M & 16M BY 16 DDR SDRAM IN LFBGA | Release 9 | Page 3.11.4-23 |
| FIGURE 3.11.4-18 4M, 8M, &16M BY 16 SDR SDRAM IN LFBGA | Release 9c10 | Page 3.11.4-24 |


**Release 11a**



Micron Technology Inc. et al.
Ex. 1017, p. 175

| Section | Release # | Page # |
|---|---|---|
| FIGURE 3.11.4–19 8M, 16M, & 32M BY 16 DDR SDRAM IN LFBGA | Release 9c10r11 | Page 3.11.4–25 |
| FIGURE 3.11.4–20 4M TO 64M BY 16 & 18 SLDRAM IN R–PZIP | Release 9 | Page 3.11.4–26 |
| FIGURE 3.10.4–21 4M BY 16/18 SLRAM IN TSOP2 | Release 9 | Page 3.11.4–27 |
| FIGURE 3.11.4–22 128K, 256K, & 512K X 32 X 4 BANK DDR SDRAM IN QFP | Release 9r10r11 | Page 3.11.4–28 |
| FIGURE 3.11.4–23 2M, 4M & 8M BY 32 DDR SDRAM IN FBGA | Release 11a | Page 3.11.4–29 |
| FIGURE 3.11.4–24 8M, 16M & 32M BY 16 SDR SDRAM IN FBGA | Release 11a | Page 3.11.4–30 |
| FIGURE 3.11.4–25 16M & 32M BY 16 SDR SDRAM IN FBGA | Release 11a | Page 3.11.4–31 |
| FIGURE 3.11.4–26 8M, 16M, 32M & 64M BY 16 DDR SDRAM IN FBGA | Release 11a | Page 3.11.4–32 |
| FIGURE 3.11.4–27 2M & 4M BY 32 SDR SDRAM IN LFBGA | Release 11a | Page 3.11.4–33 |
| FIGURE 3.11.4–28 2M, 4M & 8M BY 32, Low Power SDR SDRAM IN LFBGA | Release 11a | Page 3.11.4–34 |
| **3.11.5 SDRAM Architectural and Operational Features See P 3.11.5–1 for detailed Table of Contents** | **Release 4–9** | **Page 3.11.5–1** |
| 3.11.5.1 – General SDRAM Functions | Release 4–r9 | Page 3.11.5.1–1 |
| 3.11.5.2 – DDR Specific SDRAM Functions | Release 9 | Page 3.11.5.2–1 |
| 3.11.5.3 – ESDRAM Specific SDRAM Functions | Release 9 | Page 3.11.5.3–1 |
| 3.11.5.4 – VCSDRAM Specific SDRAM Functions | Release 9 | Page 3.11.5.4–1 |
| **3.11.6 – SDRAM Parametric Specifications** | **Release 9** | **Page 3.11.6–1** |
| 3.11.6.1 – DDR SDRAM/SGRAM I/O Voltage | Release 9 | Page 3.11.6–3 |
| 3.11.6.2 – 256M SDRAM/SGRAM REFRESH SPECIFICATION | Release 9 | Page 3.11.6–3 |
| 3.11.6.3–16MB & 64MB TIMING SPECIFICATIONS (LVTTL) | Release 8 | Pages 3.11.6–4⇒6 |
| 3.11.6.4 – STANDARD FOR DOUBLE DATA RATE (DDR) SDRAM/SGRAM INPUT INTERFACE SPECIFICATIONS | Release 9 | Pages 3.11.6–7 |
| 3.11.6.5 – DDR SDRAM Self-Refresh Exit Timing | Release 9 | Pages 3.11.6–8 |
| 3.11.6.6 – AC TIMING PARAMETERS FOR DDR SDRAMs/SGRAMs | Release 9 | Pages 3.11.6–9⇒19 |
| **3.20. MEMORY DEVICE COMPLETE SPECIFICATION APPENDIX** | **Release 11** | **Page 3.20–1** |
| 3.20.1 – DDR SDRAM Device Specification | Release 11 | Page 3.20–1 |
| 3.20.2 – DDR2 SDRAM Device Specification | Release 11 | Page 3.20–1 |
| **4. MULTI–CHIP MEMORY MODULES & CARDS** | **Release 7r11** | **Page 4–1** |
| **4.1. Memory Module Nomenclature and General Features** | **Release 7r11** | **Page 4.1–1** |
| 4.1.1 Memory Module Nomenclature | Release 1–7 | Page 4.1–1 |
| 4.1.2 Serial Presence Detect General Standard | Release 1–7r9 | Page 4.1.2–1 |
| 4.1.2.1 SPD Appendix A, Table of Fundamental Memory Types | Release 8r9 | Page 4.1.2.1–1 |
| 4.1.2.2 SPD Appendix B, Table of Superset Memory Types | Release 7r9r11 | Page 4.1.2.2–1 |
| 4.1.2.3 SPD Appendix C, Specific PDs for FP and EDO DRAM | Release 7 | Page 4.1.2.3–1 |
| 4.1.2.4 SPD Appendix D, Specific PDs for DDR SDRAM | Release 7r11 | Page 4.1.2.4–1 |
| 4.1.2.5 SPD Appendix E, Specific PDs for SDR SDRAM | Release 7r8$_2$c9r11 | Page 4.1.2.5–1 |
| 4.1.2.6 SPD Appendix F, Specific PDs for Addr. MX ROM | Release 7 | Page 4.1.2.6–1 |
| 4.1.2.7 SPD Appendix G, Not yet assigned | Release 9 | Page 4.1.2.7–1 |
| 4.1.2.8 SPD Appendix H, Table of ESDRAM Attributes | Release 9 | Page 4.1.2.8–1 |
| 4.1.2.9 SPD Appendix V, Specific PDs for VCSDRAM | Release 9 | Page 4.1.2.9–1 |
| **4.2. One BYTE Modules** | **Release 7** | **Page 4.2–1** |
| 4.2.1 – 22 PIN SIP/SIMM 4 bit DRAM MODULE | Release 1-7 | Page 4.2–1 |
| 4.2.2 – 24 PIN SIP/SIMM 4 bit DRAM MODULE | Release 1-7 | Page 4.2–1 |
| 4.2.3 – 30 PIN SIP/SIMM 8 or 9 bit DRAM MODULE | Release 4-7 | Page 4.2–1 |
| 4.2.4 – 30 PIN SIP/SIMM 1, 2, 4, 5, or 8 bits DRAM MODULE FAMILY | Release 1-7 | Page 4.2–1 |
| 4.2.5 – 23/25/26/28 PIN ZIP/SIMM 1 or 4 bit DRAM MODULE FAMILY | Release 1-7 | Page 4.2–2 |
| 4.2.6 – 60 PIN ZIP/SIMM 4 bit SRAM MODULE | Release 1-7 | Page 4.2–2 |
| 4.2.7 – 70 PIN ZIP/SIMM 9 bit SRAM MODULE | Release 1-7 | Page 4.2–2 |


**Release 11a**



Micron Technology Inc. et al.
Ex. 1017, p. 176

| Section | Release # | Page # |
|---|---|---|
| FIGURE 4.2-1, 22, 24,& 30 PIN DRAM MODULES | Release 4-7 | Page 4.2-3 |
| FIGURE 4.2-2, 30 PIN DRAM MODULE FAMILY | Release 1-7 | Page 4.2-4 |
| FIGURE 4.2-3, 23/25/26/28 PIN DRAM MODULE FAMILY | Release 1-7 | Page 4.2-5 |
| FIGURE 4.2-4, 2 X 64K TO 1M BY 4, 60 PIN SRAM MODULE FAMILY | Release 1-7 | Page 4.2–6 |
| FIGURE 4.2-5, 64K TO 1M BY 9, 70 PIN SRAM MODULE FAMILY | Release 1-7 | Page 4.2–7 |
| **4.3. Two BYTE Modules and Cards** | **Release 7** | **Page 4.3–1** |
| 4.3.1 – 76 PIN ZIP/SIMM 9 or 18 bit SRAM MODULE | Release 1-7 | Page 4.3–1 |
| 4.3.2 – 40 PIN SIP/SIMM 1, 2, 4, 5, 8, 9, 16, or 18 DRAM MOD FAMILY | Release 1-7 | Page 4.3–1 |
| 4.3.3 – 60 PIN DRAM 16 or 18 bit CARD FAMILY | Release 2-7 | Page 4.3–1 |
| 4.3.4 – 68 PIN MULTIPLE TECHNOGY MEMORY 16 bit CARD FAMILY | Release 3-7 | Page 4.3–1 |
| FIGURE 4.3-1, 2 X 64K TO 1M BY 9, 76 PIN SRAM MODULE FAMILY | Release 1-7 | Page 4.3-3 |
| FIGURE 4.3-2, 40 PIN DRAM MODULE FAMILY | Release 1-7 | Page 4.3-4 |
| FIGURE 4.3-3A, 60 PIN DRAM CARD FAMILY PIN CONNECTIONS | Release 2-7 | Page 4.3-5 |
| FIGURE 4.3-3B, 60 PIN CARD FAMILY BLOCK DIAGRAMS | Release 2-7 | Page 4.3-6 |
| FIGURE 4.3-4A, 68 PIN MULTIPLE TECHNOLOGY CARD FAMILY | Release 3-7 | Page 4.3-7 |
| FIGURE 4.3-4B, 68 PIN MULTIPLE TECHNOLOGY CARD FAMILY FUNCTION TRUTH TABLES | Release 3-7 | Page 4.3-8 |
| **4.4. Four BYTE Modules and Cards** | **Release 7** | **Page 4.4–1** |
| 4.4.1 – 64 & 72 PIN ZIP/SIMM 32 bit SRAM MODULE | Release 6-7 | Page 4.4.1–1 |
| FIGURE 4.4.1-1, 16K TO 4M BY 32, 64 & 72 PIN SRAM MODULE FAMILY | Release 6-7 | Page 4.4.1–2 |
| 4.4.2 – 72 PIN SIMM 32 or 36 bit DRAM MODULE FAMILY | Release 6-7 | Page 4.4.2–1 |
| – 72 PIN SIMM 36 or 39 DRAM ECC MODULE FAMILY | Release 6-7 | Page 4.4.2–1 |
| FIGURE 4.4.2-2 A, 256K TO 256M BY 36. 72 PIN DRAM MODULE PINOUT | Release 6-7c8 | Page 4.4.2-3 |
| FIGURE 4.4.2-2 B⇒K, 72 PIN 36 BIT DRAM SIMM BLOCK DIAGRAMS | Release 6-7 | Page 4.4.2-4⇒13 |
| FIGURE 4.4.2-3 A, 256K TO 256M BY 32, 36. & 40 BIT 72 PIN DRAM MODULE | Release 6-7 | Page 4.4.2-14 |
| FIGURE 4.4.2-3 B⇒C 72 PIN 32, 36, & 40 BIT DRAM SIMM BLOCK DIAGRAMS | Release 6-7 | Page 4.4.2-15⇒16 |
| 4.4.3 – 88 PIN, 32/36/39 bit DRAM CARD FAMILY | Release 6-7 | Page 4.4–1 |
| FIGURE 4.4.3-1 A, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY | Release 6-7 | Page 4.4.3-3 |
| FIGURE 4.4.3-1 B, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY CONFIGURATION TABLES | Release 6-7 | Page 4.4.3-4 |
| FIGURE 4.4.3-1 C, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG. | Release 6-7 | Page 4.4.3-5 |
| FIGURE 4.4.3-1 D, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG. | Release 6-7 | Page 4.4.3-6 |
| FIGURE 4.4.3-1 E, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG. | Release 6-7 | Page 4.4.3-7 |
| FIGURE 4.4.3-1 F, 256K TO 128M BY 36, 88 PIN DRAM CARD FAMILY BLOCK DIAG. | Release 6-7 | Page 4.4.3-8 |
| – 88 PIN, 40 bit DRAM CARD FAMILY | Release 4-7 | Page 4.4.3-1 |
| FIGURE 4.4.3-2 A, 256K TO 128M BY 40 DRAM CARD | Release 4-7 | Page 4.4.3-9 |
| FIGURE 4.4.3-2 B, 256K TO 128M BY 40 DRAM CARD PD TRUTH TABLE | Release 4-7 | Page 4.4.3-10 |
| FIGURE 4.4.3-2 C, 256K TO 64M BY 40 DRAM CARDUSING BY 4 DEVICES | Release 4-7 | Page 4.4.3-11 |
| FIGURE 4.4.3-2 D, 512K TO 128M BY 40 DRAM CARD USING BY 4 DEVICES | Release 4-7 | Page 4.4.3-12 |
| FIGURE 4.4.3-2 E, 512K TO 32M BY 40 DRAM CARD USING BY 8 DEVICES | Release 4-7 | Page 4.4.3-13 |
| FIGURE 4.4.3-2 F, 1M TO 64M BY 40 DRAM CARD USING BY 8 DEVICES | Release 4-7 | Page 4.4.3-14 |
| 4.4.4 – 72 PIN 32 or 36 bit DRAM SO–DIMM FAMILY | Release 5-7 | Page 4.4.4–1 |
| FIGURE 4.4.4- A 32 & 36 BIT 72 PIN DRAM SO-DIMM PINOUT, PRESENCE DETECT & CONFIGURATION TABLES | Release 6-7 | Page 4.4.4-1 |
| FIGURE 4.4.4-B-D 32 & 36 BIT DRAM SO-DIMM BLOCK DIAGRAMS | Release 5-7 | Page 4.4.4-2⇒5 |
| 4.4.5 – 88 PIN 32 or 36 bit DRAM SO–DIMM FAMILY | Release 5-7 | Page 4.4.5–1 |
| FIGURE 4.4.5-A, 88 PIN 32 & 36 BIT DRAM SO-DIMM PINOUT | Release 6-7 | Page 4.4.5-2 |
| FIGURE 4.4.5-B, 88 PIN 32 & 36 BIT DRAM SO-DIMM PD TRUTH TABLES | Release 6-7 | Page 4.4.5-3 |
| FIGURE 4.4.5-C⇒F, 88 PIN 32 & 36 BIT DRAM SO-DIMM BLOCK DIAGRAMS | Release 6-7 | Page 4.4.5-4⇒7 |
| 4.4.6 – 112 PIN 32 bits MPDRAM SO–DIMM FAMILY | Release 5-7 | Page 4.4.6–1 |




Micron Technology Inc. et al.
Ex. 1017, p. 177

| Section | Release # | Page # |
|---|---|---|
| FIGURE 4.4.6-A, 112 PIN 32 BIT MPDRAM DIMM PINOUT | Release 6-7 | Page 4.4.6-2 |
| FIGURE 4.4.6- B, C, 112 PIN 32 BIT MPDRAM DIMM PD TRUTH TABLES AND BLOCK DIAGRAMS | Release 6-7 | Page 4.4.6-3, 4 |
| 4.4.7 – 80 PIN 32 bit EEPROM SIMM FAMILY | Release 4-7c8 | Page 4.4.7–1 |
| FIGURE 4.4.7-A, 128K TO 8M BY 32 EEPROM SIMM, PINOUT AND PD TABLES | Release 4-7 | Page 4.4.7-3 |
| FIGURE 4.4.7-B, 128K TO 8M BY 32 EEPROM SIMM BLOCK DIAGRAM | Release 4-7 | Page 4.4.7-4 |
| 4.4.8 – 100 PIN 32, 36, or 40 BIT DRAM, SDRAM, ROM DIMM FAMILY | Release 7 | Page 4.4.8–1 |
| FIGURE 4.4.8-B & C, 32, 36, or 40 bit 100 PIN MODULE PINOUT | Release 7c8 | Page 4.4.8-3, 4 |
| FIGURE 4.4.8-D, 32, 36, or 40 bit 100 PIN MODULE PIN COMPARISON | Release 7 | Page 4.4.8-5 |
| FIGURE 4.4.8-E, 32, 36, or 40 bit 100 PIN MODULE CLOCK WIRING | Release 7c8 | Page 4.4.8-6 |
| FIGURE 4.4.8-F⇒AE, 32, 36, or 40 bit 100 PIN MODULE BLOCK DIAGRAMS | Release 7c8 | Page 4.4.8-7⇒32 |
| **4.5. Eight BYTE Modules and Cards** | **Release 7r8r9** | **Page 4.5–1** |
| 4.5.1 – 168 PIN Buffered DRAM, 64, 72, or 80 Bit DIMM FAMILY | Release 6-7 | Page 4.5.1–1 |
| FIGURE 4.5.1-A-B, 64, 72, or 80 BIT SIMM PINOUT, TOP & BOTTOM HALVES | Release 4-7r9 | Page 4.5.1-2,3 |
| FIGURE 4.5.1-C, 64, 72, or 80 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES | Release 6-7 | Page 4.5.1-4 |
| FIGURE 4.5.1-D, 64, 72, & 80 BIT DRAM SIMM Capacity Table | Release 4-7 | Page 4.5.1-5 |
| FIGURE 4.5.1-E-AB, 64, 72, & 80 BIT CONFIGURATION BLOCK DIAGRAMS | Release 4-c7c8 | Page 4.5.1-6-29 |
| 4.5.2 – 200 PIN SDRAM, 64, 72, or 80 DIMM FAMILY | Release 5-7c8c9r11 | Page 4.5.2–1 |
| FIGURE 4.5.2-A, B, 8 -BYTE SDRAM DIMM PINOUT | Release 5-7r8r11 | Page 4.5.2-3,4 |
| FIGURE 4.5.2- C, 8-BYTE SDRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES | Release 5-7 | Page 4.5.2-5 |
| FIGURE 4.5.2-D, E, 8-BYTE SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS | Release 5-7 | Page 4.5.2-6 |
| FIGURE 4.5.2-F-M, 8-BYTE SDRAM DIMM BLOCK DIAGRAMS | Release 5-7 | Page 4.5.2-7,14 |
| 4.5.3 – 168 PIN Unbuffered DRAM, 64, 72, or 80 DIMM FAMILY with SPD | Release 5-7 | Page 4.5.3–1 |
| FIGURE 4.5.3-A, B, 8 -BYTE DRAM DIMM PINOUT | Release 5-7r9 | Page 4.5.3-2,3 |
| FIGURE 4.5.3-D, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS | Release 5-7 | Page 4.5.3-5 |
| FIGURE 4.5.3-E, Pinout comparison, 168P DRAM & SDRAM | Release 5-7c8 | Page 4.5.3-6 |
| FIGURE 4.5.3- F, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES | Release 5-7r8-1 | Page 4.5.3-7 |
| FIGURE 4.5.3-G-U, 8-BYTE DRAM DIMM BLOCK DIAGRAMS | Release 5-7r8 | Page 4.5.3-8,20 |
| 4.5.4 – 168 PIN Unbuffered SDRAM, 64, 72, or 80 DIMM FAMILY with SPD | Release 5-7c8 | Page 4.5.4–1 |
| FIGURE 4.5.4-A, B, 8 -BYTE SDRAM DIMM PINOUT | Release 5-7r9 | Page 4.5.4-2,3 |
| FIGURE 4.5.4- C, 8-BYTE SDRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES | Release 5-7r8 | Page 4.5.4-4 |
| FIGURE 4.5.4-E, 8-BYTE SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS | Release 5-7r8 | Page 4.5.4-6 |
| FIGURE 4.5.4-I-AK, 8-BYTE SDRAM DIMM BLOCK DIAGRAMS | Release 5-7r8r9 | Page 4.5.4-10⇒38 |
| 4.5.5 – 144 PIN Unbuffered DRAM, 64, or 72, SO-DIMM FAMILY with SPD | Release 5-7r8 | Page 4.5.5–1 |
| FIGURE 4.5.5-A, B, 8 -BYTE DRAM DIMM PINOUT | Release 5-7r9 | Page 4.5.5-2,3 |
| FIGURE 4.5.5-C, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS | Release 5-7 | Page 4.5.5-4 |
| FIGURE 4.5.5- E, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES | Release 5-7 | Page 4.5.5-6 |
| FIGURE 4.5.5-F-AB, 8-BYTE DRAM DIMM BLOCK DIAGRAMS | Release 5-7r8 | Page 4.5.5-7⇒16 |
| 4.5.6 – 144 PIN Unbuffered SDRAM, 64, or 72 SO-DIMM FAMILY with SPD | Release 5-7 | Page 4.5.6–1 |
| FIGURE 4.5.6-A, B, 8 -BYTE DRAM DIMM PINOUT | Release 5-7r9 | Page 4.5.6-2,3 |
| FIGURE 4.5.6- C, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES | Release 5-7 | Page 4.5.6-6 |
| FIGURE 4.5.6-D, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS | Release 5-7 | Page 4.5.6-4 |
| FIGURE 4.5.6-G-P, 8-BYTE DRAM DIMM BLOCK DIAGRAMS | Release 5-7 | Page 4.5.6-7⇒17 |
| 4.5.7 – 168 PIN Registered SDRAM, 64, 72 or 80 DIMM FAMILY with SPD | Release 8r11 | Page 4.5.7–1 |
| FIGURE 4.5.7-A, B, 8 -BYTE DRAM DIMM PINOUT | Release 8r9 | Page 4.5.7-2,3 |




Micron Technology Inc. et al.
Ex. 1017, p. 178

| Section | Release # | Page # |
|---|---|---|
| FIGURE 4.5.7- C, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES | Release 8 | Page 4.5.7-4 |
| FIGURE 4.5.7-D, 8-BYTE DRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS | Release 8 | Page 4.5.7-5 |
| FIGURE 4.5.7-I-X, 8-BYTE DRAM DIMM BLOCK DIAGRAMS | Release 8c9r10r11 | Page 4.5.7-9⇒24 |
| 4.5.8 – 144 PIN SGRAMSDRAM, 32 & 64 SO-DIMM FAMILY with SPD | Release 8r10 | Page 4.5.8–1 |
| FIGURE 4.5.8-A, B, 8 -BYTE DRAM DIMM PINOUT | Release 8r9r10 | Page 4.5.8-2,3 |
| FIGURE 4.5.8- C, 8-BYTE DRAM DIMM PRESENCE DETECT & CONFIGURATION TABLES | Release 8 | Page 4.5.8-4 |
| FIGURE 4.5.8-D-F, 8-BYTE DRAM DIMM LAYOUT CONSIDERATIONS | Release 8 | Page 4.5.8-5⇒9 |
| FIGURE 4.5.8-G-J, 8-BYTE DRAM DIMM BLOCK DIAGRAMS | Release 8r10 | Page 4.5.8-10⇒13 |
| 4.5.9 – 144 PIN SGRAM SO–DIMM FAMILY | Release 9 | Page 4.5.9–1 |
| FIGS. 4.5.9-A & B, PIN ASSIGNMENTS | Release 9 | Page 4.5.9–2,3 |
| FIGURE 4.5.9-C, CLOCK NET ROUTING | Release 9 | Page 4.5.9–6 |
| FIGURE 4.5.9-D TO G, BLOCK DIAGRAMS | Release 9 | Page 4.5.9–7⇒10 |
| 4.5.10 – 184 PIN UNBUFFERED DDR SDRAM DIMM FAMILY | Release 9 | Page 4.5.10–1 |
| FIGURES. 4.5.10-A, & B, PIN ASSIGNMENTS | Release 9 | Page 4.5.10–2,3 |
| FIGURES. 4.5.10-C, SUMMARY OF FEATURES AND PIN DESCRIPTION | Release 9 | Page 4.5.10–4 |
| FIGURE 4.5.10-D, SPD TABLE & INFORMATION | Release 9 | Page 4.5.10–5 |
| FIGURE 4.5.10-E, COMPARISON OF 184 PIN UNBUFFERED SDR SDRAM & DDR SDRAM DIMM-- | Release 9 | Page 4.5.10–6 |
| FIGURE 4.5.10-F, KEYING METHODOLOGY | Release 9 | Page 4.5.10–7 |
| FIGURE 4.5.10-G & H, VDDID DEFINITION | Release 9 | Page 4.5.10-8 & 9 |
| FIGURES 4.5.10-I through P, CONFIGURATION BLOCK DIAGRAM-- | Release 9 | Page 4.5.10-10⇒17 |
| 4.5.11 – 184 PIN UNBUFFERED SDR SDRAM DIMM FAMILY | Release 10 | Page 4.5.11–1 |
| FIGURES. 4.5.11-A, & B, PIN ASSIGNMENTS | Release 10 | Page 4.5.11–2,3 |
| FIGURES. 4.5.11-C, SUMMARY OF FEATURES AND PIN DESCRIPTION | Release 10 | Page 4.5.11–4 |
| FIGURE 4.5.11-D, SPD TABLE & INFORMATION | Release 10 | Page 4.5.11–5 |
| FIGURE 4.5.11-E, COMPARISON OF 184 PIN UNBUFFERED SDR SDRAM & DDR SDRAM DIMM-- | Release 10 | Page 4.5.11–6 |
| FIGURE 4.5.11-F, KEYING METHODOLOGY | Release 10 | Page 4.5.11–7 |
| FIGURE 4.5.11-G & H, VDDID DEFINITION | Release 10 | Page 4.5.11-8 & 9 |
| FIGURE 4.5.11-I & J, CLOCK LAYOUT | Release 10 | Page 4.5.11-10 & 11 |
| FIGURE 4.5.11-G & H, FET SWITCH STRUCTURE | Release 10 | Page 4.5.11-12 |
| FIGURES 4.5.11-L through U, CONFIGURATION BLOCK DIAGRAM-- | Release 10 | Page 4.5.11-13⇒23 |
| 4.5.12 – 184 PIN DIMM FAMILY SUPPLEMENTARY DESIGN STANDARDS | Release 10 | Page 4.5.12–1, 2 |
| FIGURES 4.5.12-A through Q, CONFIGURATION BLOCK DIAGRAM-- | Release 10 | Page 4.5.12-3⇒19 |
| FIGURE 4.5.12-R & S, CLOCK LAYOUT | Release 10 | Page 4.5.12-20⇒ 23 |
| FIGURES. 4.5.12-TA, & TB, 184P DDR REGISTERED DIMM PIN ASSIGNMENTS | Release 10 | Page 4.5.12-24⇒26 |
| 4.5.13 – 144 & 168 PIN PROCESSOR ENHANCED MEMORY MODULE FAMILIES WITH EDO–DRAM OR SDRAM | Release 10 | Page 4.5.13–1 |
| 4.5.13.1, PEMM SPECIFIC TERMS AND DEFINITIONS | Release 10 | Page 4.5.13–2 |
| 4.5.13.2, PEMM MODES OF OPERATION | Release 10 | Page 4.5.13–3⇒7 |
| 4.5.13.3, REPRESENTATIVE BLOCK DIAGRAMS | Release 10 | Page 4.5.13-8⇒12 |
| 4.6. Sixteen BYTE Modules | Release 7 | Page 4.6–1 |
| 4.6.1 – 278 PIN Buffered SDRAM, 144 Bit DIMM FAMILY | Release 7 | Page 4.6.1–1 |
| FIGURE 4.6.1-A,B,C, 144 BIT SIMM PINOUT, TOP, MIDDLE, & BOTTOM PARTS | Release 7c8 | Page 4.6.1-2,3,4 |
| FIGURE 4.6.1-D, 144 BIT SIMM PRESENCE DETECT & CONFIGURATION TABLES | Release 7 | Page 4.6.1-5 |
| FIGURE 4.6.1-E, F, 144 BIT SDRAM DIMM MECHANICAL KEY AND PIN DEFINITIONS | Release 5-7 | Page 4.6.1-6 |
| FIGURE 4.6.1-G, H, 144 BIT SDRAM CONFIGURATION BLOCK DIAGRAMS | Release 7 | Page 4.6.1-7, 8 |
| 4.20 – MODULE SPECIFICATION APPENDIX | Release 11 | Page 4.20–1 |




Micron Technology Inc. et al.
Ex. 1017, p. 179

| Section | Release # | Page # |
|---|---|---|
| 4.20.1 – Standard Template for JEDEC Module Specification Standards | Release 11 | Page 4.20.1-1⇒4 |
| 4.20.2 – 168 Pin PC133 SDRAM Registered DIMM Design Specification | Release 11 | Page 4.20.2-1⇒71 |
| 4.20.3 – 144 Pin PC133 SDRAM Unbuffered SO-DIMM Reference Design Specification | Release 11 | Page 4.20.3-1⇒26 |
| 4.20.4 – 184 Pin PC1600/2100 DDR SDRAM Registered DIMM Design Specification | Release 11 | Page 4.20.4-1⇒61 |
| 4.20.5 – 184 Pin PC1600/2100 DDR SDRAM Unbuffered DIMM Design Specification | Release 11 | Page 4.20.5-1⇒41 |
| 4.20.6 – 200 Pin PC2700 DDR SDRAM Unbuffered SO-DIMM Reference Design Spec. | Release 11 | Page 4.20.6-1⇒26 |
| **5 PROGRAMMABLE LOGIC AND ASIC DEVICES** | **Release 1** | **Page 5–1** |
| **5.1 Pin Out Standards** | **Release 1** | **Page 5–1** |
| **5.1.1 PIN–OUT STANDARDS FOR PLD DIP TO SCC CONVERSION** | **Release 4** | **Page 5–1** |
| 5.1.1.1 – 20 PIN DIP to 20 TERMINAL SCC, 0.350“ BY 0.350”, Fig. 5–1 | Release 1 | Page 5–1 |
| 5.1.1.2 – 24 PIN DIP to 28 TERMINAL SCC, 0.450“ BY 0.450”, Fig. 5–2 | Release 1 | Page 5–1 |
| 5.1.1.3 – 28 PIN DIP to 28 TERMINAL SCC, 0.450“ BY 0.450”, Fig. 5–2 | Release 1 | Page 5–1 |
| 5.1.1.4 – 24 PIN FUNCTIONS IN 28 PIN DIP & 28 TERMINAL SCC, Fig. 5–9 | Release 1 | Page 5–1 |
| 5.1.1.5 – 20 PIN FUNCTIONS IN 28 TERMINAL SCC AND 24 PIN DIP FOR HIGH SPEED OPERATION, Fig. 5–11 | Release 4 | Page 5–1 |
| **5.1.2 POWER PIN LOCATIONS FOR PLD and ASIC DEVICES** | **Release 1** | **Page 5–1** |
| 5.1.2.1 – POWER PIN LOCATIONS FOR ECL PLD IN DIP | Release 1 | Page 5–1 |
| 5.1.2.2 – POWER PIN LOCATIONS FOR TTL PLD IN DIP and CC | Release 1 | Page 5–1 |
| 5.1.2.3 – POWER PIN LOCATIONS FOR TTL PROGRAMMABLE ASIC IN DIP and CC | Release 1 | Page 5–1 |
| 5.1.2.4 – POWER PIN LOCATIONS FOR PLD IN 132 PIN QFP | Release 1 | Page 5–1 |
| **5.1.3 Nomenclature for FPLD** | **Release 1** | **Page 5–1** |
| **5.1.4 PLD Data Transfer Format** | **Release 1** | **Page 5–1** |
| **5.1.5 PLD Standard OUTPUT LOADS** | **Release 5** | **Page 5–1** |
| FIGURE 5-1, 20 PIN DIP TO 20 TERMINAL CC PLD CONVERSION | Release 1 | Page 5-3 |
| FIGURE 5-2, 24 & 28 PIN DIP TO 27 TERMINAL CC CONVERSION | Release 2 | Page 5-4 |
| FIGURE 5-3, POWER PIN PLACEMENT FOR ECL PLD | Release 1 | Page 5-5 |
| FIGURE 5-4, 40 PIN DIP PLD POWER PIN PLACEMENT | Release 1 | Page 5-6 |
| FIGURE 5-5, 44 TERMINAL CC POWER PIN PLACEMENT | Release 1 | Page 5-7 |
| FIGURE 5-6, 48 & 64 PIN DIP ASIC POWER PIN PLACEMENT | Release 1 | Page 5-8 |
| FIGURE 5-7, 52, 68, & 84 TERMINAL CC ASIC POWER PIN PLACEMENT | Release 1 | Page 5-9 |
| FIGURE 5-8A, PLD STANDARD LOADS, DEFINITIONS | Release 5 | Page 5-11 |
| FIGURE 5-8B, PLD STANDARD LOAD CIRCUIT | Release 5 | Page 5-12 |
| FIGURE 5-8C, PLD OUTPUT LOAD CALCULATIONS | Release 5 | Page 5-13 |
| FIGURE 5-8D, PLD AC LOAD LINES | Release 5 | Page 5-14 |
| FIGURE 5-9, 24 PIN PLD FUNCTIONS IN 28 PIN DIP AND SCC | Release 3 | Page 5-15 |
| FIGURE 5-10, 132 PIN PQFP POWER PIN LOCATIONS | Release 3 | Page 5-16 |
| FIGURE 5-11, HIGH SPEED PINOUT FOR 20 PIN PLD FUNCTIONS | Release 4 | Page 5-17 |
| **6 APPLICABLE OTHER DOCUMENTS** | **Release 1** | **Page 6–1** |
| **6.1 – Standard Manufacturers Identification Code., JEDEC Publication No. 106A** | **Release 1** | **Page 6–1** |
| **6.2 – Interface Standard for Low Voltage TTL–Compatible Devices (LVTTL), JEDEC Standard No. 8 and Addendum No. 1** | **Release 1** | **Page 6–1** |
| **6.3 – Package Outlines, JEDEC Publication 95** | **Release 1** | **Page 6–1** |
| **6.4 – PLD Data Transfer Format, JEDEC Standard 3–B** | **Release 1** | **Page 6–1** |
| **6.5 – Nomenclature for FPLD, EIA Standard RS–428** | **Release 1** | **Page 6–1** |
| **6.6 – DDR SDRAM Device Specification, JESD–79** | **Release 11** | **Page 6–1** |


**Release 11a**



Micron Technology Inc. et al.
Ex. 1017, p. 180

R9 TOC HISTORY AND REVISION LOG

10–5–94 . . . . . Edit TOC from R5 Book. Add all new items except DRAM.
10–6–94 . . . . . Complete addition of new items
10–18–94 . . . . Add additional items
10–24–94 . . . . Complete TOC changes
12–16–94 . . . . Add SO–DIMM Module
10–31–95 . . . . Update to R6
12–?–96 . . . . . Update to R7
1–13–98 . . . . . Update to R8
7–16–98 . . . . . Update to R8–2
2–22–99 . . . . . Update to R9
4–14–99 . . . . . Additional R9 updates
9–13–99 . . . . . Add Features to TOC Ver 9.2

R–10 TOC HISTORY & REVISION LOG

10–23–00 . . . . Update to R10 changes.
11–09–00 . . . . Final edit of sec 3.11.n, not include 3.11.6 additions

R–11 TOC HISTORY and REVISION LOG.

11–9–01 . . . . . Update to R11
11–16–01 . . . . Correct PC1800 to PC1600
2–14–02 . . . . . Update to R11a



Micron Technology Inc. et al.
Ex. 1017, p. 181

# Exhibit D

The Wayback Machine - https://web.archive.org/web/20031208154552/http://www.jedec.org:80/service_members/New_Members/memberco.cfm
08-Dec-2003

• Home »
• Join JEDEC »
• For members »
• Standards-publications »
• JEDEC Store»
• Meetings and events »
• Press and news »
• Search »
• To JEDEX »
• GaAs workshop »
• Obtain an ID code »
• Contacts & Help »
• Privacy »

JEDEC

## JEDEC MEMBER COMPANIES

«Go Back

**The following is a list of the member companies that participate in JEDEC, they are listed alphabetically.**

| | |
|---|---|
| Actel Corporation | Mathios Associates |
| Adtec Corporation | Micro Memory Bank |
| Advanced Memory International | Micron Technology Inc. |
| Advanced Micro Devices | Micropac Industries |
| Advanced Power Technology | Microsemi Corporation |
| Advanced Semiconductor Engineering | Minco Technology Inc. |
| Aeluros | Mini Systems Inc. |
| Aeroflex Labs Inc. | Molex Inc. |
| Aeroflex UTMC | Mosel Vitelic Corporation |
| Agere Systems | Motorola Inc. |
| Agilent Technologies | Nanya Technology Semiconductor |
| ALi Corporation | National Semiconductor |
| Allegro MicroSystems | NEC Electronics |
| Alliance Semiconductor | Netlist Incorporated |
| Altera Corporation | New Jersey Micro Electronic Testing Inc. |
| Amkor Technology | NewLogic Technologies AG |
| Anadigics Inc. | Nimbus Wireless Inc. |
| Analog Devices Inc. | Nitto Denko America |
| Apacer Technology | Nokia Research Center |
| Apple Computer Inc. | |
| ArrayComm Inc. | |

**NEWS ARTICLES**

Click here for article:
Micron rolls out GDDR3 SDRAM for graphics applications
Proposed by: Youri Pepplinkhuizen

Micron Technology Inc. Wednesday said it has delivered what it claimed are the industry's first samples of the next-generation GDDR3 SDRAM for graphics applications.

••>SUGGEST AN ARTICLE<••

Try online JEDEC dictionary
digital-to-analog [D/A] converter (DAC):
A converter that represents a limited number of different digital input codes by a corresponding number

From JEDEC Catalog:
MO112-B open/download
Registration - Metric Quad Flatpack Family (Plastic) 3.9 mm Footprint. Item 11.11-422.
FREE Registration to search our database

JEDEX San Jose 2004

**Deadline for CALL FOR PAPERS is December 15, 2003.**

**Papers are now being solicited from industry experts in areas such as packaging, memory and wireless technology.**

International Conference On LEAD-FREE ELECTRONIC COMPONENTS AND ASSEMBLIES IPC JEDEC

**CD from Lead Free Conference (including Tin Whiskers papers) Oct. 2003 Frankfurt,Germany.**

JEDEX Shanghai 上海

**Videos (Chinese TV) from JEDEX Shanghai, International conference on seminconductor applications. October 21-22, 2003 Shanghai, China**

• **JEDEC STORE NOW OPEN**

**Purchase educational CD's proceedings, JEDEC dictionary etc... CLICK HERE TO ENTER.**



Micron Technology Inc. et al.
Ex. 1017, p. 183

- Arrow Zeus Electronics
- Artisan Components
- ASAT Inc.
- ATI Research Silicon Valley Inc.
- Atmel Corporation
- ATP Electronics Inc.
- Austin Semiconductor
- Avant Technology L.P.
- Aved Memory Products
- Avnet Inc.
- BAE Systems
- Bourns Ltd.
- Broadcom Corporation
- Buffalo Inc.
- C-MAC Microcircuits Ltd.
- California Eastern Labs
- Carsem Inc.
- Caspian Networks Inc.
- Catalyst Semiconductor Inc.
- Celestica Inc.
- Centon Electronics Inc.
- Chartered Semiconductor Manufacturing
- ChipPac Inc.
- Chip Supply Inc.
- Cirrus Logic Inc.
- Cisco Systems Inc.
- CMC Electronics Cincinnati
- Northrup Grumman
- NVIDIA Corporation
- OKI Electric Industry Company
- Olin Aegis
- ON Semiconductor
- OSE USA
- Peak International
- Pericom Semiconductor
- Philips Semiconductors
- Plastronics Inc.
- PMC/Sierra
- PNY Technologies Inc.
- Power Integrations Inc.
- Powerex Inc.
- Pulse Engineering
- QP Semiconductor
- Qualcomm
- REMEC
- RF Micro Devices
- Radia Communication
- Ramaxel Technology Ltd.
- Raza Foundries
- Renesas Technology
- Ricoh Company Limited
- Rochester Electronics
- Saifun Semiconductor
- Samsung Semiconductor
- SanDisk Corporation



Micron Technology Inc. et al.
Ex. 1017, p. 184

Cogiscan Inc.

Corsair Memory Inc.

Crane Interpoint Corporation

Cray Incorporated

CST (Comp.Serv.Tech)

Cypress Semiconductor

Daewon USA

Dane-Elec Corporation

Data Device Corporation

Dataram

Delkin Devices Inc.

Dell Computer

Delphi Corporation

Denali Software

DPAC Technologies Corporation

e.PAK International Incorporated

EEMS Italia SpA

Elite Semiconductor Memory Technology

Elpida Memory Inc.

EMC Corporation

EMS Technologies Inc.

Endicott Interconnect Technologies

Enplas Tesco Inc.

Entegris Incorporated

Etron Technology Inc.

Exar Corporation

Fairchild Semiconductor

San Max Technologies Inc.

Sanyo Semiconductor

Sarnoff Corporation

Semicoa Semiconductor

Semtech Corporation

Sensitron Semiconductor

Serverworks Corporation

Shanghai Meadvile Science & Technology Co. Ltd.

Sharp Electronics

Shikatronics Inc.

Shinko Electric America

Siemens

Silego Technology

Silicon Integrated Systems

Silicon Graphics Inc.

Silicon Mountain Memory

Silicon Storage Technology

Siliconware USA Inc.

Simple/SiliconTech Technology

Smart Modular Technology

Sony Corporation

ST Assembly Test Services

Staktek Corporation

STMicroelectronics

Sud-Chemie Performace Packaging



Micron Technology Inc. et al.
Ex. 1017, p. 185

| | |
|---|---|
| FCI USA Inc. | Summit Computer Systems Inc. |
| Flomerics Inc. | Sun Microsystems Inc. |
| Fluent Incorporated | Swissbit Germany AG |
| FormFactor Inc. | T-RAM Inc. |
| Foxconn International Inc. | Taiwan Semiconductor |
| Fujitsu Microelectronics America | Tektronix |
| General Test Laboratory | Teledyne Microelectronics |
| Globespan Virata Inc. | Teradyne Inc. |
| GSI Technology | Texas Instruments |
| Hagiwara Systems | Thermo KeyTek |
| Hana Microelectronics Inc. | Theta Microelectronics |
| Hewlett Packard Company | Toshiba America |
| Hi/FN Inc. | Transmeta Corporation |
| Honeywell SSEC | TriQuint Semiconductor |
| Huawei Technologies Co. Ltd. | Twinmos Technologies |
| Hynix Semiconductor America Inc. | Tyco Electronics |
| Hytek Microsystems Inc. | U.S. Army |
| I/O Data Device Inc. | Ubicom |
| Ibiden USA Corporation | Unigen Corporation |
| IBM Corporation | Unisys Corporation |
| IceFyre Semiconductor Inc. | United Test & Assembly Center |
| Infineon Technologies | United Test Center Inc. |
| Inphi Corporation | Universal Networking Machines |
| Integrated Circuit Systems | Vanguard International Semiconductor |
| Integrated Device Technology | Ventura Technology Corp. |
| | VIA Technologies Inc. |



Micron Technology Inc. et al.
Ex. 1017, p. 186

| | |
|---|---|
| Integrated Silicon Solution Inc.<br>Intel Corporation<br>International Rectifier Company<br>Intersil Corporation<br>ITW/Camtex<br>IXYS Corporation<br>JAE Electronics Inc.<br>Kentron Technologies<br>Kingmax Semiconductor Inc.<br>Kingston Technology Company Inc.<br>King Tiger Technology Inc.<br>Kostat Incorporated<br>Lansdale Semiconductor Inc.<br>LeCroy Corporation<br>Legacy Electronics Inc.<br>Linear Technology Corporation<br>Littelfuse Inc.<br>LSI Logic Corporation<br>M/A-Com Inc.<br>M.S. Kennedy Corporation<br>Macronix Int'l Co. Ltd.<br>Manufacturing Technology Inc. | Viking Interworks<br>Virtium Technology Inc.<br>Vishay Siliconix<br>Wells-CTI<br>White Electronic Designs<br>Winbond Electronics<br>Wintec Industries Inc.<br>Xilinx Inc.<br>Yamaichi Electronics |

Top

JEDEC Home: http://www.jedec.org



Micron Technology Inc. et al.
Ex. 1017, p. 187