IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC. Plaintiff, v. **SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC.** Defendants.	Civil Action No.2:21-cv-463 JURY TRIAL DEMANDED

COMPLAINT

1. Plaintiff Netlist, Inc. ("Netlist"), by its undersigned counsel, for its Complaint against defendants Samsung Electronics Co., Ltd. ("SEC"), Samsung Electronics America, Inc. ("SEA"), and Samsung Semiconductor, Inc. ("SSI") (collectively, "Samsung" or "Defendants"), states as follows, with knowledge as to its own acts, and on information and belief as to the acts of others:

2. This action involves three of Netlist's patents: U.S. Patent Nos. 10,860,506 (the "'506 Patent," Ex. 1), 10,949,339 (the "'339 Patent," Ex. 2), and 11,016,918 (the "'918 Patent," Ex. 3) (collectively, the "Patents-in-Suit").

I. THE PARTIES

3. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Drive, Suite 100, Irvine, CA 92617.

4. On information and belief, SEC is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129 Samsung-ro, Yeongtong-gu, Suwon, Gyeonggi, 16677, Republic of Korea. On information and belief, SEC is the worldwide parent corporation for SEA and SSI, and is responsible for the infringing activities identified in this complaint. On information and belief, SEC's Device Solutions division is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, SEC is also involved in the design, manufacture, and provision of products sold by SEA.

5. On information and belief, SEA is a corporation organized and existing under the laws of the State of New York. On information and belief, SEA, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. Defendant SEA maintains facilities at 6625 Excellence Way, Plano, Texas 75023. SEA may be served with process through its registered agent for service in Texas: CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, Texas 75201. SEA is a wholly owned subsidiary of SEC.

6. On information and belief, SSI is a corporation organized and existing under the laws of the State of California. On information and belief, SSI, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined

below. Defendant SSI maintains facilities at 6625 Excellence Way, Plano, Texas 75023. Defendant SSI may be served with process through its registered agent National Registered Agents, Inc., 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136. On information and belief, SSI is a wholly owned subsidiary of SEA.

7. On information and belief, Defendants have used, sold or offered to sell products and services, including the Accused Instrumentalities, in this judicial district.

II. JURISDICTION AND VENUE

8. Subject matter jurisdiction is based on 28 U.S.C. § 1338, in that this action arises under federal statute, the patent laws of the United States (35 U.S.C. §§ 1, *et seq.*).

9. Each Defendant is subject to this Court's personal jurisdiction consistent with the principles of due process and/or the Texas Long Arm Statute.

10. Personal jurisdiction exists generally over the Defendants because each Defendant has sufficient minimum contacts and/or has engaged in continuous and systematic activities in the forum as a result of business conducted within the State of Texas and the Eastern District of Texas. Personal jurisdiction also exists over each Defendant because each, directly or through subsidiaries, makes, uses, sells, offers for sale, imports, advertises, makes available, and/or markets products within the State of Texas and the Eastern District of Texas that infringe one or more claims of the Patents-in-Suit. Further, on information and belief, Defendants have placed or contributed to placing infringing products into the stream of commerce knowing or understanding that such products would be sold and used in the United States, including in this District.

11. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b). For example, SEC maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district. As another example, SEA maintains a regular and established place of

business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district. Venue is also proper for SSI because it maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district.

12. Defendants have not contested proper venue in this District. *See, e.g.*, Answer at ¶ 10, *Arbor Global Strategies LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-333, Dkt. 43 (E.D. Tex. Apr. 27, 2020); Answer at ¶ 29, *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-347, Dkt. 14 (E.D. Tex. Feb. 12, 2020).

III. FACTUAL ALLEGATIONS

Background

13. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

14. Netlist has a long history of being the first to market with disruptive new products such as the first load-reduced dual in-line memory module ("LR-DIMM"), HyperCloud®, based on Netlist's distributed buffer architecture later adopted by the industry for DDR4 LRDIMM. Netlist was also the first to bring NAND flash to the memory channel with its NVvault® NVDIMM. These innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate (DDR) technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory.

15. Generally speaking, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard.

16. Memory modules are designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications. The structure, function, and operation of memory modules is defined, specified, and standardized by the JEDEC Solid State Technology Association ("JEDEC"), the standard-setting body for the microelectronics industry. Memory modules are typically characterized by, among other things, the generation of DRAM on the module (*e.g.*, DDR5, DDR4, DDR3) and the type of module (*e.g.*, RDIMM, LRDIMM).

The Asserted Netlist Patents

The '506 Patent

17. The '506 Patent is entitled "Memory Module With Timing-Controlled Data Buffering." Netlist owns the '506 Patent by assignment from the listed inventors Hyun Lee and Jayesh R. Bhakta. The '506 Patent was filed as Application No. 16/391,151 on April 22, 2019, issued as a patent on December 8, 2020, and claims priority to, among others, a utility application filed on July 27, 2013 (No. 13/952,599) and a provisional application filed on July 27, 2012 (No. 61/676,883).

18. Samsung had knowledge of the '506 Patent no later than August 2, 2021 via its access to Netlist's patent portfolio docket.

19. As described in the '506 Patent, in conventional memory modules, the "distribution of control signals and a control clock signal in the memory module is subject to strict constraints"

to ensure that memory devices on the memory module can be properly accessed. Ex. 1 at 2:16-17. For example, in some conventional memory modules, "control wires are routed so there is an equal length to each memory component, in order to eliminate variation of the timing of the control signals and the control clock signal between different memory devices in the memory modules." *Id.* at 2:20-24. But as noted in the '506 Patent, "[t]he balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections." *Id.* at 2:24-27. In yet other conventional memory systems, the memory controller includes mechanisms for compensating for unbalanced wire lengths on the memory module. *Id.* at 2:30-32. However, with increasing memory operating speed and memory density "such leveling mechanisms are also insufficient to ensure proper timing of the control and/or data signals received and/or transmitted by the memory modules." *Id.* at 2:32-36.

20. The '506 Patent discloses a memory module operable in a memory system with a memory controller that includes memory devices, a module control circuit, and a plurality of buffer circuits coupled between respective sets of data signal lines in a data bus and respective sets of the memory devices. As summarized in the Abstract, "[e]ach respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal. Each respective buffer circuit includes a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals." *Id.*, Abstract.

21. The buffer circuits (118, highlighted below) are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective groups of memory devices as illustrated in the exemplary configuration of Figure 2A.

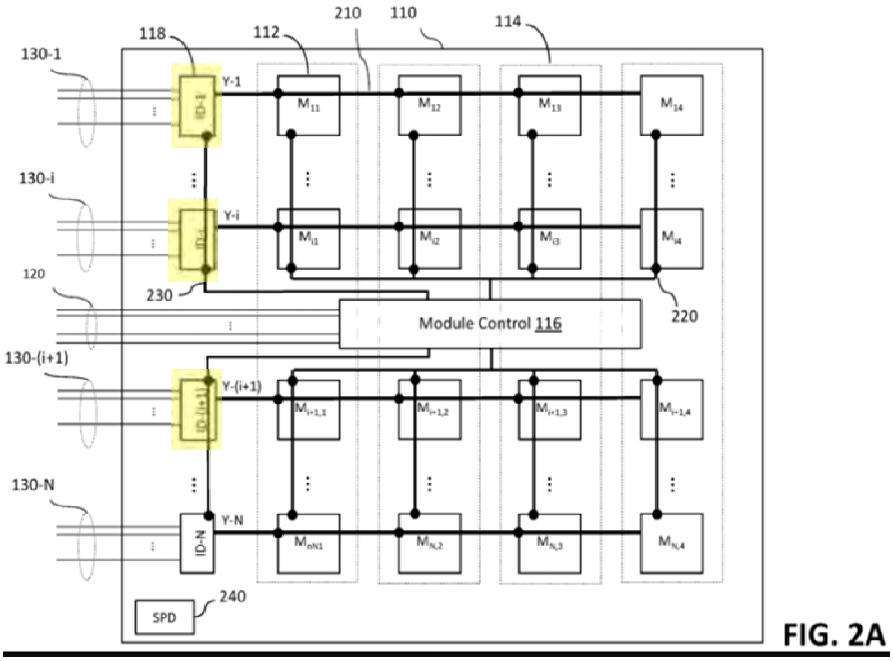


FIG. 2A

'506 Patent, Figure 2A. However, because the buffer circuits—or "isolation devices"—are distributed across the memory module, at high speeds of operation, the same set of module control signals may reach different buffer circuits at different times across one cycle of the system clock. *Id.* at 9:51-62 ("Because the isolation devices 118 are distributed across the memory module 110, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines 230 from the module control device 116 to the farthest positioned isolation devices 118, such as isolation device ID-1 and isolation device ID-(n−1) in the exemplary configuration shown in FIG. 2."). The '506 Patent discloses an embodiment wherein "each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit 116 and a time when a write strobe or write data signal is received from the MCH 101. This time interval is used during a subsequent read operation to time the transmission of read data to the MCH 101, such that the read data follows a read command by a read latency value associated with the system 100." *Id.* at 10:11-21.

The '339 Patent

22. The '339 Patent is entitled "Memory Module With Controlled Byte-Wise Buffers." Netlist owns the '339 Patent by assignment from the listed inventors Hyun Lee and Jayesh R. Bhakta. The '339 Patent was filed as Application No. 15/470,856 on March 27, 2017, issued as a patent on March 16, 2021, and claims priority to U.S. Patent Application No. 12/504,131 filed on July 16, 2009, U.S. Patent Application No. 12/761,179 filed on April 15, 2010 and U.S. Application No. 13/970,606 filed on August 20, 2013.

23. Samsung had knowledge of the '339 Patent no later than August 2, 2021 via its access to Netlist's patent portfolio docket.

24. As described in the '339 Patent, in optimizing performance of memory subsystems (e.g. memory modules) "consideration is always given to memory density, power dissipation (or thermal dissipation, speed, and cost." Ex. 2 at 2:5-7. The '339 Patent further explains that "[g]enerally, these attributes are not orthogonal to each other, meaning that optimizing one attribute may detrimentally affect another attribute. For example, increasing memory density typically causes higher power dissipation, slower operational speed, and higher costs." *Id.* at 2:7-12. The '339 Patent is generally directed to a memory module optimized to reduce the load experienced by a system memory controller via the use of configurable data transmission circuits.

25. The '339 Patent discloses a memory module configured to communicate with a memory controller that includes DDR DRAM devices arranged in multiple ranks each of the same width as the memory module, and a module controller configured to receive and register input control signals for a read or write operation from the memory controller and to output registered address and control signals. As summarized in the Abstract, "[t]he registered address and control signals selects one of the multiple ranks to perform the read or write operation. The module controller further outputs a set of module control signals in response to the input address and

control signals. The memory module further comprises a plurality of byte-wise buffers controlled by the set of module control signals to actively drive respective byte-wise sections of each data signal associated with the read or write operation between the memory controller and the selected rank." *Id.*, Abstract.

26. Figure 3A illustrates an example of a memory subsystem consistent with embodiments disclosed in the '339 patent.

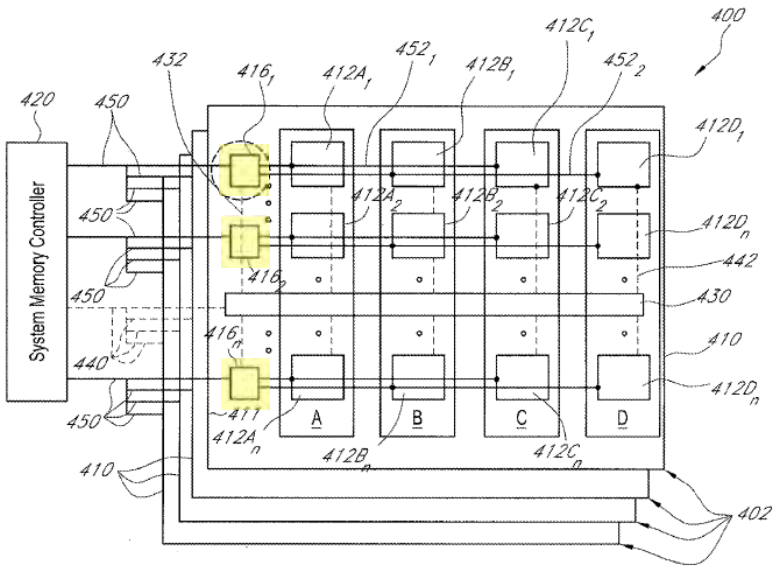


FIG. 3A

'339 Patent, Figure 3A. As shown above, Figure 3A depicts a memory subsystem 400 including memory modules 402 comprising memory devices 412, data transmission circuits 416 (highlighted above), and module control circuits 430. The data transmission circuits 416 operate to reduce the load experienced by the memory controller 420 to improve performance of a read or write operation. *Id.* at 17:14-44 ("Referring again to FIG. 3A, when the memory controller 420 executes read or write operations, each specific operation is targeted to a specific one of the ranks A, B, C, and D of a specific memory module 402. The data transmission circuit 416 on the specifically

targeted one of the memory modules 402 functions as a bidirectional repeater/multiplexor, such that it drives the data signal when connecting from the system memory controller 420 to the memory devices 412. The other data transmission circuits 416 on the remaining memory modules 402 are disabled for the specific operation. . . . Thus, the memory controller 420, when there are four four-rank memory modules, sees four load-reducing switching circuit loads, instead of sixteen memory device loads. The reduced load on the memory controller 420 enhances the performance and reduces the power requirements of the memory system . . . .”). In certain embodiments, “the data transmission circuit 416 comprises or functions as a byte-wise buffer. In certain such embodiments, each of the one or more data transmission circuits 416 has the same bit width as does the associated memory devices 412 per rank to which the data transmission circuit 416 is operatively coupled.” *Id.* at 13:31-36.

The ’918 Patent

27. The ’918 Patent is entitled “Flash-DRAM Hybrid Memory Module.” Netlist owns the ’918 Patent by assignment from the listed inventors Chi-She Chen, Jeffrey C. Solomon , Scott H. Milton, and Jayesh Bhakta. The ’918 Patent was filed as Application No. 17/138,766 on December 30, 2020, issued as a patent on May 25, 2021, and claims priority to, among others, U.S. Application No. 13,559,476 filed on July 26, 2012, U.S. Application No. 12/240,916 filed on September 29, 2008, and U.S. Application No. 12/131,873 filed on June 2, 2008 as well as to two provisional applications, filed on June 1, 2007 (No. 60/941,586) and July 28, 2011 (No. 61/512,871).

28. Samsung had knowledge of the ’918 Patent no later than August 2, 2021 via its access to Netlist’s patent portfolio docket via notice of U.S. Patent Application No. 12/240,916 and U.S. Patent Application No. 12/131,873 on August 2, 2021.

Micron Technology Inc. et al.
Ex. 1044, p. 10

29. As summarized in the Abstract, the '918 Patent discloses a memory module that includes a printed circuit board with an interface that couples it to a host system for provision of power, data, address and control signals, and additionally features "[f]irst, second, and third buck converters [that] receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage." Ex. 3, Abstract.

30. The '918 Patent discloses, *inter alia*, a power module that provides power to various components of the memory system as depicted in Figure 16, shown below.

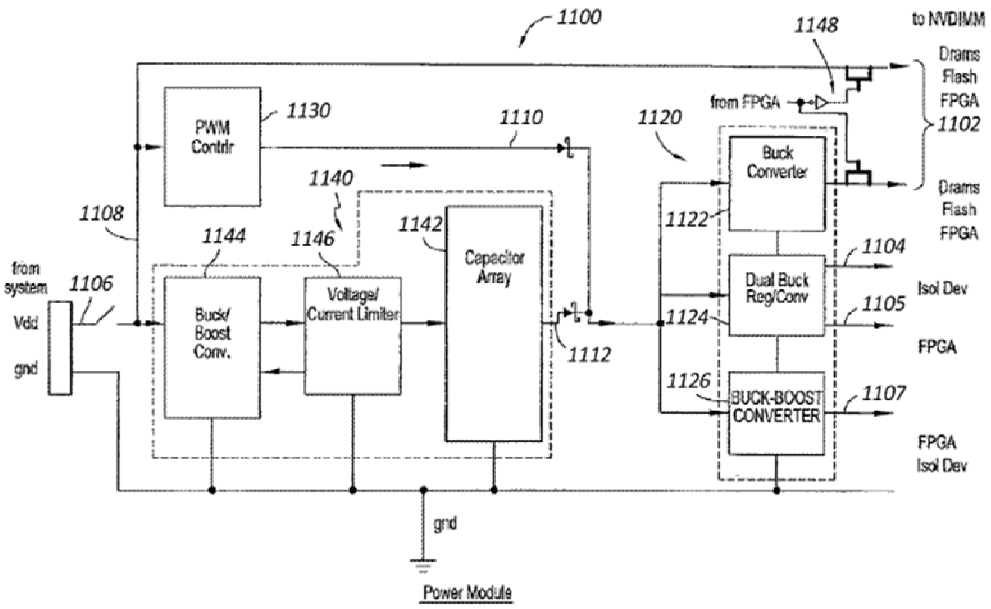


FIG. 16

31. The '918 Patent explains that "[t]he power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems

1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller." *Id.* at 28:3-15. "The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters." *Id.* at 29:18-19.

32. Relatedly, on December 10, 2021, the United States Patent and Trademark Office issued a Notice of Allowance for the pending claims of Application No. 17/138,019, a continuation of the '918 Patent. *See* Ex. 4 (allowed claims of App. No. 17/138,019). Netlist intends to assert the allowed claims of App. No. 17/138,019 upon issuance against Samsung.

33. The inventions of the '918 Patent and App. No. 17/138,019 provide for the effective operation of DDR5 memory modules, by enabling, among other benefits, greater power efficiency than previous generations of DDR technology. The DDR5 standard is characterized by the use of an on-module power management system. Samsung itself notes "[t]he on-DIMM PMIC further boosts power management efficiency and power supply stability." Ex. 12 at 5.

Samsung's Infringing Activities

34. Samsung is a global technology company that manufactures semiconductor memory products such as DRAM, NAND Flash and MCP (Multi-Chip Package). Samsung develops, manufactures, sells and imports into the United States memory components and memory modules designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications.

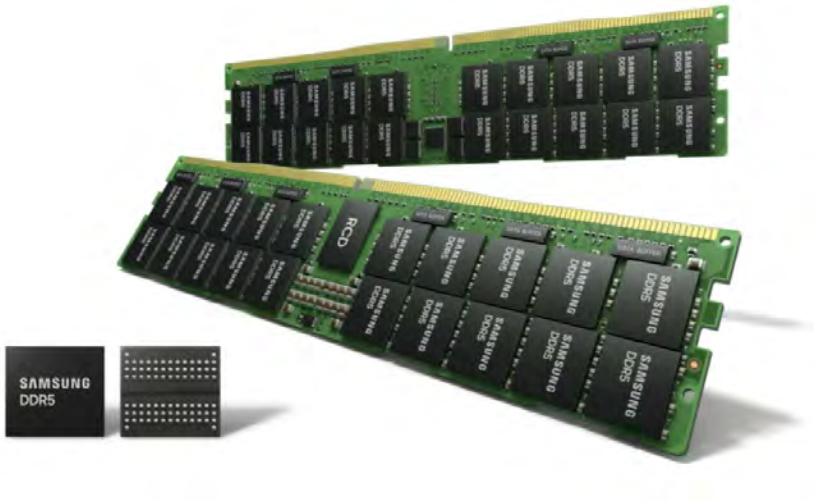
Micron Technology Inc. et al.
Ex. 1044, p. 12

35. Samsung was a licensee of Netlist until July 15, 2020. *See Netlist Inc. v. Samsung Elecs. Co., Ltd.*, No. 20-cv-993, Dkt. 186 at 20-21 (C.D. Cal. Oct. 14, 2021). Immediately after Samsung's license was deemed terminated, Samsung filed an improper declaratory judgment action in the District of Delaware concerning unrelated patents directed at different aspects of memory module technology than the patents in the present suit. *See Samsung Elecs. Co., Ltd. et al v. Netlist, Inc.*, No. 21-cv-1453, Dkt. 1 (D. Del. Oct. 15, 2021). Netlist has moved to dismiss each count of Samsung's declaratory judgment complaint in Delaware.

36. On information and belief, Samsung makes, uses, sells, offers to sell, and/or imports within this District and elsewhere in the United States, without authority, infringing DDR4 LRDIMMs, DDR5 LRDIMMs, DDR5 RDIMMs, DDR5 SODIMMs, DDR5 UDIMMs, and other products that have materially the same structures and designs in relevant parts (the "Accused Instrumentalities").

37. The accused DDR4 LRDIMMs include, without limitation, any Samsung DDR4 LRDIMM products made, sold, used and/or imported into the United States by Samsung. By way of non-limiting example, the accused DDR4 LRDIMMs products include, Samsung products having the following part numbers: M386A4K40BB0-CRC, M386A8K40BM1-CRC, M386A8K40BM2-CTD, M386A8K40BMB-CRC, M386A8K40CM2-CRC, M386A8K40CM2-CTD, M386A8K40CM2-CVF, M386A8K40DM2-CTD, M386A8K40DM2-CVF, M386A8K40DM2-CWE, M386AAG40AM3-CWE, M386AAG40MM2-CVF, M386AAG40MMB-CVF, M386AAK40B40-CUC, M386AAK40B40-CWD, M386ABG40M50-CYF, M386ABG40M51-CAE, M386ABG40M5B-CYF. Further examples of Samsung's DDR4 LRDIMM products can be found via Samsung's module-selector web page. *See Module: Memory Modules For Extensive Use*, Samsung, *available at* https://www.samsung.com/semiconductor/dram/module.

38. As further example, the Accused Instrumentalities include, without limitation, any Samsung DDR5 LRDIMM and DDR5 RDIMM products made, sold, used and/or imported into the United States by Samsung that are JEDEC-standard compliant memory modules. By way of non-limiting example, the accused DDR5 LRDIMM and DDR5 RDIMM products include products marketed and publicized in an October 12, 2021 Samsung Press release, as shown below.



Ex. 5 at 1 (depiction of a Samsung DDR5 LRDIMM).



Id. at 3 (depiction of a Samsung DDR5 RDIMM).

IV. FIRST CLAIM FOR RELIEF – '506 PATENT

39. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

40. On information and belief, Samsung directly infringed and is currently infringing at least one claim of the '506 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example, and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '506 Patent.[1]

41. For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus. As an example, Samsung's website markets and contains datasheets for the accused DDR4 LRDIMMs.



LRDIMM

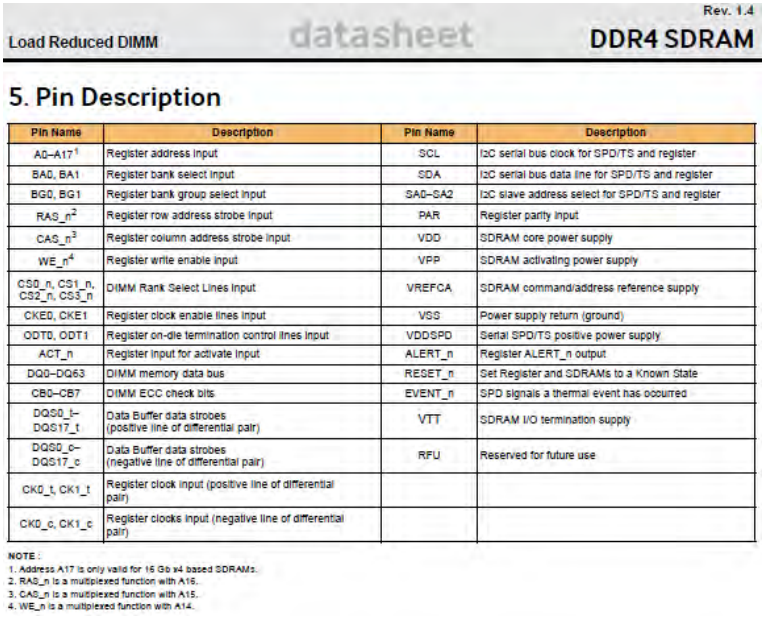
Load Reduced DIMM

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

42. Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM). Each LRDIMM includes "a register for enhancing clock, command and control signals" as well as data buffers for "[e]nhanced

[1] The theories set forth herein are based on Netlist's present understanding of the Samsung Accused Instrumentalities. Netlist reserves the right to supplement or amend these contentions as permitted by the Local Rules and any Orders of the Court as discovery progresses. Further, Netlist's contentions contain images and examples illustrating Netlist's infringement theories. As such, the images and examples are not intended, and should not be read, as narrowing or limiting the scope of these contentions.

data signal." *Id.* It communicates with a server's memory controller via control and address signal lines in a memory bus as well as a data bus. For example:



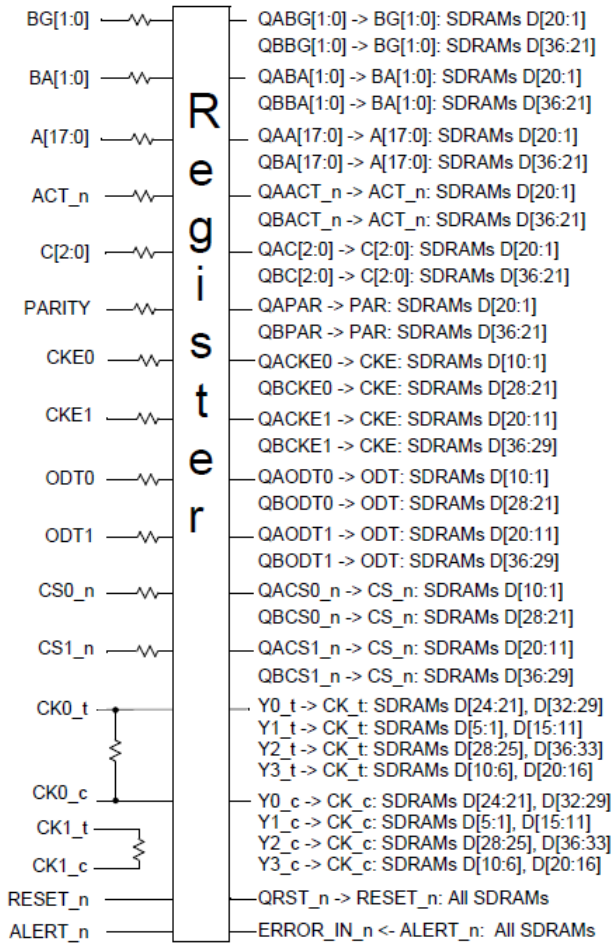
Load Reduced DIMM datasheet Rev. 1.4 DDR4 SDRAM

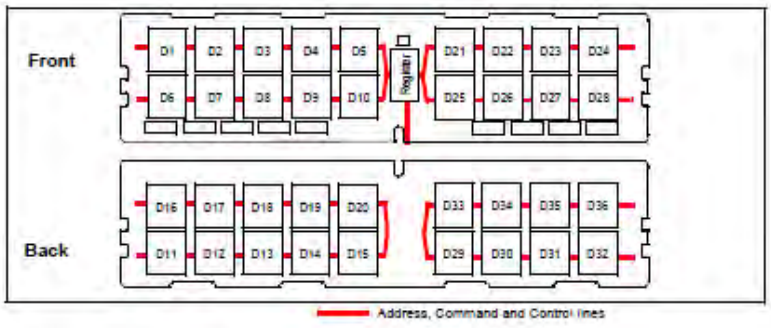
5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0–SA2	I2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input for activate input	ALERT_n	Register ALERT_n output
DQ0–DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
CK0_t, CK1_t	Register clock input (positive line of differential pair)		
CK0_c, CK1_c	Register clocks input (negative line of differential pair)		

NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Ex. 7 (M386AAK40B40 Datasheet) at 6.





NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

- 10 -

SAMSUNG

Id. at 10 (red lines in original).

43. The accused DDR4 LRDIMMs further each comprise a module board having edge connections to be coupled to respective signal lines in the memory bus, as illustrated in the examples below.



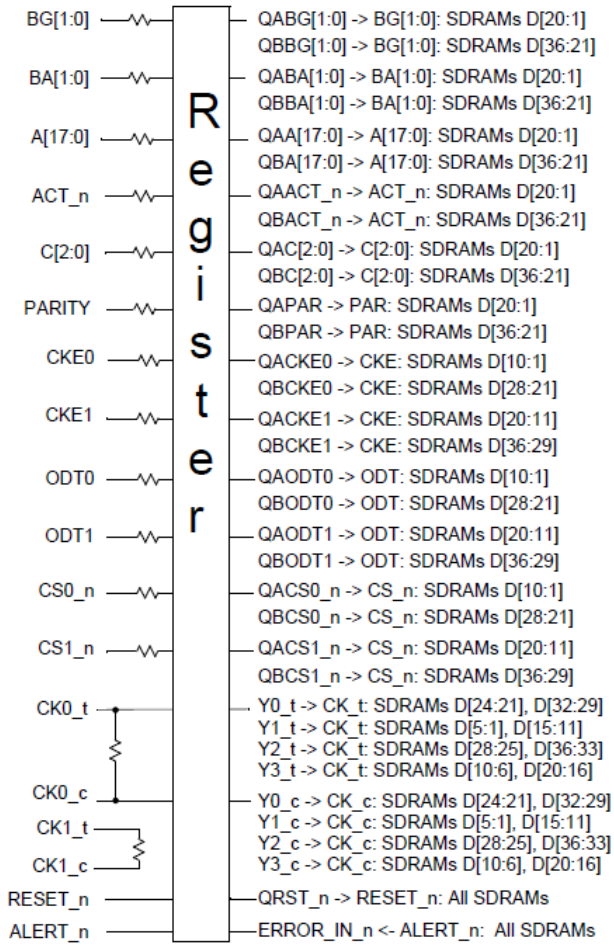
LRDIMM

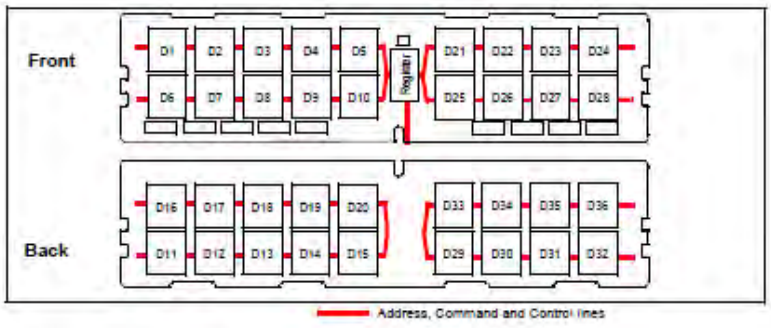
Load Reduced DIMM

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM); *see also* Ex. 7 (M386AAK40B40 Datasheet) at 42.

44. The accused DDR4 LRDIMMs further each comprise a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals, as illustrated in the example below.



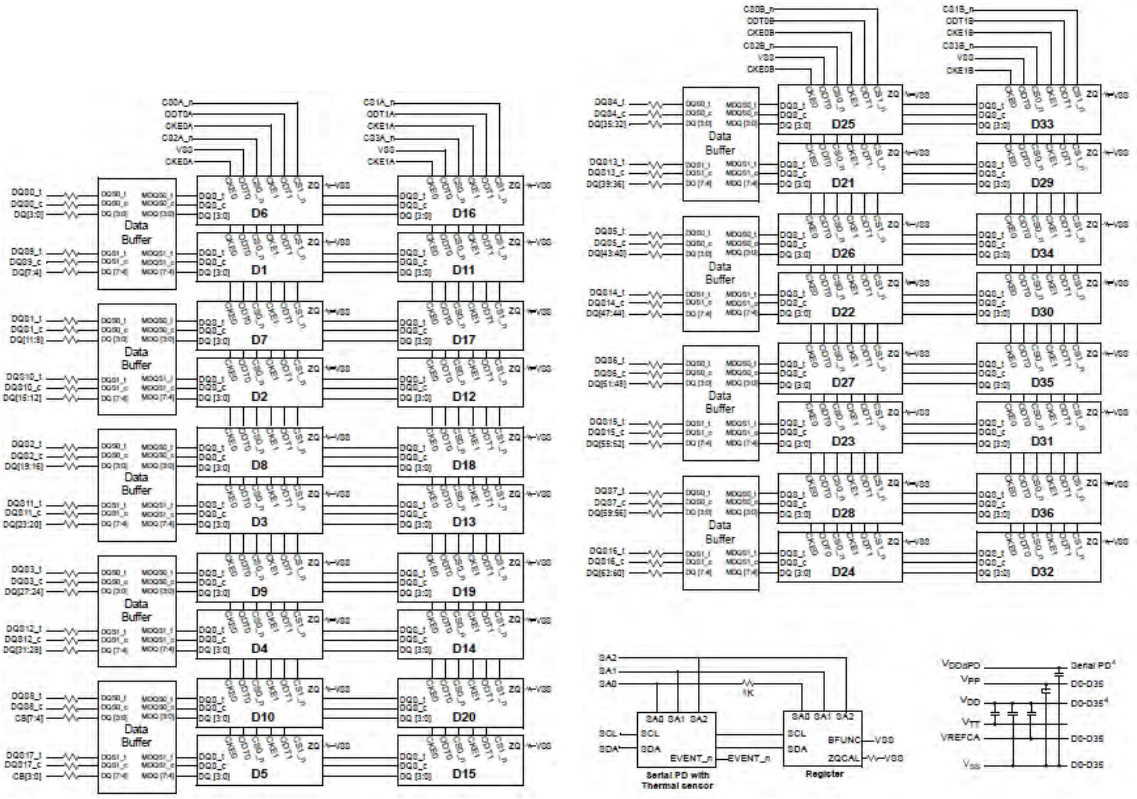


NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

- 10 -

SAMSUNG

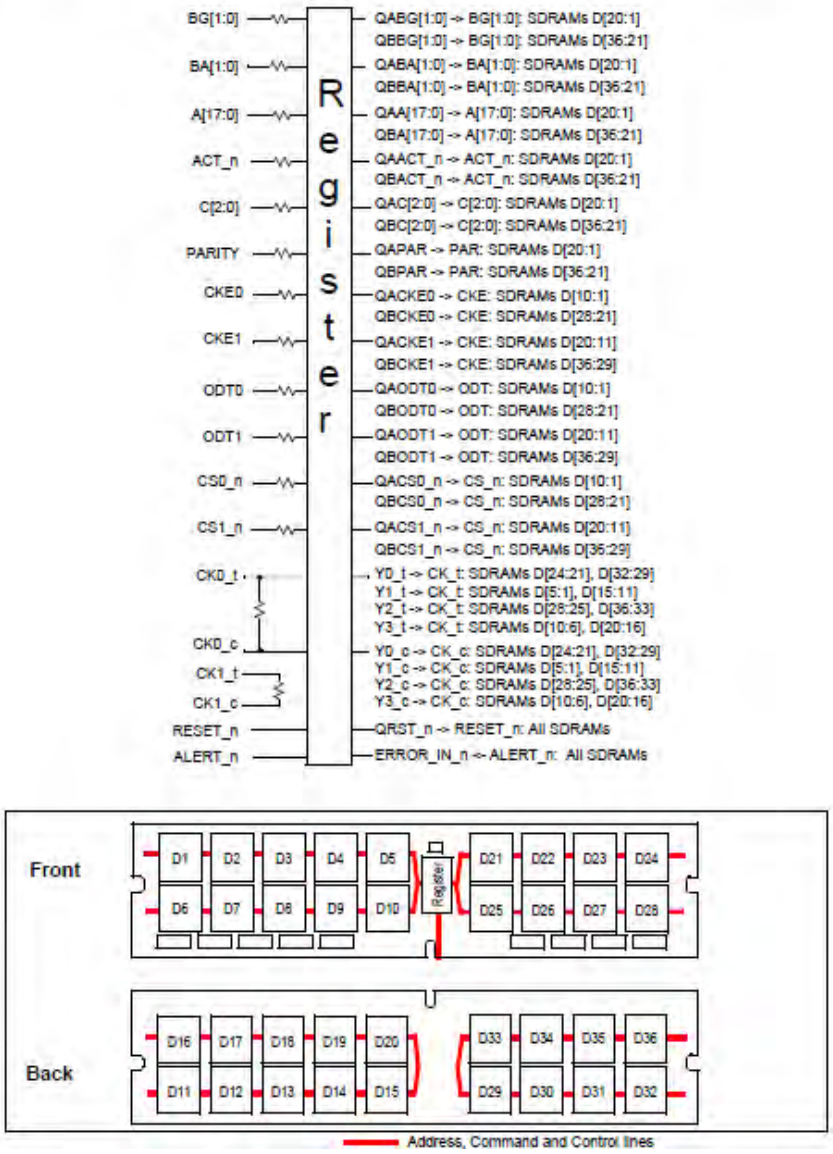
Ex. 7 (M386AAK40B40 Datasheet) at 10; *see also id.* at 42.



Id. at 11-12.

45. The accused DDR4 LRDIMMs also each include memory devices arranged in multiple ranks on the module board and coupled to the module control device (*e.g.*, RCD) via module C/A signal lines that conduct the registered C/A signals, as illustrated in the examples below.

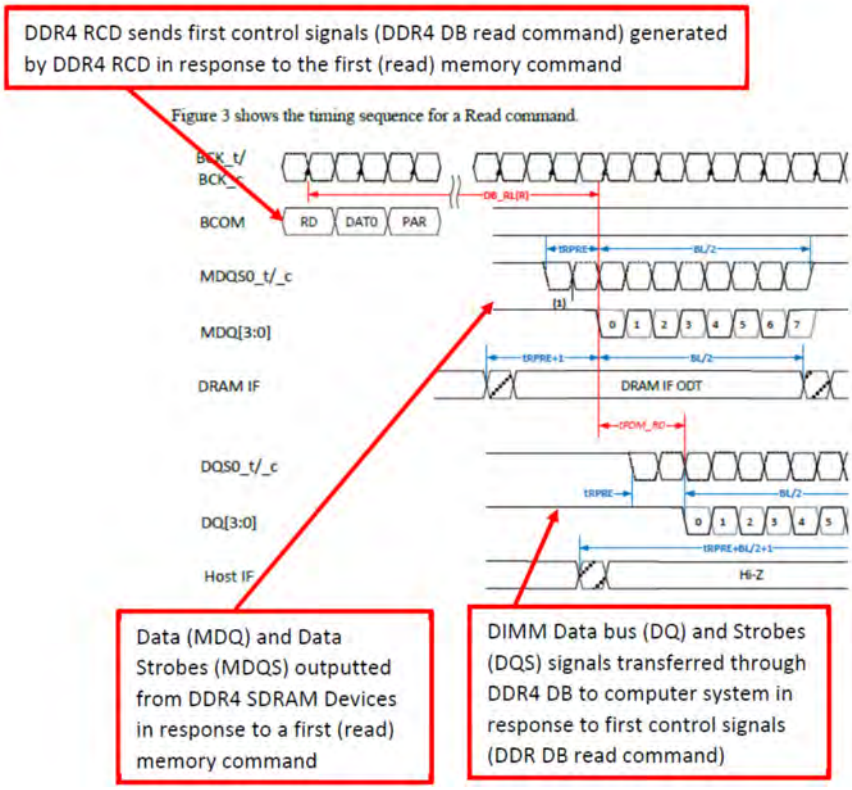
9.1 128GB, 16Gx72 Module
(Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAM



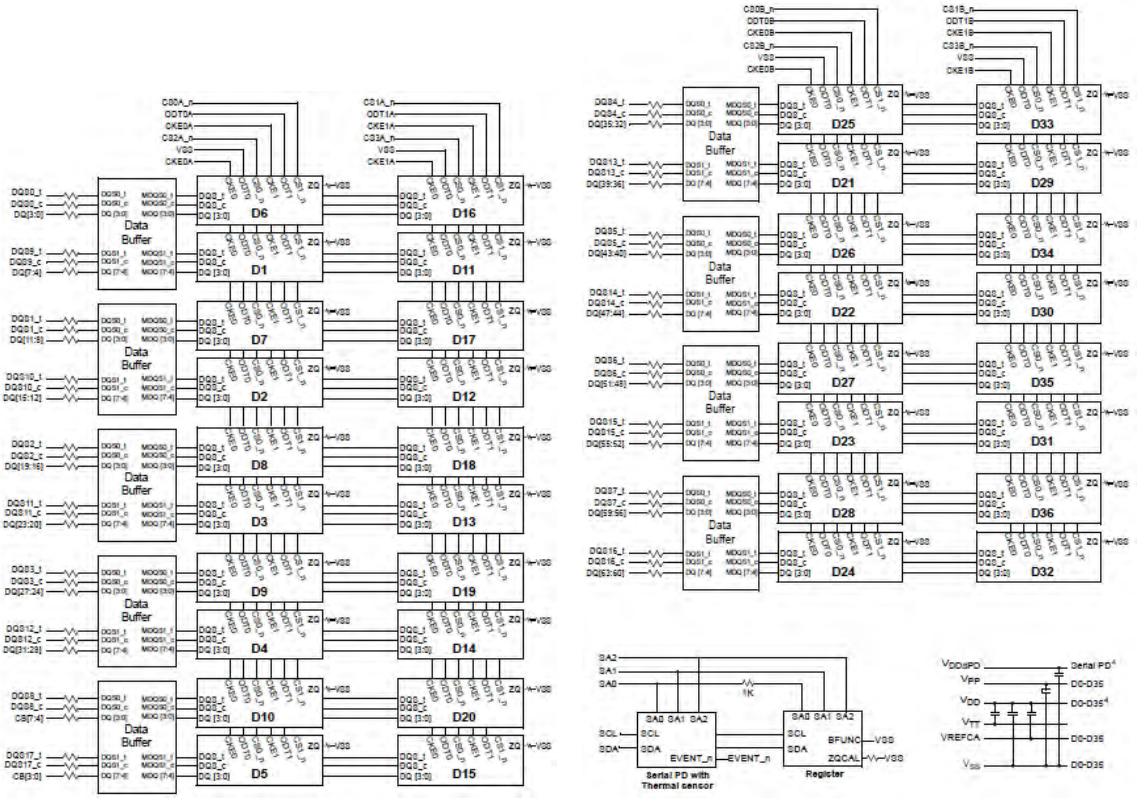
Id. at 10; *see also id.* at 42.

46. In each accused DDR4 LRDIMM's memory devices, the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a

first read strobe. For example, each accused DDR4 LRDIMM follows the timing sequence for a READ command shown below.



Ex. 9 (JEDEC JESD82-32A Standard), at 14 (annotated); *see also*, *e.g.*, Ex. 8 (M386A8K40BM1 Datasheet) at 11-12 (functional block for a representative product).

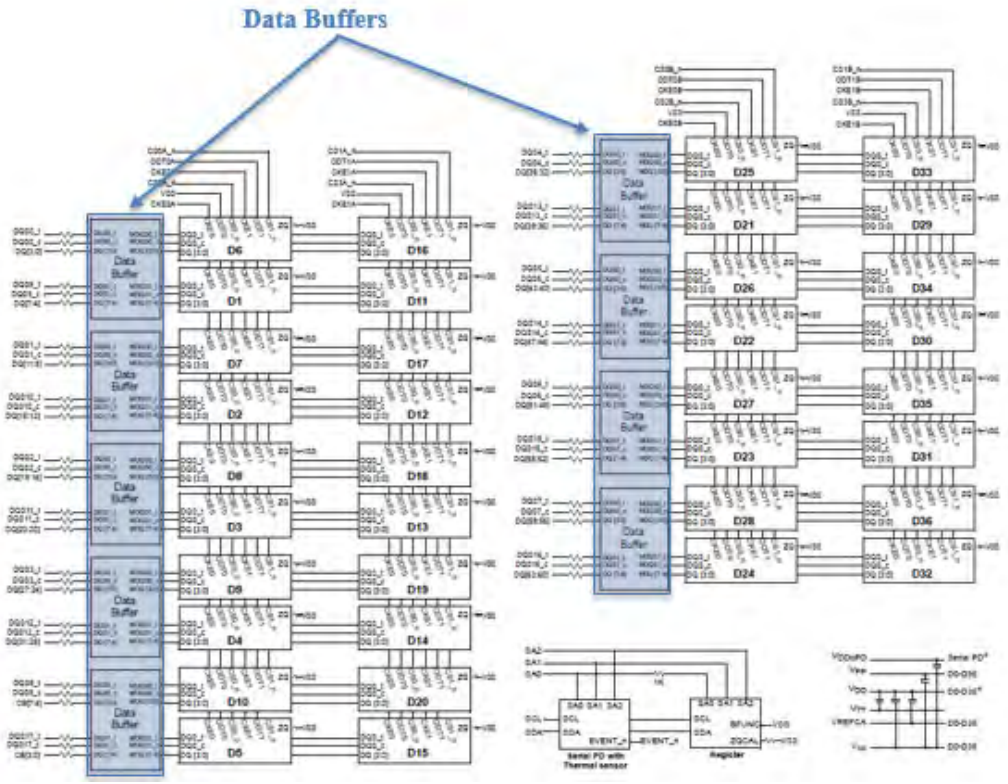


Ex. 8 (M386A8K40BM1 Datasheet) at 11-12.

47. The accused DDR4 LRDIMMs further each include data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, as illustrated below.

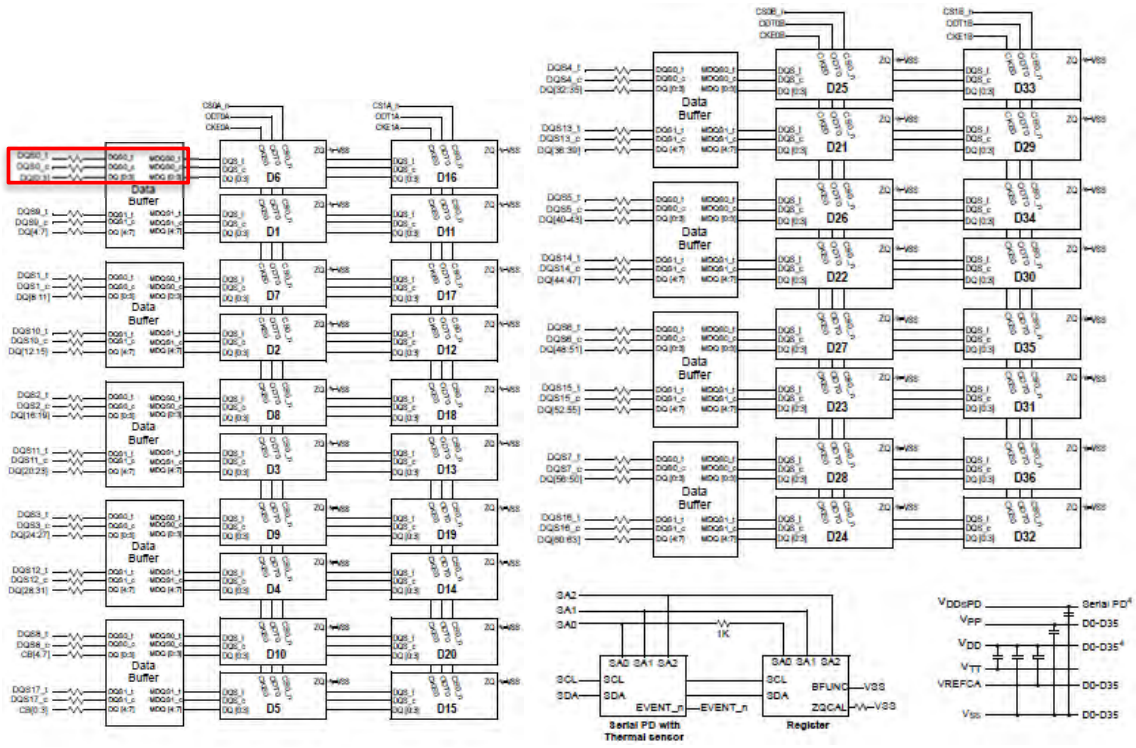


Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM).



Ex. 8 (M386A8K40BM1 Datasheet) at 11-12 (annotated to illustrate data buffers coupled between the plurality of 72-bit wide ranks and the 72-bit wide data bus).

48. In each accused DDR4 LRDIMM, a first data buffer on the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals: delay the first read strobe by a first predetermined amount to generate a first delayed read strobe; sample the first section of the read data using the first delayed read strobe; and transmit the first section of the read data to a first section of the data bus; wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations. For example, the strobes MDQSO_t and MDQSO_c are delayed by a variable delay circuitry and produce DQS0_t, DQS1_t and DQS0_c, DQS1_c. The predetermined amount of delay is determined based on training.



Ex. 7 (M386AAK40B40 Datasheet) at 11-12.

49. On information and belief, Samsung also indirectly infringes the '506 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information

and belief, Samsung has induced, and currently induces, the infringement of the '506 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM and other materially similar products that infringe the '506 Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

50. On information and belief, Samsung also indirectly infringes the '506 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers and end-users infringement of the '506 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM and other materially similar products that infringe the '506 Patent. On information and belief, the accused DDR4 LRDIMM products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM and other materially similar products would be covered by one or more claims of the '506 Patents. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM and other materially similar products infringes at least one claim of the '506 Patent.

51. Samsung's infringement of the '506 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the '506 Patent since at least August 2, 2021. Samsung's infringement of the '506 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement,

Micron Technology Inc. et al.
Ex. 1044, p. 26

and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

V. SECOND CLAIM FOR RELIEF – '339 PATENT

52. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

53. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '339 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '339 Patent.

54. For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a N-bit-wide memory module (*e.g.*, 72-bit-wide) mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide. For instance, each LRDIMM includes "a register for enhancing clock, command and control signals" as well as data buffers for "[e]nhanced data signal." Ex. 6 at 2. It communicates with a server's memory controller via control and address signal lines in a memory bus as well as a data bus.

Micron Technology Inc. et al.
Ex. 1044, p. 27



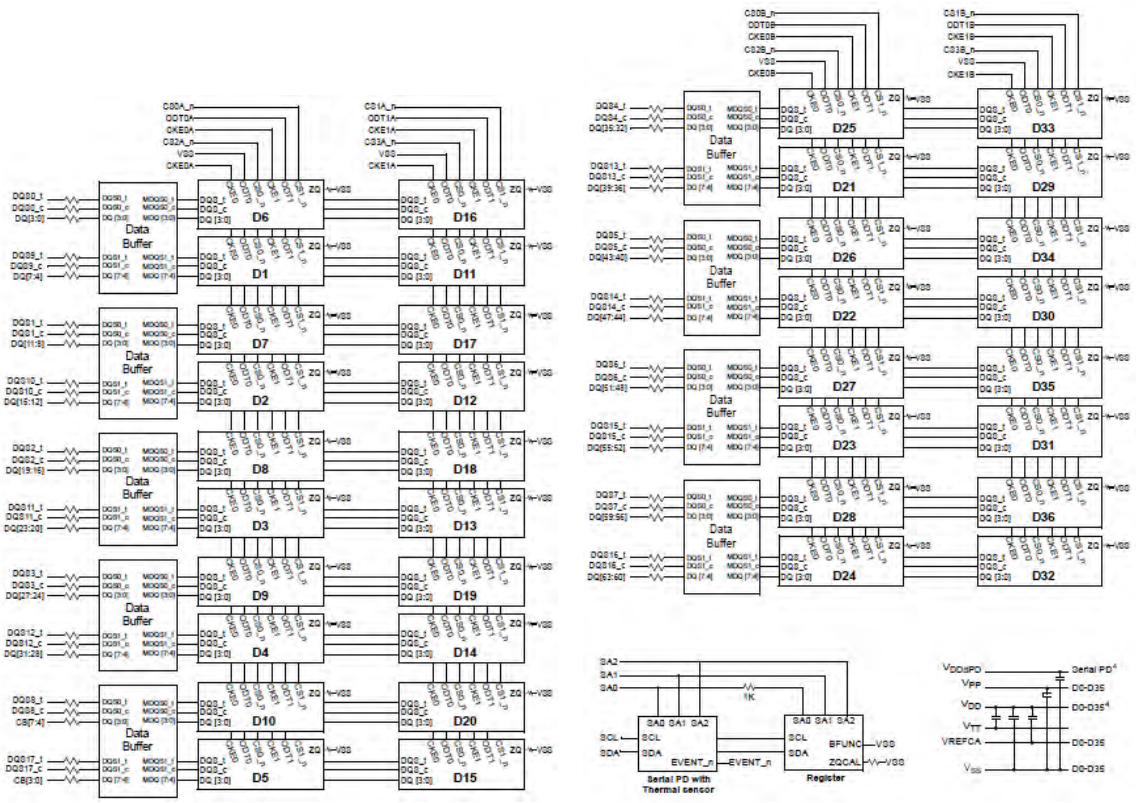
LRDIMM

Load Reduced DIMM

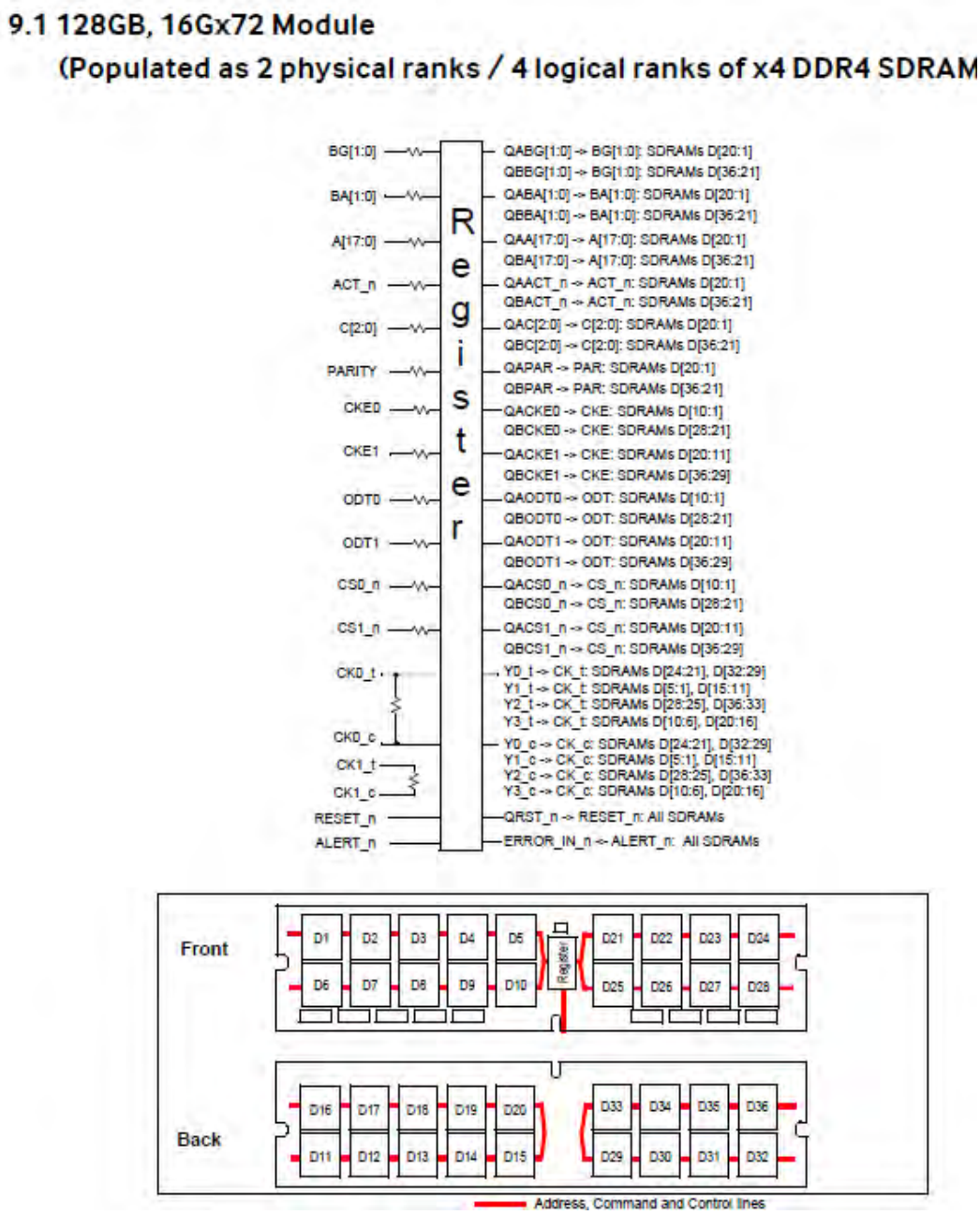
- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

Id. at 2 (depiction of a Samsung DDR4 LRDIMM).

55. In the configuration above, there are 9 sets of byte-wide data signal lines for a 72-bit wide data signal lines. For example:



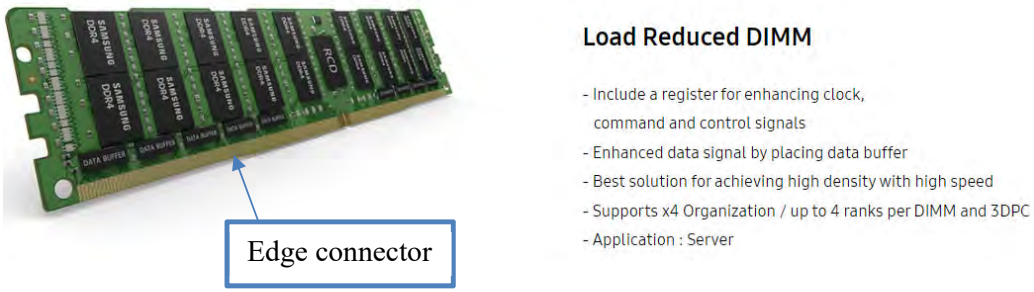
Ex. 8 (M386A8K40BM1 Datasheet) at 11-12.



Ex. 7 (M386AAK40B40 Datasheet) at 10; *see also id.* at 42.

56. The accused DDR4 LRDIMMs each comprise a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of

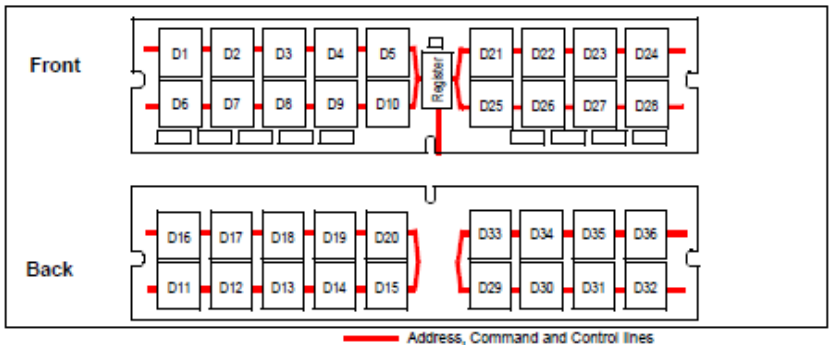
the PCB and configured to be releasably coupled to corresponding contacts of the memory socket. For example:



Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM).

57. The accused DDR4 LRDIMMs each include double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks. As shown above, each DDR4 LRDIMM module includes 9 ranks of memory devices.

58. The accused DDR4 LRDIMMs further comprise a module controller (such as a register clock driver, RCD) coupled to the PCB and operatively coupled to the DDR DRAM devices. For example:



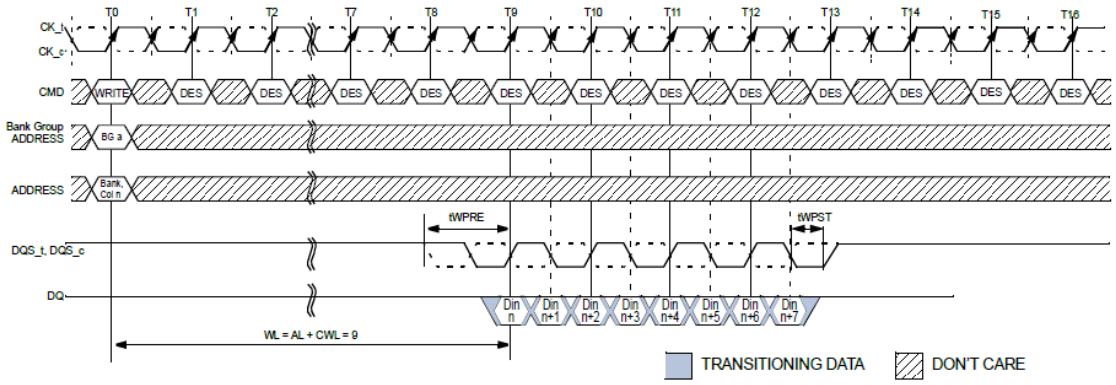
Ex. 7 (M386AAK40B40 Datasheet) at 10; *see also id.* at 42.

59. The module controller is configurable to receive from the memory controller via the address and control signal lines (e.g., red lines above) input address and control signals for a

memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation (when BCOM [3:0] is 1000) by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals. For example, a Write burst operation results in a burst of data and data strobes received by the DDR4 LRDIMM via the DQS/DQ pins of the memory bus, and to write the data via data buffers into a memory device as determined by input address and control signal (e.g., CS signal).

4.25.5 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.

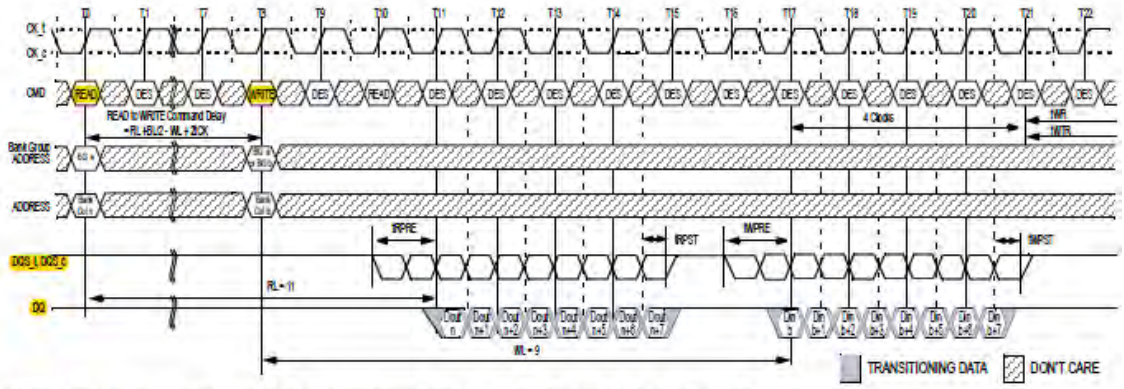


NOTE 1 BL = 8, WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
NOTE 2 DIN n = data-in to column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

Figure 128 — WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)

See, e.g., Ex. 10 (JESD79-4C DDR4 SDRAM Standard), at 122.

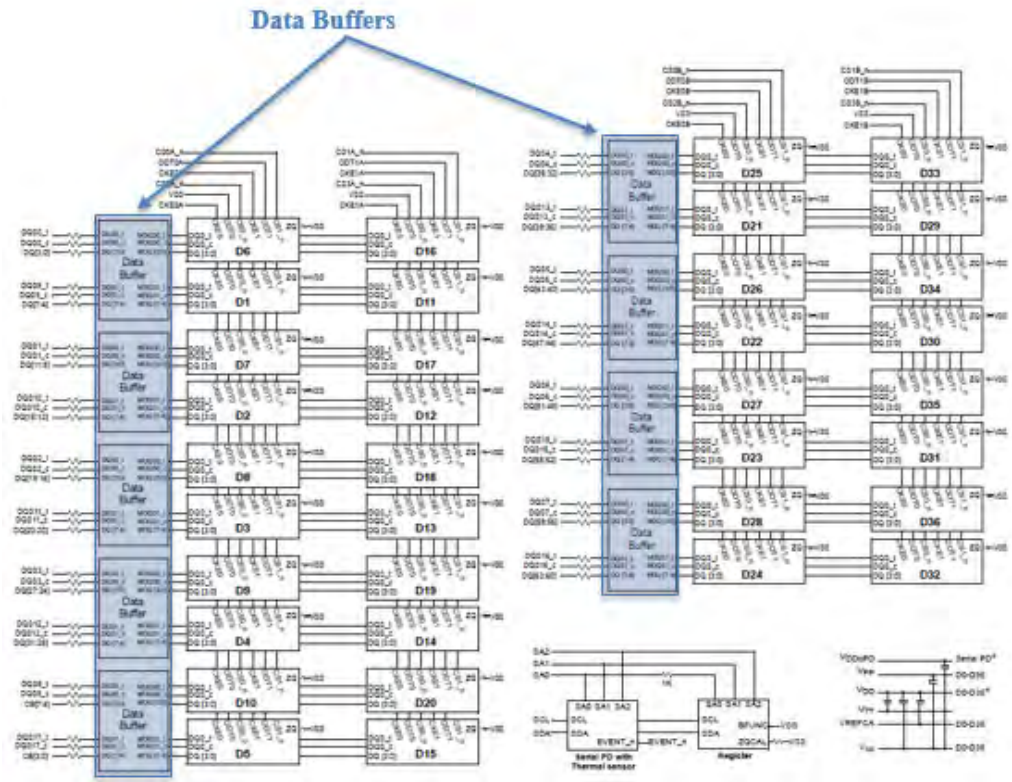
4.24.2 READ Burst Operation (cont'd)



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 98 — READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group

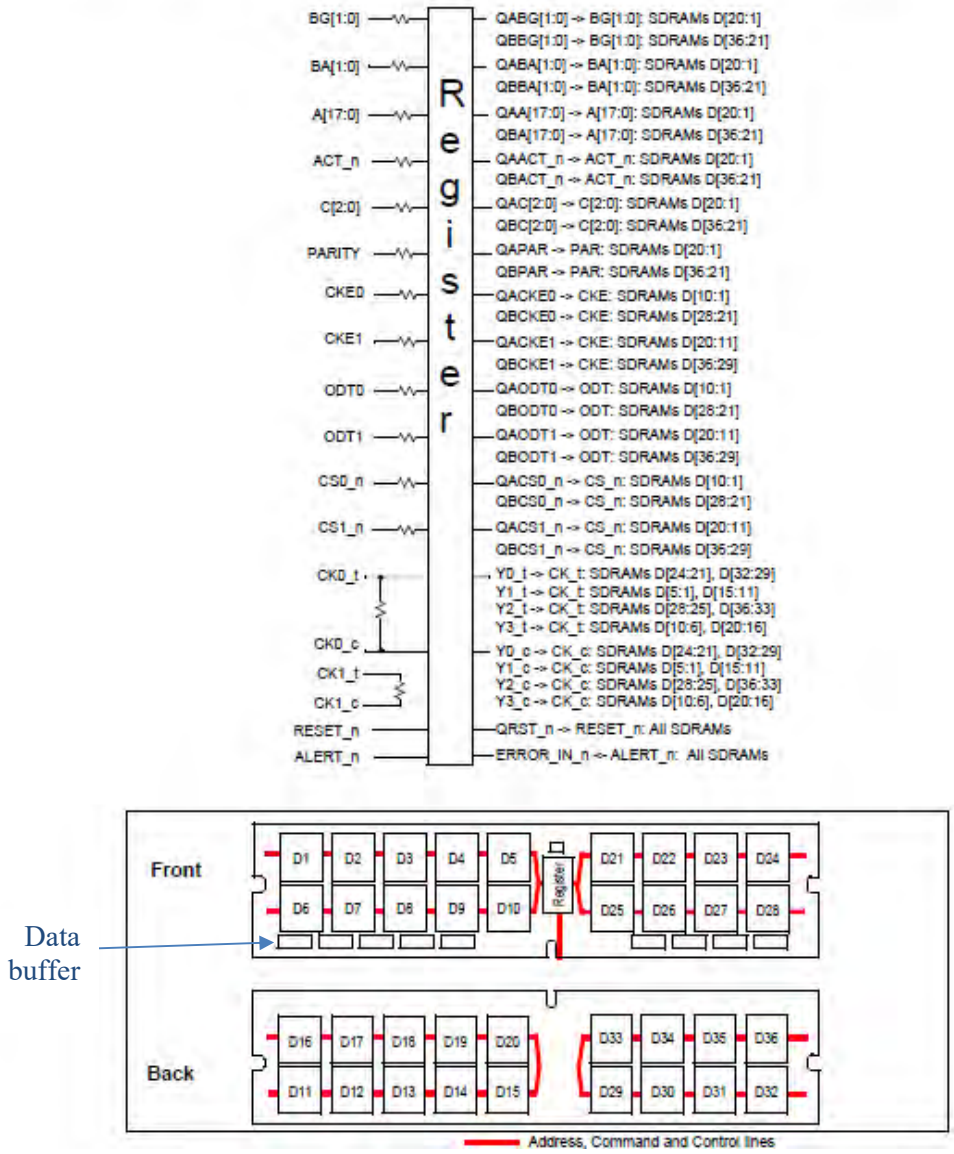
See, e.g., *id.* at 105 (annotated) (showing burst operations used by various ranks in the Accused Instrumentality).



Ex. 8 (M386A8K40BM1 Datasheet) at 11-12.

9.1 128GB, 16Gx72 Module

(Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAM



Ex. 7 (M386AAK40B40 Datasheet) at 10; *see also id.* at 42.

60. Further, as illustrated above and below, the accused DDR4 LRDIMMs also each comprise a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals, wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second

side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side, wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines.

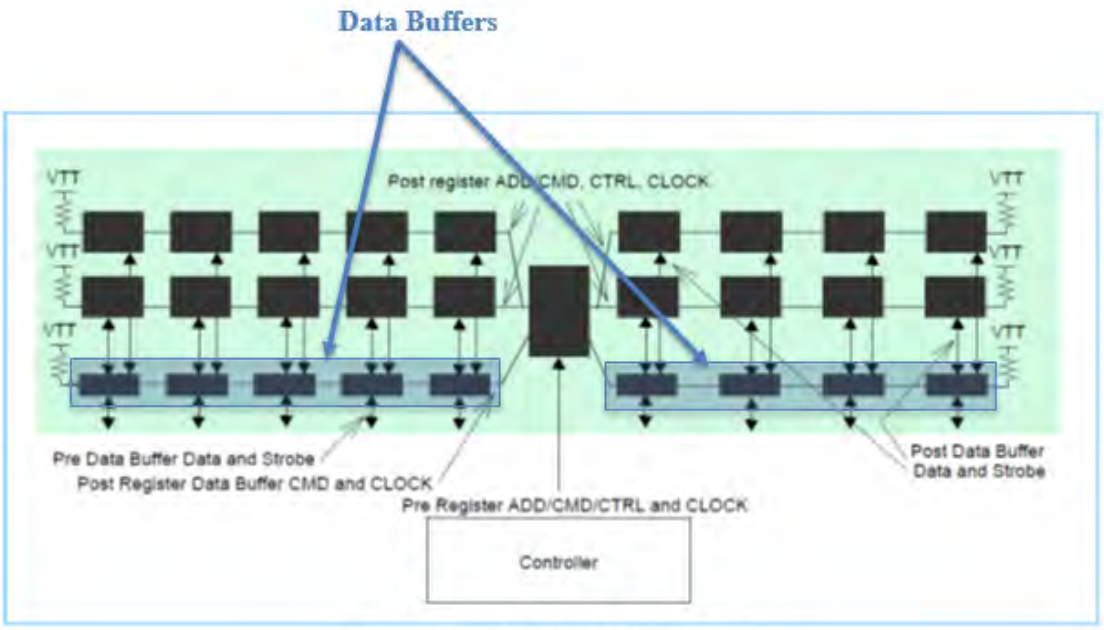


Figure 3 — LRDIMM Topologies

Ex. 11 (JEDEC 21C Standard), at 4.20.27-17.

61. In each of the accused DDR4 LRDIMMs, the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals and the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period. For example:

4.61 Logic Diagram

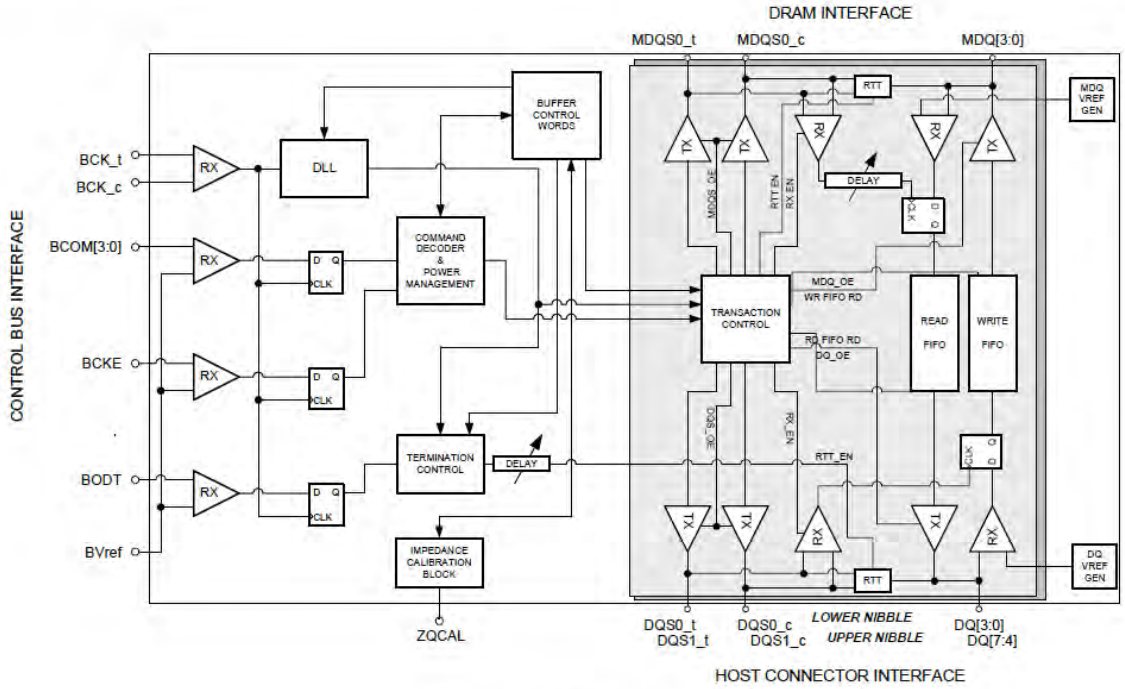
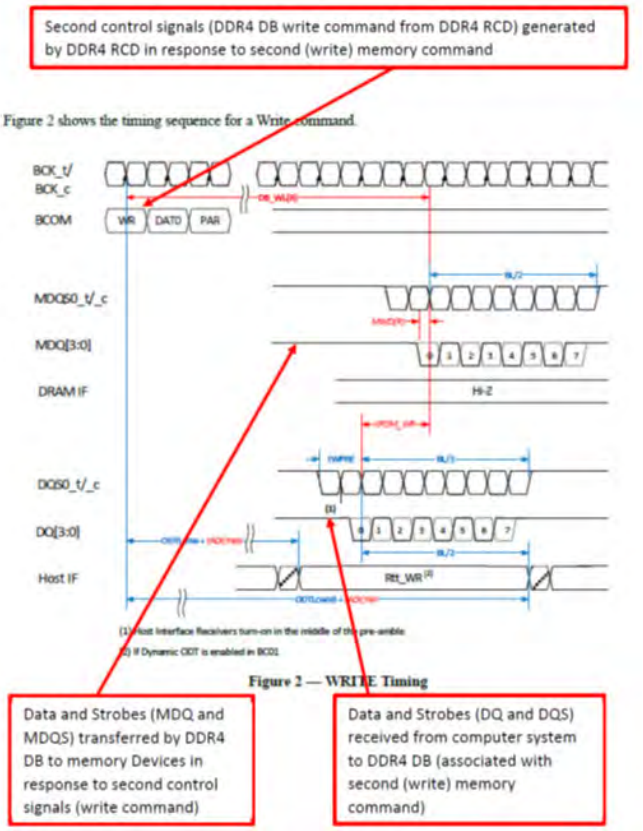


Figure 15 — Logic Diagram

Ex. 9 (JESD82-32A Standard), at 95.

62. The MDQ/MDQS driver can be disabled or enabled based on DRAM Interface MDQ Driver control word, such as DA[3:0] = 0xxx (enabled) and 1xxx (disabled).

63. In each of the accused DDR4 LRDIMMs, the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period. For example:



Id. at 13.

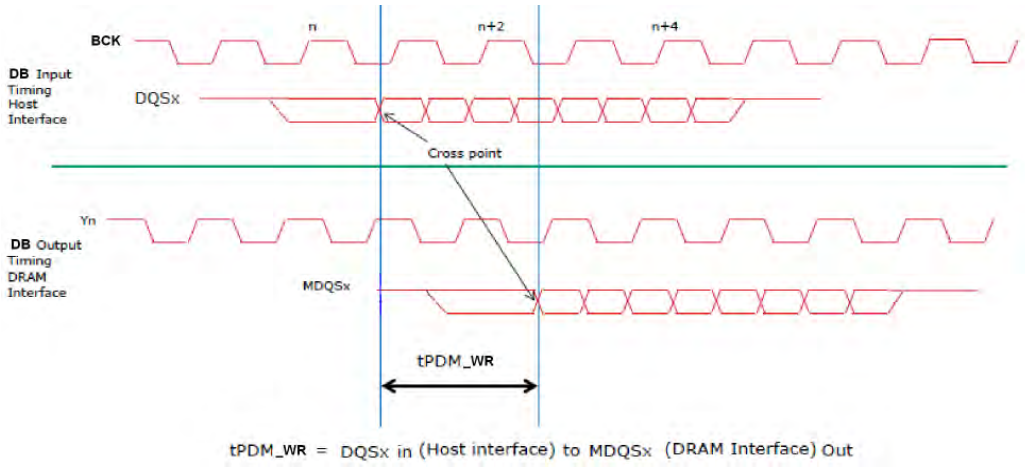


Figure 56 — tPDM_WR Latency Measurement

Id. at 165.

Table 146 — WRITE Output Timings

		DDR4-1600/ 1866/2133		DDR4-2400/ 2666		DDR4- 2933		DDR4-3200		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing											
tDVB	Data valid before MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
tDVA	Data valid after MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
Data Strobe Timing											
MDQS_t - MDQS_c differential output low time	tMQSL	0.46	-	0.46	-	0.46	-	0.46	-	tCK	1, 3
MDQS_t - MDQS_c differential output high time	tMQSH	0.46	-	0.46	-	0.46	-	0.46	-	tCK	2, 3

Unit UI = tCK(avg).min/2

NOTE 1: tMQSL describes the instantaneous differential output low pulse width on MDQS_t - MDQS_c, as measured from on falling edge to the next consecutive rising edge

NOTE 2: tMQSH describes the instantaneous differential output high pulse width on MDQS_t - MDQS_c, as measured from on rising edge to the next consecutive falling edge

NOTE 3: The specification values are affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.). However, these parameters should be met whether clock jitter is present or not.

Id. at 169.

64. On information and belief, Samsung also indirectly infringes the '339 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the '339 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM products and other materially similar products that infringe the '339 Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

65. On information and belief, Samsung also indirectly infringes the '339 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on

information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers and end-users infringement of the '339 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the '339 Patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM products and other materially similar products would be covered by one or more claims of the '339 Patent. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the '339 Patent.

66. Samsung's infringement of the '339 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the '339 Patent since at least August 2, 2021. Samsung's infringement of the '339 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VI. THIRD CLAIM FOR RELIEF – '918 PATENT

67. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

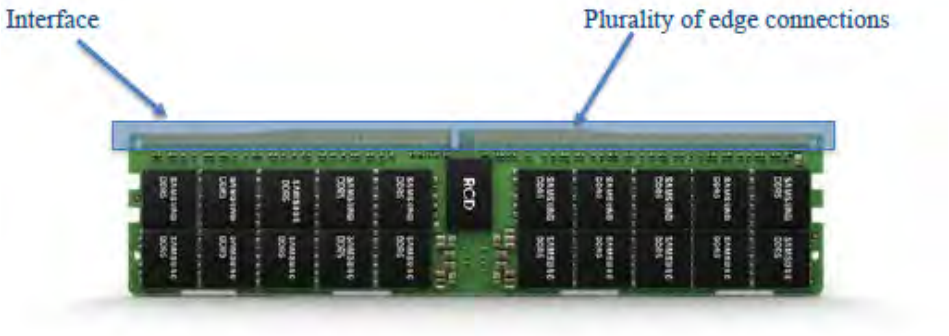
68. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '918 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR5 LRDIMMs, DDR5 RDIMMs, DDR5 SODIMMs, DDR5 UDIMMs, and other products with materially the same structures in relevant parts. For example, and as

shown below, the accused DDR5 memory modules and other products with materially the same structures in relevant parts infringe at least one claim of the '918 patent.

69. For example, the accused DDR5 products comprise a memory module comprising: a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system, as illustrated below.



Ex. 5 at 1 (depiction of a Samsung DDR5 LRDIMM).



Id. at 3 (depiction of a Samsung DDR5 RDIMM).

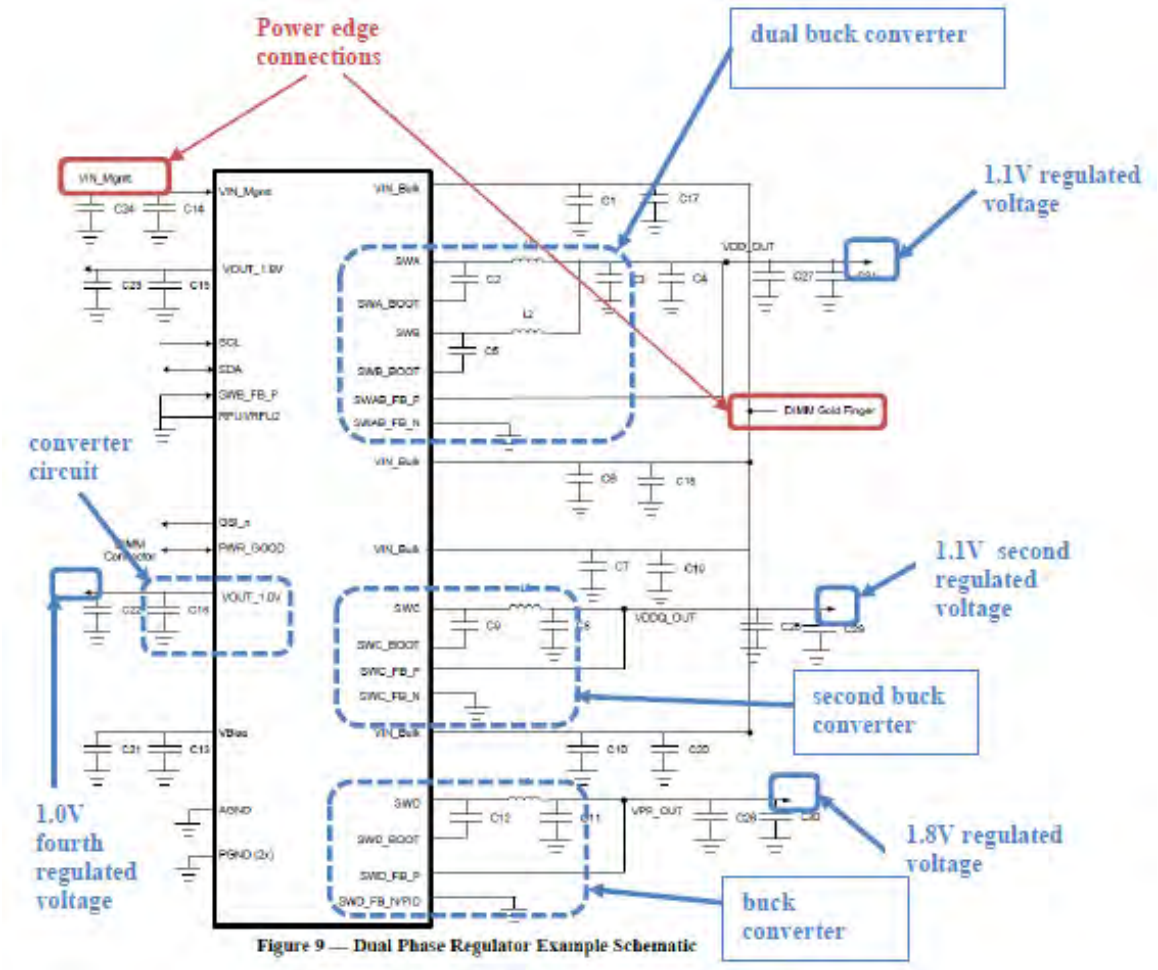
70. The accused DDR5 products further comprise a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; and a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude. For example, Samsung notes on its web site that its DDR5 modules include an "on-DIMM PMIC" that "further boosts power management efficiency and power supply stability." Ex. 12 at 5; *see also* Ex. 13 at 2 ("One major design improvement to the newest generation DRAM solution involves integrating the PMIC into the memory module — previous generations placed the PMIC on the motherboard — offering increased compatibility and signal integrity, and providing a more reliable and sustained performance.").

71. Samsung's PMIC for DDR5 includes a high-efficiency hybrid gate driver and an asynchronous-based dual-phase buck control scheme. *Id.* The dual-phase buck control scheme "allows the DC voltage to step down from high to low with a fast transient response to changes in the output load current and adapts the conversion accordingly to efficiently regulate its output voltage at near-constant levels." *Id*.

72. The PMIC provides the required regulated voltages, in accordance with the latest DDR5 standards.

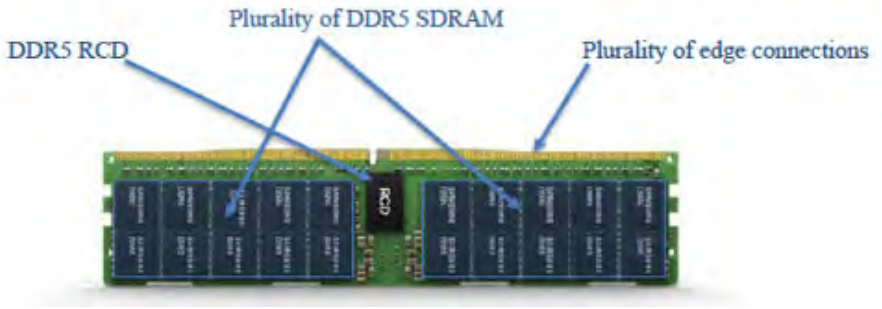


Ex. 5 at 1 (depiction of a Samsung DDR5 LRDIMM).

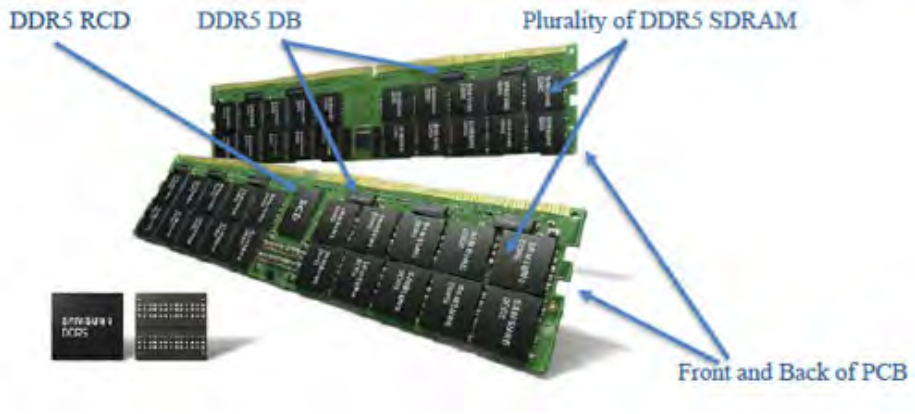


Ex. 14 (JEDEC Power Management Specification for DDR5) (annotated), at 19; *see also id.* at 20.

73. The accused DDR5 products further comprise a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising: a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and at least one circuit (*e.g.*, RCD) coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, as illustrated below.



Ex. 5 at 3 (depiction of a Samsung DDR5 RDIMM).



Ex. 5 at 1 (depiction of a Samsung DDR5 LRDIMM).

2.4 DDR5 SDRAM X4/8 Ballout using MO-210

Table 1 provides the ballout for DDR5 SDRAM X4/8 using MO-210.

Table 1 — DDR5 SDRAM X4/8 Ballout Using MO-210

AN	1	2	3	4	5	6	7	8	9	10	11
AL		1	2	3	4	5	6	7	8	9	
A	DNU	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	DNU
B		VDD	VDDQ	DQ2				DQ3	VDDQ	VDD	
C		VSS	DQ0	DQS_t				DM_n, TDQS_t	DQ1	VSS	
D		VDDQ	VSS	DQS_c				TDQS_c	VSS	VDDQ	
E		VDD	DQ4	DQ6				DQ7	DQ5	VDD	
F		VSS	VDDQ	VSS				VSS	VDDQ	VSS	
G		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	
H		ALERT_n	VSS	CS_n				CK_c	VSS	VDD	
J		VDDQ	CA4	CA0				CA1	CA5	VDDQ	
K		VDD	CA6	CA2				CA3	CA7	VDD	
L		VDDQ	VSS	CA8				CA9	VSS	VDDQ	
M		CAI	CA10	CA12				CA13	CA11	RESET_n	
N	DNU	VDD	VSS	VDD				VPP	VSS	VDD	DNU

Ex. 15 (JEDEC 79-5 DDR5 SDRAM Standard), at 3.

Table 3 — Pinout Description (Continued)

Symbol	Type	Function
LBDQ	Output	Loopback Data Output. The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.1 V
VDD	Supply	Power Supply: 1.1 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 1.8V
ZQ	Reference	Reference Pin for ZQ calibration. This ball is tied to an external 240 ohm resistor(RZQ), which is tied to V_{SS}

Id. at 5.

10.1 Operating Electrical Characteristics

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 189 — Operating Electrical Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage[1]	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V
V_{DDIO}	DDR5RCD01 Sideband Interface I/O Supply Voltage		0.95	1.0	1.05	V

Ex. 16 (JEDEC DDR5 RCD Standard, JESD 82-511), at 176.

74. The at least one circuit (e.g., RCD) is operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices. For example:

3.1 Description

The DDR5RCD01 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

Id. at 5.

75. The at least one circuit is coupled to both the second regulated voltage and the fourth regulated voltage. For example, the RCD receives both 1.0V VDDIO and 1.1V VDD input, with the amplitude of VDDIO being less than the amplitude of VDD.

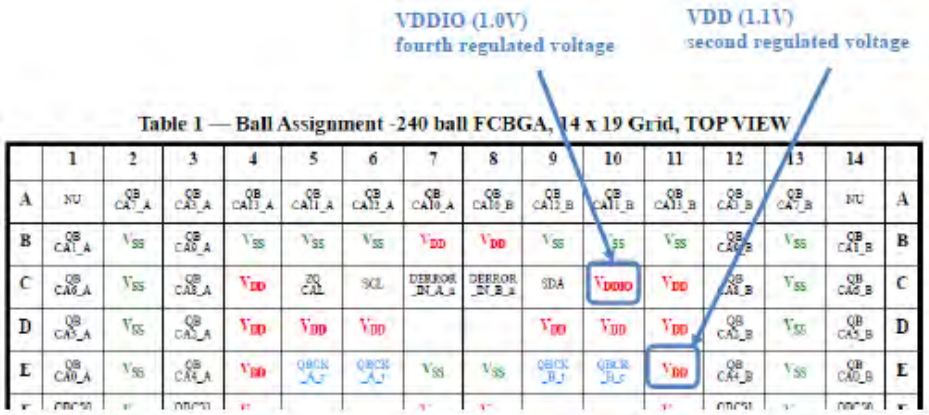


Table 1 — Ball Assignment -240 ball FCBGA, 14 x 19 Grid, TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NU	QB CA7_A	QB CA5_A	QB CA13_A	QB CA11_A	QB CA12_A	QB CA10_A	QB CA10_B	QB CA12_B	QB CA11_B	QB CA13_B	QB CA7_B	QB CA5_B	NU	A
B	QB CA1_A	V_{SS}	QB CA6_A	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	QB CA0_B	V_{SS}	QB CA1_B	B
C	QB CA6_A	V_{SS}	QB CA8_A	V_{DD}	ZQ CAL	SCL	DERROR_INT_A_n	DERROR_INT_B_n	SDA	V_{DDIO}	V_{DD}	QB CA1_B	V_{SS}	QB CA6_B	C
D	QB CA3_A	V_{SS}	QB CA2_A	V_{DD}	V_{DD}	V_{DD}			V_{DD}	V_{DD}	V_{DD}	QB CA2_B	V_{SS}	QB CA3_B	D
E	QB CA0_A	V_{SS}	QB CA4_A	V_{DD}	QBCK0_A_t	QBCK0_A_c	V_{SS}	V_{SS}	QBCK0_B_t	QBCK0_B_c	V_{DD}	QB CA4_B	V_{SS}	QB CA0_B	E

Id. at 3.

10.1 Operating Electrical Characteristics

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 189 — Operating Electrical Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage[1]	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V
V_{DDIO}	DDR5RCD01 Sideband Interface I/O Supply Voltage		0.95	1.0	1.05	V

Id. at 176.

76. On information and belief, Samsung also indirectly infringes the '918 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the '918 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR5 products and other materially similar products that infringe the '918

Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR5 memory modules and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

77. On information and belief, Samsung also indirectly infringes the '918 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers and end-users infringement of the '918 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR5 memory modules and other materially similar products that infringe the '918 Patent. On information and belief, the accused DDR5 products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR5 products and other materially similar products may be covered by one or more claims of the '918 Patent. On information and belief, the use of the product or process that includes the accused DDR5 products and other materially similar products infringes at least one claim of the '918 Patent.

78. Samsung's infringement of the '918 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the '918 Patent since at least August 2, 2021. Samsung's infringement of the '506 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

Micron Technology Inc. et al.
Ex. 1044, p. 47

VII. DEMAND FOR JURY TRIAL

79. Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

VIII. PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Samsung infringes the Patents-in-Suit;

B. all equitable relief the Court deems just and proper as a result of Samsung's infringement;

C. an award of damages resulting from Samsung's acts of infringement in accordance with 35 U.S.C. § 284;

D. that Samsung's infringement of the Patents-in-Suit is willful;

E. enhanced damages pursuant to 35 U.S.C. § 284;

F. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

G. an accounting for acts of infringement and supplemental damages, without limitation, prejudgment and post-judgment interest; and

H. such other equitable relief which may be requested and to which Netlist is entitled.

Dated: December 20, 2021

Respectfully submitted,

/s/ Sam Baxter

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Exhibit 1

US010860506B2

(12) **United States Patent**
Lee et al.

(10) **Patent No.: US 10,860,506 B2**
(45) **Date of Patent: *Dec. 8, 2020**

(54) **MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Hyun Lee**, Ladera Ranch, CA (US); **Jayesh R. Bhakta**, Cerritos, CA (US)

(73) Assignee: **NETLIST, INC.**, Irvine, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **16/391,151**

(22) Filed: **Apr. 22, 2019**

(65) **Prior Publication Data**

US 2019/0347220 A1 Nov. 14, 2019

Related U.S. Application Data

(63) Continuation of application No. 15/820,076, filed on Nov. 21, 2017, now Pat. No. 10,268,608, which is a (Continued)

(51) **Int. Cl.**
G06F 3/00 (2006.01)
G06F 12/00 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G06F 13/1673*** (2013.01); ***G06F 1/10*** (2013.01); ***G06F 3/0613*** (2013.01);
(Continued)

(58) **Field of Classification Search**
None
See application file for complete search history.

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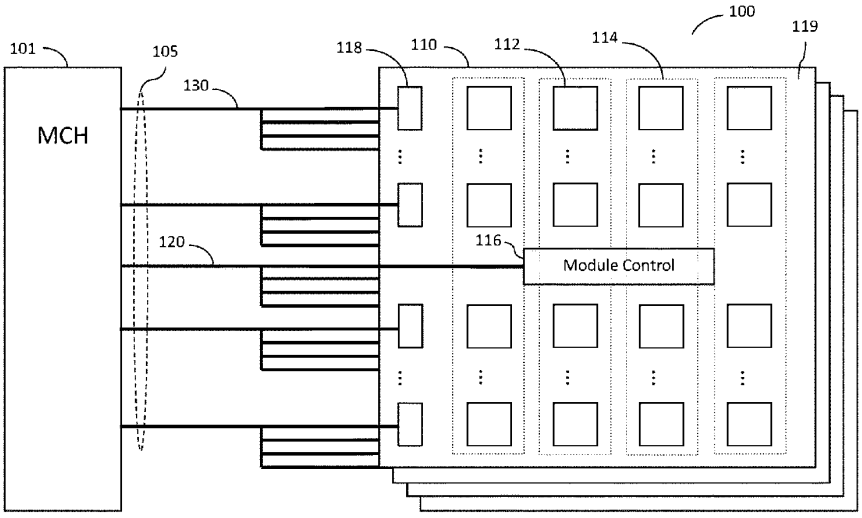
Lee, Office Action, U.S. Appl. No. 15/426,064, dated Jun. 2, 2017, 11 pgs.
(Continued)

Primary Examiner — Michael Sun
(74) *Attorney, Agent, or Firm* — Morgan, Lewis & Bockius LLP

(57) **ABSTRACT**

A memory module is operable in a memory system with a memory controller. The memory module comprises memory devices, a module control circuit, and a plurality of buffer circuits coupled between respective sets of data signal lines in a data bus and respective sets of the memory devices. Each respective buffer circuit is mounted on the module board and coupled between a respective set of data signal lines and a respective set of memory devices. Each respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal. Each respective buffer circuit includes a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals.

20 Claims, 26 Drawing Sheets



Related U.S. Application Data

continuation of application No. 15/426,064, filed on Feb. 7, 2017, now Pat. No. 9,824,035, which is a continuation of application No. 14/846,993, filed on Sep. 7, 2015, now Pat. No. 9,563,587, which is a continuation of application No. 13/952,599, filed on Jul. 27, 2013, now Pat. No. 9,128,632.

(60) Provisional application No. 61/676,883, filed on Jul. 27, 2012.

(51) **Int. Cl.**

G06F 13/00	(2006.01)
G06F 13/16	(2006.01)
G06F 3/06	(2006.01)
G11C 5/04	(2006.01)
G11C 7/10	(2006.01)
G11C 29/02	(2006.01)
G11C 16/00	(2006.01)
G06F 1/10	(2006.01)
G06F 13/28	(2006.01)
G06F 13/40	(2006.01)
G11C 8/18	(2006.01)
G11C 8/12	(2006.01)
G11C 7/20	(2006.01)
G11C 29/04	(2006.01)

(52) **U.S. Cl.**

CPC ***G06F 3/0647*** (2013.01); ***G06F 3/0656*** (2013.01); ***G06F 3/0659*** (2013.01); ***G06F 3/0683*** (2013.01); ***G06F 13/1642*** (2013.01); ***G06F 13/28*** (2013.01); ***G06F 13/4027*** (2013.01); ***G11C 5/04*** (2013.01); ***G11C 7/1006*** (2013.01); ***G11C 7/1066*** (2013.01); ***G11C 7/1093*** (2013.01); ***G11C 8/18*** (2013.01); ***G11C 16/00*** (2013.01); ***G11C 29/023*** (2013.01); ***G11C 29/028*** (2013.01); ***H05K 999/99*** (2013.01); *G11C 7/109* (2013.01); *G11C 7/20* (2013.01); *G11C 8/12* (2013.01); *G11C 2029/0407* (2013.01)

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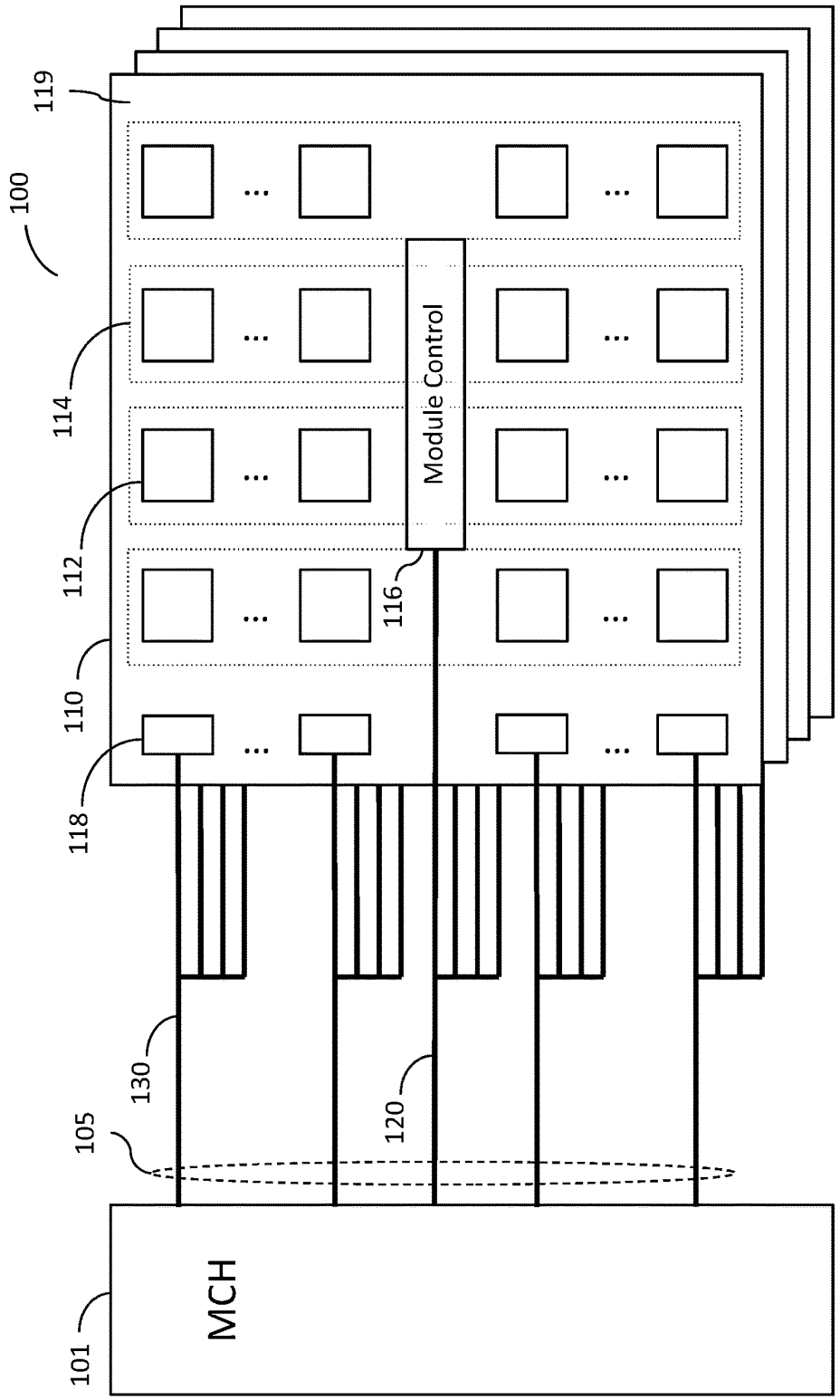


FIG. 1

FIG. 2A

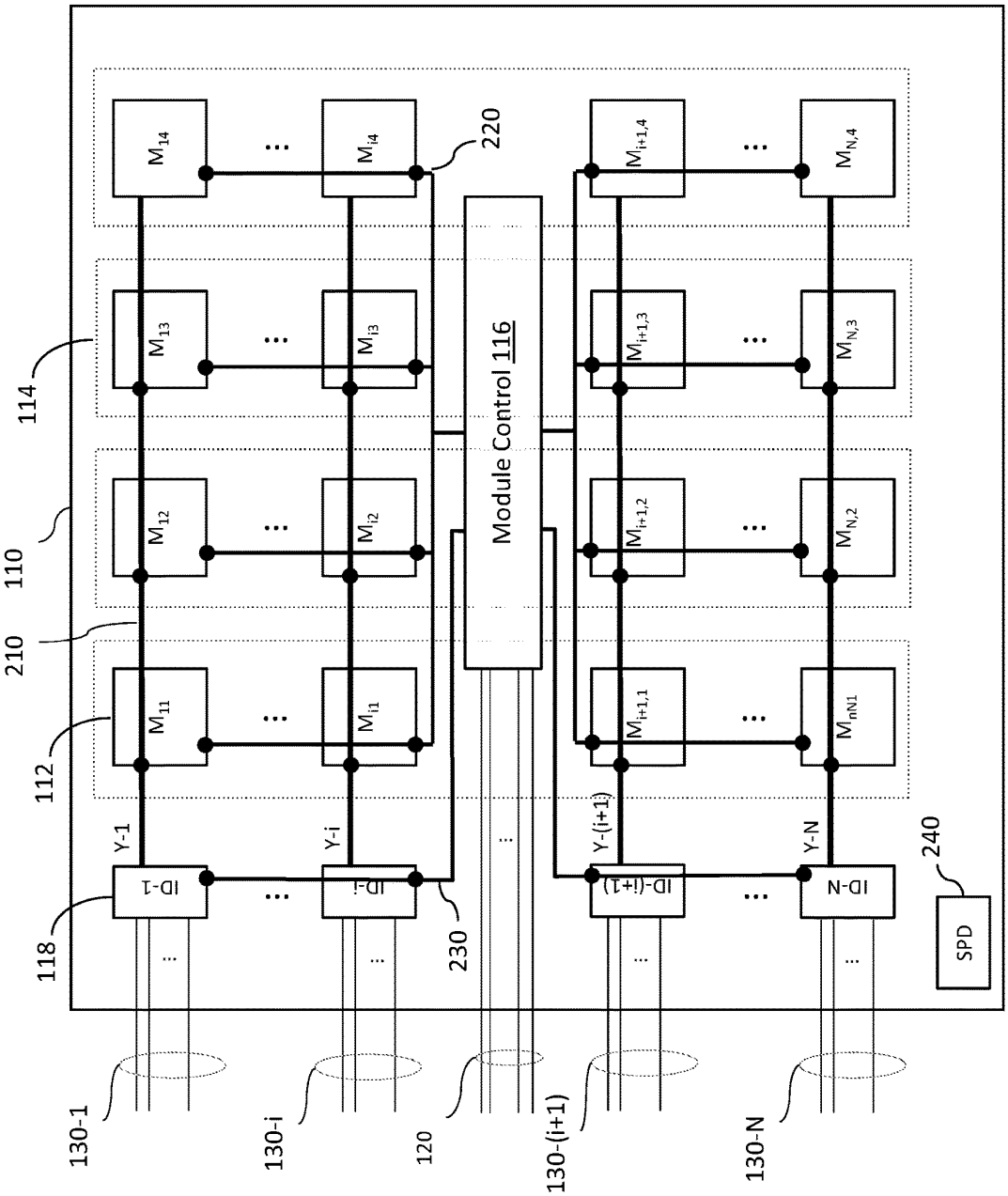
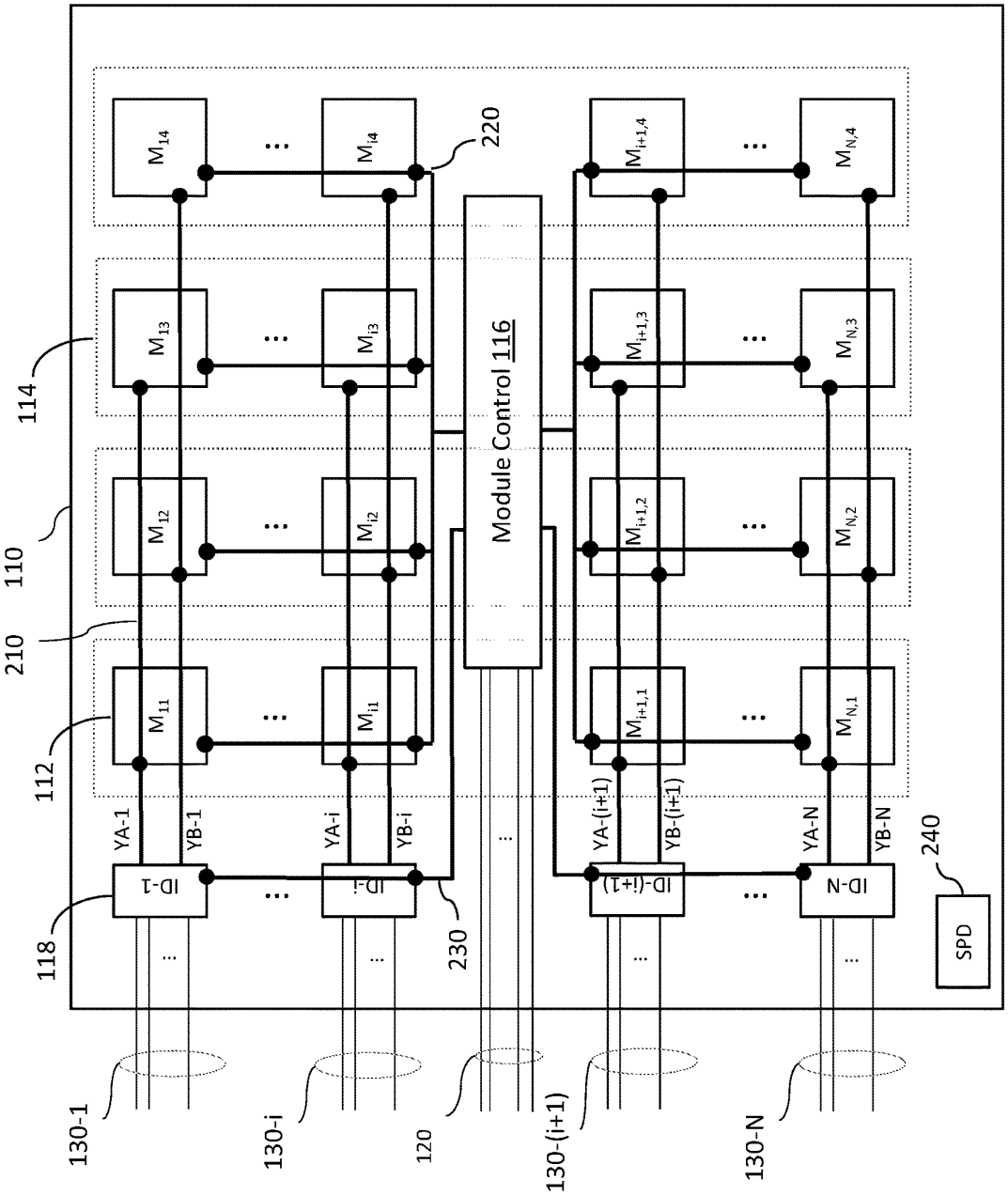

Module Control 116
220
230
240
SPD
114
110
210
112
118
Y-1
Y-i
Y-(i+1)
Y-N
ID-1
ID-i
ID-(i+1)
ID-N
130-1
130-i
120
130-(i+1)
130-N

FIG. 2B


Module Control 116
220
230
240
SPD
114
110
210
112
118
120
130-1
130-i
130-(i+1)
130-N
YA-1
YB-1
YA-i
YB-i
YA-(i+1)
YB-(i+1)
YA-N
YB-N
ID-1
ID-i
ID-(i+1)
ID-N
M11
M12
M13
M14
Mi1
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Mi3
Mi4
Mi+1,1
Mi+1,2
Mi+1,3
Mi+1,4
MN,1
MN,2
MN,3
MN,4

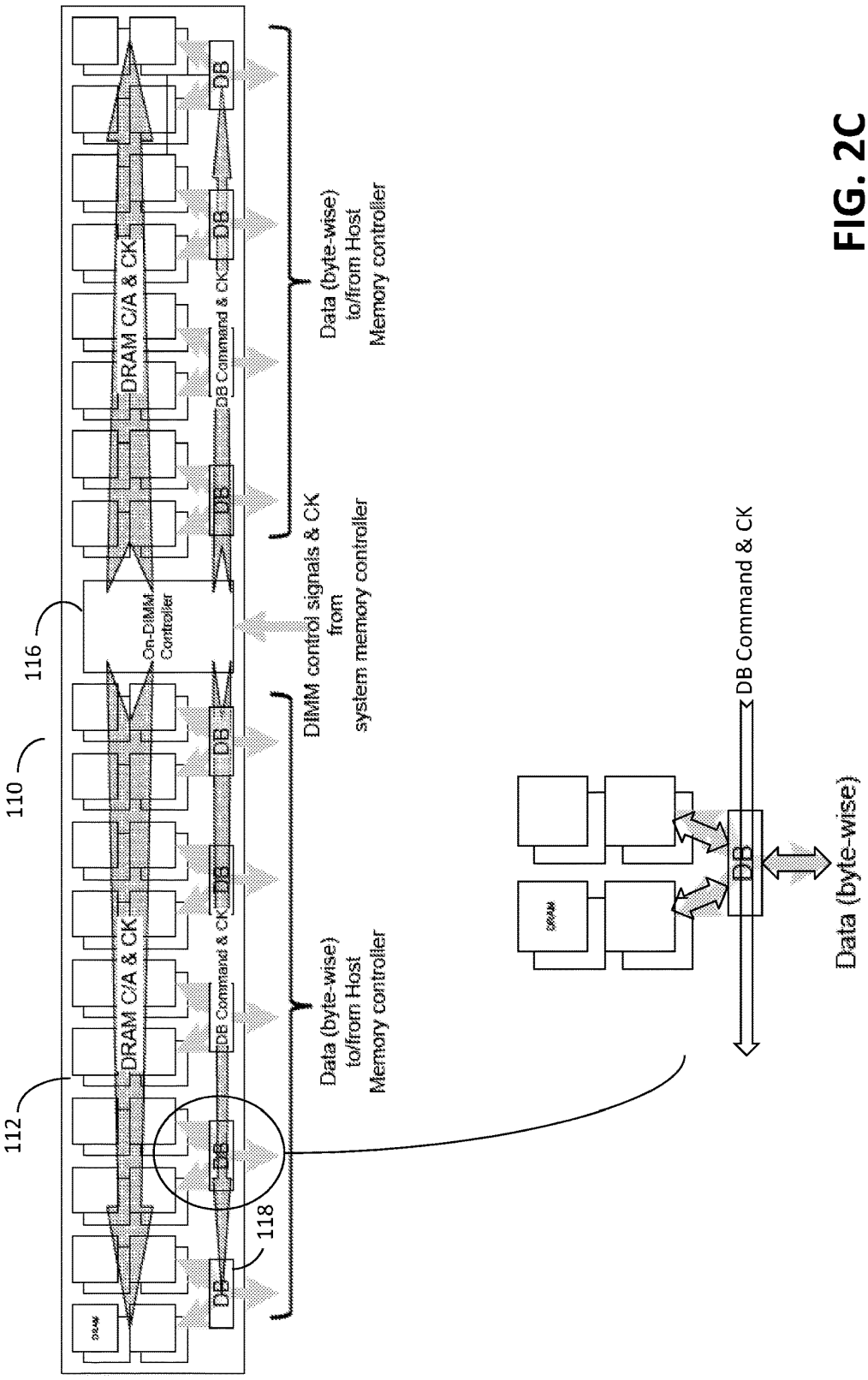

DRAM C/A & CK
DB Command & CK
DB
On-DIMM Controller
116
110
112
118
DIMM control signals & CK from system memory controller
Data (byte-wise) to/from Host Memory controller
DB Command & CK
Data (byte-wise)

FIG. 2C

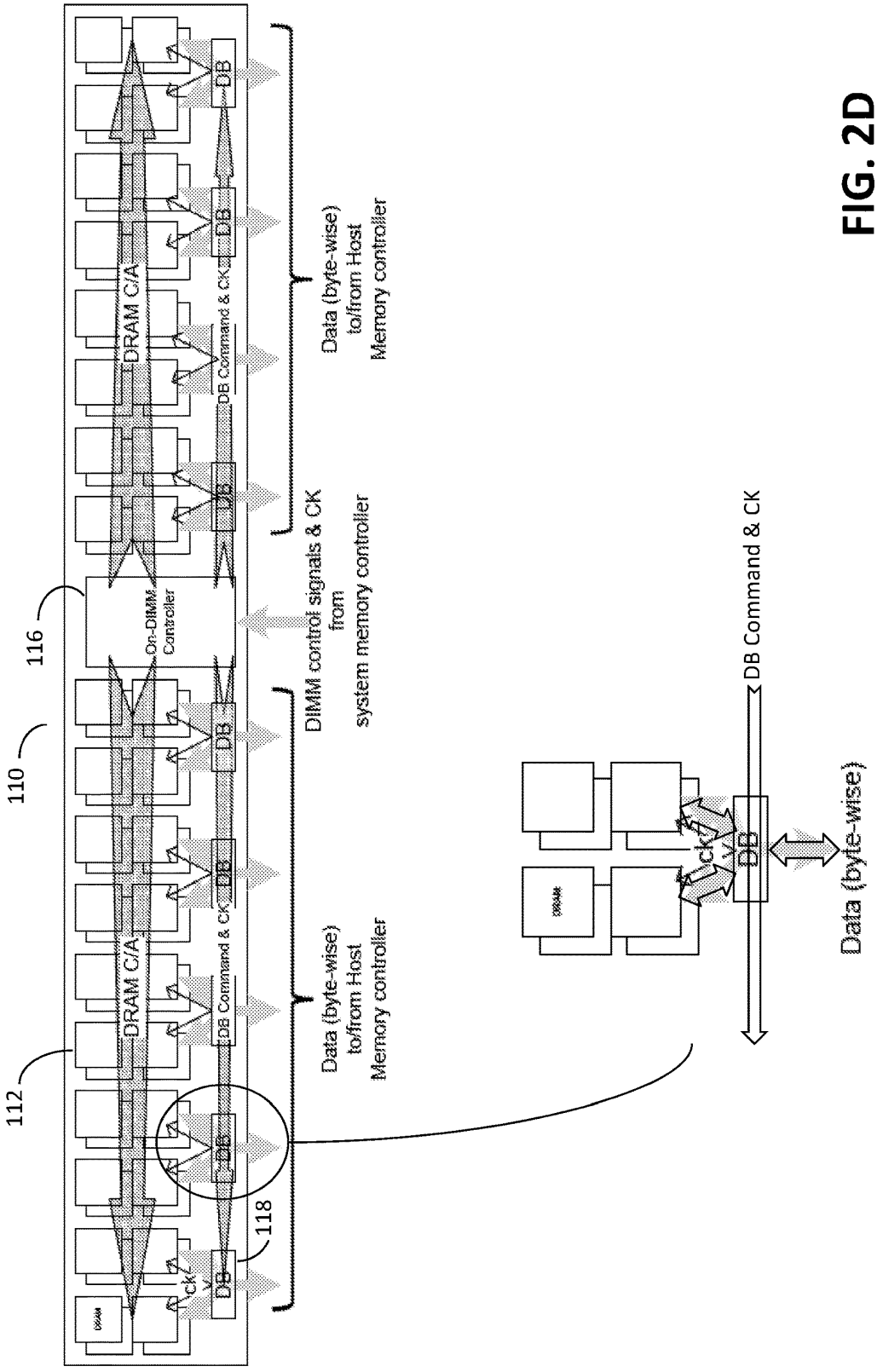

112
110
116
118
DRAM C/A
DB Command & CK
DB
On-DIMM Controller
DIMM control signals & CK from system memory controller
Data (byte-wise) to/from Host Memory controller
Data (byte-wise) to/from Host Memory controller
DB Command & CK
Data (byte-wise)

FIG. 2D

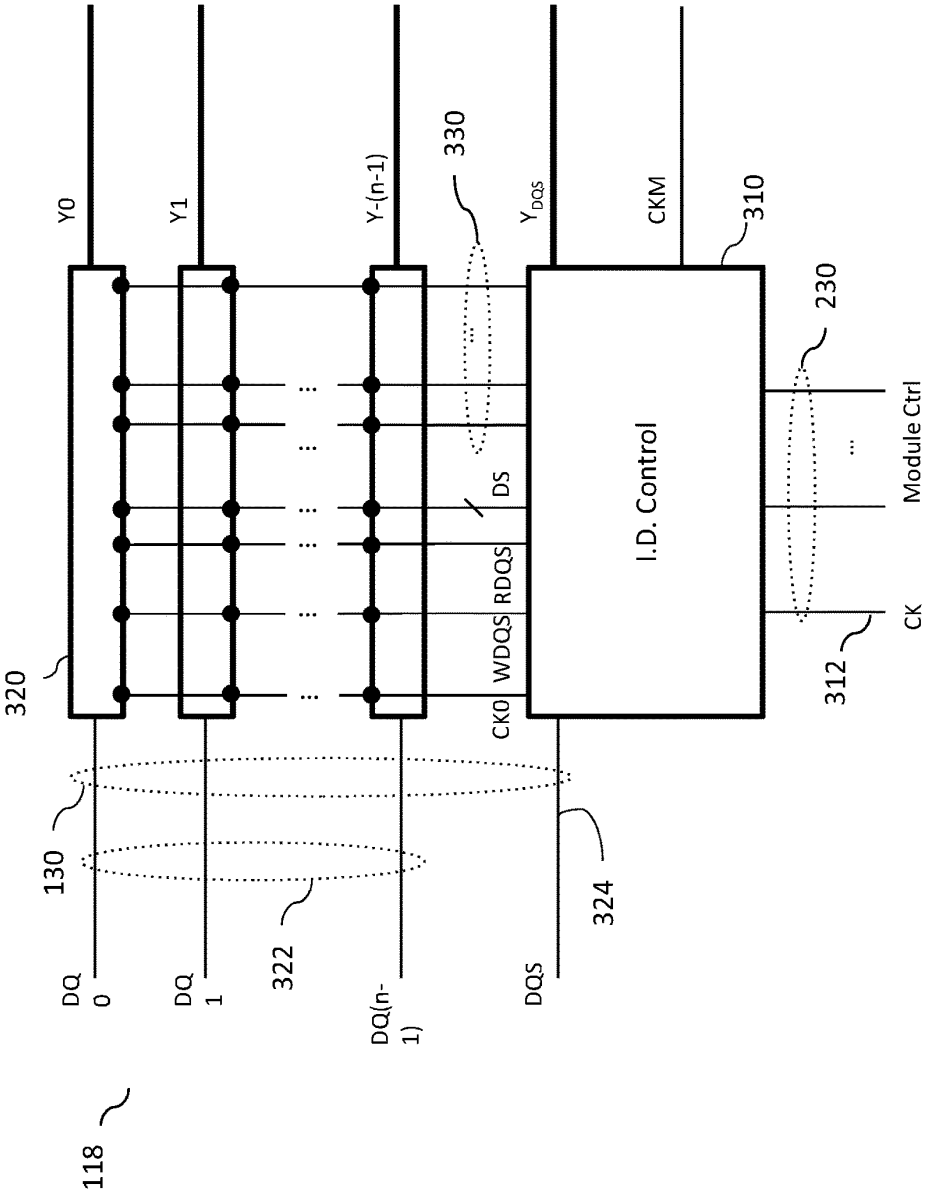

Y0
Y1
Y-(n-1)
330
Y_{DQS}
CKM
310
230
I.D. Control
DS
RDQS
WDQS
CK0
Module Ctrl
CK
312
320
130
322
324
DQ 0
DQ 1
DQ(n-1)
DQS
118

FIG. 3

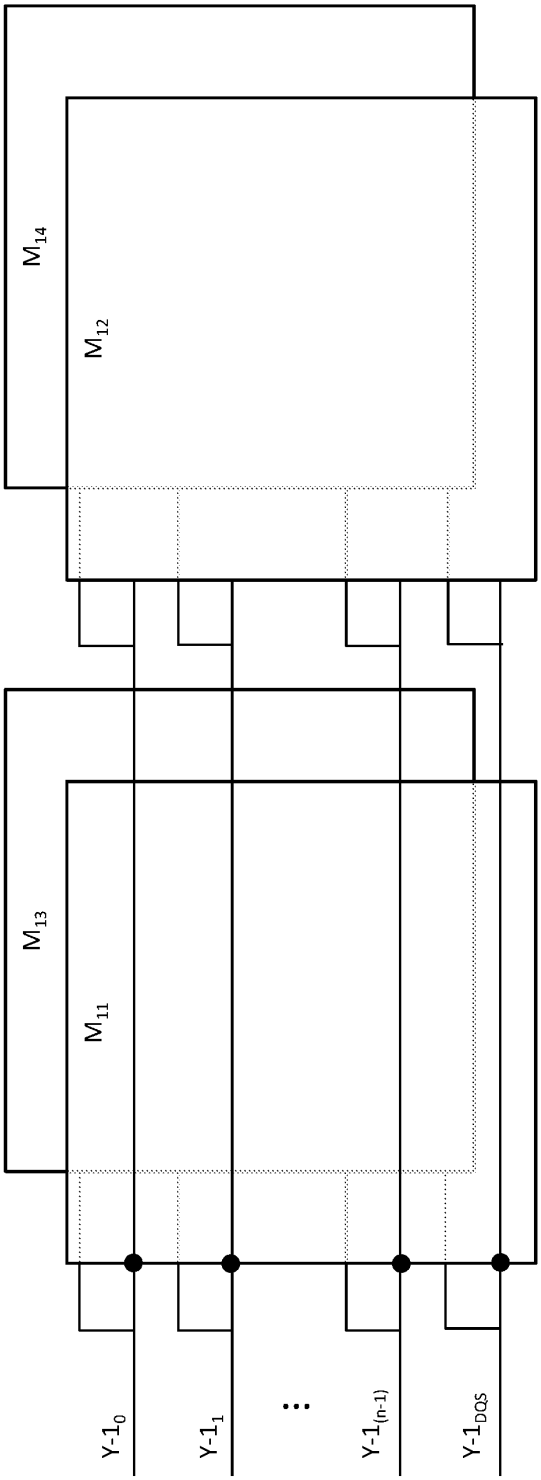


FIG. 4A

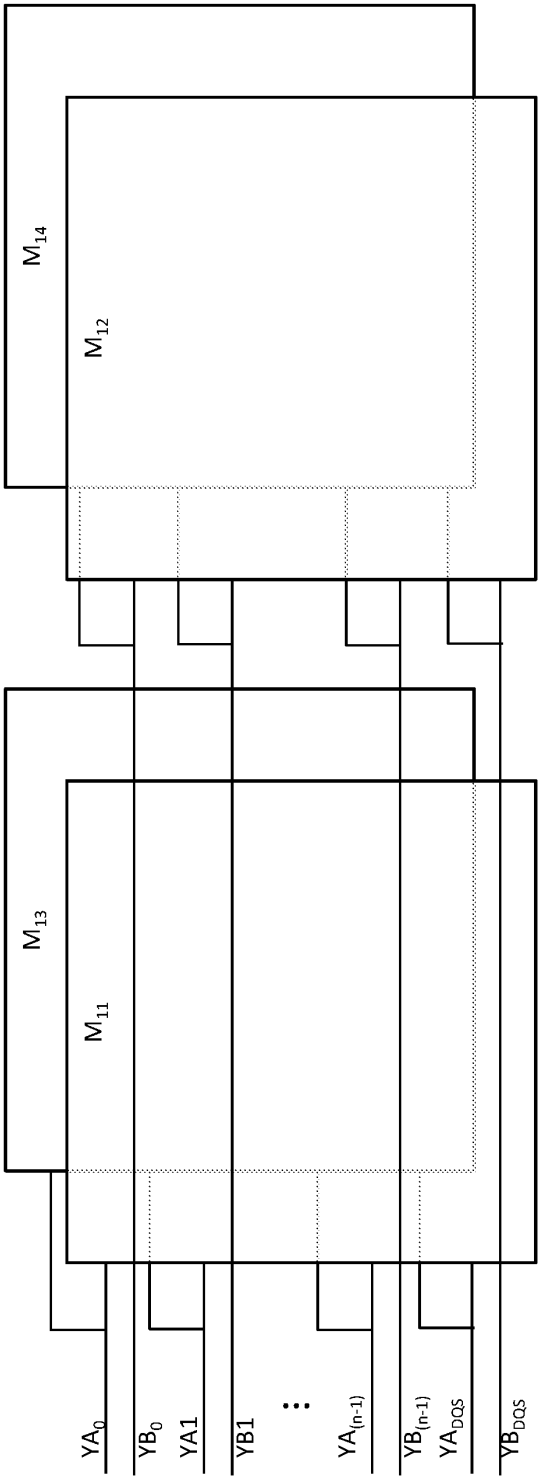


FIG. 4B

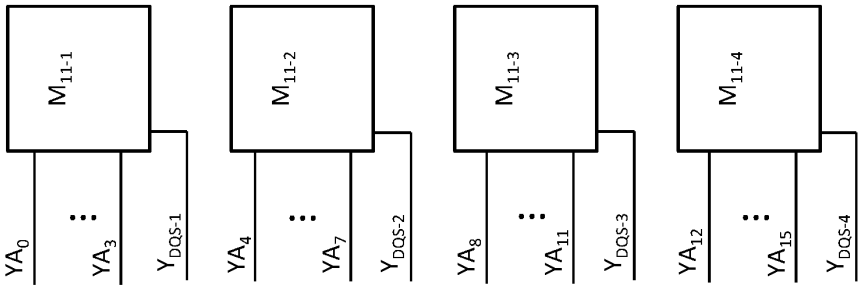

M11-1
M11-2
M11-3
M11-4
YA0
YA3
YDQS-1
YA4
YA7
YDQS-2
YA8
YA11
YDQS-3
YA12
YA15
YDQS-4

FIG. 5B

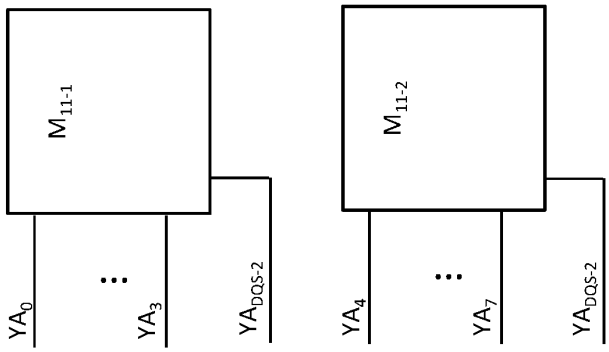

M11-1
M11-2
YA0
YA3
YADQS-2
YA4
YA7
YADQS-2

FIG. 5A

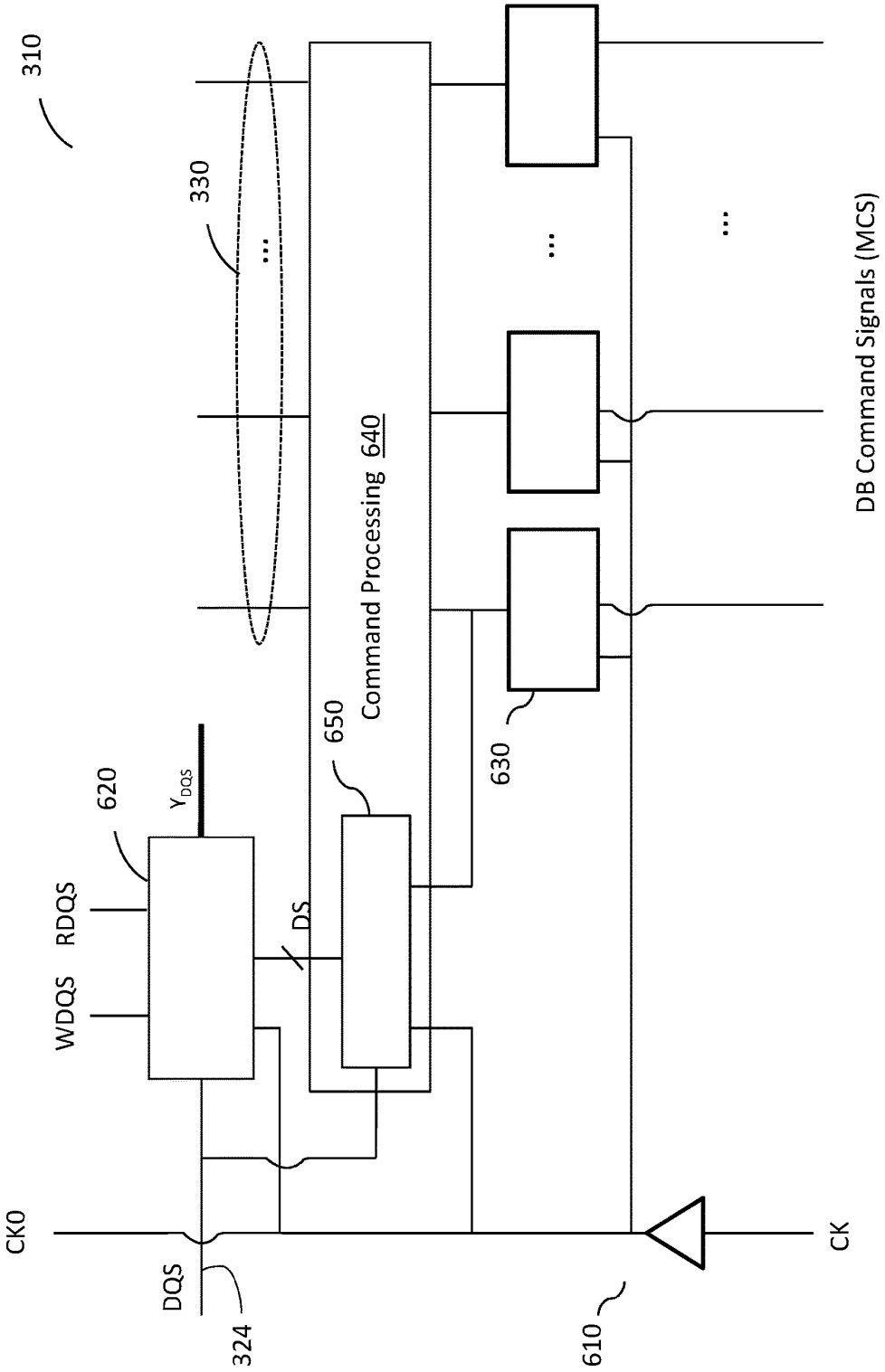

310
330
Command Processing 640
650
620
630
Y_{DQS}
RDQS
WDQS
DS
DB Command Signals (MCS)
CK0
CK
DQS
324
610

FIG. 6

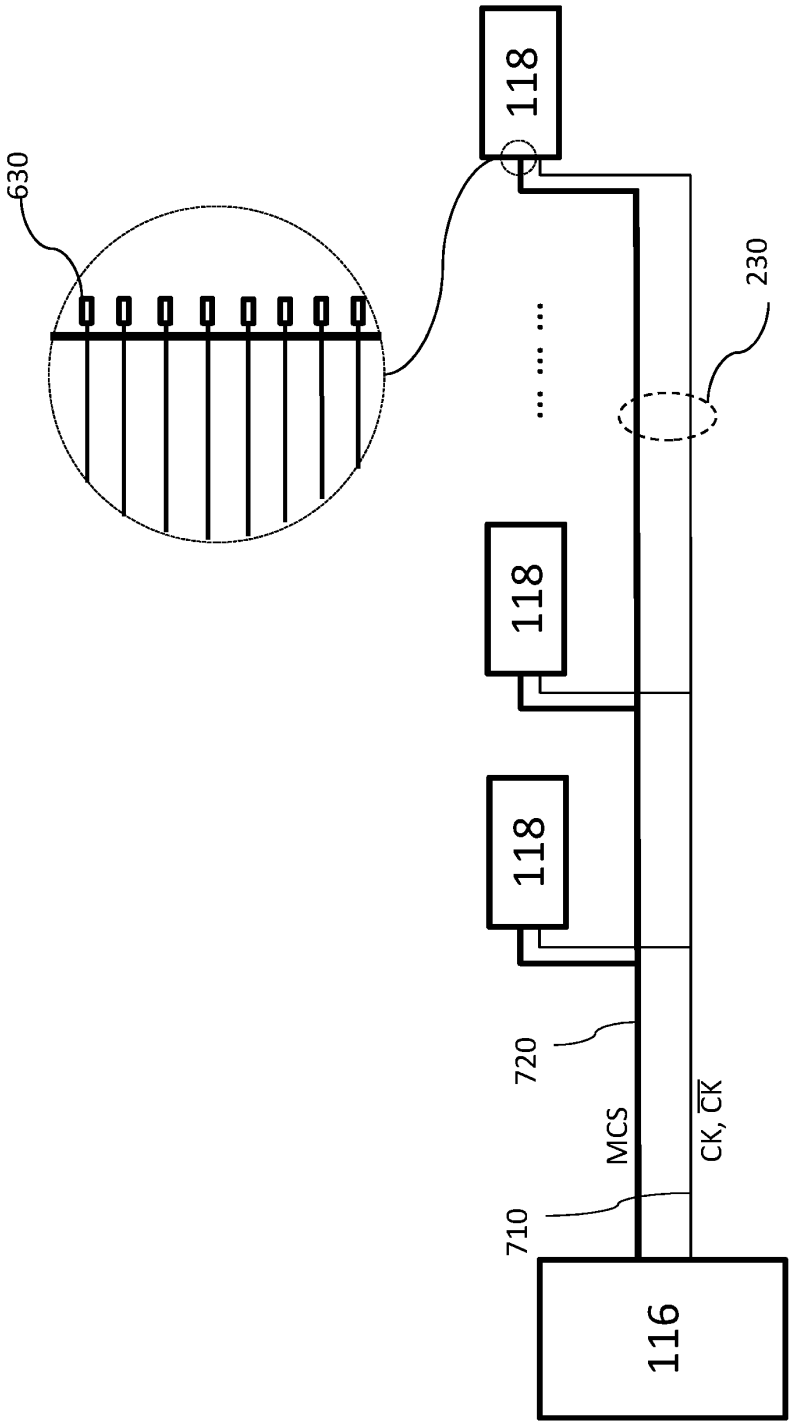


FIG. 7

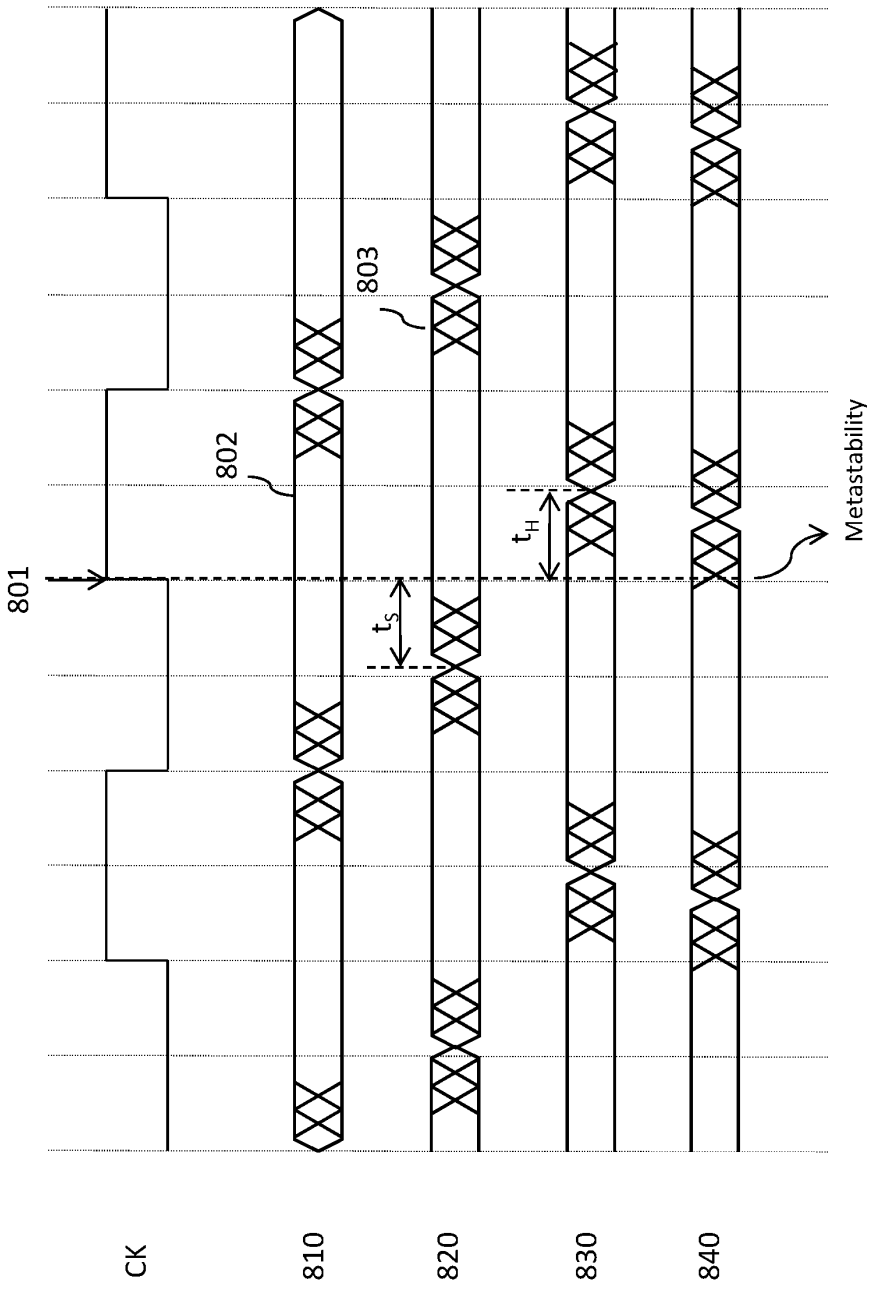


FIG. 8

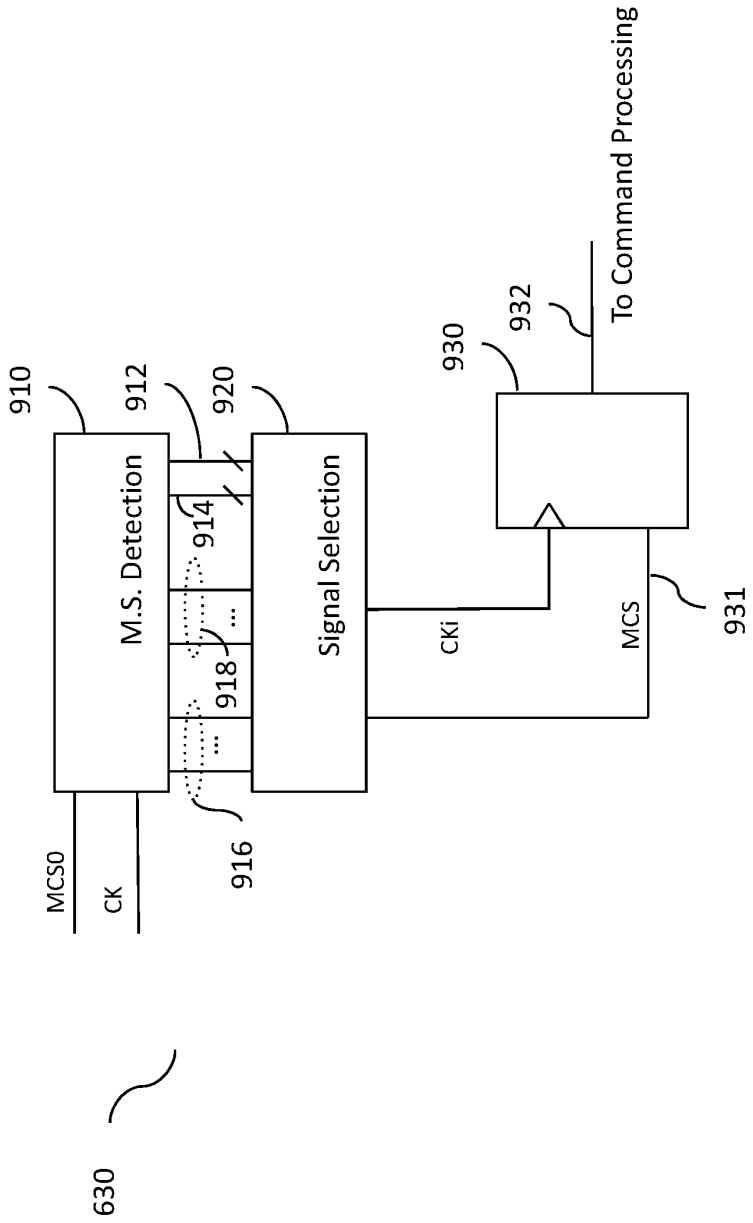

630
910
912
920
930
932
To Command Processing
M.S. Detection
914
918
916
Signal Selection
CKi
MCS
931
MCS0
CK

FIG. 9

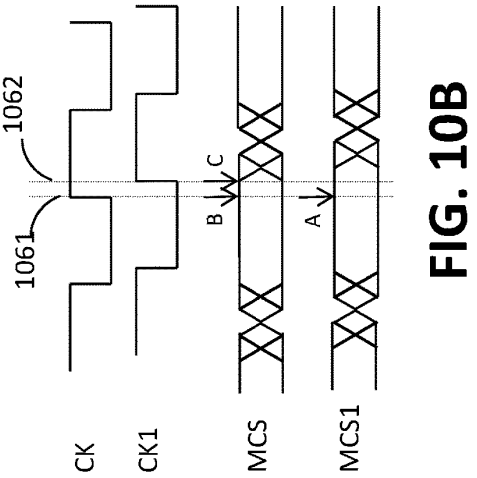


FIG. 10B

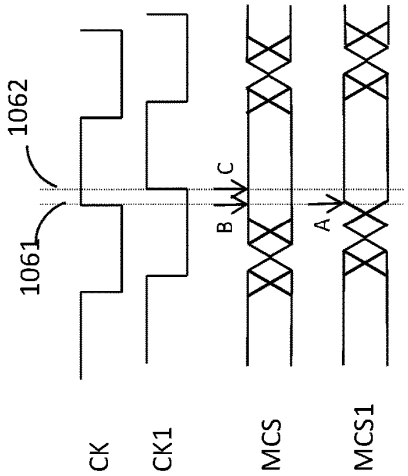


FIG. 10C

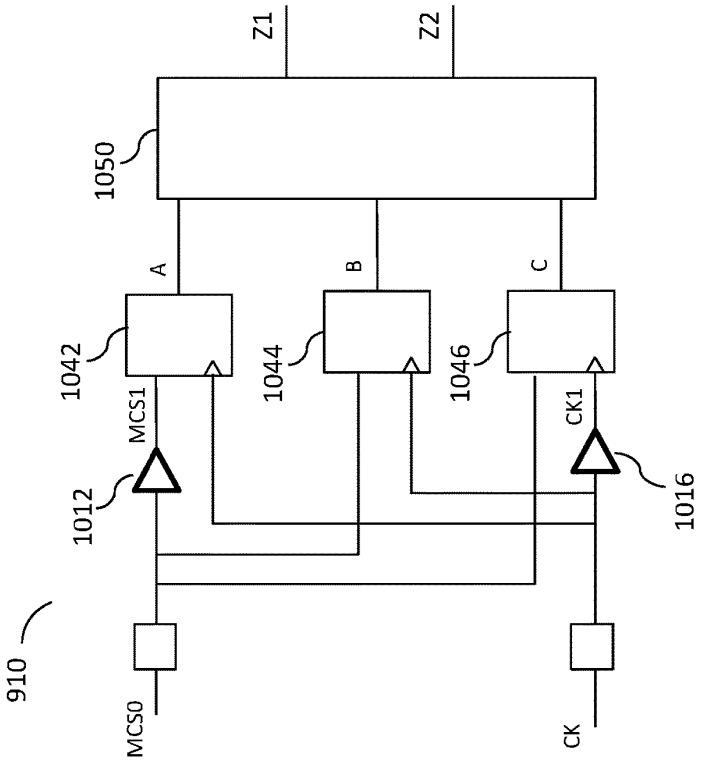


FIG. 10A

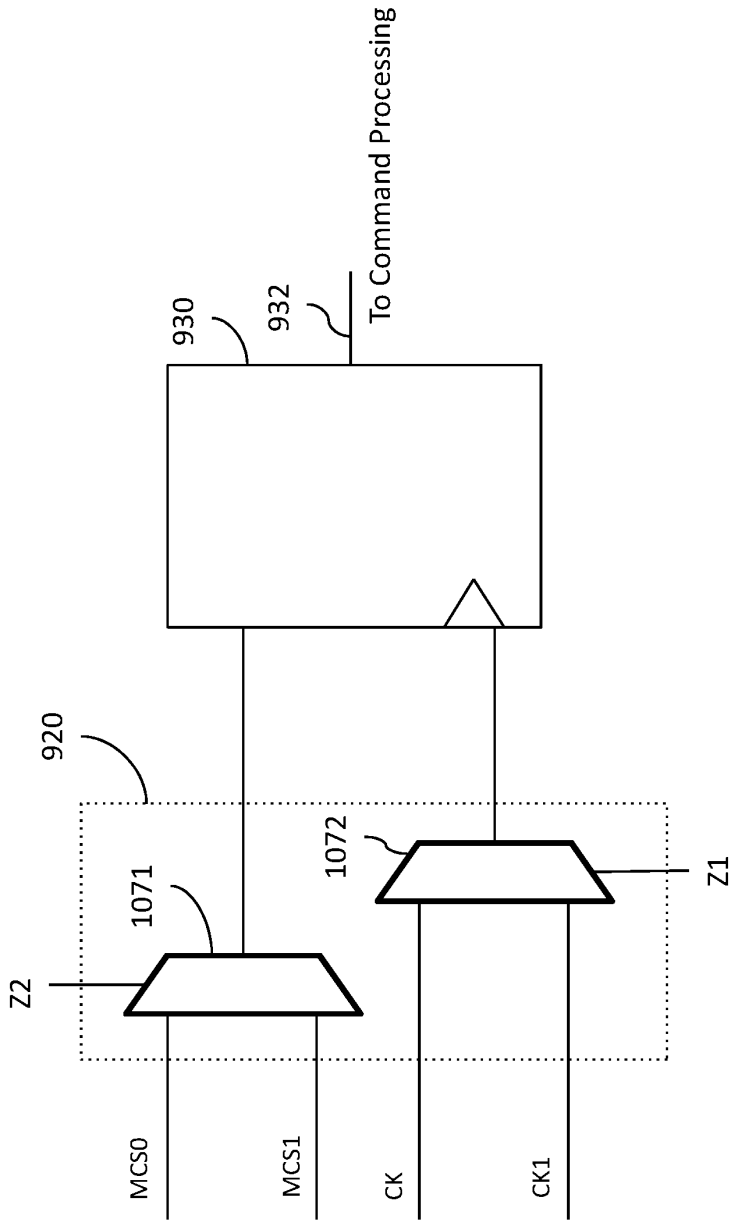
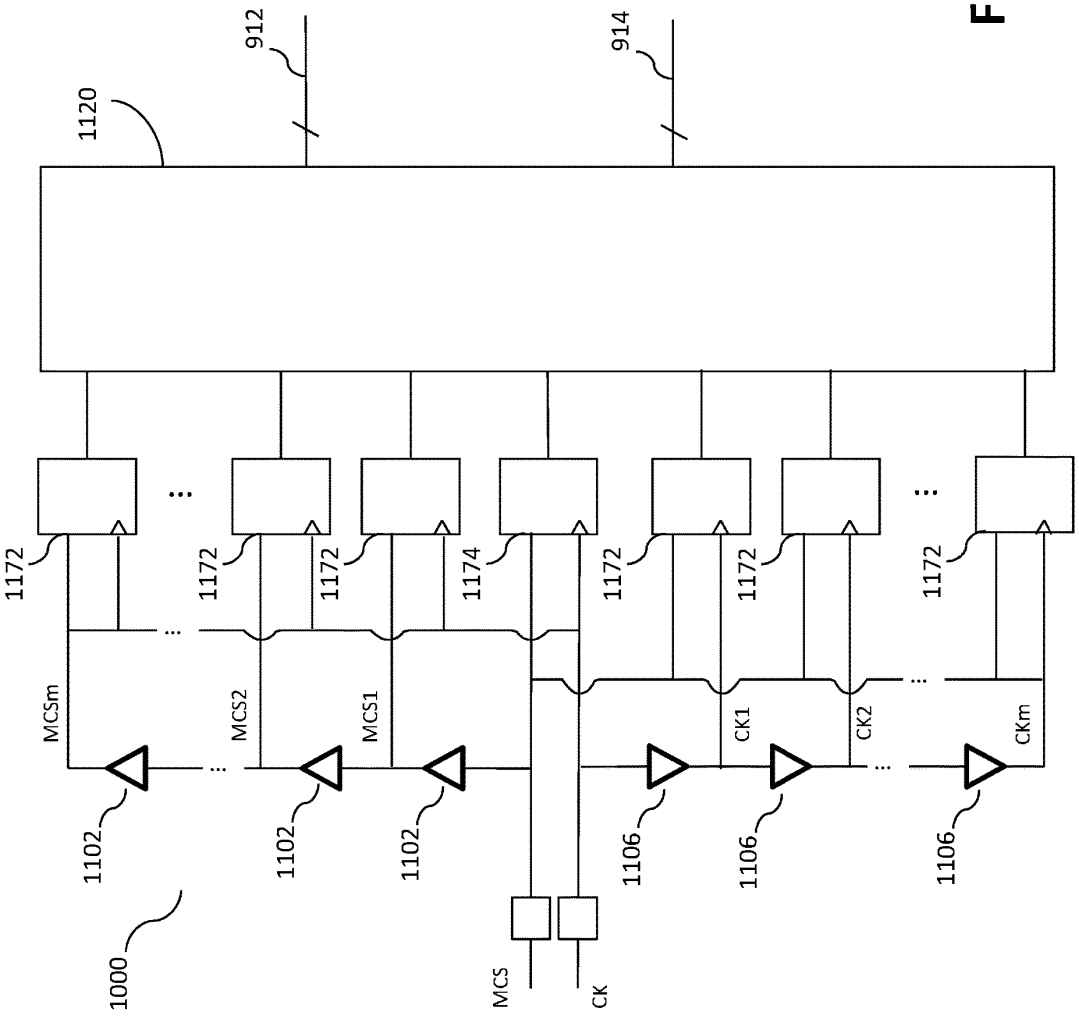

To Command Processing
930
932
920
1071
1072
Z2
Z1
MCS0
MCS1
CK
CK1

FIG. 10D

FIG. 11A


912
914
1120
1172
1174
MCSm
MCS2
MCS1
CK1
CK2
CKm
1102
1106
1000
MCS
CK

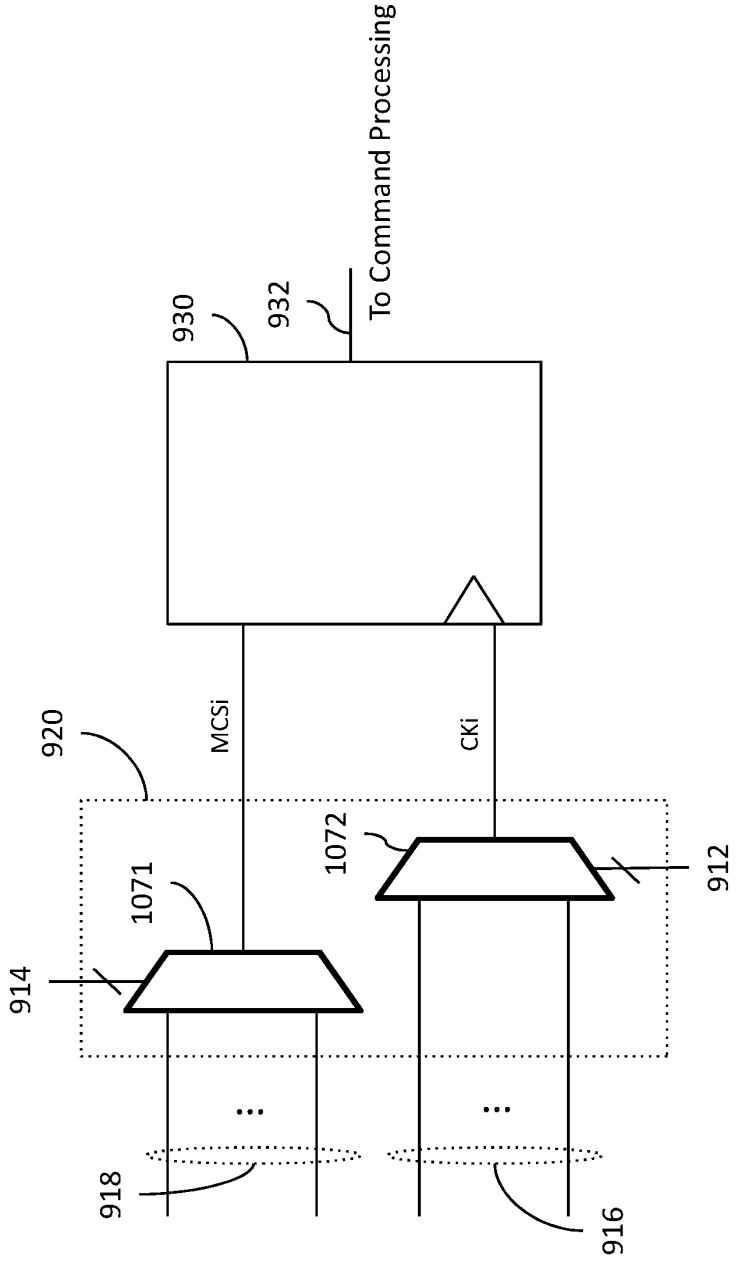

To Command Processing
930
932
MCSi
CKi
920
1071
1072
912
914
918
916

FIG. 11B

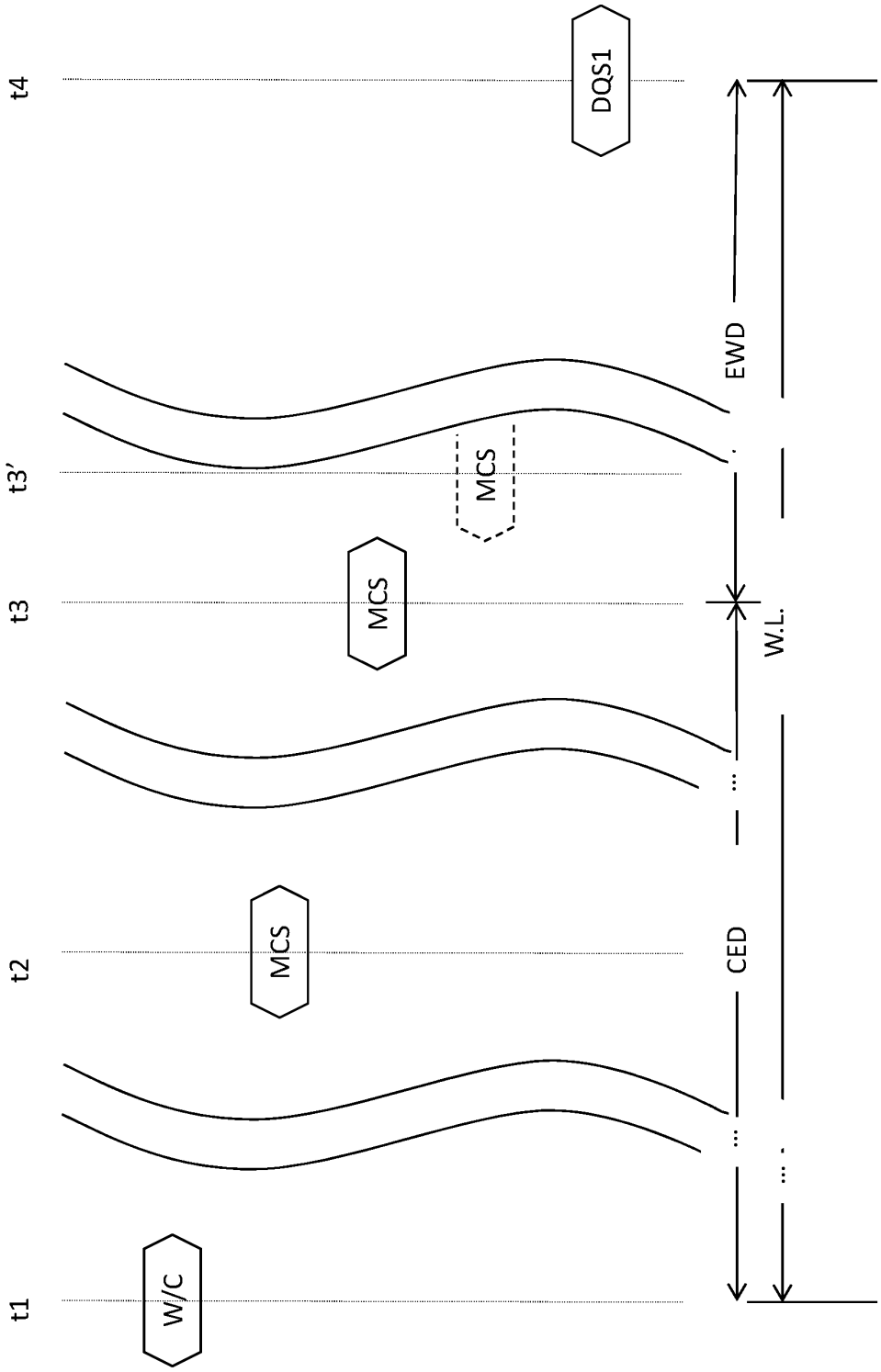


FIG. 12A

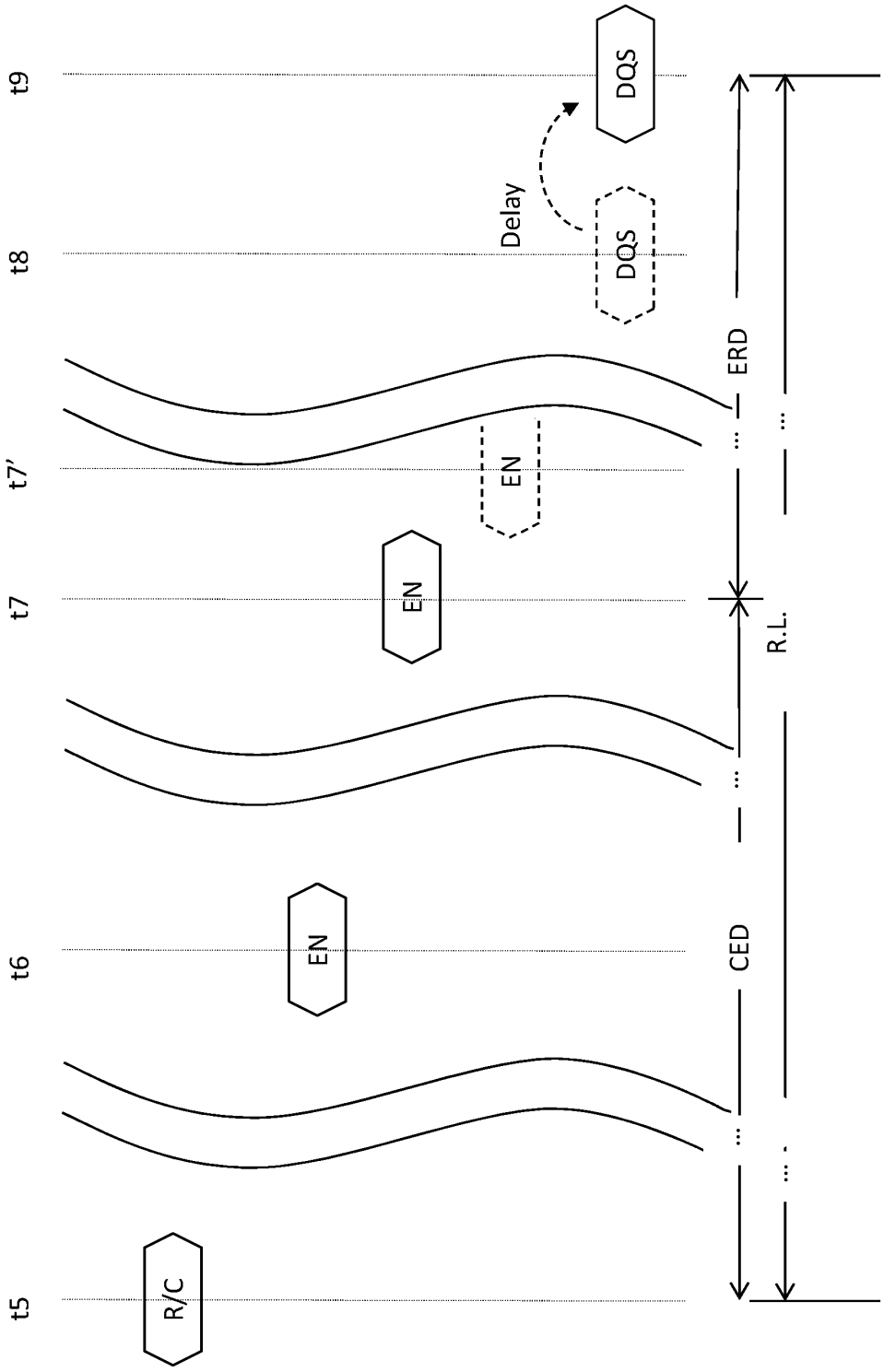


FIG. 12B

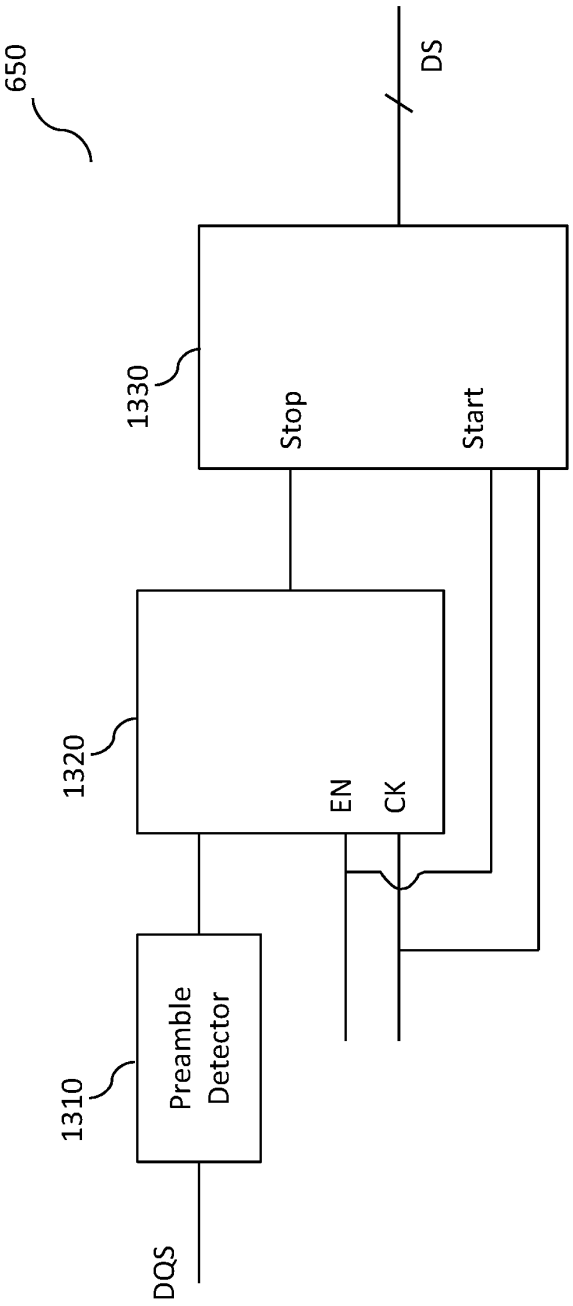


FIG. 13

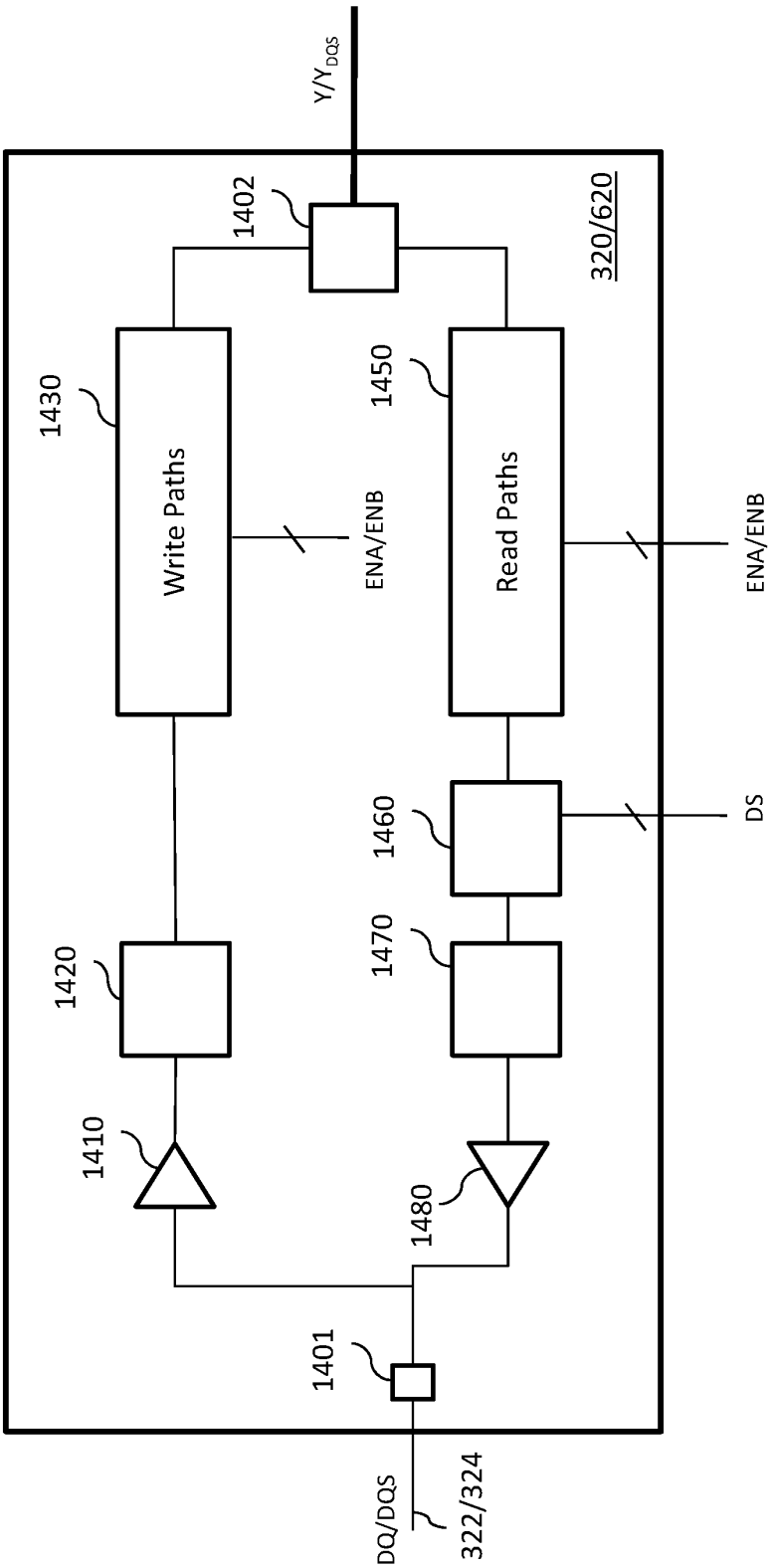

Y/Y_DQS
1402
320/620
1430
Write Paths
1450
Read Paths
ENA/ENB
ENA/ENB
1460
DS
1470
1420
1410
1480
1401
DQ/DQS
322/324

FIG. 14

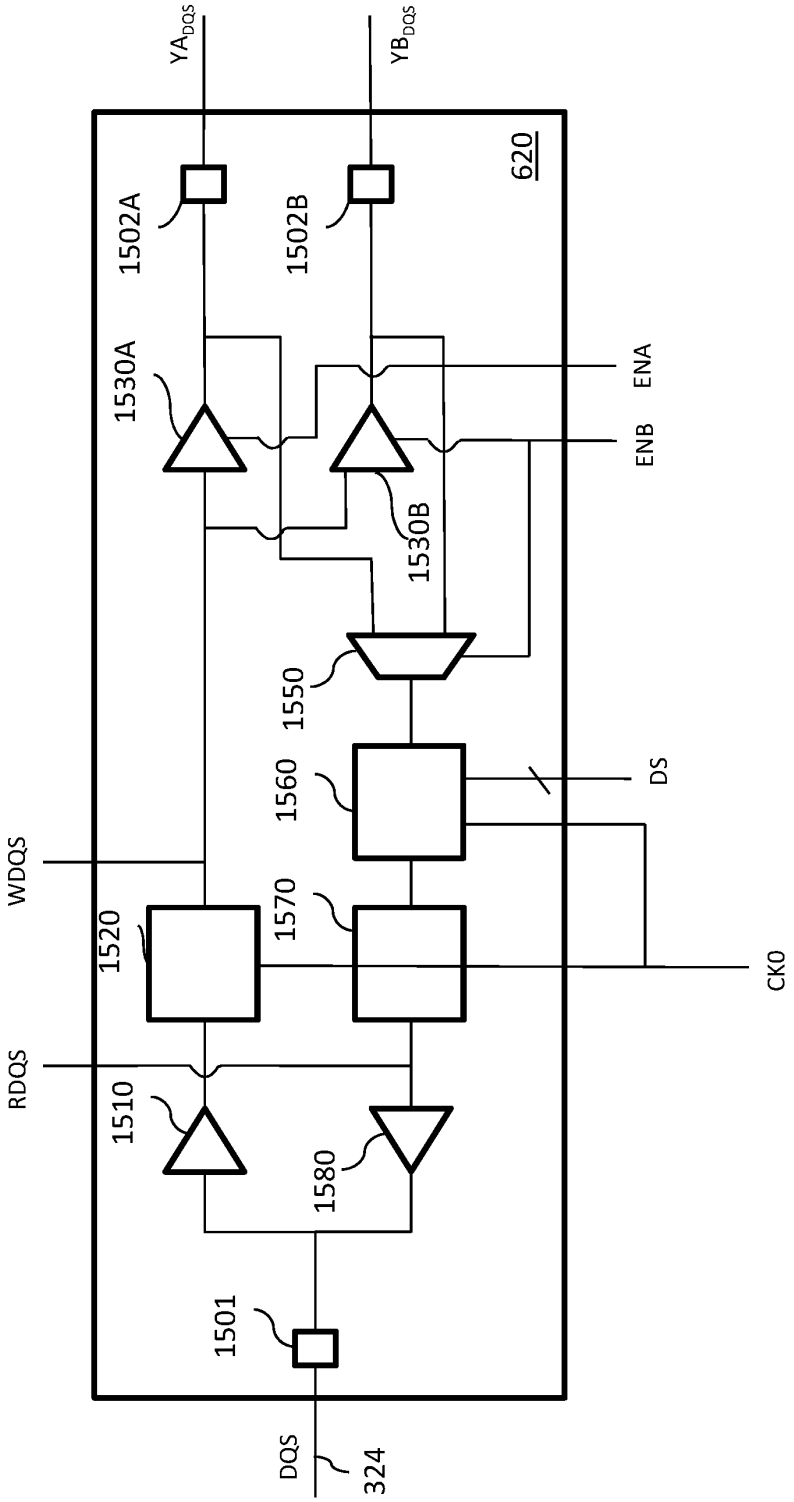

YA_DQS
YB_DQS
620
1502A
1502B
1530A
1530B
ENA
ENB
1550
1560
DS
WDQS
1520
1570
CK0
RDQS
1510
1580
1501
DQS
324

FIG. 15

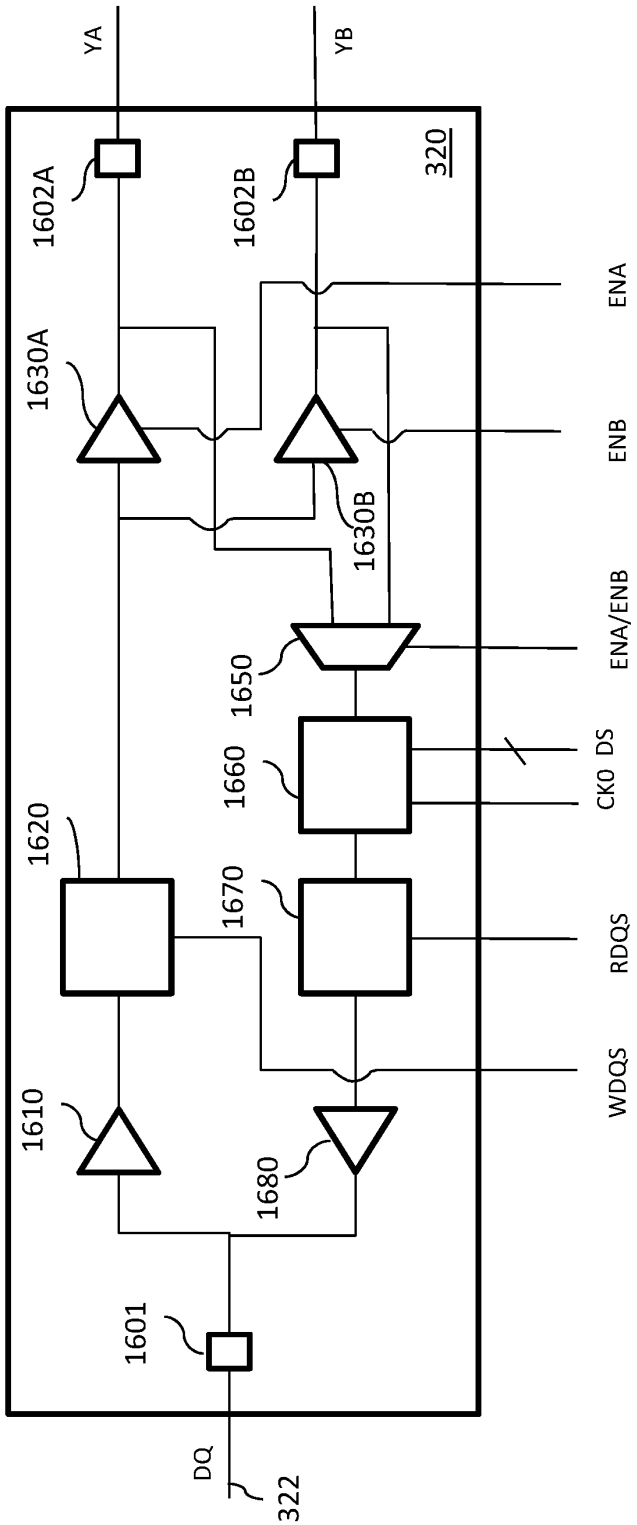

YA
YB
320
1602A
1602B
ENA
1630A
ENB
1630B
ENA/ENB
1650
1660
CK0 DS
1620
1670
RDQS
WDQS
1610
1680
1601
DQ
322

FIG. 16

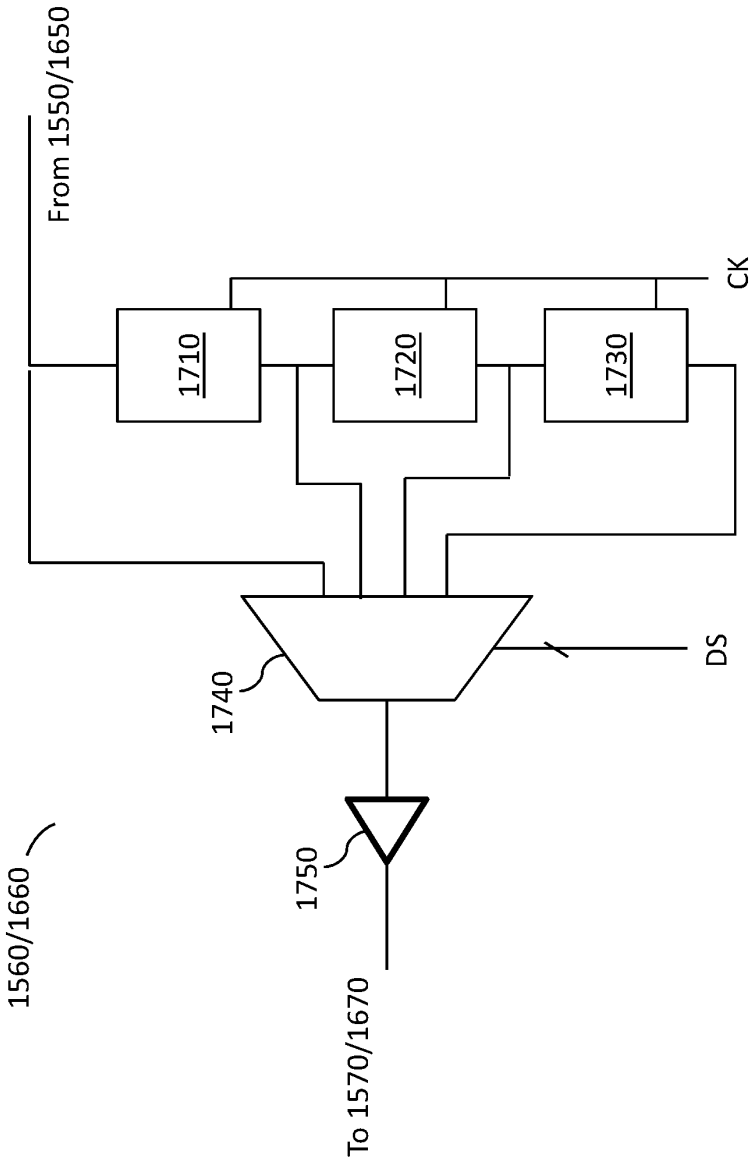

From 1550/1650
CK
1710
1720
1730
DS
1740
1750
1560/1660
To 1570/1670

FIG. 17

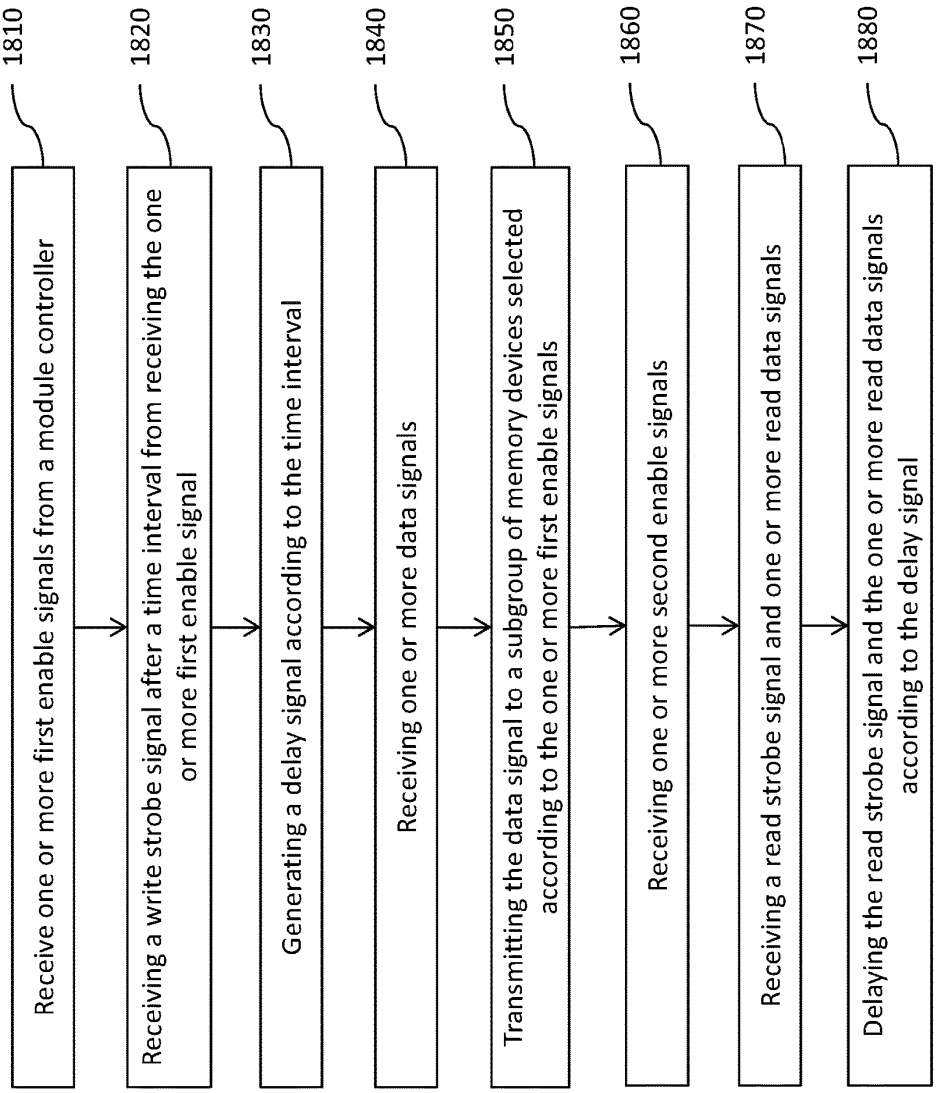

1810
Receive one or more first enable signals from a module controller
1820
Receiving a write strobe signal after a time interval from receiving the one or more first enable signal
1830
Generating a delay signal according to the time interval
1840
Receiving one or more data signals
1850
Transmitting the data signal to a subgroup of memory devices selected according to the one or more first enable signals
1860
Receiving one or more second enable signals
1870
Receiving a read strobe signal and one or more read data signals
1880
Delaying the read strobe signal and the one or more read data signals according to the delay signal

FIG. 18

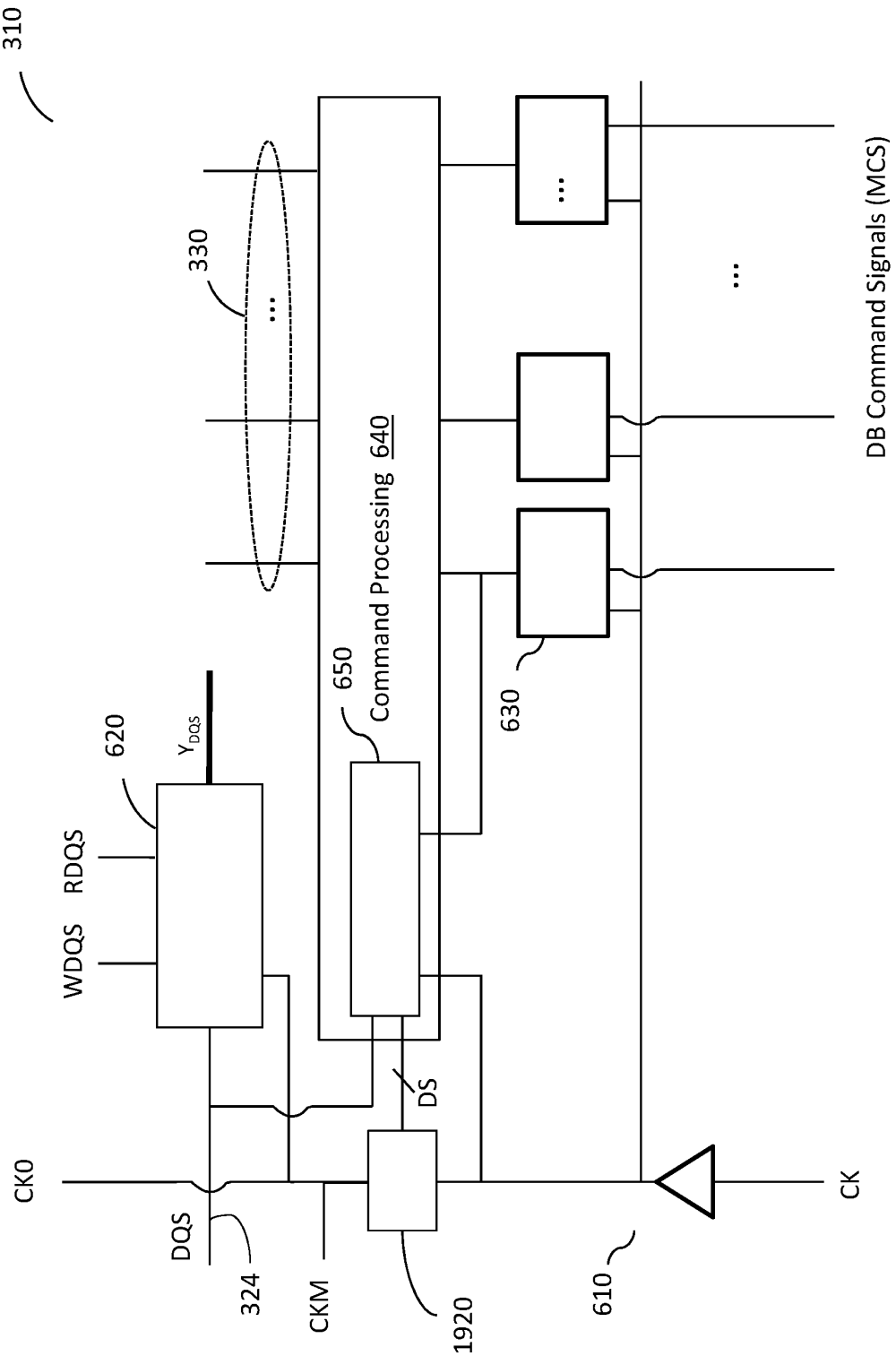

310
330
650
Command Processing 640
630
620
Y_{DQS}
RDQS
WDQS
DS
CK0
DQS
324
CKM
1920
610
CK
DB Command Signals (MCS)

FIG. 19

MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING

CLAIM OF PRIORITY

The present application is a continuation of U.S. patent application Ser. No. 15/820,076, filed Nov. 21, 2017, which is a continuation of U.S. patent application Ser. No. 15/426,064, filed Feb. 7, 2017 (U.S. Pat. No. 9,824,035), which is a continuation of U.S. patent application Ser. No. 14/846,993, filed Sep. 7, 2015 (U.S. Pat. No. 9,563,587), which is a continuation of U.S. patent application Ser. No. 13/952,599, filed Jul. 27, 2013, (U.S. Pat. No. 9,128,632), which claims priority to U.S. Provisional Pat. Appl. No. 61/676,883, filed on Jul. 27, 2012. Each of the above applications is incorporated herein by reference in its entirety.

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is related to commonly-owned U.S. patent application Ser. No. 14/715,486, filed on May 18, 2015; U.S. patent application Ser. No. 13/970,606, filed on Aug. 20, 2013, now U.S. Pat. No. 9,606,907; U.S. patent application Ser. No. 12/504,131, filed on Jul. 16, 2009, now U.S. Pat. No. 8,417,870; U.S. patent application Ser. No. 12/761,179, filed on Apr. 15, 2010, now U.S. Pat. No. 8,516,185; U.S. patent application Ser. No. 13/287,042, filed on Nov. 1, 2011, now U.S. Pat. No. 8,756,364; and U.S. patent application Ser. No. 13/287,081, filed on Nov. 1, 2011, now U.S. Pat. No. 8,516,188; each of which is incorporated herein by reference in its entirety.

FIELD

The disclosure herein is related generally to memory modules, and more particularly to multi-rank memory modules and methods of operation.

BACKGROUND

With recent advancement of information technology and widespread use of the Internet to store and process information, more and more demands are placed on the acquisition, processing, storage and dissemination of vocal, pictorial, textual and numerical information by microelectronics-based combination of computing and communication means. In a typical computer or server system, memory modules are used to store data or information. A memory module usually includes multiple memory devices, such as dynamic random access memory devices (DRAM) or synchronous dynamic random access memory devices (SDRAM), packaged individually or in groups, and/or mounted on a printed circuit board (PCB). A processor or a memory controller accesses the memory module via a memory bus, which, for a single-in-line memory module (SIMM), can have a 32-bit wide data path, or for a dual-in-line memory module (DIMM), can have a 64-bit wide data path.

The memory devices of a memory module are generally organized in ranks, with each rank of memory devices generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x64" or "by 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x72" or "by 72" organization.

The memory capacity or memory density of a memory module increases with the number of memory devices on the memory module. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks.

In certain conventional memory modules, the ranks are selected or activated by control signals from a processor or memory controller during operation. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support a limited number of ranks per memory module, which limits the memory density of the memory modules that can be used in these computer and server systems.

For memory devices in such as a memory module to be properly accessed, distribution of control signals and a control clock signal in the memory module is subject to strict constraints. In some conventional memory modules, control wires are routed so there is an equal length to each memory component, in order to eliminate variation of the timing of the control signals and the control clock signal between different memory devices in the memory modules. The balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections.

In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagram illustrating a memory system including at least one memory module according to one embodiment.

FIGS. **2**A-**2**D are each a diagrams illustrating interactions among components in a a memory module according to certain embodiments.

FIG. **3** is a diagram illustrating one of a plurality of data buffers in a memory module according to one embodiment.

FIGS. **4**A-**4**B are each a diagram illustrating data and data strobe signal lines coupled to memory devices in a memory module according to certain embodiments.

FIGS. **5**A-**5**B are diagrams illustrating different numbers of memory devices that can be coupled to each data buffer in a memory module according to certain embodiments.

FIG. **6** is a diagram illustrating a control circuit in a data buffer according to certain embodiments.

FIG. **7** is a diagram illustrating control signals from a module control device to a plurality of data buffers in a memory module according to certain embodiments.

FIG. **8** is a timing diagram illustrating alignment of module control signals with respect to module clock signals.

FIG. **9** is a diagram illustrating a metastability detection circuit and signal adjustment circuit in a data buffer according to certain embodiments.

FIGS. **10**A-**10**C are diagrams illustrating a metastability detection circuit according to certain embodiments.

FIG. **10**D is a diagram illustrating a signal adjustment circuit according to certain embodiments.

FIGS. **11**A-**11**B are diagrams illustrating a metastability detection circuit and signal adjustment circuit, respectively, according to certain embodiments.

FIGS. **12**A-**12**B are a timing diagrams illustrating a write operation and a read operation, respectively, performed by a memory module according to one embodiment.

FIG. **13** is a diagram illustrating a delay control circuit in a data buffer according to certain embodiments.

FIG. **14** is a diagram illustrating a DQ or DQS routing circuit in a data buffer according to an embodiment.

FIG. **15** a diagram illustrating a DQS routing circuit having a delay circuit in a data buffer according to an embodiment.

FIG. **16** a diagram illustrating a DQ routing circuit having a delay circuit in a data buffer according to an embodiment.

FIG. **17** is a diagram illustrating a delay circuit in a DQ or DQS routing circuit according to an embodiment.

FIG. **18** is a flowchart illustrating a method for data edge alignment according to embodiments.

FIG. **19** is a diagram illustrating a control circuit in a data buffer according to certain embodiments.

DESCRIPTION OF EMBODIMENTS

A memory module according to one embodiment includes memory devices organized in groups, a module control device, and data buffers (DB). The data buffers are sometimes referred to herein as buffer circuits, isolation devices (I.D.) or load reduction devices. The memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals. The memory controller may also transmit a system clock signal to the memory module. In one embodiment, the C/A signals and the system clock signal are received by the module control device, which generates a set of module command signals and a set of module control signals in response to each memory command from the memory controller. The module command signals are transmitted by the module control device to the memory devices via module C/A signal lines, and the module control signals (referred sometimes herein as module control signals) are transmitted by the module control device to the buffer circuits via module control signal lines.

The buffer circuits are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective groups of memory devices. Thus, during certain high speed operations, each module control signal may arrive at different buffer circuits at different points of time across more than one clock cycle of the system clock. Also, each buffer circuit associated with a respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller. Thus, the memory controller does not have direct control of the memory devices. In one embodiment, each group of memory devices include at least two subgroups, each subgroup including at least one memory device. Each buffer circuit is configured to select a subgroup in the respective group of memory devices to communicate data with the memory controller in response to the module control signals. Thus, the memory module can have more ranks of memory devices than what is supported by the memory controller.

In one embodiment, each buffer circuit includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or a module clock signal to mitigate any metastability condition in the module control signals.

Further, in one embodiment, each buffer circuit includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit and a time when a strobe or data signal is received from the memory controller. This time interval is used during a subsequent read operation to time transmission of read data to the memory controller, such that the read data arrives at the memory controller within a time limit in accordance with a read latency parameter associated with the memory system.

FIG. **1** shows a system **100** including a memory controller (MCH) **101** and one or more memory modules **110** coupled to the MCH by a memory bus **105**, according to one embodiment. As shown, the memory bus includes C/A signal lines **120** and groups of system data/strobe signal lines **130**. Also as shown, each memory module **110** has a plurality of memory devices **112** organized in a plurality of ranks **114**. Each memory module **110** further includes a module control circuit (module controller or module control device) **116** coupled to the MCH **101** via the C/A signal lines **120**, and a plurality of buffer circuits or isolation devices **118** coupled to the MCH **101** via respective groups of system data/strobe signal lines **130**. In one embodiment, the memory devices **112**, the module control circuit **116** and the isolation devices **118** can be mounted on a same side or different sides of a printed circuit board (module board) **119**.

In the context of the present description, a rank refers to a set of memory devices that are selectable by a same chip select signal from the memory controller. The number of ranks of memory devices in a memory module **110** may vary. For example, as shown, each memory module **110** may include four ranks of memory devices **112**. In another embodiment, the memory module **110** may include 2 ranks of memory devices. In yet another embodiment, the memory module may include six or more ranks of memory devices **112**.

In the context of the present description, a memory controller refers to any device capable of sending instructions or commands, or otherwise controlling the memory devices **112**. Additionally, in the context of the present description, a memory bus refers to any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller. For example, in various embodiments, the memory bus **105** may include printed circuit board (PCB) transmission lines, module connectors, component packages, sockets, and/or any other components or connections that provide connections for signal transmission.

Furthermore, the memory devices **112** may include any type of memory devices. For example, in one embodiment, the memory devices **112** may include dynamic random access memory (DRAM) devices. Additionally, in one embodiment, each memory module **110** may include a dual in-line memory module (DIMM).

Referring to FIG. **2**A, which illustrates one memory module **110** according to an embodiment, the module control device **116** receives system memory commands repre-

sented by a set of system control/address (C/A) signals from the MCH **101** via signal lines **120** and generates module command signals and module control signals based on memory commands from the system. The module control device **116** also received a system clock MCK and generates a module clock signal CK in response to the system clock signal MCK. The MCK signal may include a pair of complementary clock signals, MCK and $\overline{\text{MCK}}$, and the module clock signal may include a pair of complementary clock signals CK and $\overline{\text{CK}}$.

Examples of the system C/A signals include, but are not limited to, Chip Select (or /CS) signal, which is used to select a rank of memory devices to be accessed during a memory (read or write) operation; Row Address Strobe (or /RAS) signal, which is used mostly to latch a row address and to initiate a memory cycle; Column Address Strove (or /CAS) signal, which is used mostly to latch a column address and to initiate a read or write operation; address signals, including bank address signals and row/column address signals, which are used to select a memory location on a memory device or chip; Write Enable (or /WE) signal, which is used to specify a read operation or a write operation, Output Enable (or /OE) signal, which is used to prevent data from appearing at the output until needed during a read operation, and the system clock signal MCK.

Examples of module command signals include, but are not limited to module/CS signals, which can be derived from the system /CS signals and one or more other system C/A signals, such as one or more bank address signals and/or one or more row/column address signals; a module /RAS signal, which can be, for example, a registered version of the system /RAS signal; a module /CAS signal, which can be, for example, a registered version of the system /CAS signal; module address signals, which can be, for example, registered versions of some or all of the address signals; a module /WE signal, which can be, for example, a registered version of the system /WE signal; a module /OE signal, which can be, for example a registered version of the system /OE signal. In certain embodiments, the module command signals may also include the module clock signal CK.

Examples of module control signals include, but are not limited to a mode signal (MODE), which specifies a mode of operation (e.g., test mode or operating mode) for the isolation devices **118**; one or more enable signals, which are used by an isolation device to select one or more subgroups of memory devices to communicate data with the memory controller; and one or more ODT signals, which are used by the isolation devices to set up on-die termination for the data/strobe signals. In one embodiment, the module control signals are transmitted to the isolation devices **118** via respective module control signal lines **230**. Alternatively, the module control signals can be packetized before being transmitted to the isolation devices **118** via the module control signal lines and decoded/processed at the isolation devices.

Module control device **116** transmits the module command signals to the memory devices **112** via module C/A signal lines **220**. The memory devices **112** operate in response to the module command signals to receive write data or output read data as if the module command signals were from a memory controller. The module control device transmits the module control signals together with the module clock signal CK to the isolation devices **118** via module control signal lines **230**. As shown in FIG. **2**, at least some of the memory devices in a same rank share a same set of module C/A signal lines **220**, and at least some of the isolation devices **118** share a same set of module control signal lines **230**.

As shown n FIGS. **2**A and **2**B, each rank **114** includes N memory devices, where N is an integer larger than one. For example, a first rank includes memory devices M_{11}, . . . , M_{i1}, $M_{i+1,1}$, . . . , M_{N}, a second rank includes memory devices M_{12}, . . . , M_{i2}, $M_{i+1,2}$, . . . , $M_{N,2}$, and so on. In one embodiment, the memory devices **112** are also organized in groups or sets, with each group corresponding to a respective group of system data/strobe signal lines **130** and including at least one memory device from each rank. For example, memory devices M_{11}, M_{12}, M_{13}, and M_{14} form a first group of memory devices, memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4} form an ith group of memory devices, and so on.

As shown, the isolation devices **118** are associated with respective groups of memory devices and are coupled between respective groups of system data/strobe signal lines **130** and the respective groups of memory devices. For example, isolation device ID-**1** among the isolation devices **118** is associated with the first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14} and is coupled between the group of system data/strobe signal lines **130-1** and the first group of memory devices, isolation devices ID-i among the isolation devices **118** is associated with the ith group of memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4} and is coupled between the group of system data/strobe signal lines **130-***i* and the ith group of memory devices, and so on.

In one embodiment, each group or sets of memory devices are coupled to the associated isolation device **118** via a set of module data/strobe lines **210**. Each group or set of memory devices is organized in subgroups or subsets, with each subgroup or subset including at least one memory device. The subgroups in a group of memory devices may be coupled to the associated isolation device **118** via a same set of module data/strobe lines **210** (as shown in FIG. **2**A) or via respective subsets of module data/strobe lines **210** (as shown in FIG. **2**B). For example, as shown in FIG. **2**B, in the first group of memory devices, memory devices M_{11} and/or M_{13} form a first subgroup, and memory devices M_{12} and/or M_{14} form a second subgroup; in the ith group of memory devices, memory devices M_{i1} and/or M_{i3} form a first subgroup, and memory devices M_{i2} and/or M_{i4} form a second subgroup; and so on. The first subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device **118** via an associated first subset of module data/strobe lines YA, and the second subgroup of at least one memory device in each group of memory devices is coupled to the associated isolation device via an associated second subset of module data/strobe lines YB, as shown. For example, memory devices M_{11} and/or M_{13} form the first subgroup are/is coupled to the isolation device ID-**1** via the corresponding first subset of module data/strobe lines YA-**1**, and memory devices M_{12} and/or M_{14} form the second subgroup are/is coupled to the isolation device ID-**1** via the corresponding second subset of module data/strobe lines YA-**2**.

In one embodiment, the isolation devices **118** are in the data paths between the MCH **101** and the memory module **110** and include data buffers between the MCH **101** and the respective groups of memory devices. In one embodiment, each isolation device **118** is configured to select a subgroup in the respective group of memory devices to communicate data with the MCH **101** in response to the module control signals, such that the memory module can include more ranks than what is supported by the MCH **101**. Further, each

isolation devices **118** is configured to isolate unselected subgroup(s) of memory devices from the MCH **101** during write operations, so that the MCH sees a load on each data line that is less than a load associated with the respective group of memory devices. In one embodiment, the MCH sees only a load associated with one memory device on each data/strobe signal line during write operations.

In one embodiment, the isolation devices **118** are distributed across the memory module **110** or the module board **119** in positions corresponding to the respective groups of memory devices. For example, isolation device ID-**1** is disposed in a first position corresponding to the first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14}, and isolation device ID-i is disposed in an ith position separate from the first position and corresponding to the ith group of memory devices M_{i1}, M_{i2}, M_{i3}, and M_{i4}. In one embodiment, the first position is between the first group of memory devices and an edge **201** of the module board **119** where connections (not shown) to the data/strobe signal lines **130** are placed, and i^{th} position is between the ith group of memory devices and the edge **201** of the module board **119**. In one embodiment, the isolation devices **118** are distributed along the edge **201** of the memory module **110**. In one embodiment, each isolation device **118** is a separate integrated circuit device packaged either by itself or together with at least some of the respective group of memory devices. In one embodiment, the module data/strobe signal lines **210**, the module C/A signal lines **220**, and the module control signal lines **230** include signal traces formed on and/or in the module board **119**.

As an option, memory module **110** may further include a serial-presence detect (SPD) device **240**, which may include electrically erasable programmable read-only memory (EEPROM) for storing data that characterize various attributes of the memory module **110**. Examples of such data include a number of row addresses, a number of column addresses, a data width of the memory devices, a number of ranks on the memory module **110**, a memory density per rank, a number of memory device on the memory module **110**, and a memory density per memory device, etc. A basic input/output system (BIOS) of system **100** can be informed of these attributes of the memory module **110** by reading from the SPD **240** and can use such data to configure the MCH **101** properly for maximum reliability and performance.

In certain embodiments, the SPD **240** and/or the control circuit **116** store module configuration information, such as: memory space translation code, memory address mapping function code, input and output signals timing control information for the control circuit **116**, input and output signals electrical and logical level control information for the control circuit **116**, etc. In certain embodiments, the SPD **240** contains a system view of the module **110** which can be different from an actual physical construction of the module **110**. For example, the SPD **240** stores at least one memory operation parameter that is different from a corresponding memory operation parameter in a system memory controller setting. The SPD **240** may also store at least on data buffer operation parameter that is different from a corresponding parameter in the system memory controller setting.

Thus, in certain embodiment, in the memory module **110**, C/A signals representing a memory command are received and buffered by the module control circuit **116**, so that the MCH sees only the module control circuit **116** as far as the C/A signals are concerned. Write data and strobe signals from the controller are received and buffered by the isolation devices **118** before being transmitted to the memory devices **112** by the isolation devices **118**. On the other hand, read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines **130**. Thus, MCH **101** does not directly operate or control the memory devices **112**. As far as data/strobe signals are concerned, the MCH **101** mainly sees the isolation devices **118**, and the system **100** depends on the isolation devices **118** to properly time the transmission of the read data and strobe signals to the MCH **101**.

In certain embodiments, the memory module **110** is a dual in-line memory module (DIMM) and the memory devices are double data rate (DDR) dynamic random access memory devices (DRAM). In certain embodiments, the control circuit **116** includes a DDR register, and logic for memory space translation between a system memory domain and a module level physical memory domain. Such translation may produce address mapping, proper interface timing for the control signals to the module level physical memory domain, and a proper interface electrical and logical level for the control signals to the module level physical memory domain.

As shown in FIG. **2**C, in certain embodiments, the control circuit **116** transmits registered C/A and clock signals to the memory devices **112**, and transmits module control signals and a registered clock signal (or module clock signal) to the isolation devices **118**, in a fly-by configuration. As the speed of memory operations increase, issues can arise with respect to signal alignment for input, output delay variation due process, voltage and temperature (PVT) variations, synchronization with system memory controller interface, and phase drift accumulation during operation, etc. Electrical interface calibration drift during operation due to charge build up and timing interface calibration drift during operation due to environment change can also create issues.

For example, load reduction mechanism in the isolation devices **118** would provide a single data bus interface to the respective set of memory devices, which is hidden from the system memory controller **101**. Thus, a long sequence of interface timing training may be required due to limited controllability of the system memory controller **101** over the interface between the memory devices **112** and the associated isolation devices **118**. Furthermore, interface signal alignment-drift after the initial training would not be easily detected by the system memory controller **101**, which may cause silent system failure.

Moreover, clock skew amongst the memory devices **112** and the associated isolation devices **118** due to the distributed architecture of the memory module **110** can cause synchronization issues. As the speed of memory operation increase, data period can become very close to the signal propagation delay time. Thus, such issues cannot simply be addressed by pipelining the data paths, as variation of the signal propagation time through I/Os becomes a very significant portion of a data period.

To address at least some of the above issues, in certain embodiments, as shown in FIG. **2**D, the control circuit **116** transmits registered C/A signals to the memory devices **112**, and transmits the module control signals and the module clock signal to the data buffers **118**, in a fly-by arrangement. The memory devices **112** do not receive the module clock signal from the control circuit **116**. Instead, each data buffer **118** regenerates the clock that is used by the respective set of memory devices **112**. Each Data buffer **118** is thus responsible for providing a correct data timing interface between the respective set of memory devices **112** and the system memory controller **101**. Each data buffer **118** is also

responsible for providing the correct control signal timing between the control circuit **116** and the respective set of memory devices **112**.

Thus, the memory module **110** in FIG. **2**D allows a locally synchronized operation for each respective set of memory devices **112**, which can correspond to a nibble or a byte of a DDR data bus between the memory module **110** and the system memory controller **101**. Also, signal interface between each data buffer **118** and the respective set of memory devices **112** can be synchronized. In one embodiment, each data buffer **118** has a set of configurable operations, including, for example: programmable phase relationship between the clock it receives and the clock it regenerates, programmable phase adjustment for the data and data-strobe signals coupled to the memory devices **112**, programmable phase adjustment for the data and data-strobe signals coupled to the system memory controller **101**, programmable phase adjustment related to at least one control signal that is coupled to the control circuit **116**. The locally synchronized operation also makes it easier for each data buffer **118** to perform self-testing of the associated set of memory devices **112**, independent of the self-testing of other sets of memory devices performed by the other data buffers, as disclosed in commonly-owned U.S. Pat. No. 8,001,434, entitled "Memory Board with Self-Testing Capability," which is incorporated herein by reference in its entirety.

In certain embodiments, operations of the isolation devices **118** are controlled by the module control signals from the module control circuit **116**, which generates the module control signals according to the C/A signals received from the MCH. Thus, the module control signals need to be properly received by the isolation devices **118** to insure their proper operation. In one embodiment, the module control signals are transmitted together with the module clock signal CK, which is also generated by the module control circuit **116** based on the system clock signal MCK. The isolation circuits **118** buffers the module clock signal, which is used to time the sampling of the module control signals. Since the isolation devices **118** are distributed across the memory module, the module control signal lines **230** can stretch across the memory module **110**, over a distance of several centimeters. As the module control signals travel over such a distance, they can become misaligned with the module clock signal, resulting in metastability in the received module control signals. Therefore, in one embodiment, the isolation circuits **118** includes metastability detection circuits to detect metastability condition in the module control signals and signal adjustment circuits to adjust the module control signals and/or the module clock signal to mitigate any metastability condition in the module control signals, as explained in further detail below.

Because the isolation devices **118** are distributed across the memory module **110**, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines **230** from the module control device **116** to the farthest positioned isolation devices **118**, such as isolation device ID-**1** and isolation device ID-(n−1) in the exemplary configuration shown in FIG. **2**. In other words, a same set of module control signals may reach different isolation devices **118** at different times across more than one clock cycle of the system clock. For example, when the clock frequency of the system clock is higher than 800 MHz, the clock cycle time is less than about 1.2 ns. With a signal travel speed of about 70 ps per centimeter of signal line, a module control signal would travel about 15 cm during one clock cycle. When the clock frequency increases to 1600 MHz, a module control signal would travel less than 8 cm during one clock cycle. Thus, a module control signal line can have multiple module control signals on the line at the same time, i.e., before one module control signal reaches an end of the signal line, another module control signal appear on the signal line.

With the isolation devices **118** receiving module control signals at different times across more than one clock cycle, the module control signals alone are not sufficient to time the transmission of read data signals to the MCH **101** from the isolation devices **118**. In one embodiment, each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit **116** and a time when a write strobe or write data signal is received from the MCH **101**. This time interval is used during a subsequent read operation to time the transmission of read data to the MCH **101**, such that the read data follows a read command by a read latency value associated with the system **100**, as explained in more detail below.

More illustrative information will now be set forth regarding various optional configurations, architectures, and features with which the foregoing framework may or may not be implemented, per the desires of the user. It should be strongly noted that the following information is set forth for illustrative purposes and should not be construed as limiting in any manner. Any of the following features may be optionally incorporated with or without the exclusion of other features described.

In one embodiment, as shown in FIG. **3**, each group of signal lines **130** include a set of n data (DQ) signal lines **322** each for transmitting one of a set of data signals DQ_0, DQ_1, . . . , DQ_{n-1}, and at least one strobe (DQS) signal line **324** for transmitting at least one strobe signal DQS. Each set of module data/strobe lines Y include a set of n module data signal lines Y_0, Y_1, . . . , Y_{n-1} and at least one module strobe signal line Y_{DQS}. When the subsets of memory devices are coupled to the associated isolation device **118** via respective subsets of memory devices, each set of module data/strobe lines Y may include multiple subsets of module data/strobe lines, such as the subsets of module data/strobe lines YA and YB shown in FIG. **2**B. Each subset of module data/strobe lines YA include a set of n first module data lines YA_0, YA_1, . . . , YA_n and at least one first module strobe signal line YA_{DQS}; and each subset of module data/strobe lines YB include a set of n second module data lines YB_0, YB_1, . . . , YB_n and at least one second module strobe signal line YB_{DQS}.

Each isolation device **118** includes a set of DQ routing circuits **320** coupled on one side to respective ones of the set of n DQ signal lines **322**, and on another side to respective ones of the respective set of n module data lines, or respective ones of the respective subsets of module data lines, such as the first module data lines YA_0, YA_1, . . . , YA_n and the second module data lines YB_0, YB_1, . . . , YB_n. Each isolation device **118** further includes an ID control circuit **310** coupled on one side to the at least one DQS signal line **324**, on another side to the one or more module strobe signal lines Y_{DQS}, or the first module strobe signal line YA_{DQS} and second module strobe signal line YB_{DQS}. The ID control circuit **310** also receives the module clock signal CK and the module control signals via the module control signal lines **230**, and outputs ID control signals **330** to the DQ routing circuits **320**, including, for example, one or more enable signals ENA and/or ENB, and some or all of the other received, decoded, and/or otherwise processed module con-

trol signals, a delay signal DS, a read DQS signal RDQS, a write DQS signal WDQS, and a buffer clock signal CK**0**. Each DQ routing circuit **320** is configured to enable data communication between the respective DQ signal line **322** with a selected subgroup of one or more memory devices in response to the module control signals, as explained in more detail below.

In certain embodiments, the ID control circuit **310** also provides a delay signal DS, which is used by the DQ routing circuits **320** to align read data output by the isolation device **118** with read data output by the other isolation devices **118**, as explained in further detail below. In certain embodiments, the ID control circuit **310** regenerates a clock signal from the module clock signal CK, which can have a programmable delay from the module clock signal. The regenerated clock signal is used as the clock signal CK**0** and a clock signal CKM that is provided to the corresponding set of memory devices, as explained in more detail below.

The memory devices **112** are coupled to the isolation devices **118** via a same set of module data/strobe signal lines or different subsets of module data/strobe signal lines. For example, as shown in FIG. **4**A, memory devices M_{11}, M_{12}, M_{13}, and M_{14} in the first group of memory devices can be coupled to the isolation device ID-**1** via a same set of module data lines Y-$\mathbf{1}_0$, Y-$\mathbf{1}_1$, . . . , Y-$\mathbf{1}_{n-1}$ and module strobe line Y-$\mathbf{1}_{DQS}$. In such embodiment, a subgroup in the group of memory devices can be selected by the isolation devices to communicated data with the MCH based on the phases of the data/strobe signals, which can be different with respect to different subgroups of memory devices.

Alternatively, as shown in FIG. **4**B, memory devices M_{11} and M_{13}, which form a subgroup in the first group of memory devices, are coupled to the isolation device ID-**1** via the module data lines YA-$\mathbf{1}_0$ YA-$\mathbf{1}_1$, . . . , YA-$\mathbf{1}_n$ and module strobe line YA-$\mathbf{1}_{DQS}$ and memory devices M_{12} and M_{14}, which form another subgroup in the first group of memory devices, are coupled to the isolation device ID-**1** via the module data lines YB-1_0, YB-1_1, . . . , YB-1_n and module strobe line YB-1_{DQS}. Memory devices coupled to the same isolation devices can be disposed on a same side or different sides of the memory board **119**. Memory devices coupled to the same isolation devices may be placed side by side, on opposite sides of the module boards **119**, or stacked over each other, and/or over the associated isolation device.

Multiple memory devices having a data width that is less than a data width of the isolation devices **118** may be used in place of one of the memory devices **112**, which has the same data width as that of the isolation devices. For example, as shown in FIG. **5**A, two memory devices $M_{11\text{-}1}$ and $M_{11\text{-}2}$ may be used in place of the memory device M_{11}. Each of the two memory devices $M_{11\text{-}1}$ and $M_{11\text{-}2}$ has a data width of 4, and together they act like a memory device M_{11} of a data width of 8. Thus, memory device $M_{11\text{-}1}$ is coupled to the isolation device ID-**1** via module data lines YA-$\mathbf{1}_0$, . . . , YA-$\mathbf{1}_3$ and module strobe line YA-$\mathbf{1}_{DQS\text{-}1}$ while memory circuit $M_{11\text{-}2}$ is coupled to the isolation device ID-**1** via module data lines YA-$\mathbf{1}_4$, . . . , YA-$\mathbf{1}_7$ and module strobe line YA-$\mathbf{1}_{DQS\text{-}2}$.

In another embodiment, as shown in FIG. **5**B, four memory devices $M_{11\text{-}1}$ to $M_{11\text{-}4}$ may be used as the memory device M_{11}. Each of the four memory devices $M_{11\text{-}1}$ to $M_{11\text{-}4}$ has a data width of 4, and together they act like a memory device M_{11} of a data width of 16. Thus, memory device $M_{11\text{-}1}$ is coupled to the isolation device ID-**1** via module data lines YA-$\mathbf{1}_0$, . . . , YA-$\mathbf{1}_3$ and module strobe line YA-$\mathbf{1}_{DQS\text{-}1}$ while memory device $M_{11\text{-}2}$ is coupled to the isolation device ID-**1** via module data lines YA-$\mathbf{1}_4$, . . . , YA-$\mathbf{1}_7$ and module strobe line YA-$\mathbf{1}_{DQS\text{-}2}$, and so on.

FIG. **6** illustrates the ID control circuit **310** in an isolation device **118**. As shown, the ID control circuit **310** includes a clock buffer **610** to receive the module clock signal CK from the module control device **116**, and to output a module clock signal CK**0**. The ID control circuit **310** further includes a strobe routing circuit **620** that are coupled on one side to the corresponding system DQS signal line **324** and on another side to the corresponding module DQS signal lines YA_{DQS} and YB_{DQS}. The ID control circuit **310** further includes a receiver circuit **630** with respect to each of at least some of the module control signals (MCS) to receive a respective one of the module control signals. The ID control circuit **310** further includes a command processing circuit **640** that provides the received, decoded, and/or otherwise processed module control signals **330** to the DQ routing circuits **320** and the strobe routing circuit **620** either directly or after further processing, if needed. The received/decoded/processed module control signals may include, for example, one or more enable signals ENA and/or ENB that are used by the DQ routing circuits **320** and the strobe routing circuit **620** to selectively enabling data communication between the MCH **101** and one of the subgroups in the respective group of memory devices, with which the isolation device is associated.

The strobe routing circuit **620** also buffers strobe signals received from either the MCH **101** or the memory devices **112**, and output either a write strobe WDQS or read strobe RDQS to the DQ routing circuits **320**. In one embodiment, the ID control circuit **310** further includes a delay control circuit **650** that receives one of the module control signals and either a data signal or a strobe signal and determines a delay amount to be used by the DQ routing circuit **320** and the strobe routing circuit **620**. The delay amount is provided to the DQ routing circuit **320** and the strobe routing circuit in a delay signal DS.

In a receiver circuit **630**, the respective MCS is received in accordance with the module clock signal CK**0**. In one embodiment, receiver circuit **630** samples the respective MCS using rising (or falling) edges of the module clock CK**0**. Since the isolation devices **118** are distributed across the memory module **110** at positions corresponding to the respective groups of memory devices, the module control signal lines **230** that carry the MCS to the isolation devices can stretch over a distance of more than 10 centimeters, as shown in FIG. **7**. As the MCS and CK**0** travel along their respective module control signal lines **710** and **720**, they can become misaligned with each other when they reach the input pins **730** of an isolation device **118**.

For example, a module control signal, like the MCS **810** shown in FIG. **8**, can be perfectly aligned with the module clock signal CK, with a rising edge **801** of the module clock signal CK being at a center of a data eye **802**, when the MCS signal and the clock signal leave the module control circuit **116**. When the module control signal and the module clock signal reach an isolation device, however, their alignment can become shifted like the MCS **820** with respect to the CK signal, i.e., the rising edge **801** of the clock signal is near a left edge of a data eye of the MCS **820**, barely providing enough set up time for proper sampling of the module control signal. Or, the module control signal, like the MCS **830**, can be shifted with respect to the module clock signal such that a rising edge **801** of the clock signal is near a right edge of a data eye of the MCS, barely providing enough hold time for proper sampling of the module control signal. Or, ever worse, the module control signal, like the MCS **840**,

can be so shifted with respect to the module clock signal such that a rising edge **801** of the clock signal falls in the glitches **803** at the edge of a data eye of the MCS, meaning that the sampled results could be metastable.

In one embodiment, as shown in FIG. **9**, a receiver circuit **630** includes a metastability detection circuit (MDC) **910** to determine a metastability condition in a corresponding module control signal MCS**0**. In one embodiment, the MDC **910** generates at least one delayed version of the module clock signal CK and at least one delayed version of the corresponding MCS**0**. The MDC **910** also generates one or more metastability indicators and outputs the one or more metastability indicators via lines **912** and/or **914**.

The receiver circuit **630** further includes a signal selection circuit **920** that receives the module clock CK and the at least one delayed version of the module clock via signal lines **916**. The signal selection circuit **920** also receives the corresponding MCS and the at least one delayed version of the corresponding MCS via signal lines **918**. The signal selection circuit **920** selects a clock signal CK, from among the module clock CK and the at least one delayed version of the module clock based on one or more of the metastability indicators. The signal selection circuit **920** may also select an MCS signal MCS, from among the corresponding MCS and the at least one delayed version of the corresponding MCS based on at least one other metastability indicator.

The receiver circuit **630** further includes a sampler or register circuit **930** that samples the selected module control signal MCS, according to the selected clock signal CK, and outputs the sampled signal as the received module control signal, which is provided to the command processing circuit **640** for further processing (if needed) before being provided to the DQ routing circuits **320** and DQS routing circuit **620**.

FIG. **10**A illustrates an MDC **910** according to one embodiment. As shown, the MDC **910** includes a delay circuit **1012** that generates a delayed version MCS**1** of the corresponding MCS**0** by adding a predetermined amount of delay (e.g., lops) to MCS**0**. MDC **910** also includes a delay circuit **1016** that generates a delayed version CK**1** of the clock signal CK**0** by adding a predetermined amount of delay to CK**0**. In one embodiment, CK**1** is delayed from CK**0** by about 1/10th of a clock cycle, e.g., 50-70 ps for an operating frequency of about 1600 MHz. The MDC **910** further includes a sampler circuit **1042** that samples MCS**1** according to CK**0** and outputs a sampled result A, a sampler circuit **1044** that samples MCS**0** according to CK**0** and outputs a sampled result B, and a sampler circuit **1046** that samples MCS**0** according to CK**1** and outputs a sampled result C. The MDC **910** further includes a logic circuit (e.g., a majority decision circuit) that generates metastability indicators Z**1** and Z**2** based on the sampled results A, B, and C.

In one embodiment, Z**1** is the result of a logic operation (e.g., an XNOR operation) on the sampled result, e.g., Z**1**=$\overline{A \oplus B}$, and Z**2** is the result of another logic operation on the sampled results, e.g., Z**2**=$\overline{B \oplus C}$. Thus, as shown in FIG. **10**B and Table 1 below, when a metastability condition of insufficient hold time occurs, i.e., a rising clock edge **1061** of CK**0** is close to the right side of a data eye where glitches at the edges of the data eyes can make C unpredictable, A and B can be in agreement (i.e., Z**1** is true) while B and C are likely not in agreement (i.e., Z**2** is false). FIG. **10** C illustrates a metastability condition when there is insufficient set-up time. As shown in FIG. **10**C and Table 1 below, a rising clock edge **1061** of CK**0** is close to the left side of a data eye where glitches at the edges of the data eyes can make A unpredictable. Thus, A and B can be in disagreement so Z**1** is false while B and C can be in agreement so Z**2** is true. Not shown in the figures is the situation that all A, B, and C are in agreement, meaning that both the rising clock edge **1061** of CK**0** and the rising clock edge **1062** of CK**1** are near the middle of an MCS**0** data eye so there is no metastability issues and both Z**1** and Z**2** are true, as shown in Table 1.

FIG. **10**D illustrates a signal selection circuit **920** according to an embodiment. As shown, in one embodiment, the signal selection circuit **920** includes a first multiplexor **1071** that selects between CK**0** and CK**1** based on the metastability indicator Z**1**, and a second multiplexor **1072** that selects between MCS**0** and MCS**1** based on the metastability indicator Z**2**. Thus, as shown in Table 1, where a metastability condition of insufficient hold time occurs, Z**1**=1 and Z**2**=0, and MCS**1** is output from multiplexor **1071** while CK**0** is output from multiplexor **1072**. Sampler **930** thus samples MCS**1** according to the rising edges of CK**0**. Thus, more hold time is provided to mitigate the metastability condition since MCS**1** is shifted from MCS**0** toward the right.

On the other hand, where a metastability condition of insufficient set-up time occurs, Z**1**=0 and Z**2**=1, and CK**1** is output from multiplexor **1071** while MCS**0** is output from multiplexor **1072**. Sampler **930** thus samples MCS**0** according to the rising edges of CK**1**. Since CK**1** is shifted from CK**0** toward the right, more set-up time is provided to mitigate the metastability condition.

TABLE 1

Metastability Detection and Signal Selection

Sampler Output			MS Indicators			Signal Selection	
A	B	C	Z1	Z2	MS Condition	CK	MCS
D1	D1	D2	1	0	insufficient hold time	CK0	MCS1
D1	D2	D2	0	1	insufficient set-up time	CK1	MCS0
D1	D1	D1	1	1	no metastability	CK0	MCS0

In the case when no metastability is detected, Z**1**=1 and Z**2**=1, and CK**0** is output from multiplexor **1071** while MCS**0** is output from multiplexor **1072**. So, the unshifted module control signal is sampled according to the unshifted module clock signal.

FIGS. **10**A-**10**D illustrate a relatively simple implementation of the metastability detection circuit (MDC) **910** where only three different sample points are provided to detect metastability condition in the module control signal. In general, the MDC **910** may generate more delayed versions of the module clock signal CK**0** and/or the corresponding module control signal MCS**0**, and may include more sampler circuits to sample any additional delayed versions of the module control signal according to either the module clock signal or one of the delayed versions of the module clock signal. For example, as shown in FIG. **11**A, the MDC **910** can include a plurality of delay circuits **1102** that generate m delayed versions of MCS**0**, e.g., MCS**1**, MCS**2**, . . . MCSm, and m delayed versions of CK**0**, e.g., CK**1**, CK**2**, . . . , CKm. The MDC **910** can include sampler circuits **1104** that sample MCS**0** according to CK**0**, CK**1**, . . . , CKm, respectively, and sampler circuits **1104** that sample MCS**0**, MCS**1**, MCS**2**, . . . MCSm according to CK**0**, respectively. The outputs of the samplers **1104** are provided to a logic circuit **1120**, which determines a metastability condition in MCK**0** based on the sampler outputs using, for

example, a majority decision logic. The logic circuit **1120** outputs a first metastability indicator on line(s) **912** and a second metastability indicator on line(s) **914**.

FIG. **11**B illustrates a signal selection circuit **920** according to an embodiment. As shown, in one embodiment, the signal selection circuit **920** includes a first multiplexor **1171** that selects between CK**0**, CK**1**, . . . , CKm based on the metastability indicator provided on line(s) **912**, and a second multiplexor **1172** that selects between MCS**0**, MCS**1**, . . . , MCSm based on the metastability indicator provided on line(s) **914**, such that the rising edges of the selected clock signal, e.g., Cki, are close to the middle of the respective data eyes in the selected module control signal, e.g., MCSi. The selected signals MCSi and Cki are provided to the sampler **930**, which samples MCSi according to the rising edges of CKi.

As stated above, in certain embodiments, since the isolation devices **118** are in the data paths between the MCH **101** and the respective groups of memory devices **112**, the MCH **101** does not have direct control of the memory devices **112**. Thus, conventional read/write leveling techniques are not sufficient for managing read/write data timing. In one embodiment, the isolation devices **118** includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation, as discussed further below.

FIG. **12**A is a timing diagram for a write operation according to one embodiment. As shown, after a write command W/C associated with the write operation is received by the module control circuit **116** at time t1, the module control circuit **116** outputs one or more enable signals EN at time t2 in response to the write commands. The one or more enable signals are received by an isolation device **118** at time t3, which afterwards receives one or more strobe signal DQS from the MCH **101** at time t4. Note that the same enable signal may be received by another isolation device **118** at time t3', which can be in a different cycle of the system clock MCK from the cycle which t3 is in. The time interval between t4 and t1 is consistent with a write latency W.L. associated with the system **100**, and is controllable by the MCH **101** and knowable to the isolation device **118**. The time interval between t4 and t3, referred to hereafter as an enable-to-write data delay EWD, can be determined by the isolation device **118** since both these signals are received by the isolation device. Based on such determination, the isolation device **118** can have knowledge of the time interval between t3 and t1, referred to hereafter as a command-to-enable delay CED, which can be used by the isolation device **118** to properly time transmission of read data to the MCH, as explained further below.

FIG. **12**B is a timing diagram for a read operation according to one embodiment. As shown, after a read command R/C associated with the read operation is received by the module control circuit **116** at time t5, the module control circuit **116** outputs one or more enable signals EN at time t6 in response to the read commands. The one or more enable signals are received by an isolation device **118** at time t7, which afterwards receives at time t8 read data signals (not shown) and one or more strobe signal DQS from the respective group of memory devices. Note that the same enable signal may be received by another isolation device **118** at time t3', which can be in a different cycle of the system clock MCK from the cycle which t3 is in. Thus, the enable signals alone cannot be used to time the transmission of the read signals by the isolation devices **118**.

With knowledge of the time interval between t7 and t5, which should be about the same as the time interval between t3 and t1, i.e., the command-to-enable delay CED, in certain embodiments, the isolation device can add a proper amount of delay to the read data signals and the one or more DQS signal such that the read data signals and the one or more DQS signal are transmitted at time t9 by the isolation device to the MCH **101** via the respective group of data/strobe signal lines **130**, with the time interval between t9 and t5 being consistent with a read latency R.L. associated with the system **100**.

The time interval between t4 and t3, i.e., the enable to write data delay EWD, is determined by the delay control circuit **650** in the ID control circuit **310**, as shown in FIG. **6**. According to one embodiment, as shown in FIG. **13**, the delay control circuit **650** includes a preamble detector **1310** to detect a write preamble in the DQS, a flip-flop circuit **1320** having an enable input EN receiving one of the module control signals and a clock input CK receiving the buffered module clock signal CK**0**, and a counter circuit **1330** having a Start input receiving the one of the module control signals, a Stop input receiving an output of the flip-flop circuit **1320**. Thus, the output of the counter circuit, i.e., the delay signal DS, would indicate a time interval from when the write preamble is detected and when the one of the module control signal is received.

FIG. **14** illustrates a DQ or DQS routing circuit **320** or **620** according to an embodiment. As shown, the DQ/DQS routing circuit **320**/**620** includes a DQ/DQS pin **1401** that is coupled to the corresponding DQ/DQS signal line **322**/**324**, a set of one or more DQS pins **1402** that is coupled to a corresponding module DQ/DQS line(s) Y/Y_{DQS}, or YA/YA_{DQS} and YB/YB_{DQS}. The DQ/DQS routing circuit **320**/**620** further includes a write strobe buffer **1410** that buffers write data/strobe, and a write data/strobe receiver **1420** that samples the write data/strobe. The DQ/DQS routing circuit **320**/**620** further includes a plurality of write paths **1430** that are selectable or can be selectively enabled by one or more of the module control signals, such as the enable signals ENA and ENB.

The DQS routing circuit further includes a plurality of read paths **1450** that are selectable by the one or more of the module control signals. Output from the selected read path is delayed in a delay circuit **1460** by an amount controlled by the delay signal DS, and sampled by a sampler circuit **1470**. The sampled read data/strobe is transmitted by transmitter **1480** onto the corresponding data/strobe signal line **322**/**324** via the DQ/DQS pin **1401**.

FIG. **15** illustrates a DQS routing circuit **620** according to an embodiment. As shown, the DQS routing circuit **620** includes a first DQS pin **1501** that is coupled to a corresponding DQS signal line **324**, a second DQS pin **1502**A that is coupled to a corresponding module DQS line YA_{DQS}, a third DQS pin **1502**B that is coupled to a corresponding module DQS line YB_{DQS}. The DQS routing circuit **620** further includes a first write strobe path coupled between the first DQS pin **1501** and the second DQS pin **1502**A and a second write strobe path coupled between the first DQS pin **1501** and the third DQS pin **1502**B. The first write strobe path includes a write strobe buffer **1510** that buffers a write strobe, a write strobe receiver **1520** that samples the write strobe according to the buffered module signal CK**0**. The sampled write strobe is provided to the DQ routing circuits **320** as the write strobe WDQS. The first write strobe path further includes a first write strobe transmitter **1530**A that transmits the write strobe to one or more memory devices **112** coupled to the module strobe line YA_{DQS}. The second write strobe path includes the write strobe buffer **1510**, the write strobe receiver **1520**, and a second write strobe trans-

mitter **1530**B that transmits the write strobe to one or more memory devices **112** coupled to the module strobe line YB_{DQS}. The first and second write strobe transmitters, **1530**A and **1530**B, are controlled by two enable signals, ENA and ENB, respectively, such that the first write strobe path and the second write strobe path can be selectively enabled/disabled by the enable signals, ENA and ENB.

The DQS routing circuit further includes a read strobe path coupled between the first DQS pin **1501** and a selected one of the second and third DQS pins **1502**A and **1502**B. In the read strobe path, a select circuit **1550** (e.g., a multiplexor) selects either a read strobe signal received via DQS pin **1502**A or a read strobe signal received via DQS pin **1502**B based on one or both of the enable signals ENA or ENB. The selected read strobe signal is delayed in a delay circuit **1560** by an amount controlled by the delay signal DS, and sampled by a sampler circuit **1570** according to the buffered module clock signal CK**0**. The sampled read strobe is provided to the DQ routing circuits **320** as the read strobe RDQS and is transmitted by transmitter **1580** onto the corresponding strobe signal line **324** via the first DQS pin **1501**.

FIG. **16** illustrates a DQ routing circuit **320** according to an embodiment. As shown, the DQ routing circuit **320** includes a first DQ pin **1601** that is coupled to a corresponding DQ signal line **130**, a second DQ pin **1602**A that is coupled to a corresponding module DQ line YA_{DQ}, a third DQ pin **1602**B that is coupled to a corresponding module DQ line YB_{DQ}. The DQ routing circuit **320** further includes a first write data path coupled between the first DQ pin **1601** and the second DQ pin **1602**A and a second write data path coupled between the first DQ pin **1601** and the third DQ pin **1602**B. The first write data path includes a write data buffer **1610**, a write data receiver **1620** that samples write data according to the write strobe WDQS from the DQS routing circuit **620**, and a first write data transmitter **1630**A that transmits the write data to one or more memory devices **112** coupled to the module data line YA_{DQ}. The second write data path includes the write data buffer **1610**, the write data receiver **1620**, and a second write data transmitter **1630**B that transmits the write data to one or more memory devices **112** coupled to the module data line YB_{DQ}. The first and second write data transmitters, **1530**A and **1530**B, are controlled by two enable signals, ENA and ENB, respectively. Thus, the first write data path and the second write data path can be selectively enabled/disabled by the enable signals, ENA and ENB.

The DQ routing circuit further includes a read data path coupled between the first DQ pin **1601** and a selected one of the second and third DQ pins **1602**A and **1602**B. In the read data path, a select circuit **1650** (e.g., a multiplexor) selects either a read data signal received via DQ pin **1602**A or a read data signal received via DQ pin **1602**B based on one or both of the enable signals ENA or ENB. The selected read data signal is delayed in a delay circuit **1660** by an amount controlled by the delay signal DS. The delayed read data signal is then sampled by a receiver circuit **1670** according to the read strobe RDQS from the DQS routing circuit **620**, and transmitted by transmitter **1680** onto the corresponding data signal line **130** via the first DQ pin **1601**.

FIG. **17** illustrate a delay circuit **1560** or **1660** according to an embodiment. As shown, the delay circuit **1560** or **1660** includes a plurality of delay stages, such as delay stages **1710**, **1720**, and **1730**, each delaying a read data or read strobe signal from the select circuit **1550**/**1650** by a predetermined amount. The delay circuit **1560** or **1660** further includes a select circuit **1740** (e.g., a multiplexor) that selects from among the read data or read strobe signal and the outputs from the delay stages according to the delay signal DS. The output of the select circuit **1740**, is provided to the sampler circuit **1570** or **1670**, either directly or after being buffered by a buffer circuit **1750**.

Thus, as shown in FIG. **18**, in one embodiment, a memory module **110** operates in the memory system **100** according to a method **1800**. In the method, during a write operation, one or more module control signals are received by an isolation device **118** from a module control circuit or module controller **116** (**1810**). The module controller **116** generates the one or more module control signals in response to C/A signals representing a write command from the MCH **101**. The one or more module control signals are used to control the isolation device **118**. For example, the one or more module control signals may include one or more first enable signals to enable a write path to allow write data be communicated to a selected subgroup of memory devices among the group of memory devices coupled to the isolation device **118**. After a time interval from receiving the one or more first enable signals, write data DQ and write strobe DQS are received by the isolation device **118** from the MCH **101** (**1820**). In one embodiment, upon receiving the one or more first enable signal, a counter is started, which is stopped when the write data DQ or write strobe DQS is received. Thus, a time interval EWD between receiving the one or more first enable signals and receiving the write strobe signal DQS is recorded.

Since the time interval between the arrival of the command signals from the MCH **101** and the arrival of the write data/strobe signal DQ/DQS from the MCH **101** is a set according to a write latency parameter associated with the system **100**, the time interval EWD can be used to ascertain a time interval CED between the time when a command signal is received by the memory module **110** and the time when the one or more enable signals are received by the isolation device **118**. The time interval CED can be used by the isolation device **118** to properly time the transmission of read data to the MCH **101**, as described above and explained further below.

As shown in FIG. **18**, a delay signal DS is generated according to the time interval EWD (**1830**). Concurrent to receiving the write strobe signal DQS, the isolation device **118** also receives a set of write data signals DQ (**1840**). The received write data signals are transmitted to the subgroup of memory devices (**1850**), which are selected from the group of memory devices coupled to the isolation device **118** by the one or more first enable signals.

During a read operation, another set of module control signals including, for example, one or more second enable signals, are received by the isolation device **118** from the module controller **116** (**1860**). The one or more second enable signals are generated by the module controller **116** in response to read command signals received from the MCH **101**, and are used by the isolation device **118** to select a subgroup of memory devices from which to receive read data. Afterwards, a read strobe signal DQS and a set of read data signal DQ are received from the selected subgroup of memory devices (**1870**). To properly time the transmission of the DQS and DQ signals to the MCH **101**, the DQS and DQ signals are adjusted (e.g., delayed) according to the delay signal DS, such that the DQS and DQ signals follow a read command by a time interval consistent with a read latency parameter associated with the system **100**.

In certain embodiments, especially the embodiments shown in FIG. **2**D, the delay circuits **1560** and **1660** shown in FIGS. **15** and **16** are not needed to provide alignment of

the read data. As shown in FIG. **19**, the ID control circuit **310** includes a clock regeneration circuit **1920** that regenerates the clock signal CK received from the control circuit **116**, according to the delay signal DS. The regenerated clock signals CK**0** and CKM each includes a proper amount of delay as compared to the clock signal CK. The clock CK**0** is provided to the strobe routing circuit **620** so that the strobe signals are properly timed to result in proper data alignment. The regenerated clock signal CKM is provided to the respective set of memory devices so that the respective data buffer **118** and the respective set of memory devices are locally synchronized.

We claim:

1. A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:

a module board having edge connections to be coupled to respective signal lines in the memory bus;

a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;

memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and

data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:

delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sample the first section of the read data using the first delayed read strobe; and

transmit the first section of the read data to a first section of the data bus;

wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.

2. The memory module of claim **1**, wherein a second memory device in the selected rank is configurable to output at least a second section of the read data and at least a second read strobe, and wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals:

delay the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sample the second section of the read data using the second delayed read strobe; and

transmit the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based at least on signals received by the second data buffer during one or more previous operations.

3. The memory module of claim **2**, wherein a third memory device in the selected rank is configurable to output a third section of the read data and a third read strobe, wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals:

delay the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and

transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.

4. The memory module of claim **2**, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and wherein the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation.

5. The memory module claim **2**, wherein each of the first section and the second section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

6. The memory module of claim **1**, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation.

7. The memory module of claim **1**, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal, and wherein the first data buffer is further configurable to:

receive the module clock signal;

generate a local clock signal having a programmable phase relationship with the module clock signal; and

output the local clock signal;

wherein the first memory device is configurable to receive the local clock signal and to output the first section of the read data and first read strobe in accordance with the local clock signal.

8. The memory module of claim **1**, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal together with the module control signals to the data buffers, and wherein the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals, a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.

9. The memory module of claim **8**, wherein the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at

least one delayed version of the respective module control signal, and wherein the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal, and to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.

10. The memory module of claim **9**, wherein the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal, and to select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators; and wherein the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.

11. The memory module of claim **1**, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations.

12. The memory module of claim **1**, wherein the first section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.

13. The memory module of claim **1**, wherein the memory devices are selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory.

14. A method, comprising:

at a memory module in a computer system and operable to communicate data with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module including a module board having edge connections to be coupled to respective signal lines in the memory bus, a module control device on the module board, memory devices arranged in multiple ranks on the module board and coupled to the module control device, and data buffers on the module board and coupled between the edge connections and the memory devices, the data buffers including a first data buffer, wherein each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks;

receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines;

outputting, at the module control device, registered C/A signals in response to the input C/A signals, wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe;

outputting, at the module control device, module control signals;

receiving, at each of the data buffers, the module control signals from the module control device;

the method further comprising, at the first data buffer, in response to one of more of the module control signals:

delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe;

sampling the first section of the read data using the first delayed read strobe; and

transmitting the first section of the read data to a first section of the data bus; and

the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer.

15. The method of claim **14**, wherein the data buffers further include a second data buffer, and wherein a second memory device in the selected rank is coupled to the second data buffer and is configurable to output at least a second section of the read data and at least a second read strobe, the method further comprising, at the second data buffer, in response to the one or more of the module control signals:

delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe;

sampling the second section of the read data using the second delayed read strobe; and

transmitting the second section of the read data to a second section of the data bus;

wherein the second predetermined amount is determined based on signals received by the second data buffer during one or more previous operations.

16. The method of claim **15**, wherein a third memory device in the selected rank is coupled to the first data buffer and is configurable to output a third section of the read data and a third read strobe, the method further comprising, at the first data buffer, in response to the one or more of the module control signals:

delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe;

sampling the third section of the read data using the third delayed read strobe concurrently with receiving the first section of the read data using the first delayed read strobe; and

transmitting the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;

wherein the third predetermined amount is determined based on the signals received by the first data buffer during one or more previous operations.

17. The method of claim **15**, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation.

18. The method of claim **14**, further comprising:

receiving, at the module control device, a system clock signal concurrently with receiving the input C/A signals;

outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;

receiving, at the first data buffer, the module clock signal;

generating, at the first data buffer, a local clock signal having a programmable phase relationship with the module clock signal; and

outputting, at the first data buffer, the local clock signal;

receiving, at the first memory device, the local clock signal; and

outputting, at the first memory device, the first section of the read data and first read strobe in accordance with the local clock signal.

19. The method of claim **14**, further comprising:

receiving, at the module control device, a system clock signal concurrently with receiving the input control and address signal;

outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;

generating, at the first data buffer, one or more metastability indicators indicating a metastability condition in a respective module control signal of the module control signals with respect to the module clock signal.

20. The method of claim **19**, further comprising, at the first data buffer:

generating at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal;

selecting a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least one of the metastability indicators;

selecting a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on another metastability indicator; and

sampling the selected module control signal according to the selected module clock signal to output received respective module control signal.

* * * * *

Exhibit 2

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(54) **MEMORY MODULE WITH CONTROLLED BYTE-WISE BUFFERS**

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CPC ***G06F 12/00*** (2013.01); ***G11C 5/025*** (2013.01); ***G11C 5/04*** (2013.01); ***G11C 5/066*** (2013.01); ***G11C 8/12*** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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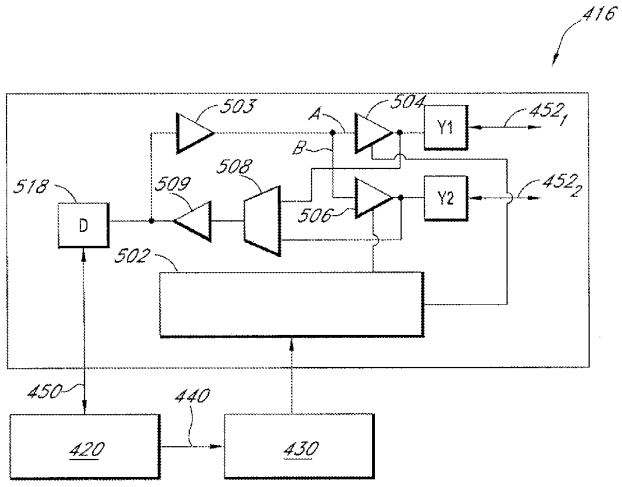
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(57) **ABSTRACT**

A memory module is configured to communicate with a memory controller. The memory module comprises DDR DRAM devices arranged in multiple ranks each of the same width as the memory module, and a module controller configured to receive and register input control signals for a read or write operation from the memory controller and to output registered address and control signals. The registered address and control signals selects one of the multiple ranks to perform the read or write operation. The module controller further outputs a set of module control signals in response to the input address and control signals. The memory module further comprises a plurality of byte-wise buffers controlled by the set of module control signals to actively drive respective byte-wise sections of each data signal associated with the read or write operation between the memory controller and the selected rank.

35 Claims, 13 Drawing Sheets



Related U.S. Application Data

continuation of application No. 12/761,179, filed on Apr. 15, 2010, now Pat. No. 8,516,185, which is a continuation-in-part of application No. 12/504,131, filed on Jul. 16, 2009, now Pat. No. 8,417,870.

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Figure 1A: (Prior Art)

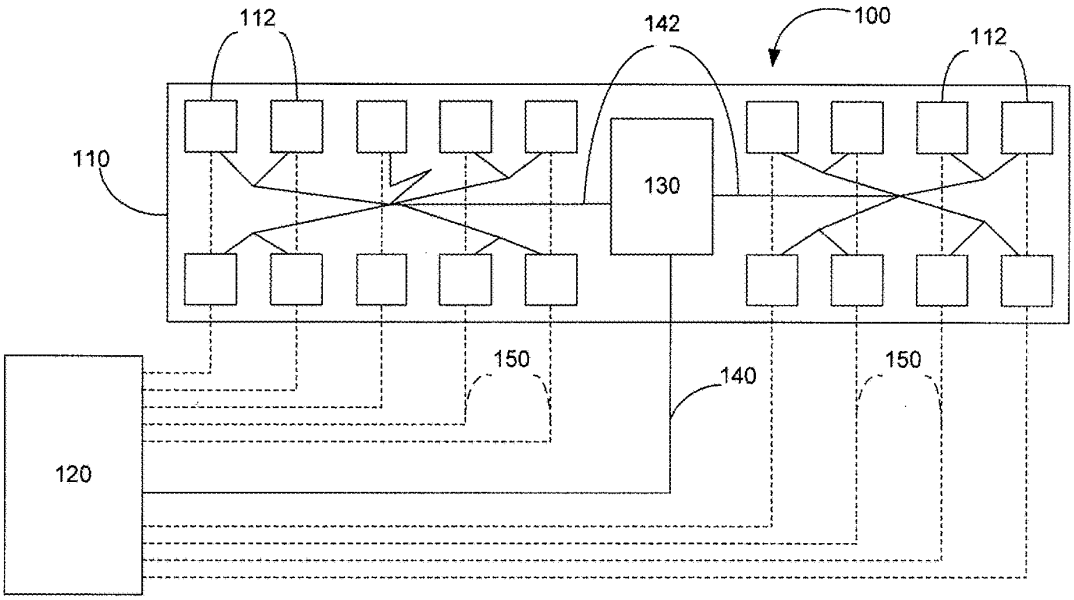


Figure 1B: (Prior Art)

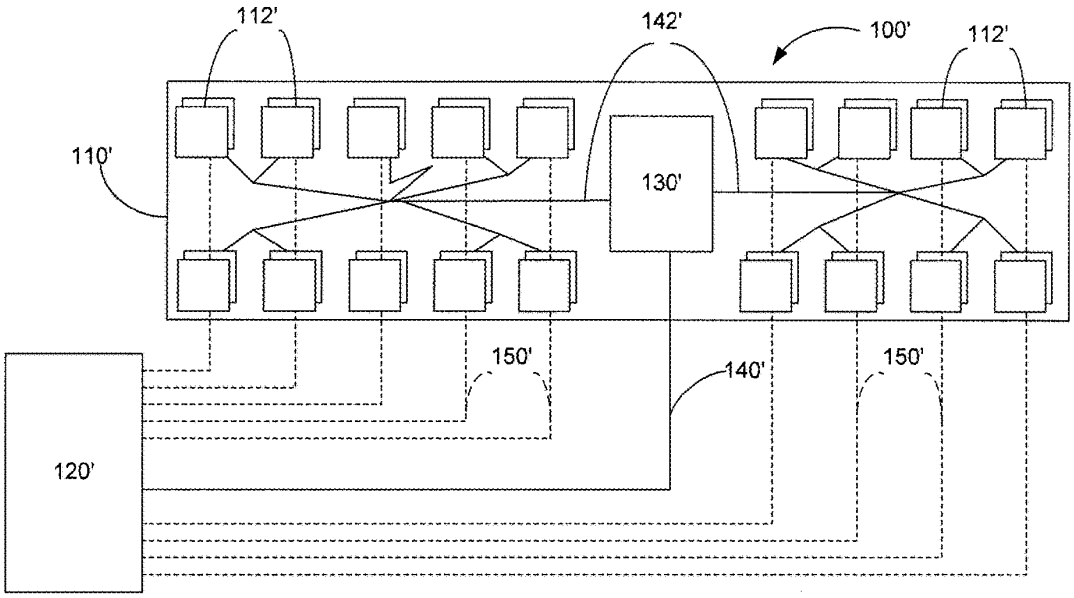


Figure 2A: (Prior Art)

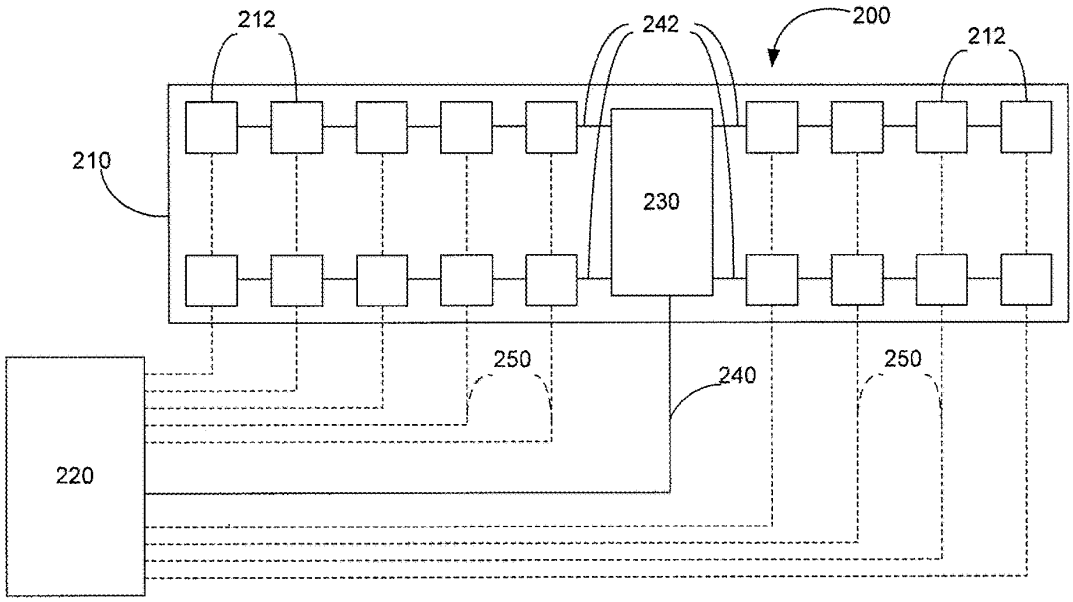


Figure 2B: (Prior Art)

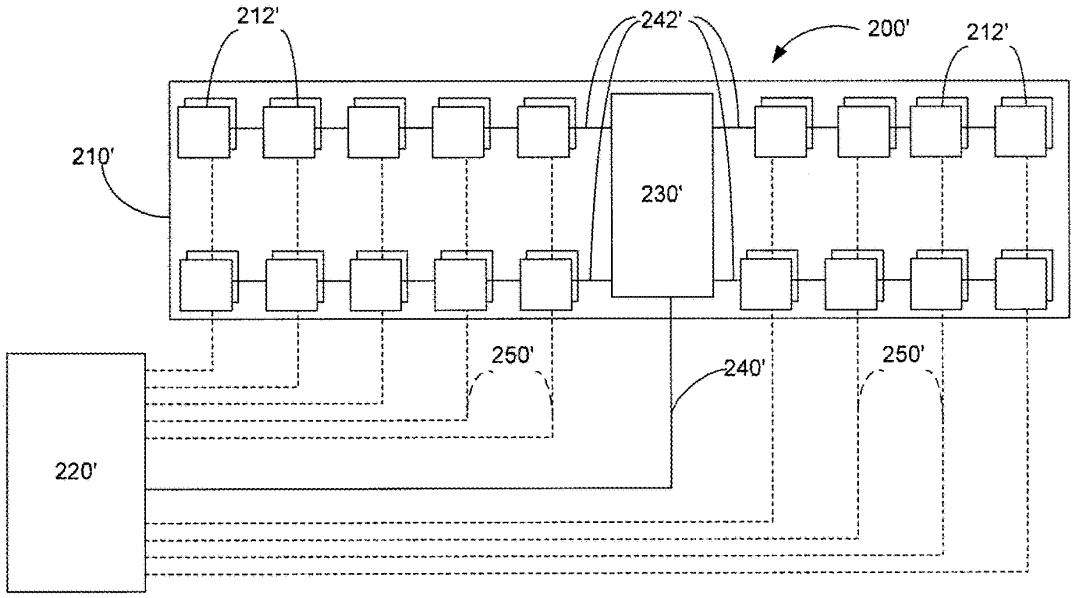


Figure 2C: (Prior Art)

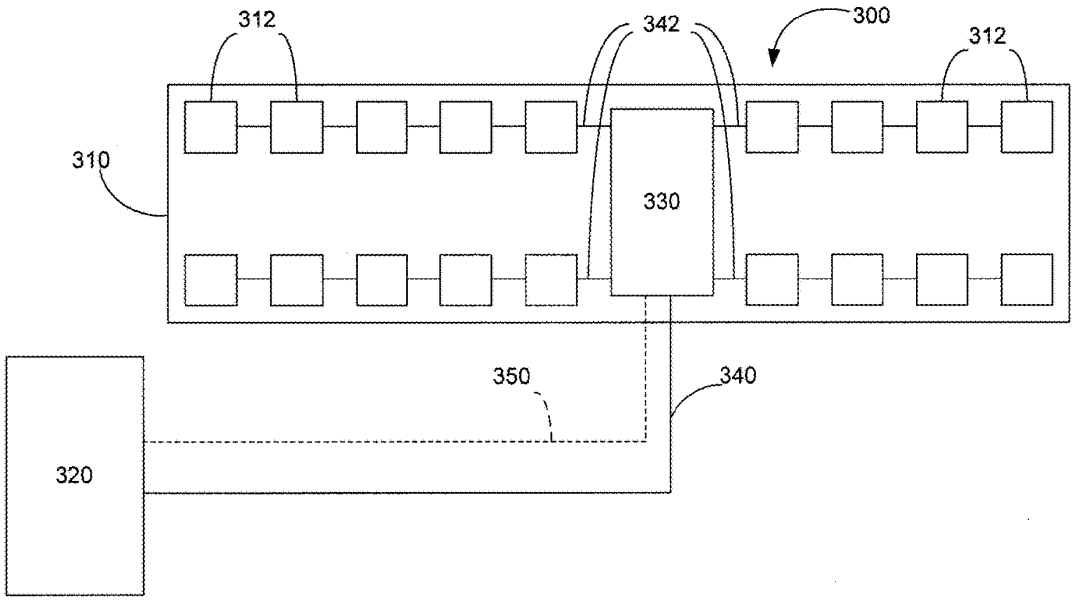
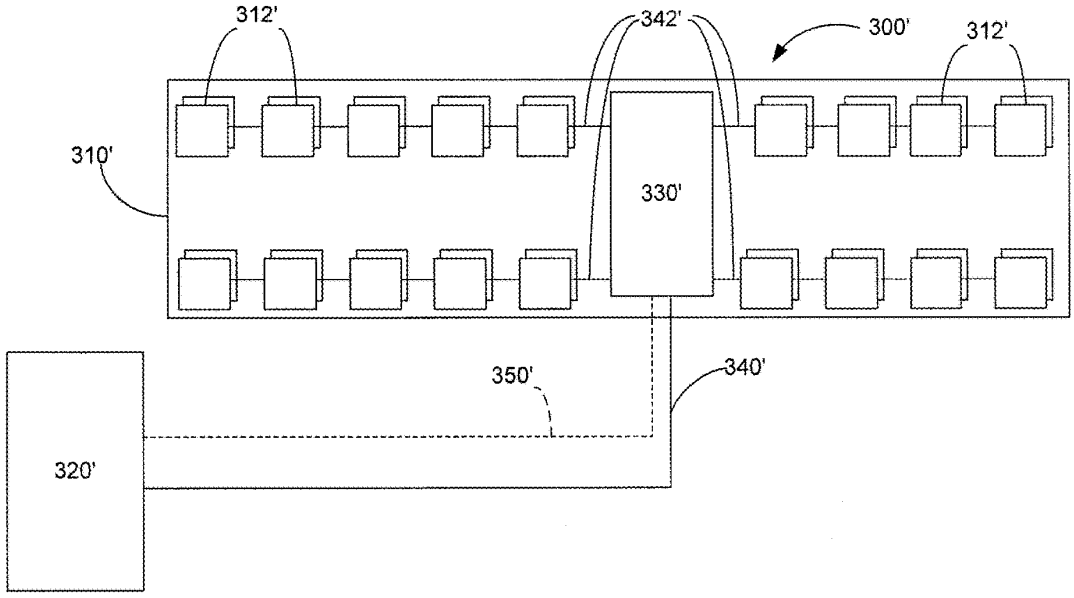


Figure 2D: (Prior Art)



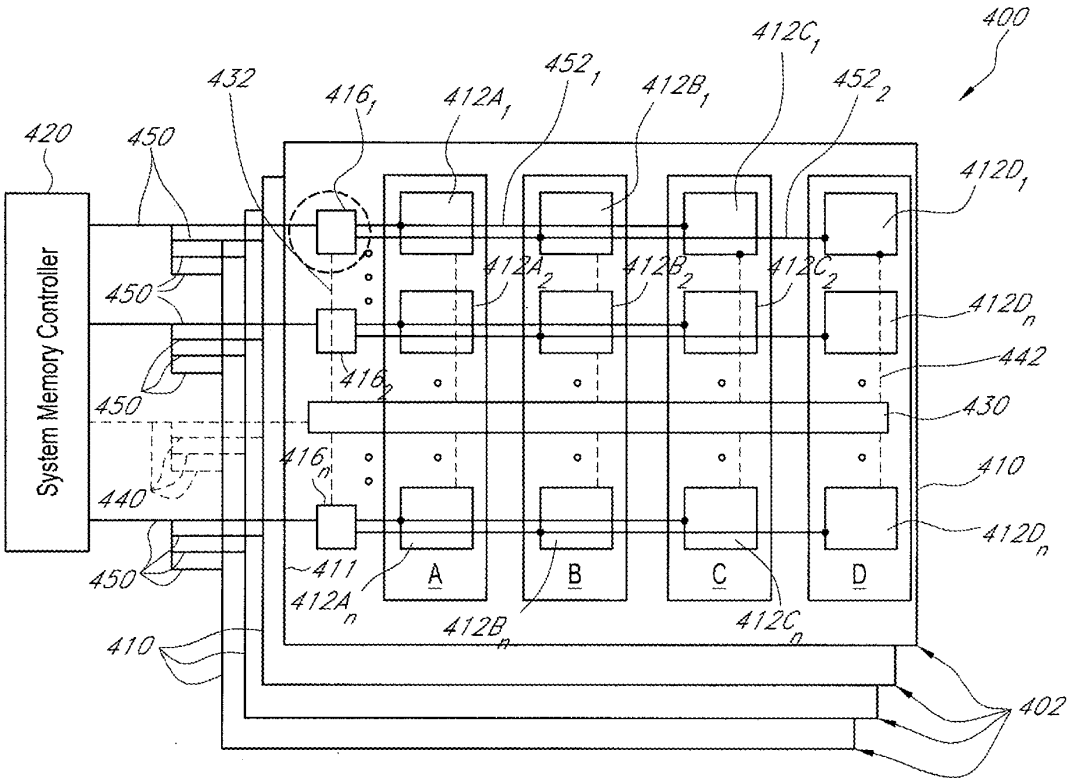

400
420
System Memory Controller
450
432
416_1
$412A_1$
452_1
$412B_1$
$412C_1$
452_2
$412D_1$
$412A_2$
$412B_2$
$412C_2$
$412D_n$
442
430
410
416_2
416_n
440
411
$412A_n$
$412B_n$
$412C_n$
A
B
C
D
402

FIG. 3A

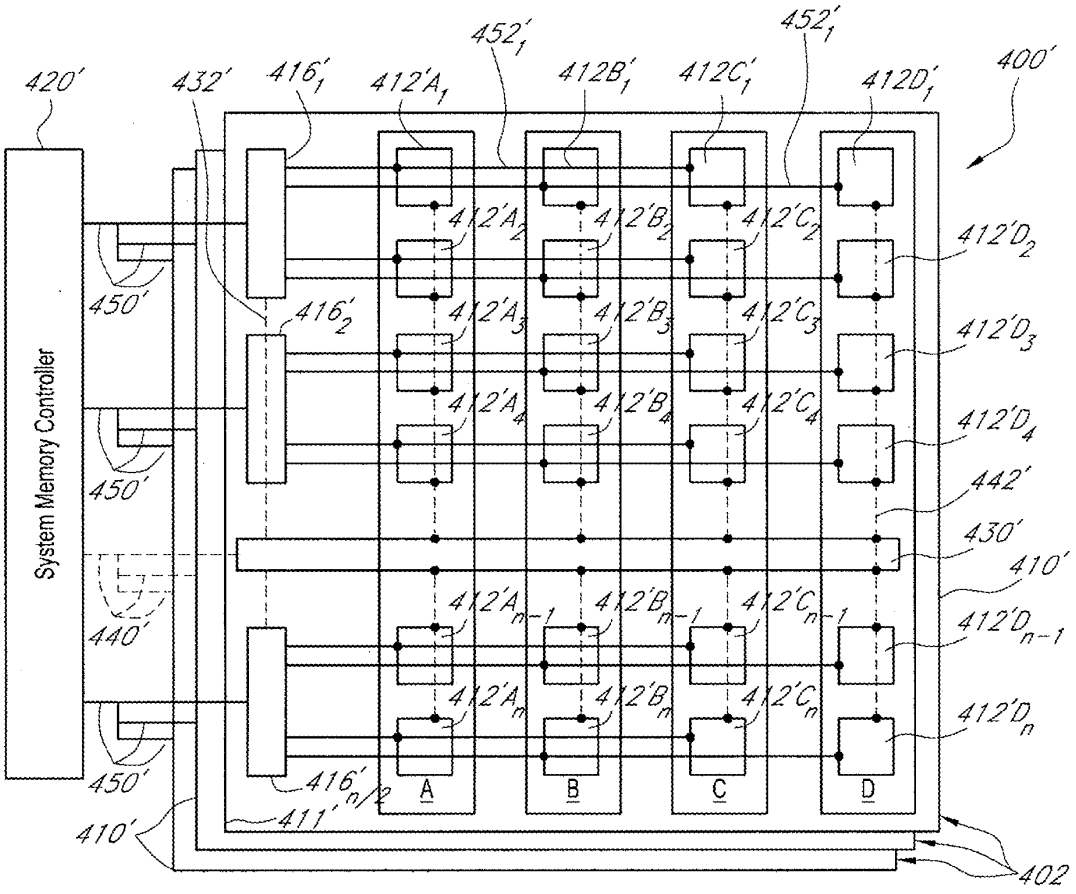

System Memory Controller
420′
432′
416′1
412′A1
452′1
412B′1
412C′1
452′1
4120′1
400′
412′A2
412′B2
412′C2
412′D2
450′
416′2
412′A3
412′B3
412′C3
412′D3
412′A4
412′B4
412′C4
412′D4
442′
430′
410′
440′
412′An−1
412′Bn−1
412′Cn−1
412′Dn−1
412′An
412′Bn
412′Cn
412′Dn
450′
416′n/2
A
B
C
D
411′
410′
402

FIG. 3B

Figure 3C:

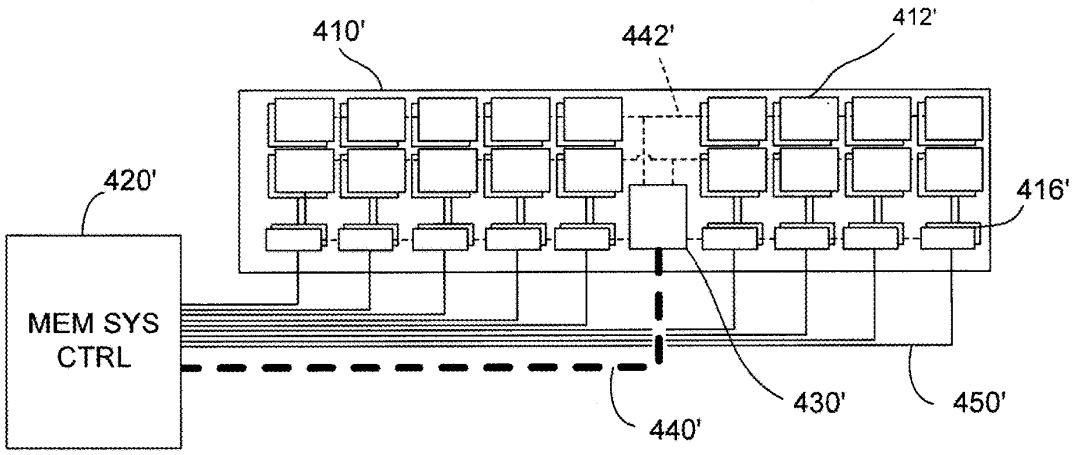
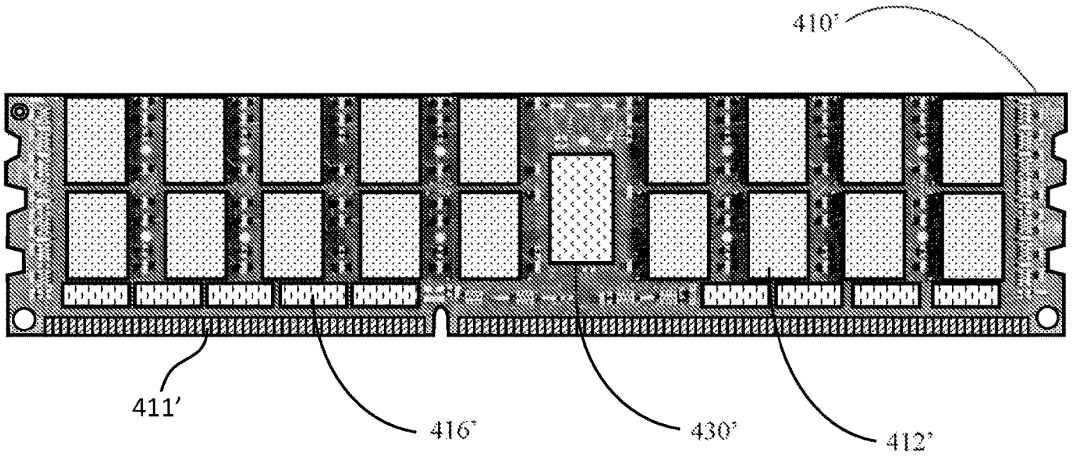


Figure 3D:



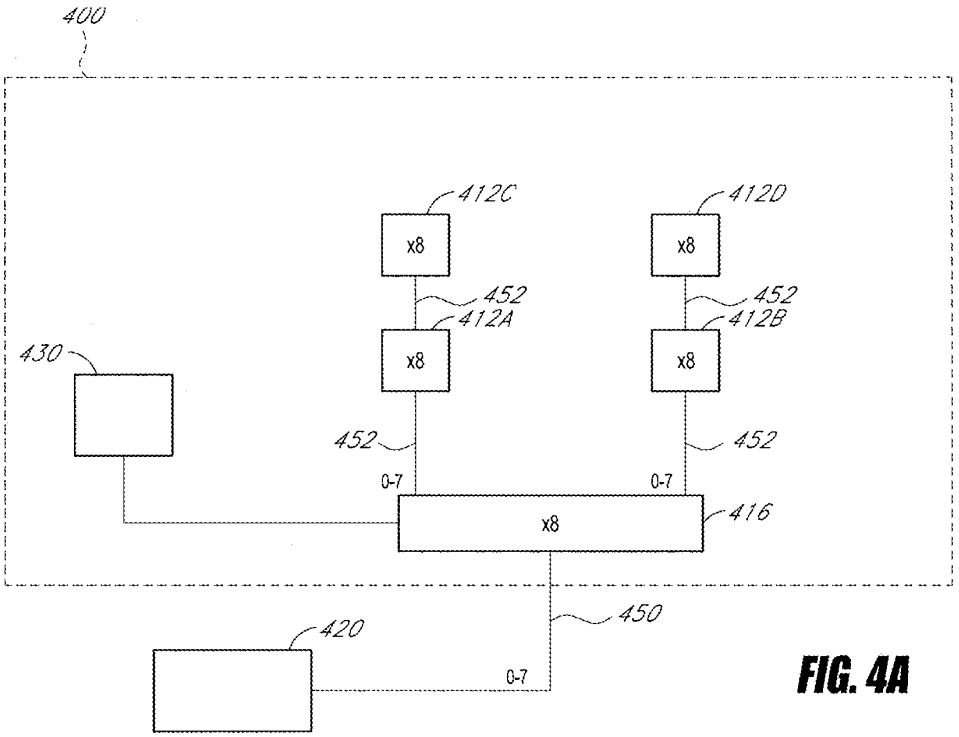

400
412C
412D
x8
x8
452
412A
452
412B
x8
x8
430
452
452
0-7
0-7
x8
416
450
420
0-7

FIG. 4A

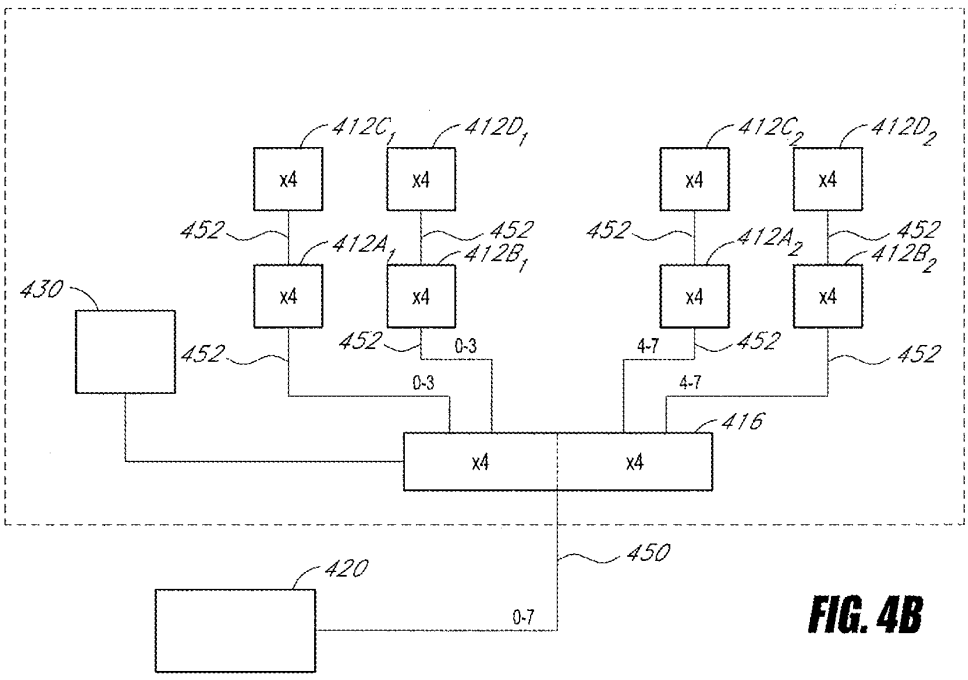

412C1
412D1
412C2
412D2
x4
x4
x4
x4
452
412A1
452
412B1
452
412A2
452
412B2
x4
x4
x4
x4
430
452
452
0-3
4-7
452
452
0-3
4-7
416
x4
x4
450
420
0-7

FIG. 4B

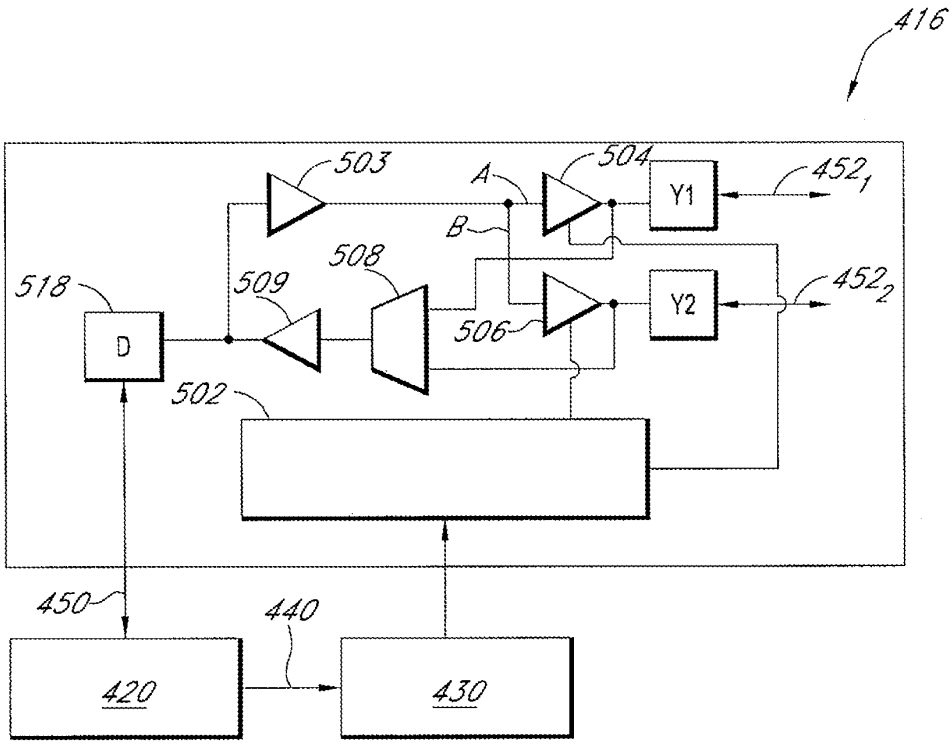

416
503
504
A
B
Y1
452_1
508
509
518
D
506
Y2
452_2
502
450
440
420
430

FIG. 5

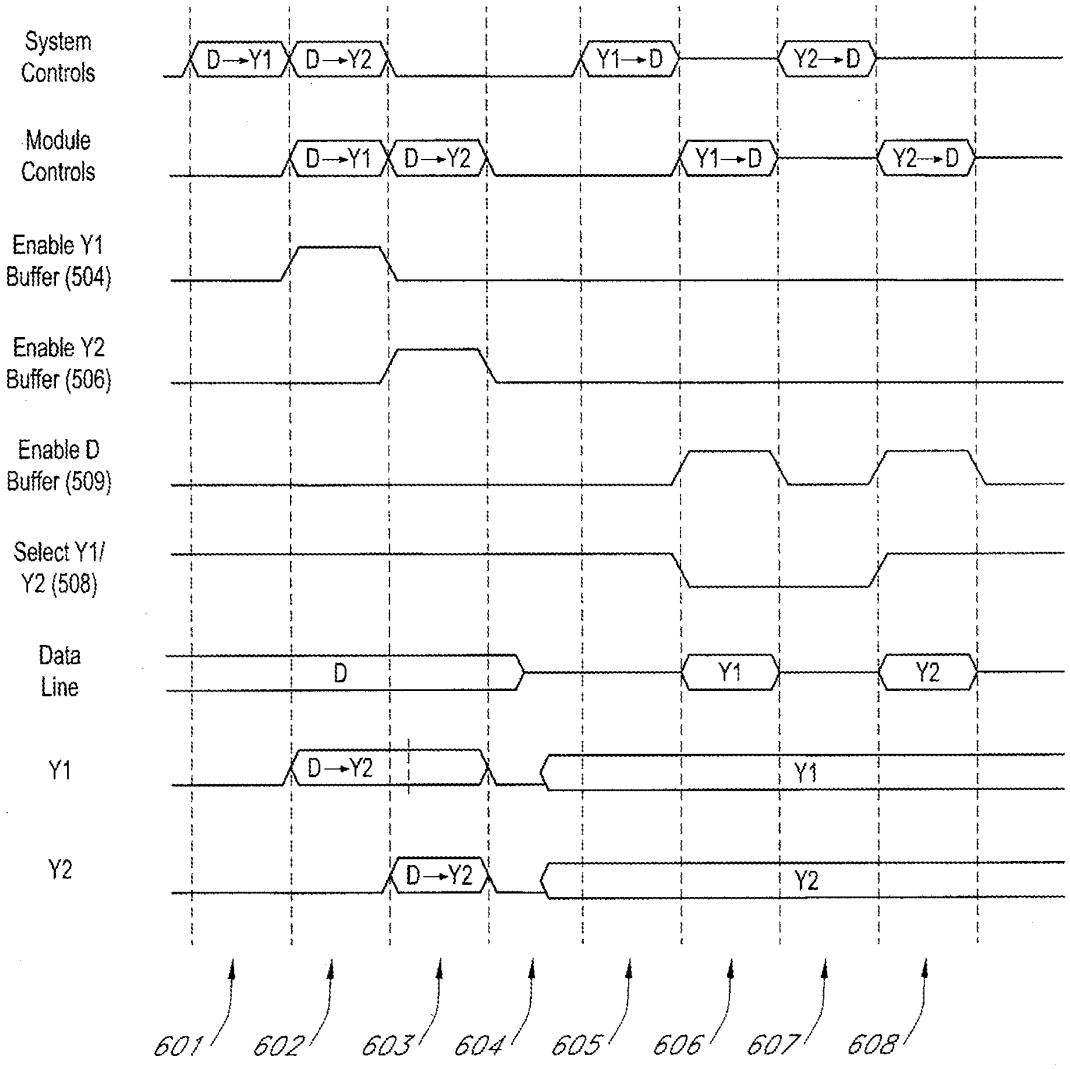

System Controls
Module Controls
Enable Y1 Buffer (504)
Enable Y2 Buffer (506)
Enable D Buffer (509)
Select Y1/ Y2 (508)
Data Line
Y1
Y2
D→Y1
D→Y2
Y1→D
Y2→D
D
Y1
Y2
601
602
603
604
605
606
607
608

FIG. 6

MEMORY MODULE WITH CONTROLLED BYTE-WISE BUFFERS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation from U.S. patent application Ser. No. 13/970,606, filed Aug. 20, 2013, to be issued as U.S. Pat. No. 9,606,907, which is a continuation from U.S. patent application Ser. No. 12/761,179, filed Apr. 15, 2010, now U.S. Pat. No. 8,516,185, which is a continuation-in-part from U.S. patent application Ser. No. 12/504,131, filed Jul. 16, 2009, now U.S. Pat. No. 8,417,870, each of which is incorporated in its entirety by reference herein.

BACKGROUND

The present disclosure relates generally to memory subsystems of computer systems, and more specifically to systems, devices, and methods for improving the performance and the memory capacity of memory subsystems or memory "boards," particularly memory boards that include dual in-line memory modules (DIMMs).

Certain types of computer memory subsystems include a plurality of dynamic random-access memory (DRAM) or synchronous dynamic random access memory (SDRAM) devices mounted on a printed circuit board (PCB). These memory subsystems or memory "boards" are typically mounted in a memory slot or socket of a computer system, such as a server system or a personal computer, and are accessed by the processor of the computer system. Memory boards typically include one or more memory modules, each with a plurality of memory devices (such as DRAMs or SDRAMs) in a unique configuration of rows, columns, and banks, which provide a total memory capacity for the memory module.

The memory devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" or "by 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" or "by 72" organization.

The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

During operation, the ranks of a memory module are selected or activated by control signals that are received from the processor. Examples of such control signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support a limited number of ranks per memory module, which limits the memory density that can be incorporated in each memory module.

The memory space in an electronic system is limited by the physical addressable space that is defined by the number of address bits, or by the number of chips selected. In general, once the memory space is defined for an electronic system, it would not be feasible to modify the memory space without an extensive design change. This is especially true for the case in which a memory space is defined by a consortium, such as the Joint Electron Device Engineering Council (JEDEC). A problem arises when a user's application requires a larger addressable memory space than the memory space that the current electronic system is designed to support.

In developing a memory subsystem, consideration is always given to memory density, power dissipation (or thermal dissipation), speed, and cost. Generally, these attributes are not orthogonal to each other, meaning that optimizing one attribute may detrimentally affect another attribute. For example, increasing memory density typically causes higher power dissipation, slower operational speed, and higher costs.

Furthermore, the specifications of the memory subsystem may be guided by physical limitations associated with these attributes. For example, high thermal dissipation may limit the speed of the operation, or the physical size of the memory module may limit the density of the module.

These attributes generally dictate the design parameters of the memory module, usually requiring that the memory system slow down operation speed if the memory subsystem is populated with more memory devices to provide higher density memory cards.

SUMMARY

In certain embodiments, a memory module is configured to communicate with a memory controller of a computer system via a set of control signal lines and a plurality of sets of data signal lines. Each set of the plurality sets of data signal lines is a byte wide. The memory module has a width of, for example, 32 bits, 64 bits, 72 bits, 128 bits, or 256 bits, etc., and comprises a printed circuit board configured to be coupled to the memory controller via the set of control signal lines and the first number of data signal lines. The module board is mountable in a memory socket of the computer system and has an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and are positioned to be releasably coupled to corresponding contacts of the memory socket. The memory module further comprises memory devices such as double data rate dynamic random access memory (DDR DRAM) devices coupled to the module board and arranged in multiple ranks each of the same width (i.e., N bits) as the memory module. The memory module further comprises a module controller coupled to the module board and operatively coupled to the DDR DRAM devices via a set of registered control lines. The module controller is configured to register input address and control signals for a read or write operation received from the memory controller via the set of address and control signal lines, and to output registered address and control signals onto the set of registered control lines. The read or write operation being targeted at a specific N-bit-wide rank of the multiple N-bit-wide ranks, so that the specific N-bit-wide rank is an only N-bit-wide rank among the multiple N-bit wide ranks selected to perform the read or write operation. The module controller is further configured to output a set of module control signals in response to the input control signals, the set of module control signals including signals that are dependent on which of the multiple N-bit-wide ranks is the specific N-bit-wide rank.

The memory module further comprises a plurality of byte-wise buffers coupled to the circuit board and configured to receive the second module control signals. Each respective byte-wise buffer of the plurality of byte-wise buffers is coupled to a respective set of the plurality of sets of data signal lines and to at least one respective DDR DRAM

device in each of the multiple ranks. The plurality of byte-wise buffers are disposed on the module board at respective positions corresponding to respective sets of the plurality of sets of data signal lines. In certain embodiments, each respective byte-wise buffer includes data paths and logic controlling the data paths in response to the second module control signals so that each respective byte-wise buffer is configured to actively drive a respective byte-wise section of each N-bit wide data signal associated with the read or write operation between the respective set of the plurality of sets of data signal lines and the at least one respective DDR DRAM device in the specific N-bit-wide rank. In certain embodiments, the each respective byte-wise buffer includes configurable data paths and logic that configures the data paths in response to the second module control signals so as to enable a respective byte-wise section of each N-bit wide data signal associated with the read or write operation be communicated between the memory controller and the at least one respective DDR DRAM device in the specific N-bit-wide rank. The logic configures the data paths differently depending on which of the multiple N-bit-wide ranks is performing the read or write operation.

In certain embodiments, the byte-wise buffers are configured to present to the memory controller one DDR DRAM device load on each data line of the plurality of sets of data lines during a write operation. In certain embodiments, the control circuit controls the byte-wise buffers in accordance with a CAS latency parameter.

BRIEF DESCRIPTION OF THE DRAWINGS

A complete understanding of the present invention may be obtained by reference to the accompanying drawings, when considered in conjunction with the subsequent, detailed description, in which:

FIG. **1**A is a schematic representation of a conventional memory subsystem populated with at least one JEDEC-standard two-rank memory module;

FIG. **1**B is a schematic representation of a conventional memory subsystem populated with at least one JEDEC-standard four-rank memory module.

FIG. **2**A is a schematic representation of another conventional memory subsystem populated with at least one two-rank memory module.

FIG. **2**B is a schematic representation of another conventional memory subsystem populated with at least one four-rank memory module.

FIGS. **2**C and **2**D schematically illustrate a conventional two-rank memory module and a four-rank memory module, respectively, each comprising a memory buffer.

FIG. **3**A is a schematic representation of an example memory subsystem in accordance with an embodiment of the disclosure.

FIG. **3**B schematically illustrates another example memory subsystem in accordance with certain embodiments described herein.

FIG. **3**C schematically illustrates an example layout of the memory devices, the data transmission circuits, and the control circuit of a memory module in accordance with certain embodiments described herein.

FIG. **3**D is a photograph of an example memory subsystem in accordance with certain embodiments described herein.

FIG. **4**A schematically illustrates an example memory subsystem comprising a data transmission circuit with a bit width which is the same as that of the individual memory devices.

FIG. **4**B schematically illustrates an example memory subsystem comprising a data transmission circuit with a bit width different from that as the individual memory devices.

FIG. **5** is a schematic representation of an example embodiment of a data transmission circuit compatible with the memory subsystem of FIG. **3**A.

FIG. **6** is an example timing diagram illustrating operation of the memory system of FIGS. **3**A and **5**.

For purposes of clarity and brevity, like elements and components bear like designations and numbering throughout the figures.

DETAILED DESCRIPTION

One method for increasing memory space is based on an address decoding scheme. This method is very widely adopted in the electronics industry in designing Application-Specific Integrated Circuit (ASIC) and System-On-Chip (SOC) devices to expand system memories. Another method increases the addressable memory space without extensive alteration of the software or hardware of an existing electronics system. This method combines chip-select signals with an address signal to increase the number of physically addressable memory spaces (e.g., by a factor of 2, by a factor of 4, by a factor of 8, or by other factors as well).

These methods have several shortcomings. For example, since these methods increase the addressable memory space by directly adding memory chips, a heavier load is presented to the outputs of the system controller and the outputs of the memory devices, resulting in a slower system. Also, increasing the number of memory devices results in higher power dissipation. In addition, since an increase in the number of memory devices on each memory module alters the physical properties of the memory module while the system board remains the same, the overall signal (transmission line) wave characteristics deviate from the original design intent or specification. Furthermore, especially when registered DIMMs (RDIMMs) are used, the increase in the number of the memory devices translates to an increase in the distributed RC load on the data paths, but not on the control paths (e.g., address paths), thereby introducing uneven signal propagation delay between the data signal paths and control signal paths. As used herein, the terms "control lines" and "control paths" include address lines or paths and command lines or paths, and the term "control signals" includes address signals and command signals.

FIGS. **1**A and **1**B illustrate a prior art approach of increasing the number of memory devices. Specifically, FIG. **1**A shows a conventional memory subsystem **100** with at least one JEDEC-standard two-rank memory module **110**, such as a registered dual inline memory module (RDIMM), only one of which is shown for clarity. Each rank of the memory module **110** comprises a plurality of memory devices **112**, such as dynamic random access memory (DRAM) devices or synchronous DRAM (SDRAM) devices. A register **130** receives a plurality of control lines **140** (shown as a single solid line) from the system memory controller **120** and is connected via control lines **142** to the memory devices **112** of each rank of the memory module **110**. This memory subsystem **100** connects each data line of an array of data lines **150** (shown as dashed lines) from a system memory controller **120** to corresponding memory devices **112** in the two ranks in each memory module **110**. Therefore, during a write operation, the system memory controller **120** sees all the memory devices **112** as its load via the data lines **150**, and during a read operation, each memory

device **112** sees multiple other memory devices **112**, as well as the system memory controller **120**, as its load via the data lines **150**.

FIG. **1**B is a schematic view of another conventional memory subsystem **100'** with at least one JEDEC-standard four-rank memory module **110'** (only one of which is shown for clarity), each rank comprising a plurality of memory devices **112'**. The register **130'** receives the plurality of control lines **140'** (shown as a single solid line) from the system memory controller **120'** and is connected via control lines **142'** to the memory devices **112'** of each rank of the memory module **110'**. Each data line of the array of data lines **150'** (shown as dashed lines) from the system memory controller **120'** is connected (e.g., by four fanouts) to corresponding memory devices **112'** in the four ranks in each memory module **110'**. Therefore, as with the two-rank memory module **110** shown in FIG. **1**A, during a write operation, the system memory controller **120'** sees all the memory devices **112'** as its load via the data lines **150'**, and during a read operation, each memory device **112'** sees multiple other memory devices **112'** and the system memory controller **120'** as its load via the data lines **150'**.

For both the conventional two-rank memory module **110** and the conventional four-rank memory module **110'**, the multiple loads seen by the memory controller **120**, **120'** during write operations and the multiple loads seen by the memory devices **112**, **112'** during read operations cause significant performance issues. For example, for synchronous operation, time delays of the various signals are desired to be substantially equal to one another such that the operation of the memory module **110**, **110'** is synchronized with the system bus of the computer system. Thus, the trace lengths of the memory module **110**, **110'** are selected such that the signals are at the same clock phase. For example, the lengths of the control lines **142**, **142'** from the register **130**, **130'** to each of the memory devices **112**, **112'** are substantially equal to one another. However, for faster clock speeds, small errors in the trace lengths make such synchronous operation difficult or impossible. Therefore, these prior art techniques not only reduce the speed of the memory systems, but they also require hardware modifications to minimize any deviation of the transmission line wave characteristics from the original design specification.

FIGS. **2**A and **2**B illustrate another prior art approach of increasing the number of memory devices. Specifically, FIG. **2**A shows a conventional memory subsystem **200** with at least one two-rank memory module **210**, only one of which is shown for clarity. Each rank of the memory module **210** comprises a plurality of memory devices **212**, such as dynamic random access memory (DRAM) devices or synchronous DRAM (SDRAM) devices. A register **230** receives a plurality of control lines **240** (shown as a single solid line) from the system memory controller **220** and is connected via control lines **242** to the memory devices **212** of each rank of the memory module **210**. This memory subsystem **200** connects each data line of an array of data lines **250** (shown as dashed lines) from a system memory controller **220** to corresponding memory devices **212** in the two ranks in each memory module **210**. Therefore, during a write operation, the system memory controller **220** sees all the memory devices **212** as its load via the data lines **250**, and during a read operation, each memory device **212** sees multiple other memory devices **212**, as well as the system memory controller **220**, as its load via the data lines **250**.

FIG. **2**B is a schematic view of another conventional memory subsystem **200'** with at least one four-rank memory module **210'** (only one of which is shown for clarity), each rank comprising a plurality of memory devices **212'**. The register **230'** receives the plurality of control lines **240'** (shown as a single solid line) from the system memory controller **220'** and is connected via control lines **242'** to the memory devices **212'** of each rank of the memory module **210'**. Each data line of the array of data lines **250'** (shown as dashed lines) from the system memory controller **220'** is connected (e.g., by four fanouts) to corresponding memory devices **212'** in the four ranks in each memory module **210'**. Therefore, as with the two-rank memory module **210** shown in FIG. **2**A, during a write operation, the system memory controller **220'** sees all the memory devices **212'** as its load via the data lines **250'**, and during a read operation, each memory device **212'** sees multiple other memory devices **212'** and the system memory controller **220'** as its load via the data lines **250'**.

For the memory modules **210**, **210'**, the control lines **242**, **242'** have a "flyby" configuration. In such a configuration, control signals are sent along the control lines **242**, **242'** (e.g., in a single-path daisy-chain) from the register **230**, **230'** to the memory devices **212**, **212'** of a given rank. These control signals reach each memory device **212**, **212'** of the rank sequentially, with the control signals first reaching the memory device **212**, **212'** having the shortest control line **242**, **242'**, then reaching the memory device **212**, **212'** having the next-shortest control line **242**, **242'**, and so on. For example, a control signal may reach the memory device **212**, **212'** having the longest control line **242**, **242'** a significant period of time after the same control signal reaches the memory device **212**, **212'** having the shortest control line **242**, **242'**. For synchronous operation, the memory subsystems **200**, **200'** have the data lines **250**, **250'** configured so that the time delays of the various data signals between the memory controller **220**, **220'** and the particular memory devices **212**, **212'** are substantially tailored such that the data signals and the control signals reach the particular memory device **212**, **212'** so that operation of the memory module **210**, **210'** is synchronized with the system bus of the computer system. Such "fly-by" configurations have been described as operating in "local sync" while having "global async."

For such "fly-by" configurations, the memory controller **220**, **220'** of FIGS. **2**A and **2**B is more complicated than the memory controller **120**, **120'** of FIGS. **1**A and **1**B in that the memory controller **220**, **220'** accounts for the time delays between the various memory devices **212**, **212'** and adjusts the timing of these signals appropriately for synchronous operation. However, in some situations, the clock cycle time is approximately equal to or less than the time difference (e.g., about 900 picoseconds) between the control signals reaching the memory device **212**, **212'** having the longest control line **242**, **242'** and reaching the memory device **212**, **212'** having the shortest control line **242**, **242'**. Under such situations, synchronous operation is not achievable. Thus, the time difference between the control signals reaching the memory devices **212**, **212'** at the extremes of the control lines **242**, **242'** provide a limit to the clock speed with which the memory module **210**, **210'** may be operated. These time differences, which can be more than one clock cycle, will limit the operational speed and performance of the memory module. In addition, as with the memory subsystems **100**, **100'** of FIGS. **1**A and **1**B, the "fly-by" memory subsystems **200**, **200'** of FIGS. **2**A and **2**B suffer from large loads which result in slower clock speeds.

One recent suggestion for the "fly-by" configurations is to provide a memory buffer which handles both the control signals and the data signals. FIGS. **2**C and **2**D schematically

illustrate a conventional two-rank memory module **310** and a four-rank memory module **310'**, respectively, each comprising a memory buffer **330**, **330'**. The control lines **340**, **340'** provide conduits for control signals from the memory controller **320**, **320'** to the memory buffer **330**, **330'**, and the control lines **342**, **342'** provide conduits for control signals from the memory buffer **330**, **330'** to the memory devices **312**, **312'**. The plurality of data lines **350**, **350'** (shown as one dashed line for clarity) provide conduits for data signals from the memory controller **320**, **320'** to the memory buffer **330**, **330'**, and data lines (not shown for clarity) on the memory module **310**, **310'** provide conduits for data signals from the memory controller **320**, **320'** to the memory devices **312**, **312'**.

The configurations of FIGS. **2**C and **2**D seek to have both the data signals and the control signals going to the memory buffer **330**, **330'**. However, such configurations have significant drawbacks. To send the data signals to the various memory devices **312**, **312'**, the memory module **310**, **310'** includes an extremely large number of data lines (not shown for clarity) coupling the memory buffer **330**, **330'** to the memory devices **312**, **312'**. For example, in certain circumstances, the memory buffer **330**, **330'** for an LRDIMM is a 628-pin device, which is extremely large. In addition, the logistics of tailoring the time delays of these many data lines is complicated or difficult to provide the desired timing of data signals from the memory buffer **330**, **330'** to the memory devices **312**, **312'**. Also, the memory module **310**, **310'** utilizes significant modifications of the memory controller **320**, **320'** since the memory buffer **330**, **330'** is taking over some of the control of data signal timing that conventional memory controllers have. Even so, the memory modules **310**, **310'** of FIGS. **2**C and **2**D can only operate in asynchronous mode, not synchronous mode, due to the long fly-by times as compared to the desired clock frequencies. For example, for a fly-by delay of 1 nanosecond, if the data rate is 1 Gb/second, there is the possibility of collisions on the data lines during read/write turnaround. To combat such collisions, the data rate can be slowed down or "dead" cycles can be inserted. The memory module **310**, **310'**, as a single unit, cannot be operated in synchronous mode, but operates as locally synchronous, globally (DIMM level) asynchronous.

FIG. **3**A schematically illustrates an example memory subsystem **400** with loadreduced memory modules **402** in accordance with certain embodiments described herein. FIG. **3**B schematically illustrates another example memory subsystem **400'** with loadreduced memory modules **402'** in accordance with certain embodiments described herein. FIG. **3**C schematically illustrates an example layout of the memory devices **412'**, the data transmission circuits **416'**, and the control circuit **430'** of a memory module **402'** in accordance with certain embodiments described herein. FIG. **3**D is a photograph of an example memory subsystem in accordance with certain embodiments described herein. In FIGS. **3**A-**3**C, control lines (e.g., address and control lines **440**, **440'** coupling the system memory controller **420**, **420'** to the memory modules **410**, **410'**) are shown as dashed lines, data lines (e.g., data lines **450**, **450'** coupling the system memory controller **420**, **420'** to the memory modules **410**, **410'**) are shown as solid lines, and in FIGS. **3**A and **3**B, input/output connections are shown as black dots. In certain embodiments, as schematically illustrated by FIGS. **3**A-**3**C, the address and control lines **440**, **440'** coupling the system memory controller **420**, **420'** to the memory module **410**, **410'** (e.g., to the control circuit **430**, **430'**) are separate from the data lines **450**, **450'** coupling the system memory controller **420**, **420'** to the memory module **410**, **410'** (e.g., to the data transmission circuits **416**, **416'**). In certain embodiments, the memory subsystem **400**, **400'** is designed, for example, to deliver higher speed and higher memory density with lower thermal dissipation as compared with conventional memory subsystems. In the following discussion, aspects of the example subsystem **400** and corresponding components (e.g., memory modules **402**, memory devices **412**A, **412**B, **412**C, **412**D, data transmission circuits **416**, control circuit **430**) and of the example subsystem **400'** and corresponding components (e.g., memory modules **402'**, memory devices **412'**A_1, **412'**A_2, **412'**B_1, **412'**B_2, **412'**C_1, **412'**C_2, **412'**D_1, **412'**D_2, data transmission circuits **416'**, control circuit **430'**) should be understood to apply to certain other embodiments as well.

As schematically illustrated in FIGS. **3**A and **3**B, the example memory module **402**, **402'** comprises at least one printed circuit board **410**, **410'** and a plurality of memory devices **412**, **412'** mechanically coupled to the at least one printed circuit board **410**, **410'**. The memory module **402**, **402'** further comprises a control circuit **430**, **430'** mechanically coupled to the at least one printed circuit board **410**, **410'**. The control circuit **430**, **430'** is configurable to receive control signals from the system memory controller **420**, **420'** and to transmit module control signals to the plurality of memory devices **412**, **412'**. The memory module **402**, **402'** further comprises a plurality of data transmission circuits **416**, **416'** mechanically coupled to the at least one printed circuit board **410**, **410'** and distributed at corresponding positions relative to the at least one printed circuit board **410**, **410'**. The plurality of data transmission circuits **416**, **416'** is configurable to be operatively coupled to the system memory controller **420**, **420'** and configurable to receive module control signals from the control circuit **430**, **430'**. At least one first data transmission circuit of the plurality of data transmission circuits **416**, **416'** is operatively coupled to at least two memory devices of the plurality of memory devices **412**, **412'**. At least one second data transmission circuit of the plurality of data transmission circuits **416**, **416'** is operatively coupled to at least two memory devices of the plurality of memory devices **412**, **412'**. The at least one first data transmission circuit is configurable to respond to the module control signals by selectively allowing or inhibiting data transmission between the system memory controller **420**, **420'** and at least one selected memory device of the at least two memory devices operatively coupled to the at least one first data transmission circuit. The at least one second data transmission circuit is configurable to respond to the module control signals by selectively allowing or inhibiting data transmission between the system memory controller **420**, **420'** and at least one selected memory device of the at least two memory devices operatively coupled to the at least one second data transmission circuit.

As shown in FIGS. **3**A and **3**B, the memory subsystem **400**, **400'** is configurable to be operationally coupled to a system memory controller **420**, **420'**, of a type well-known in the art (e.g., Intel Nehalem EP, EX chipsets; AM D Opteron chipset). The memory subsystem **400**, **400'** typically comprises one or more memory modules **402**, **402'**, such as DIMMs or RDIMMs, additional details of which are shown only for one for clarity. Various types of memory modules **402**, **402'** are compatible with embodiments described herein. For example, memory modules having memory capacities of 512 MB, 1 GB, 2 GB, 4 GB, 8 GB, as well as other capacities, are compatible with embodiments described herein. In addition, memory modules having widths of 4 bytes, 8 bytes, 9 bytes, 16 bytes, 32 bytes, or 32

bits, 64 bits, 72 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. Furthermore, memory modules **402**, **402'** compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMMs (FBDIMMs), mini-DIMMs, and micro-DIMMs.

The one or more memory modules **402**, **402'** comprise one or more printed circuit boards (PCBs) **410**, **410'**, which may be arranged in a vertical stack (as shown), or in a back-to-back array. Each memory module **402**, **402'** in certain embodiments comprises a single PCB **410**, **410'**, while in certain other embodiments, each of one or more of the memory modules **402** comprises multiple PCBs **410**, **410'**. In some embodiments, the PCBs **410**, **410'** are mountable in module slots (not shown) of the computer system. A PCB **410**, **410'** of certain such embodiments has at least one edge connector **411** comprising a plurality of electrical contacts which are positioned on an edge of the PCB **410**, **410'** (as shown in FIG. **3***d*) and are configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the system memory controller **420**, **420'** and the various components of the memory modules **402**, **401'** on the PCBs **410**, **410'**.

At least one memory module **402**, **402'** comprises a plurality of memory devices **412**, **412'** (such as DRAMs or SDRAMs). The memory devices **412**, **412'** of the memory module **402**, **402'** may advantageously be arranged in a plurality of rows or ranks. Memory devices **412**, **412'** compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., DDR, DDR2, DDR3, etc.). In addition, memory devices **412**, **412'** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices **412**, **412'** compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (OGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

In certain embodiments, the memory devices **412**, **412'** of the memory module **402**, **402'** are arranged in four ranks, although embodiments with less than four ranks (e.g., one rank, two ranks, three ranks) or more than four ranks (e.g., 6 ranks, 8 ranks) per memory module **402**, **402'** may be employed. In certain embodiments, each rank comprises eight or nine memory modules, while in certain other embodiments, other numbers of memory modules per rank may also be used. In certain embodiments, as schematically shown in FIG. **3**A, the memory devices **412** are arranged in four ranks, denoted A, B, C, and D, and each rank comprises n memory devices. For the sake of this disclosure, in the example memory subsystem **400** of FIG. **3**A, rank A comprises memory devices **412**A_1, **412**A_2, . . . , **412**A_n; rank B comprises memory devices **412**B_1, **412**B_2, . . . , **412**B_n; rank C comprises memory devices **412**C_1, **412**C_2, . . . , **412**C_n; and rank D comprises memory devices **412**D_1, **412**D_2, **412**D_n. For the sake of this disclosure, in the example memory subsystem **400'** of FIG. **3**B, rank A comprises memory devices **412'**A_1, **412'**A_2, . . . , **412'**A_n; rank B comprises memory devices **412'**B_1, **412'**B_2, . . . , **412'**B_n; rank C comprises memory devices **412'**C_1, **412'**C_2, **412'**C_n; and rank D comprises memory devices **412'**D_1, **412'**D_2, . . . , **412'**D_n.

In certain embodiments, at least one memory module **402**, **402'** comprises one or more electrical components (not shown) which may be mounted on the PCB **410**, **410'**, within the PCB **410**, **410'**, or both on and within the PCB **410**, **410'**, and are operationally coupled to one another and to the plurality of memory devices **412**, **412'**. For example, the electrical components may be surface-mounted, through-hole mounted, embedded or buried between layers of the PCB **410**, **410'**, or otherwise connected to the PCB **410**, **410'**. These electrical components may include, but are not limited to, electrical conduits, resistors, capacitors, inductors, transistors, buffers, registers, logic elements, or other circuit elements. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

In certain embodiments, at least one memory module **402**, **402'** comprises a control circuit **430**, **430'** configured to be operatively coupled to the system memory controller **420**, **420'** and to the memory devices **412**, **412'** of the memory module **402**, **402'** (e.g., via lines **442**, **442'**). In certain embodiments, the control circuit **430**, **430'** may include one or more functional devices, such as a programmable-logic device (PLD), an applicationspecific integrated circuit (ASIC), a field-programmable gate array (FPGA), a customdesigned semiconductor device, or a complex programmable-logic device (CPLD). In certain embodiments, the control circuit **430**, **430'** may comprise one or more custom devices. In certain embodiments, the control circuit **430**, **430'** may comprise various discrete electrical elements; while in other embodiments, the control circuit **430**, **430'** may comprise one or more integrated circuits.

The control circuit **430**, **430'** of certain embodiments is configurable to be operatively coupled to control lines **440**, **440'** to receive control signals (e.g., bank address signals, row address signals, column address signals, address strobe signals, and rank-address or chip-select signals) from the system memory controller **420**, **420'**. The control circuit **430**, **430'** of certain embodiments registers signals from the control lines **440**, **440'** in a manner functionally comparable to the address register of a conventional RDIMM. The registered control lines **440**, **440'** are also operatively coupled to the memory devices **412**, **412'**. Additionally, the control circuit **430**, **430'** supplies control signals for the data transmission circuits **416**, **416'** (e.g., via lines **432**, **432'**), as described more fully below. The control signals indicate, for example, the direction of data flow, that is, to or from the memory devices **412**, **412'**. The control circuit **430**, **430'** may produce additional chip-select signals or output enable signals based on address decoding. Examples of circuits which can serve as the control circuit **430**, **430'** are described in more detail by U.S. Pat. Nos. 7,289,386 and 7,532,537, each of which is incorporated in its entirety by reference herein.

In certain embodiments, at least one memory module **402**, **402'** comprises a plurality of data transmission circuits **416**, **416'** mounted on the one or more PCBs **410**, **410'**, within the one or more PCBs **410**, **410'**, or both on and within the one or more PCBs **410**, **410'**. The plurality of data transmission circuits **416**, **416'** are operatively coupled to the control circuit **430**, **430'** (e.g., via lines **432**, **432'**), and configured to be operatively coupled to the system memory controller **420**, **420'** (e.g., via the data lines **450**, **450'**) upon operatively coupling the memory module **402**, **402'** to the computer system. In certain embodiments, these data transmission circuits **416**, **416'** can be referred to as "load-reducing circuits" or "load-reducing switching circuits." As used herein, the terms "load-reducing" or "load-reducing switch-

ing" refer to the use of the data transmission circuits **416**, **416'** to reduce the load seen by the system memory controller **420**, **420'** when operatively coupled to the memory module **402**, **402'**. In certain embodiments, as schematically illustrated by FIG. **3**A, the memory module **402** comprises n data transmission circuits **416**, where n is the number of memory devices per rank of the memory module **410**. For example, as schematically shown in FIG. **3**A, the memory devices **412** of the memory module **410** are arranged in four ranks of n memory devices each, and the memory module **410** comprises at least a first data transmission circuit **416**$_1$ and a second data transmission circuit **416**$_2$. The first data transmission circuit **416**$_1$ of certain such embodiments is operatively coupled to at least one memory device **412** of each rank (e.g., memory devices **412**A$_1$, **412**B$_1$, **412**C$_1$, **412**D$_1$). The second data transmission circuit **416**$_2$ of certain such embodiments is operatively coupled to at least one memory device **412** of each rank (e.g., memory devices **412**A$_2$, **412**B$_2$, **412**C$_2$, **412**D$_2$). In certain embodiments, as schematically illustrated by FIG. **3**B, the memory module **402'** comprises n/2 data transmission circuits **416'**, where n is the number of memory devices per rank of the memory module **410'**. For example, as schematically shown in FIG. **3**B, the memory devices **412'** of the memory module **410'** are arranged in four ranks of n memory devices each, and the memory module **410'** comprises at least a first data transmission circuit **416**$_1$ and a second data transmission circuit **416'2**. The first data transmission circuit **416**$_1$ of certain such embodiments is operatively coupled to at least two memory devices **412'** of each rank (e.g., memory devices **412**A$_1$, **412**A$_2$, **412**B$_1$, **412**B$_2$, **412**C$_1$, **412**C$_2$, **412**D$_1$, **412**D$_2$). The second data transmission circuit **416**$_2$ of certain such embodiments is operatively coupled to at least two memory devices **412'** of each rank (e.g., memory devices **412'**A$_3$, **412'**A$_4$, **412'**B$_3$, **412'**B$_4$, **412'**C$_3$, **412'**C$_4$, **412'**D$_3$, **412'**D$_4$). In certain embodiments, at least one data transmission circuit **416**, **416'** selectively switches between two or more memory devices **412**, **412'** so as to operatively couple at least one selected memory device **412**, **412'** to the system memory controller **420**, **420'** (e.g., the data transmission circuit **416**, **416'** is configurable to respond to module control signals by selectively allowing or inhibiting data transmission between the system memory controller **420**, **420'** and at least one selected memory device **412**, **412'**).

In certain such embodiments, the at least one data transmission circuit **416**, **416'** selectively operatively couples two selected memory devices to the system memory controller **420**, **420'**. For example, as schematically shown in FIG. **3**A, the first data transmission circuit **416**$_1$ is configurable to respond to module control signals by selectively allowing or inhibiting data transmission between the system memory controller **420** and either selected memory devices **412**A$_1$ and **412**C$_1$ or selected memory devices **412**B$_1$ and **412**D$_1$), and the second data transmission circuit **416**$_2$ is configurable to respond to module control signals by selectively allowing or inhibiting data transmission between the system memory controller **420** and either selected memory devices **412**A$_2$ and **412**C$_2$ or selected memory devices **412**B$_2$ and **412**D$_2$). Conversely, in a conventional memory module without the data transmission circuits **416**, the two or more memory devices **412** (e.g., memory devices **412**A$_1$, **412**B$_1$, **412**C$_1$, **412**D$_1$) are concurrently operatively coupled to the system memory controller **420**. A data transmission circuit **416** of certain embodiments bidirectionally buffer data signals between the memory controller **420** and the memory devices **412** corresponding to the data transmission circuit **416**. For another example, as schematically shown in FIG. **3**B, the first data transmission circuit **416'**$_1$ is configurable to respond to module control signals by selectively allowing or inhibiting data transmission between the system memory controller **420'** and either selected memory devices **412'**A$_1$ and **412'**C$_1$ or selected memory devices **412'**B$_1$ and **412'**D$_1$ and either selected memory devices **412'**A$_2$ and **412'**C$_2$ or selected memory devices **412'**B$_2$ and **412'**D$_2$), and the second data transmission circuit **416'**$_2$ is configurable to respond to module control signals by selectively allowing or inhibiting data transmission between the system memory controller **420'** and either selected memory devices **412'**A$_3$ and **412'**C$_3$ or selected memory devices **412'**B$_3$ and **412'**D$_3$ and either selected memory devices **412'**A$_4$ and **412'**C$_4$ or selected memory devices **412'**B$_4$ and **412'**D$_4$).

In certain embodiments, two or more of the data transmission circuits **416**, **416'** are mechanically coupled to the at least PCB **410**, **410'** at corresponding positions which are separate from one another. For example, as schematically illustrated by FIG. **3**A, the first data transmission circuit **416**$_1$ and the second data transmission circuit **416**$_2$ are at corresponding positions which are separate from one another (e.g., the package containing the first data transmission circuit **416**$_1$ is at a location spaced from the location of the package containing the second data transmission circuit **416**$_2$). For another example, as schematically illustrated by FIG. **3**B, the first data transmission circuit **416'**$_1$ and the second data transmission circuit **416'**$_2$ are at corresponding positions which are separate from one another (e.g., the package containing the first data transmission circuit **416'**$_1$ is at a location spaced from the location of the package containing the second data transmission circuit **416'**$_2$). In certain such embodiments, two or more of the data transmission circuits **416**, **416'** are distributed across a surface of the PCB **410**, **410'** of the memory module **402**, **402'**. In certain embodiments, the corresponding positions of two or more data transmission circuits **416**, **416'** (e.g., first data transmission circuit **416**$_1$ and second data transmission circuit **416**$_2$ of FIG. **3**A or first data transmission circuit **416'**$_1$ and second data transmission circuit **416'**$_2$ of FIG. **3**B) are along an edge **411**, **411'** of the at least one PCB **410**, **410'** such that a data transmission circuit **416**, **416'** is located substantially between the edge **411**, **411'** and at least some of the at least two memory devices **412**, **412'** to which the data transmission circuit **416**, **416'** is operatively coupled. For example, as schematically illustrated by FIG. **3**A, the first data transmission circuit **416**$_1$ is located substantially between the edge **411** and the memory devices **412**A$_1$, **412**B$_1$, **412**C$_1$, **412**D$_1$ to which the first data transmission circuit **416**$_1$ is operatively coupled, and the second data transmission circuit **416**$_2$ is located substantially between the edge **411** and the memory devices **412**A$_2$, **412**B$_2$, **412**C$_2$, **412**D$_2$ to which the second data transmission circuit **416**$_1$ is operatively coupled. For another example, as schematically illustrated by FIG. **3**B, the first data transmission circuit **416'**$_1$ is located substantially between the edge **411'** and the memory devices **412'**A$_1$, **412'**A$_2$, **412'**B$_1$, **412'**B$_2$, **412'**C$_1$, **412'**C$_2$, **412'**D$_1$, **412'**D$_2$ to which the first data transmission circuit **416'**$_1$ is operatively coupled, and the second data transmission circuit **416'**$_2$ is located substantially between the edge **411'** and the memory devices **412'**A$_3$, **412'**A$_4$ **412'**B$_3$, **412'**B$_4$, **412'**C$_3$, **412'**C$_4$, **412'**D$_3$, **412'**D$_4$ to which the second data transmission circuit **416'**$_2$ is operatively coupled.

FIGS. **3**C and **3**D illustrate the positioning of the data transmission circuits **416'** in accordance with certain embodiments described herein. In certain embodiments, the position of at least one of the data transmission circuits **416'**

is generally aligned with one or more of the memory devices **412'** to which the data transmission circuit **416'** is operatively coupled. For example, the one or more of the data transmission circuits **416'** and the memory devices **412'** to which it is operatively coupled can be positioned generally along a line that is substantially perpendicular to the edge **411'** of the PCB **410'**. In certain embodiments, the position of at least one of the data transmission circuits **416'** is generally offset from a line defined by the positions of the one or more of the memory devices **412'** to which the data transmission circuit **416'** is operatively coupled. For example, as shown in FIGS. **3**C and **3**D, the memory devices **412'** operatively coupled to a data transmission circuit **416'** can be positioned along a line that is substantially perpendicular to the edge **411'** of the PCB **410'** and the data transmission circuit **416'** can be generally offset from this line in a direction generally along the edge **411'** of the PCB **410'**. In certain such embodiments, the data transmission circuits **416'** are sufficiently small in width and breadth (e.g., 2.5 mm by 7.5 mm) to fit between the edge **411'** and the corresponding memory devices **412'** while maintaining the desired size of the memory module **400'**. Other positions and sizes of the separate data transmission circuits **416'** are also compatible with certain embodiments described herein. For example, in certain embodiments, one or more of the data transmission circuits **416**, **416'** can be positioned between two or more memory devices **412**, **412'**, or can be spaced away from an edge **411**, **411'** of the PCB **410**, **410'** with one or more memory devices **412**, **412'** between the edge **411**, **411'** and the one or more data transmission circuits **416**, **416'**.

In certain embodiments, the data transmission circuit **416** comprises or functions as a byte-wise buffer. In certain such embodiments, each of the one or more data transmission circuits **416** has the same bit width as does the associated memory devices **412** per rank to which the data transmission circuit **416** is operatively coupled. For example, as schematically illustrated by FIG. **4**A (which corresponds generally to FIG. **3**A), the data transmission circuit **416** can be operatively coupled to a single memory device **412** per rank, and both the data transmission circuit **416** and the memory device **412** per rank to which the data transmission circuit **416** is operatively coupled can each have the same bit width (e.g., 4 bits, 8 bits, or 16 bits). The data transmission circuit **416** of FIG. **4**A has a bit width of 8 bits, and receives data bits **0-7** from the system memory controller **420** and selectively transmits the data bits **0-7** to selected memory devices **412**A, **412**B, **412**C, **412**D in response to the module control signals from the control circuit **430**. Similarly, data transmission circuits **416'** of certain embodiments can function as a byte-wise buffer for associated memory devices **412'**A, **412'**B, **412'**C, **412'**D to which the data transmission circuits **416'** are operatively coupled in response to the module control signals from the control circuit **430'**.

In certain other embodiments, the bit widths of one or more of the memory devices **412** may be different from the bit widths of the one or more data transmission circuits **416** to which they are connected. For example, as schematically illustrated by FIG. **4**B (which corresponds generally to FIG. **3**B), the data transmission circuits **416** may have a first bit width (e.g., a bit width of 8 bits) and the memory devices **412** may have a second bit width which is less than the first bit width (e.g., one-half the first bit width, or a bit width of 4 bits), with each data transmission circuit **416** operatively coupled to multiple memory devices **412** per rank (e.g., two memory devices **412** in each rank). In certain such embodiments, the total bit width of the multiple memory devices **412** per rank connected to the circuit **416** equals the bit width of the circuit **416** (e.g., 4 bits, 8 bits, or 16 bits). The data transmission circuit **416** of FIG. **4**B has a total bit width of 8 bits, and receives data bits **0-7** from the system memory controller **420** and selectively transmits data bits **0-3** to a first memory device **412**A_1, **412**B_1, **412**C_1, **412**D_1 and data bits **4-7** to a second memory device **412**A_2, **412**B_2, **412**C_2, **412**D_2 in response to the module control signals from the control circuit **430**. Similarly, data transmission circuits **416'** of certain embodiments can function with different bit widths than those of the associated memory devices **412'**A_1, **412'**A_2, **412'**B_1, **412'**B_2, **412'**C_1, **412'**C_2, **412'**D_1, **412'**D_2 to which the data transmission circuits **416'** are operatively coupled in response to the module control signals from the control circuit **430'**.

In certain embodiments, by having the data transmission circuit **416** comprise or serve as a "byte-wise" buffer (e.g., as shown in the examples of FIGS. **4**A and **4**B), the data signals are synchronous with the synch clock. In addition, for certain such embodiments in which the memory module **400** experiences variations in one or more characteristics (e.g., temperature, voltage, manufacturing parameters), the memory module **400** can be designed to optimize the circuits of a smaller number of components as compared to other configurations which do not utilize byte-wide buffering (e.g., having four ranks of 8-bit memory devices and having two 4-bit buffers). In certain embodiments, the data transmission circuits **416** are used for bit slicing in which the data are defined in sections. For example, rather than defining data to be 64-bit-wide (e.g., [63:0]), the data can be defined or sliced in 16-bit-wide sections (e.g., [15:0], [31:16], [47:32], [63:48]). In certain such embodiments, not all the bits are grouped together and not all the bits produce the same behavior (e.g., logic- and/or time-wise).

One or more of the data transmission circuits **416**, in accordance with an embodiment of this disclosure, is operatively coupled to a corresponding one or more of the data lines **452** connected to one or more memory devices **412** in each of the ranks A, B, C, D. For example, in certain embodiments, each data transmission circuit **416** is connected to one or more data lines **452** connected to one corresponding memory device in each of the ranks (e.g., memory devices **204**A, **204**B, **204**C, and **204**D, as shown in FIG. **3**A). Each data line **450**, **452** thus carries data from the system memory controller **420**, through the data transmission circuits **416**, to the memory devices **204**A, **204**B, **204**C, **204**D connected to the data transmission circuits **416**. The data transmission circuits **416** of certain embodiments may be used to drive each data bit to and from the memory controller **420** and the memory devices **412**, instead of the memory controller **420** and the memory devices **412** directly driving each data bit to and from the memory controller **420** and the memory devices **412**. Specifically, as described in more detail below, one side of each data transmission circuit **416** of certain embodiments is operatively coupled to a memory device **412** in each rank (e.g., via data lines **452**), while the other side of the data transmission circuit **416** is operatively coupled to the corresponding data line **450** of the memory controller **420**.

To reduce the memory device loads seen by the system memory controller **420** (e.g., during a write operation), the data transmission circuit **416** of certain embodiments is advantageously configured to be recognized by the system memory controller **420** as a single memory load. This advantageous result is desirably achieved in certain embodiments by using the data transmission circuits **416** to electrically couple only the enabled memory devices **412** to the memory controller **420** (e.g., the one, two, or more memory

devices **412** to which data is to be written) and to electrically isolate the other memory devices **412** from the memory controller **420** (e.g., the one, two, or more memory devices **412** to which data is not to be written). Therefore, during a write operation in which data is to be written to a single memory device **412** in a rank of the memory module **400**, each data bit from the system memory controller **420** sees a single load from the memory module **400**, presented by one of the data transmission circuits **416**, instead of concurrently seeing the loads of all of the four memory devices **412**A, **412**B, **412**C, **412**D to which the data transmission circuit **416** is operatively coupled. In the example of FIG. **3**A, during a write operation in which data is to be written to two memory device **412** in two ranks (e.g., memory devices **412**A and **412**C or memory devices **412**B and **412**D), each data bit from the system memory controller **420** sees a single load from the memory module **402**, which is presented by one of the data transmission circuits **416**, instead of concurrently seeing the loads of all of the four memory devices **412**A, **412**B, **412**C, **412**D to which the data transmission circuits **416** is operatively coupled. In comparison to the standard JEDEC four-rank DEVINI configuration (see FIG. **2**A and FIG. **2**B), the memory system **402** of certain embodiments may reduce the load on the system memory controller **420** by a factor of four.

FIG. **5** schematically illustrates an example data transmission circuit **416** compatible with certain embodiments described herein. In one embodiment, the data transmission circuits **416** includes control logic circuitry **502** used to control the various components of the data transmission circuit **416**, which may include one or more buffers, one or more switches, and one or more multiplexers among other components. The illustrated embodiment of FIG. **5** is 1-bit wide and switches a single data line **518** between the memory controller **420** and the memory devices **412**. In other embodiments, the data transmission circuit **416** may be multiple bits wide, for example, 8 bits, and switch a corresponding number of data lines **518**. In a multiple bit wide embodiment, the control logic circuitry **502** may be shared over the multiple bits.

As a part of isolating the memory devices **412** from the system memory controller **420**, in one embodiment, the data transmission circuits **416** allow for "driving" write data and "merging" read data. In the operational embodiment shown in FIG. **5**, in a write operation, data entering a data transmission circuit **416** via a data line **518** is driven onto two data paths, labeled path A and path B, preferably after passing through a write buffer **503**. The ranks of memory devices **412** are likewise divided into two groups with one group associated with path A and one group associated with path B. As shown in FIG. **3**A, rank A and rank C are in the first group, and rank B and rank D are in the second group. Accordingly, the memory devices **412**A, **412**C of rank A and rank C are connected to the data transmission circuits **416** by a first one of the two data paths, and the memory devices **412**B, **412**D of rank B and rank D are connected to the data transmission circuits **416** by a second one of the two data paths. In other embodiments, the driving of write data and merging of read data may be performed over more than two data paths.

As is known, Column Address Strobe (CAS) latency is a delay time which elapses between the moment the memory controller **420** informs the memory modules **402** to access a particular column in a selected rank or row and the moment the data for or from the particular column is on the output pins of the selected rank or row. The latency may be used by the memory module to control operation of the data transmission circuits **416**. During the latency, address and control signals pass from the memory controller **420** to the control circuit **430** which produces controls sent to the control logic circuitry **502** (e.g., via lines **432**) which then controls operation of the components of the data transmission circuits **416**.

For a write operation, during the CAS latency, the control circuit **430**, in one embodiment, provides enable control signals to the control logic circuitry **502** of each data transmission circuit **416**, whereby the control logic circuitry **502** selects either path A or path B to direct the data. Accordingly, when the control logic circuitry **502** receives, for example, an "enable A" signal, a first tristate buffer **504** in path A is enabled and actively drives the data value on its output, while a second tristate buffer **506** in path B is disabled with its output in a high impedance condition. In this state, the data transmission circuit **416** allows the data to be directed along path A to a first terminal Y**1**, which is connected to and communicates only with the first group of the memory devices **412**, e.g., those in ranks A and C. Similarly, if an "enable B" signal is received, the first tristate **504** opens path A and the second tristate **506** closes path B, thus directing the data to a second terminal Y**2**, which is connected to and communicates only with the second group of the memory devices **412**, e.g., those in ranks B and D.

For a read operation, the data transmission circuit **416** operates as a multiplexing circuit. In the illustrated embodiment of FIG. **5**, for example, data signals read from the memory devices **412** of a rank are received at the first or second terminals Y**1**, Y**2** of the data transmission circuit **416**. The data signals are fed to a multiplexer **508**, which selects one to route to its output. The control logic circuitry **502** generates a select signal to select the appropriate data signal, and the selected data signal is transmitted to the system memory controller **420** along a single data line **518**, preferably after passing through a read buffer **509**. The read buffer **509** may be a tristate buffer that is enabled by the control logic circuitry **502** during read operations. In another embodiment, the multiplexer **508** and the read buffer **509** may be combined in one component. In yet another embodiment, the multiplexer **508** and the read buffer **509** operations may be split over two tristate buffers, one to enable the value from Y**1** to the data line **518** and another to enable the value from Y**2** to the data line **518**.

The data transmission circuits **416** present a load on the data lines **518** from the write buffer **503** and the read buffer **509**. The write buffer **503** is comparable to an input buffer on one of the memory devices **412**, and the read buffer **509** is comparable to an output buffer on one of the memory devices **412**. Therefore, the data transmission circuits **416** present a load to the memory controller **420** that is substantially the same as the load that one of the memory devices **412** would present. Similarly, the data transmission circuits **416** present a load on the first and second terminals Y**1**, Y**2** from the multiplexer **508** and the first tristate buffer **504** (on the first terminal Y**1**) and the second tristate buffer **506** (on the second terminal Y**2**). The multiplexer **508** is comparable in loading to an input buffer on the memory controller **420**, and the first and second tristate buffers **504**, **506** are each comparable to an output buffer on the memory controller **420**. Therefore, the data transmission circuits **416** present a load to the memory devices **412** that is substantially the same as the load that the memory controller **420** would present.

Additionally, the data transmission circuits **416** operate to ameliorate quality of the data signals passing between the memory controller **420** and the memory devices **412**. With-

out the data transmission circuits **416**, waveforms of data signals may be substantially degraded or distorted from a desired shape between source and sink. For example, signal quality may be degraded by lossy transmission line characteristics, mismatch between characteristics of transmission line segments, signal crosstalk, or electrical noise. However, in the read direction, the read buffer **509** regenerates the signals from the memory devices **412** thereby restoring the desired signal waveform shapes. Similarly, in the write direction, the first tristate buffer **504** and the second tristate buffer **506** regenerate the signals from the memory controller **420** thereby restoring the desired signal waveform shapes.

Referring again to FIG. **3**A, when the memory controller **420** executes read or write operations, each specific operation is targeted to a specific one of the ranks A, B, C, and D of a specific memory module **402**. The data transmission circuit **416** on the specifically targeted one of the memory modules **402** functions as a bidirectional repeater/multiplexor, such that it drives the data signal when connecting from the system memory controller **420** to the memory devices **412**. The other data transmission circuits **416** on the remaining memory modules **402** are disabled for the specific operation. For example, the data signal entering on data line **518** entering into data transmission circuit **416** is driven to memory devices **412**A and **412**C or **412**B and **412**C depending on which memory devices are active and enabled. The data transmission circuit **416** then multiplexes the signal from the memory devices **412**A, **412**B, **412**C, **412**D to the system memory controller **420**. The data transmission circuits **416** may each control, for example, a nibble-wide data path or a bytewide-data path. As discussed above, the data transmission circuits **416** associated with each module **402** are operable to merge data read signals and to drive data write signals, enabling the proper data paths between the system memory controller **420** and the targeted or selected memory devices **412**. Thus, the memory controller **420**, when there are four four-rank memory modules, sees four load-reducing switching circuit loads, instead of sixteen memory device loads. The reduced load on the memory controller **420** enhances the performance and reduces the power requirements of the memory system, as compared with, for example, the conventional systems described above with reference to FIGS. **1**A, **1**B and **2**A-**2**D.

Operation of a memory module using the data transmission circuit **416** may be further understood with reference to FIG. **6**, an illustrative timing diagram of signals of the memory module **402**. The timing diagram includes first through eighth time periods **601**-**608**. When the memory devices **404** are synchronous memories, each of the time periods **601**-**608** may correspond to one clock cycle of the memory devices **404**.

The first, second, and third time periods **601**-**603** illustrate write operations with data passing from the memory controller **401** to the memory module **402**. The fourth time period **604** is a transition between the write operations and subsequent read operations. The timing diagram shows a write operation to the first group of memory devices **412**A, **412**C connected to the first terminals Y**1** of the data transmission circuits **416** and a write operation to the second group of memory devices **412**B, **412**D connected to the second terminals Y**2** of the data transmission circuits **416**. Recalling the CAS latency described above, each write operation extends over two time periods in a pipelined manner.

The write to the first group of memory devices **412**A, **412**C appears in the first time period **601** when system address and control signals **440** pass from the memory controller **420** to the module controller **430**. The control circuit **430** evaluates the address and control signals **440** to determine that data is to be written to memory devices **412**A, **412**C in the first group. During the second time period **602**, the control circuit **430** supplies control signals to the control logic circuitry **502** to enable the first tristate buffer **504** and to disable the second tristate buffer **506** and the read buffer **509**. Thus, during the second time period **602**, data bits pass from the data lines **518** to the first terminal Y**1** and on to the memory devices **412**A, **412**C.

Similarly, the write to the second group of memory devices **412**A, **412**C appears in the second time period **602** when system address and control signals **440** pass from the memory controller **420** to the control circuit **430**. The control circuit **430** evaluates the address and control signals **440** to determine that data is to be written to memory devices **412**B, **412**D in the second group. During the third time period **603**, the control circuit **430** supplies control signals to the control logic circuitry **502** to enable the second tristate buffer **506** and to disable the first tristate buffer **504** and the read buffer **509**. Thus, during the third time period **603**, data bits pass from the data lines **518** to the second terminal Y**2** and on to the memory devices **412**B, **412**D.

The fifth, sixth, seventh, and eighth time periods **605**-**608** illustrate read operations with data passing to the memory controller **420** from the memory module **402**. The timing diagram shows a read operation from the first group of memory devices **412**A, **412**C connected to the first terminals Y**1** of the data transmission circuits **416** and a read operation from the second group of memory devices **412**B, **412**D connected to the second terminals Y**2** of the data transmission circuits **416**. Recalling the CAS latency described above, each read operation extends over two time periods in a pipelined manner.

The read from the first group of memory devices **412**A, **412**C appears in the fifth time period **605** when system address and control signals **440** pass from the memory controller **420** to the control circuit **430**. The control circuit **430** evaluates the address and control signals **440** to determine that data is to be read from memory devices **412**A, **412**C in the first group. During the sixth time period **606**, the control circuit **430** supplies control signals to the control logic circuitry **502** to cause the multiplexer **58** to select data from the first terminal Y**1**, to enable the read buffer **509**, and to disable the first tristate buffer **504** and the second tristate buffer **506**. Thus, during the sixth time period **606**, data bits pass from the memory devices **412**A, **412**C via the first terminal Y**1** to data lines **518** and on to the memory controller **420**.

The read from the second group of memory devices **412**B, **412**D appears in the seventh time period **607** when system address and control signals **440** pass from the memory controller **420** to the control circuit **430**. The control circuit **430** evaluates the address and control signals **440** to determine that data is to be read from memory devices **412**B, **412**D in the second group. During the eighth time period **608**, the control circuit **430** supplies control signals to the control logic circuitry **502** to cause the multiplexer **508** to select data from the second terminal Y**2**, to enable the read buffer **509**, and to disable the first tristate buffer **504** and the second tristate buffer **506**. Thus, during the eighth time period **606**, data bits pass from the memory devices **412**B, **412**D via the second terminal Y**2** to data lines **518** and on to the memory controller **420**.

Various embodiments have been described above. Although this invention has been described with reference to

these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined in the appended claims.

We claim:

1. A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising:

a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket;

double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks;

a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals; and

a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals, wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side, wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines;

wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period; and

wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period.

2. The memory module of claim **1**, wherein the DDR DRAM devices each has a bit width of 4 bits, wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a respective pair of DDR DRAM devices, and wherein a first subset of the first tristate buffers is enabled for the first time period to drive a first nibble of the respective byte-wise section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks, while a second subset of the first tristate buffers is enabled for the first time period to drive a second nibble of the respective byte-wise section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks.

3. The memory module of claim **2**, wherein the byte-wise data path further includes a set of write buffers configurable to receive the respective byte-wise section of the N-bit wide write data from the respective set of data signal lines before the first tristate buffers regenerate and drive the respective byte-wise section of the N-bit wide data to the second side of the each respective byte-wise buffer.

4. The memory module of claim **3**, wherein each of the write buffers is comparable to an input buffer on one of the DDR DRAM devices such that the each respective byte-wise buffer presents to the memory controller one DDR DRAM device load during the memory operation.

5. The memory module of claim **1**, wherein the DDR DRAM devices each has a bit width of 8 bits, and wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a single DDR DRAM device.

6. The memory module of claim **1**, wherein the logic is configurable to enable the first tristate buffers at a beginning of the first time period and to disable the first tristate buffers at an end of first time period.

7. The memory module of claim **1**, wherein the module controller is configured to use the module control signals to control timing of the first time period in accordance with the latency parameter.

8. The memory module of claim **1**, wherein the registered address and control signals include rank select signals, the rank select signals including one rank select signal for each of the multiple N-bit-wide ranks, and wherein the rank select signal received by the first N-bit-wide rank is different from the rank select signal received by any other N-bit-wide rank of the multiple N-bit-wide ranks.

9. The memory module of claim **8**, wherein each of the respective module data lines is configured to carry data from the memory controller to a corresponding memory device in each of the multiple N-bit-wide ranks during the memory write operation.

10. The memory module of claim **1**, wherein:

the module controller is further configurable to receive from the memory controller via the address and control signal lines additional input address and control signals for a memory read operation to read N-bit-wide read data from the memory controller from a second N-bit-wide rank of the multiple N-bit-wide ranks, and to output additional registered address and control signals in response to the additional input address and control signals;

the second N bit-wide rank is configurable to output the N bit-wide read data associated with the memory read

operation in response to at least some of the additional registered address and control signals;

the module controller is further configurable to output additional module control signals in response to the additional input address and control signals;

the logic in the each respective byte-wise buffer is further configurable to control the byte-wise data path in response to the additional module control signals, wherein the byte-wise data path is enabled for a second time period to actively drive a respective byte-wise section of the N bit wide read data associated with the memory read operation from the second side to the first side during the second time period in response to the additional module control signals;

the byte-wise data path further includes second tristate buffers configurable to be enabled by the logic to drive the respective byte-wise section of the N-bit wide read data to the respective set of data signal lines during the second time period; and

the second tristate buffers are disabled during the first time period and the first tristate buffers are disabled during the second time period.

11. A N-bit-wide memory module mountable in a memory socket of a computer system and configured to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, the memory module comprising:

a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and are configured to be releasably coupled to corresponding contacts of the memory socket;

double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks, each N-bit-wide rank includes n DDR DRAM devices;

n/2 data transmission circuits mounted on the PCB, wherein each of the n/2 data transmission circuits is disposed on the PCB at respective positions corresponding to a respective set of data signal lines among the plurality of sets of data signal lines, and wherein the each of the n/2 data transmission circuits has a first side configured to be operatively coupled to the respective set of data signal lines, a second side that is operatively coupled to a respective pair of DDR DRAM devices in each of the multiple ranks via respective module data lines, and data paths between the first side and the second side;

a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, the module controller being configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank among the multiple N-bit-wide ranks, and to output registered address and control signals in response to the input address and control signal, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to transmit module control signals to the n/2 data transmission circuits in response to the input address and control signals; and

wherein, in response to the module control signals, each respective data transmission circuit is configurable to enable the data paths for a first time period in accordance with a latency parameter to actively drive a respective section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period, wherein a first subsection of the respective section of the N-bit wide write data output from the second side of the each respective data transmission circuit is written into a first one of the respective pair of DDR DRAM devices in the first N-bit wide rank, while a second subsection of the respective section of the N-bit wide write data output from the second side of the each respective data transmission circuit is written into a second one of the respective pair of DDR DRAM devices in the first N-bit wide rank; and

wherein the data paths includes first tristate buffers, and the respective data transmission circuit in response to the module control signals is configured to enable a first subset of the first tristate buffers to drive the first subsection of the respective section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks, and to enable a second subset of the first tristate buffers to drive a second subsection of the respective section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks.

12. The memory module of claim **11**, wherein the registered address and control signals include a rank select signal for each of the multiple N-bit wide ranks, the rank select signal for the first N-bit wide rank is different from the rank select signal for any other N-bit wide rank of the multiple N-bit wide ranks.

13. The memory module of claim **12**, wherein each of the respective module data lines is configured to carry data from the memory controller to a corresponding memory device in each of the multiple N-bit-wide ranks during the memory operation.

14. The memory module of claim **13**, wherein the data paths further include a set of write buffers configurable to receive the respective section of the N-bit wide data from the respective set of data signal lines before the respective section of the N-bit wide write data is regenerated and driven by—the first tristate buffers to the respective module data lines.

15. The memory module of claim **14**, wherein each of the set of write buffers is comparable in loading to an input buffer on one of the DDR DRAM devices such that the each respective data transmission circuit presents to the memory controller one DDR DRAM device load during the memory write operation.

16. The memory module of claim **11**, wherein the module controller is configurable to use the module control signals to control timing of the first time period in accordance with the latency parameter.

17. The memory module of claim **11**, wherein the each respective data transmission circuit is configured to present to the memory controller one DDR DRAM device load on each of the respective set of data lines during the memory write operation.

18. The memory module of claim **11**, wherein:

the module controller is further configurable to receive from the memory controller via the address and control signal lines additional input address and control signals

for a subsequent memory read operation to read N bit-wick: read data from a second N-bit-wide rank of the multiple N-bit-wide ranks, and to output additional registered address and control signals in response to the additional input address and control signals;

the second N-bit-wide rank of the multiple N-bit-wide ranks is configurable to output the N-bit-wide read data associated with the memory read operation in response to at least some of the additional registered address and control signals;

the module controller is further configurable to output additional module control signals in response to the additional input address and control signals; and

the each respective data transmission circuit is further configurable to enable the data paths for a second time period to actively drive a respective section of the N-bit wide read data associated with the memory read operation from the second side to the first side during the second time period in response to the additional module control signals;

the data paths further includes second tristate buffers configurable to be enabled during the second time period to drive the respective section of the N-bit wide read data to the respective set of data signal lines; and

the each respective data transmission circuit is further configurable to keep the second tristate buffers disabled during the first time period and to keep the first tristate buffers disabled during the second time period.

19. A N-bit-wide memory module mountable in a memory socket of a computer system and configured to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, the memory module comprising:

a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and are configured to be releasably coupled to corresponding contacts of the memory socket;

double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks;

a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, the module controller being configurable to receive from the memory controller via the address and control signal lines first address and control signals for a first memory operation to read first N-bit-wide data from a first N-bit-wide rank among the multiple ranks and to subsequently receive second address and control signals for a second memory operation to read second N-bit-wide data from a second N-bit-wide rank among the multiple ranks, the module controller being further configurable to output first registered address and control signals for the first memory operation in response to receiving the first address and control signals and to output second registered address and control signals for the second memory operation in response to receiving the second address and control signals, wherein the first registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N-bit-wide data associated with the second memory operation, wherein the module controller is further configurable to output first module control signals for the first memory operation in response to receiving the first address and control signals and to output second module control signals for the second memory operation in response to receiving the second address and control signals; and

a plurality of buffers coupled to the PCB and configured to receive the first module control signals and to receive the second module control signals, wherein each respective buffer of the plurality of buffers has a first side that is operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and data paths between the first side and the second-side, wherein the each respective buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines;

wherein the each respective buffer further includes logic configurable to enable the data paths for a first time period to actively drive a respective section of the first N-bit wide data associated with the first memory operation from the second side to the first side during the first time period, and to enable the data paths for a second time period subsequent to the first time period to actively drive a respective section of the second N-bit wide data associated with the second memory operation from the second side to the first side during the second time period, wherein the data paths are disabled after the first time period and before the second time period.

20. The memory module of claim **19**, wherein the DDR DRAM devices each has a bit width of 4 bits, wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a respective pair of DDR DRAM devices, and wherein a first nibble of the respective section of the first N bit wide data is output by a first one of the respective pair of DDR DRAM devices in the first N-bit wide rank, while a second nibble of the respective section of the first N bit wide data is output by a second one of the respective pair of DDR DRAM devices in the first N-bit wide rank.

21. The memory module of claim **19**, wherein the module controller is configured to use the first module control signals to control timing of the first time period in accordance with a latency parameter and to use the second module control signals to control timing of the second time period in accordance with the latency parameter.

22. The memory module of claim **19**, wherein the each respective buffer is configured to present to the at least one respective DDR DRAM device a load that is similar to that of the memory controller during the first or the second memory operation.

23. The memory module of claim **19**, wherein the first registered address and control signals include a first set of rank select signals corresponding to respective ones of the multiple N-bit wide ranks, the first set of rank select signals including a first rank select signal received by the first N-bit wide rank that is different from each of the other rank select signals in the first set of rank select signals, and wherein the second registered address and control signals include a second set of rank select signals corresponding to respective ones of the multiple N-bit wide ranks, the second set of rank select signals including a second rank select signal received by the second N-bit wide rank that is different from each of the other rank select signals in the second set of rank select signals.

24. The memory module of claim **23**, wherein each of the respective module data lines is configured to carry data from

the memory controller to a corresponding memory device in each of the multiple N-bit-wide ranks.

25. The memory module of claim **19**, wherein the data path includes at least a first input buffer and a second buffer for each bit of the respective section of the first or second N-bit wide data, wherein the first buffer is configured to receive the each bit from the second side of the each respective buffer, and the second buffer is configured to regenerate and drive the each bit to the first side of the each respective buffer, wherein at least the second buffer is a tristate buffer configurable to be enabled by the logic in response to the first or second module control signals, and wherein the first buffer is comparable to an output buffer on one of the DDR DRAM devices.

26. The memory module of claim **19**, wherein the data paths include a set of input buffers configurable to receive the respective section of the first or second N-bit wide data from the respective set of module data lines and a set of output buffers configurable to regenerate and drive the respective section of the first or second N-bit wide data to the first side, wherein at least the set of output buffers are tristate buffers configurable to be enabled by the logic during the first time period in response to the first module control signals and during the second time period in response to the second module control signals, and wherein at least the set of output buffers are disabled by the logic after the first time period and before the second time period.

27. A memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and data signal lines, the data signal lines including a plurality of sets of data signal lines, each set of data signal lines is n bit wide, the memory module comprising:

a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and are configured to be releasably coupled to corresponding contacts of the memory socket;

a module controller coupled to the PCB and configurable to receive from the memory controller via the address and control signal lines first address and control signals for a memory write operation and to subsequently receive second address and control signals for a memory read operation, the module controller being further configurable to output first registered address and control signals and first module control signals for the memory write operation in response to the first address and control signals, and to output second registered address and control signals and second module control signals for the memory read operation in response to the second address and control signals; and

double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and configurable to perform the memory write operation by receiving write data in response to the first registered address and control signals, and to perform the memory read operation by outputting read data in response to the second registered address and control signals; and

a plurality of n-bit-wide data buffers coupled to the PCB and configured to receive the first module control signals and subsequently the second module control signals, wherein each respective n-bit-wide data buffer of the plurality of n-bit-wide data buffers has a first side that is operatively coupled to a respective set of data signal lines, and a second side that is operatively coupled to a respective n-bit-wide section of the DDR DRAM devices via respective module data lines, wherein:

the each respective n-bit-wide data buffer includes a first set of input buffers configurable to receive a respective n-bit section of the write data from the respective set of data signal lines, a first set of tristate buffers configurable to drive the respective n-bit section of the write data to the respective module data lines, a second set of input buffers configurable to receive a respective n-bit section of the read data from the respective module data lines, a second set of tristate buffers configurable to drive the respective n-bit section of the read data to the respective set of data signal lines, and logic configurable to control at least the first set of tristate buffers and the second set of tristate buffers;

the logic in response to the first module control signals is configured to enable the first set of tristate buffers for a first time period corresponding to the memory write operation to drive the respective n-bit section of the write data;

the logic in response to the second module control signals is configured to enable the second set of tristate buffers for a second time period corresponding to the memory read operation to drive the respective n-bit section of the read data;

the first set of tristate buffers are disabled during the second time period; and

the second set of tristate buffers are disabled during the first time period.

28. The memory module of claim **27**, wherein the logic is configurable to keep the first set of tristate buffers and the second set of tristate buffers disabled when the memory module is not targeted by the memory controller for any memory operations.

29. The memory module of claim **27**, wherein:

the DDR DRAM devices include a plurality of ranks of DDR DRAM devices;

the each respective n-bit-wide buffer is coupled to at least one respective DDR DRAM device in each of the plurality of ranks via the respective module data lines;

the first registered address and control signals cause one rank of DDR DRAM devices to perform the memory write operation by receiving the write data; and

the second registered address and control signals cause one rank of DDR DRAM devices to perform the memory read operation by outputting the read data.

30. The memory module of claim **29**, wherein:

the at least one respective DDR DRAM device in each of the plurality of ranks includes a respective pair of DDR DRAM devices;

a first n/2-bit section of the respective n-bit section of the write_data is driven by a first subset of the first set of tristate buffers to a first one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory write operation;

a second n/2-bit section of the respective n-bit section of the write_data is driven by a second subset of the first set of tristate buffers to a second one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory write operation;

a first n/2-bit section of the respective n-bit section of the read_data is received by a first subset of the second set of input buffers from a first one of the respective pair

of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory read operation; and

a second n/2-bit section of the respective n-bit section of the read_data is received by a second subset of the second set of input buffers from the second one of the respective pair of DDR DRAM devices in the one rank of DDR DRAM devices performing the memory read operation.

31. The memory module of claim **29**, wherein:

the at least one respective DDR DRAM device in each of the plurality of ranks includes one respective DDR DRAM;

the respective n-bit section of the write_data is driven by the first set of tristate buffers to the respective DDR DRAM device in the one rank of DDR DRAM devices performing the memory write operation; and

the respective n-bit section of the read_data is received by the second set of input buffers from the respective DDR DRAM device in the one rank of DDR DRAM devices performing the memory read operation.

32. The memory module of claim **29**, wherein each of the respective module data lines is configured to carry data from the memory controller to a corresponding memory device in each of the plurality of ranks.

33. The memory module of claim **29**, wherein:

the module controller is further configurable to receive from the memory controller via the address and control signal lines third address and control signals for a subsequent memory read operation, and to output third registered address and control signals and third module control signals for the subsequent memory read operation in response to receiving the third address and control signals;

the DDR DRAM devices are configurable to perform the subsequent memory read operation by outputting additional read data in response to the third registered address and control signals;

the subsequent memory read operation is performed by another rank of DDR DRAM devices that is different from the one rank of DDR DRAM devices performing the memory read operation;

the logic in response to the third module control signals enables the second set of tristate buffers for a third time period corresponding to the subsequent memory read operation to drive a respective n-bit section of the additional read data; and

the logic is further configurable to disable the second set of tristate buffers after the second time period and before the third time period.

34. The memory module of claim **27**, wherein the first set of tristate buffers are enabled for the first time period in accordance with a latency parameter.

35. The memory module of claim **27**, wherein the second set of tristate buffers are enabled for the second time period in accordance with a latency parameter.

* * * * *

Exhibit 3

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(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 11,016,918 B2**
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(54) **FLASH-DRAM HYBRID MEMORY MODULE**

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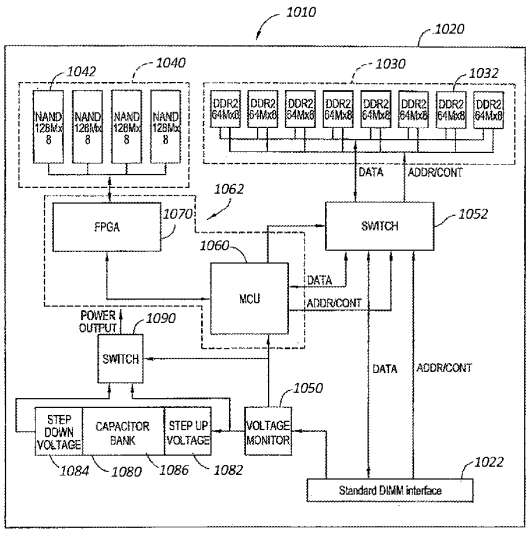
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(57) **ABSTRACT**

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

30 Claims, 22 Drawing Sheets



Related U.S. Application Data

No. 14/840,865, filed on Aug. 31, 2015, now Pat. No. 9,928,186, which is a continuation of application No. 14/489,269, filed on Sep. 17, 2014, now Pat. No. 9,158,684, which is a continuation of application No. 13/559,476, filed on Jul. 26, 2012, now Pat. No. 8,874,831, which is a continuation-in-part of application No. 12/240,916, filed on Sep. 29, 2008, now Pat. No. 8,301,833, which is a continuation of application No. 12/131,873, filed on Jun. 2, 2008, now abandoned.

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USPC 711/103, 104, 105; 710/138

See application file for complete search history.

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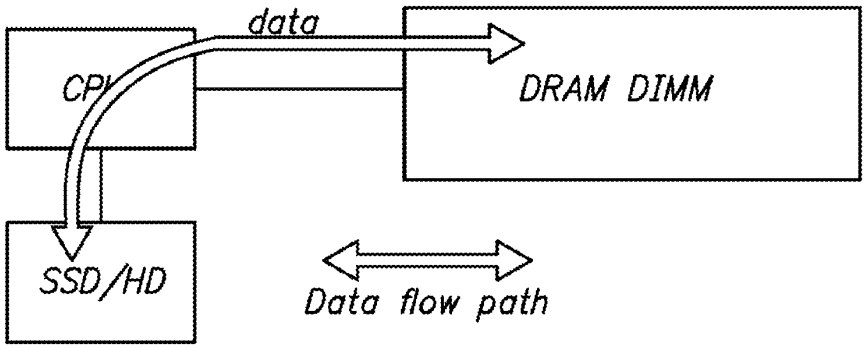


FIG. 1
(PRIOR ART)

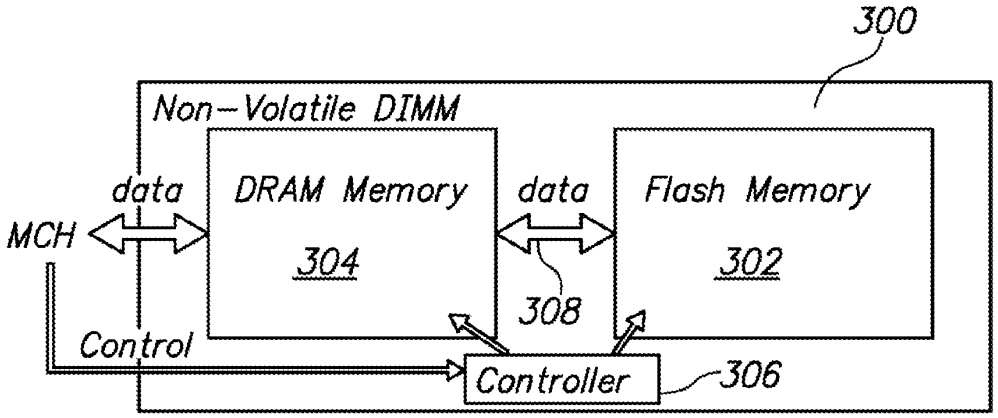


FIG. 3A

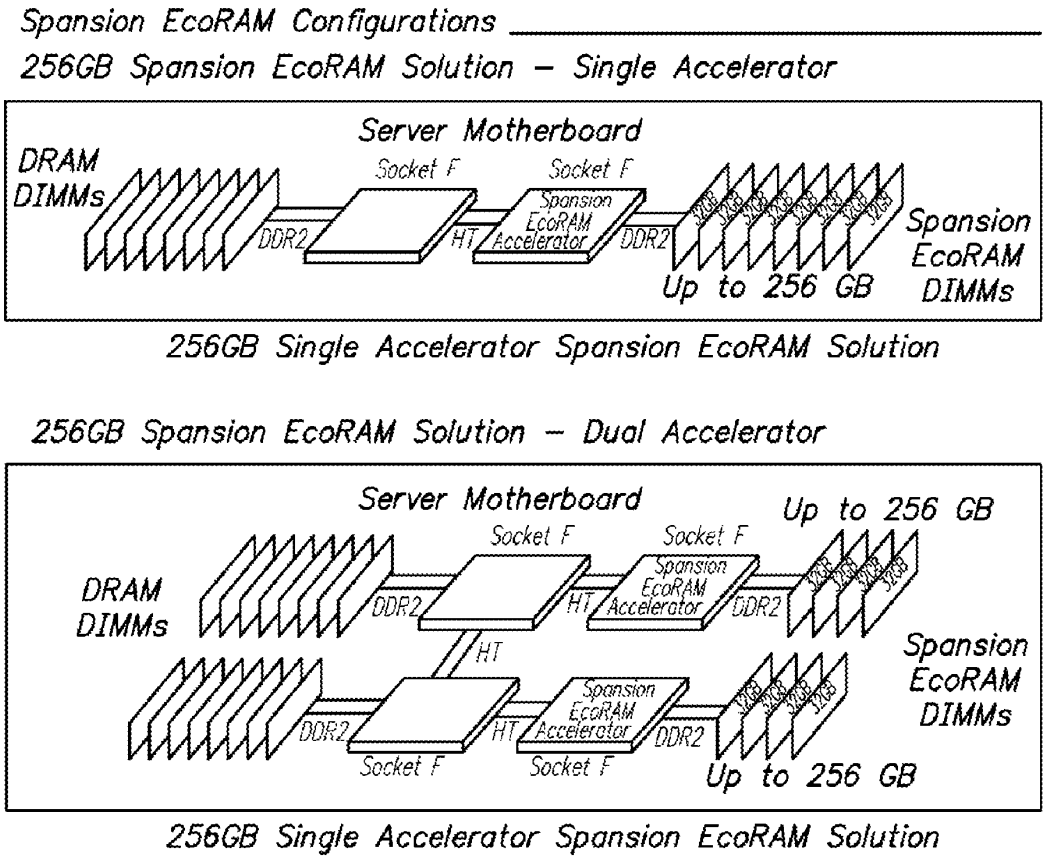


FIG. 2
(PRIOR ART)

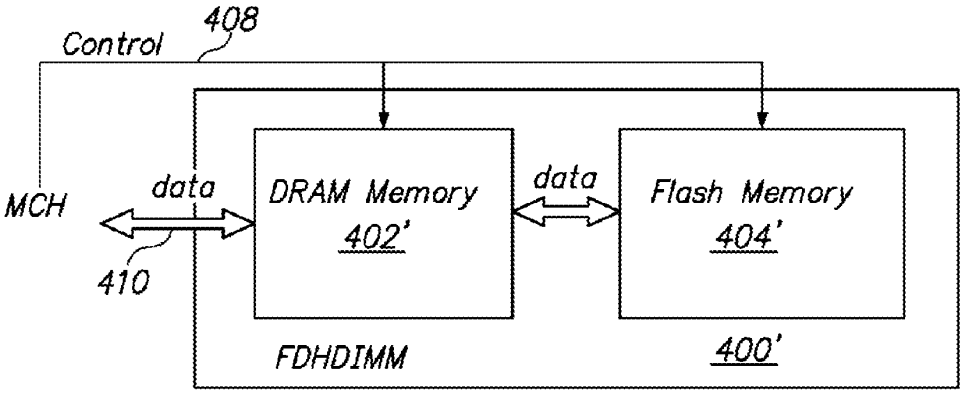


FIG. 4B

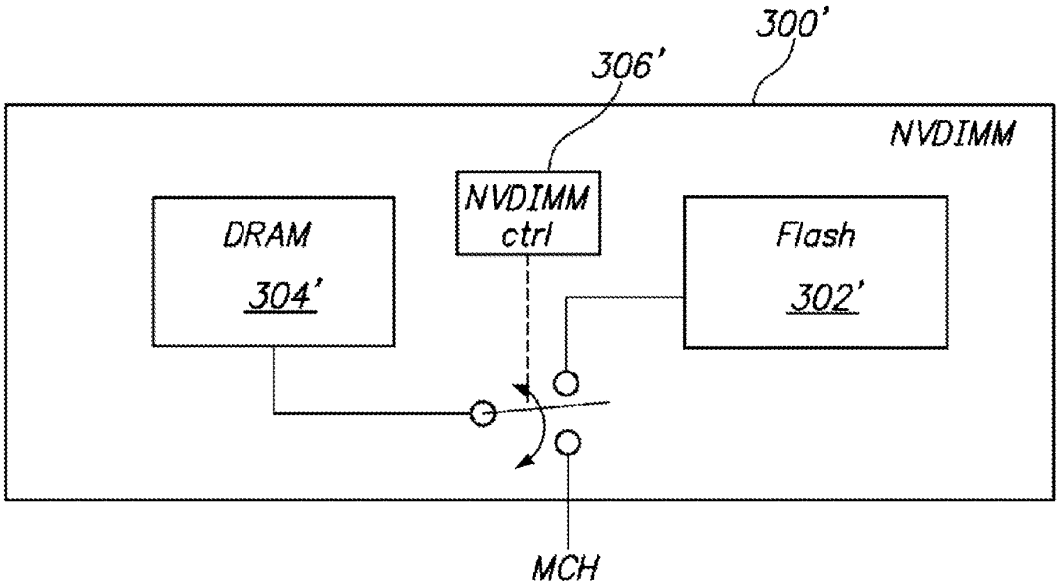

300'
306'
NVDIMM
NVDIMM ctrl
DRAM
304'
Flash
302'
MCH

FIG. 3B

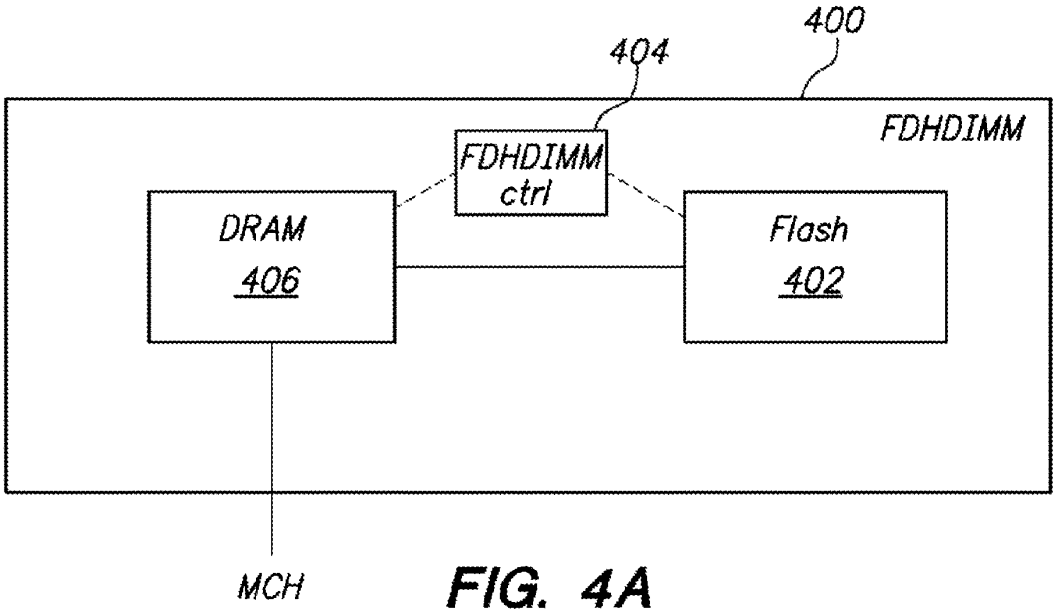

400
404
FDHDIMM
FDHDIMM ctrl
DRAM
406
Flash
402
MCH

FIG. 4A

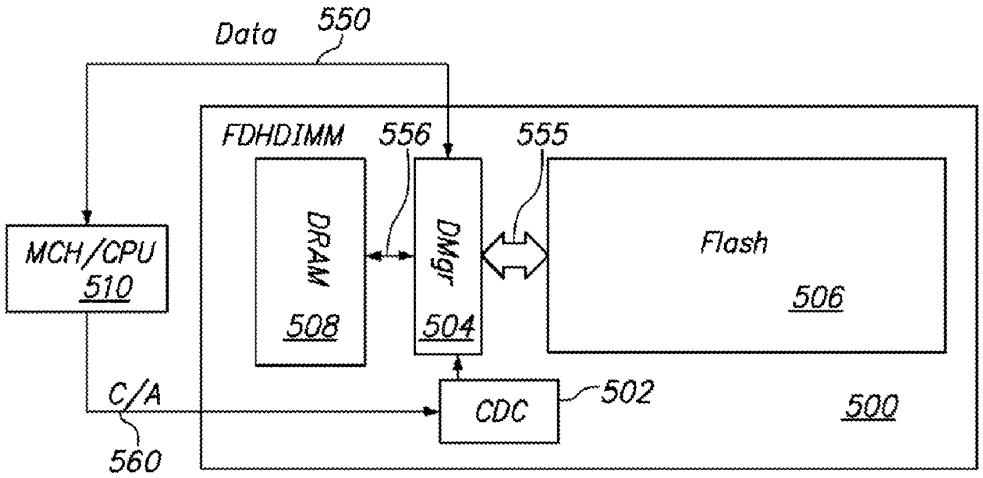

Data
550
FDHDIMM
556
555
DRAM
508
DMgr
504
Flash
506
MCH/CPU
510
C/A
560
CDC
502
500

FIG. 5A

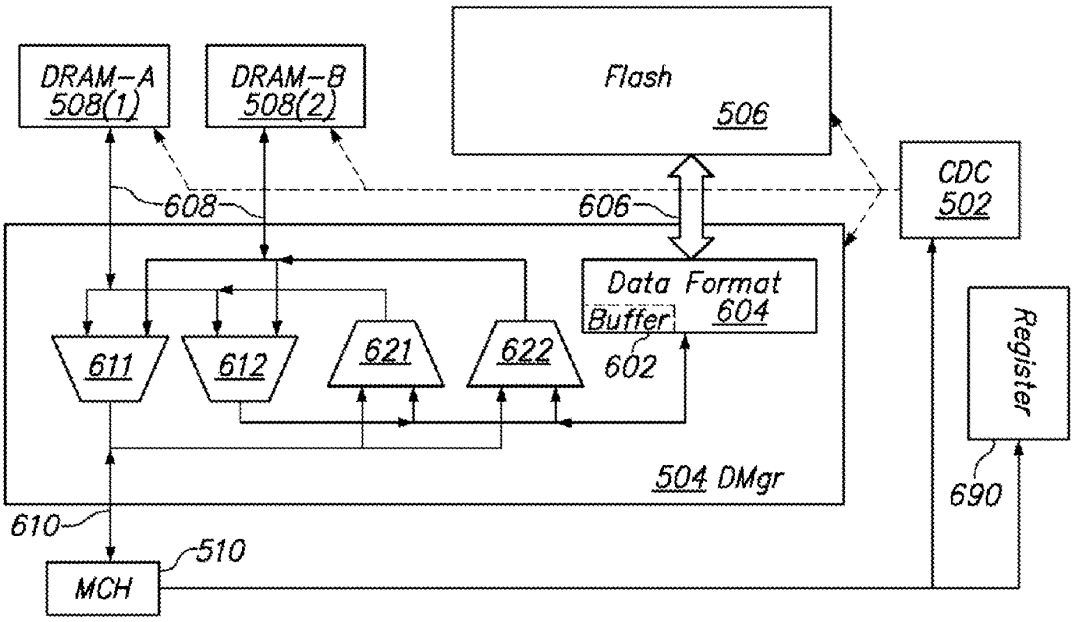

DRAM-A
508(1)
DRAM-B
508(2)
Flash
506
CDC
502
608
606
Data Format
Buffer
604
602
611
612
621
622
504 DMgr
Register
690
610
510
MCH

FIG. 6

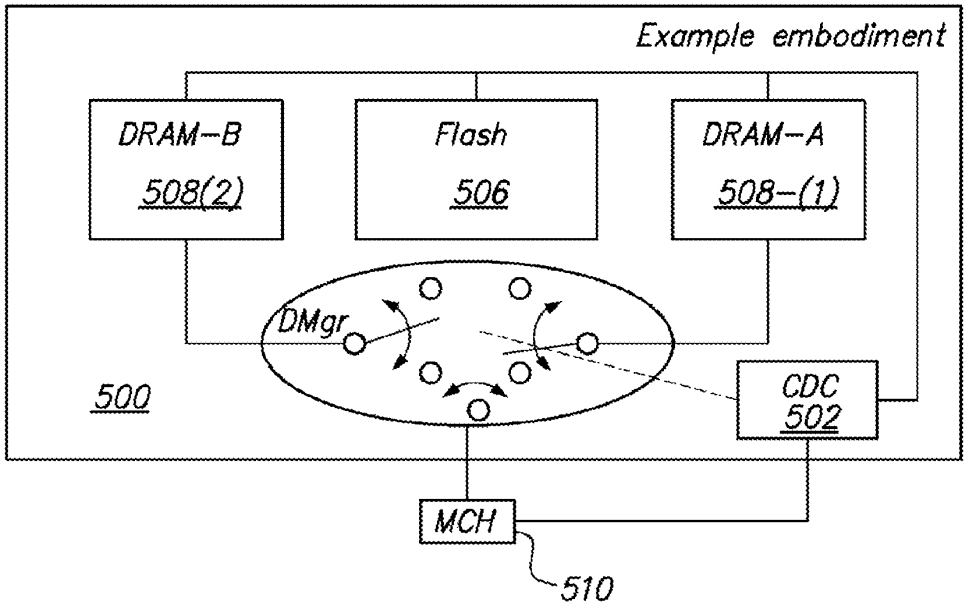

Example embodiment
DRAM–B
508(2)
Flash
506
DRAM–A
508–(1)
DMgr
500
CDC
502
MCH
510

FIG. 5B

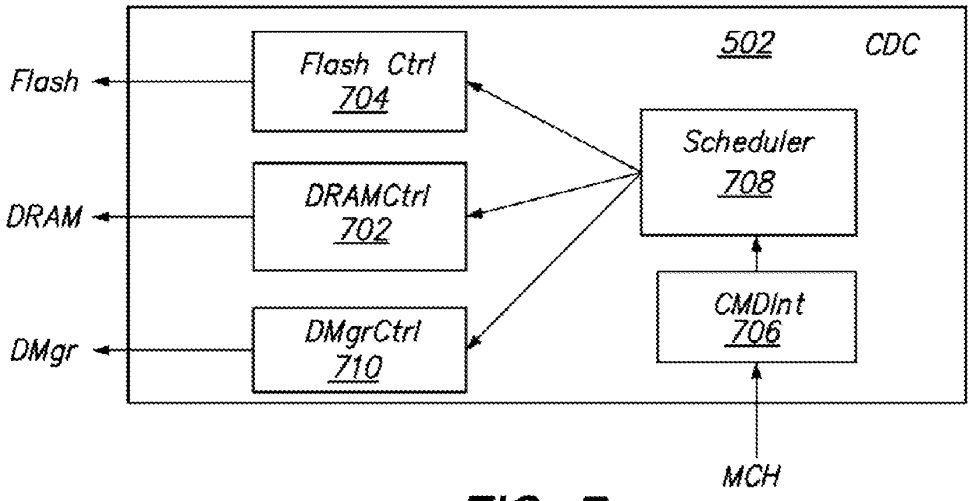

Flash
DRAM
DMgr
Flash Ctrl
704
DRAMCtrl
702
DMgrCtrl
710
502
CDC
Scheduler
708
CMDInt
706
MCH

FIG. 7

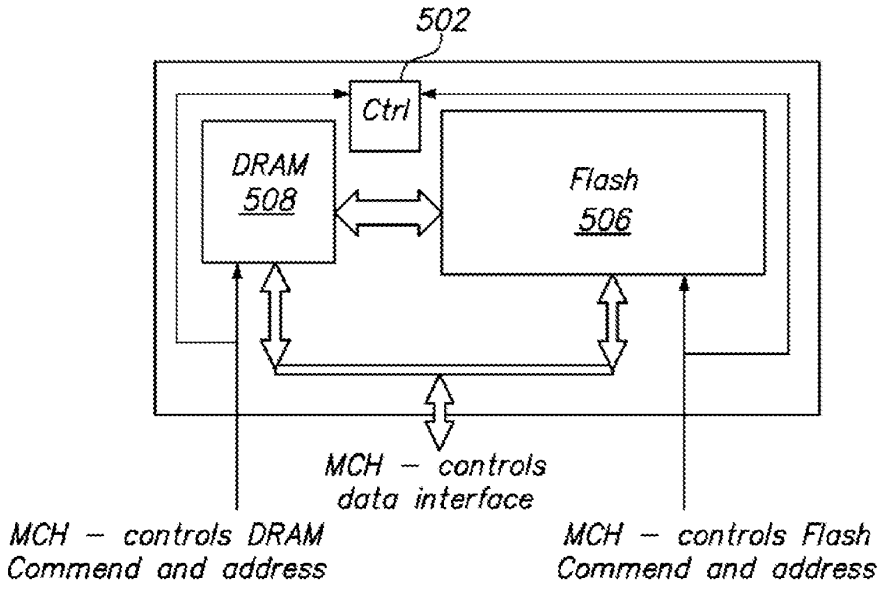

502
Ctrl
DRAM
508
Flash
506
MCH – controls
data interface
MCH – controls DRAM
Commend and address
MCH – controls Flash
Commend and address

FIG. 8A

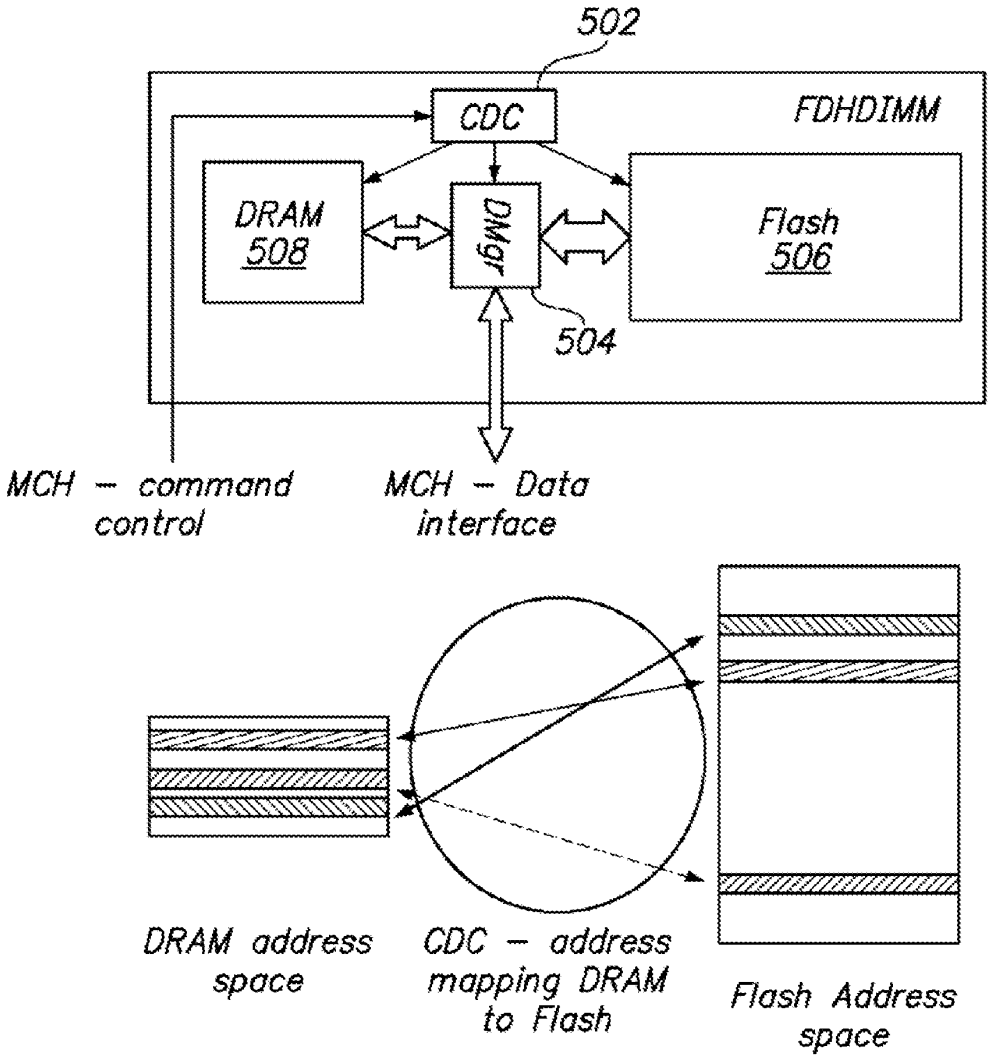

502
CDC
FDHDIMM
DRAM
508
DMGT
Flash
506
504
MCH – command control
MCH – Data interface
DRAM address space
CDC – address mapping DRAM to Flash
Flash Address space

FIG. 8B

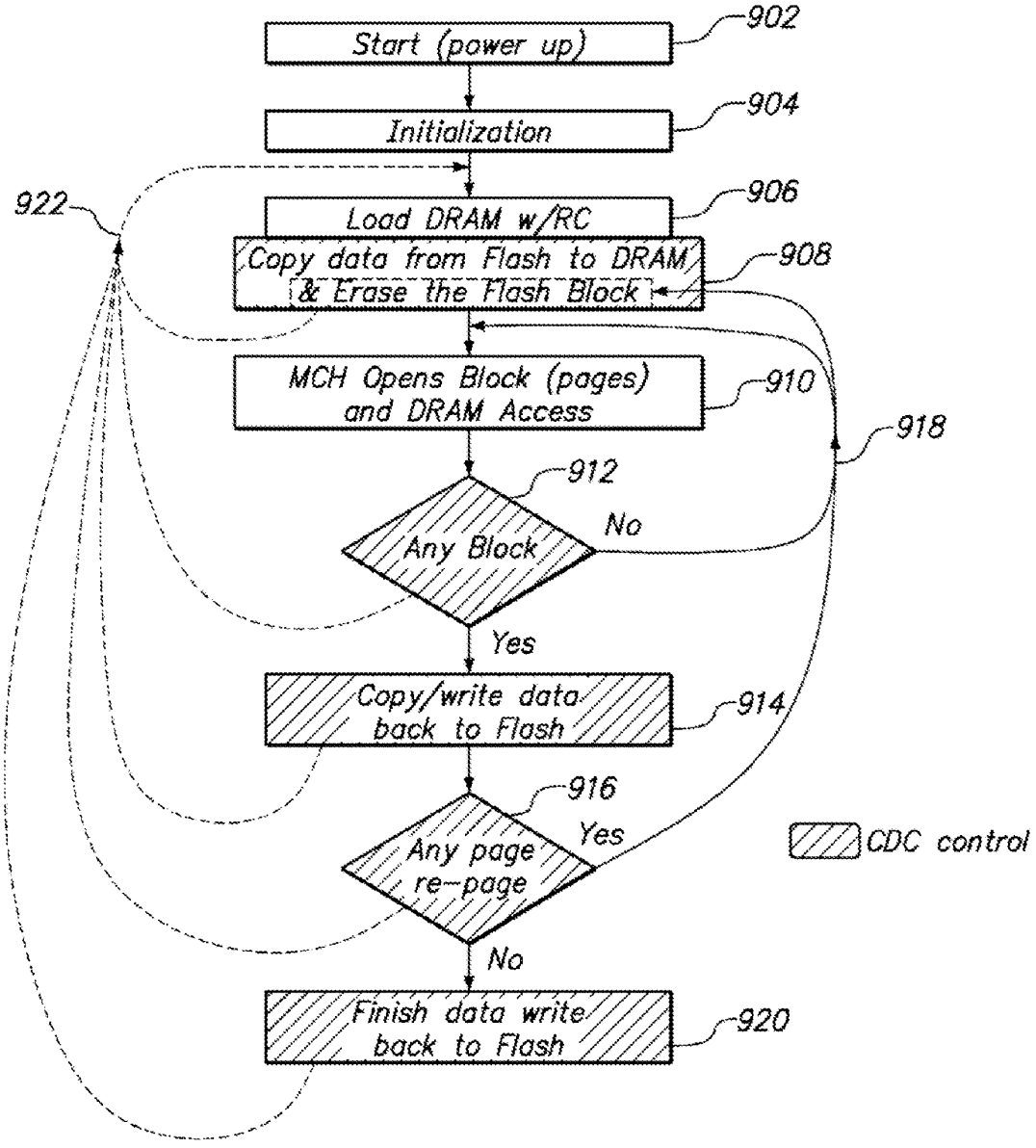

Start (power up)
902
Initialization
904
Load DRAM w/RC
906
Copy data from Flash to DRAM & Erase the Flash Block
908
MCH Opens Block (pages) and DRAM Access
910
912
Any Block
No
Yes
Copy/write data back to Flash
914
916
Any page re-page
Yes
No
Finish data write back to Flash
920
922
918
CDC control

FIG. 9

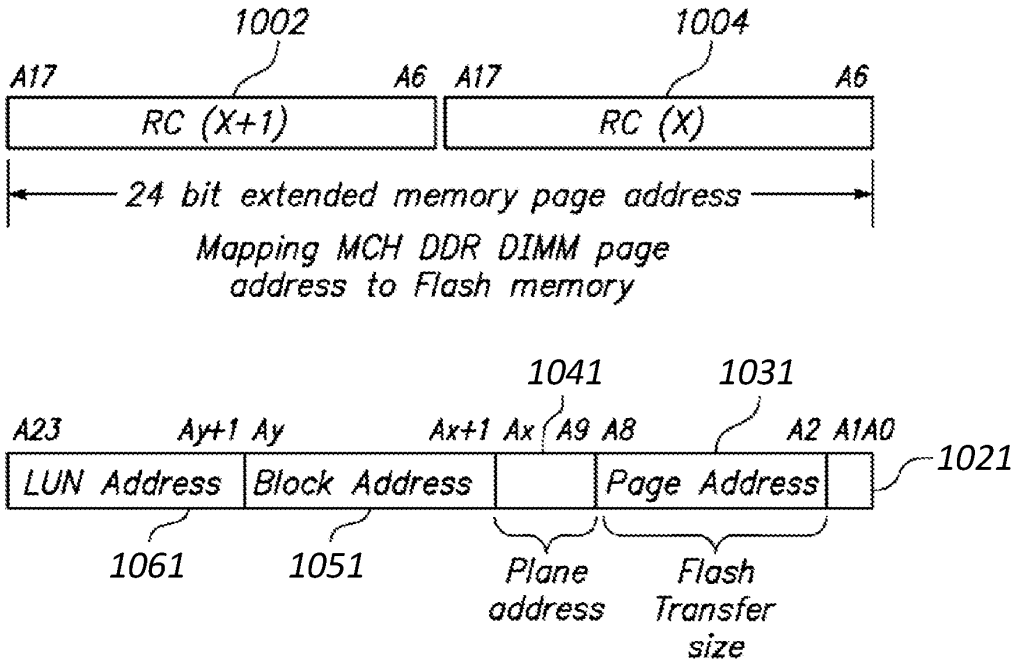

1002
1004
A17
A6
A17
A6
RC (X+1)
RC (X)
24 bit extended memory page address
Mapping MCH DDR DIMM page address to Flash memory
1041
1031
A23
Ay+1
Ay
Ax+1
Ax
A9
A8
A2
A1A0
1021
LUN Address
Block Address
Page Address
1061
1051
Plane address
Flash Transfer size

FIG. 10

DRAM density (GB)	# of blocks per bank	Flash wr-time to rd-time ratio	Avg block use time (sec)	Flash write time (sec)	Max allowed Closed Blk in queue to be written back to Flash
1	250	55	1.00E-03	2.00E-02	0
1	250	55	1.00E-02	2.00E-02	2
1	250	55	2.00E-02	2.00E-02	5
1	250	55	5.00E-02	2.00E-02	11
2	500	55	1.00E-03	2.00E-02	0
2	500	55	1.00E-02	2.00E-02	5
2	500	55	2.00E-02	2.00E-02	9
2	500	55	5.00E-02	2.00E-02	23
4	1000	55	1.00E-03	2.00E-02	1
4	1000	55	1.00E-02	2.00E-02	9
4	1000	55	2.00E-02	2.00E-02	18
4	1000	55	5.00E-02	2.00E-02	45

FIG. 11

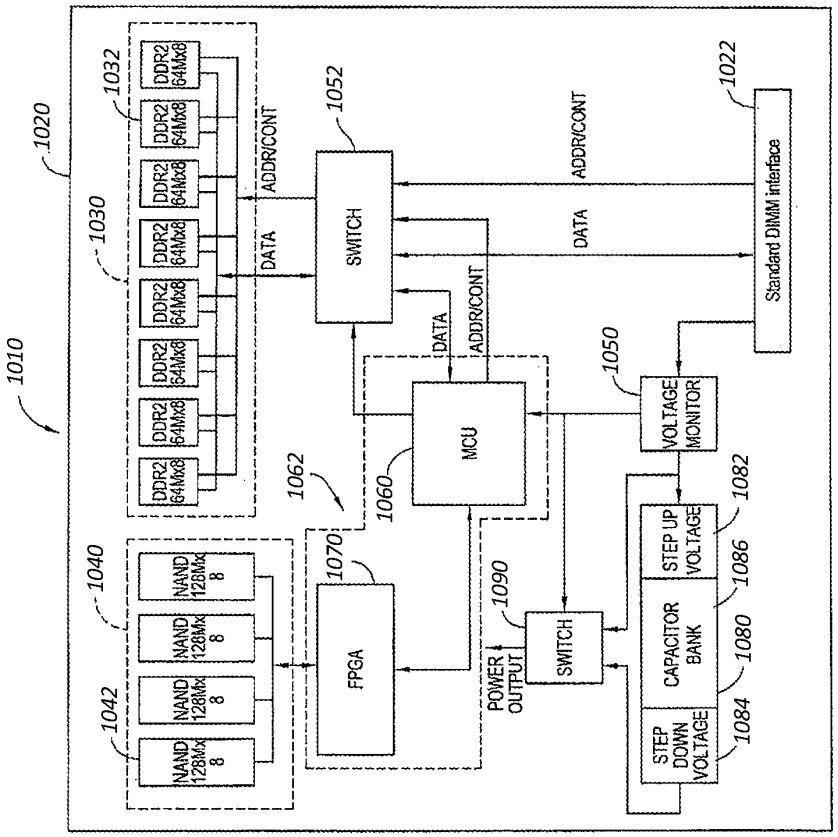

1010
1020
1030
1032
DDR2 64Mx8
ADDR/CONT
DATA
1040
1042
NAND 128Mx 8
1052
SWITCH
1022
Standard DIMM interface
1050
VOLTAGE MONITOR
1060
MCU
1062
1070
FPGA
1090
SWITCH
POWER OUTPUT
1080
CAPACITOR BANK
1082
STEP UP VOLTAGE
1084
STEP DOWN VOLTAGE
1086

FIG. 12

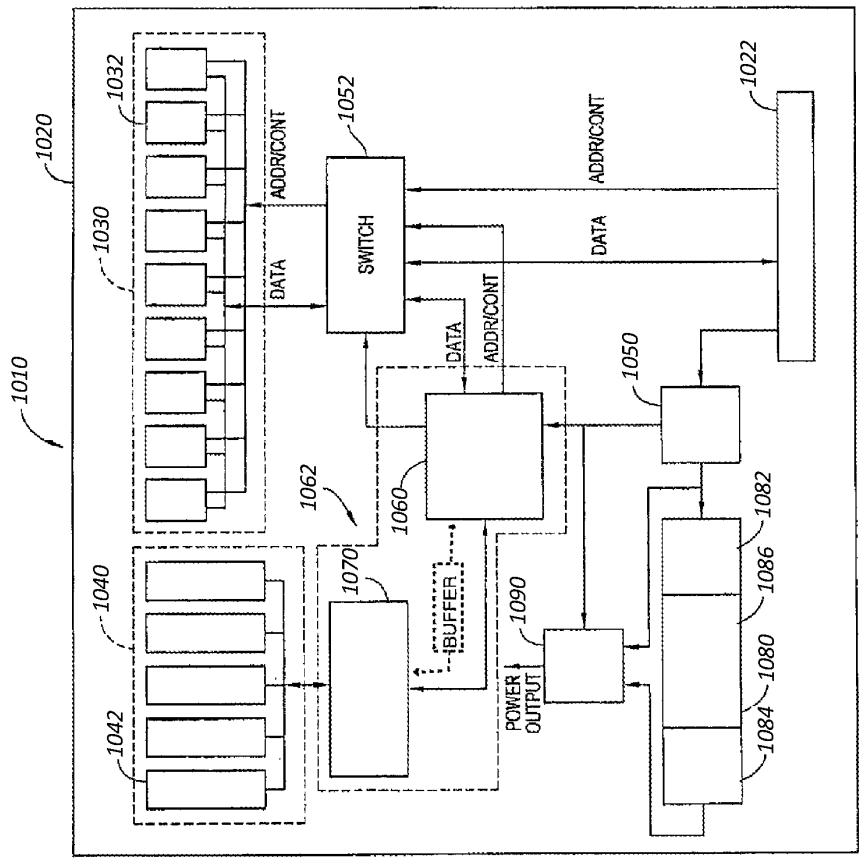

1010
1020
1030
1032
1040
1042
1050
1052
1060
1062
1070
1080
1082
1084
1086
1090
1022
ADDR/CONT
DATA
SWITCH
BUFFER
POWER OUTPUT

FIG. 13

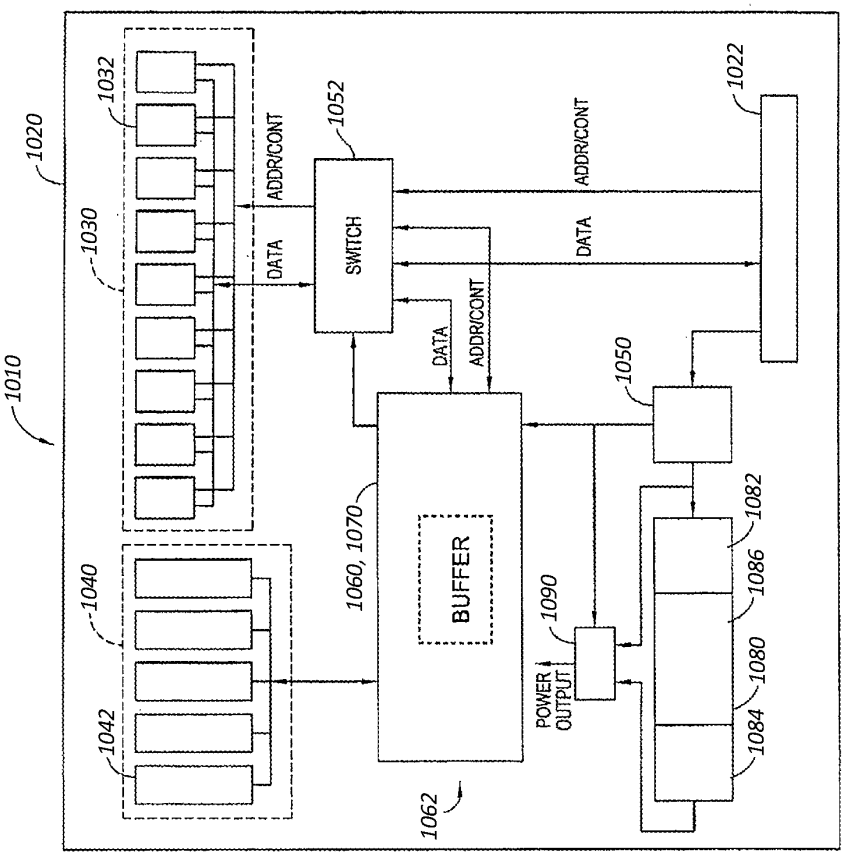

1010
1020
1030
1032
1040
1042
1050
1052
1060, 1070
1062
1080
1082
1084
1086
1090
1022
ADDR/CONT
DATA
SWITCH
BUFFER
POWER OUTPUT

FIG. 14

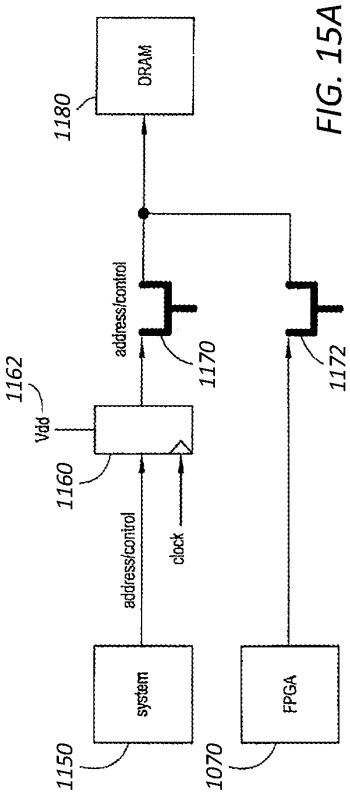


FIG. 15A

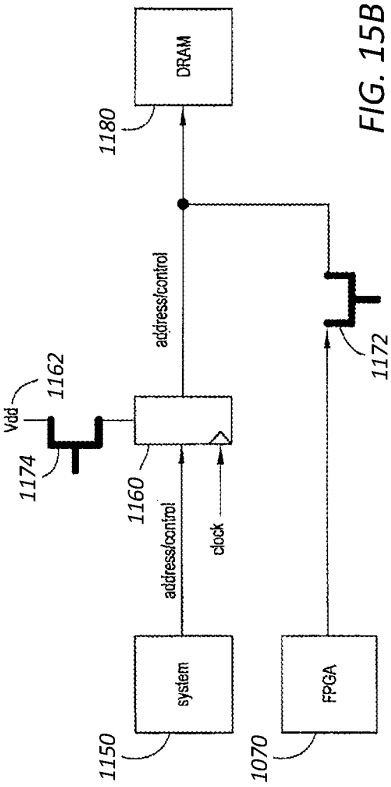


FIG. 15B

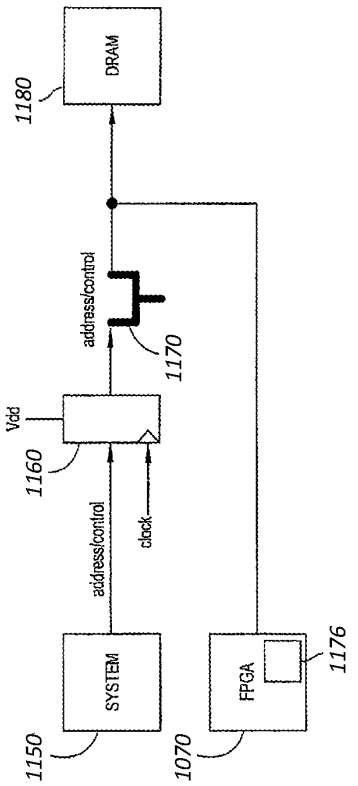

DRAM
1180
address/control
1170
Vdd
1160
address/control
clock
SYSTEM
1150
FPGA
1176
1070

FIG. 15C

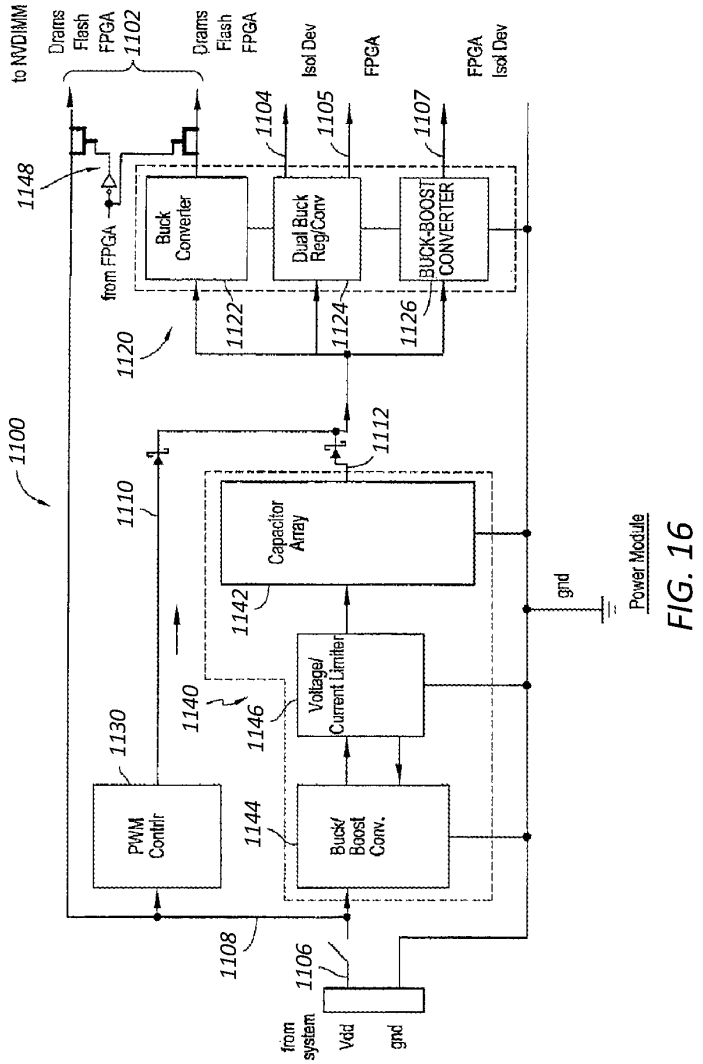

to NVDIMM
Drams
Flash
FPGA
1102
Drams
Flash
FPGA
Isol Dev
FPGA
FPGA
Isol Dev
1104
1105
1107
1148
from FPGA
Buck Converter
Dual Buck Reg/Conv
BUCK-BOOST CONVERTER
1122
1124
1126
1120
1100
1112
1110
Capacitor Array
1142
gnd
Power Module
1140
1146
Voltage/ Current Limiter
1130
PWM Contrlr
1144
Buck/ Boost Conv.
1108
1106
from system
Vdd
gnd

FIG. 16

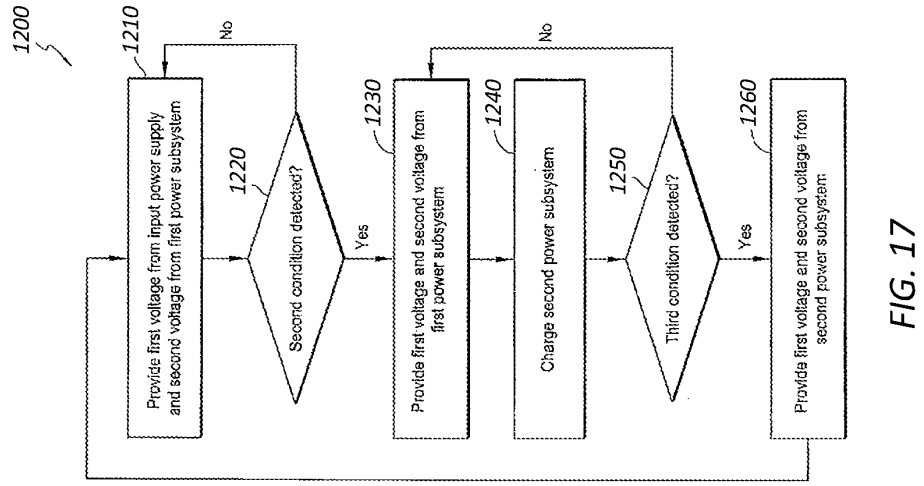

1200
1210
Provide first voltage from input power supply and second voltage from first power subsystem
1220
Second condition detected?
No
Yes
1230
Provide first voltage and second voltage from first power subsystem
1240
Charge second power subsystem
1250
Third condition detected?
No
Yes
1260
Provide first voltage and second voltage from second power subsystem

FIG. 17

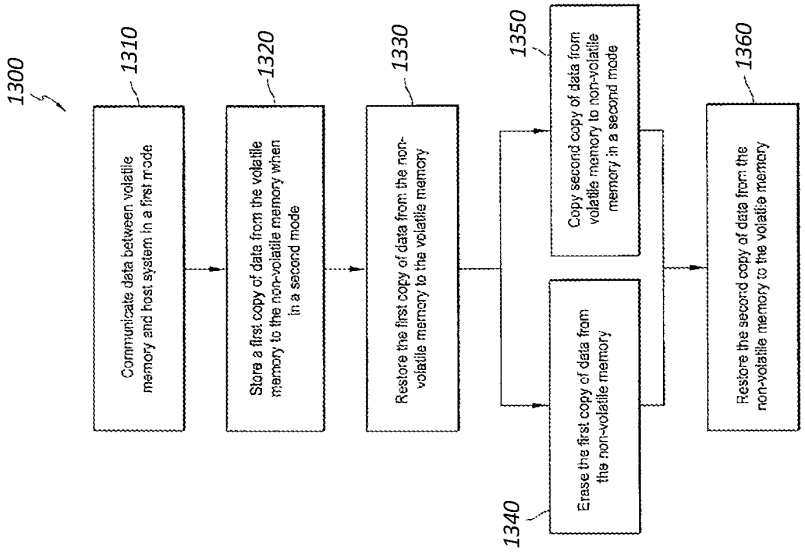

1300
1310
Communicate data between volatile memory and host system in a first mode
1320
Store a first copy of data from the volatile memory to the non-volatile memory when in a second mode
1330
Restore the first copy of data from the non-volatile memory to the volatile memory
1340
Erase the first copy of data from the non-volatile memory
1350
Copy second copy of data from volatile memory to non-volatile memory in a second mode
1360
Restore the second copy of data from the non-volatile memory to the volatile memory

FIG. 18

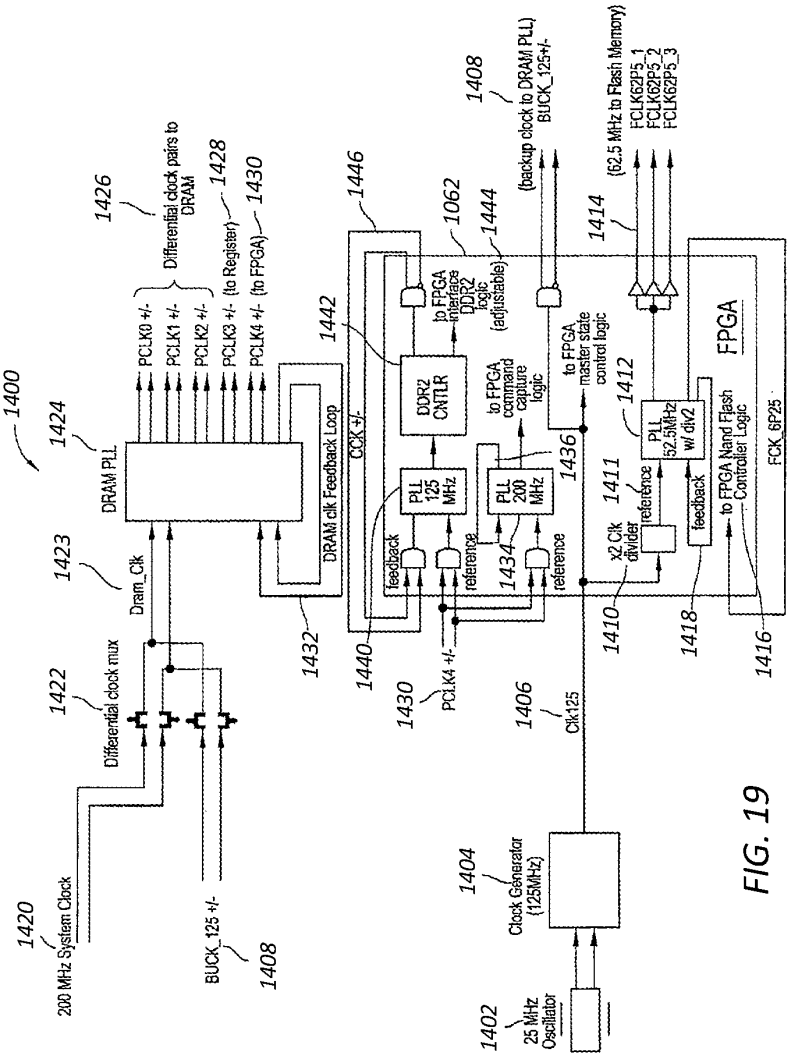

1400
1424
DRAM PLL
1423
Dram_Clk
1422
Differential clock mux
1420
200 MHz System Clock
1408
BUCK_125 +/-
1426
Differential clock pairs to DRAM
1428
(to Register)
1430
(to FPGA)
PCLK0 +/-
PCLK1 +/-
PCLK2 +/-
PCLK3 +/-
PCLK4 +/-
1442
DRAM clk Feedback Loop
1432
1446
1062
1444
1440
CCK +/-
DDR2 CNTLR
PLL 125 MHz
PLL 200 MHz
feedback
reference
reference
reference
1434
1430
PCLK4 +/-
to FPGA interface DDR2 logic (adjustable)
to FPGA command capture logic
to FPGA master state control logic
1436
1406
Clk125
1404
Clock Generator (125MHz)
1402
25 MHz Oscillator
1408
(backup clock to DRAM PLL)
BUCK_125+/-
1414
(62.5 MHz to Flash Memory)
FCLK62P5_1
FCLK62P5_2
FCLK62P5_3
1412
PLL 62.5MHz w/ div2
1411
x2 Clk divider
reference
feedback
1410
1418
1416
FPGA
to FPGA Nand Flash Controller Logic
FCK_6P25

FIG. 19

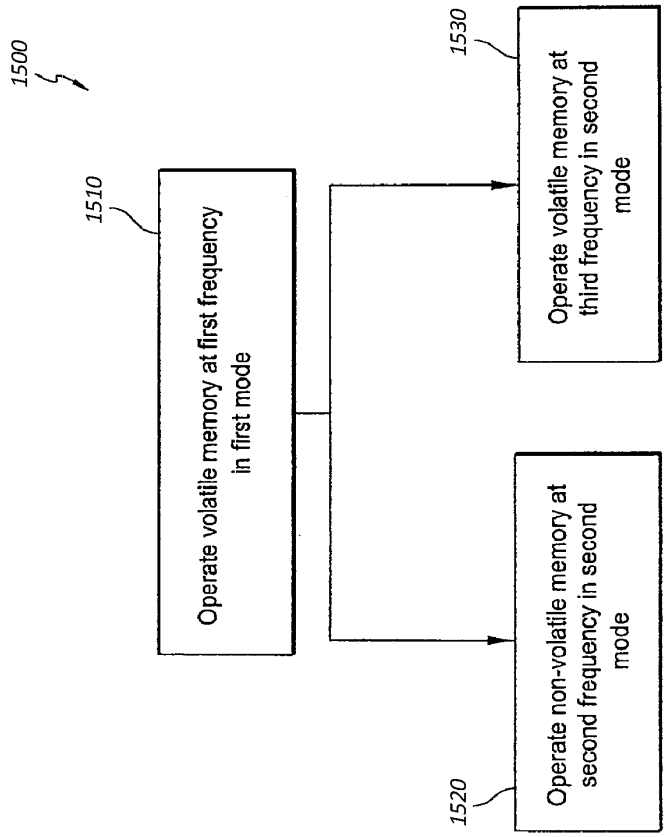

1500
1510
Operate volatile memory at first frequency in first mode
1530
Operate volatile memory at third frequency in second mode
1520
Operate non-volatile memory at second frequency in second mode

FIG. 20

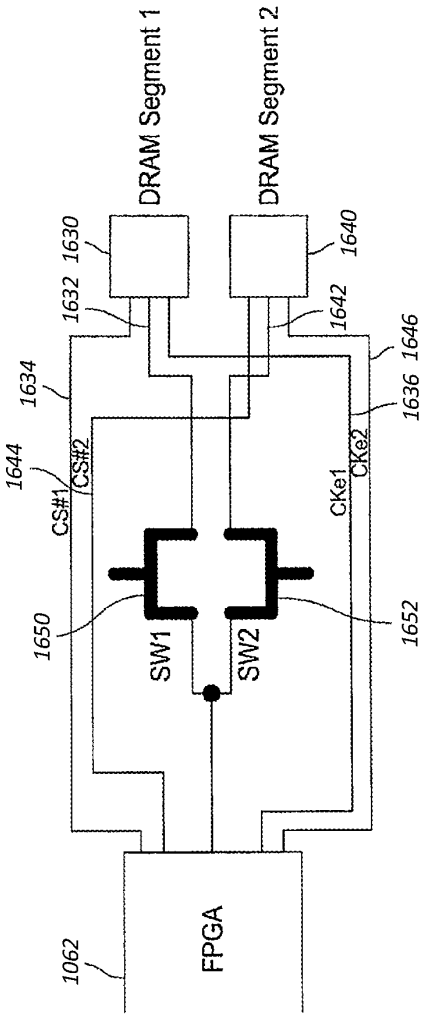

DRAM Segment 1
DRAM Segment 2
1630
1640
1632
1642
1646
1634
1636
1644
CS#2
CS#1
CKe2
CKe1
1650
SW1
SW2
1652
FPGA
1062

FIG. 21

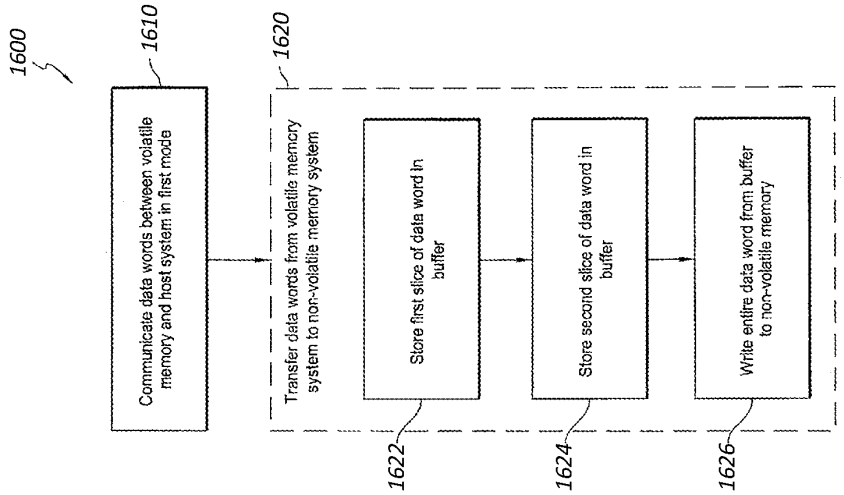

1600
1610
1620
Communicate data words between volatile memory and host system in first mode
Transfer data words from volatile memory system to non-volatile memory system
Store first slice of data word in buffer
Store second slice of data word in buffer
Write entire data word from buffer to non-volatile memory
1622
1624
1626

FIG. 22

FLASH-DRAM HYBRID MEMORY MODULE

PRIORITY CLAIM

This application is a continuation of U.S. patent application Ser. No. 15/934,416, filed Mar. 23, 2018, titled "Flash-Dram Hybrid Memory Module," which is a continuation of U.S. patent application Ser. No. 14/840,865, filed Aug. 31, 2015, titled "Flash-Dram Hybrid Memory Module," now U.S. Pat. No. 9,928,186, which is a continuation of U.S. patent application Ser. No. 14/489,269, filed Sep. 17, 2014, titled "Flash-Dram Hybrid Memory Module," now U.S. Pat. No. 9,158,684, which is a continuation of U.S. patent application Ser. No. 13/559,476, filed Jul. 26, 2012, titled "Flash-Dram Hybrid Memory Module," now U.S. Pat. No. 8,874,831, which claims the benefit of U.S. Provisional Patent Application No. 61/512,871, filed Jul. 28, 2011, and is a continuation-in-part of U.S. patent application Ser. No. 12/240,916, filed Sep. 29, 2008, titled "Non-Volatile Memory Module," now U.S. Pat. No. 8,301,833, which is a continuation of U.S. patent application Ser. No. 12/131,873, filed Jun. 2, 2008, which claims the benefit of U.S. Provisional Patent Application No. 60/941,586, filed Jun. 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

This application may be considered related to U.S. patent application Ser. No. 14/173,242, titled "Isolation Switching For Backup Of Registered Memory," filed Feb. 5, 2014, which is a continuation of U.S. patent application Ser. No. 13/905,053, titled "Isolation Switching For Backup Of Registered Memory," filed May 29, 2013, now U.S. Pat. No. 8,677,060, issued Mar. 18, 2014, which is a continuation of U.S. patent application Ser. No. 13/536,173, titled "Data Transfer Scheme For Non-Volatile Memory Module," filed Jun. 28, 2012, now U.S. Pat. No. 8,516,187, issued Aug. 20, 2013, which is a divisional of U.S. patent application Ser. No. 12/240,916, titled "Non-Volatile Memory Module," filed Sep. 29, 2008, now U.S. Pat. No. 8,301,833, issued Oct. 30, 2012, which is a continuation of U.S. patent application Ser. No. 12/131,873, filed Jun. 2, 2008, now abandoned, which claims the benefit of U.S. Provisional Application No. 60/941,586, filed Jun. 1, 2007, the contents of which are incorporated by reference herein in their entirety.

This application may also be considered related to U.S. patent application Ser. No. 15/000,834, filed Jan. 19, 2016, which is a continuation of U.S. patent application Ser. No. 14/489,332, filed Sep. 17, 2014, now U.S. Pat. No. 9,269,437, which is a continuation of U.S. patent application Ser. No. 14/173,219, filed Feb. 5, 2014, now U.S. Pat. No. 8,904,099, which is a continuation of U.S. patent application Ser. No. 13/905,048, filed May 29, 2013, now U.S. Pat. No. 6,671,243, which is a continuation U.S. patent application Ser. No. 13/536,173 above.

This application may also be considered related to U.S. patent application Ser. No. 15/924,866, which is a continuation of U.S. patent application Ser. No. 14/489,281, filed Sep. 17, 2014, now U.S. Pat. No. 9,921,762, which is a continuation of U.S. patent application Ser. No. 13/625,563, filed Sep. 24, 2012, now U.S. Pat. No. 8,904,098, which claims the benefit of U.S. Provisional Application No. 61/583,775, filed Sep. 23, 2011.

TECHNICAL FIELD

The present disclosure relates generally to computer memory devices, and more particularly, to devices that employ different types of memory devices such as combinations of Flash and random access memories.

BACKGROUND

As technology advances and the usage of portable computing devices, such as tablet notebook computers, increases, more data needs to be transferred among data centers and to/from end users. In many cases, data centers are built by clustering multiple servers that are networked to increase performance.

Although there are many types of networked servers that are specific to the types applications envisioned, the basic concept is generally to increase server performance by dynamically allocating computing and storage resources. In recent years, server technology has evolved to be specific to particular applications such as 'finance transactions' (for example, point-of-service, inter-bank transaction, stock market transaction), 'scientific computation' (for example, fluid dynamic for automobile and ship design, weather prediction, oil and gas expeditions), 'medical diagnostics' (for example, diagnostics based on the fuzzy logic, medical data processing), 'simple information sharing and searching' (for example, web search, retail store website, company home page), 'email' (information distribution and archive), 'security service', 'entertainment' (for example, video-on-demand), and so on. However, all of these applications suffer from the same information transfer bottleneck due to the inability of a high speed CPU (central processing unit) to efficiently transfer data in and out of relatively slower speed storage or memory subsystems, particularly since data transfers typically pass through the CPU input/output (I/O) channels.

The data transfer limitations by the CPU are exemplified by the arrangement shown in FIG. **1**, and apply to data transfers between main storage (for example the hard disk (HD) or solid state drive (SSD) and the memory subsystems (for example DRAM DIMM (Dynamic Random Access Memory Dual In-line Memory Module) connected to the front side bus (FSB)). In arrangements such as that of FIG. **1**, the SSD/HD and DRAM DIMM of a conventional memory arrangement are connected to the CPU via separate memory control ports (not shown). FIG. **1** specifically shows, through the double-headed arrow, the data flow path between the computer or server main storage (SSD/HD) to the DRAM DIMMs. Since the SSD/HD data I/O and the DRAM DIMM data I/O are controlled by the CPU, the CPU needs to allocate its process cycles to control these I/Os, which may include the IRQ (Interrupt Request) service which the CPU performs periodically. As will be appreciated, the more time a CPU allocates to controlling the data transfer traffic, the less time the CPU has to perform other tasks. Therefore, the overall performance of a server will deteriorate with the increased amount of time the CPU has to expend in performing data transfer.

There have been various approaches to increase the data transfer throughput rates from/to the main storage, such as SSD/HD, to local storage, such as DRAM DIMM. In one example as illustrated in FIG. **2**, EcoRAM™ developed by Spansion provides a storage SSD based system that assumes a physical form factor of a DIMM. The EcoRAM™ is populated with Flash memories and a relatively small memory capacity using DRAMs which serve as a data buffer. This arrangement is capable of delivering higher throughput rate than a standard SSD based system since the EcoRAM™ is connected to the CPU (central processing unit) via a high speed interface, such as the HT (Hyper

Transport) interface, while an SSD/HD is typically connected via SATA (serial AT attachment), USB (universal serial bus), or PCI Express (peripheral component interface express). For example, the read random access throughput rate of EcoRAM™ is near 3 GB/s compared with 400 MB/s for a NAND SSD memory subsystem using the standard PCI Express-based. This is a 7.5× performance improvement. However, the performance improvement for write random access throughput rate is less than 2×(197 MBs for the EcoRAM vs. 104 MBs for NAND SSD). This is mainly due to the fact that the write speed is cannot be faster than the NAND Flash write access time. FIG. **2** is an example of EcoRAM™ using SSD with the form factor of a standard DIMM such that it can be connected to the FSB (front side bus). However, due to the interface protocol difference between DRAM and Flash, an interface device, EcoRAM Accelerator™), which occupies one of the server's CPU sockets is used, and hence further reducing server's performance by reducing the number of available CPU sockets available, and in turn reducing the overall computation efficiency. The server's performance will further suffer due to the limited utilization of the CPU bus due to the large difference in the data transfer throughput rate between read and write operations.

The EcoRAM™ architecture enables the CPU to view the Flash DIMM controller chip as another processor with a large size of memory available for CPU access.

In general, the access speed of a Flash based system is limited by four items: the read/write speed of the Flash memory, the CPU's FSB bus speed and efficiency, the Flash DIMM controller's inherent latency, and the HT interconnect speed and efficiency which is dependent on the HT interface controller in the CPU and Flash DIMM controller chip.

The published results indicate that these shortcomings are evident in that the maximum throughput rate is 1.56 GBs for the read operation and 104 MBs for the write operation. These access rates are 25% of the DRAM read access speed, and 1.7% of the DRAM access speed at 400 MHz operation. The disparity in the access speed (15 to 1) between the read operation and write operation highlight a major disadvantage of this architecture. The discrepancy of the access speed between this type of architecture and JEDEC standard DRAM DIMM is expected to grow wider as the DRAM memory technology advances much faster than the Flash memory.

Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the computer system to provide volatile memory to the computer system.

Volatile memory generally maintains stored information only when it is powered. Batteries have been used to provide power to volatile memory during power failures or interruptions. However, batteries may require maintenance, may need to be replaced, are not environmentally friendly, and the status of batteries can be difficult to monitor.

Non-volatile memory can generally maintain stored information while power is not applied to the non-volatile memory. In certain circumstances, it can therefore be useful to backup volatile memory using non-volatile memory.

OVERVIEW

Described herein is a memory module couplable to a memory controller of a host system. The memory module includes a non-volatile memory subsystem, a data manager coupled to the non-volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager, and a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller.

Also described herein is a method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems. The method includes receiving control information from the memory controller, wherein the control information is received using a protocol of the volatile memory subsystem. The method further includes identifying a data path to be used for transferring data to or from the memory module using the received control information, and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path.

Also described herein is a memory module wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller.

Also described herein is a memory module wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller.

Also described herein is a memory module wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer.

Also described herein is a memory module wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module.

Also described herein is a memory module wherein the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

Also described herein is a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

Also described herein is a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

Also described herein is a memory module wherein the volatile memory subsystem comprises DRAM memory.

Also described herein is a memory module wherein the non-volatile memory subsystem comprises flash memory.

Also described herein is a memory module wherein at least one set of data ports is operated by the data manager to

independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

Also described herein is a memory module wherein the data manager and controller are configured to effect data transfer between the memory controller and the non-volatile memory subsystem in response to memory access commands received by the controller from the memory controller.

Also described herein is a memory module wherein the volatile memory subsystem is operable as a buffer for the data transfer between the memory controller and non-volatile memory.

Also described herein is a memory module wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

Also described herein is a memory module wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem.

Also described herein is a memory module wherein the controller is operable to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

Also described herein is a memory module wherein the controller is configured to effect operation with the host system in accordance with a prescribed protocol.

Also described herein is a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

Also described herein is a memory module wherein the controller is operable to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

Also described herein is a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

Also described herein is a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

Also described herein is a memory module wherein the controller is operable to copy booting information from the non-volatile to the volatile memory subsystem during power up.

Also described herein is a memory module wherein the controller includes a volatile memory control module, a non-volatile memory control module, data manager control module, a command interpreter module, and a scheduler module.

Also described herein is a memory module wherein commands from the volatile memory control module to the volatile memory subsystem are subordinated to commands from the memory controller to the controller.

Also described herein is a memory module wherein the controller effects pre-fetching of data from the non-volatile to the volatile memory.

Also described herein is a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

Also described herein is a memory module wherein the controller is operable to initiate a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

Also described herein is a memory module wherein, if the closed block is re-opened, the controller is operable to abort the copy operation and to erase the target block from the non-volatile memory subsystem.

Also described herein is a method for managing a memory module wherein the transfer of data includes a bidirectional transfer of data between the non-volatile and the volatile memory subsystems.

Also described herein is a method for managing a memory module further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data.

Also described herein is a method for managing a memory module further comprising operating the data manager to control data traffic between the memory controller and at least one of the volatile and non-volatile memory subsystems.

Also described herein is a method for managing a memory module wherein data traffic control relates to any one or more of data transfer size, formatting information, direction of data flow, and the starting time of the transfer of data.

Also described herein is a method for managing a memory module wherein data traffic control by the data manager is based on instructions received from the controller.

Also described herein is a method for managing a memory module further comprising operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

Also described herein is a method for managing a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

Also described herein is a method for managing a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

Also described herein is a method for managing a memory module wherein the volatile memory subsystem comprises DRAM memory.

Also described herein is a method for managing a memory module wherein the non-volatile memory subsystem comprises Flash memory.

Also described herein is a method for managing a memory module further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

Also described herein is a method for managing a memory module further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller.

Also described herein is a method for managing a memory module further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem.

Also described herein is a method for managing a memory module further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

Also described herein is a method for managing a memory module further comprising using the controller to effect communication with a host system by the volatile memory subsystem in accordance with a prescribed protocol.

Also described herein is a method for managing a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

Also described herein is a method for managing a memory module further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

Also described herein is a method for managing a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

Also described herein is a method for managing a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

Also described herein is a method for managing a memory module further comprising using the controller to copy booting information from the non-volatile to the volatile memory subsystem during power up.

Also described herein is a method for managing a memory module wherein the controller includes a volatile memory control module, the method further comprising generating commands by the volatile memory control module in response to commands from the memory controller, and transmitting the generated commands to the volatile memory subsystem.

Also described herein is a method for managing a memory module further comprising pre-fetching of data from the non-volatile memory subsystem to the volatile memory subsystem.

Also described herein is a method for managing a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

Also described herein is a method for managing a memory module further comprising initiating a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

Also described herein is a method for managing a memory module further comprising aborting the copy operation when the closed block of the volatile memory subsystem is re-opened, and erasing the target block in the non-volatile memory subsystem.

Also described herein is a memory system having a volatile memory subsystem, a non-volatile memory subsystem, a controller coupled to the non-volatile memory subsystem, and a circuit coupled to the volatile memory subsystem, to the controller, and to a host system. In a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system. In a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem to allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, and the circuit is operable to selectively isolate the volatile memory subsystem from the host system.

Also described herein is a method for operating a memory system. The method includes coupling a circuit to a host system, a volatile memory subsystem, and a controller, wherein the controller is coupled to a non-volatile memory subsystem. In a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, the circuit is used to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, the circuit is used to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

Also described herein is a nontransitory computer readable storage medium storing one or more programs configured to be executed by one or more computing devices. The programs, when executing on the one or more computing devices, cause a circuit that is coupled to a host system, to a volatile memory subsystem, and to a controller that is coupled to a nonvolatile memory subsystem, to perform a method in which, in a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, operating the circuit to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, operating the circuit to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more examples of embodiments and, together with the description of example embodiments, serve to explain the principles and implementations of the embodiments.

In the drawings:

FIG. **1** is a block diagram illustrating the path of data transfer, via a CPU, of a conventional memory arrangement;

FIG. **2** is a block diagram of a known EcoRAM™ architecture;

FIGS. **3**A and **3**B are block diagrams of a non-volatile memory DIMM or NVDIMM;

FIGS. **4**A and **4**B are block diagrams of a Flash-DRAM hybrid DIMM or FDHDIMM;

FIG. **5**A is a block diagram of a memory module **500** in accordance with certain embodiments described herein;

FIG. **5**B is a block diagram showing some functionality of a memory module such as that shown in FIG. **5**A;

FIG. **6** is a block diagram showing some details of the data manager (DMgr);

FIG. **7** is a functional block diagram of the on-module controller (CDC);

FIG. **8**A is a block diagram showing more details of the prior art Flash-DRAM hybrid DIMM (FDHDIMM) of FIGS. **4**A and **4**B;

FIG. **8**B is a block diagram of a Flash-DRAM hybrid DIMM (FDHDIMM) in accordance with certain embodiments disclosed herein;

FIG. **9** is a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM;

FIG. **10** is a block diagram showing an example of mapping of DRAM address space to Flash memory address space; and

FIG. **11** is a table showing estimates of the maximum allowed closed blocks in a queue to be written back to Flash memory for different DRAM densities using various average block use time.

FIG. **12** is a block diagram of an example memory system compatible with certain embodiments described herein.

FIG. **13** is a block diagram of an example memory module with ECC (error-correcting code) having a volatile memory subsystem with nine volatile memory elements and a non-volatile memory subsystem with five non-volatile memory elements in accordance with certain embodiments described herein.

FIG. **14** is a block diagram of an example memory module having a microcontroller unit and logic element integrated into a single device in accordance with certain embodiments described herein.

FIGS. **15**A-**15**C schematically illustrate example embodiments of memory systems having volatile memory subsystems comprising registered dual in-line memory modules in accordance with certain embodiments described herein.

FIG. **16** schematically illustrates an example power module of a memory system in accordance with certain embodiments described herein.

FIG. **17** is a flowchart of an example method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems.

FIG. **18** is a flowchart of an example method of controlling a memory system operatively coupled to a host system and which includes at least 100 percent more storage capacity in non-volatile memory than in volatile memory.

FIG. **19** schematically illustrates an example clock distribution topology of a memory system in accordance with certain embodiments described herein.

FIG. **20** is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including operating a volatile memory subsystem at a reduced rate in a back-up mode.

FIG. **21** schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments of a volatile memory subsystem of a memory system to a controller of the memory system.

FIG. **22** is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including backing up and/or restoring a volatile memory subsystem in slices.

DESCRIPTION OF EXAMPLE EMBODIMENTS

Example embodiments are described herein in the context of a system of computers, servers, controllers, memory modules, hard disk drives and software. Those of ordinary skill in the art will realize that the following description is illustrative only and is not intended to be in any way limiting. Other embodiments will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to implementations of the example embodiments as illustrated in the accompanying drawings. The same reference indicators will be used to the extent possible throughout the drawings and the following description to refer to the same or like items.

In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

In accordance with this disclosure, the components, process steps, and/or data structures described herein may be implemented using various types of operating systems, computing platforms, computer programs, and/or general purpose machines. In addition, those of ordinary skill in the art will recognize that devices of a less general purpose nature, such as hardwired devices, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), or the like, may also be used without departing from the scope and spirit of the inventive concepts disclosed herein. Where a method comprising a series of process steps is implemented by a computer or a machine and those process steps can be stored as a series of instructions readable by the machine, they may be stored on a tangible medium such as a computer memory device (e.g., ROM (Read Only Memory), PROM (Programmable Read Only Memory), EEPROM (Electrically Eraseable Programmable Read Only Memory), Flash memory, Jump Drive, and the like), magnetic storage medium (e.g., tape, magnetic disk drive, and the like), optical storage medium (e.g., CD-ROM, DVD-ROM, paper card, paper tape and the like) and other types of program memory.

The term "exemplary" where used herein is intended to mean "serving as an example, instance or illustration." Any embodiment described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments.

Disclosed herein are arrangements for improving memory access rates and addressing the high disparity (15 to 1 ratio) between the read and write data throughput rates. In one arrangement, a Flash-DRAM-hybrid DIMM (FDHDIMM) with integrated Flash and DRAM is used. Methods for controlling such an arrangement are described.

In certain embodiments, the actual memory density (size or capacity) of the DIMM and/or the ratio of DRAM memory to Flash memory are configurable for optimal use with a particular application (for example, POS, inter-bank transaction, stock market transaction, scientific computation such as fluid dynamics for automobile and ship design, weather prediction, oil and gas expeditions, medical diagnostics such as diagnostics based on the fuzzy logic, medical data processing, simple information sharing and searching such as web search, retail store website, company home

page, email or information distribution and archive, security service, and entertainment such as video-on-demand).

In certain embodiments, the device contains a high density Flash memory with a low density DRAM, wherein the DRAM is used as a data buffer for read/write operation. The Flash serves as the main memory. Certain embodiments described herein overcome the needs of having a long separation period between an Activate command (may be referred to as RAS) and a corresponding read or write command (may be referred to as first CAS command).

In accordance with one embodiment, described with reference to FIGS. **3**A and **3**B, a memory system **300** includes a non-volatile (for example Flash) memory subsystem **302** and a volatile (for example DRAM) memory subsystem **304**. The examples of FIGS. **3**A and **3**B are directed to architectures of a non-volatile DIMM (NVDIMM) NVDIMM system that may use a power subsystem (not shown) that can include a battery or a capacitor as a means for energy storage to copy DRAM memory data into Flash memory when power loss occurs, is detected, or is anticipated to occur during operation. When normal power is restored, a restore NVDIMM operation is initiated and the data stored in the Flash memory is properly restored to the DRAM memory. In this architecture, the density of the Flash is about the same as the DRAM memory size or within a few multiples, although in some applications it may be higher. This type of architecture may also be used to provide non-volatile storage that is connected to the FSB (front side bus) to support RAID (Redundant Array of Independent Disks) based systems or other type of operations. An NVDIMM controller **306** receives and interprets commands from the system memory controller hub (MCH). The NVDIMM controller **306** control the NVDIMM DRAM and Flash memory operations. In FIG. **3**A, the DRAM **304** communicates data with the MCH, while an internal bus **308** is used for data transfer between the DRAM and Flash memory subsystems. In FIG. **3**B, the NVDIMM controller **306'** of NVDIMM **300'** monitors events or commands and enables data transfer to occur in a first mode between the DRAM **304'** and Flash **302'** or in a second mode between the DRAM and the MCH.

In accordance with one embodiment, a general architecture for a Flash and DRAM hybrid DIMM (FDHDIMM) system **400** is shown in FIG. **4**A. The FDHDIMM interfaces with an MCH (memory controller hub) to operate and behave as a high density DIMM, wherein the MCH interfaces with the non-volatile memory subsystem (for example Flash) **402** is controlled by an FDHDIMM controller **404**. Although the MCH interfaces with the Flash via the FDHDIMM controller, the FDHDIMM overall performance is governed by the Flash access time. The volatile memory subsystem (for example DRAM) **406** is primarily used as a data buffer or a temporary storage location such that data from the Flash memory **402** is transferred to the DRAM **406** at the Flash access speed, and buffered or collected into the DRAM **406**, which then transfers the buffered data to the MCH based on the access time of DRAM. Similarly, when the MCH transfers data to the DRAM **406**, the FDHDIMM controller **404** manages the data transfer from the DRAM **406** to the Flash **402**. Since the Flash memory access speed (both read and write) is relatively slower than DRAM, (e.g. for example a few hundred microseconds for read access), the average data throughput rate of FDHDIMM **400** is limited by the Flash access speed. The DRAM **406** serves as a data buffer stage that buffers the MCH read or write data. Thus, the DRAM **406** serves as a temporary storage for the data to be transferred from/to the Flash **402**. Furthermore, in accordance with one embodiment, the MCH recognizes the physical density of an FDHDIMM operating as a high density DIMM as the density of Flash alone.

In accordance with one embodiment, a read operation can be performed by the MCH by sending an activate command (may be simply referred to as RAS, or row address strobe) to the FDHDIMM **400** to conduct a pre-fetch read data operation from the Flash **402** to the DRAM **406**, with the pre-fetch data size being for example a page (1 KB or 2 KB, or may be programmable to any size). The MCH then sends a read command (may be simply referred to as CAS, or column address strobe) to read the data out input of the DRAM. In this embodiment, the data transfer from Flash to DRAM occurs at Flash access speed rates, while data transfer from DRAM to MCH occurs at DRAM access speed rates. In this example, data latency and throughput rates are the same as any DRAM operation as long as the read operations are executed onto the pages that were opened with the activate command previously sent to pre-fetch data from the Flash to DRAM. Thus, a longer separation time period between the RAS (e.g. Activate command) and the first CAS (column address strobe e.g. read or write command) is required to account for the time it takes to pre-fetch data from the Flash to DRAM.

An example of FDHDIMM operating as a DDR DIMM with SSD is shown in FIG. **4**B, wherein the FDHDIMM **400'** supports two different interface interpretations to the MCH. In the first interface interpretation, the MCH views the FDHDIMM **400'** as a combination of DRAM DIMM and SSD (not illustrated). In this mode the MCH needs to manage two address spaces, one for the DRAMs **402'** and one for the Flash **404'**. The MCH is coupled to, and controls, both of the DRAM and Flash memory subsystems. One advantage of this mode is that the CPU does not need to be in the data path when data is moved from DRAM to Flash or from Flash to DRAM. In the second interface interpretation, the MCH views the FDHDIMM **400'** as an on-DIMM Flash with the SSD in an extended memory space that is behind the DRAM space. Thus, in this mode, the MCH physically fetches data from the SSD to the DDR DRAM and then the DRAM sends the data to the MCH. Since all data movement occurs on the FDHDIMM, this mode will provide better performance than if the data were to be moved through or via the CPU.

In accordance with one embodiment and as shown in FIG. **4**B, the FDHDIMM **400'** receives control signals **408** from the MCH, where the control signals may include one or more control signals specifically for the DRAM **402'** operation and one or more control signals specifically for the Flash **404'** operation. In this embodiment, the MCH or CPU is coupled to the FDHDIMM via a single data bus interface **410** which couples the MCH to the DRAM.

FIGS. **5**A and **5**B are block diagrams of a memory module **500** that is couplable to a host system (not shown). The host system may be a server or any other system comprising a memory system controller or an MCH for providing and controlling the read/write access to one or more memory systems, wherein each memory system may include a plurality of memory subsystems, a plurality of memory devices, or at least one memory module. The term "read/write access" means the ability of the MCH to interface with a memory system or subsystem in order to write data into it or read data from it, depending on the particular requirement at a particular time.

In certain embodiments, memory module **500** is a Flash-DRAM hybrid memory subsystem which may be integrated with other components of a host system. In certain embodiments, memory module **500** is a Flash-DRAM hybrid

memory module that has the DIMM (dual-inline memory module) form factor, and may be referred to as a FDHDIMM, although it is to be understood that in both structure and operation it may be different from the FDHDIMM discussed above and described with reference to FIGS. **4**A and **4**B. Memory module **500** includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) **502** and an on-DIMM data manager (DMgr) **504**. While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well. CDC **502** and data manager DMgr **504** are operative to manage the interface between a non-volatile memory subsystem such as a Flash **506**, a volatile memory subsystem such as a DRAM **508**, and a host system represented by MCH **510**.

In certain embodiments, CDC **502** controls the read/write access to/from Flash memory **506** from/to DRAM memory **508**, and to/from DRAM memory from/to MCH **510**.

Read/write access between DRAM **508**, Flash **506** and MCH **510** may be referred to herein generally as communication, wherein control and address information C/A **560** is sent from MCH **510** to CDC **502**, and possible data transfers follow as indicated by Data **550**, Data **555**, and/or Data **556**. In certain embodiments, the CDC **502** performs specific functions for memory address transformation, such as address translation, mapping, or address domain conversion, Flash access control, data error correction, manipulation of data width or data formatting or data modulation between the Flash memory and DRAM, and so on. In certain embodiments, the CDC **502** ensures that memory module **500** provides transparent operation to the MCH in accordance with certain industry standards, such as DDR, DDR2, DDR3, DDR4 protocols. In the arrangement shown in FIGS. **5**A and **5**B, there is no direct access from the MCH **510** to the Flash **506** memory subsystem. Thus in accordance with certain embodiments, the Flash access speed has minimal impact on the overall FDHDIMM access speed. In the schematic illustration of FIG. **5**B and in accordance with one embodiment, the CDC controller **502** receives standard DDR commands from the MCH, interprets, and produces commands and/or control signals to control the operation of the Data manager (DMgr), the Flash memory and the DRAM memory. The DMgr controls the data path routing amongst DRAMs, Flash and MCH, as detailed below. The data path routing control signals are independently operated without any exclusivity.

An exemplary role of DMgr **504** is described with reference to FIG. **6**. In certain embodiments and in response to communication from CDC **502**, DMgr **504** provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction. For example, these functions or operations can be performed on-the-fly (while data is being transferred via the DMgr **504**) or performed on buffered or stored data in DRAM or a buffer. In addition, one role of DMgr **504** is to provide interoperability among various memory subsystems or components and/or MCH **510**.

In one embodiment, an exemplary host system operation begins with initialization. The CDC **502** receives a first command from the MCH **510** to initialize FDHDIMM **500** using a certain memory space. The memory space as would be controlled by MCH **510** can be configured or programmed during initialization or after initialization has completed. The MCH **510** can partition or parse the memory space in various ways that are optimized for a particular application that the host system needs to run or execute. In one embodiment, the CDC **502** maps the actual physical Flash **506** and DRAM **508** memory space using the information sent by MCH **510** via the first command. In one embodiment, the CDC **502** maps the memory address space of any one of the Flash **506** and DRAM **508** memory subsystems using memory address space information that is received from the host system, stored in a register within FDHDIMM **500**, or stored in a memory location of a non-volatile memory subsystem, for example a portion of Flash **506** or a separate non-volatile memory subsystem. In one embodiment, the memory address space information corresponds to a portion of initialization information of the FDHDIMM **500**.

In one embodiment, MCH **510** may send a command to restore a certain amount of data information from Flash **506** to DRAM **508**. The CDC **502** provides control information to DMgr **504** to appropriately copy the necessary information from Flash **506** to the DRAM **508**. This operation can provide support for various host system booting operations and/or a special host system power up operation.

In one embodiment, MCH **510** sends a command which may include various fields comprising control information regarding data transfer size, data format options, and/or startup time. CDC **502** receives and interprets the command and provides control signals to DMgr **504** to control the data traffic between the Flash **506**, the DRAM **508**, and the MCH **510**. For example, DMgr **504** receives the data transfer size, formatting information, direction of data flow (via one or more multiplexers such as **611**, **612**, **621**, **622** as detailed below), and the starting time of the actual data transfer from CDC **502**. DMgr **504** may also receive additional control information from the CDC **502** to establish a data flow path and/or to correctly establish the data transfer fabric. In certain embodiments, DMgr **504** also functions as a bi-directional data transfer fabric. For example, DMgr **504** may have more than 2 sets of data ports facing the Flash **506** and the DRAM **508**. Multiplexers **611** and **612** provide controllable data paths from any one of the DRAMs **508**(**1**) and **508**(**2**) (DRAM-A and DRAM-B) to any one of the MCH **510** and the Flash **506**. Similarly multiplexers **621** and **622** provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs **508**(**1**) and **508**(**2**) (DRAM-A and DRAM-B). In one embodiment, DRAM **508**(**1**) is a segment of DRAM **508**, while in other embodiments, DRAM **508**(**1**) is a separate DRAM memory subsystem. It will be understood that each memory segment can comprise one or more memory circuits, a memory devices, and/or memory integrated circuits. Of course other configurations for DRAM **508** are possible, and other data transfer fabrics using complex data paths and suitable types of multiplexing logic are contemplated.

In accordance with one embodiment, the two sets of multiplexors **611**, **612** and **621**, **622** allow independent data transfer to Flash **506** from DRAM-A **508**(**1**) and DRAM-B **508**(**2**). For example, in response to one or more control signals or a command from CDC **502**, DMgr **504** can transfer data from DRAM-A **508**(**1**) to MCH **510**, via multiplexer **611**, at the same time as from DRAM-B **508**(**2**)

to the Flash **506**, via multiplexer **612**; or data is transferred from DRAM-B **508**(**2**) to MCH **510**, via multiplexer **611**, and simultaneously data is transferred from the Flash **506** to DRAM-A **508**(**1**), via multiplexer **621**. Further, in the same way that data can be transferred to or from the DRAM in both device-wide or segment-by-segment fashion, data can be transferred to or from the flash memory in device-wide or segment-by-segment fashion, and the flash memory can be addressed and accessed accordingly.

In accordance with one embodiment the illustrated arrangement of data transfer fabric of DMgr **504** also allows the CDC **502** to control data transfer from the Flash memory to the MCH by buffering the data from the Flash **506** using a buffer **602**, and matching the data rate and/or data format of MCH **510**. The buffer **602** is shown in FIG. **6** as a portion of a data format module **604**; however, buffer **602** may also be a distributed buffer such that one buffer is used for each one of the set of multiplexer logic elements shown as multiplexers **611**, **612**, **621**, and **622**. Various buffer arrangements may be used, such as a programmable size buffer to meet the requirement of a given system design requirement, for example the disparity between read/write access time; or overall system performance, for example latency. In certain embodiments, the buffer **604** may introduce one or more clock cycle delays into a data communication path between MCH **510**, DRAM **508**, and Flash **506**.

In certain embodiments, data format module **604** contains a data formatting subsystem (not shown) to enable DMgr **504** to format and perform data transfer in accordance with control information received from CDC**502**. Data buffer **604** of data format module **602**, discussed above, also supports a wide data bus **606** coupled to the Flash memory **506** operating at a first frequency, while receiving data from DRAM **508** using a relatively smaller width data bus **608** operating at a second frequency, the second frequency being larger than the first frequency in certain embodiments. The buffer **602** is designed to match the data flow rate between the DRAM **508** and the Flash **506**.

A register **690** provides the ability to register commands received from MCH **510** via C/A **560** (FIG. **5**A). The register **690** may communicate these commands to CDC **502** and/or to the DRAM **508** and/or Flash **506**. The register **690** communicates these registered commands to CDC **502** for processing. The register **690** may also include multiple registers (not shown), such that it can provide the ability to register multiple commands, a sequence of commands, or provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received form MCH **510**.

In certain embodiments, the register **690** may register commands from MCH **510** and transmit the registered commands to DRAM **508** and/or Flash **506** memory subsystems. In certain embodiments, the CDC **502** monitors commands received from MCH **510**, via control and address bus C/A **560**, and provides appropriate control information to DMgr **504**, DRAM **508**, or Flash **506** to execute these commands and perform data transfer operations between MCH **510** and FDHDIMM **500** via MCH data bus **610**.

FIG. **7** illustrates a functional block diagram of the CDC **502**. In certain embodiments, the major functional blocks of the CDC **502** are a DRAM control block DRAMCtrl **702**, Flash control block FlashCtrl **704**, MCH command interpreter Cmdlnt **706**, DRAM-Flash interface scheduler Scheduler **708**, and DMgr control block (DMgrCtrl) **710**.

In accordance with one embodiment, DRAMCtrl **702** generates DRAM commands that are independent from the commands issued by the MCH **510**. In accordance with one embodiment, when the MCH **510** initiates a read/write operation from/to the same DRAM **508** that is currently executing a command from the DRAMCtrl **702**, then the CDC **502** may choose to instruct DRAMCtrl **702** to abort its operation in order to execute the operation initiated by the MCH. However, the CDC **502** may also pipeline the operation so that it causes DRAMCtrl **702** to either halt or complete its current operation prior to executing that of the MCH. The CDC **502** may also instruct DRAMCtrl **702** to resume its operation once the command from MCH **510** is completed.

In accordance with one embodiment, the FlashCtrl **704** generates appropriate Flash commands for the proper read/write operations. The Cmdlnt **706** intercepts commands received from MCH **510** and generates the appropriate control information and control signals and transmit them to the appropriate FDHDIMM functional block. For example, Cmdlnt **706** issues an interrupt signal to the DRAMCtrl **702** when the MCH issues a command that collides (conflicts) with the currently executing or pending commands that DRAMCtrl **702** has initiated independently from MCH **510**, thus subordinating these commands to those from the MCH. The Scheduler **708** schedules the Flash-DRAM interface operation such that there is no resource conflict in the DMgr **504**. In accordance with one embodiment, the Scheduler **708** assigns time slots for the DRAMCtrl **702** and FlashCtrl **704** operation based on the current status and the pending command received or to be received from the MCH. The DMgrCtrl **710** generates and sends appropriate control information and control signals for the proper operation and control of the data transfer fabric to enable or disable data paths between Flash **506**, DRAM **508**, and the MCH **510**.

FIG. **8**A is a block diagram showing a Flash-DRAM hybrid DIMM (FDHDIMM). As seen from FIG. **8**A, this Flash-DRAM hybrid DIMM requires two separate and independent address buses to separately control the address spaces: one for the Flash memory Flash **506** and the other for the DRAM memory DRAM **508**. The MCH treats the DRAM **508** and Flash **506** as separate memory subsystems, for example DRAM and SSD/HD memory subsystems. The memory in each address space is controlled directly by the MCH. However, the on-DIMM data path between Flash **506** and DRAM **508** allows for direct data transfer to occur between the Flash **506** and the DRAM **508** in response to control information from Ctrl **502**. In this embodiment, this data transfer mechanism provides direct support for executing commands from the MCH without having the MCH directly controlling the data transfer, and thus improving data transfer performance from Flash **506** to the DRAM **508**. However, the MCH needs to manage two address spaces and two different memory protocols simultaneously. Moreover, the MCH needs to map the DRAM memory space into the Flash memory space, and the data interface time suffers due to the difference in the data access time between the Flash memory and the DRAM memory.

In accordance with one embodiment, a memory space mapping of a Flash-DRAM hybrid DIMM is shown in FIG. **8**B. A memory controller of a host system (not shown) controls both of the DRAM **508** address space and the Flash **506** address space using a single unified address space. The CDC **502** receives memory access commands from the MCH and generates control information for appropriate mapping and data transfer between Flash and DRAM memory subsystem to properly carry out the memory access commands. In one embodiment, the memory controller of the host system views the large Flash memory space as a DRAM memory space, and accesses this unified memory

space with a standard DDR (double data rate) protocol used for accessing DRAM. The unified memory space in this case can exhibit overlapping memory address space between the Flash **506** and the DRAM **508**. The overlapping memory address space may be used as a temporary storage or buffer for data transfer between the Flash **506** and the DRAM **508**. For example, the DRAM memory space may hold a copy of data from the selected Flash memory space such that the MCH can access this data normally via DDR memory access commands. The CDC **502** controls the operation of the Flash **506** and DRAM **508** memory subsystems in response to commands received from a memory controller of a host system.

In one embodiment, the unified memory space corresponds to a contiguous address space comprising a first portion of the address space of the Flash **506** and a first portion of the address space of the DRAM **508**. The first portion of the address space of the Flash **506** can be determined via a first programmable register holding a first value corresponding to the desired Flash memory size to be used. Similarly, the first portion of the address space of the DRAM **508** can be determined via a second programmable register holding a second value corresponding to the desired DRAM memory size to be used. In one embodiment, any one of the first portion of the address space of the Flash **506** and the first portion of the address space of the DRAM **508** is determined via a first value corresponding to a desired performance or memory size, the first value being received by the CDC **502** via a command sent by memory controller of the host system.

In accordance with one embodiment, a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM is shown in FIG. **9**. In certain embodiments, data transfer from the Flash **506** to the DRAM **508** occurs in accordance with memory access commands which the CDC **502** receives from the memory controller of the host system. In certain embodiments, the CDC **502** controls the data transfer from the DRAM **508** to the Flash **506** so as to avoid conflict with any memory operation that is currently being executed. For example, when all the pages in a particular DRAM memory block are closed. The CDC **502** partitions the DRAM memory space into a number of blocks for the purpose of optimally supporting the desired application. The controller can configure memory space in the memory module based on at least one of one or more commands received from the MCH, instructions received from the MCH, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value. Furthermore, the block size can be configurable by the memory controller of the host system, such that the number pages in a block can be optimized to support a particular application or a task. Furthermore, the block size may be configured on-the-fly, e.g. CDC **502** can receive instruction regarding a desired block size from the memory controller via a memory command, or via a programmable value.

In certain embodiments, a memory controller can access the memory module using a standard access protocol, such as JEDEC's DDR DRAM, by sending a memory access command to the CDC **502** which in turn determines what type of a data transfer operation it is and the corresponding target address where the data information is stored, e.g. data information is stored in the DRAM **508** or Flash **506** memory subsystems. In response to a read operation, if the CDC **502** determines that data information, e.g. a page (or block), does not reside in the DRAM **508** but resides in Flash **506**, then the CDC **502** initiates and controls all necessary data transfer operations from Flash **506** to DRAM **508** and subsequently to the memory controller. In one embodiment, once the CDC **502** completes the data transfer operation of the requested data information from the Flash **506** to the DRAM **508**, the CDC **502** alerts the memory controller to retrieve the data information from the DRAM **508**. In on embodiment, the memory controller initiates the copying of data information from Flash **506** to DRAM **508** by writing, into a register in the CDC **502**, the target Flash address along with a valid block size. The CDC **502** in turn, executes appropriate operations and generates control information to copy the data information to the DRAM **508**. Consequently, the memory controller can access or retrieve the data information using standard memory access commands or protocol.

An exemplary flow chart is shown in FIG. **9**, a starting step or power up **902**, is followed by an initialization step **904**, the memory controller initiates, at step **906**, a data move from the Flash **506** to the DRAM **508** by writing target address and size, to a control register in the CDC **502**, which then copies, at **908**, data information from the Flash **506** to the DRAM **508** and erases the block in the Flash. Erasing the data information from Flash may be accomplished independently from (or concurrently with) other steps that CDC **502** performs in this flow chart, i.e. other steps can be executed concurrently with the Erase the Flash block step. Once the data information or a block of data information is thus moved to the DRAM **508**, the memory controller can operate on this data block using standard memory access protocol or commands at **910**. The CDC **502** checks, at **912**, if any of the DRAM **508** blocks, or copied blocks, are closed. If the memory controller closed any open blocks in DRAM **508**, then the CDC **502** initiate a Flash write to write the closed block from the DRAM **508** to the Flash **506**, at **914**. In addition, the memory controller, at **916**, reopens the closed block that is currently being written into the Flash **506**, then the CDC **502** stops the Flash write operation and erases the Flash block which was being written to, as shown at **918**. Otherwise, the CDC **502** continues and completes the writing operation to the Flash at **920**.

The dashed lines in FIG. **9** indicate independent or parallel activities that can be performed by the CDC **502**. At any time the CDC **502** receives a DRAM load command from a memory controller which writes a Flash target address and/or block size information into the RC register(s) at **922**, as described above, then the CDC **502** executes a load DRAM w/RC step **906** and initiates another branch (or a thread) of activities that includes steps **908-922**. In one embodiment, the CDC **502** controls the data transfer operations between DRAM **508** and Flash **506** such that the Flash **506** is completely hidden from the memory controller. The CDC **502** monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulate both Flash **506** and DRAM **508** memory subsystems to perform the requested memory access operation and thus achieve the desired results. The memory controller does not interface directly with the Flash memory subsystem. Instead, the memory controller interfaces with the CDC **502** and/or DMgr **504** as shown in FIG. **5** and FIG. **6**. Moreover, the memory controller may use one or more protocol, such as DDR, DDR2, DDR3, DDR4 protocols or the like.

In accordance with one embodiment, an example of mapping a DRAM address space to Flash memory address space is shown in FIG. **10**. Two sets (**1002**, **1004**) of address

bits AD**6** to AD**17**, forming a 24 bit extended memory page address, are allocated for the block address. For example, assuming a Block size of 256K Bytes, then a 24-bit block address space (using the two sets of AD**6** to AD**17** **1002** and **1004**) would enable access to 4 TB of Flash memory storage space. If a memory module has 1 GB of DRAM storage capacity, then it can hold approximately 4K Blocks of data in the DRAM memory, each Block comprise 256 K Bytes of data. The DRAM address space, corresponding to the 4K blocks, can be assigned to different virtual ranks and banks, where the number of virtual ranks and banks is configurable and can be manipulated to meet a specific design or performance needs. For example, if a 1G Bytes memory module is configured to comprise two ranks with eight banks per rank, then each bank would hold two hundred fifty (**250**) blocks or the equivalent of 62 M Bytes or 62K pages, where each page correspond to a 1K Bytes. Other configurations using different page, block, banks, or ranks numbers may also be used. Furthermore, an exemplary mapping of 24-bit DDR DIMM block address to Flash memory address, using Block addressing as described above, is shown in FIG. **10**. The 24-bit can be decomposed into fields, such as a logical unit number LUN address **1061** field, a Block address **1051** field, a Plane address **1041**, a Page address **1031**, and a group of least significant address bits A_0A_1 **1021**. The Plane address **1041** is a sub address of the block address, and it may be used to support multiple page IO so as to improve Flash memory subsystem operation. In this example, it is understood that different number of bits may be allocated to each field of the 24-bit

The CDC **502** manages the block write-back operation by queuing the blocks that are ready to be written back to the Flash memory. As described above, if any page in a queued block for a write operation is reopened, then the CDC **502** will stop the queued block write operation, and remove the block from the queue. Once all the pages in a block are closed, then the CDC **502** restarts the write-back operation and queue the block for a write operation.

In accordance with one embodiment, an exemplary read operation from Flash **506** to DRAM **508** can be performed in approximately 400 μs, while a write operation from DRAM **508** to Flash **506** can be performed in approximately 22 ms resulting in a read to write ratio of 55 to 1. Therefore, if the average time a host system's memory controller spends accessing data information in a Block of DRAM is about 22 ms (that is the duration that a Block comprises one or more pages that are open), then the block write-back operation from DRAM to Flash would not impact performance and hence the disparity between read and write access may be completely hidden from the memory controller. If the block usage time is 11 ms instead of 22 ms, then the CDC **502** control the data transfer operation between DRAM **508** and Flash **506** such that there are no more than 9 closed blocks in the queue to be written-back to the Flash memory, hence approximately an average of 100 ms can be maintained for a standard DDR DRAM operation. Moreover, the number of closed Blocks in the queue to be written-back to the Flash memory subsystem varies with the average block usage time and the desired performance for a specific host system or for a specific application running using the host system resources.

Consequently, the maximum number of closed Blocks to be written-back to Flash can be approximated to be

((# of blocks per bank)/(ratio of 'Flash_block_write-_time' to 'Flash_read_time'))*((Block usage time)/('Flash_block_write_time'))

In order to maintain less than 100 ms time period for queued write-back Blocks, then using a Flash memory subsystem having 22 ms write access time per Block would results in a maximum number of four Blocks to be queued for write operation to Flash **506**. Therefore, on average approximately 88 ms (=22 ms*4) for blocks means that each bank should not have more than four Blocks that need to be written back to the Flash **506**.

The above equation also indicates that bigger DRAM memory space can support shorter block usage times. For example, 2 GB of DRAM memory allows the 8 closed blocks to be written-back to Flash. The table in FIG. **11** provides an estimation of the maximum allowed closed blocks in the queue to be written back to the Flash memory for different DRAM density using various average block use time.

Certain embodiments described herein include a memory system which can communicate with a host system such as a disk controller of a computer system. The memory system can include volatile and non-volatile memory, and a controller. The controller backs up the volatile memory using the non-volatile memory in the event of a trigger condition. Trigger conditions can include, for example, a power failure, power reduction, request by the host system, etc. In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source which does not comprise a battery and may include, for example, a capacitor or capacitor array.

In certain embodiments, the memory system can be configured such that the operation of the volatile memory is not adversely affected by the non-volatile memory or by th controller when the volatile memory is interacting with the host system. For example, one or more isolation devices may isolate the non-volatile memory and the controller from the volatile memory when the volatile memory is interacting with the host system and may allow communication between the volatile memory and the non-volatile memory when the data of the volatile memory is being restored or backed-up. This configuration generally protects the operation of the volatile memory when isolated while providing backup and restore capability in the event of a trigger condition, such as a power failure.

In certain embodiments described herein, the memory system includes a power module which provides power to the various components of the memory system from different sources based on a state of the memory system in relation to a trigger condition (e.g., a power failure). The power module may switch the source of the power to the various components in order to efficiently provide power in the event of the power failure. For example, when no power failure is detected, the power module may provide power to certain components, such as the volatile memory, from system power while charging a secondary power source (e.g., a capacitor array). In the event of a power failure or other trigger condition, the power module may power the volatile memory elements using the previously charged secondary power source.

In certain embodiments, the power module. transitions relatively smoothly from powering the volatile memory with system power to powering it with the secondary power source. For example, the power system may power volatile memory with a third power source from the time the memory system detects that power failure is likely to occur until the time the memory system detects that the power failure has actually occurred.

In certain embodiments, the volatile memory system can be operated at a reduced frequency during backup and/or

restore operations which can improve the efficiency of the system and save power. In some embodiments, during backup and/or restore operations, the volatile memory communicates with the non-volatile memory by writing and/or. reading data words in bit-wise slices instead of by writing entire words at once. In certain embodiments, when each slice is being written to or read from the volatile memory the unused slice(s) of volatile memory is not active, which can reduce the power consumption of the system.

In yet other embodiments, the non-volatile memory can include at least 100 percent more storage capacity than the volatile memory. This configuration can allow the memory system to efficiently handle subsequent trigger conditions.

FIG. **12** is a block diagram of an example memory system **1010** compatible with certain embodiments described herein. The memory system **1010** can be coupled to a host computer system and can include a volatile memory subsystem **1030**, a non-volatile memory subsystem **1040**, and a controller **1062** operatively coupled to the non-volatile memory subsystem **1040**. In certain embodiments, the memory system **1010** includes at least one circuit **1052** configured to selectively operatively decouple the controller **1062** from the volatile memory subsystem **1030**.

In certain embodiments, the memory system **1010** comprises a memory module. The memory system **1010** may comprise a printed-circuit board (PCB) **1020**. In certain embodiments, the memory system **1010** has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, or 8-GB. Other volatile memory capacities are also compatible with certain embodiments described herein. In certain embodiments, the memory system **10** has a non-volatile memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or 32-GB. Other non-volatile memory capacities are also compatible with certain embodiments described herein. In addition, memory systems **1010** having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the PCB **1020** has an industry-standard form factor. For example, the PCB **1020** can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB **1020** has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB **1020** has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FB-DIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. For example, in other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

In certain preferred embodiments, the memory system **1010** is in electrical communication with the host system. In other embodiments, the memory system **1010** may communicate with a host system using some other type of communication, such as, for example, optical communication. Examples of host systems include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The memory system **1010** can be in communication with a disk controller of a computer system, for example. The PCB **1020** can comprise an interface **1022** that is configured to be in electrical communication with the host system (not shown). For example, the interface **1022** can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface **1022** of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system **1010** and the host system. For example, the interface **1022** can comprise a standard 240-pin DDR2 edge connector.

The volatile memory subsystem **1030** comprises a plurality of volatile memory elements **1032** and the non-volatile memory subsystem **1040** comprises a plurality of non-volatile memory elements **1042**. Certain embodiments described herein advantageously provide nonvolatile storage via the non-volatile memory subsystem **1040** in addition to high-performance (e.g., high speed) storage via the volatile memory subsystem **1030**. In certain embodiments, the first plurality of volatile memory elements **1032** comprises two or more dynamic random-access memory (DRAM) elements. Types of DRAM elements **1032** compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and synchronous DRAM (SDRAM). For example, in the block diagram of FIG. **12**, the first memory bank **1030** comprises eight 64M×8 DDR2 SDRAM elements **1032**. The volatile memory elements **1032** may comprise other types of memory elements such as static random-access memory (SRAM). In addition, volatile memory elements **1032** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Volatile memory elements **1032** compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

In certain embodiments, the second plurality of non-volatile memory elements **1042** comprises one or more flash memory elements. Types of flash memory elements **1042** compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC). For example, in the block diagram of FIG. **12**, the second memory bank **1040** comprises 512 MB of flash memory organized as four 128 Mb×8 NAND flash memory elements **1042**. In addition, nonvolatile memory elements **1042** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Non-volatile memory elements **1042** compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BOA), fine-pitch BOA (FBGA), micro-BOA (POA), mini-BGA (mBGA), and chip-scale packaging (CSP).

FIG. **13** is a block diagram of an example memory module **10** with ECC (error-correcting code) having a volatile memory subsystem **1030** with nine volatile memory elements **1032** and a non-volatile memory subsystem **1040** with five non-volatile memory elements **1042** in accordance with certain embodiments described herein. The additional memory element **1032** of the first memory bank **1030** and the additional memory element **1042** of the second memory bank **1040** provide the ECC capability. In certain other embodiments, the volatile memory subsystem **1030** comprises other numbers of volatile memory elements **1032** (e.g., 2, 3, 4, 5, 6, 7, more than 9). In certain embodiments, the non-volatile memory subsystem **1040** comprises other numbers of nonvolatile memory elements **1042** (e.g., 2, 3, more than 5).

Referring to FIG. **12**, in certain embodiments, the logic element **1070** comprises a field-programmable gate array (FPGA). In certain embodiments, the logic element **1070** comprises an FPGA available from Lattice Semiconductor Corporation which includes an internal flash. In certain other embodiments, the logic element **1070** comprises an FPOA available from another vendor. The internal flash can improve the speed of the memory system **1010** and save physical space. Other types of logic elements **1070** compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element **1070** is a custom device. In certain embodiments, the logic element **1070** comprises various discrete electrical elements, while in certain other embodiments, the logic element **1070** comprises one or more integrated circuits. FIG. **14** is a block diagram of an example memory module **1010** having a microcontroller unit **1060** and logic element **1070** integrated into a single controller **1062** in accordance with certain embodiments described herein. In certain embodiments, the controller **1062** includes one or more other components. For example, in one embodiment, an FPGA without an internal flash is used and the controller **1062** includes a separate flash memory component which stores configuration information to program the FPGA.

In certain embodiments, the at least one circuit **1052** comprises one or more switches coupled to the volatile memory subsystem **1030**, to the controller **1062**, and to the host computer (e.g., via the interface **1022**, as schematically illustrated by FIGS. **12-14**). The one or more switches are responsive to signals (e.g., from the controller **1062**) to selectively operatively decouple the controller **1062** from the volatile memory subsystem **1030** and to selectively operatively couple the controller **1062** to the volatile memory subsystem **1030**. In addition, in certain embodiments, the at least one circuit **1052** selectively operatively couples and decouples the volatile memory subsystem **1030** and the host system.

In certain embodiments, the volatile memory subsystem **1030** can comprise a registered DIMM subsystem comprising one or more registers **1160** and a plurality of DRAM elements **1180**, as schematically illustrated by FIG. **15**A. In certain such embodiments, the at least one circuit **1052** can comprise one or more switches **1172** coupled to the controller **1062** (e.g., logic element **1070**) and to the volatile memory subsystem **1030** which can be actuated to couple and decouple the controller **1062** to and from the volatile memory subsystem **1030**, respectively. The memory system **1010** further comprises one or more switches **1170** coupled to the one or more registers **1160** and to the plurality of DRAM elements **1180** as schematically illustrated by FIG. **15**A. The one or more switches **1170** can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem **1030** to the host system **1150**. In certain other embodiments, as schematically illustrated by FIG. **15**B, the one or more switches **1174** are also coupled to the one or more registers **1160** and to a power source **1162** for the one or more registers **1160**. The one or more switches **1174** can be selectively switched to turn power on or off to the one or more registers **1160**, thereby selectively operatively coupling the volatile memory subsystem **1030** to the host system **1150**. As schematically illustrated by FIG. **15**C, in certain embodiments the at least one circuit **1052** comprises a dynamic on-die termination (ODT) **1176** circuit of the logic element **1070**. For example, the logic element **1070** can comprise a dynamic ODT circuit **1176** which selectively operatively couples and decouples the logic element **1070** to and from the volatile memory subsystem **1030**, respectively. In addition, and similar to the example embodiment of FIG. **15**A described above, the one or more switches **1170** can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem **1030** to the host system **1150**.

Certain embodiments described herein utilize the non-volatile memory subsystem **1040** as a flash "mirror" to provide backup of the volatile memory subsystem **1030** in the event of certain system conditions. For example, the non-volatile memory subsystem **1040** may backup the volatile memory subsystem **1030** in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system. In one embodiment, the nonvolatile memory subsystem **1040** holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition. In certain embodiments, the trigger condition occurs when the memory system **1010** detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is **1010** percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, **1010** percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. In various embodiments, a backup and/or restore operation may occur in reboot and/or non-reboot trigger conditions.

As schematically illustrated by FIGS. **12** and **13**, in certain embodiments, the controller **1062** may comprise a microcontroller unit (MCU) **1060** and a logic element **1070**. In certain embodiments, the MCU **1060** provides memory management for the non-volatile memory subsystem **1040** and controls data transfer between the volatile memory subsystem **30** and the nonvolatile memory subsystem **1040**. The MCU **1060** of certain embodiments comprises a 16-bit microcontroller, although other types of microcontrollers are also compatible with certain embodiments described herein. As schematically illustrated by FIGS. **12** and **13**, the logic element **1070** of certain embodiments is in electrical communication with the non-volatile memory subsystem **1040** and the MCU **1060**. The logic element **1070** can provide signal level translation between the volatile memory elements **1032** (e.g., 1.8V SSTL-2 for DDR2 SDRAM elements) and the non-volatile memory elements **1042** (e.g., 3V TTL for NAND flash memory elements). In certain embodiments, the logic element **1070** is also programmed to perform address/address translation between the volatile memory subsystem **1030** and the non-volatile memory subsystem **1040**. In certain preferred embodiments, 1-NAND type flash are used for the non-volatile memory elements **1042** because of their superior read speed and compact structure.

The memory system **1010** of certain embodiments is configured to be operated in at least two states. The at least two states can comprise a first state in which the controller **1062** and the non-volatile memory subsystem **1040** are operatively decoupled (e.g., isolated) from the volatile memory subsystem **1030** by the at least one circuit **1052** and a second state in which the volatile memory subsystem **1030** is operatively coupled to the controller **1062** to allow data to

be communicated between the volatile memory subsystem **1030** and the nonvolatile memory subsystem **1040** via the controller **1062**. The memory system **1010** may transition from the first state to the second state in response to a trigger condition, such as when the memory system **1010** detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up.

The memory system **1010** may further comprise a voltage monitor **1050**. The voltage monitor circuit **1050** monitors the voltage supplied by the host system via the interface **1022**. Upon detecting a low voltage condition (e.g., due to a power interruption to the host system), the voltage monitor circuit **1050** may transmit a signal to the controller **1062** indicative of the detected condition. The controller **1062** of certain embodiments responds to the signal from the voltage monitor circuit **1050** by transmitting a signal to the at least one circuit **1052** to operatively couple the controller to the volatile memory system **1030**, such that the memory system **1010** enters the second state. For example, the voltage monitor **1050** may send a signal to the MCU **1060** which responds by accessing the data on the volatile memory system **1030** and by executing a write cycle on the nonvolatile memory subsystem **1040**. During this write cycle, data is read from the volatile memory subsystem **1030** and is transferred to the non-volatile memory subsystem **1040** via the MCU **1060**. In certain embodiments, the voltage monitor circuit **1050** is part of the controller **1062** (e.g., part of the MCU **1060**) and the voltage monitor circuit **1050** transmits a signal to the other portions of the controller **1062** upon detecting a power threshold condition.

The isolation or operational decoupling of the volatile memory subsystem **1030** from the non-volatile memory subsystem in the first state can preserve the integrity of the operation of the memory system **1010** during periods of operation in which signals (e.g., data) are transmitted between the host system and the volatile memory subsystem **1030**. For example, in one embodiment during such periods of operation, the controller **1062** and the nonvolatile memory subsystem **1040** do not add a significant capacitive load to the volatile memory system **1030** when the memory system **1010** is in the first state. In certain such embodiments, the capacitive load of the controller **1062** and the non-volatile memory subsystem **1040** do not significantly affect the signals propagating between the volatile memory subsystem **1030** and the host system. This can be particularly advantageous in relatively high-speed memory systems where loading effects can be significant. In one preferred embodiment, the at least one circuit **1052** comprises an FSA1208 Low-Power, Eight-Port, Hi-Speed Isolation Switch from Fairchild Semiconductor. In other embodiments, the at least one circuit **1052** comprises other types of isolation devices.

Power may be supplied to the volatile memory subsystem **1030** from a first power supply (e.g., a system power supply) when the memory system **1010** is in the first state and from a second power supply **1080** when the memory system **1010** is in the second state. In certain embodiments, the memory system **1010** is in the first state when no trigger condition (e.g., a power failure) is present and the memory system **1010** enters the second state in response to a trigger condition. In certain embodiments, the memory system **1010** has a third state in which the controller **1062** is operatively decoupled from the volatile memory subsystem **1030** and power is supplied to the volatile memory subsystem **1030** from a third power supply (not shown). For example, in one embodiment the third power supply may provide power to the volatile memory subsystem **1030** when the memory system **1010** detects that a trigger condition is likely to occur but has not yet occurred.

In certain embodiments, the second power supply **1080** does not comprise a battery. Because a battery is not used, the second power supply **1080** of certain embodiments may be relatively easy to maintain, does not generally need to be replaced, and is relatively environmentally friendly. In certain embodiments, as schematically illustrated by FIGS. **12-14**, the second power supply **1080** comprises a step-up transformer **1082**, a step-down transformer **1084**, and a capacitor bank **1086** comprising one or more capacitors (e.g., double-layer capacitors). In one example embodiment, capacitors may take about three to four minutes to charge and about two minutes to discharge. In other embodiments, the one or more capacitors may take a longer time or a shorter time to charge and/or discharge. For example, in certain embodiments, the second power supply **1080** is configured to power the volatile memory subsystem **1030** for less than thirty minutes. In certain embodiments, the second power supply **1080** may comprise a battery. For example, in certain embodiments, the second power supply **1080** comprises a battery and one or more capacitors and is configured to power the volatile memory subsystem **1030** for no more than thirty minutes.

In certain embodiments, the capacitor bank **1086** of the second power supply **1080** is charged by the first power supply while the memory system **1010** is in the first state. As a result, the second power supply **1080** is fully charged when the memory system **1010** enters the second state. The memory system **1010** and the second power supply **1080** may be located on the same printed circuit board **1020**. In other embodiments, the second power supply **1080** may not be on the same printed circuit board **1020** and may be tethered to the printed circuit board **1020**, for example.

When operating in the first state, in certain embodiments, the step-up transformer **1082** keeps the capacitor bank **1086** charged at a peak value. In certain embodiments, the step-down transformer **1084** acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements **1032** and 3.0V to the non-volatile flash memory elements **1042**) when operating in the second state (e.g., during power down). In certain embodiments, as schematically illustrated by FIGS. **12-14**, the memory module **1010** further comprises a switch **1090** (e.g., FET switch) that switches power provided to the controller **1062**, the volatile memory subsystem **1030**, and the non-volatile memory subsystem **1040**, between the power from the second power supply **1080** and the power from the first power supply (e.g., system power) received via the interface **1022**. For example, the switch **1090** may switch from the first power supply to the second power supply **1080** when the voltage monitor **1050** detects a low voltage condition. The switch **1090** of certain embodiments advantageously ensures that the volatile memory elements **1032** and non-volatile memory elements **1042** are powered long enough for the data to be transferred from the volatile memory elements **1032** and stored in the non-volatile memory elements **1042**. In certain embodiments, after the data transfer is complete, the switch **1090** then switches back to the first power supply and the controller **1062** transmits a signal to the at least one circuit **1052** to operatively decouple the controller **1062** from the volatile memory subsystem **1030**, such that the memory system **1010** reenters the first state.

When the memory system **1010** re-enters the first state, data may be transferred back from the non-volatile memory

subsystem **1040** to the volatile memory subsystem **1030** via the controller **1062**. The host system can then resume accessing the volatile memory subsystem **1030** of the memory module **1010**. In certain embodiments, after the memory system **1010** enters or re-enters the first state (e.g., after power is restored), the host system accesses the volatile memory subsystem **1030** rather than the non-volatile memory subsystem **1040** because the volatile memory elements **1032** have superior read/write characteristics. In certain embodiments, the transfer of data from the volatile memory bank **1030** to the nonvolatile memory bank **1040**, or from the non-volatile memory bank **1040** to the volatile. memory bank **1030**, takes less than one minute per GB.

In certain embodiments, the memory system **1010** protects the operation of the volatile memory when communicating with the host-system and provides backup and restore capability in the event of a trigger condition such as a power failure. In certain embodiments, the memory system **1010** copies the entire contents of the volatile memory subsystem **1030** into the nonvolatile memory subsystem **1040** on each backup operation. Moreover, in certain embodiments, the entire contents of the non-volatile memory subsystem **1040** are copied back into the volatile memory subsystem **1030** on each restore operation. In certain embodiments, the entire contents of the non-volatile memory subsystem **1040** are accessed for each backup and/or restore operation, such that the non-volatile memory subsystem **1040** (e.g., flash memory subsystem) is used generally uniformly across its memory space and wear-leveling is not performed by the memory system **1010**. In certain embodiments, avoiding wear-leveling can decrease cost and complexity of the memory system **1010** and can improve the performance of the memory system **1010**. In certain other embodiments, the entire contents of the volatile memory subsystem **1030** are not copied into the non-volatile memory subsystem **1040** on each backup operation, but only a partial copy is performed. In certain embodiments, other management capabilities such as bad-block management and error management for the flash memory elements of the non-volatile memory subsystem **1040** are performed in the controller **1062**.

The memory system **1010** generally operates as a write-back cache in certain embodiments. For example, in one embodiment, the host system (e.g., a disk controller) writes data to the volatile memory subsystem **1030** which then writes the data to non-volatile storage which is not part of the memory system **1010**, such as, for example, a hard disk. The disk controller may wait for an acknowledgment signal from the memory system **1010** indicating that the data has been written to the hard disk or is otherwise secure. The memory system **1010** of certain embodiments can decrease delays in the system operation by indicating that the data has been written to the hard disk before it has actually done so. In certain embodiments, the memory system **1010** will still be able to recover the data efficiently in the event of a power outage because of the backup and restore capabilities described herein. In certain other embodiments, the memory system **1010** may be operated as a write-through cache or as some other type of cache.

FIG. **16** schematically illustrates an example power module **1100** of the memory system **1010** in accordance with certain embodiments described herein. The power module **1100** provides power to the various components of the memory system **1010** using different elements based on a state of the memory system **1010** in relation to a trigger condition. In certain embodiments, the power module **1100** comprises one or more of the components described above with respect to FIG. **12**. For example, in certain embodiments, the power module **1100** includes the second power supply **1080** and the switch **1090**.

The power module **1100** provides a plurality of voltages to the memory system **1010** comprising non-volatile and volatile memory subsystems **1030**, **1040**. The plurality of voltages comprises at least a first voltage **1102** and a second voltage **1104**. The power module **1100** comprises an input **1106** providing a third voltage **1108** to the power module **1100** and a voltage conversion element **1120** configured to provide the second voltage **1104** to the memory system **1010**. The power module **1100** further comprises a first power element **1130** configured to selectively provide a fourth voltage **1110** to the conversion element **1120**. In certain embodiments, the first power element **1130** comprises a pulse-width modulation power controller. For example, in one example embodiment, the first power element **1130** is configured to receive a 1.8V input system voltage as the third voltage **1108** and to output a modulated 5V output as the fourth voltage **1110**.

The power module **1100** further comprises a second power element **1140** can be configured to selectively provide a fifth voltage **1112** to the conversion element **1120**. The power module **1100** can be configured to selectively provide the first voltage **1102** to the memory system **1010** either from the conversion element **1120** or from the input **1106**.

The power module **1100** can be configured to be operated in at least three states in certain embodiments. In a first state, the first voltage **1102** is provided to the memory system **1010** from the input **1106** and the fourth voltage **1110** is provided to the conversion element **1120** from the first power element **1130**. In a second state, the fourth voltage **1110** is provided to the conversion element **1120** from the first power element **1130** and the first voltage **1102** is provided to the memory system **1010** from the conversion element **1120**. In the third state, the fifth voltage **1112** is provided to the conversion element **1120** from the second power element **1140** and the first voltage **1104** is provided to the memory system **1010** from the conversion element **1120**.

In certain embodiments, the power module **1100** transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition has occurred. For example, the power module **1100** may transition to the second state when it detects that a power failure is about to occur and transitions to the third state when it detects that the power failure has occurred. In certain embodiments, providing the first voltage **1102** in the second state from the first power element **1130** rather than from the input **1106** allows a smoother transition from the first state to the third state. For example, in certain embodiments, providing the first voltage **1102** from the first power element **1130** has capacitive and other smoothing effects. In addition, switching the point of power transition to be between the conversion element **1120** and the first and second power elements **1130**, **1140** (e.g., the sources of the pre-regulated fourth voltage **1110** in the second state and the pre-regulated fifth voltage **1112** in the third state) can smooth out potential voltage spikes.

In certain embodiments, the second power element **1140** does not comprise a battery and may comprise one or more capacitors. For example, as schematically illustrated in FIG. **16**, the second power element **1140** comprises a capacitor array **1142**, a buck-boost converter **1144** which adjusts the voltage for charging the capacitor array and a voltage/current limiter **1146** which limits the charge current to the capacitor array **1142** and stops charging the capacitor array **1142** when it has reached a certain charge voltage. In one

example embodiment, the capacitor array **1142** comprises two 50 farad capacitors capable of holding a total charge of 4.6V. For example, in one example embodiment, the buck-boost converter **1144** receives a 1.8V system voltage (first voltage **1108**) and boosts the voltage to 4.3V which is outputted to the voltage current limiter **1146**. The voltage/current limiter **1146** limits the current going to the capacitor array **1142** to 1A and stops charging the array **1142** when it is charged to 4.3V. Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the second power element **1140** may include alternative embodiments. For example, different components and/or different value components may be used. For example, in other embodiments, a pure boost converter may be used instead of a buck-boost converter. In another embodiment, only one capacitor may be used instead of a capacitor array **1142**.

The conversion element **1120** can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element **1120** may comprise a plurality of sub-blocks **1122**, **1124**, **1126** as schematically illustrated by FIG. **16**, which can provide more voltages in addition to the second voltage **1104** to the memory system **1010**. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system **1010**. For example, in one embodiment, sub-block **1122** comprises a buck converter, sub-block **1124** comprises a dual buck converter, and sub-block **1126** comprises a buck-boost converter as schematically illustrated by FIG. **16**. Various other components for the sub-blocks **1122**, **1124**, **1126** of the conversion element **1120** are also compatible with certain embodiments described herein. In certain embodiments, the conversion element **1120** receives as input either the fourth voltage **1110** from the first power element **1130** or the fifth voltage **1112** from the second power element **1140**, depending on the state of the power module **1100**, and reduces the input to an appropriate amount for powering various components of the memory system. For example, the buck-converter of sub-block **1122** can provide 1.8V at 2A for about 60 seconds to the volatile memory elements **1032** (e.g., DRAM), the non-volatile memory elements **1042** (e.g., flash), and the controller **1062** (e.g., an FPGA) in one embodiment. The sub-block **1124** can provide the second voltage **1104** as well as another reduced voltage **1105** to the memory system **1010**. In one example embodiment, the second voltage **1104** is 2.5V and is used to power the at least one circuit **1052** (e.g., isolation device) and the other reduced voltage **1105** is 1.2V and is used to power the controller **1062** (e.g., FPGA). The subblock **1126** can provide yet another voltage **1107** to the memory system **1010**. For example, the voltage **1107** may be 3.3V and may be used to power both the controller **1062** and the at least one circuit **1052**.

Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the conversion element **1120** may include alternative embodiments. For example, there may be more or less sub-blocks which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values. In one embodiment, the volatile memory elements **1032** and nonvolatile memory elements **1042** are powered using independent voltages and are not both powered using the first voltage **1102**.

FIG. **17** is a flowchart of an example method **1200** of providing a first voltage **1102** and a second voltage **1104** to a memory system **1010** including volatile and nonvolatile memory subsystems **1030**, **1040**. While the method **1200** is described herein by reference to the memory system **1010** schematically illustrated by FIGS. **12-15**, other memory systems are also compatible with embodiments of the method **1200**. During a first condition, the method **1200** comprises providing the first voltage **1102** to the memory system **1010** from an input power supply **1106** and providing the second voltage **1104** to the memory system **1010** from a first power subsystem in operational block **1210**. For example, in one embodiment, the first power subsystem comprises the first power element **1130** and the voltage conversion element **1120** described above with respect to FIG. **16**. In other embodiments, other first power subsystems are used.

The method **1200** further comprises detecting a second condition in operational block **1220**. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. During the second condition, the method **1200** comprises providing the first voltage **1102** and the second voltage **1104** to the memory system **1010** from the first power subsystem in an operational block **1230**. For example, referring to FIG. **16**, a switch **1148** can be toggled to provide the first voltage **1102** from the conversion element **1120** rather than from the input power supply.

The method **1200** further comprises charging a second power subsystem in operational block **1240**. In certain embodiments, the second power subsystem comprises the second power element **1140** or another power supply that does not comprise a battery. For example, in one embodiment, the second power subsystem comprises the second power element **1140** and the voltage conversion element **1120** described above with respect to FIG. **16**. In other embodiments, some other second power subsystem is used.

The method **1200** further comprises detecting a third condition in an operational block **1250** and during the third condition, providing the first voltage **1102** and the second voltage **1104** to the memory system **1010** from the second power subsystem **1140** in an operational block **1260**. In certain embodiments, detecting the third condition comprises detecting that the trigger condition has occurred. The trigger condition may comprise various conditions described herein. In various embodiments, for example, the trigger condition comprises a power reduction, power failure, or system hang-up. The operational blocks of the method **1200** may be performed in different orders in various embodiments. For example, in certain embodiments, the second power subsystem **1140** is charged before detecting the second condition.

In certain embodiments, the memory system **1010** comprises a volatile memory subsystem **1030** and a non-volatile memory subsystem **1040** comprising at least 100 percent more storage capacity than does the volatile memory subsystem. The memory system **1010** also comprises a controller **1062** operatively coupled to the volatile memory subsystem **1030** and operatively coupled to the non-volatile memory subsystem **1040**. The controller **1062** can be configured to allow data to be communicated between the volatile memory subsystem **1030** and the host system when the memory system **1010** is operating in a first state and to allow data to be communicated between the volatile memory subsystem **1030** and the non-volatile memory subsystem **1040** when the memory system **1010** is operating in a second state.

Although the memory system **1010** having extra storage capacity of the non-volatile memory subsystem **1040** has been described with respect to certain embodiments, alter-

native configurations exist. For example, in certain embodiments, there may be more than 100 percent more storage capacity in the non-volatile memory subsystem **1040** than in the volatile memory subsystem **1030**. In various embodiments, there may be at least 200, 300, or 400 percent more storage capacity in the non-volatile memory subsystem **1040** than in the volatile memory subsystem **1030**. In other embodiments, the non-volatile memory subsystem **1040** includes at least some other integer multiples of the storage capacity of the volatile memory subsystem **1030**. In some embodiments, the non-volatile memory subsystem **1040** includes a non-integer multiple of the storage capacity of the volatile memory subsystem **1030**. In one embodiment, the non-volatile memory subsystem **1040** includes less than 100 percent more storage capacity than does the volatile memory subsystem **1030**.

The extra storage capacity of the non-volatile memory subsystem **1040** can be used to improve the backup capability of the memory system **1010**. In certain embodiments in which data can only be written to portions of the non-volatile memory subsystem **1040** which do not contain data (e.g., portions which have been erased), the extra storage capacity of the nonvolatile memory subsystem **1040** allows the volatile memory subsystem **1030** to be backed up in the event of a subsequent power failure or other trigger event. For example, the extra storage capacity of the non-volatile memory subsystem **1040** may allow the memory system **1010** to backup the volatile memory subsystem **1030** efficiently in the event of multiple trigger conditions (e.g., power failures). In the event of a first power failure, for example, the data in the volatile memory system **1030** is copied to a first, previously erased portion of the nonvolatile memory subsystem **1040** via the controller **1062**. Since the non-volatile memory subsystem **1040** has more storage capacity than does the volatile memory subsystem **1030**, there is a second portion of the non-volatile memory subsystem **1040** which does not have data from the volatile memory subsystem **1030** copied to it and which remains free of data (e.g., erased). Once system power is restored, the controller **1062** of the memory system **1010** restores the data to the volatile memory subsystem **1030** by copying the backed-up data from the non-volatile memory subsystem **1040** back to the volatile memory subsystem **1030**. After the data is restored, the memory system **1010** erases the non-volatile memory subsystem **1040**. While the first portion of the non-volatile memory subsystem **1040** is being erased, it may be temporarily unaccessible.

If a subsequent power failure occurs before the first portion of the non-volatile memory subsystem **1040** is completely erased, the volatile memory subsystem **1030** can be backed-up or stored again in the second portion of the non-volatile memory subsystem **1040** as described herein. In certain embodiments, the extra storage capacity of the non-volatile memory subsystem **1040** may allow the memory system **1010** to operate more efficiently. For example, because of the extra storage capacity of the non-volatile memory subsystem **1040**, the memory system **1010** can handle a higher frequency of trigger events that is not limited by the erase time of the non-volatile memory subsystem **1040**.

FIG. **18** is a flowchart of an example method **1300** of controlling a memory system **1010** operatively coupled to a host system and which includes a volatile memory subsystem **1030** and a non-volatile memory subsystem **1040**. In certain embodiments, the non-volatile memory subsystem **1040** comprises at least 100 percent more storage capacity than does the volatile memory subsystem **30** as described herein. While the method **1300** is described herein by reference to the memory system **1010** schematically illustrated by FIGS. **12-14**, the method **1300** can be practiced using other memory systems in accordance with certain embodiments described herein. In an operational block **1310**, the method **1300** comprises communicating data between the volatile memory subsystem **1030** and the host system when the memory system **1010** is in a first mode of operation. The method **1300** further comprises storing a first copy of data from the volatile memory subsystem **1030** to the non-volatile memory subsystem **1040** at a first time when the memory system **1010** is in a second mode of operation in an operational block **1320**.

In an operational block **1330**, the method **1300** comprises restoring the first copy of data from the non-volatile memory subsystem **1040** to the volatile memory subsystem **1030**. The method **1300** further comprises erasing the first copy of data from the non-volatile memory subsystem **1040** in an operational block **1340**. The method further comprises storing a second copy of data from the volatile memory subsystem **1030** to the non-volatile memory subsystem **1040** at a second time when the memory system **1010** is in the second mode of operation in an operational block **1350**. Storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem **1040**.

In some embodiments, the memory system **1010** enters the second mode of operation in response to a trigger condition, such as a power failure. In certain embodiments, the first copy of data and the second copy of data are stored in separate portions of the nonvolatile memory subsystem **1040**. The method **1300** can also include restoring the second copy of data from the non-volatile memory subsystem **1040** to the volatile memory subsystem **1030** in an operational block **1360**. The operational blocks of method **1300** referred to herein may be performed in different orders in various embodiments. For example, in some embodiments, the second copy of data is restored to the volatile memory subsystem **1030** at operational block **1360** before the first copy of data is completely erased in the operational block **1340**.

FIG. **19** schematically illustrates an example clock distribution topology **1400** of a memory system **1010** in accordance with certain embodiments described herein. The clock distribution topology **1400** generally illustrates the creation and routing of the clock signals provided to the various components of the memory system **1010**. A clock source **1402** such as, for example, a 25 MHz oscillator, generates a clock signal. The clock source **1402** may feed a clock generator **1404** which provides a clock signal **1406** to the controller **1062**, which may be an FPGA. In one embodiment, the clock generator **1404** generates a 125 MHz clock signal **1406**. The controller **1062** receives the clock signal **1406** and uses it to clock the controller **1062** master state control logic. For example, the master state control logic may control the general operation of an FPGA controller **1062**.

The clock signal **1406** can also be input into a clock divider **1410** which produces a frequency-divided version of the clock signal **1406**. In an example embodiment, the clock divider **1410** is a divide by two clock divider and produces a 62.5 MHz clock signal in response to the 125 MHz clock signal **1406**. A non-volatile memory phase-locked loop (PLL) block **1412** can be included (e.g., in the controller **1062**) which distributes a series of clock signals to the non-volatile memory subsystem **1040** and to associated control logic. For example, a series of clock signals **1414** can

be sent from the controller **1062** to the non-volatile memory subsystem **1040**. Another clock signal **1416** can be used by the controller logic which is dedicated to controlling the non-volatile memory subsystem **1040**. For example, the clock signal **1416** may clock the portion of the controller **1062** which is dedicated to generating address and/or control lines for the non-volatile memory subsystem **1040**. A feedback clock signal **1418** is fed back into the non-volatile memory PLL block **1412**. In one embodiment, the PLL block **1412** compares the feedback clock **1418** to the reference clock **1411** and varies the phase and frequency of its output until the reference **1411** and feedback **1418** clocks are phase and frequency matched.

A version of the clock signal **1406** such as the backup clock signal **1408** may be sent from the controller to the volatile memory subsystem **1030**. The clock signal **1408** may be, for example, a differential version of the clock signal **1406**. As described herein, the backup clock signal **1408** may be used to clock the volatile memory subsystem **1030** when the memory system **1010** is backing up the data from the volatile memory subsystem **1030** into the non-volatile memory subsystem **1040**. In certain embodiments, the backup clock signal **1408** may also be used to clock the volatile memory subsystem **1030** when the memory system **1010** is copying the backed-up data back into the volatile memory subsystem **1030** from the nonvolatile memory subsystem **1040** (also referred to as restoring the volatile memory subsystem **1030**). The volatile memory subsystem **1030** may normally be run at a higher frequency (e.g., DRAM running at 400 MHz) than the nonvolatile memory subsystem **1040** (e.g., flash memory running at 62.5 MHz) when communicating with the host system (e.g., when no trigger condition is present). However, in certain embodiments the volatile memory subsystem **1030** may be operated at a reduced frequency (e.g., at twice the frequency of the non-volatile memory subsystem **1040**) without introducing significant delay into the system during backup operation and/or restore operations. Running the volatile memory subsystem **1030** at the reduced frequency during a backup and/or restore operation may advantageously reduce overall power consumption of the memory system **1010**.

In one embodiment, the backup clock **1408** and the volatile memory system clock signal **1420** are received by a multiplexer **1422**, as schematically illustrated by FIG. **19**. The multiplexer **1422** can output either the volatile memory system clock signal **1420** or the backup clock signal **1408** depending on the backup state of the memory system **1010**. For example, when the memory system **1010** is not performing a backup or restore operation and is communicating with the host system (e.g., normal operation), the volatile memory system clock signal **1420** may be provided by the multiplexer **422** to the volatile memory PLL block **1424**. When the memory system **1010** is performing a backup (or restore) operation, the backup clock signal **1408** may be provided.

The volatile memory PLL block **1424** receives the volatile memory reference clock signal **1423** from the multiplexer **1422** and can generate a series of clock signals which are distributed to the volatile memory subsystem **1030** and associated control logic. For example, in one embodiment, the PLL block **1424** generates a series of clock signals **1426** which clock the volatile memory elements **1032**. A clock signal **1428** may be used to clock control logic associated with the volatile memory elements, such as one or more registers (e.g., the one or more registers of a registered DIMM). Another clock signal **1430** may be sent to the controller **1062**. A feedback clock signal **1432** is fed back into the volatile memory PLL block **1424**. In one embodiment, the PLL block **1424** compares the feedback clock signal **1432** to the reference clock signal **1423** and varies the phase and frequency of its output until the reference clock signal **1423** and the feedback clock signal **1432** clocks are phase and frequency matched.

The clock signal **1430** may be used by the controller **1062** to generate and distribute clock signals which will be used by controller logic which is configured to control the volatile memory subsystem **1030**. For example, control logic in the controller **1062** may be used to control the volatile memory subsystem **1030** during a backup or restore operation. The clock signal **1430** may be used as a reference clock signal for the PLL block **1434** which can generate one or more clocks **1438** used by logic in the controller **1062**. For example, the PLL block **1434** may generate one or more clock signals **1438** used to drive logic circuitry associated with controlling the volatile memory subsystem **1030**. In certain embodiments, the PLL block **1434** includes a feedback clock signal **1436** and operates in a similar manner to other PLL blocks described herein.

The clock signal **1430** may be used as a reference clock signal for the PLL block **1440** which may generate one or more clock signals used by a sub-block **1442** to generate one or more other clock signals **1444**. In one embodiment, for example, the volatile memory subsystem **1030** comprises DDR2 SDRAM elements and the sub-block **1442** generates one or more DDR2 compatible clock signals **1444**. A feedback clock signal **1446** is fed back into the PLL block **1440**. In certain embodiments, the PLL block **1440** operates in a similar manner to other PLL blocks described herein.

While described with respect to the example embodiment of FIG. **19**, various alternative clock distribution topologies are possible. For example, one or more of the clock signals have a different frequency in various other embodiments. In some embodiments, one or more of the clocks shown as differential signals are single ended signals. In one embodiment, the volatile memory subsystem **1030** operates on the volatile memory clock signal **1420** and there is no backup clock signal **1408**. In some embodiments, the volatile memory subsystem **1030** is operated at a reduced frequency during a backup operation and not during a restore operation. In other embodiments, the volatile memory subsystem **1030** is operated at a reduced frequency during a restore operation and not during a backup operation.

FIG. **20** is a flowchart of an example method **1500** of controlling a memory system **1010** operatively coupled to a host system. Although described with respect to the memory system **1010** described herein, the method **1500** is compatible with other memory systems. The memory system **1010** may include a clock distribution topology **1400** similar to the one described above with respect to FIG. **19** or another clock distribution topology. The memory system **1010** can include a volatile memory subsystem **1030** and a non-volatile memory subsystem **1040**.

In an operational block **1510**, the method **1500** comprises operating the volatile memory subsystem **1030** at a first frequency when the memory system **1010** is in a first mode of operation in which data is communicated between the volatile memory subsystem **1030** and the host system. In an operational block **1520**, the method **1500** comprises operating the non-volatile memory subsystem **1040** at a second frequency when the memory system **1010** is in a second mode of operation in which data is communicated between the volatile memory subsystem **1030** and the non-volatile memory subsystem **1040**. The method **1500** further comprises operating the volatile memory subsystem **1030** at a

third frequency in an operational block **1530** when the memory system **1010** is in the second mode of operation. In certain embodiments, the memory system **1010** is not powered by a battery when it is in the second mode of operation. The memory system **1010** may switch from the first mode of operation to the second mode of operation in response to a trigger condition. The trigger condition may be any trigger condition described herein such as, for example, a power failure condition. In certain embodiments, the second mode of operation includes both backup and restore operations as described herein. In other embodiments, the second mode of operation includes backup operations but not restore operations. In yet other embodiments, the second mode of operation includes restore operations but not backup operations.

The third frequency can be less than the first frequency. For example, the third frequency can be approximately equal to the second frequency. In certain embodiments, the reduced frequency operation is an optional mode. In yet other embodiments, the first, second and/or third frequencies are configurable by a user or by the memory system **1010**.

FIG. **21** schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments **1630**, **1640** of a volatile memory subsystem **1030** of a memory system **1010** to a controller **1062** of the memory system **1010**. While the example of FIG. **21** shows a topology including two DRAM segments **1630**, **1640** for the purposes of illustration, each address location of the volatile memory subsystem **1030** comprises more than the two segments in certain embodiments. The data lines **1632**, **1642** from the first DRAM segment **1630** and the second DRAM segment **1640** of the volatile memory subsystem **1030** are coupled to switches **1650**, **1652** which are coupled to the controller **1062** (e.g., logic element **1070**) of the memory system **1010**. The chip select lines **1634**, **1644** and the self-refresh lines **1636**, **1646** (e.g., CKe signals) of the first and second DRAM segments **1630**, **1640**, respectively, are coupled to the controller **1062**. In certain embodiments, the controller **1062** comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem **1030**. In certain embodiments, the buffer is a first-in, first out buffer (FIFO). In certain embodiments, data slices from each DRAM segment **1630**, **1640** comprise a portion of the volatile memory subsystem data bus. In one embodiment, for example, the volatile memory subsystem **1030** comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment **1630** may comprise 40 bits of the data word, and the second data slice from the second DRAM segment **1640** may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.

In certain embodiments, the switches **1650**, **1652** can each be selectively switched to selectively operatively couple the data lines **1632**, **1642**, respectively from the first and second DRAM segments **1630**, **1640** to the controller **1062**. The chip select lines **1634**, **1644** enable the first and second DRAM segments **1630**, **1640**, respectively, of the volatile memory subsystem **1030**, and the self-refresh lines **1636**, **1646** toggle the first and second DRAM segments **1630**, **1640**, respectively, from self-refresh mode to active mode. In certain embodiments, the first and second DRAM segments **1630**, **1640** maintain stored information but are not accessible when they are in self-refresh mode, and maintain stored information and are accessible when they are in active mode.

In certain embodiments, when the memory system **1010** is backing up the volatile memory system **1030**, data slices from only one of the two DRAM segments **1630**, **1640** at a time are sent to the controller **1062**. For example, when the first slice is being written to the controller **1062** during a back-up, the controller **1062** sends a signal via the CKe line **1636** to the first DRAM segment **1630** to put the first DRAM segment **1630** in active mode. In certain embodiments, the data slice from the first DRAM segment **1630** for multiple words (e.g., a block of words) is written to the controller **1062** before writing the second data slice from the second DRAM segment **1640** to the controller **1062**. While the first data slice is being written to the controller **1062**, the controller **1062** also sends a signal via the CKe line **1646** to put the second DRAM segment **1640** in self-refresh mode. Once the first data slice for one word or for a block of words is written to the controller **1062**, the controller **1062** puts the first DRAM segment **1630** into self-refresh mode by sending a signal via the CKe line **1636** to the first DRAM segment **1640**. The controller **1062** also puts the second DRAM segment **1640** into active mode by sending a signal via the CKe line **1646** to the DRAM segment **1640**. The second slice for a word or for a block of words is written to the controller **1062**. In certain embodiments, when the first and second data slices are written to the buffer in the controller **1062**, the controller **1062** combines the first and second data slices **1630**, **1640** into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem **1040**. In certain embodiments, this process is called "slicing" the volatile memory subsystem **1030**.

In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements **1042** write each backed-up data word to the controller **1062** which writes a first slice of the data word to the volatile memory subsystem **1030** and then a second slice of the data word to the volatile memory subsystem **1030**. In certain embodiments, slicing the volatile memory subsystem **1030** during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem **1030** during a backup operation.

FIG. **22** is a flowchart of an example method **1600** of controlling a memory system **1010** operatively coupled to a host system and which includes a volatile memory subsystem **1030** and a non-volatile memory subsystem **1040**. Although described with respect to the memory system **1010** described herein with respect to FIGS. **12-14** and **21**, the method **1600** is compatible with other memory systems. The method **1600** comprises communicating data words between the volatile memory subsystem **1030** and the host system when the memory system **1010** is in a first mode of operation in an operational block **1610**. For example, the memory system **1010** may be in the first mode of operation when no trigger condition has occurred and the memory system is not performing a backup and/or restore operation or is not being powered by a secondary power supply.

In an operational block **1620**, the method further comprises transferring data words from the volatile memory subsystem **1030** to the non-volatile memory subsystem **1040** when the memory system **1010** is in a second mode of operation. In certain embodiments, each data word comprises the data stored in a particular address of the memory system **1010**. The memory system **1010** may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first

portion (also referred to as a slice) of the data word in a buffer in an operational block **1622**, storing a second portion of the data word in the buffer in an operational block **1624**, and writing the entire data word from the buffer to the non-volatile memory subsystem **1040** in an operational block **1626**.

In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller **1062**. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller **1062** which comprises an FPGA. The method **1600** may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller **1062** and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).

In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.

In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements **1040** write each backed-up data word to the controller **1062** which writes a first portion of the data word to the volatile memory subsystem **1030** and then a second portion of the data word to the volatile memory **1030**. In certain embodiments, slicing the volatile memory subsystem **1030** during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem **1030** during a backup operation.

The method **1600** can advantageously provide significant power savings and can lead to other advantages. For example, in one embodiment where the volatile memory subsystem **1030** comprises DRAM elements, only the slice of the DRAM which is currently being accessed (e.g., written to the buffer) during a backup is configured in full-operational mode. The slice or slices that are not being accessed may be put in self-refresh mode. Because DRAM in self-refresh mode uses significantly less power than DRAM in full-operational mode, the method **1600** can allow significant power savings. In certain embodiments, each slice of the DRAM includes a separate self-refresh enable (e.g., CKe) signal which allows each slice to be accessed independently.

In addition, the connection between the DRAM elements and the controller **1062** may be as large as the largest slice instead of as large as the data bus. In the example embodiment, the connection between the controller **1062** and the DRAM may be 40 bits instead of 72 bits. As a result, pins on the controller **1062** may be used for other purposes or a smaller controller may be used due to the relatively low number of pin-outs used to connect to the volatile memory subsystem **1030**. In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem **1030** and the controller **1062** but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.

While embodiments and applications have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts disclosed herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

What is claimed is:

1. A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;

a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;

a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;

a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and

a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:

a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and

at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

2. The memory module of claim **1**, wherein the first and third buck converters are further configured to operate as a dual buck converter.

3. The memory module of claim **1**, wherein the first voltage amplitude is 1.8 volts.

4. The memory module of claim **1**, wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively.

5. The memory module of claim **1**, further comprising:

a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.

6. The memory module of claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage.

7. The memory module of claim 6, wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage.

8. The memory module of claim 1, the plurality of components further comprising:

one or more registers coupled to one of the first, second, third and fourth regulated voltages, the one or more registers configured to register, in response to a clock, the first plurality of address and control signals, wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on.

9. The memory module of claim 5, wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage.

10. The memory module of claim 5, the plurality of components further comprising:

a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information.

11. The memory module of claim 10, wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory.

12. The memory module of claim 5, the plurality of components further comprising:

a non-volatile memory; and

a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.

13. The memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit.

14. The memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.

15. The memory module of claim 1, the plurality of components further comprising:

a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information.

16. A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively;

a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage, wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively;

a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and

a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

17. The memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter.

18. The memory module of claim 16, the plurality of components further including:

a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal.

19. The memory module of claim 18, wherein the write operation includes writing data information into non-volatile memory.

20. The memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

21. The memory module of claim 16, the plurality of components further including:

at least one circuit coupled between the interface and the plurality of SDRAM devices, the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

22. The memory module of claim 16, the plurality of components further including:

a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element.

23. A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices, wherein a plu-

rality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections;

first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively; and

a converter circuit configured to provide the fourth regulated voltage,

wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on,

wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices, and

wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals.

24. The memory module of claim **23**, further comprising:

a voltage monitor circuit configured to monitor an input voltage received from the host system via the interface, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

25. The memory module of claim **24**, the plurality of components further including:

a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation.

26. The memory module of claim **25**, wherein the write operation includes writing data information to non-volatile memory.

27. The memory module of claim **24**, wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage.

28. The memory module of claim **23**, wherein the second and third buck converters are configured to operate as a dual buck converter.

29. The memory module of claim **23**, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

30. The memory module of claim **23**, wherein the first, second, and third buck converters are configured to receive a pre-regulated input voltage and to provide the first, second and third regulated voltages, respectively, and wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage.

* * * * *

Exhibit 4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.	CONF. NO: 6552
APPLICATION NO: 17/328,019	ART UNIT: 2135
FILING DATE: 05/24/2021	EXAMINER: HASHEM FARROKH

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

AMENDMENT AND RESPONSE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Non-Final Office Action dated September 27, 2021, making a response due on or before December 27, 2021. Accordingly, this paper is timely filed.

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 9 of this paper.

A Conclusion appears at page 13 of this paper.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Currently Amended) A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;

a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and a first circuit that is coupled to the plurality of ~~synchronous dynamic random access memory (~~SDRAM~~)~~ devices and to a first set of edge connections of the plurality of edge connections, wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.

3. (Previously presented) The memory module of claim 2, wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude; and wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes.

4. (Previously presented) The memory module of claim 2, wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts.

5. (Currently Amended) The memory module of claim 2, further comprising:
a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal ~~the predetermined threshold voltage is ten percent below a specified operating voltage~~.

6. (Currently Amended) The memory module of claim 2, further comprising:
a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal ~~the predetermined threshold voltage is ten percent above a specified operating voltage~~.

7. (Previously presented) The memory module of claim 2, further comprising:
a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections, wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller.

8. (Currently Amended) The memory module of claim 7, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage, and wherein the first predetermined threshold voltage is above a specified operating voltage.

9. (Currently Amended) The memory module of claim 8, wherein the first predetermined threshold voltage is ten percent above the specified operating voltage.

10. (Currently Amended) The memory module of claim [[7]]8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage, ~~and~~wherein the second predetermined threshold voltage is below ~~a~~ the specified operating voltage, and wherein the memory module transitions from a first operable state to a second operable state in response to the signal.

11. (Currently Amended) The memory module of claim 10, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage.

12. (Previously presented) The memory module of claim 7, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage.

13. (Previously presented) The memory module of claim 7, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system.

14. (Canceled)

15. (Currently Amended) The memory module of claim [[14]]2, wherein two of the at least three buck converters are configured to operate as a dual-buck converter.

16. (Currently Amended) A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;

a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory

(SDRAM) devices, the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages; and

a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage, wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.

17. (Currently Amended) The memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage~~, and wherein the first predetermined threshold voltage is ten percent above a specified operating voltage, and the second predetermined threshold voltage is ten percent below the specified operating voltage~~.

18. (Previously presented) The memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.

19. (Previously presented) The memory module of claim 18, wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit, and wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit.

20. (Previously presented) The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.

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21. (Previously presented) The memory module of claim 16, further comprising:

a first circuit having a first input, a second input and an output, the first input coupled to a first pre-regulated voltage, the second input coupled to a second pre-regulated voltage, the output coupled to the voltage conversion circuit, wherein the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a supply voltage, wherein, in the first operable state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the first pre-regulated voltage, and wherein, in the second state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the second pre-regulated voltage.

22. (Previously presented) The memory module of claim 21, wherein the first circuit includes a first diode coupled between the first input and the output and a second diode coupled between the second input and the output.

23. (Currently Amended) A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;

a voltage conversion circuit configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages; and

a controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface of the PCB, the voltage monitor circuit configured to monitor the input voltage, wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and wherein the one or more operations include a write operation to transfer data into non-volatile memory.

24. (Currently Amended) The memory module of claim 23, wherein, in response to

the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state ~~of operation of operation~~ to a second operable state ~~of operation of operation~~.

25. (Currently Amended) The memory module of claim 24, wherein, in the first operable state ~~of operation of operation~~, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and wherein, in the second operable state ~~of operation of operation~~, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.

26. (Currently Amended) The memory module of claim 23, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage or below a second predetermined threshold voltage.

27. (Currently Amended) The memory module of claim 26, wherein the first predetermined threshold voltage is ~~ten percent ten percent~~ above a specified operating voltage, and the second predetermined threshold voltage is below the specified operating voltage.

28 - 29. (Canceled)

30. (Previously presented) The memory module of claim 25, wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via a first diode.

31. (Previously presented) The memory module of claim 30, wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via a second diode.

32. (New) The memory module of claim 5, further comprising:

a controller coupled to the voltage monitor circuit; wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

33. (New) The memory module of claim 6, further comprising:

a controller coupled to the voltage monitor circuit; wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

34. (New) The memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

REMARKS

The Non-Final Office Action issued September 27, 2021, has been carefully considered.

Reconsideration in view of the following remarks is respectfully requested.

Claims 2, 5-6, 8-11, 15-17, 23-27 have been amended, and claims 32-34 have been added.

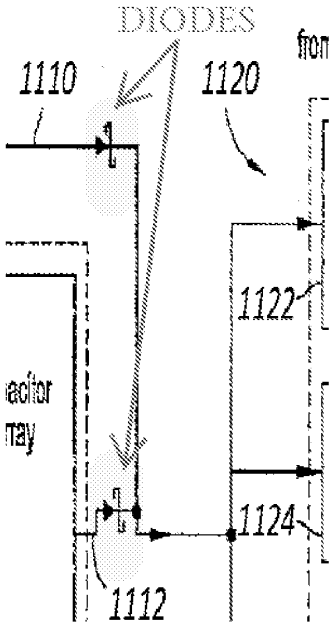
Claim Interpretation

Applicant acknowledges that the Examiner is not interpreting the claims under 35 USC 112(f), or under pre-AIA paragraph six.

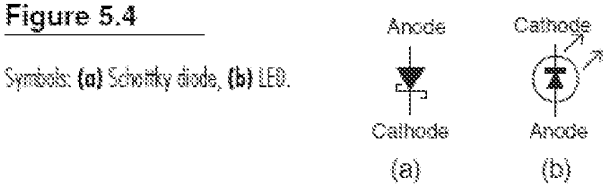
Rejection under 35 USC 112

Claims 20, 22, and 30-31 stand rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-A/A), first paragraph, as allegedly failing to comply with the written description requirement. According to the Office Action, the "claimed specification does not appear to describe or support" the claimed first and second diodes.

Applicant respectfully disagrees, and directs the Examiner's attention to FIG. 16, and specifically to the symbols therein highlighted below, which represent diodes as is known in the electrical arts.



Referring for example to Chapter 5 of the Practical Electronics Handbook, Sixth Edition, 2007, it illustrates, in FIG. 5.4, a Schottky diode as follows:



It will be appreciated that the symbols highlighted in FIG. 16 are identical to those in the Practical Electronics Handbook that are used to represent a Schottky diode, and the drawings therefore illustrate the claimed diodes. Namely, in FIG. 16, and consistently with the claims, one diode is depicted having an input coupled to a pre-regulated fourth voltage 1110 from first power conversion element 1130 and an output coupled to voltage conversion element 1120; and another diode is depicted having an input coupled to a pre-regulated fifth voltage 1112 from second power element 1140 and an output coupled to voltage conversion element 1120.[1] The MPEP states that the fundamental inquiry behind compliance with the written description requirement (under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-A/A), first paragraph) "is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed. See, e.g., *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991)."[2] The MPEP then explains that "An applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, **figures**, **diagrams**, and formulas that fully set forth the claimed invention. (Relying on *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997), emphasis added).[3]

For these reasons at least, Applicant respectfully maintains that claims 20, 22, and 30-31 are in compliance with 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-A/A), first paragraph, and the rejection should be withdrawn.

Double Patenting

Timely submitted herewith is a Terminal Disclaimer over U.S. Patent No. 11,016,918 overcoming the alleged non-statutory double patenting rejection of claims 2-15, 23, and 26 -29.

Newly-Added Claims

Claims 32-34 have been added to further particularly point out and distinctly claim the subject matter of the claimed arrangement.

[1] See parenthetical clause at end of paragraph [00146] expressly characterizing the voltages 1110 and 1112 as "pre-regulated."
[2] MPEP 2163.02 Standard for Determining Compliance With the Written Description Requirement
[3] *Id.*

Comments on the Statement of Reasons for the Indication of Allowable Subject Matter

Applicant gratefully acknowledges the indication that claims 16-19 are 21 are allowed and that claim 24-25 contain allowable subject matter. Of these allowed and allowable claims, claims 16-17 and 24-25 have been amended, and Applicant respectfully maintains that they continue to be allowable at least for the reasons cited by the Examiner. Further, pursuant to 37 C.F.R. § 1.104, Applicant respectfully submits the instant statement commenting on the Examiner's reasons for allowance.

Applicant maintains that additional and/or alternative reasons for allowance may exist apart from those expressed by the Examiner and the Applicant, and these reasons may be independently sufficient to establish the patentability of each of the allowed dependent or independent claims.

Applicant respectfully reserves the right to introduce, articulate, or otherwise comment on any such additional reasons for allowance as may be appropriate in any future proceedings concerning the one or more claimed embodiments.

To the extent that the Examiner's reasons for allowance are inconsistent with applicable case law, statutes, and regulations, Applicant respectfully disagrees with them. Furthermore, Applicant does not admit to any characterization or limitation of the claims or to any characterization of a reference by the Examiner, particularly any that are inconsistent with the language of the claims considered in their entirety and including all of their constituent limitations.

Conclusion

In view of the foregoing, Applicant submits that the application is in condition for immediate allowance. Early notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned attorney if it is believed that such contact will expedite the prosecution of the application.

In the event this paper is not timely filed, Applicant petitions for an appropriate extension of time. Please charge any fee deficiency or credit any overpayment to Deposit Account No. 22-0585.

Respectfully submitted,

VORYS, SATER, SEYMOUR and PEASE LLP

/Khaled Shami/
Khaled Shami, Registration No. 38745
Customer No.: 151145

Date: November 19, 2021

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NOTICE OF ALLOWANCE AND FEE(S) DUE

151145 7590 12/10/2021

Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
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Washington, DC 20006-1152

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 12/10/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/328,019	05/24/2021	Chi-She Chen	022955-000047	6552

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	03/10/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
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By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

151145 7590 12/10/2021
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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/328,019	05/24/2021	Chi-She Chen	022955-000047	6552

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	03/10/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2135	711-110000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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Ex. 1044, p. 195

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151145 7590 12/10/2021

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9th Floor
Washington, DC 20006-1152

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 12/10/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	**Application No.** 17/328,019	**Applicant(s)** Chen et al.	
	Examiner HASHEM FARROKH	**Art Unit** 2135	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 11/199/2021.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 2-13,15-27 and 30-34 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 11/22/2021.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

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Exhibit 5

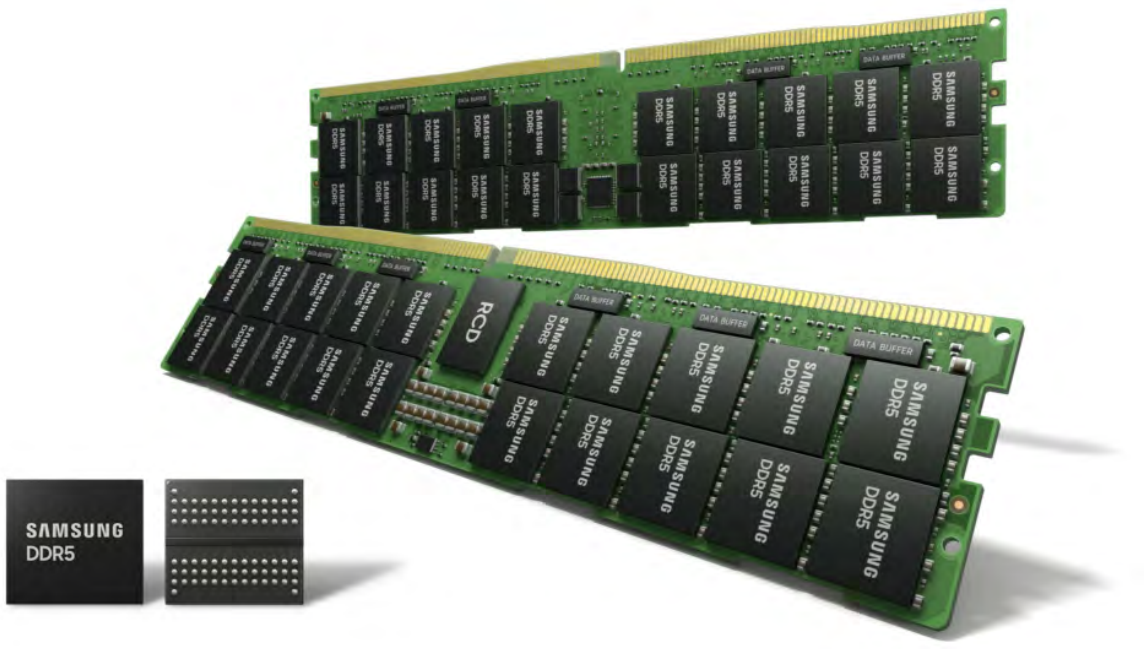
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Samsung Starts Mass Production of Most Advanced 14nm EUV DDR5 DRAM

Korea on October 12, 2021

Samsung's new five-layer EUV process enables the industry's highest DRAM bit density, enhancing productivity by approximately 20%

Based on the latest DDR5 standard, Samsung's 14nm DRAM will be ideal for handling ever-growing AI and 5G workloads



Samsung Electronics, the world leader in advanced memory technology,

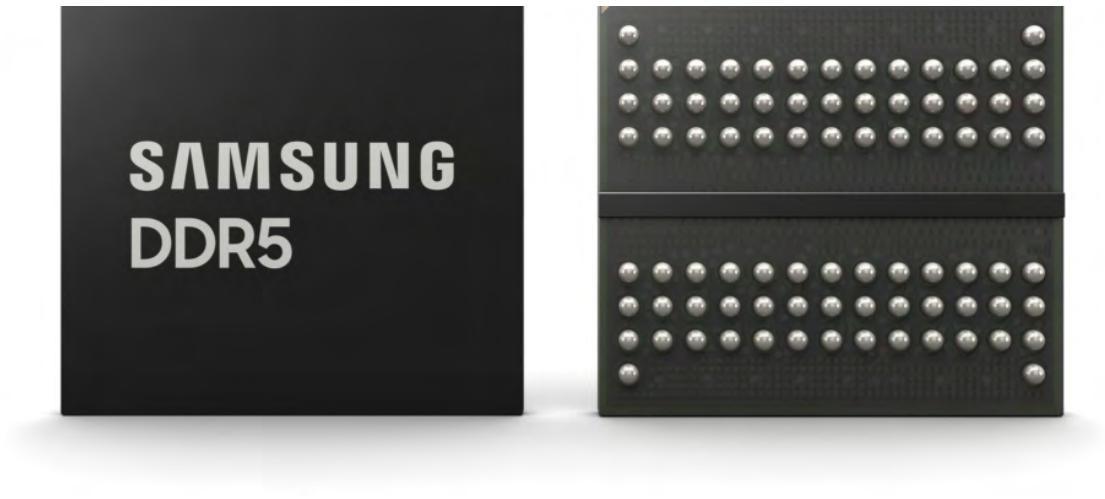
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of last year, Samsung has increased the number of EUV layers to five to deliver today's finest, most advanced DRAM process for its DDR5 solutions.

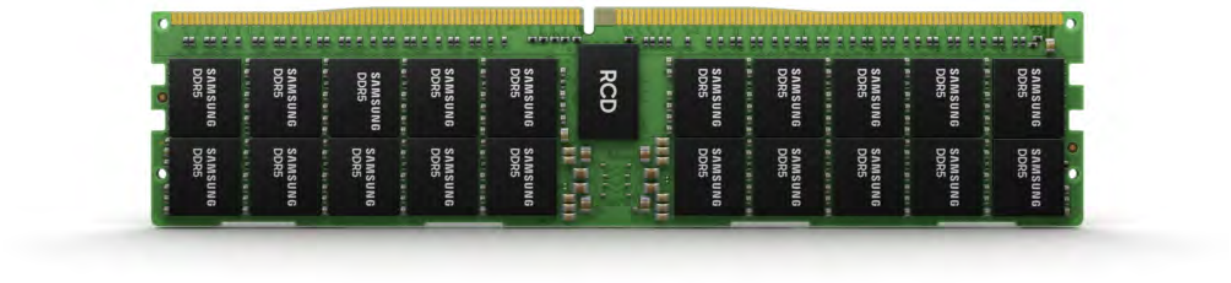
"We have led the DRAM market for nearly three decades by pioneering key patterning technology innovations," said Jooyoung Lee, Senior Vice President and Head of DRAM Product & Technology at Samsung Electronics. "Today, Samsung is setting another technology milestone with multi-layer EUV that has enabled extreme miniaturization at 14nm — a feat not possible with the conventional argon fluoride (ArF) process. Building on this advancement, we will continue to provide the most differentiated memory solutions by fully addressing the need for greater performance and capacity in the data-driven world of 5G, AI and the metaverse."

As DRAM continues to scale down the 10nm-range, EUV technology becomes increasingly important to improve patterning accuracy for higher performance and greater yields. By applying five EUV layers to its 14nm DRAM, Samsung has achieved the highest bit density while enhancing the overall wafer productivity by approximately 20%. Additionally, the 14nm process can help bring down power consumption by nearly 20% compared to the previous-generation DRAM node.

Samsung
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Leveraging the latest DDR5 standard, Samsung's 14nm DRAM will help unlock unprecedented speeds of up to 7.2 gigabits per second (Gbps), which is more than twice the DDR4 speed of up to 3.2Gbps.



Samsung plans to expand its 14nm DDR5 portfolio to support data center, supercomputer and enterprise server applications. Also, Samsung expects to grow its 14nm DRAM chip density to 24Gb in better meeting the rapidly growing data demands of global IT systems.

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Proven DRAM module solution in the global market

Samsung's memory modules are designed for a wide range of applications to deliver the best performance with low power requirements.

RDIMM

Registered DIMM

- Include a register for enhancing clock, command and control signals
- Error correction available by added 8 bit parity signals
- Supports x4 / x8 Organization / up to 2 ranks per DIMM and 3DPC configuration
- Application : Server





LRDIMM

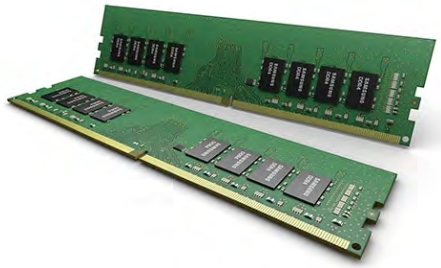
Load Reduced DIMM

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

UDIMM

Unbuffered DIMM

- No buffer or register : smaller latency value
- Supports x8 / x16 Organization / up to 2 ranks per DIMM and 2DPC configuration
- Application : Desktop



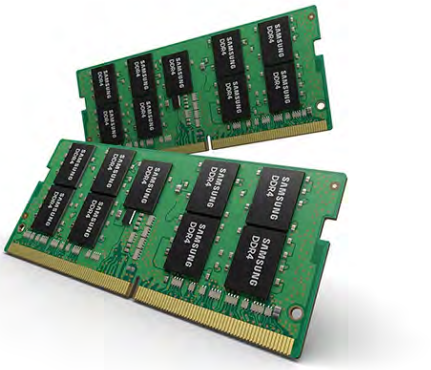


SODIMM

Small Outline DIMM

- Smaller than normal DIMMs
- Supports x8 / x16 / up to 2 ranks per DIMM and 2DPC configuration
- For systems with limited space issues
- Application : Laptop

ECC UDIMM / ECC SODIMM



Error Correction Code UDIMM / SODIMM

- Single error correction and detection available
- Supports x8 up to 2 ranks per DIMM
- Application : High-end desktop, High-end laptop, Server

Product selector

DDR	Dimm Type	Density	Rank x

Part Number	DDR	Dimm Type	Density
M378A1G44AB0-CWE	DDR4	UDIMM	8 GB
M378A1K43CB2-CPB	DDR4	UDIMM	8 GB
M378A1K43CB2-CRC	DDR4	UDIMM	8 GB
M378A1K43CB2-CTD	DDR4	UDIMM	8 GB
M378A1K43DB2-CTD	DDR4	UDIMM	8 GB
M378A1K43DB2-CVF	DDR4	UDIMM	8 GB
M378A2G43AB3-CWE	DDR4	UDIMM	16 GB
M378A2K43CB1-CPB	DDR4	UDIMM	16 GB
M378A2K43CB1-CRC	DDR4	UDIMM	16 GB
M378A2K43CB1-CTD	DDR4	UDIMM	16 GB

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Server & Network



PC

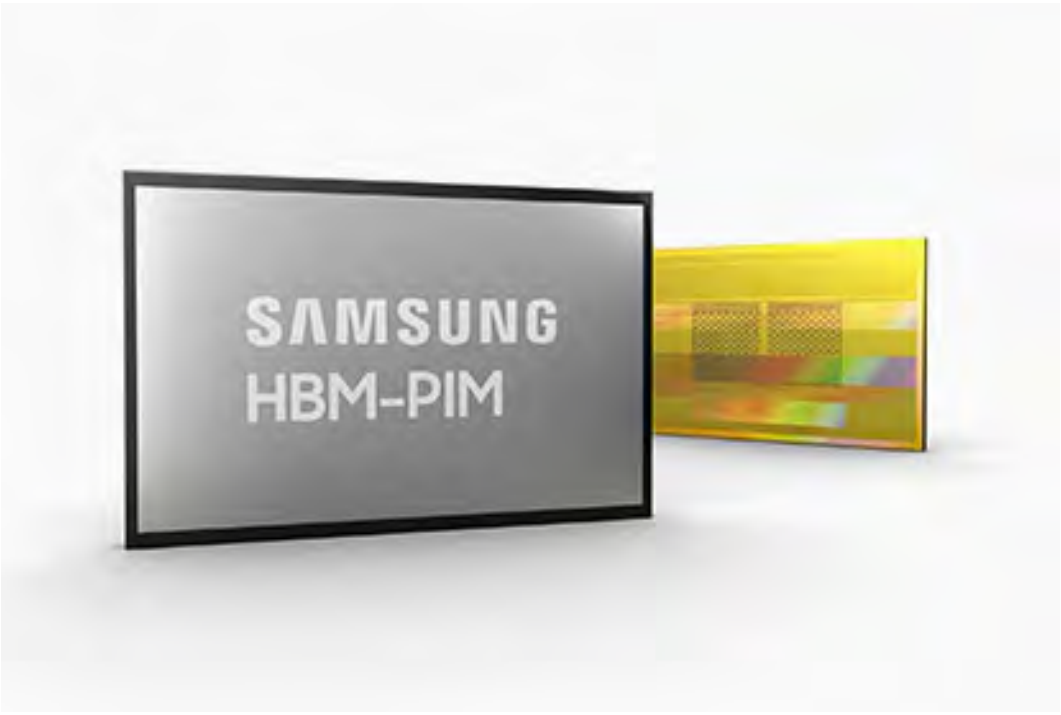
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Integration of HBM-PIM with the Xilinx Alveo AI accelerator system will boost overall system performance by 2.5X while reducing energy consumption by more than 60%

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All product specifications reflect internal test results and are subject to variations by user's system configuration. All product images shown are for illustration purposes only and may not be an exact representation of the product. Samsung reserves the right to change product images and specifications at any time without notice.

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Exhibit 7

288pin Load Reduced DIMM based on 8Gb B-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

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Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	- First SPEC release	25th Jan. 2016	-	J.Y.Lee
1.1	- Change of Electrical Characterisitics and AC timing page 28~32	7th Mar. 2016	-	J.Y.Lee
1.2	- Deletion of DDR4-2400(19-17-17)	5th Jul. 2016	-	J.Y.Lee
	- Correction of typo			
1.3	- Addition of DDR4-2666	5th Sep. 2016	-	J.Y.Lee
1.4	- Addition of IDD value (DDR4-2666)	21th Oct. 2016	-	J.Y.Lee
1.5	- Addition of Electrical Characteristics & AC Timings for DDR4-1600-3DS to DDR4-2666-3DS on page 29~30	18th Jan. 2017	-	J.Y.Lee
	- Update referring to JEDEC DDR4 datasheet rev.79-4B			
1.6	- Update Physical Dimension. 1. Add PCB hole. 2. Change Heat spread shape. 3. Change Module height information. 4. Change module edge shape to curved line.	9th Jun, 2017	Final	J.Y.Bae

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1. DDR4 Load Reduced DIMM Ordering Information

Part Number[2]	Density	Organization	Component Composition[1]	Number of Rank	Height
M386AAK40B40-CRB/UC/WD	128GB	16Gx72	4H TSV 8Gx4(K4ABG045WB-4C##)*36	8 (2 physical ranks / 4 logical ranks)	31.25mm

NOTE :
1. "##" - RB(2133Mbps 17-15-15)/UC(2400Mbps 20-18-18)/WD(2666Mbps 22-19-19)
2. RB(2133Mbps 17-15-15)/UC(2400Mbps 20-18-18)/WD(2666Mbps 22-19-19)
   - DDR4-2666(22-19-19) are backward compatible to DDR4-2400(20-18-18), DDR4-2133(17-15-15)

2. Key Features

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Unit
	13-12-11	15-14-13	17-15-15	20-18-18	22-19-19	
tCK(min)	1.25	1.071	0.937	0.833	0.750	ns
CAS Latency	13	15	17	20	22	nCK
tRCD(min)	15	15	14.06	15	14.25	ns
tRP(min)	13.75	13.92	14.06	15	14.25	ns
tRAS(min)	35	34	33	32	32	ns
tRC(min)	48.75	47.92	47.06	47	46.25	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin,1200MHz f_{CK} for 2400Mb/sec/pin, 1333MHzf_{CK} for 2666Mb/sec/pin
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 10,11,12,13,14,15,16,17,18,19,20,21,22
- Programmable Additive Latency (Posted CAS) : 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600) , 10,12 (DDR4-1866) , 11,14 (DDR4-2133) ,12,16 (DDR4-2400) and 14,18 (DDR4-2666)
- Burst Length: 8 , 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset

3. Address Configuration

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
8Gx4(32Gb 4H TSV) based Module	A0-A16	A0-A9	BG0-BG1	BA0-BA1	A10/AP

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4. Load Reduced DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	NC	145	NC	40	DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	DQS15_c	266	DQS6_c
7	DQS9_t	151	VSS	46	VSS	190	DQ27	84	CS0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	DQS17_t	195	VSS	89	CS1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n	237	CS3_n,C1	132	DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	DQS16_c	277	DQS7_c
18	DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

NOTE:
1. VPP is 2.5V DC
2. Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.
3. Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4. The 5th VPP is required on all modules. DIMMs.

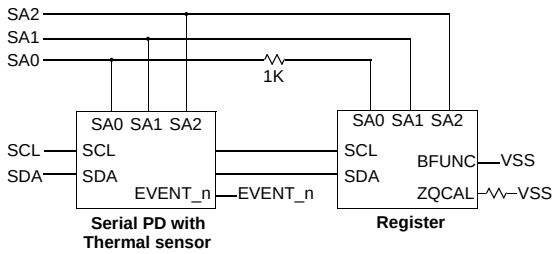
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5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A17[1]	SDRAM address input	SCL	I2C serial bus clock for SPD-TSE
BA0, BA1	SDRAM bank select	SDA	I2C serial bus data line for SPD-TSE
BG0, BG1	SDRAM bank group select	SA0–SA2	I2C slave address select for SPD-TSE
RAS_n[2]	SDRAM row address strobe	PAR	SDRAM parity input
CAS_n[3]	SDRAM column address strobe	VDD	SDRAM core power supply
WE_n[4]	SDRAM write enable	C0, C1, C2	Chip ID lines for 3DS SDRAMs
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	SDRAM clock enable lines	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines	VDDSPD	Serial SPD-TSE positive power supply
ACT_n	Register input for activate	ALERT_n	SDRAM ALERT_n
DQ0–DQ63	DIMM memory data bus	VPP	SDRAM Supply
CB0–CB7	DIMM ECC check bits	RESET_n	Set DRAMs to a Known State
DQS0_t–DQS17_t	SDRAM data strobes (positive line of differential pair)	EVENT_n	SPD-TSE signals a thermal event has occurred.
DQS0_c–DQS17_c	SDRAM data strobes (negative line of differential pair)	VTT	SDRAM I/O termination supply
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	RFU	Reserved for future use
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

6. ON DIMM Thermal Sensor



NOTE : 1. All Samsung RDIMM support Thermal sensor on DIMM

[Table 1] Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

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7. Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers,excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2, 4, 8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS0_t-DQS17_t DQS0_c- DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW

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Symbol	Type	Function
ALERT_n	Output	ALERT: It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Whether ALERT_n is used or not is system dependent.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		No Connect: No on DIMM electrical connection is present.
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VTT	Supply	Power Supply for termination of Address, Command and Control, VDD/2
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VDDSPD	Supply	Power supply used to power the I2C bus on the SPE-TSE and register.
VREFCA	Supply	Reference voltage for CA

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8. Registering Clock Driver Specification

8.1 Timing & Capacitance Values

Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400/2666		Units	Notes
			Min	Max	Min	Max		
fclock	Input Clock Frequency	application frequency	625	1080	625	1350	MHz	
t_{CH}/t_{CL}	Pulse duration, CK_t, CK_c HIGH or LOW		0.4	-	0.4	-	t_{CK}	
t_{ACT}	Inputs active time4 before DRST_n is taken HIGH	DCKE0/1 = LOW and DCS0/1_n = HIGH	16	-	16	-	t_{CK}	
t_{PDM}	Propagation delay, single-bit switching, CK_t/ CK_c to output	1.2V Operation	1	1.3	1	1.3	ns	
t_{DIS}	output disable time	Rising edge of Yn_t to output float	0.5*tCK + tQSK1(min)	-	0.5*tCK + tQSK1(min)	-	ps	
t_{EN}	output enable time	Output valid to rising edge of Yn_t	0.5*tCK - tQSK1(max)	-	0.5*tCK - tQSK1(max)	-	ps	
C_I	Input capacitance, Data inputs	NOTE[1,2]	0.8	1.1	0.8	1.0	pF	
C_{CK}	Input capacitance, CK_t, CK_c	NOTE[1,2]	0.8	1.1	0.8	1.0		
C_{IR}	Input capacitance, DRST_n	$V_I=V_{DD}$ or V_{SS} ; V_{DD}=1.2V	0.5	2.0	0.5	2.0		

Note:
1. This parameter does not include package capacitance
2. Data inputs are DCKE0/1, DODT0/1, DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DC0..DC2, DPAR, DCS0/1_n

8.2 Clock Driver Characteristics

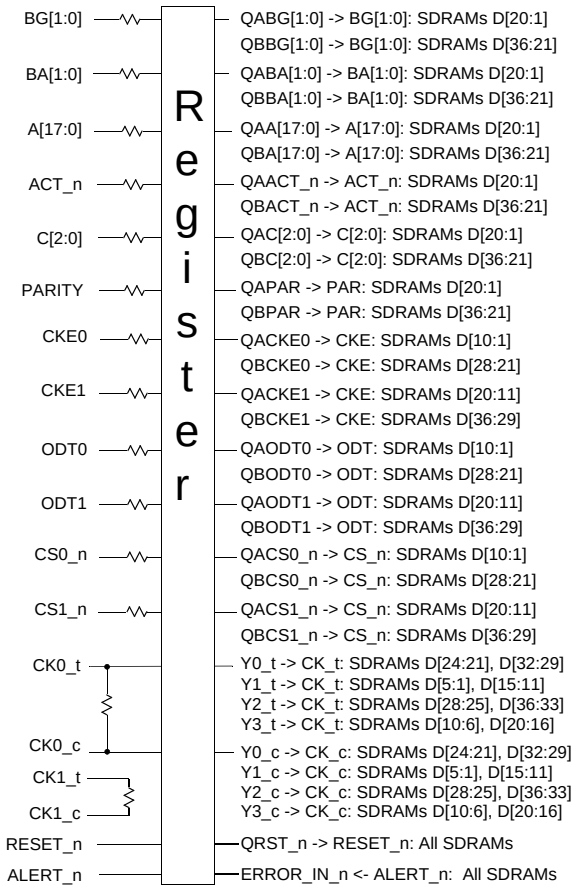
Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		Units	Notes
			Min	Max	Min	Max	Min	Max		
t_{jit} (cc)	Cycle-to-cycle period jitter	CK_t/CK_c stable	0	0.025 x tCK	0	0.025 x tCK	0	0.025 x tCK	ps	
t_{STAB}	Stabilization time		-	5	-	5	-	5	us	
t_{CKsk}	Clock Output skew		-	10	-	10	-	10	ps	
t_{jit}(per)	Yn Clock Period jitter		-0.025 * tCK	0.025 * tCK	-0.025 * tCK	0.025 * tCK	-0.025 * tCK	0.025 * tCK	ps	
t_{jit}(hper)	Half period jitter		-0.032 * tCK	0.032 * tCK	-0.032 * tCK	0.032 * tCK	-0.032 * tCK	0.032 * tCK	ps	
t_{Qsk1}	Qn Output to clock tolerance		-0.125 * tCK	0.125 * tCK	-0.125 * tCK	0.125 * tCK	-0.1 * tCK	0.1 * tCK	ps	
t_{dynoff}	Maximum re-driven dynamic clock off-set		-	50	-	45	-	45	ps	

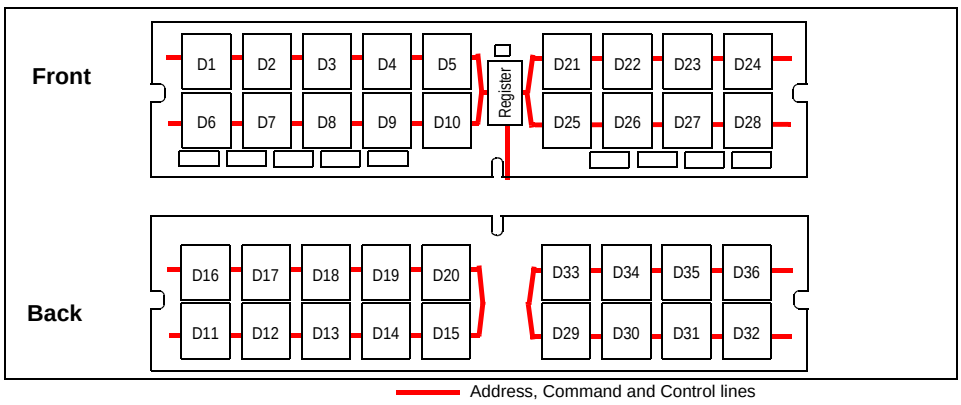
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9. Function Block Diagram:

9.1 128GB, 16Gx72 Module

(Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAMs)



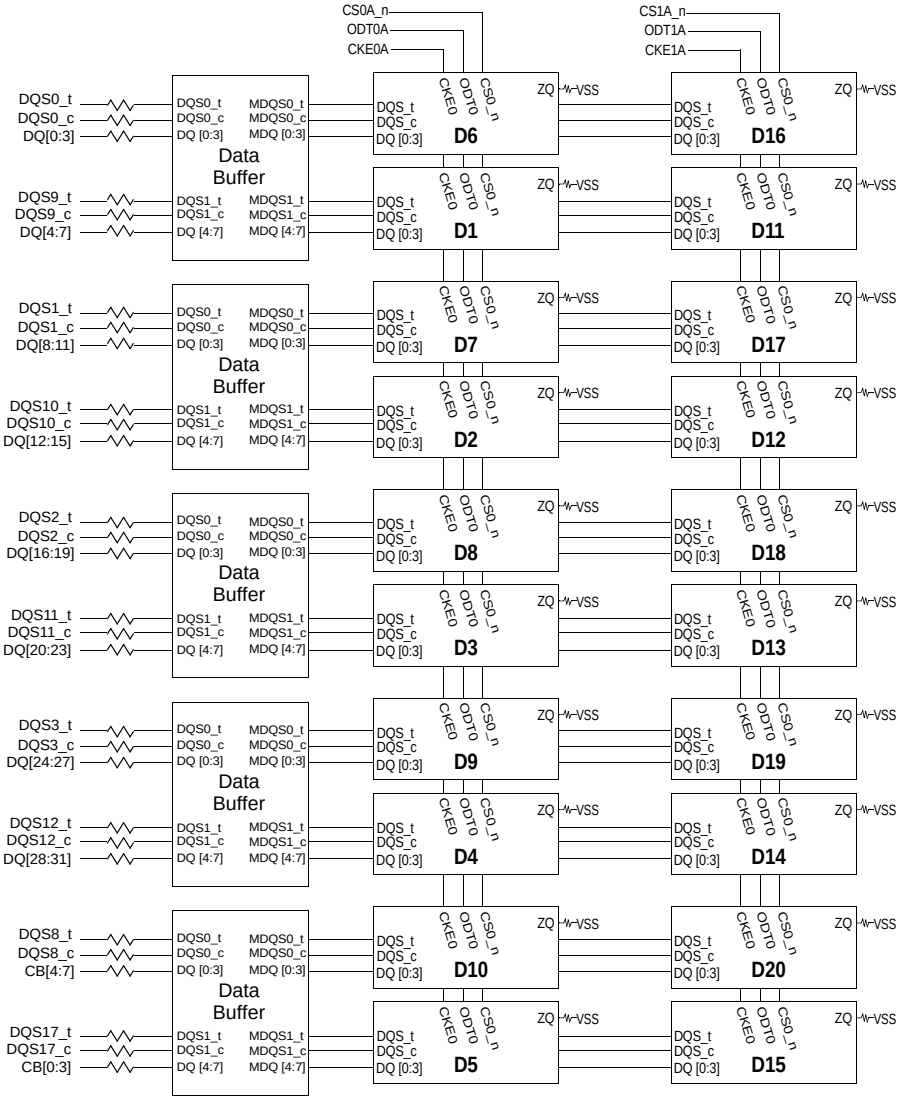


NOTE :

1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

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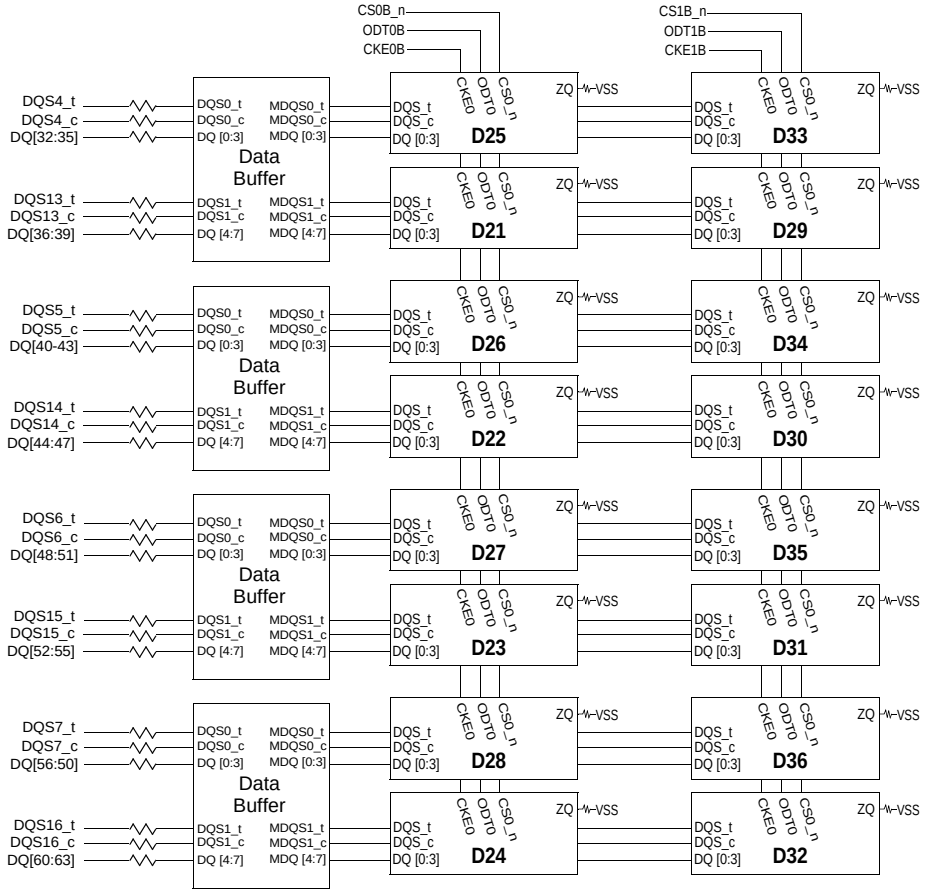


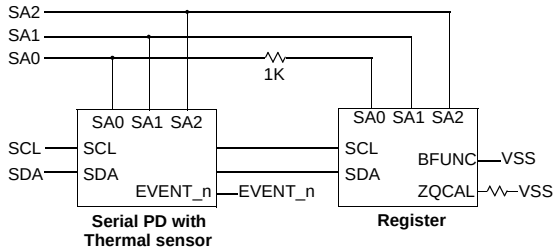
NOTE :

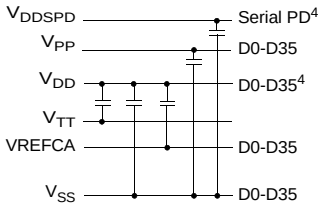
1. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. TEN pin of SDRAMs is tied to VSS.

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NOTE :

1. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. TEN pin of SDRAMs is tied to VSS.
4. VDDSPD is also applied to the register. VDD is also applied to the register and the data buffers.

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10. Absolute Maximum Ratings

10.1 Absolute Maximum DC Ratings

[Table 2] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA to Vss	-0.3 ~ 1.5	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

11. AC & DC Operating Conditions

11.1 Recommended DC Operating Conditions

[Table 3] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP		2.375	2.5	2.75	V	3

NOTE:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. DC bandwidth is limited to 20MHz.

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12. AC & DC Input Measurement Levels

12.1 AC & DC Logic input levels for single-ended signals

[Table 4] Single-ended AC & DC input levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666		Unit	NOTE
		Min.	Max.	Min.	Max.		
$V_{IH.CA}$(DC75)	DC input logic high	V_{REFCA}+ 0.075	V_{DD}	TBD	TBD	V	
$V_{IL.CA}$(DC75)	DC input logic low	V_{SS}	V_{REFCA}-0.075	TBD	TBD	V	
$V_{IH.CA}$(AC100)	AC input logic high	V_{REF} + 0.1	Note 2	TBD	TBD	V	1
$V_{IL.CA}$(AC100)	AC input logic low	Note 2	V_{REF} - 0.1	TBD	TBD	V	1
V_{REFCA}(DC)	Reference Voltage for ADD, CMD inputs	0.49*V_{DD}	0.51*V_{DD}	TBD	TBD	V	2,3

NOTE :
1. See “Overshoot and Undershoot Specifications” on section.
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)
3. For reference : approx. VDD/2 ± 12mV

12.2 AC and DC Input Measurement Levels : V_{REF} Tolerances.

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 1. It shows a valid reference voltage V_{REF}(t) as a function of time. (V_{REF} stands for V_{REFCA}).

V_{REF}(DC) is the linear average of V_{REF}(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore V_{REF}(t) may temporarily deviate from V_{REF}(DC) by no more than ± 1% V_{DD}.

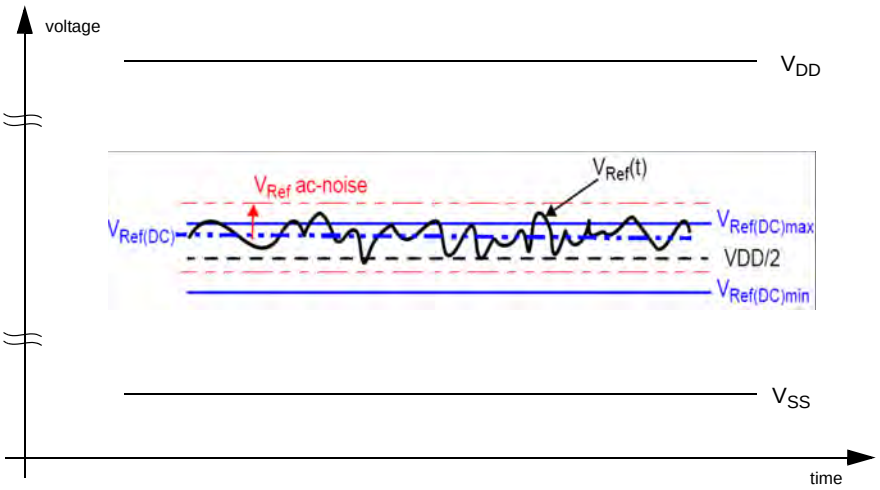


Figure 1. Illustration of V_{REF}(DC) tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{REF}.

"V_{REF}" shall be understood as V_{REF}(DC), as defined in Figure 1.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF}(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

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12.3 AC and DC Logic Input Levels for Differential Signals

12.3.1 Differential Signals Definition

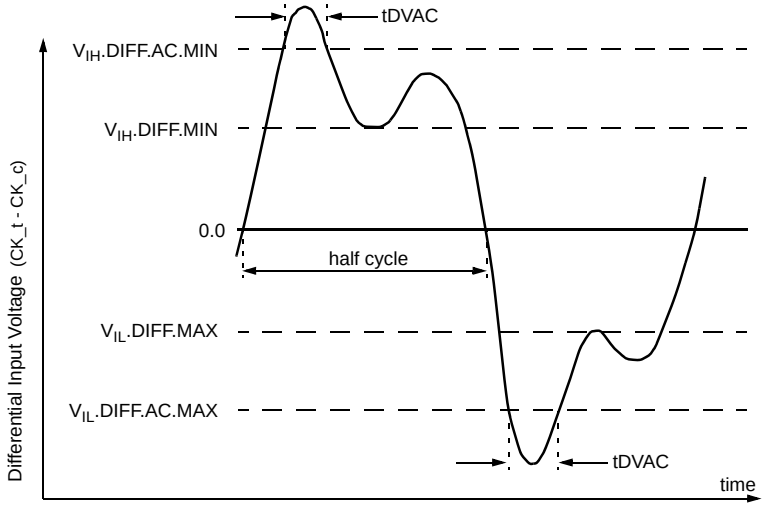


Figure 2. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

NOTE :
1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

12.3.2 Differential swing requirements for clock (CK_t - CK_c)

[Table 5] Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		DDR4 -2400/2666		unit	NOTE
		min	max	min	max		
V_{IHdiff}	differential input high	+0.150	NOTE 3	TBD	NOTE 3	V	1
V_{ILdiff}	differential input low	NOTE 3	-0.150	NOTE 3	TBD	V	1
V_{IHdiff}(AC)	differential input high ac	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2
V_{ILdiff}(AC)	differential input low ac	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	V	2

NOTE:
1. Used to define a differential signal slew-rate.
2. for CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD and V_{REFCA};
3. These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

[Table 6] Allowed time before ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	tDVAC [ps] @ |$V_{IH/Ldiff}$(AC)| = 200mV		tDVAC [ps] @ |$V_{IH/Ldiff}$(AC)| = TBDmV	
	min	max	min	max
> 4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
< 1.0	80	-	TBD	-

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12.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH.CA(AC) / VIL.CA(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than VIH.CA(AC100)/VIL.CA(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c

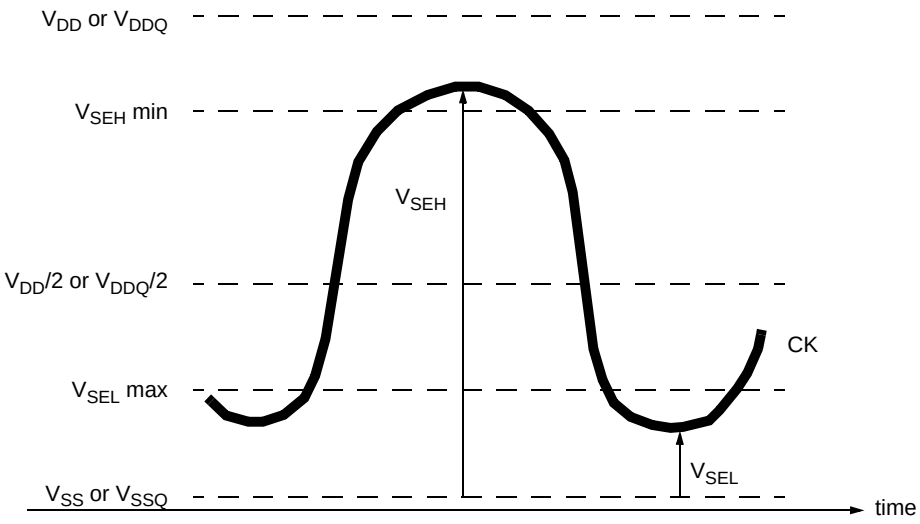


Figure 3. Single-ended requirement for differential signals.

Note that, while ADD/CMD signal requirements are with respect to VrefCA, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 7] Single-ended levels for CK_t, CK_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		Unit	NOTE
		Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK_t , CK_c	(VDD/2)+0.100	NOTE3	TBD	NOTE3	V	1, 2
V_{SEL}	Single-ended low-level for CK_t , CK_c	NOTE3	(VDD/2)-0.100	NOTE3	TBD	V	1, 2

NOTE :

1. For CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD;
2. V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};
3. These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

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12.4 Slew Rate Definitions

12.4.1 Slew Rate Definitions for Differential Input Signals (CK)

[Table 8] Differential Input Slew Rate Definition

Description	from	to	Defined by
Differential input slew rate for rising edge(CK_t - CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTRdiff
Differential input slew rate for falling edge(CK_t - CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTFdiff
NOTE: The differential signal (i,e.,CK_t - CK_c) must be linear between these thresholds.			

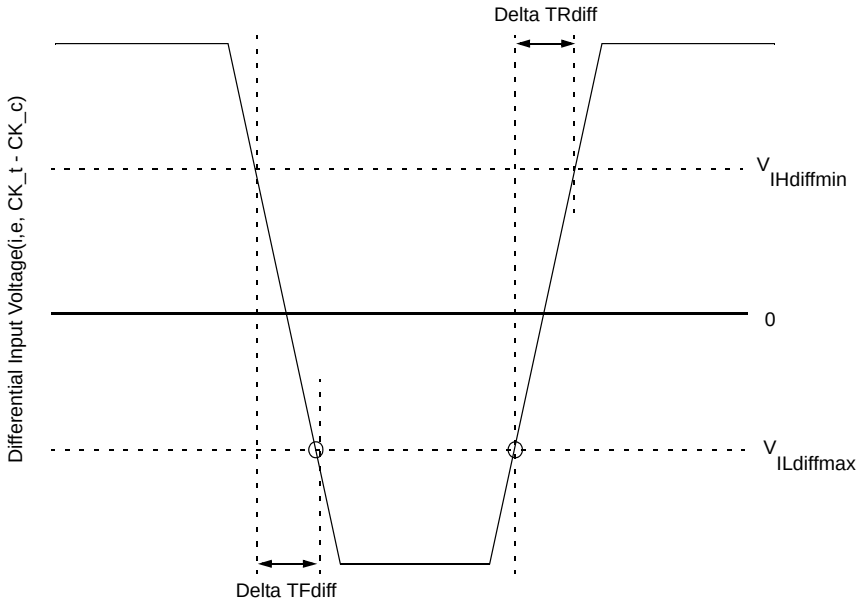


Figure 4. Differential Input Slew Rate Definition for CK_t, CK_c

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12.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 9. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

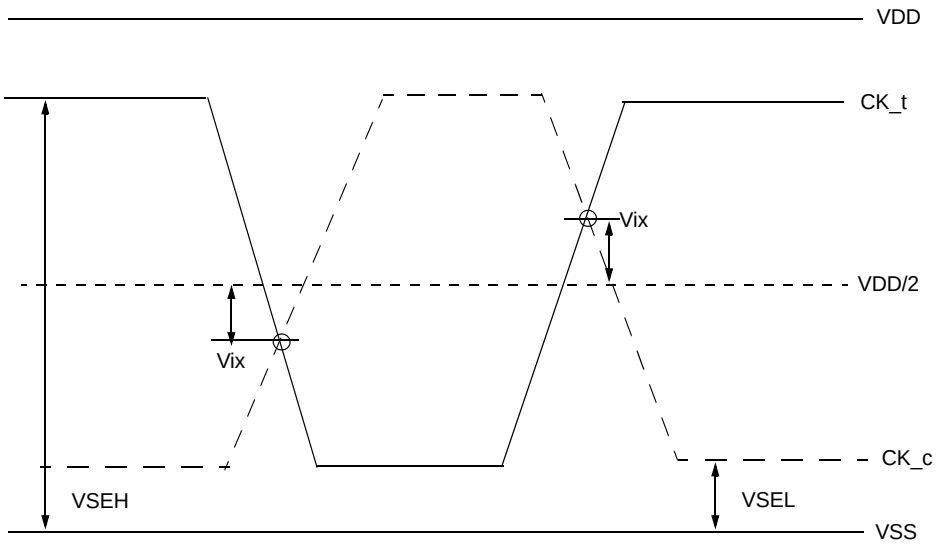


Figure 5. Vix Definition (CK)

[Table 9] Cross point voltage for differential input signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133			
		min		max	
-	Area of VSEH, VSEL	VSEL =< VDD/2 - 145mV	VDD/2 - 145mV =< VSEL =< VDD/2 - 100mV	VDD/2 + 100mV =< VSEH =< VDD/2 + 145mV	VDD/2 + 145mV =< VSEH
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120mV	-(VDD/2 - VSEL) + 25mV	(VSEH - VDD/2) - 25mV	120mV

Symbol	Parameter	DDR4-2400/2666			
		min		max	
-	Area of VSEH, VSEL	TBD	TBD	TBD	TBD
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	TBD	TBD	TBD	TBD

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12.6 Single-ended AC & DC Output Levels

[Table 10] Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Units	NOTE
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x V_{DDQ}	V	1

NOTE :
1. The swing of ± 0.15 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ}.

12.7 Differential AC & DC Output Levels

[Table 11] Differential AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Units	NOTE
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.3 x V_{DDQ}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 x V_{DDQ}	V	1

NOTE :
1. The swing of ± 0.3 × V_{DDQ} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ} at each of the differential outputs.

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12.8 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 12 and Figure 6.

[Table 12] Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TFse

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

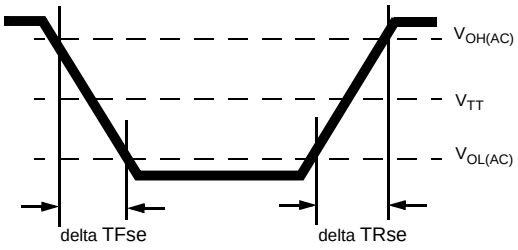


Figure 6. Single-ended Output Slew Rate Definition

[Table 13] Single-ended output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

NOTE :
1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

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12.9 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 14 and Figure 7.

[Table 14] Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TRdiff
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TFdiff

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

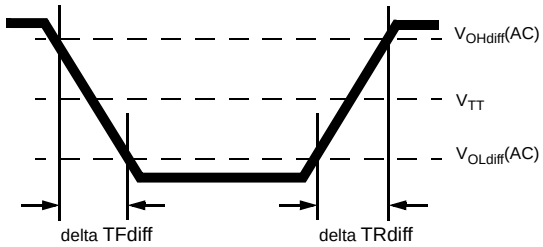


Figure 7. Differential Output Slew Rate Definition

[Table 15] Differential output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	8	18	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

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12.10 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

[Table 16] Single-ended AC & DC output levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V	1

NOTE :
1. The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.

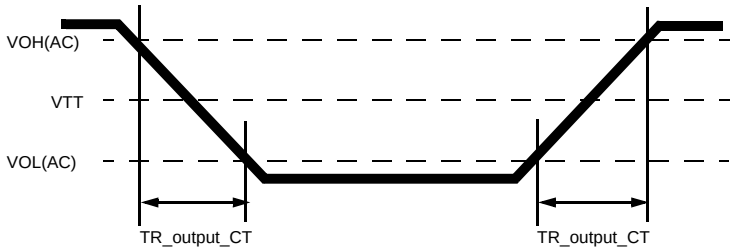


Figure 8. Output Slew Rate Definition of Connectivity Test Mode

[Table 17] Single-ended output slew rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400/2666		Unit	Notes
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

12.11 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 9.

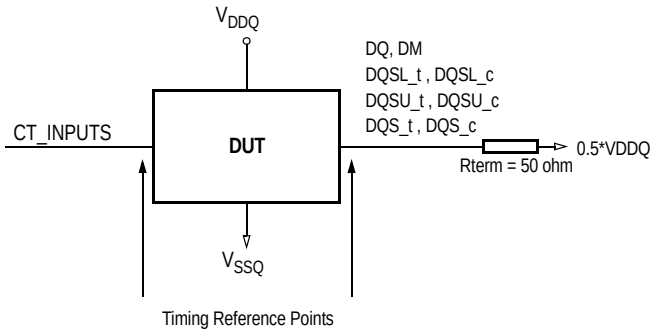


Figure 9. Connectivity Test Mode Timing Reference Load

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13. DIMM IDD specification definition

[Table 18] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
IDD2N	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD2NA	**Precharge Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N**
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according ; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current** **Same condition with IDD2P**
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0

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Symbol	Description
IDD3N	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:**Refer to Component Datasheet for detail pattern
IDD3NA	**Active Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD3N
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: sRefer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P**
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** seamless read data burst with different data between one burst and the next one according ; **DM_n**: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD4RA	**Operating Burst Read Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD4R
IDD4RB	**Operating Burst Read Current with Read DBI** **Read DBI enabled[3], Other conditions:** see IDD4R
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R**
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	**Operating Burst Read IDDQ Current with Read DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** seamless write data burst with different data between one burst and the next one ; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD4WA	**Operating Burst Write Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD4W
IDD4WB	**Operating Burst Write Current with Write DBI** **Write DBI enabled[3], Other conditions:** see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions:** see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled[3], Other conditions:** see IDD4W
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W**
IDD5B	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IPP5B	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B**
IDD5F2	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see IDD5B
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F2**

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Symbol	Description
IDD5F4	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see IDD5B
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F4**
IDD6N	**Self Refresh Current: Normal Temperature Range** **T_{CASE}:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range** **T_{CASE}:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** **T_{CASE}:** 0 - TBD (~35-45)°C; **Low Power Array Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** **Same condition with IDD6R**
IDD6A	**Auto Self-Refresh Current** **T_{CASE}:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Auto[4];**Partial Array Self-Refresh (PASR)**: Full Array; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** read data bursts with different data between one burst and the next one ; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7**
IDD8	**Maximum Power Down Current TBD**
IPP8	**Maximum Power Down IPP Current** **Same condition with IDD8**

NOTE :
1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
   - set MR1 [A12 = 0] : Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
   RTT_Nom enable
   - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
   RTT_WR enable
   - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2
   RTT_PARK disable
   - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
   010] : 1866MT/s, 2133MT/s
   011] : 2400MT/s , 2666MT/s
   Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate
   DLL disabled : set MR1 [A0 = 0]
   CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
   010] : 2400MT/s, 2666MT/s
   Read DBI enabled : set MR5 [A12 = 1]
   Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
   01] : Reduced Temperature range
   10] : Extended Temperature range
   11] : Auto Self Refresh

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14. IDD SPEC Table

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

[Table 19] I_{DD} and I_{DDQ} Specification

Symbol	M386AAK40B40 : 128GB(16Gx72) Module						Unit	NOTE
	DDR4-2133		DDR4-2400		DDR4-2666			
	17-15-15		20-18-18		22-19-19			
	VDD 1.2V	VPP2.5V	VDD 1.2V	VPP2.5V	VDD 1.2V	VPP2.5V		
	IDD Max.	IPP Max.	IDD Max.	IPP Max.	IDD Max.	IPP Max.		
I_{DD0}	3103	198	3248	198	3400	198	mA	
I_{DD0A}	3240	198	3408	198	3585	198	mA	
I_{DD1}	3695	198	3866	198	4045	198	mA	
I_{DD1A}	3859	198	4052	198	4255	198	mA	
I_{DD2N}	2814	180	2937	180	3066	180	mA	
I_{DD2NA}	3155	180	3331	180	3517	180	mA	
I_{DD2NT}	2849	180	2979	180	3115	180	mA	
I_{DD2NL}	2592	180	2703	180	2819	180	mA	
I_{DD2NG}	2784	180	2899	180	3019	180	mA	
I_{DD2ND}	2727	180	2834	180	2946	180	mA	
I_{DD2N_par}	2802	180	2917	180	3037	180	mA	
I_{DD2P}	1713	180	1770	180	1829	180	mA	
I_{DD2Q}	2730	180	2838	180	2951	180	mA	
I_{DD3N}	4115	180	4295	180	4483	180	mA	
I_{DD3NA}	4403	180	4634	180	4878	180	mA	
I_{DD3P}	2366	180	2448	180	2533	180	mA	
I_{DD4R}	6262	180	6664	180	7092	180	mA	
I_{DD4RA}	6266	180	6684	180	7130	180	mA	
I_{DD4RB}	6179	180	6581	180	7010	180	mA	
I_{DD4W}	6790	180	7230	180	7699	180	mA	
I_{DD4WA}	6840	180	7288	180	7766	180	mA	
I_{DD4WB}	6609	180	7035	180	7489	180	mA	
I_{DD4WC}	6265	180	6652	180	7063	180	mA	
I_{DD4W_par}	6376	180	6773	180	7195	180	mA	
I_{DD5B1}	11244	882	11377	882	11512	882	mA	
I_{DD5F2}	8516	648	8643	648	8772	648	mA	
I_{DD5F4}	7584	558	7658	558	7733	558	mA	
I_{DD5B2}	5867	414	6004	414	6145	414	mA	
I_{DD5F3}	4899	324	5014	324	5132	324	mA	
I_{DD5F5}	4564	306	4691	306	4822	306	mA	
I_{DD6N}	2280	252	2283	252	2287	252	mA	
I_{DD6E}	3522	360	3525	360	3529	360	mA	
I_{DD6R}	1655	180	1659	180	1664	180	mA	
I_{DD6A}	2164	252	2168	252	2173	252	mA	
I_{DD7}	7677	288	8284	288	8939	288	mA	
I_{DD8}	982	144	986	144	991	144	mA	

NOTE :

1. DIMM IDD SPEC is based on the condition that de-actived rank(IDLE) is IDD2N. Please refer to DIMM Rank Status.
2. IDD current measure method and detail patterns are described on DDR4 component datasheet.
3. VDD and VDDQ are merged on module PCB (IDDQ values are not considered by Qoff condition)
4. DIMM IDD Values are calculated based on the component IDD spec and Register power.

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DIMM Rank Status

SEC DIMM	Operating Rank	The other Rank
I_{DD0}	I_{DD0}	I_{DD2N}
I_{DD1}	I_{DD1}	I_{DD2N}
I_{DD2P}	I_{DD2P}	I_{DD2P}
I_{DD2N}	I_{DD2N}	I_{DD2N}
I_{DD2Q}	I_{DD2Q}	I_{DD2Q}
I_{DD3P}	I_{DD3P}	I_{DD3P}
I_{DD3N}	I_{DD3N}	I_{DD3N}
I_{DD4R}	I_{DD4R}	I_{DD2N}
I_{DD4W}	I_{DD4W}	I_{DD2N}
I_{DD5B}	I_{DD5B}	I_{DD2N}
I_{DD6}	I_{DD6}	I_{DD6}
I_{DD7}	I_{DD7}	I_{DD2N}
I_{DD8}	I_{DD8}	I_{DD8}

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15. Input/Output Capacitance

[Table 20] Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		Unit	NOTE
		min	max	min	max		
C_{IO}	Input/output capacitance	0.7	1.6	0.7	1.5	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	pF	1,3,4
C_{I}	Input capacitance(CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta(All CTRL pins only)	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta(All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	2.5	0.5	2.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	0.5	2.5	0.5	2.5	pF	1,3,12

NOTE:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
2. DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to 3DS devices. It is meant to represent the silicon pad capacity of the master die.
4. Absolute value CK_T-CK_C
5. Absolute value of CIO(DQS_T)-CIO(DQS_C)
6. CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. CDI CTRL applies to ODT, CS_n and CKE
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))
9. CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_C))
12. Maximum external load capacitance on ZQ pin: tbd pF.

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16. Electrical Characteristics & AC Timings for DDR4-1600-3DS to DDR4-2666-3DS

16.1 Refresh parameters

Typical platforms are designed with the assumption that no more than one physical rank is refreshed at the same time. In order to limit the maximum refresh current (IDD5B1) for a 3D stacked SDRAM, it will be required to stagger the refreshes to each device in a stack.

The tRFC time for a single logical rank is defined as tRFC_slr and is specified as the same value as for a monolithic DDR4 SDRAM of equivalent density. The minimum amount of stagger between refresh commands (=tREF_stagger) sent to different logical ranks is specified to be approximately tRFC_slr/3 - Table 21 below.

[Table 21] Refresh parameters by logical rank density

Parameter	Symbol		Logical Rank Density			Units	NOTE
			4Gb	8Gb	16Gb		
REF command to ACT or REF command time to same logical rank	tRFC_slr1 (1X mode)		260	350	TBD1	ns	
	tRFC_slr2 (2X mode)		160	260	TBD2	ns	
	tRFC_slr4 (4X mode)		110	160	TBD3	ns	
REF command to REF command to different logical rank	tRFC_slr1 (1X mode)		90	120	TBD1/3	ns	
	tRFC_slr2 (2X mode)		55	90	TBD2/3	ns	
	tRFC_slr4 (4X mode)		40	55	TBD3/3	ns	
Average periodic refresh interval in same logical rank	tREFI_slr1 (1X mode)	0°C = < T_{CASE} = < 85°C	7.8	7.8	TBD4	us	
		85°C < T_{CASE} = < 95°C	3.9	3.9	TBD4/2	us	
	tREFI_slr2 (2X mode)	0°C = < T_{CASE} = < 85°C	3.9	3.9	TBD4/2	us	
		85°C < T_{CASE} = < 95°C	1.95	1.95	TBD4/2	us	
	tREFI_slr4 (4X mode)	0°C = < T_{CASE} = < 85°C	1.95	1.95	TBD4/4	us	
		85°C < T_{CASE} = < 95°C	0.975	0.975	TBD4/8	us	

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[Table 22] Timing Parameters by Speed Grade

Parameter	Symbol	DDR4-1600-3DS		DDR4-1866-3DS		DDR4-2133-3DS		DDR4-2400-3DS		DDR4-2666-3DS		Units	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Row Activate to Row Activate Delay													
ACTIVATE to ACTIVATE command period to different bank group in the same logical rank	tRRD_S_slr	max(4nCK,5ns)	-	max(4nCK,4.2ns)	-	max(4nCK,3.7ns)	-	max(4nCK,3.3ns)	-	TBD	TBD	ns	
ACTIVATE to ACTIVATE command period to same bank group in the same logical rank	tRRD_L_slr	max(4nCK,6ns)	-	max(4nCK,5.3ns)	-	max(4nCK,5.3ns)	-	max(4nCK,4.9ns)	-	TBD	TBD	ns	
ACTIVATE to ACTIVATE command period to different logical ranks	tRRD_dlr	4	-	4	-	4	-	4	-	TBD	TBD	nCK	
Four Activate Window													
Four activate window to the same logical rank for 0.5KB page size	tFAW_slr_x4	20	-	17	-	15	-	13	-	TBD	TBD	ns	1
Four activate window to the same logical rank for 1KB page size	tFAW_slr_x8	25	-	23	-	21	-	21	-	TBD	TBD	ns	2
Four activate window to different logical ranks	tFAW_dlr	16	-	16	-	16	-	16	-	TBD	TBD	nCK	
Self-Refresh Timings													
Exit Self-Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC_slr(min)+10ns)	-	max(5nCK,tRFC_slr(min)+10ns)	-	max(5nCK,tRFC_slr(min)+10ns)	-	max(5nCK,tRFC_slr(min)+10ns)	-	TBD	TBD		3

NOTE:
1. For x4 devices only.
2. For x8 devices only.
3. Upon exit from Self-Refresh, the 3D Stacked DDR4 SDRAM requires a minimum of one extra refresh command to all logical ranks before it is put back into Self-Refresh Mode.

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16.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding bin

[Table 23] DDR4-1600 Speed Bins and Operations

Speed Bin			DDR4-1600		Unit	NOTE
CL-nRCD-nRP			13-12-11			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	16.25	21.00	ns	
ACT to internal read or write delay time		tRCD	15	-	ns	
PRE command period		tRP	13.75	-	ns	
ACT to PRE command period		tRAS	35	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	48.75	-	ns	
CWL = 9,11	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings			11,12,13,14		nCK	
Supported nRCD Timings minimum			10		nCK	
Supported nRP Timings minimum			10		nCK	
Supported CWL Settings			9,11		nCK	

[Table 24] DDR4-1866 Speed Bins and Operations

Speed Bin			DDR4-1866		Unit	NOTE
CL-nRCD-nRP			15-14-13			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	16.07	21.00	ns	
ACT to internal read or write delay time		tRCD	15	-	ns	
PRE command period		tRP	13.92 (13.75[12])	-	ns	
ACT to PRE command period		tRAS	34	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	47.92	-	ns	
CWL = 9,11	CL = 12	tCK(AVG)	Reserved		ns	1.2.3.4.6
	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings			11,12,13,14,15,16		nCK	
Supported nRCD Timings minimum			10		nCK	
Supported nRP Timings minimum			10		nCK	
Supported CWL Settings			9,10,11,12		nCK	

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[Table 25] DDR4-2133 Speed Bins and Operations

Speed Bin			DDR4-2133		Unit	NOTE
CL-nRCD-nRP			17-15-15			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	15.95	21.00	ns	
ACT to internal read or write delay time		tRCD	14.06	-	ns	
PRE command period		tRP	14.06 (13.75[12])	-	ns	
ACT to PRE command period		tRAS	33	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	47.06	-	ns	
CWL = 9,11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,7
	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 16	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 20	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,7
Supported CL Settings			11,12,13,14,15,16,17,18		nCK	
Supported nRCD Timings minimum			10		nCK	
Supported nRP Timings minimum			10		nCK	
Supported CWL Settings			9,10,11,12,14		nCK	

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[Table 26] DDR4-2400 Speed Bins and Operations

Speed Bin			DDR4-2400		Unit	NOTE
CL-nRCD-nRP			20-18-18			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	16.67	21.00	ns	
ACT to internal read or write delay time		tRCD	15	-	ns	
PRE command period		tRP	15	-	ns	
ACT to PRE command period		tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	47	-	ns	
CWL = 9,11	CL = 13	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 15	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 16	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 17	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4,8
CWL = 12,16	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	tCK(AVG)	0.833	<0.937	ns	1,2,3,4
	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4
	CL = 22	tCK(AVG)	Reserved		ns	1,2,3,4,8
Supported CL Settings			11,12,13,14,15,16,17,18,19,20		nCK	
Supported nRCD Timings minimum			10		nCK	
Supported nRP Timings minimum			10		nCK	
Supported CWL Settings			9,10,11,12,14,16		nCK	

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[Table 27] DDR4-2666 Speed Bins and Operations

Speed Bin			DDR4-2666		Unit	NOTE
CL-nRCD-nRP			22-19-19			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	16.5	21.00	ns	
ACT to internal read or write delay time		tRCD	14.25	-	ns	
PRE command period		tRP	14.25	-	ns	
ACT to PRE command period		tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	46.25	-	ns	
CWL = 9,11	CL = 13	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 15	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 16	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
	CL = 20	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
	CL = 22	tCK(AVG)	0.833	<0.937	ns	1,2,3,9
CWL = 14,18	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 22	tCK(AVG)	0.75	0.833	ns	1,2,3,4,9
	CL = 24	tCK(AVG)	0.75	0.833	ns	1,2,3,9
Supported CL Settings			11,12,13,14,15,16,17,18,19,20,22,24		nCK	
Supported nRCD Timings minimum			12		nCK	
Supported nRP Timings minimum			12		nCK	
Supported CWL Settings			9,10,11,12,14,16,18		nCK	

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16.3 Speed Bin Table Note

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-3DS-1600, 1866, 2133, 2400 Speed Bin Tables are valid only when Gear_Down mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.937 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 12 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-3DS-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-3DS-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-3DS-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR4-3DS-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characteriza-tion.
10. 13.75ns is minimum tRCD when operating by DDR4-1600K-3DS2B at tCK(AVG).min=1.25ns
11. 12.85ns is minimum tRCD when operating by DDR4-1866L-3DS2B at tCK(AVG).min=1.071ns
12. 17.14 ns is the minimum tAA when operating in DDR4-1866N-3DS2B at tCK(AVG).min=1.071ns.
13. 13.75ns is minimum tRP when operating by DDR4-1600K-3DS2B at tCK(AVG).min=1.25ns

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17. Timing Parameters by Speed Grade

[Table 28] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2666

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing													
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	8	20	ns	-
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	0.750	<0.833	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot tCK(avg)m ax + tJIT(per)max_tot										tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	-38	38	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	-19	19	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	-30	30	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	125	-	107	-	94	-	83	-	75	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	100	-	86	-	75	-	67	-	60	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	-55	55	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	-66	66	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	-73	73	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	-78	78	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	-83	83	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	-87	87	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	-91	91	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	-94	94	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	-96	96	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	-99	99	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	-101	101	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	-103	103	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	-104	104	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	-106	106	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	-108	108	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	-110	110	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	-112	112	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	^{t}ERR(nper)min = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total min) ^{t}ERR(nper)max = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total max)										ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	TBD	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	TBD	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	TBD	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	TBD	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	385	-	ps	
Command and Address Timing													
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.625 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,5ns)		Max(4nCK,4.2ns)		Max(4nCK,3.7ns)		Max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	nCK	34

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,5ns)		Max(4nCK,4.2ns)		Max(4nCK,3.7ns)		Max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7.5ns)		Max(4nCK,6.4ns)		Max(4nCK,6.4ns)		Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6ns)		Max(4nCK,5.3ns)		Max(4nCK,5.3ns)		Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,6ns)		Max(4nCK,5.3ns)		Max(4nCK,5.3ns)		Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,35ns)		Max(28nCK,30ns)		Max(28nCK,30ns)		Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,25ns)		Max(20nCK,23ns)		Max(20nCK,21ns)		Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,20ns)		Max(16nCK,17ns)		Max(16nCK,15ns)		Max(16nCK,13ns)	-	Max(16nCK,12ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max (2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-		1,2,e,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (4nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max (4nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (4nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	854	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-		50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-		
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))										nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency													
CS_n to Command Address Latency	tCAL	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	5	-	5	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL		tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL		tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
DRAM Data Timing													
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.16	-	0.18	tCK(avg)/2	13,18,39,49
DQ output hold per group, per access from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	0.74	-	tCK(avg)/2	13,17,18,39,49
Data Valid Window per device: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	TBD	-	UI	17,18,39,49
Data Valid Window , per pin per UI : (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	0.72	-	UI	17,18,39,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-390	180	-330	175	-310	170	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	-	175	-	170	ps	39
Data Strobe Timing													
DQS_t, DQS_c differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	0.9	NOTE 44	0.9	NOTE 44	tCK	40

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Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ Pre-amble (2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	1.8	NOTE 44	1.8	NOTE 44	tCK	41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Pre-amble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Pre-amble (2 clock preamble)	tWPRE2	NA		NA		NA		1.8	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-330	175	-310	170	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	-	170	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	NA	NA	NA	NA	NA	NA	TBD	TBD	TBD	TBD	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	-175	175	-170	170	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		370		330		310		290		270	ps	37,38,39
MPSM Timing													
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	TBD	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	TBD	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	TBD	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	TBD	-		
CS setup time to CKE	tMPX_S	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	TBD	-		
Calibration Timing													
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing													
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-		

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max (5nCK,10 ns)	-	max (5nCK,10 ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10 ns)+PL	-	max (5nCK,10 ns)+PL	-	max (5nCK,10 ns)+PL	-	max (5nCK,10 ns)+PL	-	max (5nCK,10 ns)+PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max (5nCK,10 ns)	-	max (5nCK,10 ns)	-		
Power Down Timing													
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing													
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		tMOD			
ODT Timing													
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing													
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	0	2	ns	
CA Parity Timing													
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	-	PL		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns		

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Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	80	160	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64		71	nCK	
Parity Latency	PL	4		4		4		5		5		nCK	
CRC Error Reporting													
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	6	10	nCK	
Geardown timing													
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	-	-	-	-	-	-	-	-	TBD			
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-	-	-	-	-	-	-	-	TBD			
MRS command to Sync pulse time(T3)	tSYNC_GEAR	-	-	-	-	-	-	-	-	TBD	-		27
Sync pulse to First valid command(T4)	tCMD_GEAR	-	-	-	-	-	-	-	-	TBD			27
Geardown setup time	tGEAR_setup	-	-	-	-	-	-	-	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	-	-	-	-	-	-	2	-	nCK	
tREFI													
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	260	-	260	-	ns	34

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NOTE :

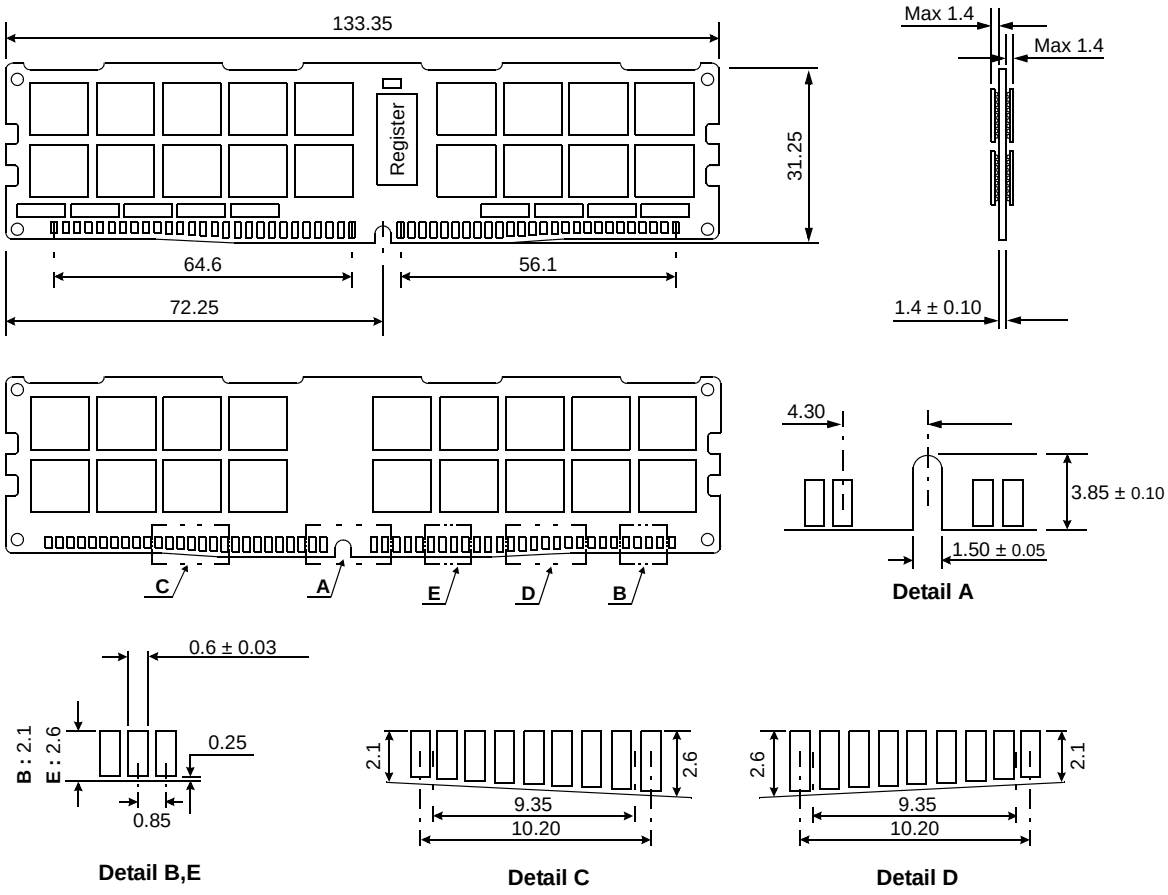
1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables .
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
    UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM
39. Value is only valid for RZQ/7 RONNOM = 34 ohms
40. 1tCK toggle mode with setting MR4:A11 to 0
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666 speed grade.
42. 1tCK mode with setting MR4:A12 to 0
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

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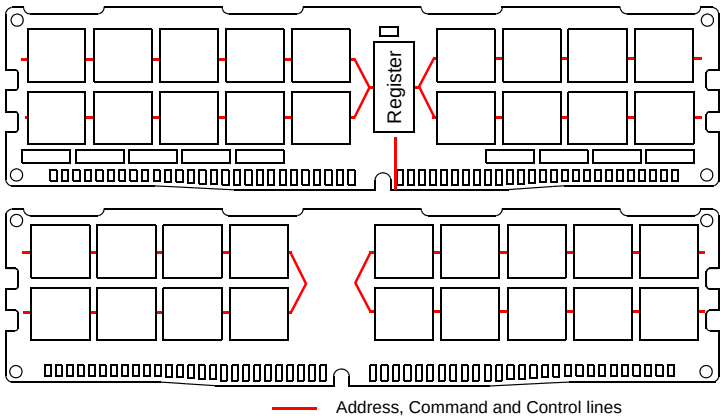
18. Physical Dimensions

18.1 8Gbx4(4H TSV) based 16Gx72 Module (2 physical ranks / 4 logical ranks)

Units : Millimeters



18.1.1 x72 DIMM, populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAMs



The used device is 8G x4(4H TSV) DDR4 SDRAM, FBGA.
DDR4 SDRAM Part NO : K4ABG045WB-4C**

* **NOTE** : Tolerances on all dimensions ±0.15 unless otherwise specified.

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Exhibit 8

Rev. 1.4, Jun. 2017

M386A8K40BM1
M386A8K40BM2

288pin Load Reduced DIMM based on 8Gb B-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

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Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	- First SPEC Release	Apr. 2015	-	J.Y.Lee
1.1	- Change of IDD value on page 25 - Change of 8.1 Timing & Capacitance values (tACT) on page 9 - Change of Physical Dimensions (Module Thickness) on page 38	2nd Feb. 2016	-	J.Y.Lee
1.2	- Addition of DDR4-2666	7th Apr. 2016	-	J.Y.Lee
1.21	- Correction of typo.	18th Apr. 2016	-	S.H.Kim
1.3	- Addition of IDD value (2666Mbps) on page 25	17th Nov. 2016	-	J.Y.Lee
1.4	- Update Physical dimension. 1. Add PCB hole. 2. Update Module height information. - Update Absolute Maximum Ratings. - Update Input/Output Capacitance.	8th Jun, 2017	Final	J.Y.Bae

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1. DDR4 Load Reduced DIMM Ordering Information

Part Number[2]	Density	Organization	Component Composition[1]	Number of Rank	Height
M386A8K40BM1-CPB/RC	64GB	8Gx72	DDP 4Gx4(K4AAG045WB-MC##)*36	4	31.25mm
M386A8K40BM2-CTD	64GB	8Gx72	DDP 4Gx4(K4AAG045WB-MC##)*36	4	31.25mm

NOTE :
1. "##" - PB/RC/TD
2. PB(2133Mbps 15-15-15)/RC(2400Mbps 17-17-17)/TD(2666Mbps 19-19-19)
   - DDR4-2666(19-19-19) is backward compatible to DDR4-2400(17-17-17)

2. Key Features

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	
tCK(min)	1.25	1.071	0.938	0.833	0.75	ns
CAS Latency	11	13	15	17	19	nCK
tRCD(min)	13.75	13.92	14.06	14.16	14.25	ns
tRP(min)	13.75	13.92	14.06	14.16	14.25	ns
tRAS(min)	35	34	33	32	32	ns
tRC(min)	48.75	47.92	47.06	46.16	46.25	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin,1200MHz f_{CK} for 2400Mb/sec/pin, 1333MHz f_{CK} for 2666Mb/sec/pin
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 10,11,12,13,14,15,16,17,18,19,20
- Programmable Additive Latency (Posted CAS): 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866), 11,14 (DDR4-2133), 12,16 (DDR4-2400) and 14,18 (DDR4-2666)
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Asynchronous Reset

3. Address Configuration

Organization	Row Address	Column Address	Bank Group Address	Bank Address	Auto Precharge
4Gx4(16Gb DDP) based Module	A0-A16	A0-A9	BG0-BG1	BA0-BA1	A10/AP

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4. Load Reduced DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V[3],NC	145	12V[3],NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

NOTE:

1. VPP is 2.5V DC
2. Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.
3. Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4. The 5th VPP is required on all modules. DIMMs.

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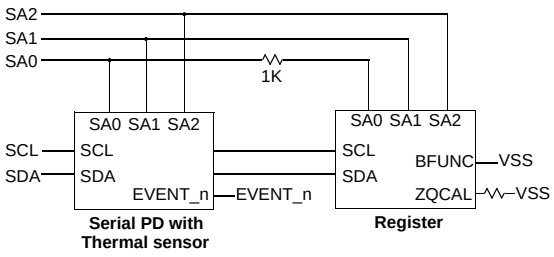
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5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0–SA2	I2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input for activate input	ALERT_n	Register ALERT_n output
DQ0–DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
CK0_t, CK1_t	Register clock input (positive line of differential pair)		
CK0_c, CK1_c	Register clocks input (negative line of differential pair)		

NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

6. ON DIMM Thermal Sensor



NOTE : 1. All Samsung RDIMM support Thermal sensor on DIMM

[Table 1] Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

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7. Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers,excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1	Input	Chip ID : Chip ID is only used for 3DS for 2and4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components only BG0 is valid.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.

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Symbol	Type	Function
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output	ALERT: It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system. In case of not connected as Signal, ALERT_n Pin must be connected to VDD on DIMM.
SA0-SA1	Input	Device address for the SPD.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		No Connect: No on DIMM electrical connection is present.
VDD[1]	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VTT[2]	Supply	Power Supply: 0.6 V
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD 2.5V ± 10%.

NOTE :

1. For PC4, VDD is 1.2 V. For PC4L VDD is TBD.
2. For PC4, VTT is 0.6 V. For PC4L VTT is TBD.

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8. Registering Clock Driver Specification

8.1 Timing & Capacitance Values

Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400/2666		Units	Notes
			Min	Max	Min	Max		
fclock	Input Clock Frequency	application frequency	625	1080	625	1350	MHz	
t_{CH}/t_{CL}	Pulse duration, CK_t, CK_c HIGH or LOW		0.4	-	0.4	-	t_{CK}	
t_{ACT}	Inputs active time4 before DRST_n is taken HIGH	DCKE0/1 = LOW and DCS0/1_n = HIGH	16	-	16	-	t_{CK}	
t_{PDM}	Propagation delay, single-bit switching, CK_t/ CK_c to output	1.2V Operation	1	1.3	1	1.3	ns	
t_{DIS}	output disable time	Rising edge of Yn_t to output float	0.5*tCK + tQSK1(min)	-	0.5*tCK + tQSK1(min)	-	ps	
t_{EN}	output enable time	Output valid to rising edge of Yn_t	0.5*tCK - tQSK1(max)	-	0.5*tCK - tQSK1(max)	-	ps	
C_I	Input capacitance, Data inputs	NOTE[1,2]	0.8	1.1	0.8	1.0	pF	
C_{CK}	Input capacitance, CK_t, CK_c	NOTE[1,2]	0.8	1.1	0.8	1.0		
C_{IR}	Input capacitance, DRST_n	$V_I=V_{DD}$ or V_{SS} ; V_{DD}=1.2V	0.5	2.0	0.5	2.0		

Note:
1. This parameter does not include package capacitance
2. Data inputs are DCKE0/1, DODT0/1, DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DC0..DC2, DPAR, DCS0/1_n

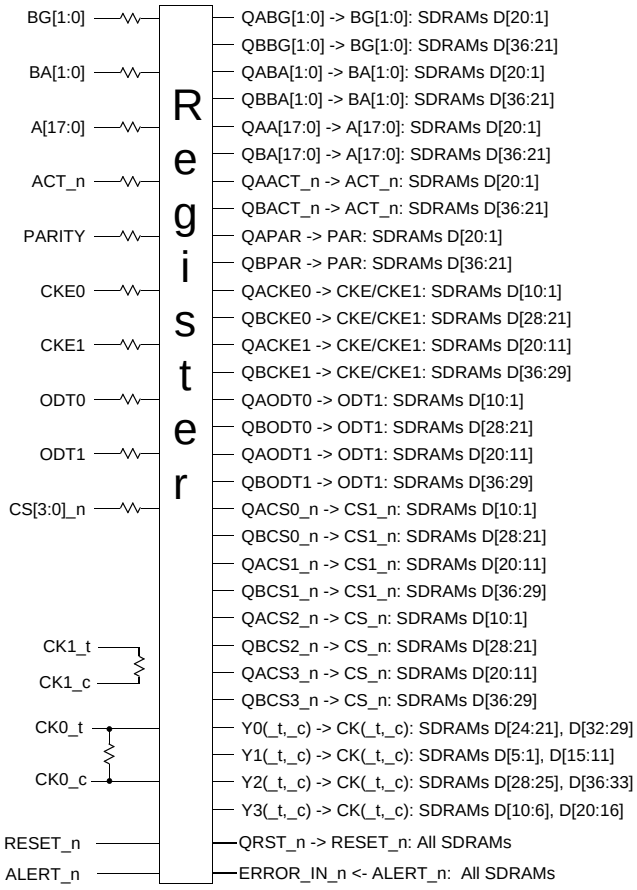
8.2 Clock Driver Characteristics

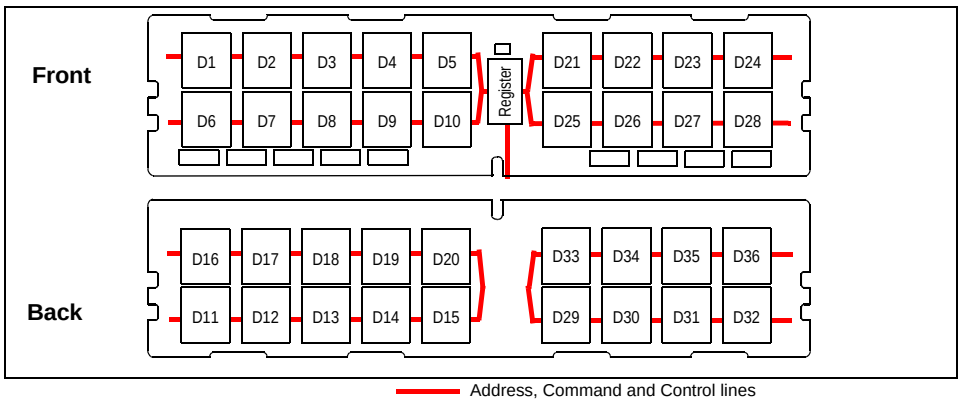
Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		Units	Notes
			Min	Max	Min	Max	Min	Max		
t_{jit} (cc)	Cycle-to-cycle period jitter	CK_t/CK_c stable	0	0.025 x tCK	0	0.025 x tCK	0	0.025 x tCK	ps	
t_{STAB}	Stabilization time		-	5	-	5	-	5	us	
t_{CKsk}	Clock Output skew		-	10	-	10	-	10	ps	
t_{jit}(per)	Yn Clock Period jitter		-0.025 * tCK	0.025 * tCK	-0.025 * tCK	0.025 * tCK	-0.025 * tCK	0.025 * tCK	ps	
t_{jit}(hper)	Half period jitter		-0.032 * tCK	0.032 * tCK	-0.032 * tCK	0.032 * tCK	-0.032 * tCK	0.032 * tCK	ps	
t_{Qsk1}	Qn Output to clock tolerance		-0.125 * tCK	0.125 * tCK	-0.125 * tCK	0.125 * tCK	-0.1 * tCK	0.1 * tCK	ps	
t_{dynoff}	Maximum re-driven dynamic clock off-set		-	50	-	45	-	45	ps	

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9. Function Block Diagram:

9.1 64GB, 8Gx72 Module (Populated as 4 ranks of x4 DDR4 SDRAMs)

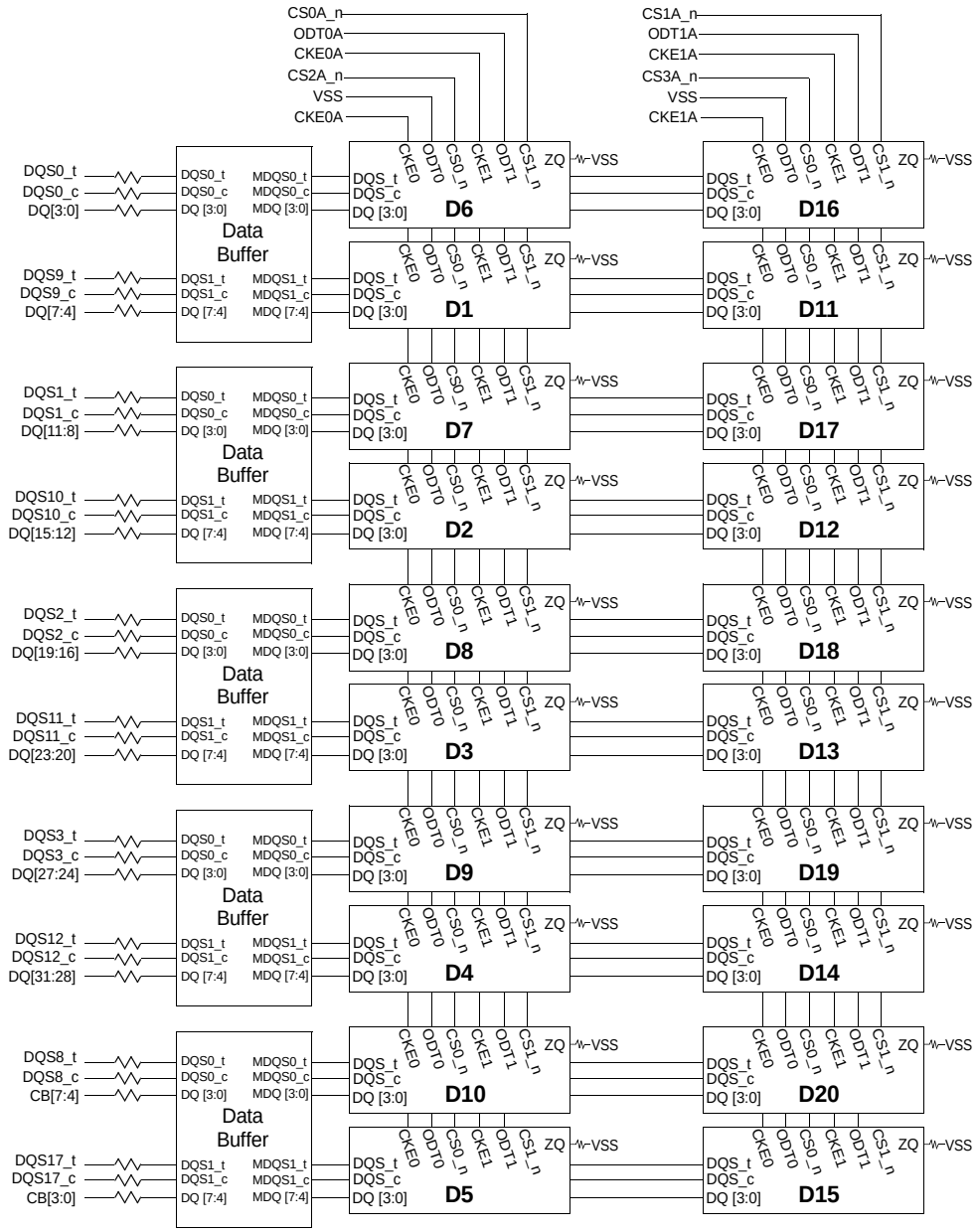




NOTE :

1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

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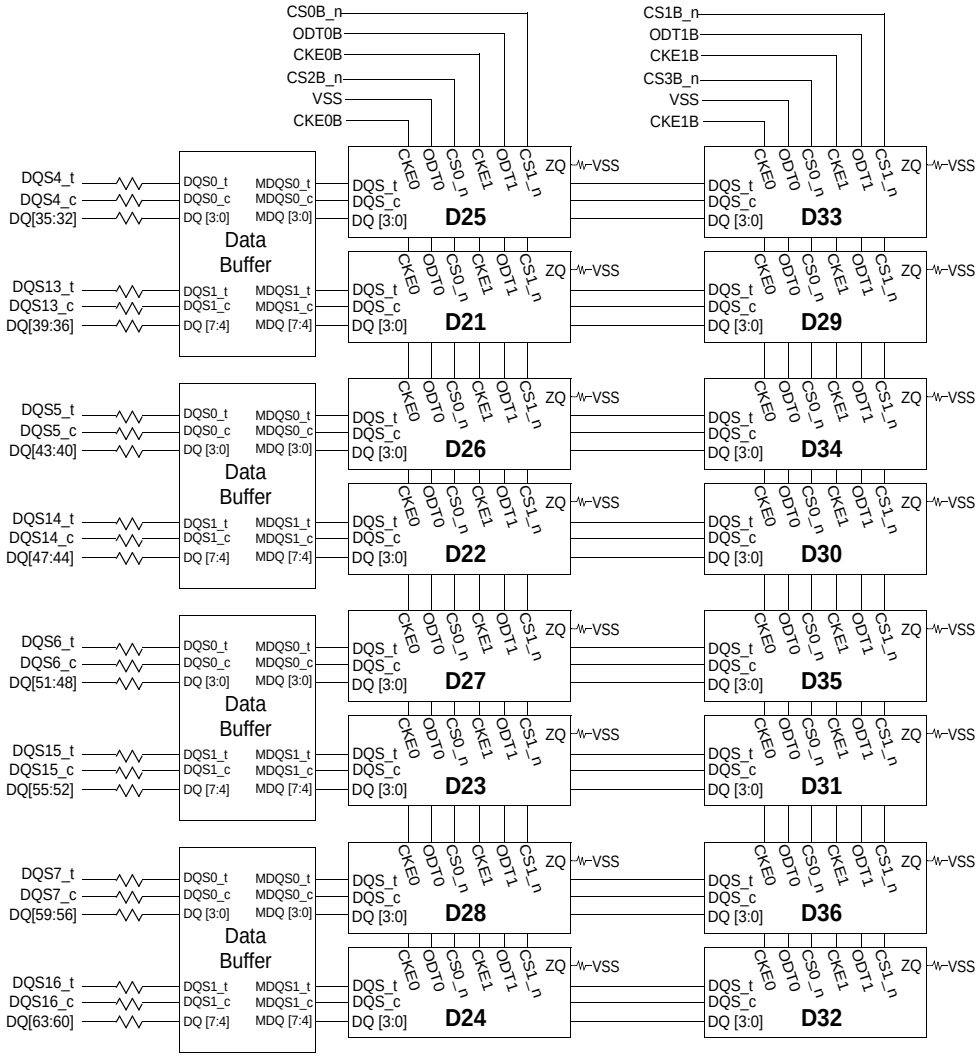


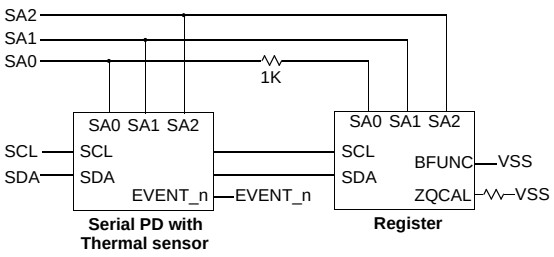
NOTE :

1. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. TEN pin of SDRAMs is tied to VSS.

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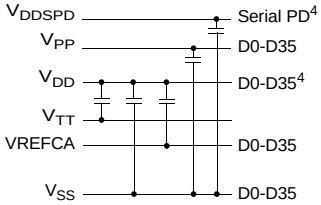
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Serial PD with Thermal sensor

Register



NOTE :

1. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. TEN pin of SDRAMs is tied to VSS.
4. VDDSPD is also applied to the register. VDD is also applied to the register and the data buffers.

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10. Absolute Maximum Ratings

10.1 Absolute Maximum DC Ratings

[Table 2] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA to Vss	-0.3 ~ 1.5	V	1,3
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

11. AC & DC Operating Conditions

11.1 Recommended DC Operating Conditions

[Table 3] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

NOTE:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. DC bandwidth is limited to 20MHz.

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12. AC & DC Input Measurement Levels

12.1 AC & DC Logic Input Levels for Single-Ended Signals

[Table 4] Single-ended AC & DC Input Levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666		Unit	NOTE
		Min.	Max.	Min.	Max.		
$V_{IH.CA}$(DC75)	DC input logic high	V_{REFCA}+ 0.075	V_{DD}	TBD	TBD	V	
$V_{IL.CA}$(DC75)	DC input logic low	V_{SS}	V_{REFCA}-0.075	TBD	TBD	V	
$V_{IH.CA}$(AC100)	AC input logic high	V_{REF} + 0.1	Note 2	TBD	TBD	V	1
$V_{IL.CA}$(AC100)	AC input logic low	Note 2	V_{REF} - 0.1	TBD	TBD	V	1
V_{REFCA}(DC)	Reference Voltage for ADD, CMD inputs	0.49*V_{DD}	0.51*V_{DD}	TBD	TBD	V	2,3

NOTE:
1. See “Overshoot and Undershoot Specifications” on section.
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)
3. For reference : approx. VDD/2 ± 12mV

12.2 AC and DC Input Measurement Levels: V_{REF} Tolerances.

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 1. It shows a valid reference voltage V_{REF}(t) as a function of time. (V_{REF} stands for V_{REFCA}).

V_{REF}(DC) is the linear average of V_{REF}(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore V_{REF}(t) may temporarily deviate from V_{REF}(DC) by no more than ± 1% V_{DD}.

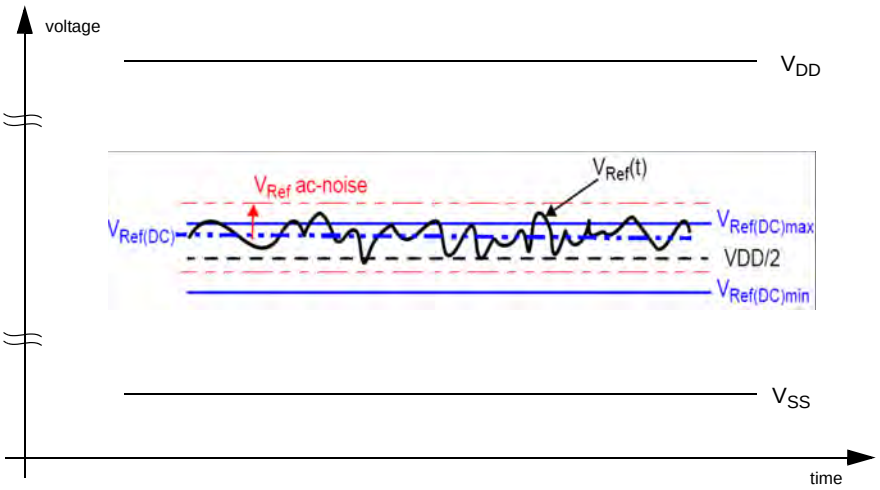


Figure 1. Illustration of V_{REF}(DC) tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{REF}.

"V_{REF}" shall be understood as V_{REF}(DC), as defined in Figure 1.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF}(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

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12.3 AC and DC Logic Input Levels for Differential Signals

12.3.1 Differential Signals Definition

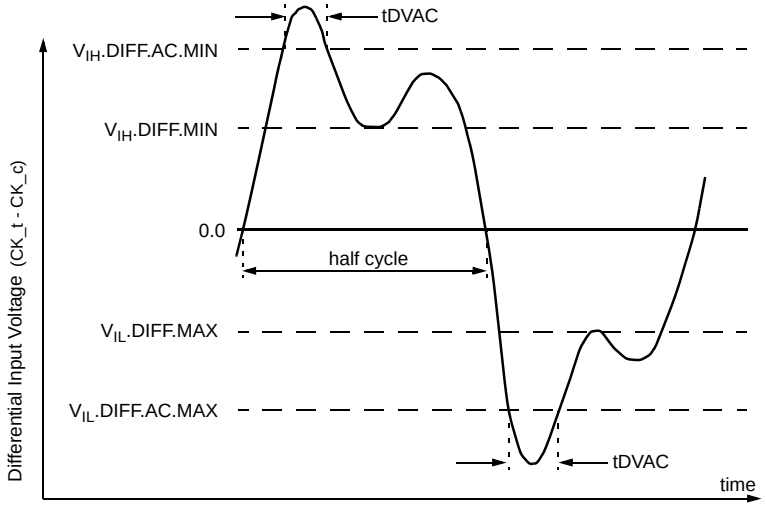


Figure 2. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

NOTE:
1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

12.3.2 Differential Swing Requirements for Clock (CK_t - CK_c)

[Table 5] Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		DDR4 -2400/2666		unit	NOTE
		min	max	min	max		
V_{IHdiff}	differential input high	+0.150	NOTE 3	TBD	NOTE 3	V	1
V_{ILdiff}	differential input low	NOTE 3	-0.150	NOTE 3	TBD	V	1
V_{IHdiff}(AC)	differential input high ac	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2
V_{ILdiff}(AC)	differential input low ac	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	V	2

NOTE:
1. Used to define a differential signal slew-rate.
2. for CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD and V_{REFCA};
3. These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

[Table 6] Allowed Time Before Ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	tDVAC [ps] @ $\|V_{IH/Ldiff}(AC)\|$ = 200mV	
	min	max
> 4.0	120	-
4.0	115	-
3.0	110	-
2.0	105	-
1.8	100	-
1.6	95	-
1.4	90	-
1.2	85	-
1.0	80	-
< 1.0	80	-

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12.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH.CA(AC) / VIL.CA(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than VIH.CA(AC100)/VIL.CA(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c

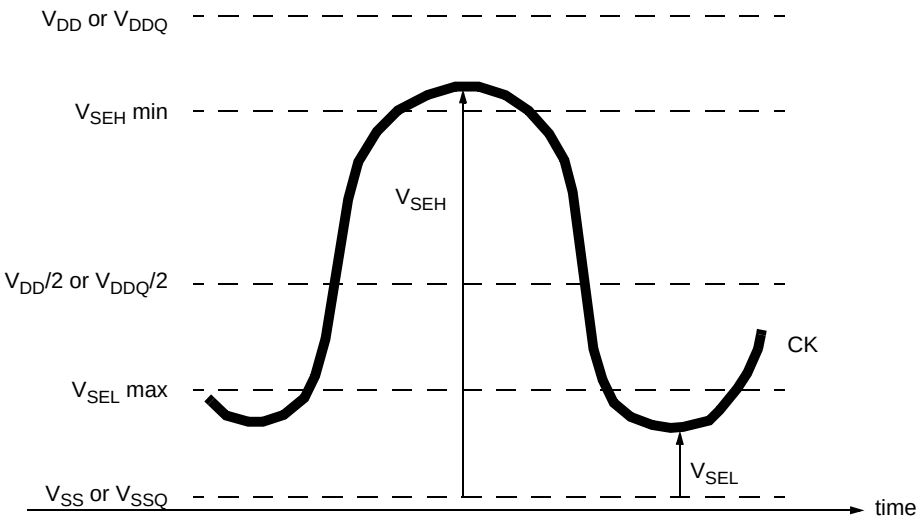


Figure 3. Single-ended requirement for differential signals.

Note that, while ADD/CMD signal requirements are with respect to VrefCA, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 7] Single-ended Levels for CK_t, CK_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		Unit	NOTE
		Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK_t , CK_c	(VDD/2)+0.100	NOTE3	TBD	NOTE3	V	1, 2
V_{SEL}	Single-ended low-level for CK_t , CK_c	NOTE3	(VDD/2)-0.100	NOTE3	TBD	V	1, 2

NOTE:

1. For CK_t - CK_c use $V_{IH.CA}/V_{IL.CA}$(AC) of ADD/CMD;
2. V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};
3. These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

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12.4 Slew Rate Definitions

12.4.1 Slew Rate Definitions for Differential Input Signals (CK)

[Table 8] Differential Input Slew Rate Definition

Description	from	to	Defined by
Differential input slew rate for rising edge(CK_t - CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTRdiff$
Differential input slew rate for falling edge(CK_t - CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTFdiff$
NOTE: The differential signal (i,e.,CK_t - CK_c) must be linear between these thresholds.			

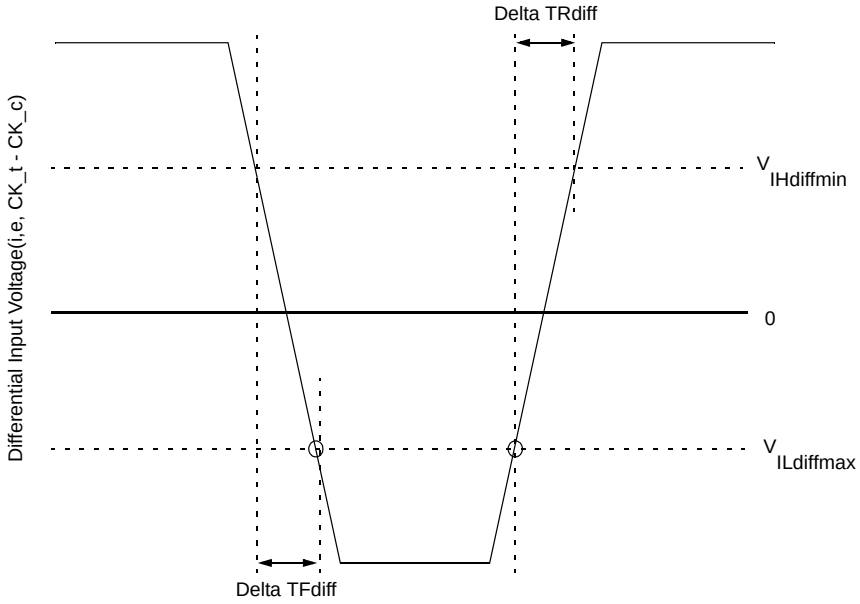


Figure 4. Differential Input Slew Rate Definition for CK_t, CK_c

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12.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 9. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

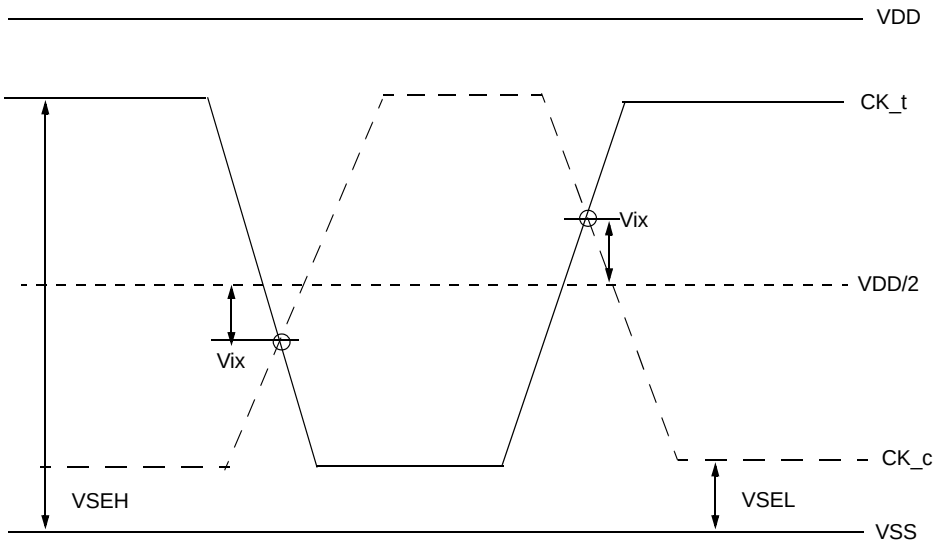


Figure 5. Vix Definition (CK)

[Table 9] Cross Point Voltage for Differential Input Signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133			
		min		max	
-	Area of VSEH, VSEL	VSEL =< VDD/2 - 145mV	VDD/2 - 145mV =< VSEL =< VDD/2 - 100mV	VDD/2 + 100mV =< VSEH =< VDD/2 + 145mV	VDD/2 + 145mV =< VSEH
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120mV	-(VDD/2 - VSEL) + 25mV	(VSEH - VDD/2) - 25mV	120mV

Symbol	Parameter	DDR4-2400/2666			
		min		max	
-	Area of VSEH, VSEL	TBD	TBD	TBD	TBD
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	TBD	TBD	TBD	TBD

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12.6 Single-ended AC & DC Output Levels

[Table 10] Single-ended AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Units	NOTE
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7 - 0.15) x V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x V_{DDQ}	V	1

NOTE:
1. The swing of ± 0.15 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ}.

12.7 Differential AC & DC Output Levels

[Table 11] Differential AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Units	NOTE
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.3 x V_{DDQ}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 x V_{DDQ}	V	1

NOTE:
1. The swing of ± 0.3 × V_{DDQ} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ} at each of the differential outputs.

12.8 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 12 and Figure 6.

[Table 12] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TFse

NOTE:
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

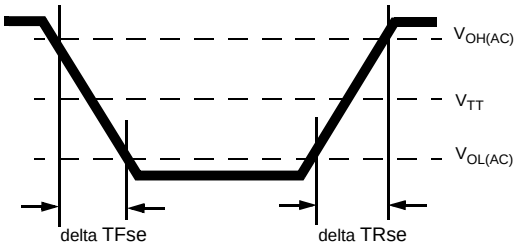


Figure 6. Single-ended Output Slew Rate Definition

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[Table 13] Single-ended Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

NOTE:
1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

12.9 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 14 and Figure 7.

[Table 14] Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}(AC)	V_{OHdiff}(AC)	[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / Delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}(AC)	V_{OLdiff}(AC)	[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / Delta TFdiff

NOTE:
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

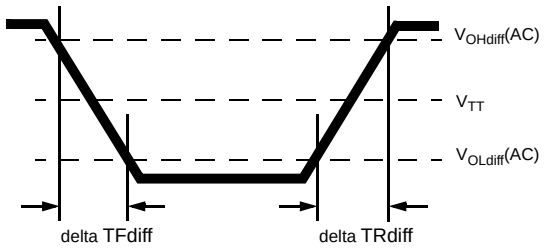


Figure 7. Differential Output Slew Rate Definition

[Table 15] Differential Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	8	18	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

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12.10 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

[Table 16] Single-ended AC & DC Output Levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V	1

NOTE:
1. The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.

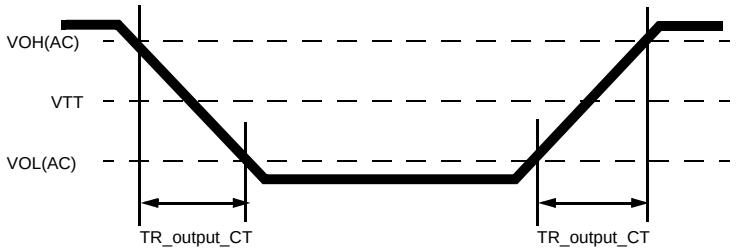


Figure 8. Output Slew Rate Definition of Connectivity Test Mode

[Table 17] Single-ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400/2666		Unit	Notes
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

12.11 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 9.

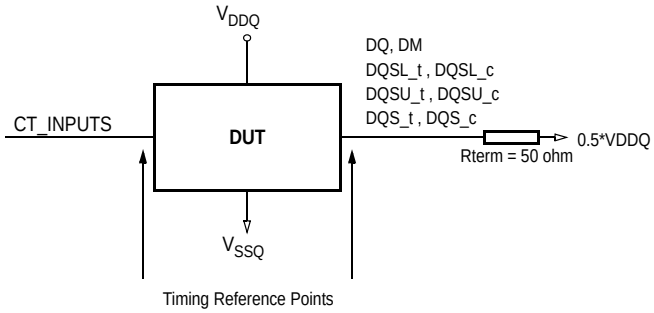


Figure 9. Connectivity Test Mode Timing Reference Load

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13. DIMM IDD Specification Definition

[Table 18] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
IDD2N	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD2NA	**Precharge Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N**
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3,5]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current** **Same condition with IDD2P**
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0

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Symbol	Description
IDD3N	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:**Refer to Component Datasheet for detail pattern
IDD3NA	**Active Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD3N
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: sRefer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P**
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** seamless read data burst with different data between one burst and the next one according; **DM_n**: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD4RA	**Operating Burst Read Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD4R
IDD4RB	**Operating Burst Read Current with Read DBI** **Read DBI enabled[3], Other conditions:** see IDD4R
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R**
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	**Operating Burst Read IDDQ Current with Read DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** seamless write data burst with different data between one burst and the next one; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD4WA	**Operating Burst Write Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD4W
IDD4WB	**Operating Burst Write Current with Write DBI** **Write DBI enabled[3], Other conditions:** see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions:** see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled[3], Other conditions:** see IDD4W
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W**
IDD5B	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IPP5B	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B**
IDD5F2	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see IDD5B
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F2**

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Symbol	Description
IDD5F4	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see IDD5B
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F4**
IDD6N	**Self Refresh Current: Normal Temperature Range** ***T*CASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR)**: Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range** ***T*CASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR)**: Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** ***T*CASE: 0 - 45°C; Low Power Array Self Refresh (LP ASR)**: Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** **Same condition with IDD6R**
IDD6A	**Auto Self-Refresh Current** ***T*CASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR)**: Auto[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** read data bursts with different data between one burst and the next one; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7**
IDD8	**Maximum Power Down Current TBD**
IPP8	**Maximum Power Down IPP Current Same condition with IDD8**

NOTE:
1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
   - set MR1 [A12 = 0]: Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00]: Output Driver Impedance Control = RZQ/7
   RTT_Nom enable
   - set MR1 [A10:8 = 011]: RTT_NOM = RZQ/6
   RTT_WR enable
   - set MR2 [A10:9 = 01]: RTT_WR = RZQ/2
   RTT_PARK disable
   - set MR5 [A8:6 = 000]
3. CAL enabled: set MR4 [A8:6 = 001]: 1600MT/s
   010]: 1866MT/s, 2133MT/s
   011]: 2400MT/s, 2666MT/s
   Gear Down mode enabled: set MR3 [A3 = 1]: 1/4 Rate
   DLL disabled: set MR1 [A0 = 0]
   CA parity enabled: set MR5 [A2:0 = 001]: 1600MT/s,1866MT/s, 2133MT/s
   010]: 2400MT/s, 2666MT/s
   Read DBI enabled: set MR5 [A12 = 1]
   Write DBI enabled: set MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR): set MR2 [A7:6 = 00]: Normal
   01]: Reduced Temperature range
   10]: Extended Temperature range
   11]: Auto Self Refresh
5. IDD2NG should be measured after sync pules (NOP) input.

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14. IDD SPEC Table

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

[Table 19] I_{DD} and I_{DDQ} Specification

Symbol	M386A8K40BM1 : 64GB(8Gx72) Module				M386A8K40BM2 : 64GB(8Gx72) Module		Unit	NOTE
	DDR4-2133		DDR4-2400		DDR4-2666			
	15-15-15		17-17-17		19-19-19			
	VDD 1.2V	VPP2.5V	VDD 1.2V	VPP2.5V	VDD 1.2V	VPP2.5V		
	IDD Max.	IPP Max.	IDD Max.	IPP Max.	IDD Max.	IPP Max.		
I_{DD0}	2674	234	2848	234	2982	234	mA	
I_{DD0A}	2698	234	2895	234	3046	234	mA	
I_{DD1}	3230	234	3427	234	3586	234	mA	
I_{DD1A}	3267	234	3473	234	3647	234	mA	
I_{DD2N}	2549	216	2727	216	2847	216	mA	
I_{DD2NA}	2664	216	2873	216	3034	216	mA	
I_{DD2NT}	2603	216	2820	216	2949	216	mA	
I_{DD2NL}	2129	216	2274	216	2372	216	mA	
I_{DD2NG}	2483	216	2662	216	2773	216	mA	
I_{DD2ND}	2369	216	2535	216	2636	216	mA	
I_{DD2N_par}	2613	216	2788	216	2903	216	mA	
I_{DD2P}	1493	216	1601	216	1655	216	mA	
I_{DD2Q}	2375	216	2539	216	2641	216	mA	
I_{DD3N}	3088	216	3355	216	3502	216	mA	
I_{DD3NA}	3241	216	3530	216	3716	216	mA	
I_{DD3P}	1791	216	1976	216	2045	216	mA	
I_{DD4R}	4485	216	4814	216	5124	216	mA	
I_{DD4RA}	4544	216	4882	216	5208	216	mA	
I_{DD4RB}	4507	216	4839	216	5155	216	mA	
I_{DD4W}	4498	216	4833	216	5147	216	mA	
I_{DD4WA}	4563	216	4904	216	5226	216	mA	
I_{DD4WB}	4498	216	4833	216	5145	216	mA	
I_{DD4WC}	4456	216	4726	216	5019	216	mA	
I_{DD4W_par}	4643	216	5005	216	5317	216	mA	
I_{DD5B}	5556	486	5758	486	5827	486	mA	
I_{DD5F2}	4600	432	4794	432	4866	432	mA	
I_{DD5F4}	4231	414	4421	414	4465	414	mA	
I_{DD6N}	1345	288	1469	288	1472	288	mA	
I_{DD6E}	2094	360	2233	360	2236	360	mA	
I_{DD6R}	978	252	1083	252	1087	252	mA	
I_{DD6A}	1305	288	1404	288	1408	288	mA	
I_{DD7}	5924	306	6423	315	6931	315	mA	
I_{DD8}	567	216	653	216	657	216	mA	

NOTE :

1. DIMM IDD SPEC is based on the condition that de-actived rank(IDLE) is IDD2N. Please refer to Table20.
2. IDD current measure method and detail patterns are described on DDR4 component datasheet.
3. VDD and VDDQ are merged on module PCB (IDDQ values are not considered by Qoff condition)
4. DIMM IDD Values are calculated based on the component IDD spec and Register power.

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[Table 20] DIMM Rank Status

SEC DIMM	Operating Rank	The other Rank
I_{DD0}	I_{DD0}	I_{DD2N}
I_{DD1}	I_{DD1}	I_{DD2N}
I_{DD2P}	I_{DD2P}	I_{DD2P}
I_{DD2N}	I_{DD2N}	I_{DD2N}
I_{DD2Q}	I_{DD2Q}	I_{DD2Q}
I_{DD3P}	I_{DD3P}	I_{DD3P}
I_{DD3N}	I_{DD3N}	I_{DD3N}
I_{DD4R}	I_{DD4R}	I_{DD2N}
I_{DD4W}	I_{DD4W}	I_{DD2N}
I_{DD5B}	I_{DD5B}	I_{DD2N}
I_{DD6}	I_{DD6}	I_{DD6}
I_{DD7}	I_{DD7}	I_{DD2N}
I_{DD8}	I_{DD8}	I_{DD8}

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15. Input/Output Capacitance

[Table 21] Silicon Pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		Unit	NOTE
		min	max	min	max		
C_{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	pF	1,3,4
C_{I}	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	pF	1,3,12
C_{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	pF	1,3,13

NOTE:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.
2. DQ, DM_n, DQS_T, DQS_c, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK_T-CK_C
5. Absolute value of CIO(DQS_T)-CIO (DQS_c)
6. CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. CDI CTRL applies to ODT, CS_n and CKE
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))
9. CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_c))
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case C_{TEN} might not be valid and system shall verify TEN signal with Vendor specific information.

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16. Electrical Characterisitics and AC Timing

16.1 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

[Table 22] DDR4-1600 Speed Bins and Operations

Speed Bin				DDR4-1600		Unit	NOTE
CL-nRCD-nRP				11-11-11			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.75[13] (13.50)[5,11]	18.00	ns	11
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	11
ACT to internal read or write delay time			tRCD	13.75[13] (13.50)[5,11]	-	ns	11
PRE command period			tRP	13.75[13] (13.50)[5,11]	-	ns	11
ACT to PRE command period			tRAS	35	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	48.75 (48.50)[5,11]	-	ns	11
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional)[5,11]	1.6	ns	1,2,3,4,10,13
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings				9,11,12		nCK	12,13
Supported CL Settings with read DBI				11,13,14		nCK	12
Supported CWL Settings				9,11		nCK	

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[Table 23] DDR4-1866 Speed Bins and Operations

Speed Bin				DDR4-1866		Unit	NOTE
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.92[13] (13.50)[5,11]	18.00	ns	11
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	11
ACT to internal read or write delay time			tRCD	13.92[13] (13.50)[5,11]	-	ns	11
PRE command period			tRP	13.92[13] (13.50)[5,11]	-	ns	11
ACT to PRE command period			tRAS	34	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	47.92 (47.50)[5,11]	-	ns	11
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional)[5,11]	1.6	ns	1,2,3,4,10,13
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional)[5,11]	<1.5	ns	1,2,3,4,6
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings				9,11,12,13,14		nCK	12,13
Supported CL Settings with read DBI				11,13,14,15,16		nCK	12
Supported CWL Settings				9,10,11,12		nCK	

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[Table 24] DDR4-2133 Speed Bins and Operations

Speed Bin				DDR4-2133		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.06[13] (13.75)[5,11]	18.00	ns	11
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal read or write delay time			tRCD	14.06 (13.75)[5,11]	-	ns	11
PRE command period			tRP	14.06 (13.75)[5,11]	-	ns	11
ACT to PRE command period			tRAS	33	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	47.06 (46.75)[5,11]	-	ns	11
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional)[5,11]	1.6	ns	1,2,3,4,10,13
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,10
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional)[5,11]	<1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071 (Optional)[5,11]	<1.25	ns	1,2,3,4,7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3
Supported CL Settings				9,11.12,13,14,15,16		nCK	12,13
Supported CL Settings with read DBI				11,13,14,15,16,18,19		nCK	
Supported CWL Settings				9,10,11,12,14		nCK	

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[Table 25] DDR4-2400 Speed Bins and Operations

Speed Bin				DDR4-2400		Unit	NOTE
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.16 (13.75)[5,11]	18.00	ns	11
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal read or write delay time			tRCD	14.16 (13.75)[5,11]	-	ns	11
PRE command period			tRP	14.16 (13.75)[5,11]	-	ns	11
ACT to PRE command period			tRAS	32	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	46.16 (45.75)[5,11]	-	ns	11
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,9
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
				(Optional)[5,11]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
				(Optional)[5,11]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
				(Optional)[5,11]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937		
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18		nCK	12,13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21		nCK	
Supported CWL Settings				9,10,11,12,14,16		nCK	

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[Table 26] DDR4-2666 Speed Bins and Operations

Speed Bin				DDR4-2666		Unit	NOTE
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.25[14] (13.75)[5,12]	18.00	ns	11
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) + 3nCK	ns	11
ACT to internal read or write delay time			tRCD	14.25 (13.75)[5,12]	-	ns	11
PRE command period			tRP	14.25[14] (13.75)[5,12]	-	ns	11
ACT to PRE command period			tRAS	32	9 x tREFI	ns	11
ACT to ACT or REF command period			tRC	46.25 (45.75)[5,12]	-	ns	11
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,10
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
				(Optional)[5,12]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
				(Optional)[5,12]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
				(Optional)[5,12]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
				(Optional)[5,12]			1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
CWL = 14.18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20		nCK	12
Supported CL Settings with read DBI				12,13,14,15,17,18,19,20,21,22,23		nCK	
Supported CWL Settings				9,10,11,12,14,16,18		nCK	

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16.2 Speed Bin Table Note

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133,2400 and 2666 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 13.5.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071ns or 0.937ns or 0.833ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
10. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
11. Parameters apply from tCK(avg) min to tCK(avg) max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
12. CL number in parentheses, it means that these numbers are optional.
13. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
14. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

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17. Timing Parameters by Speed Grade

[Table 27] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2666

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing													
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	0.750	<0.833	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_tot tCK(avg)m ax + tJIT(per)max_tot										tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	-38	38	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	-19	19	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	-30	30	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	125	-	107	-	94	-	83	-	75	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	100	-	86	-	75	-	67	-	60	ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	-55	55	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	-66	66	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	-73	73	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	-78	78	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	-83	83	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	-87	87	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	-91	91	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	-94	94	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	-96	96	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	-99	99	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	-101	101	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	-103	103	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	-104	104	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	-106	106	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	-108	108	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	-110	110	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	-112	112	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	^{t}ERR(nper)min = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total min) ^{t}ERR(nper)max = ((1 + 0.68ln(n)) * ^{t}JIT(per)_total max)										ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	TBD	-	ps	
Command and Address setup time to CK_t,CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	TBD	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	TBD	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	TBD	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	385	-	ps	
Command and Address Timing													
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.625 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,5ns)		Max(4nCK,4.2ns)		Max(4nCK,3.7ns)		Max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	nCK	34

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,5ns)		Max(4nCK,4.2ns)		Max(4nCK,3.7ns)		Max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7.5ns)		Max(4nCK,6.4ns)		Max(4nCK,6.4ns)		Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6ns)		Max(4nCK,5.3ns)		Max(4nCK,5.3ns)		Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,6ns)		Max(4nCK,5.3ns)		Max(4nCK,5.3ns)		Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,35ns)		Max(28nCK,30ns)		Max(28nCK,30ns)		Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,25ns)		Max(20nCK,23ns)		Max(20nCK,21ns)		Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,20ns)		Max(16nCK,17ns)		Max(16nCK,15ns)		Max(16nCK,13ns)	-	Max(16nCK,12ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max (2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-	ns	1,2,e,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-		1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5 ns)	-	max (4nCK,7.5 ns)	-		34
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (4nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+ max (4nCK,3.75ns)	-	tWTR_S+ max (5nCK,3.75ns)	-	tWTR_S+ max (5nCK,3.75ns)	-	tWTR_S+ max (5nCK,3.75ns)	-	tWTR_S+ max (5nCK,3.75ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+ max (4nCK,3.75ns)	-	tWTR_L+ max (5nCK,3.75ns)	-	tWTR_L+ max (5nCK,3.75ns)	-	tWTR_L+ max (5nCK,3.75ns)	-	tWTR_L+ max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	854	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))										nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency													
CS_n to Command Address Latency	tCAL	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	max(3nCK, 3.748 ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
DRAM Data Timing													
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.17	-	0.18	tCK(avg)/2	13,18,39,49
DQ output hold time per group, per access from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	0.74	-	tCK(avg)/2	13,17,18,39,49
Data Valid Window per device per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	TBD	-	UI	17,18,39,49
Data Valid Window, per pin per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	0.72	-	UI	17,18,39,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-390	180	-330	175	-310	170	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	-	175	-	170	ps	39
Data Strobe Timing													
DQS_t, DQS_c differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	0.9	NOTE 44	0.9	NOTE 44	tCK	39,40

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	1.8	NOTE 44	1.8	NOTE 44	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	39
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	tWPRE2	NA		NA		NA		1.8	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-330	175	-310	170	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	-	170	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	-175	175	-170	170	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		370		330		310		290		270	ps	37,38,39
MPSM Timing													
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	TBD	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	TBD	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	TBD	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	TBD	-		
CS setup time to CKE	tMPX_S	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	TBD	-		
Calibration Timing													
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing													
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK	

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max (5nCK,10 ns)	-	max (5nCK,10 ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10 ns)+PL	-	max (5nCK,10 ns)+PL	-	max (5nCK,10 ns)+PL	-	max (5nCK,10 ns)+PL	-	max (5nCK,10 ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max (5nCK,10 ns)	-	max (5nCK,10 ns)	-	nCK	
Power Down Timing													
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	nCK	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	nCK	
PDA Timing													
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		tMOD		nCK	
ODT Timing													
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing													
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	0	2	ns	
CA Parity Timing													
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	80	160	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64		71	nCK	
Parity Latency	PL	4		4		4		5		5		nCK	
CRC Error Reporting													
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	6	10	nCK	
Geardown timing													
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	-	-	-	-	-	-	-	-	TBD			
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-	-	-	-	-	-	-	-	TBD			
MRS command to Sync pulse time(T3)	tSYNC_GEAR	-	-	-	-	-	-	-	-	TBD	-		27
Sync pulse to First valid command(T4)	tCMD_GEAR	-	-	-	-	-	-	-	-	TBD			27
Geardown setup time	tGEAR_setup	-	-	-	-	-	-	-	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	-	-	-	-	-	-	2	-	nCK	
tREFI													
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	260	-	260	-	ns	34

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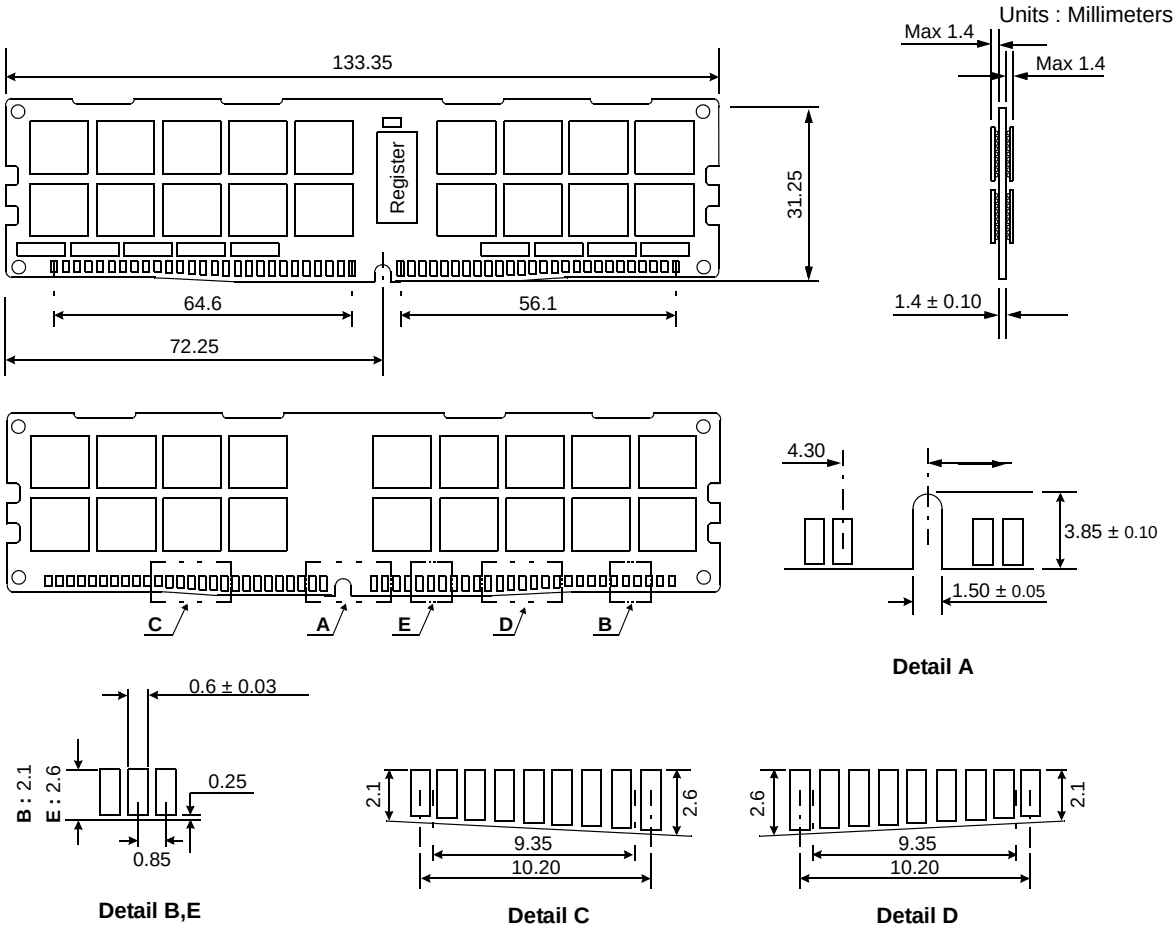
NOTE :

1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK following rounding algorithm defined in "13.5 Rounding Algorithms".
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables shown in section 10.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
    UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM
39. Value is only valid for RZQ/7 RONNOM = 34 ohms
40. 1tCK toggle mode with setting MR4:A11 to 0
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666 speed grade.
42. 1tCK mode with setting MR4:A12 to 0
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. Relationship". Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.

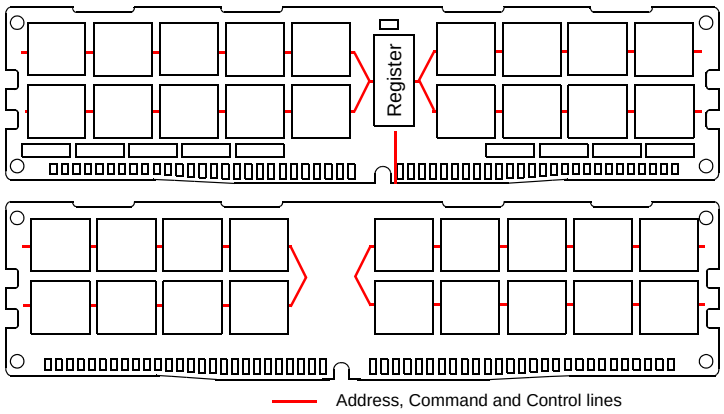
Micron Technology Inc. et al.
Ex. 1044, p. 293

18. Physical Dimensions

18.1 4Gbx4(DDP) based 8Gx72 Module (4 Ranks) - M386A8K40BM1/M386A8K40BM2



18.1.1 x72 DIMM, populated as Quad physical ranks of x4 DDR4 SDRAMs



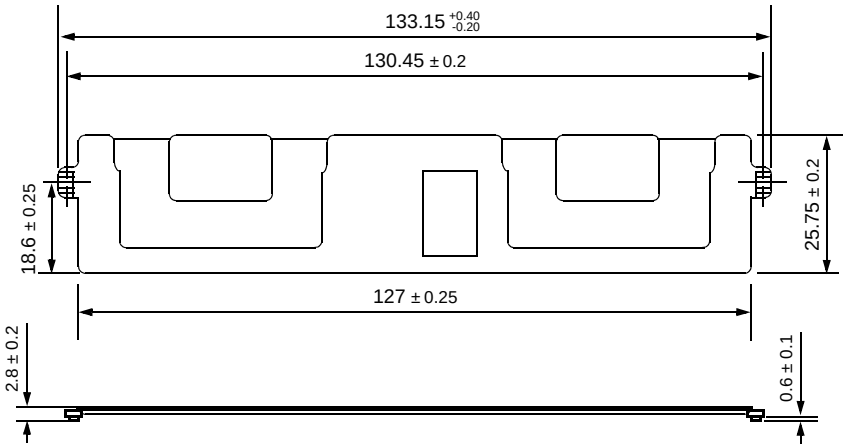
The used device is 4G x4(DDP) DDR4 SDRAM, FBGA.
DDR4 SDRAM Part NO: K4AAG045WB-MC**

* **NOTE** : Tolerances on all dimensions ±0.15 unless otherwise specified.

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Ex. 1044, p. 294

18.1.2 Heat Spreader Design Guide

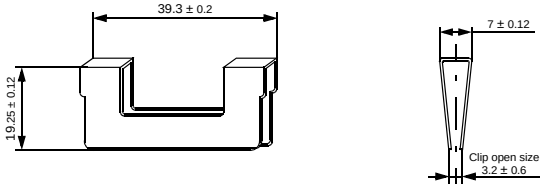
1. FRONT PART



2. BACK PART



3. CLIP PART



4. DDR4 RDIMM ASS'Y View

Reference thickness total (Maximum) : 7.30 (With Clip thickness)

H/S Assay



H/S, Clip Assay



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Exhibit 9

JEDEC STANDARD

DDR4 Data Buffer Definition (DDR4DB02)

JESD82-32A

(Revision of JESD82-32, November 2016)

AUGUST 2019

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



Figure 2 shows the timing sequence for a Write command.

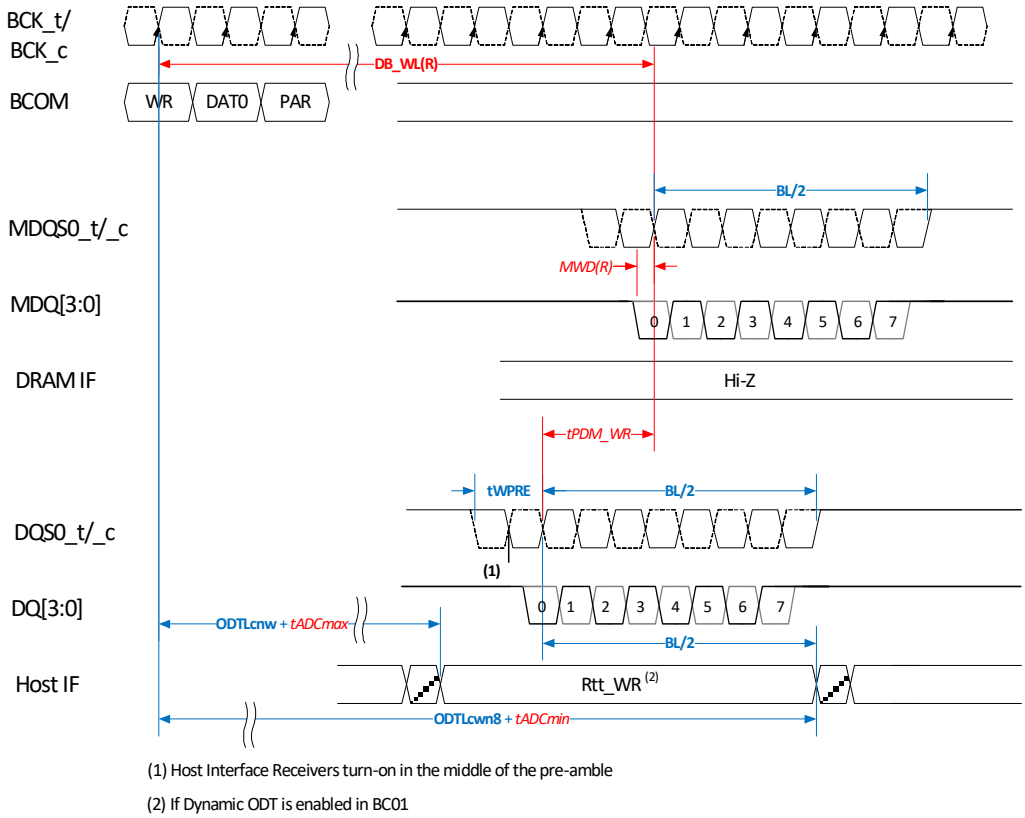


Figure 2 — WRITE Timing

2.14 Read Commands and MPR Override Reads

Table 5 shows the sequence for read (RD4, RD8) commands. Each read command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. The BCOM[2] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the DB if the BL field in the MR0 snoop register is set for fixed burst length of 8 or 4 (A[1:0] = '00' or

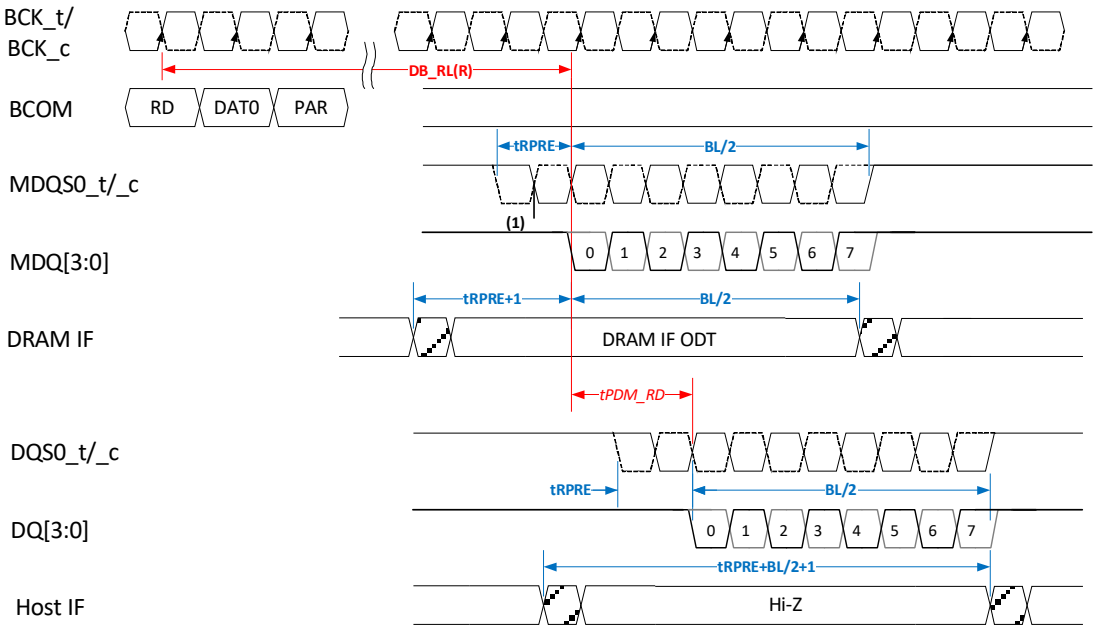
'10').

Table 5 — Multi-cycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:0] = {0, 0} for BC4[1] BCOM[3:0] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

1. BC4 is not supported for MPR override reads

Figure 3 shows the timing sequence for a Read command.



(1) DRAM Interface Receivers turn-on in the middle of the pre-amble

Figure 3 — READ Timing

4.61 Logic Diagram

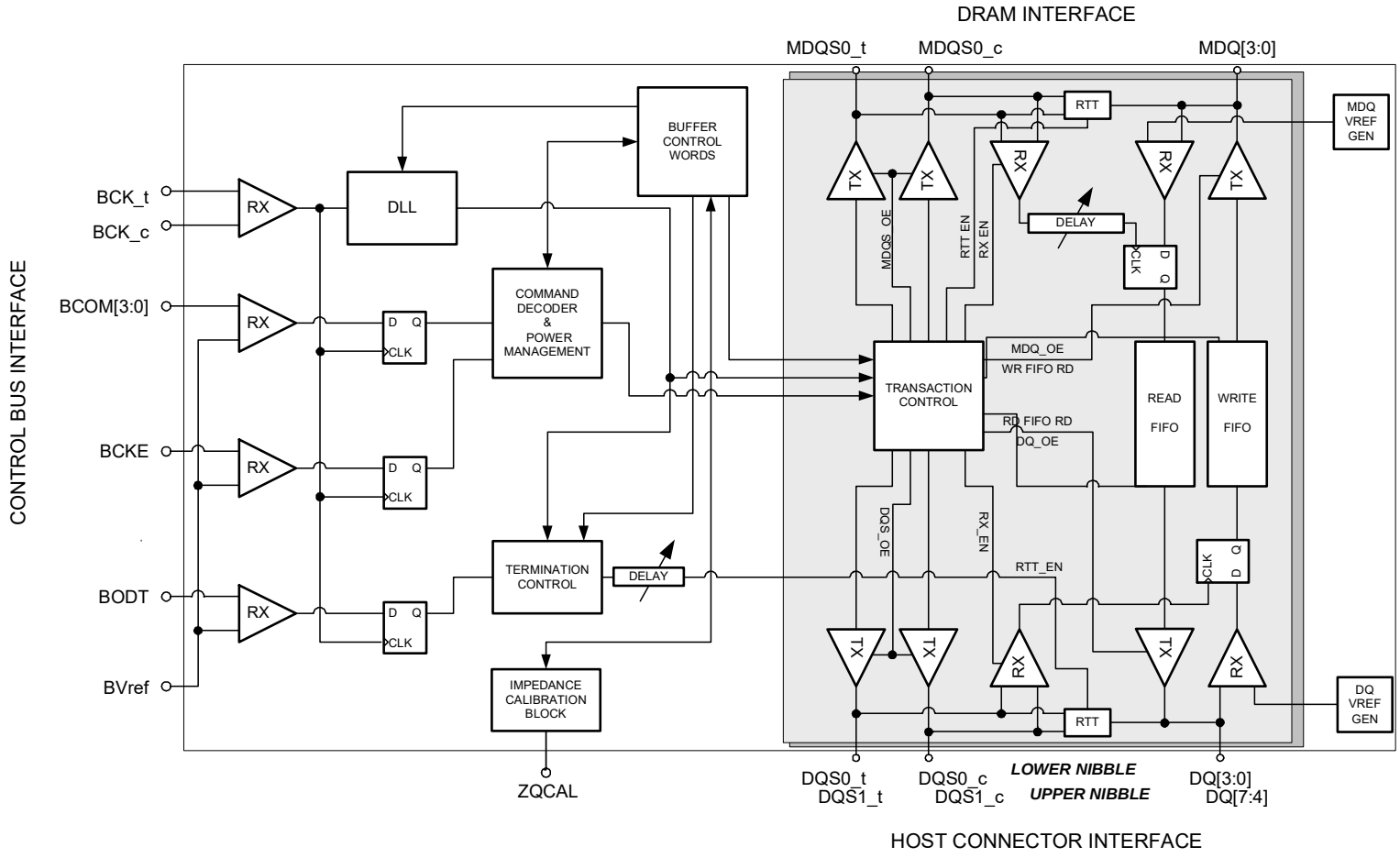


Figure 15 — Logic Diagram

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Page 95

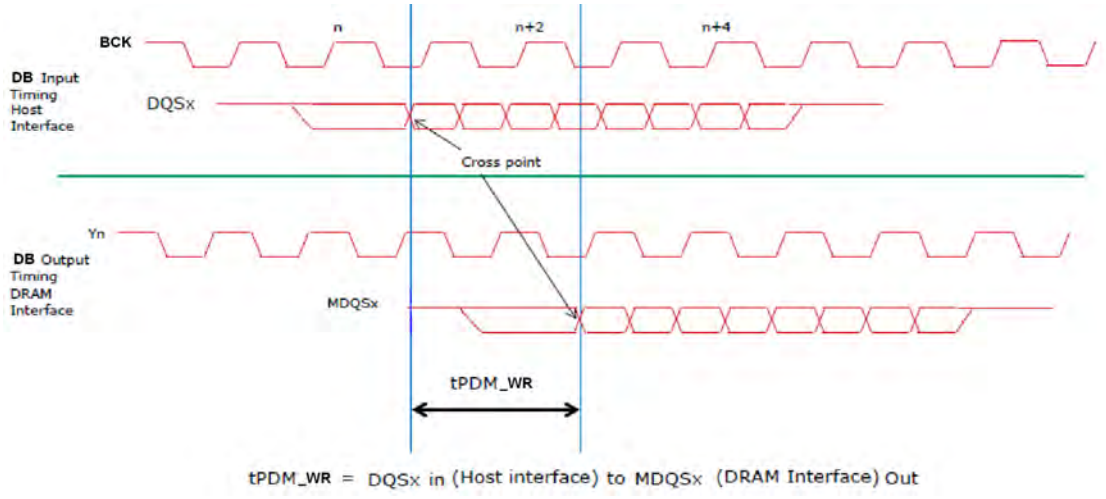


Figure 56 — tPDM_WR Latency Measurement

Table 144 — Output timing requirements in Package Rank Alignment Mode

Symbol	Parameter	Conditions		Min	Max	Unit
$t_{PDM\_RD\_RA}$[1]	MDQS to DQS Propagation Delay	1.2 V Operation[2,3]	Lower Nibble[4]	-	1.67 + tCK/4 + X(R)[5]	ns
			Upper Nibble[4]	-	1.67 + tCK/4 + Y(R)[6]	ns
$t_{PDM\_WR\_RA}$[1]	DQS to MDQS Propagation Delay	1.2 V Operation[2,3]	Lower Nibble[4]	-	1.67 + tCK/4 + Z(R)[7]	ns
			Upper Nibble[4]	-	1.67 + tCK/4 + W(R)[8]	ns

1. Applies when Package Rank Alignment mode is enabled (F0BC1x DA7 = 1). Package Rank Alignment granularity is 1/64*tCK. Upper Nibble and Lower Nibble are not required to be aligned by DDR4DB02.
2. These parameters are only guaranteed after the correct speed range has been programmed in BC0A
3. These timings are only valid with the DA[5:0] bits of the lower and upper nibble read delay and write delay control words (F[3:0]BC4x, F[3:0]BC5x, F[3:0]BC8x and F[3:0]BC9x) at their power on default of 6b'000000 and default slew rate control setting of BC0B DA[3:2] = 00.
4. Maximum temperature and voltage drift must be 170 ps or less for respective nibble.
5. The value of X is rank dependent and it is equal to the difference between MAX(F[3:0]BC2x) and the value of the Fn-BC2x corresponding to each rank. For example, for the earliest rank X = [MAX(F[3:0]BC2x) - MIN(F[3:0]BC2x)], and for the latest rank X = 0. DDR4DB02 supports the largest value of X of 500 ps.
6. The value of Y is rank dependent and it is equal to the difference between MAX(F[3:0]BC3x) and the value of the Fn-BC3x corresponding to each rank. For example, for the earliest rank Y = [MAX(F[3:0]BC3x) - MIN(F[3:0]BC3x)], and for the latest rank Y = 0. DDR4DB02 supports the largest value of Y of 500 ps.
7. The value of Z is rank dependent and it is equal to the difference between MIN(F[3:0]BCAx) and the value of the Fn-BCAx corresponding to each rank. For example, for the latest rank Z = [MAX(F[3:0]BCAx) - MIN(F[3:0]BCAx)], and for the earliest rank Z = 0. DDR4DB02 supports the largest value of Z of 500 ps.
8. The value of W is rank dependent and it is equal to the difference between MIN(F[3:0]BCBx) and the value of the Fn-BCBx corresponding to each rank. For example, for the latest rank W = [MAX(F[3:0]BCBx) - MIN(F[3:0]BCBx)], and for the earliest rank W = 0. DDR4DB02 supports the largest value of W of 500 ps.

Table 146 — WRITE Output Timings

		DDR4-1600/ 1866/2133		DDR4-2400/ 2666		DDR4- 2933		DDR4-3200		Units	Notes
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Data Timing											
tDVB	Data valid before MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
tDVA	Data valid after MDQS	0.38	-	0.36	-	0.36	-	0.36	-	UI	
Data Strobe Timing											
MDQS_t - MDQS_c differential output low time	tMQSL	0.46	-	0.46	-	0.46	-	0.46	-	tCK	1, 3
MDQS_t - MDQS_c differential output high time	tMQSH	0.46	-	0.46	-	0.46	-	0.46	-	tCK	2, 3

Unit UI = tCK(avg).min/2

NOTE 1: tMQSL describes the instantaneous differential output low pulse width on MDQS_t - MDQS_c, as measured from on falling edge to the next consecutive rising edge

NOTE 2: tMQSH describes the instantaneous differential output high pulse width on MDQS_t - MDQS_c, as measured from on rising edge to the next consecutive falling edge

NOTE 3: The specification values are affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.). However, these parameters should be met whether clock jitter is present or not.

10.6 Package Rank to Package Rank Timing Requirements

Table 147 — DDR4DB02 Operating Spec for Different Package Ranks

		DDR4-1600 to 2400		DDR4-2666/2933		DDR4 -3200			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
TRDRD	Read to Read Command Spacing	tRPRE + BL/2 + 1.8	-	tRPRE + BL/2 + 1.8	-	tRPRE + BL/2 + 1.8	-	tCK(avg)	1, 2, 4, 8
TWRWR	Write to Write Command Spacing	tWPRE + BL/2 + 1.8	-	tWPRE + BL/2 + 1.8	-	tWPRE + BL/2 + 1.8	-	tCK(avg)	1, 2, 5, 8
TRDWR	Read to Write Command Spacing	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 2.7 + (CL - CWL)	-	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 2.7+ (CL - CWL)	-	tPDM_RD + tPDM_WR + tWRPRE + tRPRE/2 + BL/2 + 2.7 + (CL - CWL)	-	tCK(avg)	1, 2, 3, 6, 8
TWRRD	Write to Read Command Spacing	tRPRE/2 + BL/2 + 2.7 - (CL - CWL)	-	tRPRE/2 + BL/2 + 2.7 - (CL - CWL)	-	tRPRE/2 + BL/2 + 2.7- (CL - CWL)	-	tCK(avg)	1, 2, 7, 8

Notes:
1. DDR4DB02 will guarantee the functionality with this minimum command spacing.
2. For operation to same package rank, this restriction does not apply. Host controller follows DRAM JESD79-4 Specification. DDR4DB02 will guarantee the functionality in accordance with DRAM JESD79-4 Specification.
3. This is meant for DDR4DB02 testing on ATE environment purpose to ensure proper buffer functionality. Host controller is likely to require additional separation to avoid the bus contention on Host controller and buffer input interface under normal operation.

Exhibit 10

JEDEC STANDARD

DDR4 SDRAM

JESD79-4C

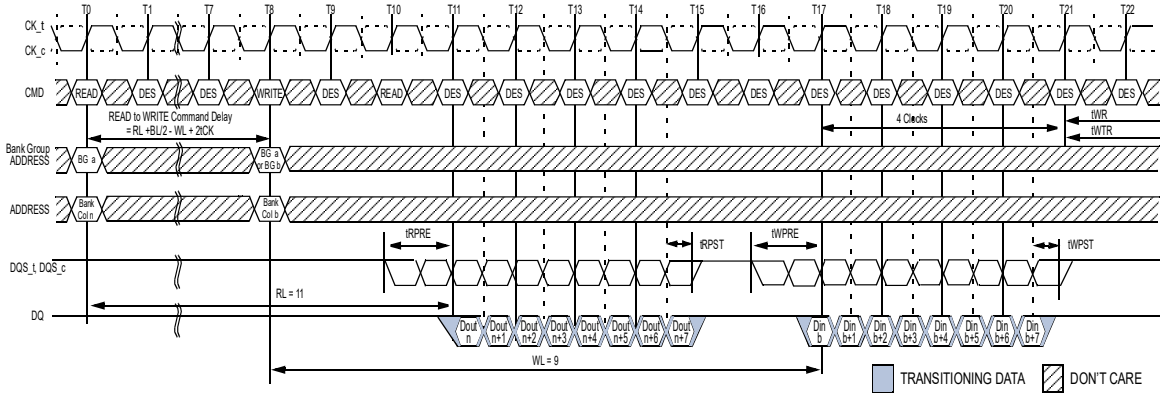
(Revision of JESD79-4B, June 2017)

JANUARY 2020

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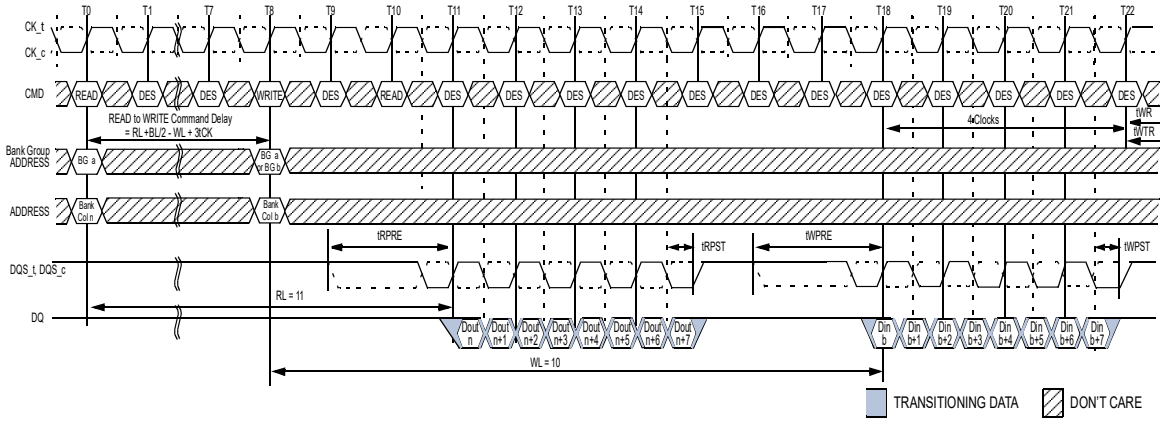


4.24.2 READ Burst Operation (cont'd)



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 98 — READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
NOTE 5 When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
NOTE 6 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 99 — READ (BL8) to WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group

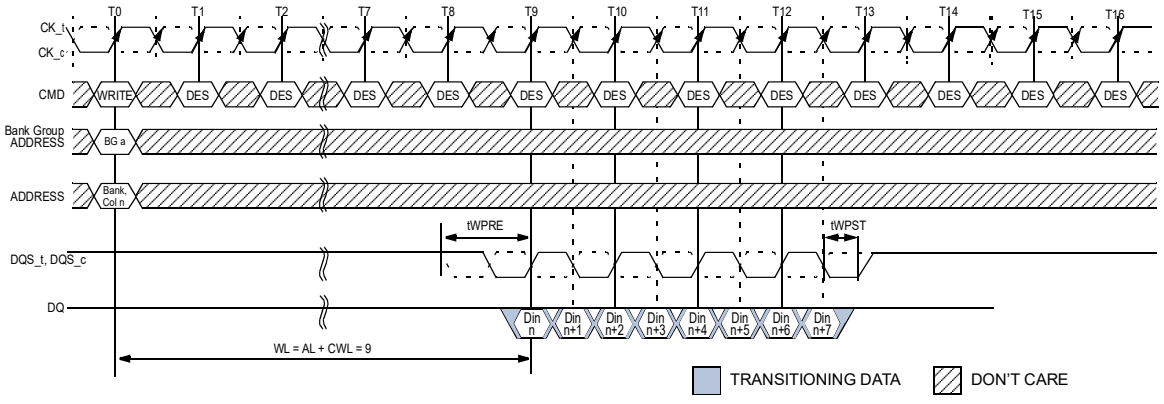
4.25.4 tWPST Calculation (cont'd)

Table 84 — Timing Parameters by Speed Grade

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c differential WRITE Preamble (1tCK Preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)	
DQS_t, DQS_c differential WRITE Preamble (2tCK Preamble)	tWPRE2	-	-	-	-	-	-	-	-	tCK(avg)	
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK(avg)	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
DQS_t, DQS_c differential input high pulse width at 2tCK Preamble	tDQSH2PRE	-	-	-	-	-	-	-	-	tCK(avg)	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1tCK Preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK(avg)	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK(avg)	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK(avg)	

4.25.5 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.



NOTE 1 BL = 8, WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
NOTE 2 DIN n = data-in to column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

Figure 128 — WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)

Exhibit 11

4.20.27 - 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/
PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification

DDR4 SDRAM Load Reduced DIMM Design Specification

Revision 1.00

August 2015

Micron Technology Inc. et al.
Ex. 1044, p. 308

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM timing-critical signals into seven groups. Figure 3 summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. The signal groups are:

1. DQ and DQS signals connector to Data Buffer (DB)
2. DQ and DQS signals DB to SDRAM
3. PreRegister ADD/CMD and CTRL
4. PreRegister CK
5. PostRegister ADD/CMD
6. PostRegister Control
7. PostRegister CK
8. PostRegister BCOM, BODT, BCKE
9. PostRegister BCK

The PreRegister ADD/CMD and CTRL group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, PARITY, CSx_n, CKEx, and ODTx.

The PostRegister ADD/CMD group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, and PARITY.

The PostRegister CTRL group includes CSx_n, CKEx, and ODTx.

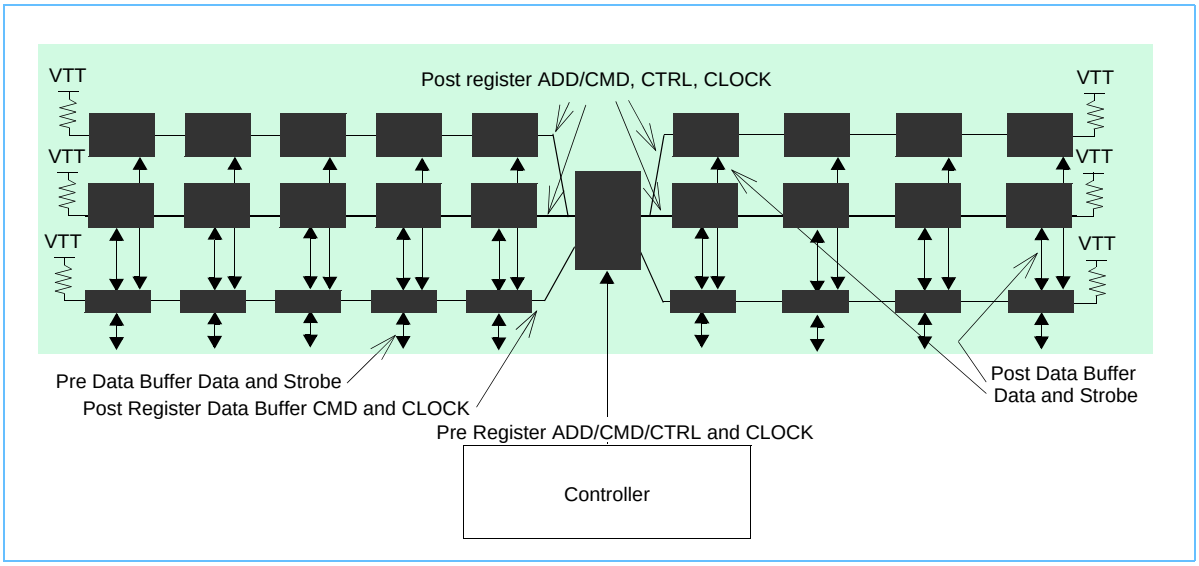


Figure 3 — LRDIMM Topologies

6.2 General Net Structure Routing Rules

The usual design process should be followed to develop an adequate design. Simulations are typically required and timing budgets considered to verify adequate performance. Documenting line lengths alone

Exhibit 12

Powering Experiences

Micron Technology Inc. et al.
Ex. 1044, p. 311

DDR5 ushers in data-centric innovation

DDR5 meets the demands of industries experiencing an enormous burst in data. A new level of speed, improved capacity, and bolstered reliability are packed into DDR5 to enhance overall system performance. Samsung's memory technology propels the next era of planet-friendly innovation with power-saving DDR5.

"As the amount of data to be moved, stored and processed increases exponentially, the transition to DDR5 comes at a critical inflection point for cloud datacenters, networks and edge deployments."

– Carolyn Duran
Vice President and GM of Memory and IO Technology
Intel

Breathtaking speed for huge real-time data

With exceptional transfer speeds of up to 7,200 megabits per second (Mbps), DDR5 effectively handles the ever-increasing demands of larger, more complex data workloads. DDR5 brings a 75% increase in performance compared to DDR4, with double the burst length from 8 to 16, and double the banks from 16 to 32. The astonishing performance raises the ceiling on AI workloads, while seamlessly handling big data.

Twice the capacity to fuel industry innovation

Samsung's 10nm-class process and EUV technology enable chip units to leap from 16Gb to 32Gb. Doubling chip capacity means one module can provide up to 512GB, to fluidly handle huge simultaneous workloads, with scalability for future innovation.

Micron Technology Inc. et al.
Ex. 1044, p. 313

Robust reliability with a self-correcting solution

On-die ECC (on-die error-correction code) technology applied in DDR5 helps maintain secure and stable data reliability, to fully leverage powerful performance. On-die ECC virtually eliminates single bit errors for enhanced reliability even with the strenuous demands of big data.

The energy-saving choice to sustain our planet

DDR5 achieves up to 30% greater power efficiency than DDR4 through improved performance and power reduction. Replacing a data center's DDR4 with DDR5 saves power of up to 1TWh annually. The on-DIMM PMIC further boosts power management efficiency and power supply stability. It is the all-around sustainable choice for our environment.

Exhibit 13

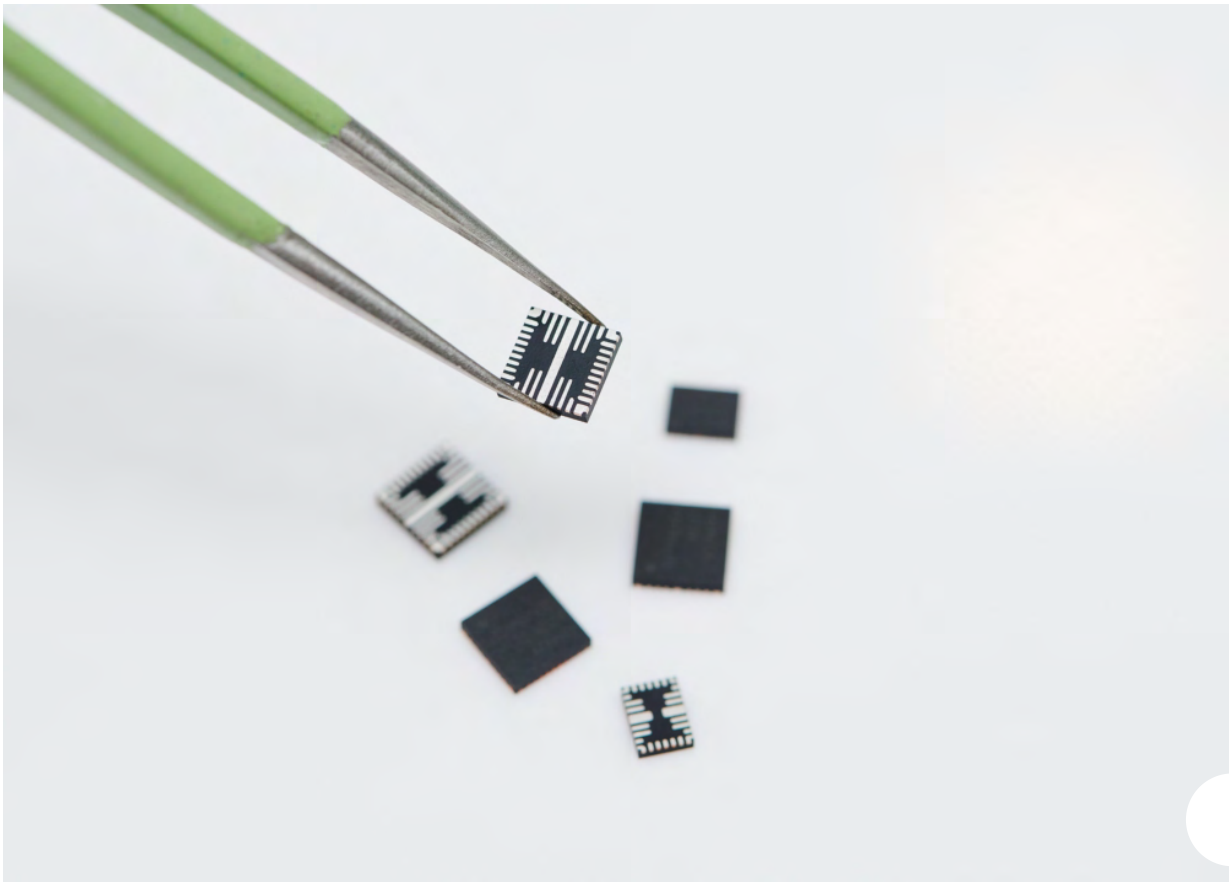
Samsung
Newsroom

Samsung Unveils New Power Management Solutions for DDR5 Modules

Korea on May 18, 2021

Samsung's two new enterprise PMICs, S2FPD01 and S2FPD02, can reduce overheating with more than 90% energy-efficiency within the memory module

The S2FPC01 offers power-saving benefits to PC DRAM modules in a compact form factor



management ICs (PMICs) – S2FPD01, S2FPD02 and S2FPC01, for the fifth generation double data rate (DDR5) dual in-line memory module (DIMM).

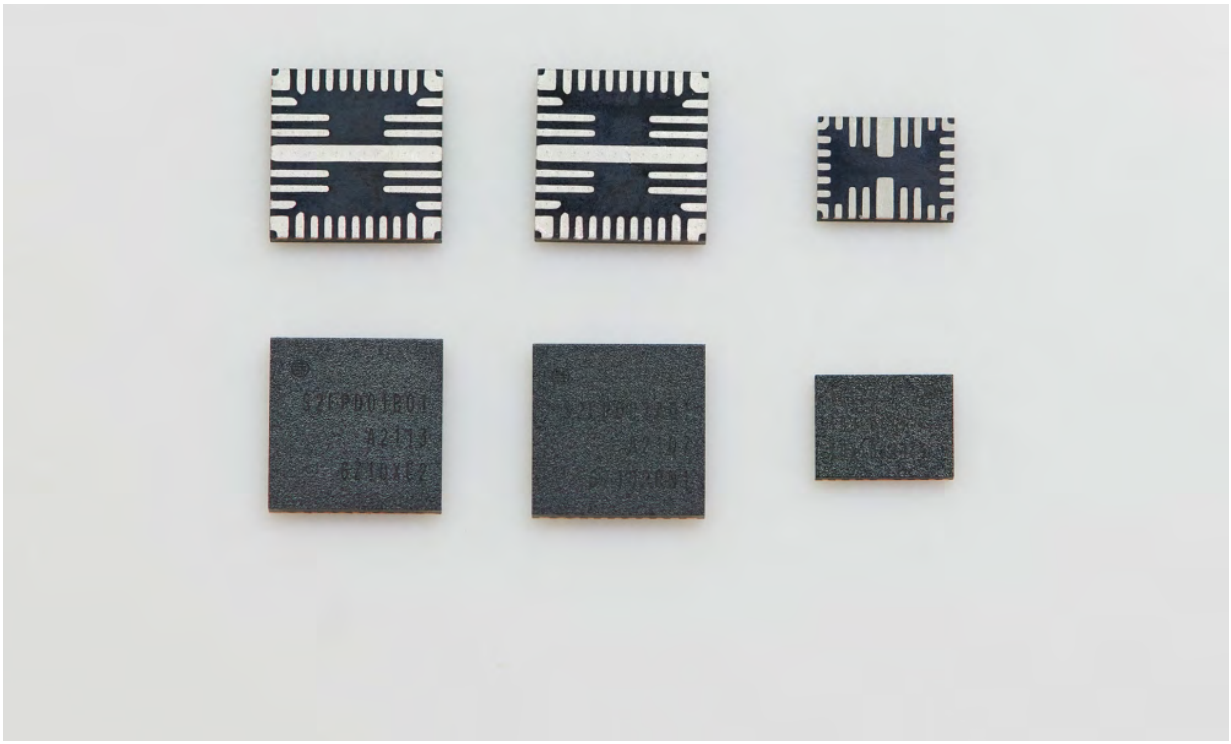
One major design improvement to the newest generation DRAM solution involves integrating the PMIC into the memory module – previous generations placed the PMIC on the motherboard – offering increased compatibility and signal integrity, and providing a more reliable and sustained performance.

For improved performance efficiency and load-transient responses, Samsung's new PMICs for DDR5 modules have been equipped with a high-efficiency hybrid gate driver and a proprietary control design (asynchronous-based dual-phase buck control scheme).

This scheme allows the DC voltage to step down from high to low with a fast transient response to changes in the output load current and adapts the conversion accordingly to efficiently regulate its output voltage at near-constant levels. The control scheme also features both pulse width and pulse frequency modulation methods, preventing delays and malfunctions when switching modes.

"With enhanced power efficiency and low output ripple voltage, the new PMICs S2FPD01, S2FPD02 and S2FPC01 allow data centers, enterprise servers and PC applications to take full advantage of their DDR5 performance for highly demanding, memory-intensive tasks," said Harry Cho, vice president of System LSI marketing at Samsung Electronics.

Samsung
Newsroom



Two of Samsung's new DDR5 DIMM PMIC solutions, the S2FPD01 and the S2FPD02, offer optimal performance for today's data center and enterprise servers that must run heavy analytics, machine and deep learning, and other various computing tasks in real time. The FPD01 is designed for modules with low density; FPD02 for higher density.

In addition, by implementing a high-efficiency hybrid gate driver instead of a linear regulator, Samsung's new PMICs can operate at up to 91-percent power efficiency.

The S2FPC01, Samsung's other new PMIC, is tailored for use in desktop or laptop PCs. Designed on a 90-nanometer (nm) process node, the PMIC solution offers a more agile performance in a smaller package.

Samsung's DDR5 DIMM power management ICs, the S2FPD01, S2FPD02 and

Micron Technology Inc. et al.
Ex. 1044, p. 319

JEDEC STANDARD

PMIC50x0 Power Management IC Specification, Rev 1.0

JESD301-1

JUNE 2020

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



7 Example Schematic

Figure 9 shows an example schematic when PMIC is configured in dual phase regulator mode. Table 26, “PMIC Schematic Values” shows all component details shown in the schematics. Note that capacitors C25, C26, C27, C29, C30, C31 represents the lump sum of distributed capacitance across the entire DIMM.

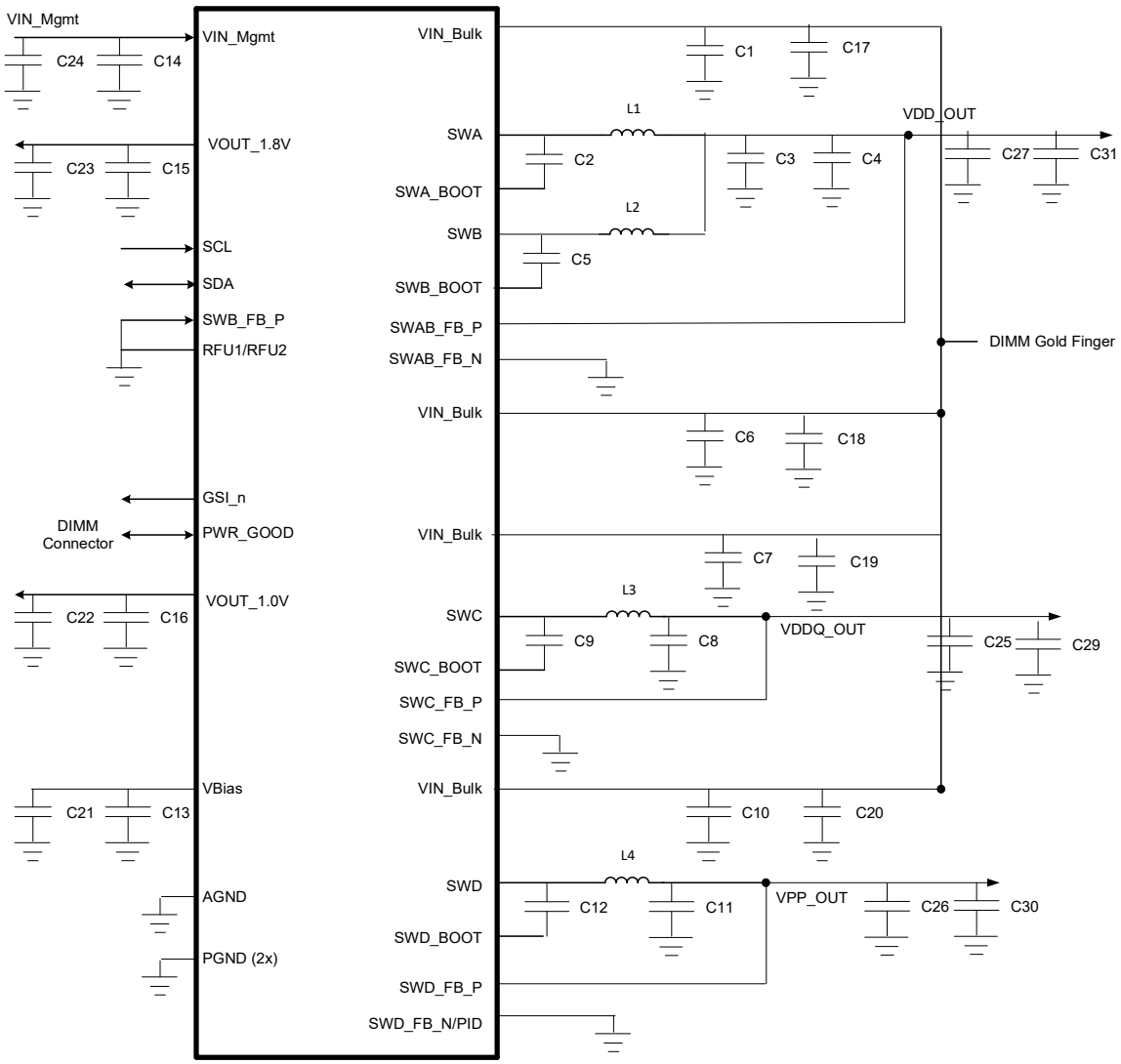


Figure 9 — Dual Phase Regulator Example Schematic

Figure 10 shows an example schematic when PMIC is configured in single phase regulator mode. Table 26, “PMIC Schematic Values” shows all component details shown in the schematics. Note that capacitors C25, C26, C27, C28, C29, C30, C31 and C32 represents the lump sum of distributed capacitance across the entire DIMM.

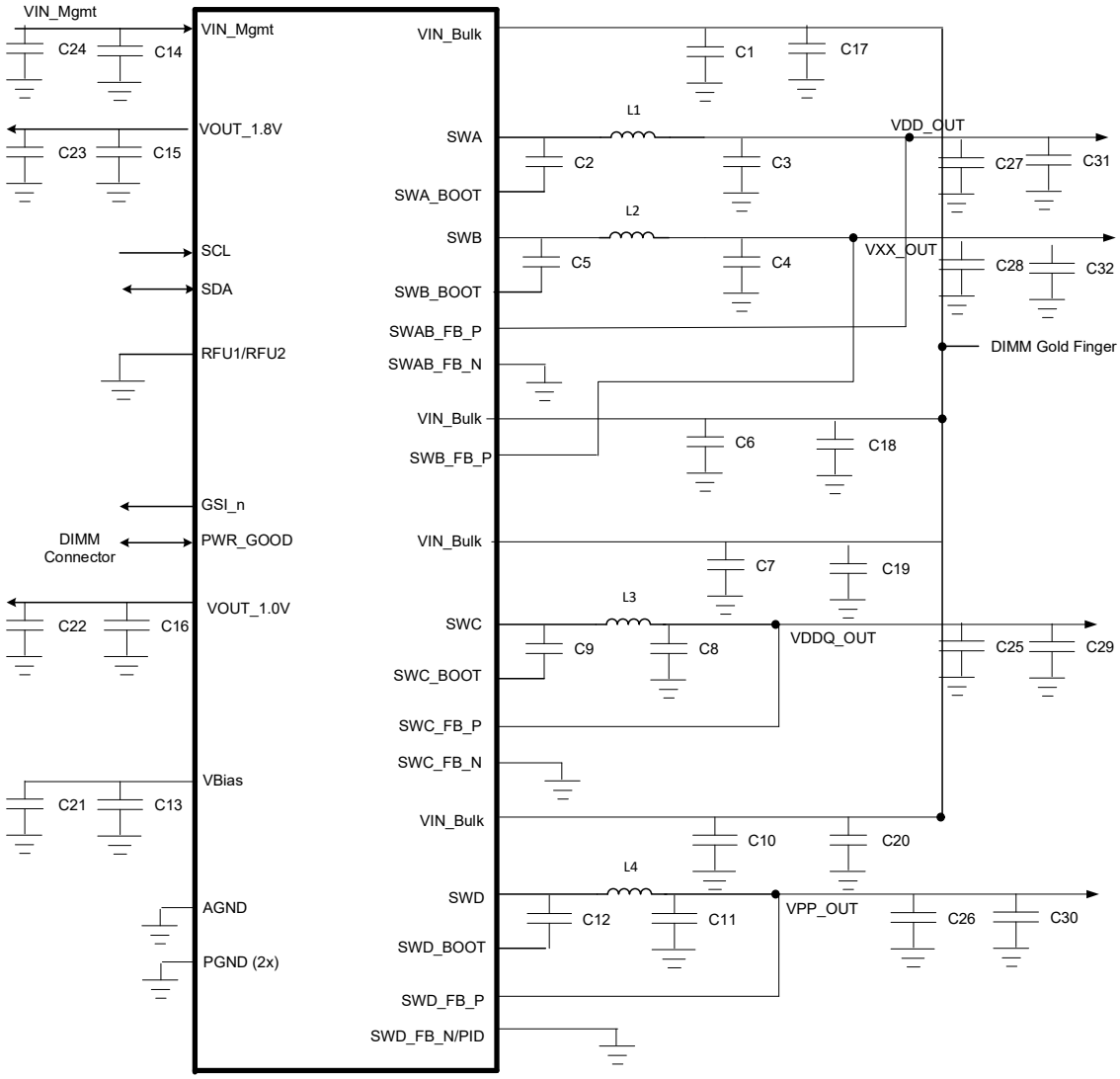


Figure 10 — Single Phase Regulator Example Schematic

Exhibit 15

JEDEC STANDARD

DDR5 SDRAM

JESD79-5

JULY 2020

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



DDR5 SDRAM STANDARD

(From JEDEC Board Ballot JCB-20-21, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

1 Scope

This document defines the DDR5 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 8Gb through 32Gb for x4, x8, and x16 DDR5 SDRAM devices. This standard was created based on the DDR4 standards (JESD79-4) and some aspects of the DDR, DDR2, DDR3 & LPDDR4 standards (JESD79, JESD79-2, JESD79-3 & JESD209-4).

1.1 JM7 Verbal Forms and Terms

JEDEC publication JM7 provides examples and directives for the use of verbal forms (e.g., 'shall' compared with 'should' and 'may' compared with 'can').'

This specification adheres to the verbal forms defined in JM7.01 July 2010 revision.

1.2 Significance of light grey Text in this Document

All light grey text is defined as something that should be considered TBD. The content may be accurate or the same as previous technologies but has not yet been reviewed or determined to be the working assumption.

LIGHT GREY - **All Light Grey text is defined as something that should be considered TBD. The content may be accurate or the same as previous technologies but has not yet been reviewed or determined to be the working assumption.**

2 DDR5 SDRAM Package, Pinout Description and Addressing

2.1 DDR5 SDRAM Row for X4, X8

The DDR5 SDRAM x4/x8 component shall have 13 electrical rows of balls. Electrical is defined as rows that contain signal ball or power/ground balls. There may be additional rows of inactive balls for mechanical support.

2.2 DDR5 SDRAM Ball Pitch

The DDR5 SDRAM component shall use a ball pitch of 0.8mm by 0.8mm.

The number of depopulated columns is 3.

2.3 DDR5 SDRAM Columns for X4, X8

The DDR5 SDRAM x4/x8 component shall have 6 electrical columns of balls in 2 sets of 3 columns.

There shall be columns between the electrical columns where there are no balls populated. The number of these is 3.

Electrical is defined as columns that contain signal ball or power/ground balls. There may be additional columns of inactive balls for mechanical support.

LIGHT GREY - **All Light Grey text is defined as something that should be considered TBD. The content may be accurate or the same as previous technologies but has not yet been reviewed or determined to be the working assumption.**

2.4 DDR5 SDRAM X4/8 Ballout using MO-210

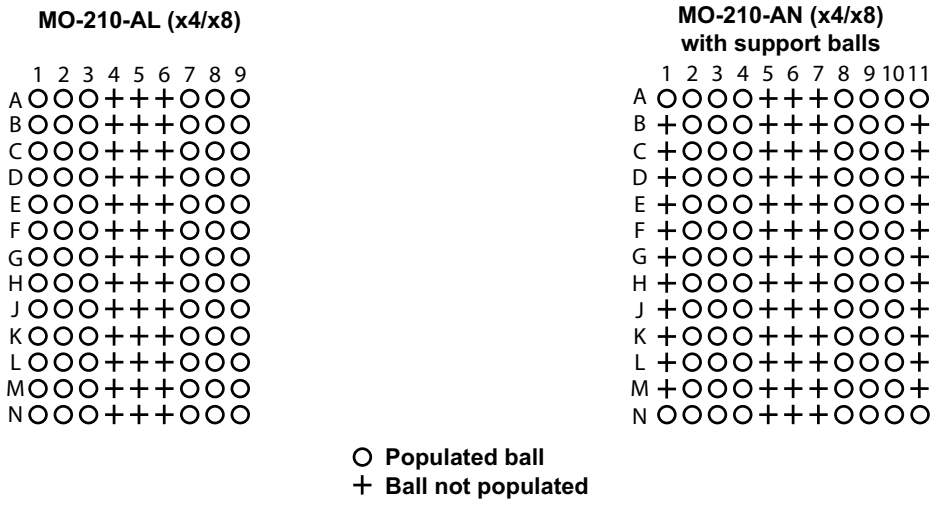
Table 1 provides the ballout for DDR5 SDRAM X4/8 using MO-210.

Table 1 — DDR5 SDRAM X4/8 Ballout Using MO-210

	1	2	3	4	5	6	7	8	9	
A	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	A
B	VDD	VDDQ	DQ2				DQ3	VDDQ	VDD	B
C	VSS	DQ0	DQS_t				DM_n, TDQS_t	DQ1	VSS	C
D	VDDQ	VSS	DQS_c				TDQS_c	VSS	VDDQ	D
E	VDD	DQ4	DQ6				DQ7	DQ5	VDD	E
F	VSS	VDDQ	VSS				VSS	VDDQ	VSS	F
G	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	G
H	ALERT_n	VSS	CS_n				CK_c	VSS	VDD	H
J	VDDQ	CA4	CA0				CA1	CA5	VDDQ	J
K	VDD	CA6	CA2				CA3	CA7	VDD	K
L	VDDQ	VSS	CA8				CA9	VSS	VDDQ	L
M	CAI	CA10	CA12				CA13	CA11	RESET_n	M
N	VDD	VSS	VDD				VPP	VSS	VDD	N

NOTE 1 DQ4-DQ7 are higher order DQ pins and are not connected for the x4 configuration.
NOTE 2 TDQS_t is not valid for the x4 configuration
NOTE 3 TDQS_c is not available for the x4 configuration
NOTE 4 DM_n not valid for the x4 configuration

Figure 1 provides the DDR5 Ball Assignments for the x4/8 component.



NOTE 1 Additional columns and rows of inactive balls in MO-210 Terminal Pattern TBD(x4/x8) with support balls are for mechanical support only, and should not be tied to either electrically high or low.
NOTE 2 Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.

Figure 1 — DDR5 Ball Assignments for the x4/8 component

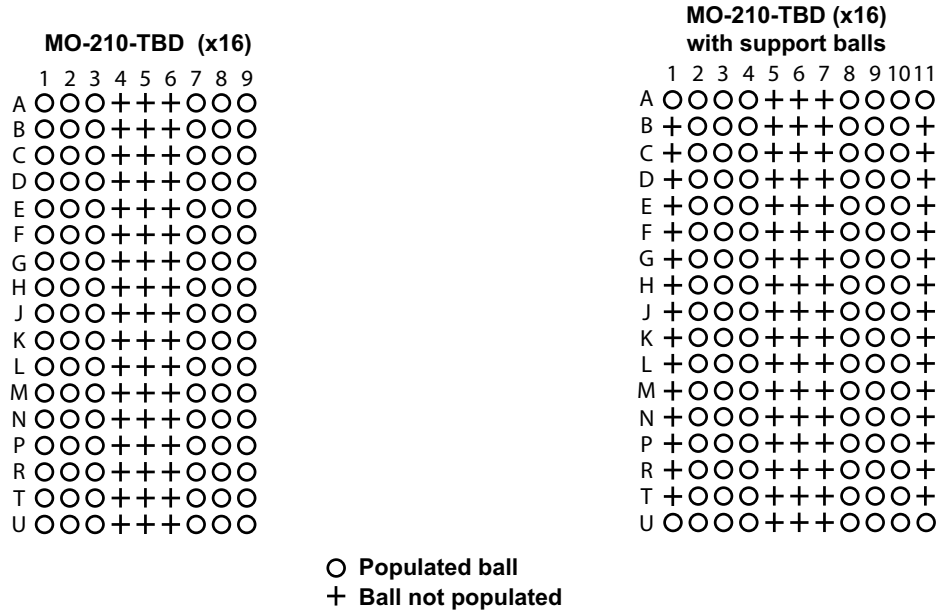
2.5 DDR5 SDRAM X16 Ballout uSing MO-210

Table 2 provides the DDR5 SDRAM X16 Ballout using MO-210.

Table 2 — DDR5 SDRAM X16 Ballout Using MO-210

	1	2	3	4	5	6	7	8	9	
A	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	A
B	VDD	VDDQ	DQU2				DQU3	VDDQ	VDD	B
C	VSS	DQU0	DQSU_t				DMU_n	DQU1	VSS	C
D	VDDQ	VSS	DQSU_c				RFU	VSS	VDDQ	D
E	VDD	DQU4	DQU6				DQU7	DQU5	VDD	E
F	VDD	VDDQ	DQL2				DQL3	VDDQ	VDD	F
G	VSS	DQL0	DQSL_t				DML_n	DQL1	VSS	G
H	VDDQ	VSS	DQSL_c				RFU	VSS	VDDQ	H
J	VDD	DQL4	DQL6				DQL7	DQL5	VDD	J
K	VSS	VDDQ	VSS				VSS	VDDQ	VSS	K
L	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	L
M	ALERT_n	VSS	CS_n				CK_c	VSS	VDD	M
N	VDDQ	CA4	CA0				CA1	CA5	VDDQ	N
P	VDD	CA6	CA2				CA3	CA7	VDD	P
R	VDDQ	VSS	CA8				CA9	VSS	VDDQ	R
T	CAI	CA10	CA12				CA13	CA11	RESET_n	T
U	VDD	VSS	VDD				VPP	VSS	VDD	U

Figure 2 provides the DDR5 Ball Assignments for the x16 component.



NOTE 1 Additional columns and rows of inactive balls in MO-210 Terminal Pattern TBD (x16) with support balls are for mechanical support only, and should not be tied to either electrically high or low.

NOTE 2 Some of the additional support balls can be selectively populated under the supplier's discretion. Refer to supplier's datasheet.

Figure 2 — DDR5 Ball Assignments for the x16 Component

2.6 Pinout Description

Table 3 provides the pinout descriptions.

Table 3 — Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CS_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DM_n, DMU_n, DML_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
CA [13:0]	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DDQ},
DQ	Input / Output	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via MR5:OP[4]=1, the DRAM shall enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via MR5:OP[4]=0, DM_n/TDQS_t shall provide the data mask function depending on MR5:OP[5]; TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via MR5:OP[4]=0.
ALERT_n	Input/Output	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to V_{DDQ} on board.
TEN	Input	Connectivity Test Mode Enable: Required on x4, x8 & x16 devices. HIGH in this pin shall enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of V_{DDQ}. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
MIR	Input	Mirror: Used to inform SDRAM device that it is being configured for Mirrored mode vs. Standard mode. With the MIR pin connected to VDDQ, the SDRAM internally swaps even numbered CA with the next higher odd number CA. Normally the MIR pin must be tied to VSSQ if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1) CA4 with CA5 (not CA3). Note that the CA[13] function is only relevant for certain densities (including stacking) of DRAM component. In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected to VDDQ
CAI	Input	Command & Address Inversion: With the CAI pin connected to VDDQ, DRAM internally inverts the logic level present on all the CA signals. Normally the CAI pin must be connected to VSSQ if no CA inversion is required.
CA_ODT	Input	ODT for Command and Address. Apply Group A settings if the pin is connected to VSS and apply Group B settings if the pin is connected to V_{DDQ}.
LBDQ	Output	Loopback Data Output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].

Table 3 — Pinout Description (Cont'd)

Symbol	Type	Function
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.1 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.1 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 1.8V
ZQ	Supply	Reference Pin for ZQ calibration

2.7 DDR5 SDRAM Addressing

Tables 4-8 provide the addressing for 8, 16, 24, 32, and 65 Gb.

Table 4 — 8 Gb Addressing Table

Configuration		2 Gb x4	1 Gb x8	512 Mb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0	BA0	BA0
	# BG / # Banks per BG / # Banks	8 / 2 / 16	8 / 2 / 16	4 / 2 / 8
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

Table 5 — 16 Gb Addressing Table

Configuration		4 Gb x4	2 Gb x8	1 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R15	R0~R15	R0~R15
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H

Table 6 — 24 Gb Addressing Table

Configuration		6 Gb x4	3 Gb x8	1.5 Gb x16
Bank Address	BG Address	BG0~BG2	BG0~BG2	BG0~BG1
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
	# BG / # Banks per BG / # Banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
Row Address		R0~R16	R0~ R16	R0~R16
Column Address		C0~C10	C0~C9	C0~C9
Page size		1KB	1KB	2KB
Chip IDs / Maximum Stack Height		CID0~3 / 16H	CID0~3 / 16H	CID0~3 / 16H
NOTE Row address R[16:15] of 00b, 01b, and 10b are valid. Row address R[16:15] of 11b is invalid.				

Exhibit 16

JEDEC STANDARD

DDR5 Registering Clock Driver Definition (DDR5RCD01)

JESD82-511

AUGUST 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



Micron Technology Inc. et al.
Ex. 1044, p. 332

DDR5 REGISTERING CLOCK DEFINITION (DDR5RCD01)

(From JEDEC Board Ballot JCB-20-46 and JCB-21-18, formulated under the cognizance of the JC-40.4 Subcommittee on Registered & Fully Buffered Memory Support Logic.)

1 Scope

This document defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the DDR5 Registering Clock Driver (RCD) with parity for driving address and control nets on DDR5 RDIMM and LRDIMM applications. The DDR5RCD01 Device ID is DID = 0x0051.

The terms ‘Registering Clock Driver’, ‘RCD’, ‘register’ or ‘device’ are used interchangeably to refer to this device in the remainder of this specification.

The purpose is to provide a standard for the DDR5RCD01 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation DDR5RCD01 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Mechanical Outline

Package options include a 240-ball Flip-Chip Fine-Pitch BGA (FCBGA) with 0.60 mm/0.70 mm ball pitch, 14 x 19 grid. The package has a number of depopulated balls. Package size is 8.70 mm x 13.50 mm as defined in MO-330 Issue A, Variation 10013.50x8.70-70x6030-240A[1]. The device pinout supports outputs on the top and outer left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way to match the corresponding pin location on the connector.

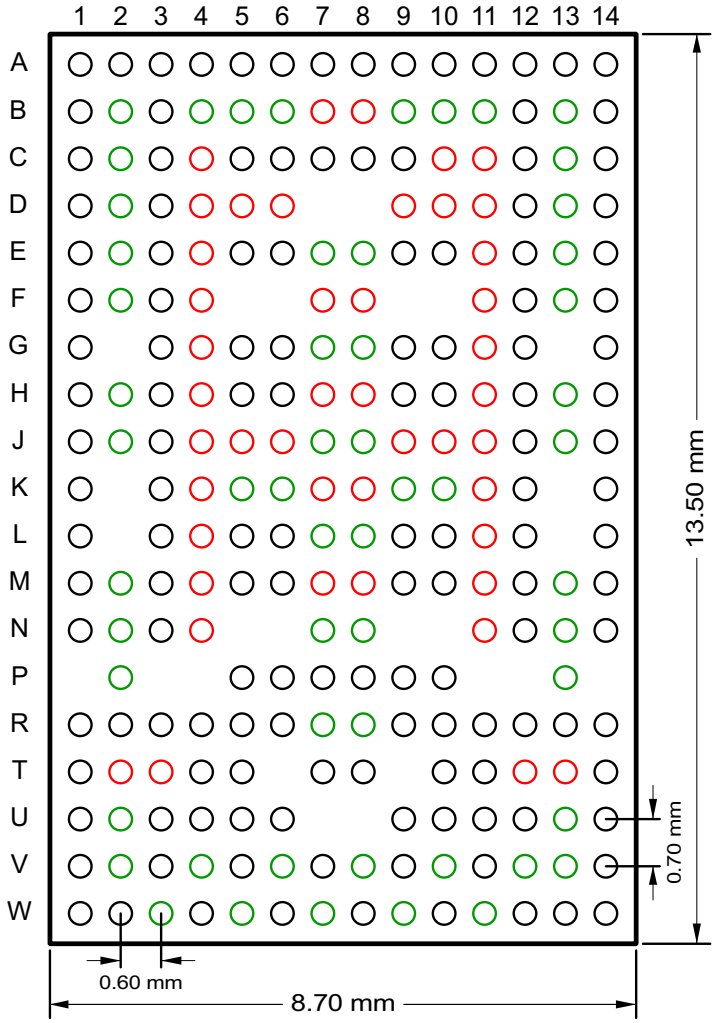


Figure 1 — Ball Configuration, TOP VIEW

Ball pitch: 0.60 mm x 0.70 mm, Size (ø 0.3 mm), SMD Pad SRO (ø 0.275 mm)
X-ray view from topside

1. This variation defines a maximum package thickness of 1.00 mm. The DDR5RCD01 must comply with a minimum thickness of 0.80 mm.

2.1 Pinout

Table 1 specifies the pinout for the DDR5RCD01.

Table 1 — Ball Assignment -240 ball FCBGA, 14 x 19 Grid, TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NU	QB CA7_A	QB CA3_A	QB CA13_A	QB CA11_A	QB CA12_A	QB CA10_A	QB CA10_B	QB CA12_B	QB CA11_B	QB CA13_B	QB CA3_B	QB CA7_B	NU	**A**
B	QB CA1_A	V_{SS}	QB CA9_A	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	QB CA9_B	V_{SS}	QB CA1_B	**B**
C	QB CA6_A	V_{SS}	QB CA8_A	V_{DD}	ZQ CAL	SCL	DERROR_IN_A_n	DERROR_IN_B_n	SDA	V_{DDIO}	V_{DD}	QB CA8_B	V_{SS}	QB CA6_B	**C**
D	QB CA5_A	V_{SS}	QB CA2_A	V_{DD}	V_{DD}	V_{DD}			V_{DD}	V_{DD}	V_{DD}	QB CA2_B	V_{SS}	QB CA5_B	**D**
E	QB CA0_A	V_{SS}	QB CA4_A	V_{DD}	QBCK_A_c	QBCK_A_t	V_{SS}	V_{SS}	QBCK_B_t	QBCK_B_c	V_{DD}	QB CA4_B	V_{SS}	QB CA0_B	**E**
F	QBCS0_A_n	V_{SS}	QBCS1_A_n	V_{DD}			V_{DD}	V_{DD}			V_{DD}	QBCS1_B_n	V_{SS}	QBCS0_B_n	**F**
G	QA CA11_A		QA CA13_A	V_{DD}	QDCK_A_c	QDCK_A_t	V_{SS}	V_{SS}	QDCK_B_t	QDCK_B_c	V_{DD}	QA CA13_B		QA CA11_B	**G**
H	QA CA9_A	V_{SS}	QA CA12_A	V_{DD}	**RFU**	**RFU**	V_{DD}	V_{DD}	**RFU**	**RFU**	V_{DD}	QA CA12_B	V_{SS}	QA CA9_B	**H**
J	QA CA10_A	V_{SS}	QA CA3_A	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	QA CA3_B	V_{SS}	QA CA10_B	**J**
K	QA CA6_A		QA CA7_A	V_{DD}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{DD}	QA CA7_B		QA CA6_B	**K**
L	QA CA1_A		QA CA4_A	V_{DD}	QA CA2_A	QA CA8_A	V_{SS}	V_{SS}	QA CA8_B	QA CA2_B	V_{DD}	QA CA4_B		QA CA1_B	**L**
M	QA CA5_A	V_{SS}	QA CA0_A	V_{DD}	QACK_A_c	QACK_A_t	V_{DD}	V_{DD}	QACK_B_t	QACK_B_c	V_{DD}	QA CA0_B	V_{SS}	QA CA5_B	**M**
N	QACS0_A_n	V_{SS}	QACS1_A_n	V_{DD}			V_{SS}	V_{SS}			V_{DD}	QACS1_B_n	V_{SS}	QACS0_B_n	**N**
P		V_{SS}			QCCK_A_c	QCCK_A_t	QLBD	QLBS	QCCK_B_t	QCCK_B_c			V_{SS}		**P**
R	**BCS_A_n**	**BCOM1_A**	**BCOM2_A**	**BRST_A_n**	**BCK_A_c**	**BCK_A_t**	V_{SS}	V_{SS}	**BCK_B_t**	**BCK_B_c**	**BRST_B_n**	**BCOM2_B**	**BCOM1_B**	**BCS_B_n**	**R**
T	**BCOM0_A**	V_{DD}	V_{DD}	DCS1_A_n	QRST_A_n		DCK_t	DCK_c		QRST_B_n	DCS0_B_n	V_{DD}	V_{DD}	**BCOM0_B**	**T**
U	DCA0_A	V_{SS}	DCS0_A_n	DLBD_A	DLBS_A	ALERT_n			DRST_n	DLBS_B	DLBD_B	DCS1_B_n	V_{SS}	DPAR_B	**U**
V	DCA1_A	V_{SS}	DCA3_A	V_{SS}	DPAR_A	V_{SS}	DCA6_A	V_{SS}	DCA1_B	V_{SS}	DCA3_B	V_{SS}	V_{SS}	DCA6_B	**V**
W	NU	DCA2_A	V_{SS}	DCA4_A	V_{SS}	DCA5_A	V_{SS}	DCA0_B	V_{SS}	DCA2_B	V_{SS}	DCA4_B	DCA5_B	NU	**W**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	

2.2 Terminal Functions

Table 2 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCS[1:0]_[B:A]_n	POD V_{REF} based	Chip Select inputs to the RCD. Two inputs per DRAM channel.
Input Address and Command bus	DCA[6:0]_[B:A]	POD V_{REF} based	Command/Address bus inputs to the RCD. Separate sets per channel.
Parity input	DPAR_[B:A]	POD V_{REF} based	Command Address input parity is received on the DPAR pin and should maintain even parity across the CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
Clock inputs	DCK_t/DCK_c	POD differential	Differential system clock input pair to the PLL. The clock is common to both RCD channels, CH_A and CH_B.
Loopback	DLBD_[B:A] DLBS_[B:A]	POD V_{REF} based	Loopback Inputs to RCD DLBD - loopback Data DLBS - loopback Strobe
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Error input	DERROR_IN_[B:A]_n	Low voltage swing POD input	DRAM CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. There is a separate signal per channel.
Data buffer control and communication outputs	BCS_[B:A]_n	POD	Data buffer chip selects. Indicate a valid command on the BCOM bus, and used to signal non-target termination. Separate per DRAM channel.
	BCOM[2:0]_[B:A]	POD	Data buffer command. The start of each command is signaled by an active chip select. Separate per DRAM channel.
	BRST_[B:A]_n	CMOS	Re-driven or CMD based reset. This is an asynchronous output. It is the responsibility of the RCD BRST to reset the DDR5 Data Buffer on all DIMM topologies.
	BCK_[B:A]_t BCK_[B:A]_c	POD differential	Differential clock output pair to the data buffer. Separate per DRAM channel.
Output Control bus	Q[B:A]CS[1:0]_[B:A]_n	POD	Chip Select signals to the DRAMs. 2 copies of each signal.
Output Address and Command bus	Q[B:A]CA[13:0]_[B:A]	POD	Command/Address bus outputs to the DRAMs, valid after the specified clock count and immediately following a rising edge of the clock. Two copies of each signal. When Output Inversion is enabled in RW00[5], Copy B output signals get inverted during all commands other than Deselect. Both copies drive High during idle cycles (i.e., Deselect).
Clock outputs	Q[D:A]CK_[B:A]_t Q[D:A]CK_[B:A]_c	POD differential	Clock outputs to the DRAMs. Four copies per channel.
Loopback	QLBD QLBS	POD	Loopback outputs to Host QLBD - loopback Data QLBS - loopback Strobe
Reset output	QRST_[B:A]_n	CMOS	Re-driven or CMD based reset. This is an asynchronous output. It is the responsibility of the RCD QRST_n to reset the DDR5 SDRAM on all DIMM topologies. The QRST outputs are asserted at power up. RCD requires MRW to independently de-assert to allow staggering of sub-channels.
Error out	ALERT_n	POD	When LOW, this output indicates that a parity error was identified associated with the CA inputs when parity checking is enabled or that the DERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not. One signal for the two channels.
SidebandBus pins[1]	SDA SCL	Open drain or push-pull I/O[2] CMOS input[3]	SidebandBus Data SidebandBus Clock
	V_{DDIO}	Power input	SidebandBus power input

Table 2 — Terminal functions

Signal Group	Signal Name	Type	Description
Miscellaneous pins	V_{DD}	Power Input	Power supply voltage
	V_{SS}	Ground Input	Ground
	ZQCAL	Reference	Reference pin for driver calibration
	NU	Mechanical ball	Do not connect on PCB
	RFU[3:0]	I/O	Reserved for future use pins, must be left floating on DIMM and in RCD

1. SA pins are not required for DDR5RCD01 as the address will be hard-coded. Refer to Section 7.5.1, “Target Address,” on page 78 for details.
2. SDA driver operation is dynamic. Depending on the SidebandBus mode of operation (I^2C RW25[5] = ‘0’ or I3C Basic RW25[5] = ‘1’), and even on the specific step (byte or bit) of a SidebandBus transaction packet, the SDA output driver can operate either in open-drain mode or push-pull mode.
3. These inputs are 1.0-V inputs.

Naming Convention:

Input Example:
DCAy_N - where ‘y’ is the signal number and ‘N’ is the sub-channel.

Output Example:
QxCAy_N - where ‘y’ is the signal number, ‘x’ is the output copy (A or B) and ‘N’ is the sub-channel.

3 Device Standard

3.1 Description

The DDR5RCD01 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels.

10 Electrical - Timing Requirements

10.1 Operating Electrical Characteristics

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 189 — Operating Electrical Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage[1]	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V
V_{DDIO}	DDR5RCD01 Sideband Interface I/O Supply Voltage		0.95	1.0	1.05	V
T_j	Junction temperature[2]		0	-	125	°C
T_{case}	Case temperature	Measurement procedure JESD51-2	-	-	103[3]	°C

1. DC bandwidth limited to 20 MHz.
2. For operation beyond Tj min and max datasheet values are not guaranteed and may de-rate. For operation above Tj max lifetime could be affected. All parametric measurements are performed at 0 °C, 25 °C and 95 °C.
3. This spec is meant to guarantee a Tj of 125 °C by the DDR5RCD01. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a DDR5RCD01 shall not be higher than 125 °C.